Electrical Characteristics of La_2O_3 gated MOS Capacitors with Different Wafer Orientation

H. Nakayama[1], K. Kakushima[2], P. Ahmet[1],
K. Tsutsui[2], N. Sugii[2], T. Hattori[1] and H. Iwai[1]

[1]Frontier Research Center, [2]Interdisciplinary Graduate School of Science, Tokyo Institute of Technology
4259, Nagatsuta, Midori-ku, Yokohama 226-8502, Japan
Tel: +81-45-924-5847, Fax: +81-45-924-5846
E-mail: nakayama.h.ab@m.titech.ac.jp

Abstract
The interface and annealing properties of La-silicate/Si interface have been investigated through fabrication of MOS capacitors on Si wafers with different orientations. A slight difference in EOT has been observed, where Si (100) has slightly reduced EOT with small interfacial layer thickness among other orientations. The interfacial state density of Si (100) has also been found to be smaller than other orientations.

Introduction
Aggressive scaling in MOSFET devices requires the introduction of metal/high-k gate stack [1-2]. To achieve an EOT of 0.5 nm, which is the ultimate specification reported in ITRS roadmap, high-k should be in directly contact with Si substrate without any SiO_2 based interfacial layer. It has been reported that rare earth oxides can achieve a direct contact structure by forming silicates at Si interface [3] and an EOT of 0.5 nm has already been demonstrated [4]. In this paper, we will focus on the interface properties of La-silicate/Si interface through fabrication of MOS capacitors on Si wafers with different orientations. The EOT growth after annealing and the chemical states of the formed silicate layer has been investigated by x-ray photoelectron spectroscopy (XPS).

Experimental Details
La_2O_3 with a thickness of 4 nm was deposited on Si (100), (110) and (111) by e-beam evaporation in an ultra-high vacuum chamber at a substrate temperature of 300 ^oC. A tungsten (W) metal with a thickness of 60 nm for electrical measurement and 8 nm for XPS measurement was *in situ* deposited by sputtering. The metal was patterned by reactive ion etching (RIE) with SF_6 chemistry to form gate electrodes. The samples were subjected to annealing at 500 ^oC for 30 min in a forming gas ambient (H_2:3%). For XPS measurement, a hard x-ray source of 7940 eV was used to collect the photoelectrons of Si 1*s* core level through 8-nm-thick metal gate [5].

Results
Fig. 1 shows the capacitance voltage (CV) characteristics of La_2O_3 gated MOS capacitors on different wafer orientations, where Si (100) has slightly small EOT than other orientations. In addition, bump in the CV curve, representing the interfacial state, was small with Si (100). The Si 1*s* spectra of the formed silicates are shown in fig. 2. The numbers of photoelectrons from silicates on Si (100) wafer was found to be slightly small, which is in good agreement with the obtained CV measurement.

Conclusions
MOS capacitors with La_2O_3 gate dielectric have been fabricated on Si substrates with different orientation. A slight difference in EOT has been observed, where Si (100) has slightly reduced EOT with small interfacial layer thickness among other orientations. The interfacial state density of Si (100) has also been found to be smaller than other orientations.

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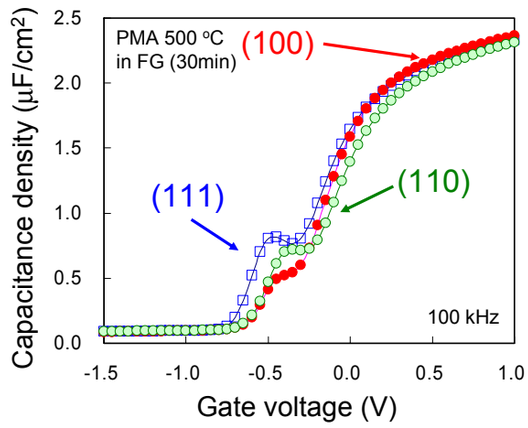

Figure 1 CV characteristics of La_2O_3 -gated MOS Capacitors on different wafer orientation after annealing at 500 ^oC

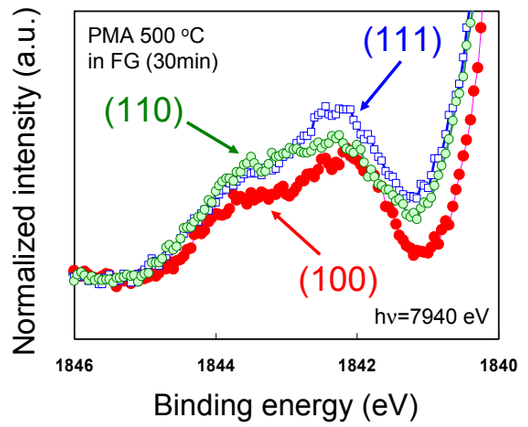

Figure 2 Normalization intensity of Si 1sLa-silicate measured by XPS.