Overwhelming the 0.5 nm EOT Level for CMOS Gate Dielectric

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Downsizing has been the most effective way to improve the performance of MOSFET. Among many important device parameters, gate oxide has faced to its scaling limit with SiO_2 based gate dielectric. Recently, this limit has been resolved with the introduction of high-k, which enables further reduction of the equivalent oxide thickness (EOT) [1]. It has been expected that performance improvement at an EOT beyond 0.5 nm may be difficult due to the presence of inversion layer capacitance [2], which is one of a quantum mechanical effect, underneath the gate dielectric as well as interfacial capacitance between the gate dielectric and metal electrode, both connected in series [3]. Therefore, one of the concerns is whether we could obtain any increase in drain drive current below an EOT of 0.5 nm. This paper deals with the scaling of EOT beyond 0.4 nm with the use of La_2O_3 gate dielectric and sufficiently large increase in drain current has been observed [4]. In addition, an efficient method to suppress the EOT growth of La_2O_3 film even with high temperature annealing is proposed to achieve an EOT below 0.5 nm.

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