

A roadmap for nano-CMOS

Hiroshi Iwai

Frontier Research Center
Tokyo Institute of Technology

4259-J2-68, Nagatsuta, Midori-ku, Yokohama,
Kanagawa, 226-8502, Japan

Tel: +81-45-924-5471, Fax: +81-45-924-5584
E-mail: iwai.h.aa@m.titech.ac.jp

The down-scaling is still the most important and effective way for achieving the high-performance logic CMOS operation with low power, regardless of its concern for the technological difficulties, and thus, the past shrinking trend of the gate-length has been very aggressive. In this paper, logic CMOS technology roadmap for '22 nm and beyond' is described with ITRS (International Technology Roadmap for Semiconductor) as a reference. In the ITRS 2008 Update published just recently, there has been some significant change in the trend of the gate length. The future gate-length shrinking trend predicted in the past several versions of the ITRS has been too aggressive even for the most advanced semiconductor companies to catch up, and thus, the predicted trend has been amended to be less aggressive from the ITRS 2008 Update, resulting in the delay in the gate-length shrinkage for 3 years in the short term and 5 years in the long term from those predicted in ITRS 2007. Corresponding to this, the pace of the introduction of new technologies becomes slower. For the long term, the limit of the downsizing is a big concern. The limit is expected to be at the gate length of around 5 nm because of the too huge off-leakage current in the entire chip. Until that we will have probably six more generations or 'technology nodes', considering that we are now in the so-called 45 nm generation. It would take probably 20–30 years until we reach the final limit, because the duration between the generations will become longer when approach-ing the limit. In order to suppress the off-leakage current, double gate (DG) or fin-FET type MOSFETs are the most promising. Then, it is a natural extension for DG FETs to evolve to Si-nanowire MOSFETs as the ultimate structure of transistors for CMOS circuit applications. Si-nanowire FETs are more attractive than the conventional DG FETs because of higher on-current conduction due to their quantum nature and also because of their adoptability for high-density integration including that of 3D. Then, what will come next after reaching the final limit of the downsizing? The answer is new algorithm. In the latter half of this century, the application of algorithm used for the natural bio system such as the brains of insects and even human will make the integrated circuits operation tremendously high efficiency. Much higher performance with ultimately low power consumption will be realized.