Electrical Properties of Lanthanum-scandate Gate Dielectric Directly Deposited on Ge

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Introduction

Germanium is regaining considerable attention because of its inherent high bulk carrier mobility, which can provide solutions for major obstacles that state-of-the-art Si technology is facing for advanced CMOS devices with high-k gate insulators. As known, the Ge CMOS technology having native Ge oxide as a gate insulator appears to be detrimental because of its poor thermo-dynamic and electrical properties and the resulting interface with Ge. Therefore, deposition of a non-native insulator appears to be only possible way to realize Ge-based MOS devices of acceptable quality. Recently, rare-earth scandates ($ReScO_x$, Re being Y, La or a lanthanide) have drawn much attention as a promising high-k candidate since it can provide higher band-offsets as well as higher k values while it maintains amorphous phase over a wide temperature range [1-2]. In this study, we report for the first time the electrical characteristics of $LaScO_x$ with various ScO concentrations directly deposited on Ge.

Experimental details

The (100) oriented n-type Ge wafers with a resistivity of 0.1-1.0 Ω-cm were used as the starting substrate in this experiment. After the chemical treatment with $NH_4OH:H_2O_2:H_2O$ (1:2:20) solutions followed by cyclic HF (1%) dip with rinsing in de-ionized water, the Ge wafers were then transferred into the MBE chamber to perform *in-situ* high-vacuum (~10^{-9} Torr) anneal at 550°C in order to remove the remaining native oxides of Ge. Thereafter, ultrathin $LaScO_x$ (~8nm) films were deposited on Ge by e-beam evaporation under the pressure of ~$2x10^{-8}$Torr at room temperature. Tungsten (W) gate-electrodes were deposited *in-situ* to avoid any moisture absorption or carbon-related surface contamination from the ambient. Ge p-MOSFETs were fabricated following conventional gate-first self-aligned process.

Results and discussion

The high-frequency (1 MHz) C-V characteristics of $LaScO_x$ with three different ScO concentrations in the range from 40-70% are shown in Fig. 1a. The tendency of flat-band voltage (V_{fb}) shift towards its lower values with increasing ScO concentrations are being observed in general irrespective of PMA ambient (N_2 and FG in this case) even though considering hysteresis. It has also been noticed that inversion capacitance increases with increasing ScO concentration. Meanwhile, the energy distribution of interface state density, D_{it} extracted following the conductance method is shown in Fig. 1b. Indeed, a moderate D_{it} values usually observed for Ge devices are being obtained while 50% ScO concentrated sample exhibit the lowest value (~$8x10^{12}$ $eV^{-1}cm^{-2}$). The frequency dispersion in C-V hysteresis of $LaScO_x$ with 50% ScO is shown in Fig. 2a. Although, well- behaved C-V stretch-out behaviors have been observed along with small humps that emerged in the depletion and week inversion regimes arising likely due to slow interface states, however, significant hysteresis are noticed possibly due to re-growth of GeO_x after PMA at the $LaScO_x$/Ge interface [3]. In fact, an increase in hysteresis with rising annealing temperature along with increasing ScO concentrations are being observed for PMA samples which is anticipated as a result of more pronounce intermixing or Ge out-diffusion into $LaScO_x$. However, it is worth mentioning here that PDA samples treated in FG or N_2+O_2(5%) ambient demonstrates slightly higher hysteresis compare to PMA samples treated in FG or N_2 ambient. Another noticeable phenomenon is the significant frequency dispersion in the strong inversion region, which is consistent with a high intrinsic carrier concentration and a large density of bulk traps close to the midgap in Ge; consequently, a fast accumulation of minority carriers could occur at Ge surface. Nevertheless, a drastic improvement over hysteresis can be achieved by incorporating an ultrathin Si IPL (see Fig. 2b). Figure 3 shows the measured I_{ds}-V_{ds} characteristics of Ge p-MOSFET with 50% ScO concentrated $LaScO_x$. In fact, reasonable output characteristics have been observed.

Conclusion

In summary, the electrical properties of $LaScO_x$ directly deposited on Ge have been investigated. It has been demonstrated that higher ScO concentration in $LaScO_x$ may cause lower V_{fb} shift while it introduces larger hysteresis. This work suggests that 50% ScO concentration along with PMA treatment at 500°C will be the key to ensure reasonable electrical performance for $LaScO_x$ directly deposited on Ge.

Acknowledgement

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References

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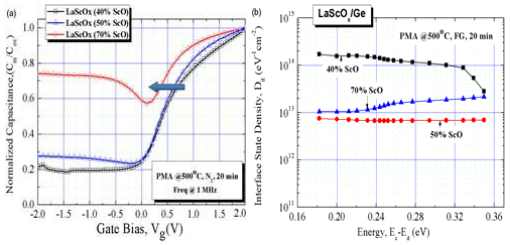

Fig. 1: (a) High-frequency (1 MHz) C-V characteristics and (b) energy distribution of interface state density of $LaScO_x$ on Ge with several ScO concentrations along with various annealing ambient.

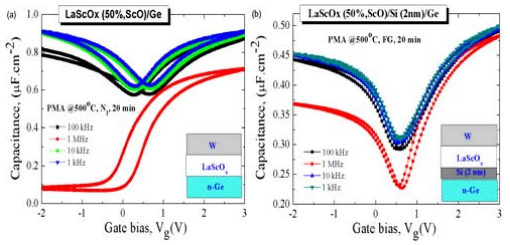

Fig. 2: C-V hysteresis characteristics of W/$LaScO_x$ (50% ScO)/Ge MISCAPs (a) without and (b) with Si IPL.

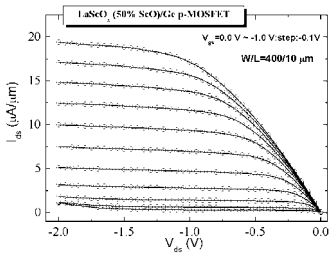

Fig. 3: Measured I_{ds}-V_{ds} characteristics of Ge p-MOSFET with 50% ScO concentrated $LaScO_x$.