2009 Master thesis

Performance Improvement of Sub-1nm EOT MOSFET

- Selection of Metal/high-k Materials for Effective Oxygen Control -

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Chapter1. Introduction

1.1. Scaling of MOSFET with SiO_2

Since the invention of the bipolar transistor in 1947, there has been unprecedented growth of the semiconductor industry, with an enormous impact on the way people work and live [1]. Now the basic and fundamental building-block of modern silicon technology in current ultra-large-scale integration (ULSI) integrated circuits (ICs), the metal-oxide-semiconductor field-effective transistor (MOSFET). A schematic cross section of modern CMOS transistors, consisting of an n-channel MOSFET and p-channel MOSFET integrated on the same chip, is shown in figure 1.1. In the electrical design of modern CMOS transistor, the power-supply voltage is reduced with the physical dimension in some coordinated manner. A great deal of design detail goes into determining the channel length, or separation between the source and drain, accurately, maximizing the on current of the transistor while maintaining an adequately low off current, minimizing variation of the transistor characteristics with process tolerances, and minimizing the parasitic resistances and parasitic capacitances [1]. To make circuit speed up, devices dimensions and the power-supply voltage must be scaled down. Figure 1.2 shows the schematic model of MOSFET constant-electric-field scaling. In Si technology, SiO_2 has important roll, such as dielectric film of MOS structure and shallow-trench isolation (STI). Especially gate dielectric SiO_2 was the key to determine electrical performance. According to Moore's low, SiO_2 gate film has become thin, however extremely thin gate oxide has large leakage current cased by direct-tunneling current. Now the thickness of SiO_2 reached sub-1nm. This thickness corresponds to 3 layers of atoms (fig. 1.3). The thickness of gate oxide and other physical sizes are

downsized along with ITRS roadmap, from this roadmap, Equivalent oxide thickness (EOT) was required to be reduced to 0.5 nm in near future [2] (fig. 1.4). Figure 1.5 shows

$J_{g\ limit}$ vs. simulated gate leakage current density for SiON gate dielectric plot, SiON has higher dielectric constant than that of SiO_2 and often used as gate oxide instead of traditional SiO_2 gate oxide. As you can see, simulated gate leakage current become larger than the limit of J_g in 2009. So, new materials for gate oxide, gate metal, and substrate and new structure MOS devices are eagerly studied.

Aggressive scaling of MOSFET devices requires a metal gate/high-k gate stacks to overcome the excess leakage problem [3-4]. High-k materials has larger dielectric constant than that of SiO_2 (= 3.9). So, with high-k gate dielectric, we can fabricate small EOT transistor keeping gate oxide physical thickness relatively large and reduce direct-tunneling current. Now, high-k materials are extensively studied, but there are a lot of obstacles to overcome. One of these problems is that interface quality of high-k/Si-substrate is worse than that of SiO_2/Si, bad quality interface can not compensate MOSFET high performance.

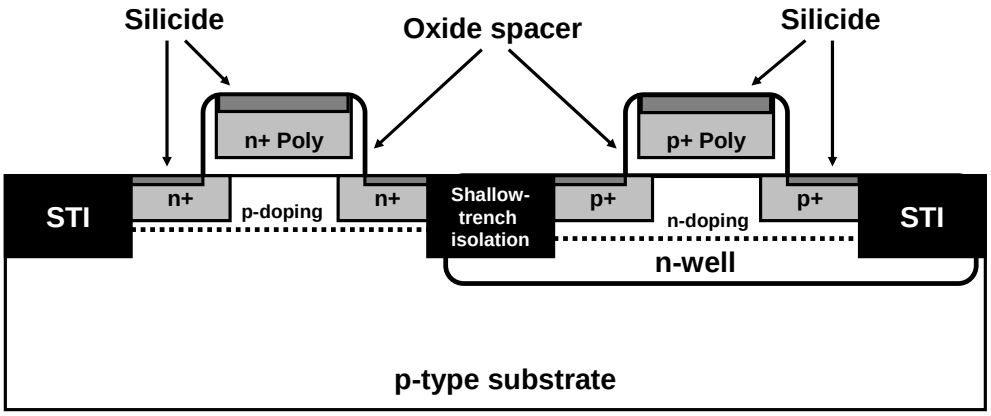

Figure 1.1 Schematic device cross section for an advanced CMOS technology.

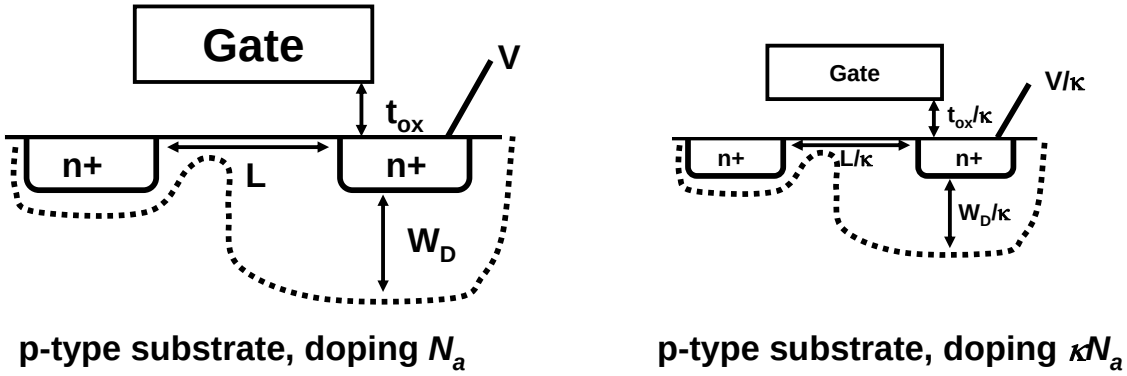

Figure 1.2 Principles of MOSFET constant-electric-field scaling. Thanks to aggressive scaling of MOSFET the circuit speed becomes high.

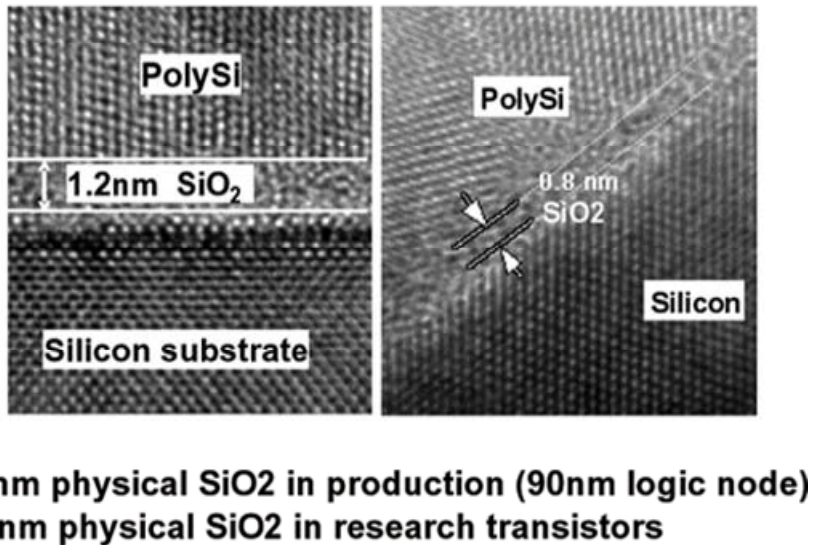

Figure 1.3 Cross sectional TEM image of MOS structure; the thickness of SiO_2 becomes as thin as 0.8 nm.

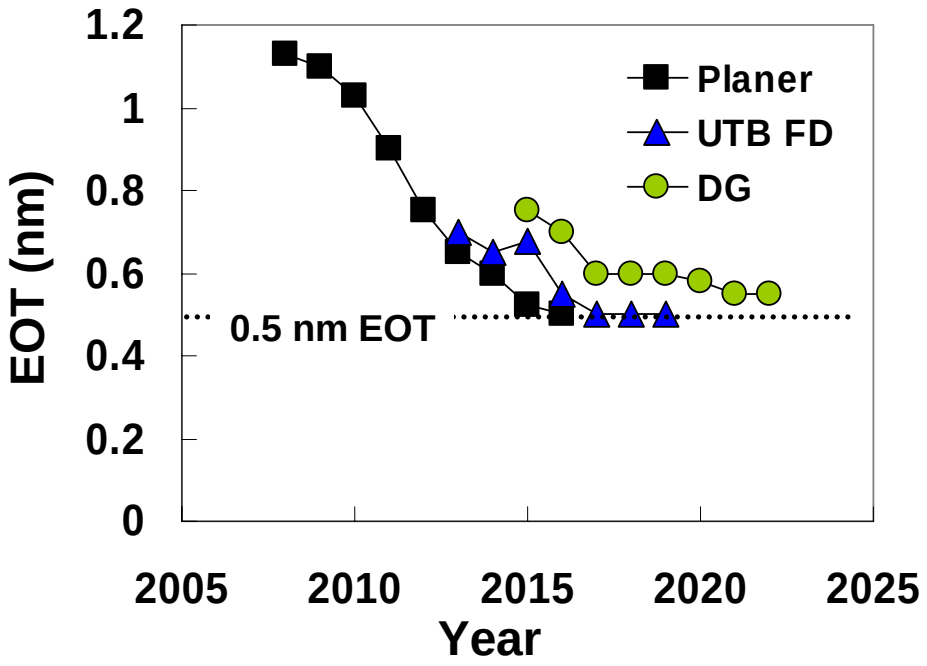

Figure 1.4 EOT scaling road map of various structures MOS transistors (ITRS2008).

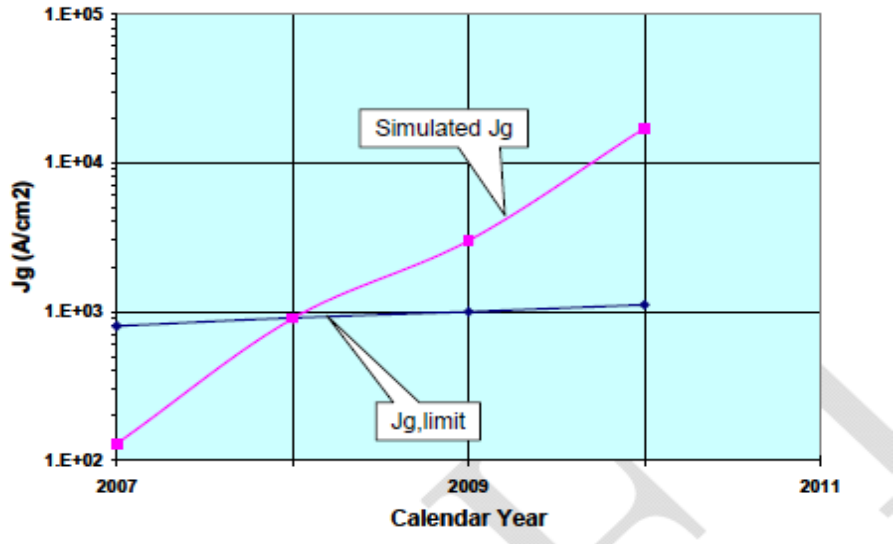

Figure 1.5 High performance Logic (HPL); $J_{g\ limit}$ vs. simulated gate leakage current density for SiON gate dielectric. Simulated gate leakage current become larger than the limit of J_g in 2009.

1.2. Introduction of high-k materials for gate insulator

In CMOS technology, SiO_2 has been used as gate dielectric for more than 30 years. However, recent downsizing has made gate leakage current extremely large. Now we must find alternative materials for gate oxide, high-k materials which has larger relative dielectric constant introduction is effective materials for further scaling. There are many high-k materials studied for gate oxide such as HfO_2, La_2O_3 and so on. When we select high-k materials, a value of dielectric constant and band gap are important factor. Figure 1.6 shows band gap vs. dielectric constant plot [5]. Generally speaking, dielectric constant decreases as the band gap increases. Considering that high-k materials are introduced mainly because of excess leakage problem, too narrow band gap materials such as TiO_2 are not suitable for gate oxide. Recent research shows that HfO_2 based materials with SiO_2 interfacial layer stacks have been one of the promising candidates thanks to their high dielectric constant and relatively high thermal endurance. As shown in fig. 1.6, HfO_2 is mid-gap material and has relatively high dielectric constant (< 23). La_2O_3 is also expecting material thanks to its advantage for leakage current, EOT of 0.3 nm gate stacks with $LaAlO_3$/Si [6] was reported. In this study, we mainly used HfO_2 and La_2O_3 mainly because of their advantage shown above. Figure 1.7 shows a recent trend of high-k reports which had been reported in VLSI symposium and IEDM symposium. As we can see, Hf-base materials such as HfSiO(N), HfLaO(N) and HfO_2 were studied eagerly. Especially, Hf-based materials occupies majority of all the reports in 2006.

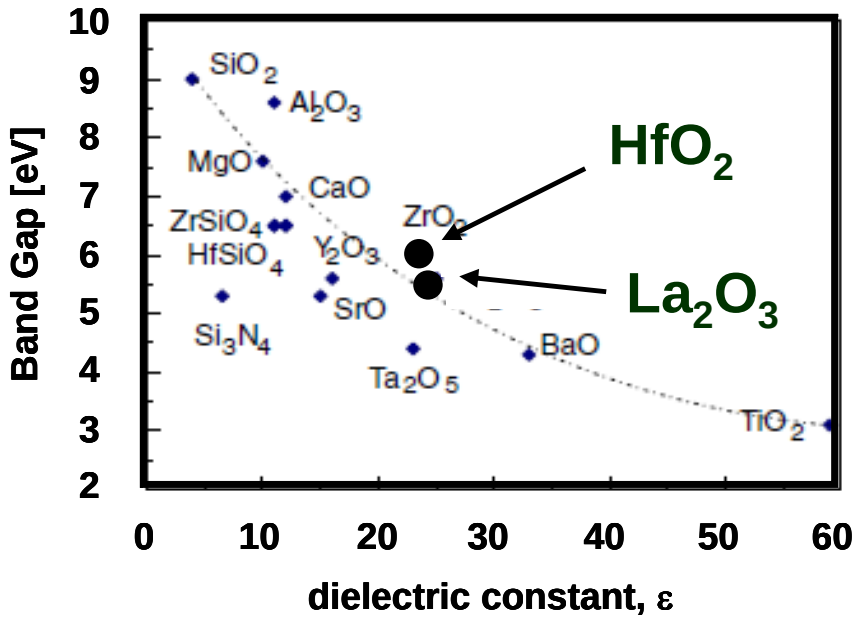

Figure 1.6 Band gap vs. dielectric constant plot of various high-k materials studied for gate insulator.

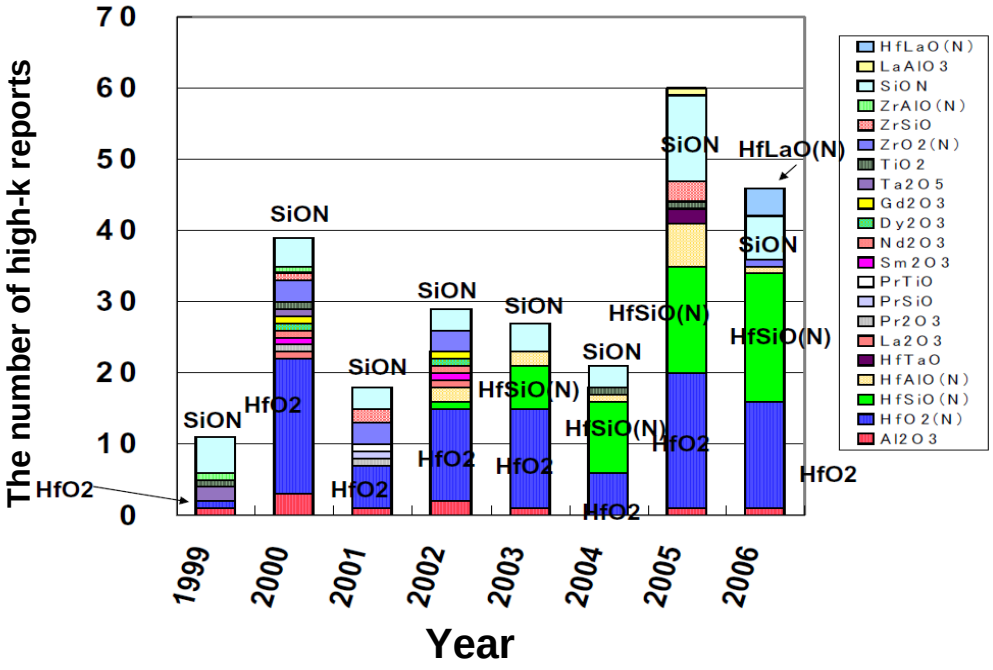

Figure 1.7 Recent trend of high-k reports which had been reported in VLSI symposium and IEDM symposium.

In leakage current, high-k materials shows advantage compared with that of SiO_2(N) (fig. 1.8). However, high-k MOSFET has large obstacles to overcome though eager study for high-k has been continued. For example difficulty in controlling threshold voltage and thermal endurance carrier mobility problems were one of the main issues of high-k MOSFET. In HfO_2 gate stacks, we could not control V_{th} enough. Figure 1.9 shows the schematic illustration of work function error by introduction of high-k insulators, gate metal n^+ poly-Si and gate metal p^+ poly-Si are on SiO_2 and HfO_2 gate dielectric. When gate metals are deposited on SiO_2, each metal has n-metal and p-metal work functions, however on HfO_2 both gate electrodes show mid-metal work function. This effect is called fermi-level-pinning (FLP) and FLP causes V_{th} for n-MOSFET increase. One solution is that metal gate electrode is introduced to avoid FLP. There are many candidates for metal gate, pure metal, metal nitride and full silicide (FUSI). We have to select these candidates carefully taking it account to controlling V_{th} and thermal endurance. And another way to overcome the difficulty in controlling V_{th} is selection of highi-k materials. Figure 1.10 shows electron mobility vs. V_{th} plot of n-MOSFET [7]. Electron mobility and V_{th} changed widely by capping various rare metals such as La and Sc on HfSiON. Recently, the origin of this V_{th} change by incorporating another high-k revealed to be the dipoles which exist at the interface of high-k/Si-substrate and high-k/SiO_2 [8-9]. And these dipoles also have the effect on electron mobility [9]. So, we have to select both gate metal and high-k insulators which can achieve low V_{th}, high thermal endurance and high mobility.

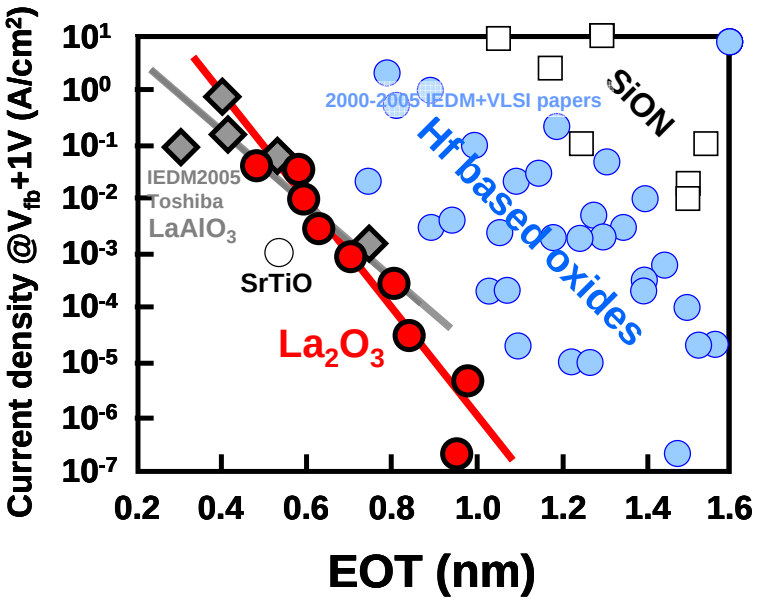

Figure 1.8 Leakage current of various high-k materials. Hf-based materials and La_2O_3 had smaller leakage current compared with SiON.

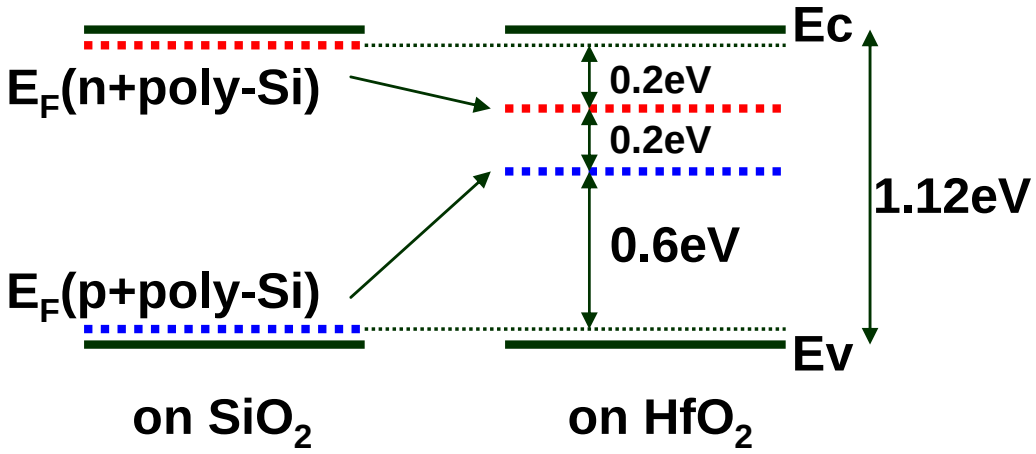

Figure 1.9 Fermi-level-pinning; In HfO_2 devices, work function control is difficult compared with SiO_2.

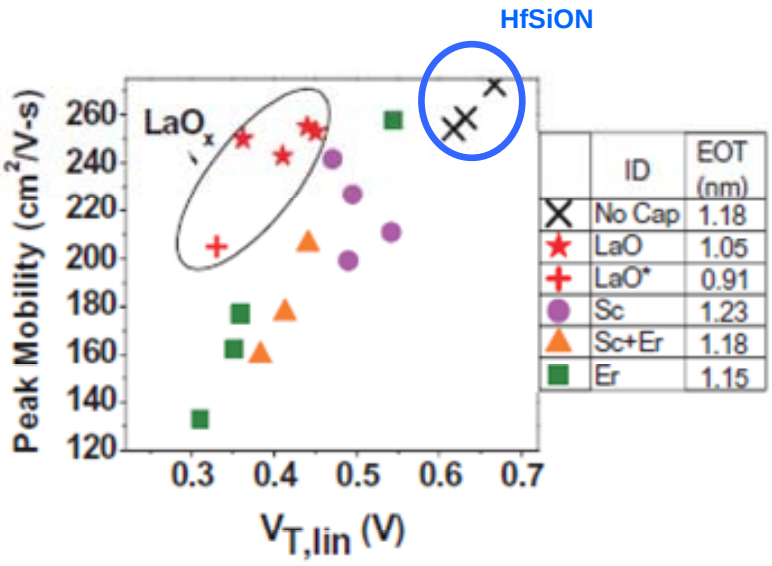

Figure 1.10 Electron mobility vs. V_{th} plot; Electron mobility and V_{th} changed widely by capping various rare metals on HfSiON.

There are many high-k materials which are studied for gate oxides, Hf-based materials are one of the most promising high-k materials thanks to their high dielectric constant and relatively high thermal endurance. Popular structure of Hf-based materials is shown in fig. 1.11 [10], to realize good interface quality SiO(N) interfacial layer (IL) was inserted at the Si interface. However, to achieve 0.5 nm EOT which is the ultimate specification in ITRS roadmap, high-k should be directly contacted on Si substrate and SiO_2 IL should be removed. Indeed 0.5 nm EOT gate stack with HfSiO(N)/Si [11] without IL was reported, the number of reports which study sub-0.5 nm gate stack has not been enough. Figure 1.12 shows 0.5 nm MOS structure reported in IEDM 2007 [11]. This MOS structure realized high-k/Si directly contacted interface, however fabrication process of this MOS transistor was complex. In addition, Hf-based materials have large

V_{th} even n-metals are used as gate metal, so especially for n-MOSFET, proper choice of gate metal has been eagerly studied. Recent research shows that not only gate metal choice but also high-k choice is the key to realize low V_{th} n-MOSFET. Rare earth oxides such as La_2O_3, Sc_2O_3 are remarked because they could reduce high V_{th} as shown in fig.1.10.

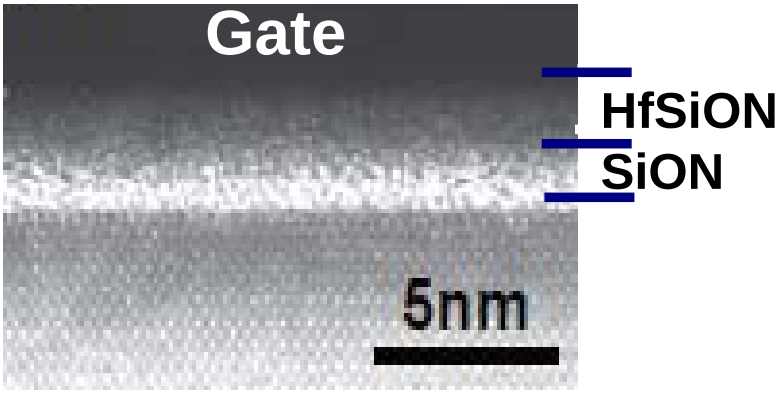

Figure 1.11 Hf-based MOS structure [10]; To realize good interface quality SiO(N) interfacial layer (IL) was inserted at the Si interface.

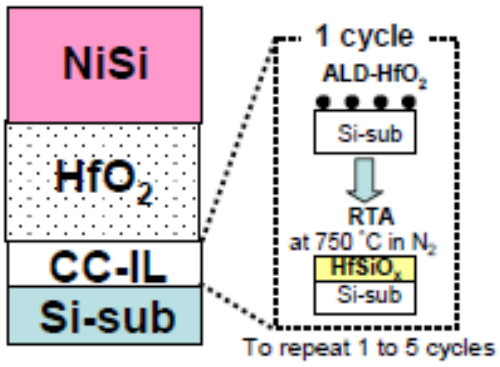

Figure 1.12 0.5 nm MOS structure reported in IEDM 2007 [11]; high-k/Si directly contacted interface could be realized.

La based materials are also remarked for next generation gate oxide thanks to its advantage of leakage current, which means that La based materials can realize smaller EOT. Figure 1.13 shows the MOS structure with $LaAlO_3$ which achieve 0.3 nm EOT in gate last process [12]. In addition, La_2O_3 can reduce MOSFET V_{th} by incorporating to Hf based materials [7]. So, La-based materials are used mainly for n-MOSFET.

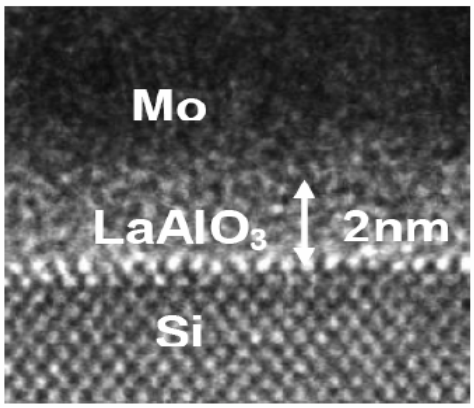

Figure 1.13 0.3 nm EOT MOS structure with $LaAlO_3$ which was reported in IEDM 2005 [12].

1.3. Selection of gate electrode for Metal/high-k MOSFET

Gate electrode selection also has large impact on MOSFET electrical characteristics such as V_{th} and thermal endurance. Figure1.14 shows gate insulator, electrode transition. In modern CMOS technology, double Poly-Si (N+/P+) are used as gate electrode, but double metal gate is needed for further scaling with high-k because in small EOT region, depletion capacitance of poly-Si can not be negligible.

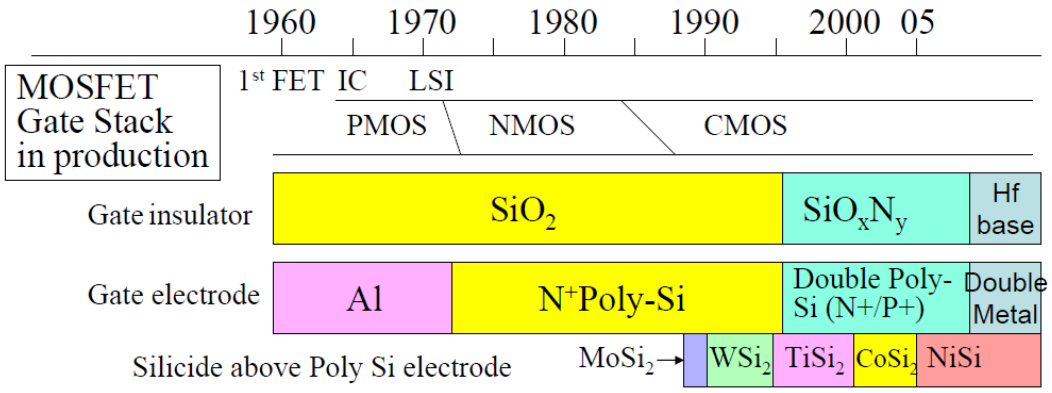

Figure 1.14 Gate insulator, electrode transition from 1960 to the future.

In this study, we mainly focused on thermal endurance change by gate metal choice. Recent study shows that full-silicide gate electrode (FUSI) and metal-nitride gate are used because they have good thermal stability. Figure 1.15 shows annealing temperature vs. EOT plot of 2 type gate electrodes. As you see, TaN gate has better thermal stability

compared with Ta gate [13] after high temperature annealing. So, to achieve 0.5 nm EOT even after annealing, proper gate metal selection is needed.

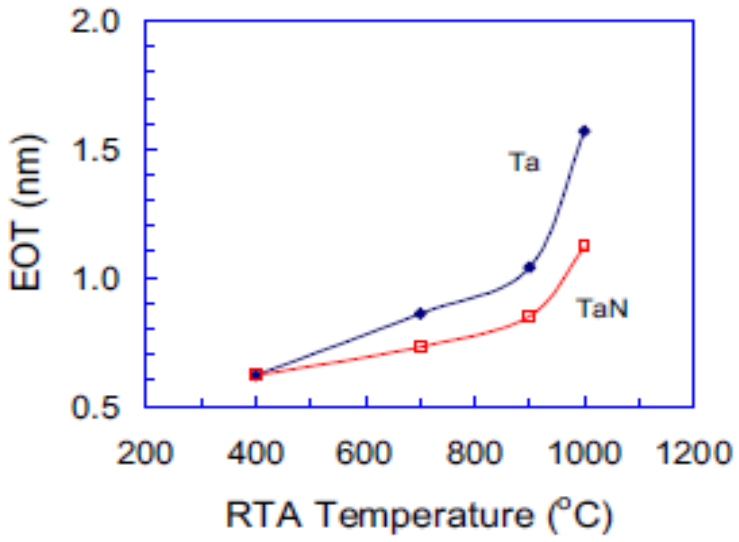

Figure 1.15 Annealing temperature vs. EOT plot of 2 type gate electrodes, Ta and TaN [13].

1.4. Purpose of this study

The main purpose of this study is to find gate metals and gate insulators which can achieve 0.5 nm EOT n-channel MOS transistor in the gate-last-process and fabricate sub-1nm EOT MOSFET to examine its electrical characteristics. In sub-1nm region, nMOSFET has large leakage ate current (J_g) even with high-k materials and carrier mobility (μ_{eff}) degradation along with EOT scaling is serious problem. I measured J_g and μ_{eff} to compare these parameters in different gate structures with various metals and high-k materials.

For this purpose, various structures of MOS capacitors and MOSFETs using HfO_2, La_2O_3, CeO_2 and SrO as gate oxide and $TaSi_2$ and W as gate electrode were fabricated (shown in figure 1.16).

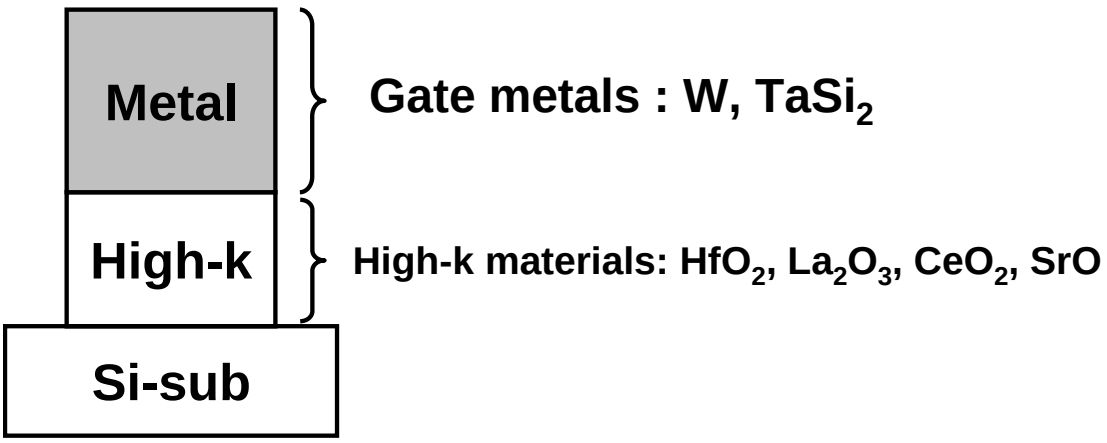

Figure 1.16 MOS structure in this study. Various materials were used for 0.5 nm EOT MOSFET.

1.5. References

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Chapter 2. Fabrication and Characterization Method

2.1. Introduction

In this chapter, detailed fabrication steps on MOS capacitors (MOSCAPs) and MOSFETs will be discussed. The principles of measurement and the experiment instruments such as electron beam epitaxy and RF sputtering are also shown.

2.2. Fabrication Procedure for MOS Capacitors

Figure 2.1 shows the fabrication process flow of high-k gated MOS capacitors. High-k dielectrics were deposited on a 300-nm-thick SiO_2 isolated n-Si(100) wafer with thermally grown interfacial oxide layer (IL) with a thickness of 3.5 nm. HfO_2 and La_2O_3 were deposited by electron beam evaporation. Substrate temperature during depositing was set to 300 ^oC and the deposition rate of high-k was controlled to be 0.3 nm/min. After high-k deposition, 60 nm-thick tungsten (W) was *in-situ* deposited using sputtering without exposing the wafers to air in order to avoid any moisture or carbon-related contamination absorption. W was patterned by reactive ion etching (RIE) using SF_6 chemistry to form gate electrode for MOS capacitors. Wafers were then post-metallization annealed (PMA) using a rapid thermal annealing (RTA) furnace in forming gas (F.G) (N_2:H_2=97%:3%) ambient at 420 ^oC for 30 min. Backside Al was deposited as a bottom electrode by thermal evaporation. Capacitance-voltage (C-V) characteristics of MOS capacitors were measured at 100 kHz and 1 MHz using Agilent 4284A precision LCR meter. The thickness of IL is chosen to be sufficient to avoid any

formation of oxygen vacancy in high-k. Moreover, as the annealing temperature studied in this work is below 500 ^{o}C, the Fermi level pining effect on V_{fb} can be neglected.

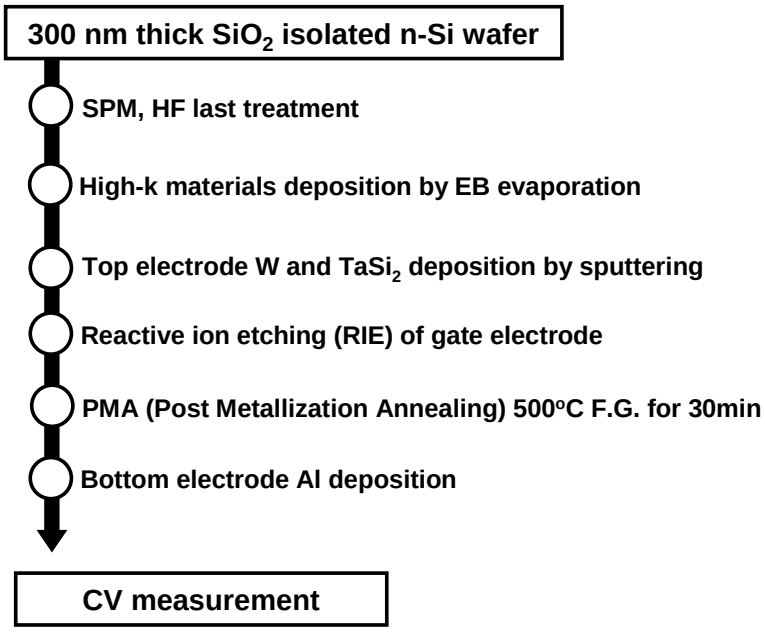

Figure 2.1 Fabrication process flow of high-k gated MOS capacitors

2.3. Fabrication Procedure for n-channel MOSFET

For nMOSFET, p-Si(100) with LOCOS isolated wafers with source/drain pre-formed substrates were used (shown in fig. 2.2). No IL was intentionally formed before high-k deposition. HfO_2 and La_2O_3 were deposited in the same way as the MOS capacitors. For MOSFET, the annealing temperature was set to 500 ^{o}C. The process flow is shown in fig. 2.2. The electrical characteristics of the fabricated high-k gated MOSFETs were

measured using Agilent 4156C semiconductor parameter analyzer. The fabricated transistor was shown in fig. 2.4.

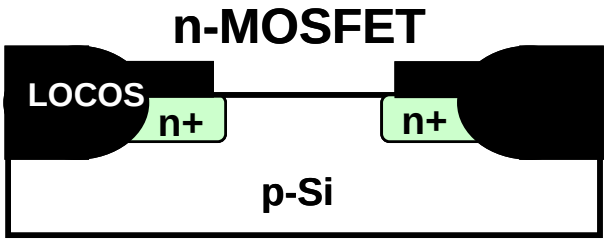

Figure 2.2 MOSFET substrate before cleaning; the substrate was LOCOS isolated and S/D pre doped.

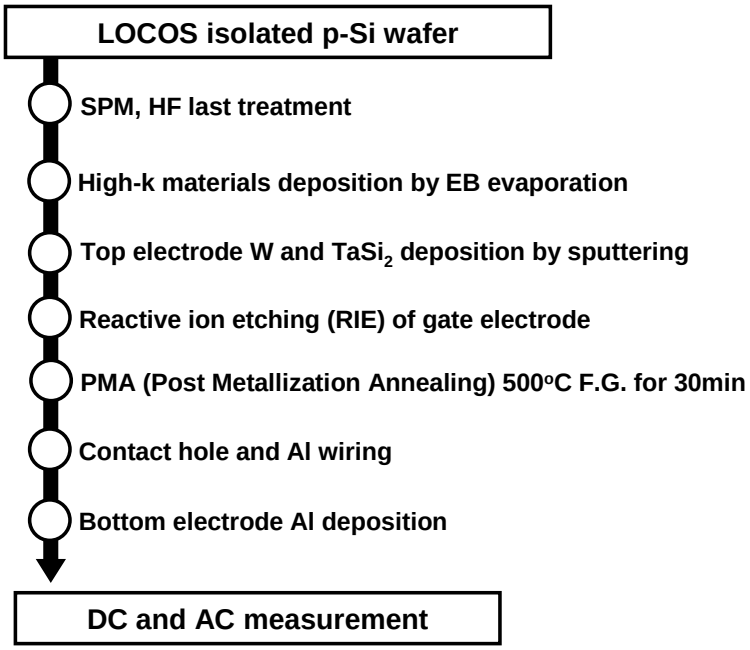

Figure 2.3 Fabrication process flow of high-k gated n-channel MOSFET.

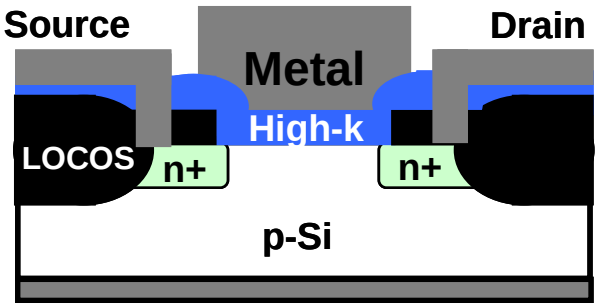

Figure 2.4 Fabricated n-channel MOSFET; in this study, gate length (L) and gate width (W) are 2.5 μm and 50 μm each.

2.4. Instrument used in Fabrication Process

2.4.1. Wet Cleaning

For deposition of thin film maintaining the quality requires quite clean surface of Si substrate. There are many method of cleaning substrate. But one of the most used methods is wet cleaning by chemical liquid. There are some kinds of the liquids which are used in wet cleaning process shown in Table 2.1. And these liquid have each effect against substrate pollutions. So, one liquid can't eliminate all pollutions. In this Study, I used the process like fig.2.5. First step is SPM Cleaning (H_2SO_4:H_2O_2:H_2O=4 : 1) eliminates metal and organic materials. And then, the native or chemical oxide was removed by diluted hydrofluoric acid (H_2O_2:H_2O=1:100).

Table 2.1 Main Cleaning Process

The name of Cleaning	Chemical liquid	The Characteristic
APM Cleaning	**$NH_4OH/H_2O_2/H_2O$**	**The effect of elimination against organic materials and particles**
FPM Cleaning	**$HF/H_2O_2/H_2O$**	**The effect of elimination against metal and oxidation layer**
HPM Cleaning	**$HCl/H_2O_2/H_2O$**	**The effect of elimination against metal**
SPM Cleaning	**H_2SO_4/H_2O_2**	**The effect of elimination against metal and organic materials**
DHF Cleaning	**H_2O_2/H_2O**	**The effect of elimination against metal and oxidation layer**
BHF Cleaning	**$HF/NH_4F/H_2O$**	**The effect of elimination against oxidation layer**

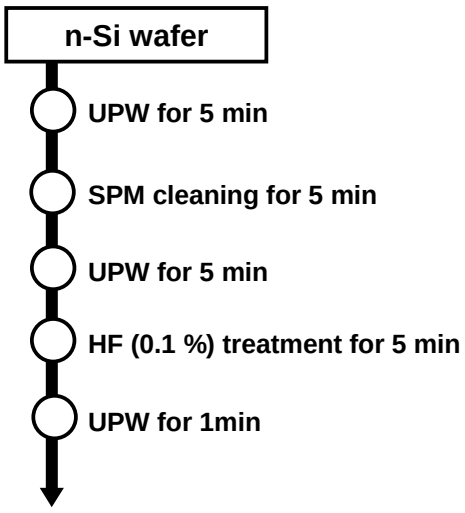

Figure 2.5 Wet cleaning process of MOS capacitors and MOS transistors used in this study

2.4.2. Molecular Beam Epitaxy (MBE)

As discussed and reported in various literatures, there are many ways to deposit high-k dielectric films on Si substrate. Various deposition methods have been proposed. These include MOCVD, LPCVD, ALD, PLD and e-beam evaporation. In this study, e-beam evaporation method was adopted. High-k materials were deposited in ultra high vacuum chamber as shown in figure 2.6. There are four compartments to allocate same/difference solid sources at the bottom of the chamber. HfO_2 and La_2O_3 were placed there and subsequently heated by the e-beam which was located near the each high-k source. The electron beam was controlled by a magnetic sweep controller, and the power of the beam is set to be 5 kV. The base pressure inside growth chamber is maintained at 10^{-8} Pa by TMP, when high-k was deposited the pressure inside the chamber increased to 10^{-7} Pa. Then, since the chamber is maintained at the ultra high vacuum state, the La_2O_3 molecule begins to evaporate when the temperature is reported as 3620 ^{o}C. In deposition, the physical thickness of each high-k film was measured by crystal oscillator and the sample folder was rotated. Deposition rate was set to be 0.3 nm/s, the rate was important for the film quality. Too fast deposition rate made the quality worse than slow deposition rate.

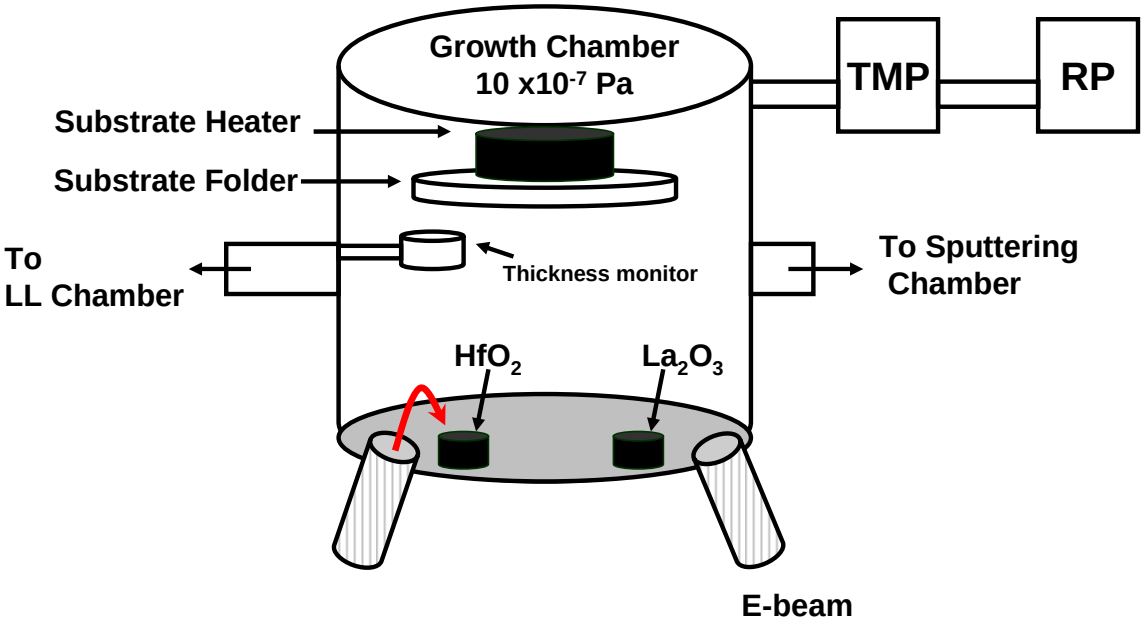

Figure 2.6 Schematic model of molecular beam epitaxy (MBE)

2.4.3. RF Sputtering

In this experiment, gate metals W and $TaSi_2$ were deposited using RF sputtering. The base pressure of sputtering chamber was maintained to be 10^{-7} Pa by TRP and RP (shown in Fig.2.7). In sputtering, Ar was flowed into the chamber and the pressure of which was set to be 10^{-4} Pa, the AC current power was 150W.

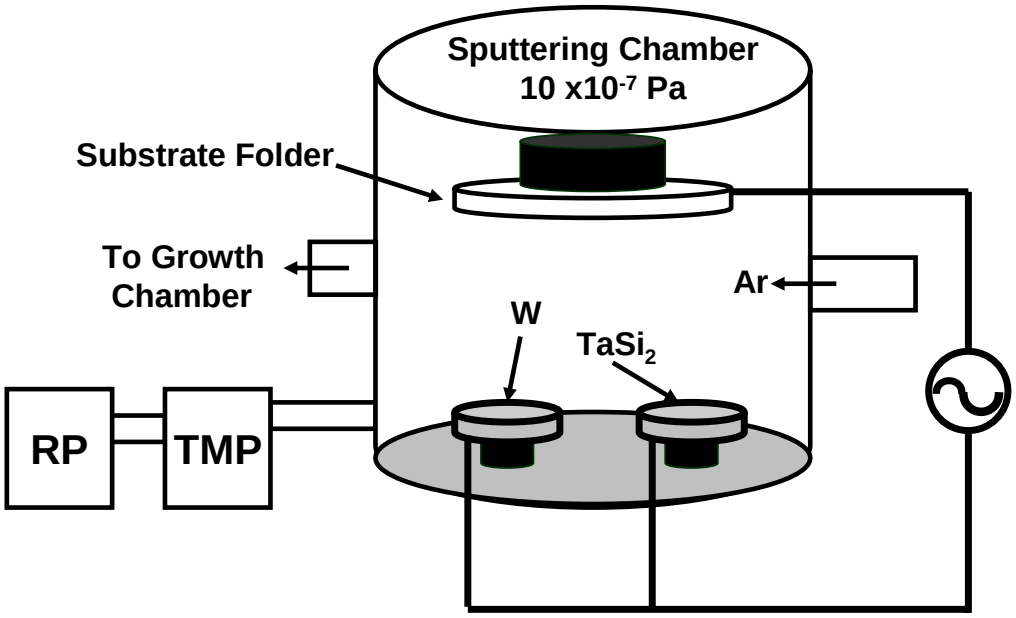

Figure 2.7 Schematic model of RF Sputtering

2.4.4. Reactive Ion Etching (RIE)

Reactive Ion Etching (RIE) which uses one of chemical reactive plasma to remove materials deposited on wafers was adopted to etch gate electrode in this study. There are two electrodes in vacuum chamber (shown in fig. 2.8). One is usually connected to ground and gas is put into the chamber and exits to the pump, in this study SF_6 and O_2 are used to remove gate W, $TaSi_2$ and resist each. And plasma is generated and ion direct for substrate and remove gate electrode and resist chemically.

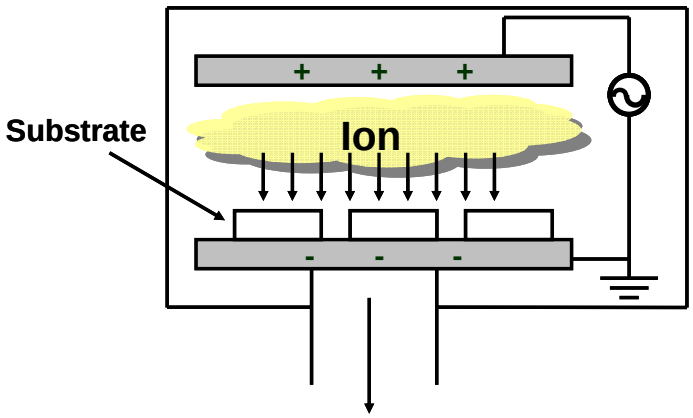

Figure 2.8 Schematic illustration of Reactive Ion Etching (RIE).

2.4.5. Rapid Thermal Annealing (RTA)

Thermal annealing processes are often used in modern semiconductor fabrication for defects recovery, lattice recovery and impurity electrical activation of doped or ion implanted wafers. In this study, MOS capacitors and MOSFETs were post metallization annealed after gate electrode deposition. To confirm the EOT growth of MOSFET in gate-last-process after PMA, annealing temperature was mainly set to 500 ^{o}C.

2.5. Measurement Method

After fabricating MOS capacitors and MOSFETs, I measured electrical characteristics of those devices. In this study, we mainly focused on EOT, gate leakage current J_g and effective electron mobility m and interface states density D_{it} using various method. In this section the method to estimate each parameter is explained.

2.5.1. C-V measurement

Detail introduction of C-V and its basic operating principles will not be discussed. High frequency C-V measuring technique was used to evaluate the C-V curves in terms of frequency dependency (1 kHz – 1 MHz), magnitude of hysteresis, flatband voltage (V_{fb}) shift and EOT determination. In this study, C-V hysteresis was estimated from capacitance difference between forward and back ward sweeps at $V_g = V_{fb}$. V_{fb} shift is accurate determined by ploting ($1/C^2$) versus V_g. The lower knee of this curve occurs at $V_g=V_{fb}$. Such a transition is sometimes difficult to determine due to distortion on initial *C-V* curve. Differntiating this curve and finding the maximum slope of the left flank of this differential curve a second time results in a sharply peaked curve whose peak coincide with V_{fb}. For comparison purposes, CVC program developed by North Carolina State University was also used to estimate EOT and V_{fb} and C-V curves are measured using Agilent 4284A precision LCR meter.

2.5.2. J_g-V measurement

The is done using HP4156A semiconductor analyzer with minimum measurement count 10 times for every samples to confirm proper distribution on leakage current density.

2.5.3. V_{th} extraction

Threshold voltage (V_{th}) is an important MOSFET parameter. However, V_{th} is a voltage which is not uniquely defined. The existence of nonlinear curve at subthreshold region on the I_d-V_g plot makes it difficult to have a universal definition. One of the most common threshold voltage estimation methods is the “liner extrapolation method” with the drain current measured as a function of gate voltage at a low drain voltage of 100 mV to ensure operation in the linear MOSFET region. The threshold voltage is not zero below threshold and approaches zero only asymptotically. Hence the I_d versus V_g curve is extrapolated to I_d=0, and the threshold voltage is determined from the extrapolation or intercept gate voltage V_g by

$$V_{th}=V_{gSi} - V_d/2 \qquad \text{Eq 2-1}$$

where V_{GSi} is the intercepted Vg value at I_d=0 and V_d is the drain voltage used during the measurement (100 mV in this study).

The I_d-V_g curve deviates from the straight line at low gate voltage below V_{th} due to subthreshold currents and above threshold voltage due to series resistance and mobility degradation effects. Thus, in order to determine the V_{th} accurately, it is common practice to find the point of maximum slope on the I_d-V_g curve by maximum in the transconductance, fit a straight line to the I_d-V_g curve at the oint and extrapolation to Id =0, as illustrated in fig. 2.9 [2-1].

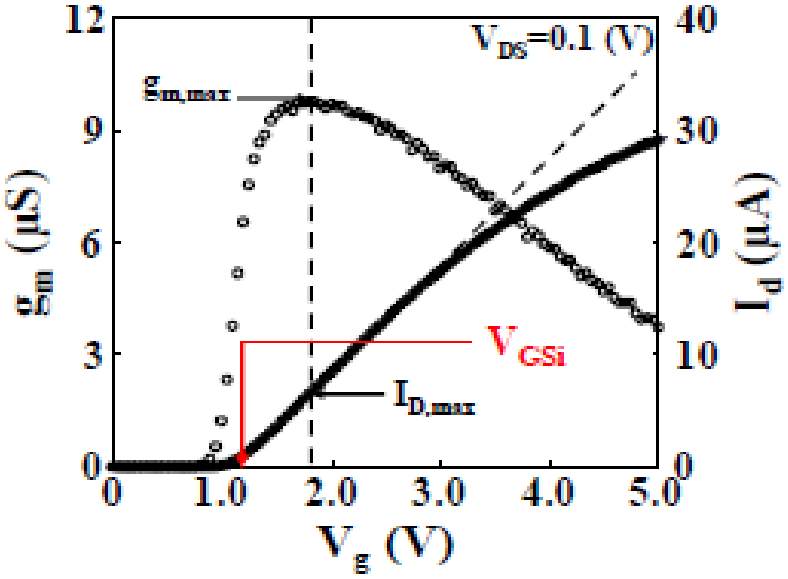

Fig 2.9 Threshold voltage determination by liner extrapolation technique.

2.5.4. Subthreshold slope measurement

Depending on the gate and source-drain voltages, a MOSFET device can be biased in one of the three following regions, linear or saturation. In the subthreshold region where $V_g < V_{th}$, the drain on the linear scale appears to approach zero immediately below the threshold voltage. However, on a logarithmic scale, the descending drain current remains at nonnegligible levels for several tenths of a volt below threshold voltage. This is because the inversion charge density does not drop to zero abruptly. Rather, it follows an exponential dependence on gate voltage. Subthreshold behavior is of particular important in modern ULSI application because it describes how a MOSFET device switches off (or turns on).

The subthreshold current is independent of the drain voltage once drain voltage is larger than a few *kT/q*, as would be expected for diffusion-dominated current transport. The dependence on gate voltage, on the other hand, is exponential with an inverse subthreshold slope [2-2].

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \qquad \text{Eq 2-2}$$

Subthreshold slope, which is that gate voltage necessary to change the drain current by one decade, is typically 70 ~ 100 mV/decade in modern MOSFET device [2-2]. Figure 2.10 illustrates the determination technique of subthreshold slope from log I_d versus linear V_g plot.

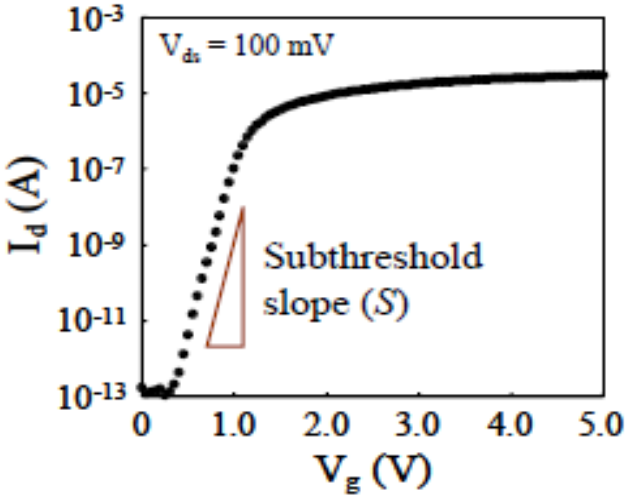

Fig 2.10 Determination technique of subthreshold slope.

If the oxide-Si interface trap density is high, the subthreshold slope will be more graded since the capacitance associated with the interface is in parallel with the depletion-layer caopacitance C_{dm}. Hence Eq.2-2 can be rewrite as,

$$S = 2.3\frac{kT}{q}\left(1+\frac{C_{dm}}{C_{ox}}\right) = 2.3\frac{kT}{q}\left(1+\frac{C_{dm}+C_{it}}{C_{ox}}\right) \qquad \text{Eq 2-3}$$

where C_{it} is the interface trap capacitance. The direct relationship between S and C_{it}, as shown in Eq.2-3 can be used to obtain the interface trap density (D_{it}) with simple assumption of $D_{it} \sim C_{it}$ [2-3].

$$D_{it} = \frac{1}{q}\left(\frac{qS}{2.3kT}-1\right)C_{ox} - C_{dm} \qquad \text{Eq 2-4}$$

This tequnique required an accurate knowledge of C_{ox} and C_{dm}. However, interface trap density obtained from this technique is usually used as a comparative technique to other more accurate and sensitive measurement techniques, like charge pumping on MOSFET or conductance method on MOS capacitor.

2.5.5. Split *CV* method

The MOSFET drain current is due to drift and diffusion of the mobile carriers in the inverted Si channel. Let consider an n-channel device of gate length L_g and gate width W_g for the derivation. The derivation for p-channel device is similar to n-channel device with minor changes. The drain current I_d can be written as

$$I_d = \frac{W\mu_{eff} Q_n V_{ds}}{L} - W\mu_{eff} \frac{kT}{q} \frac{dQ_n}{dx} \qquad \text{Eq 2-5}$$

where Q_n is the carrier channel charge density and μ_{eff} the effective mobility. The effective mobility is measured at low drain voltage of 100 mV. At low V_{ds}, one can assume that channel charge to fairy distribute and uniform from the source to drain, allowing the diffusive second term in Eq. 2-5 to be dropped. Solving Eq. 2-5 then given,

$$\mu_{eff} = \frac{g_d L}{W Q_n} \qquad \text{Eq 2-6}$$

where the drain conductance g_d is defined as

$$g_d = \left.\frac{\partial I_d}{\partial V_{ds}}\right|_{V_g\text{-constant}} \qquad \text{Eq 2-7}$$

To accurately determine the Q_n, direct measurement of Q_n from 100 kHz high frequency capacitance measurement, with mobile channel density or inverted charge density determined from the gate-to-channel capacitance/unit area (C_{gc}) according to the following equation

$$Q_n = \int_{V_{fb}}^{V_g} C_{gc} dV_g \qquad \text{Eq 2-8}$$

where V_{fb} is the flatband voltage and V_g is gate voltage. The C_{gc} is measured using the connection of fig. 2.13 (a). The capacitance meter is connected between the gate and the source-drain connected together with substrate grounded. Setup in fig 2.13(b) is used to measure the gate-substrate capacitance/unit area (C_{gs}). The connected source-drain is grounded during C_{gs} measurement. C_{gs} is used calculated bulk charge density (Q_b) according to the following equation

$$Q_b = \int_{V_{fb}}^{V_g} C_{gs} dV_g \qquad \text{Eq 2-9}$$

Bothe Qn and Qb are then used to calculate the effective vertical electric field (E_{eff}) according to

$$E_{eff} = \frac{Q_b + \eta Q_n}{\kappa_s \varepsilon_o}$$

Eq 2-10

where Q_b and Q_n are the charge densities in the space-charge region and the inversion layer, respectively. Then η in the inversion layer charge accounts for averaging of the electric field over the electron distribution in the inversion layer. The parameter η =1/2 for the electron mobility and η =1/3 for the hole mobility. Ks and e0 are thr Si dielectric constant and permittivity of vacuum, respectively [2-4, 5 6]. The capacitance, both C_{gc} and C_{gs} as a function of gate voltage is shown in fig. 2.14.

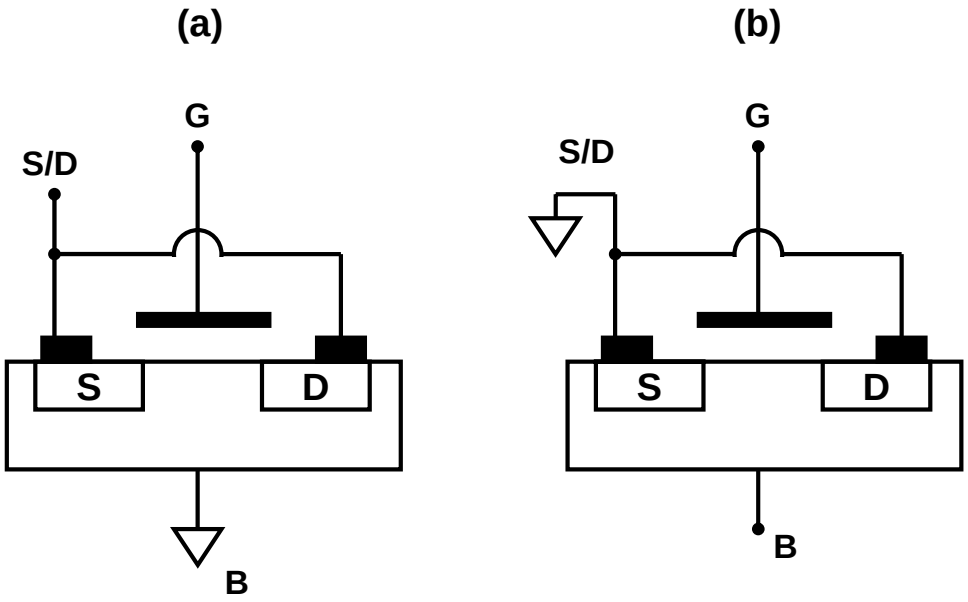

Figure 2.13 Configuration for (a) gate-to-channel, (b) gate-to- substrate capacitance measurement for split C-V measurement [2-18].

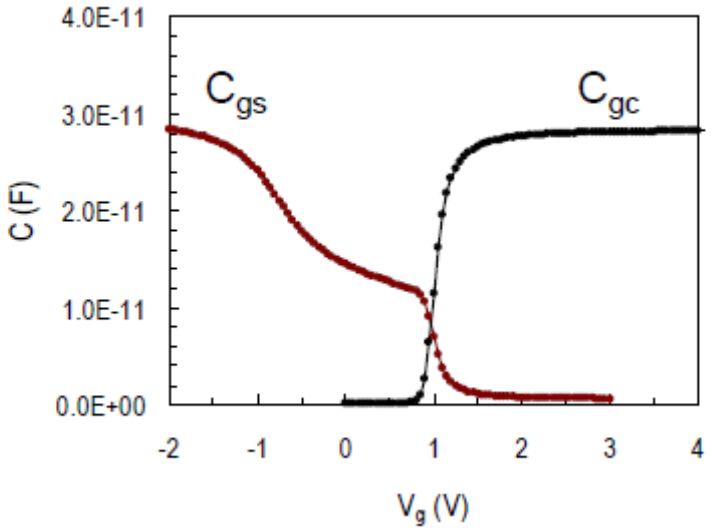

Figure 2.14 Capacitance as a function of gate voltage.

2.6. References

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[2-6] S. Takagi et al. IEDM Tech. Digest, pp.398-401 (1988).

Chapter 3. Electrical characteristics of MOS capacitors with W gate electrode

3.1. Characterization of W/HfO_2 MOS capacitors

In this chapter, HfO_2 MOS capacitors with W gate electrode were fabricated and the process to realize small EOT and small C-V hysteresis capacitors was investigated by changing deposition conditions. Deposition temperature and the amount of supplied oxygen in HfO_2 deposition were changed for small EOT MOS structure. In this experiment, HfO_2 was directly deposited on HF last Si substrate. HfO_2 is one of the promising high-k materials, which was written in chapter 1. W metal was chosen as gate metal because of its low electrical residence and high thermal endurance.

Figure 3.1 shows V_g vs. leakage current (J_g) plot with different deposition temperatures, the thickness of deposited HfO_2 was set to 5 nm in both capacitors. From the figure, we can see that in capacitor before PMA, J_g of 300 ^oC deposition was about 100 times larger than that of 100 ^oC deposition. This is why at HfO_2/Si interface, Hf-silicide was grown in deposition temperature at 300 ^oC, the Hf-silicide caused excess leakage current. On the other hand, capacitors anneled at 500 ^oC had almost the same leakage current. This result implied that after PMA 500 ^oC, SiO_2 IL grows in both capacitors (deposited at 100 and 300 ^oC) and reduces their leakage current. Eq (1) and (2) show chemical reactions of Hf-silicide and SiO_2 formation[1]. The equation means that HfO_2 easily makes SiO_2 or Hf-silicide, this reaction makes it difficult for HfO_2 to realize small EOT and low leakage current.

$$SiO_x + (x\text{-}1)Si \longrightarrow xSiO \quad \text{--------} \quad (1)$$

$$HfO_2 + 4SiO \longrightarrow HfSi_2 + 2SiO_2 \quad \text{----} \quad (2)$$

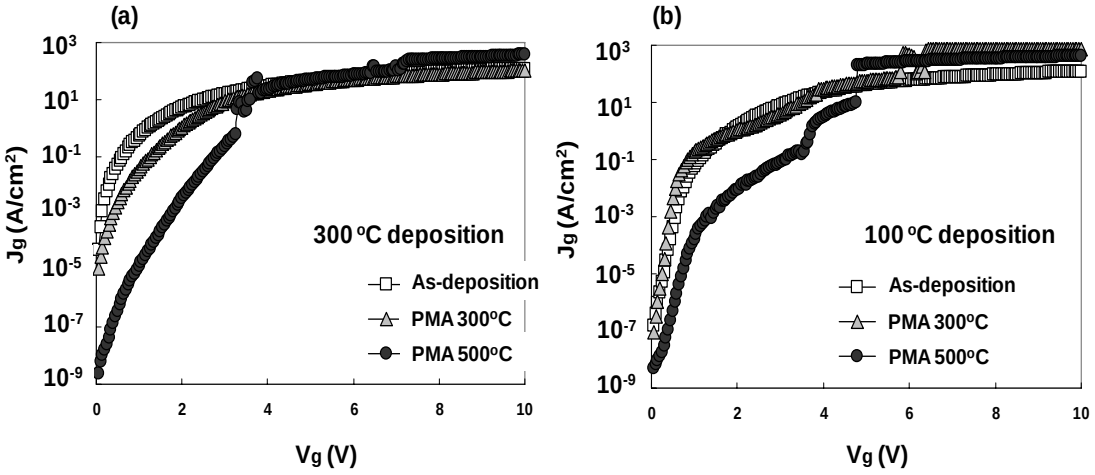

Figure 3.1 J_g-V_g plot (a) HfO_2 thin film was deposited at 300 ^oC (B) at 100 ^oC.

Figure 3.2 (a) shows CV characteristics of W/HfO_2 MOS capacitor (HfO_2 was deposited at 100 ^oC). The capacitor after PMA (post metalization annealing) at 500 ^oC had smaller capacitance density compared with that of as-deposited (non-annealing) and after PMA at 300 ^oC. This is because SiO_2 IL grew after 500 ^oC PMA according to Eq(1). This SiO_2 formation was confirmed by XPS analysis (fig. 3.3(a)), from the figure, Hf-silicate peaks were also observed. This result means that though HfO_2 was deposited directly on HF-lasted Si substrate, after PMA 500 ^oC, dielectric layer can not realize high-k/Si directly contacted interface and HfO_2/SiO_2 interface was formed (fig. 3.3(b)). But this SiO_2 formation could reduce C-V hysteresis because SiO_2 IL has little defects. So in aspect of C-V hysteresis, IL reaction is effective.

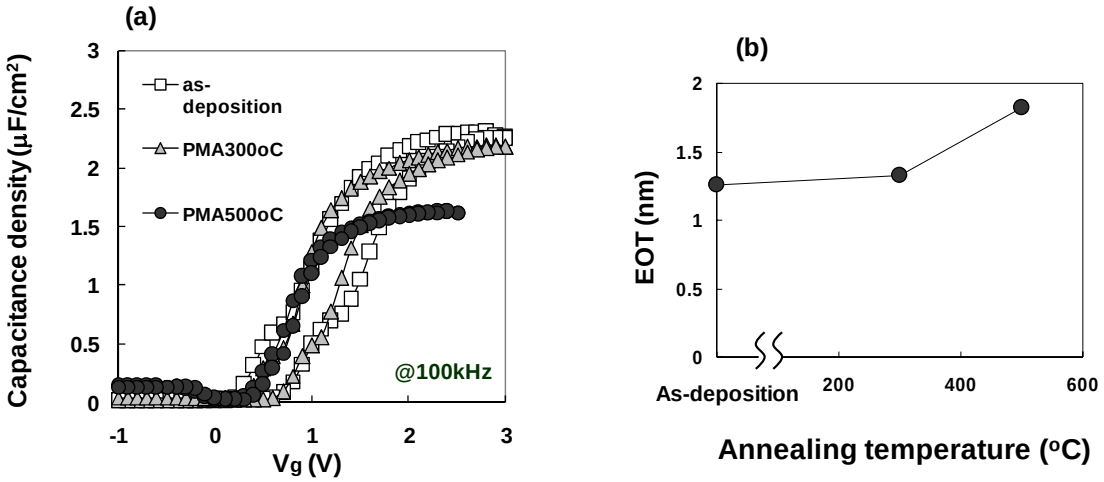

Figure 3.2 Electrical characteristic of HfO_2/Si MOSCAPs; (a) C-V curves in various annealing temperatures and (b) Annealing temperature vs. EOT plot.

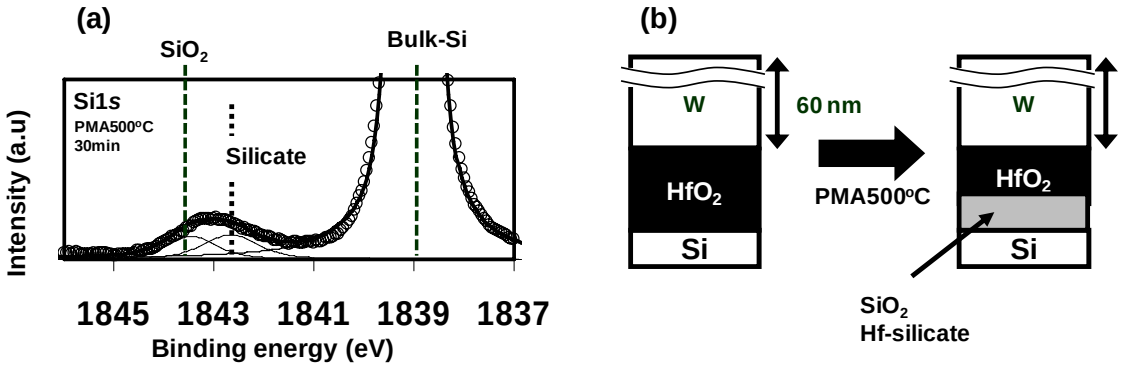

Figure 3.3 HfO_2/Si MOSCAPs; (a) XPS analysis and (b) the MOS structure before and after PMA.

In this experiment, I fabricated W/HfO_2 MOSCAPs changing the deposition temperature and found that in capacitors deposited at 300 ^oC, Hf-silicide was grown and large gate leakage current occur. This large leakage could not be confirmed in the capacitors whose HfO_2 was deposited at 100 ^oC. Figure 3.4 shows Annealing temperature vs. J_g

plot in each capacitor deposited at 100 and 300 ^{o}C. Each J_g values were almost the same after 500 ^{o}C PMA. This is because SiO_2 layer grew after PMA 500 ^{o}C, so in the gate-last transistors, HfO_2 deposition temperature is not a serious problem.

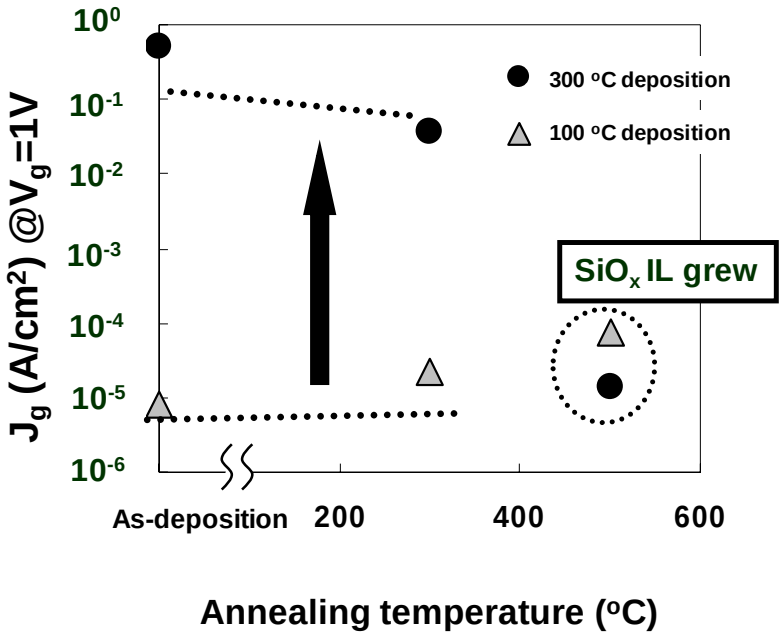

Figure 3.4 HfO_2/Si MOSCAPs; Annealing temperature vs. J_g plot, SiO_2 formation after PMA 500 ^{o}C made J_g small in each capacitor depositited at 100 and 300 ^{o}C.

HfO_2 deposition temperature is the key to control the Hf-silicide reaction and SiO_2 growth, so I fabricated W/HfO_2 MOS capacitors with supplying oxygen during HfO_2 deposition to reduce Hf-silicide reaction and C-V hysteresis (in this experiment HfO_2 was deposited at 100 ^{o}C). Figure 3.5 shows CV curves of MOSCAPs deposited in oxygen ambient, oxygen pressure is set to 8.0 x 10^{-6} and 2.0 x 10^{-5} Pa each. In both MOSCAPs, the capacitance density decreased after PMA 500 ^{o}C and large C-V hysteresis observed in as-deposition and PMA 300 ^{o}C decreased to almost zero after

PMA 500 ^{o}C. Gate leakage current was also measured (fig. 3.6). From the figure we can see that oxygen supply in HfO_2 deposition had small effect on the leakage current. In this experiment we fabricated W/HfO_2 MOS capacitors which were deposited in oxygen ambient. The effect of oxygen supply was small in aspect of thermal endurance and leakage current.

In chapter 3.1, I measured capacitance density and C-V hysteresis of MOS capacitors by changing deposition conditions and found that HfO_2 deposition temperature was large impact on the leakage current due to Hf-silicide formation and 100 ^{o}C HfO_2 deposition could reduce J_g compared with 300 ^{o}C deposition. On the other hand, oxygen supply in oxide deposition has small effect on the capacitance and C-V hysteresis.

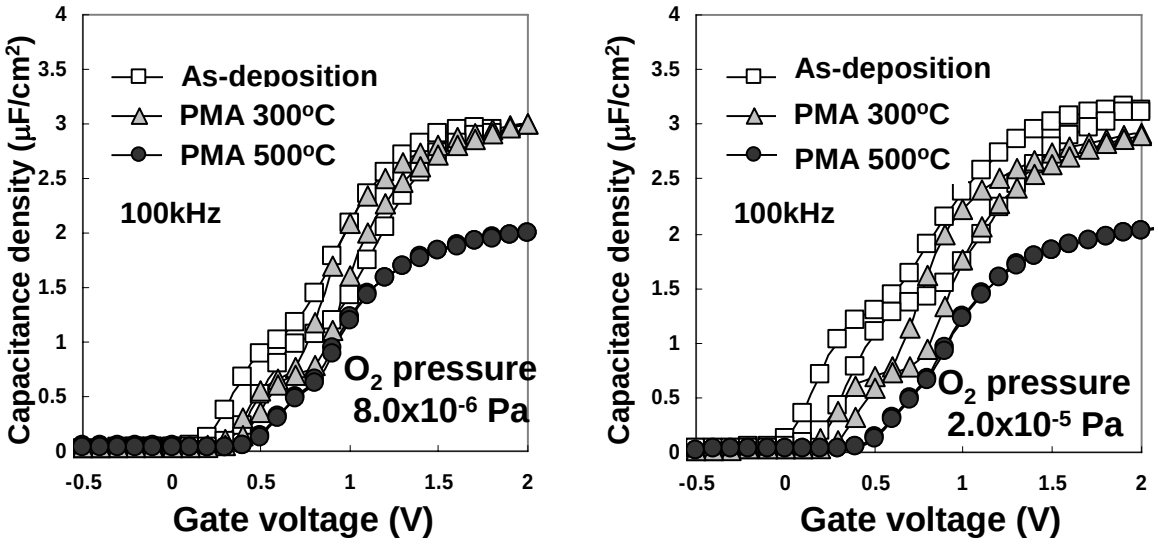

Figure 3.5 HfO_2/Si MOSCAPs; (a) deposited in oxygen pressure x10^{-6} Pa (b) deposited in oxygen pressure x10^{-6} Pa.

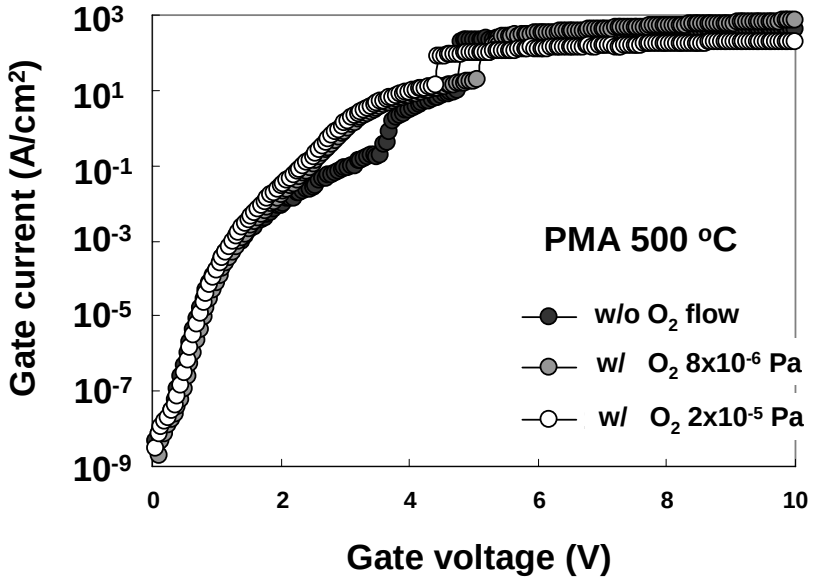

Figure 3.6 J_g-V_g plot of HfO_2/Si MOSCAPs (PMA 300 ^oC). The effect of oxygen supply in HfO_2 deposition was small.

3.2. Characterization of W/La_2O_3 MOS capacitors

I fabricated W/La_2O_3 MOS capacitors. La_2O_3 has relatively large dielectric constant (> 20) with high band off set for electron. However, La_2O_3 easily absorbs water from the air [2] so *in-situ* process to avoid any moisture is needed [3]. Figure 3.7 shows C-V characteristics of the MOSCAPs which were fabricated throw the *ex-situ* process and the *in-situ* process each. In both capacitors, La_2O_3 thickness was set to 5 nm, capacitance density was different although the insulator thickness was the same. La_2O_3 changed to $La(OH)_x$ after absorption of the water and the dielectric constant decreased, so I have to fabricate MOSCAP through in-situ process to realize small EOT MOS devices. Figure 3.8 shows schematic illustration of La_2O_3's water absorption, without W gate capping, La_2O_3 easily absorbs water and forms $La(OH)_x$ which has lower dielectric constant compared with that of La_2O_3 without water absorption. The dielectric constant of $La(OH)_x$ depends on the amount of absorbed water. As the amount of absorbed H_2O increases, the ε_r of $La(OH)_x$ decreases. So, in this study, all MOS capacitors and MOSFETs were fabricated through the *in-situ* process (La_2O_3 was deposited at 300^oC). At 100^oC deposition, MOS capacitors have large EOT compared with 300^oC deposition. This result implied that in 100^oC deposition, La_2O_3 can easily react with H_2O in the deposition chamber, so I need high temperature deposition to avoid water absorption of La_2O_3. Capacitance density after PMA 500 ^oC was smaller than that of as-deposition. Like HfO_2 MOSCAPs, IL growth occurs. The IL was composed of La-silicate layer (ε_r ~ 9), not SiO_2 layer [3]. And this La-silicate was composed of various ratios of La and Si. So, La_2O_3 was one of the candidates which can realize high-k/Si directly connected interface without SiO_2 layer (fig. 3.9).

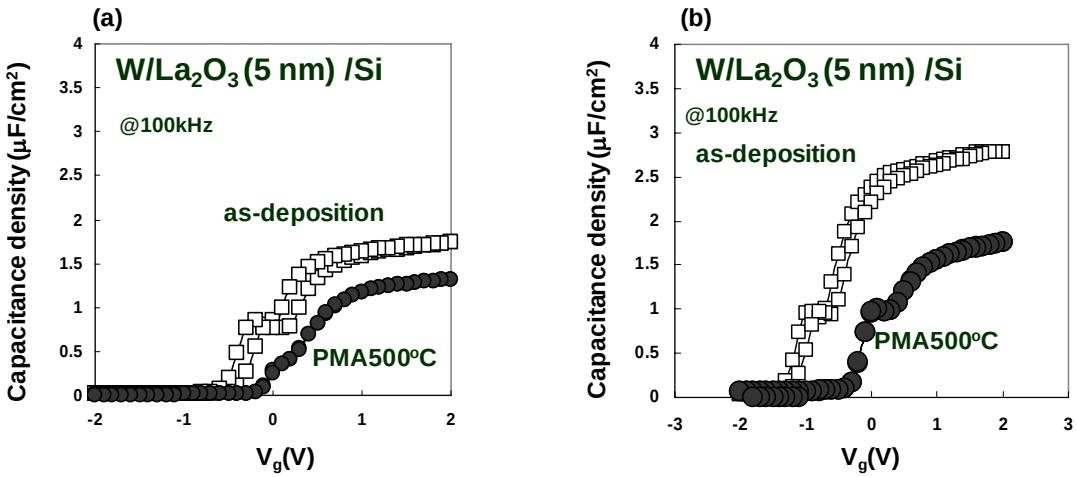

Figure 3.7 C-V characteristics of La_2O_3/Si MOSCAPs; (a) through the *ex-situ* process .and (b) through the *in-situ* process.

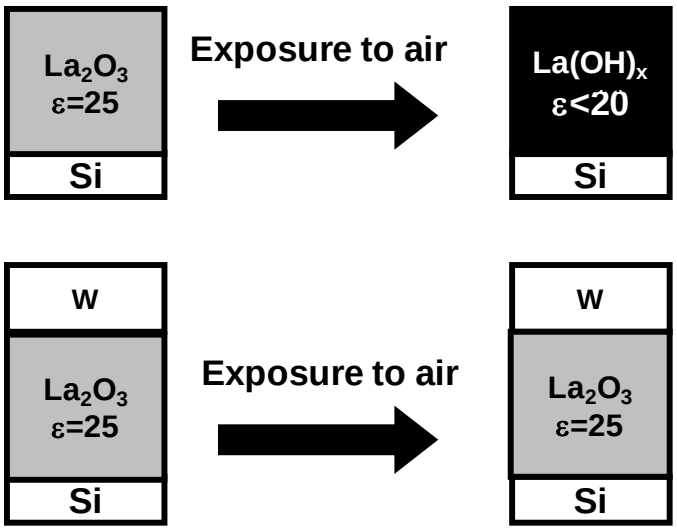

Figure 3.8 The model of water absorption; By capping W gate electrode on La_2O_3 through the *in-situ* process, water absorption into La_2O_3 was stopped.

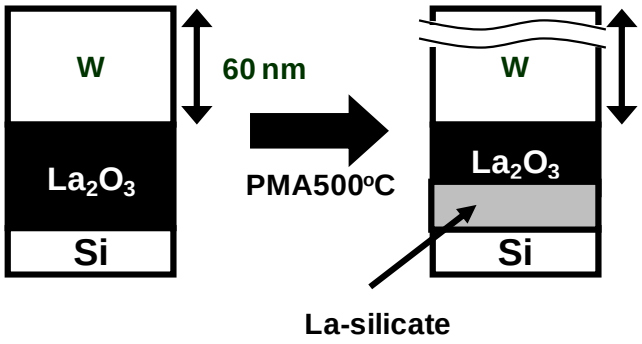

Figure 3.9 A Structure of W/ La_2O_3 before and after PMA; La_2O_3 could realize high-k/Si directly contacted interface without SiO_2 even after PMA 500 ^oC.

3.3. Characterization of HfO_2/La_2O_3 stacked MOS capacitors with W

Recent study shows that La_2O_3 incorporation to Hf-based materials can reduce V_{th} for n-channel MOSFET [4]. In this experiment, HfO_2 and La_2O_3 stacked MOS capacitors were fabricated (shown in Fig. 3.10(a)), La_2O_3 was inserted at HfO_2/Si interface. Fabricated capacitor's *C-V* curves are shown in fig. 3.10 (b). Like HfO_2 and La_2O_3 single capacitors, capacitance density after PMA 500 ^oC decreased because of interfacial layer growth. On the other hand, the V_{fb} was smaller than that of HfO_2 single layer capacitor. That is why V_{fb} (V_{th}) is determined by the proportion of Hf and La atoms at Si or SiO_2 interface [5]. This V_{fb} shift was caused by the existence of dipole slayer at high-k/Si or high-k/SiO_2 interface and the areal density of dipoles are different from

atoms which combines to Si atoms (fig. 3.11). So, in order to reduce high threshold voltage in HfO_2, La_2O_3 insertion to Si substrate is effective way (fig. 3.12). In the current study, the purpose is to fabricate n-channel MOSFET, so La_2O_3 insertion to Si interface is effective way to reduce V_{th} of the MOSFET. with W gate electrode

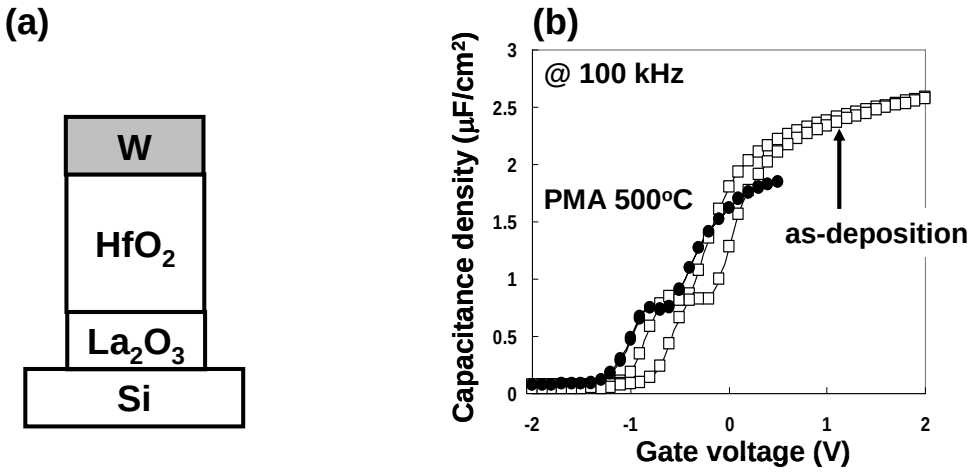

Figure 3.10 (a) Schematic illustration of HfO_2/La_2O_3 stacked MOS capacitor and (b) the C-V characteristics.

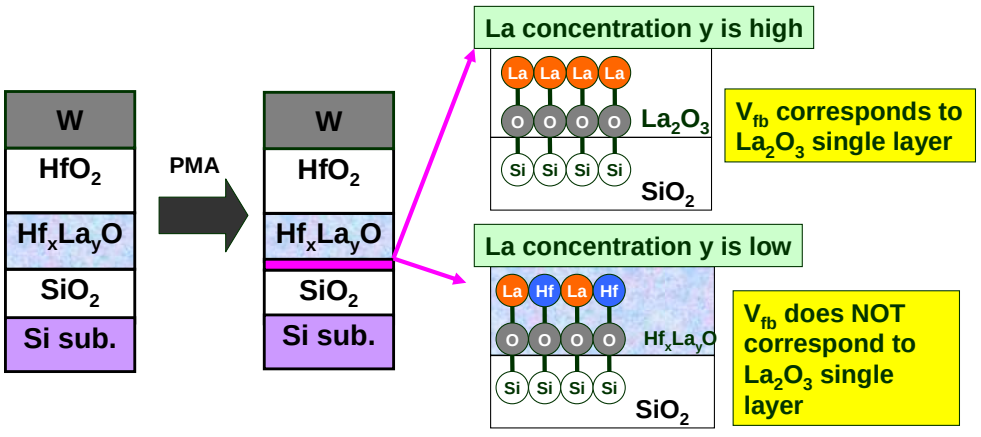

Figure 3.11 V_{fb} shift model by incorporating La_2O_3 to the HfO_2 interface [4]. This model shows that changing high-k proportion at the SiO_2 interface can control V_{fb}.

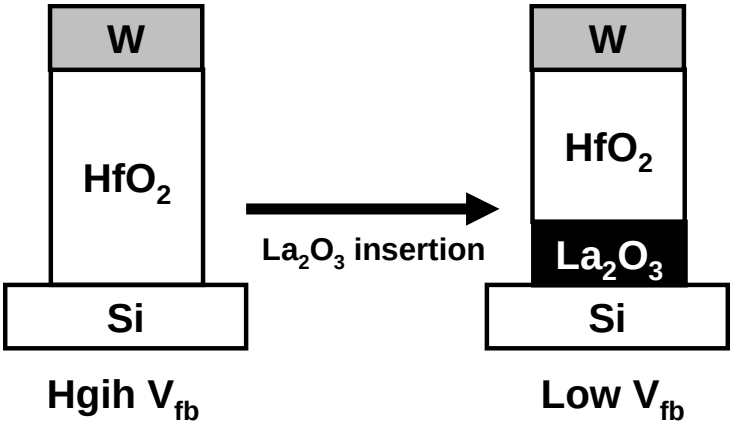

Figure 3.12 A V_{fb} reduction method by inserting La_2O_3 at HfO_2/Si interface.

La_2O_3 incorporation is effective in changing V_{fb}, I also examined EOT change after PMA. Figure 3.13 shows EOT change of each structure. All MOS capacitors have about 0.6 nm EOT before annealing, the EOT increased to 1.0 - 1.2 nm after PMA. From the result, HfO_2 /La_2O_3 could not suppress EOT growth after PMA.

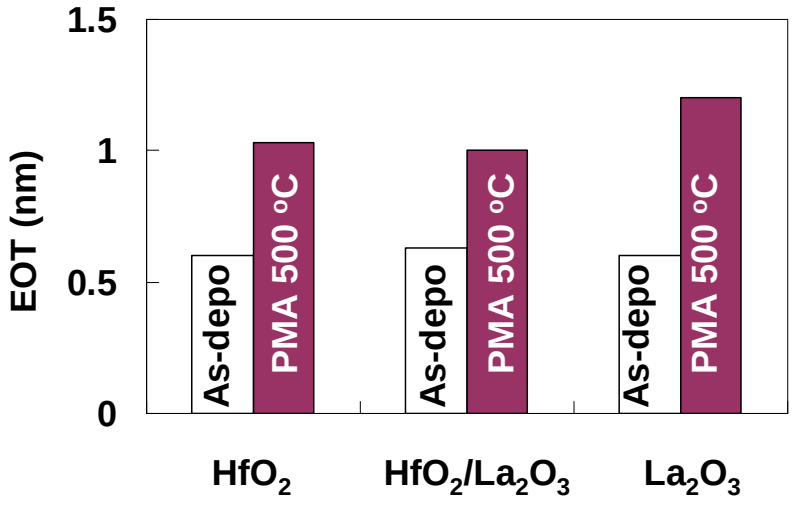

Figure 3.13 EOT changes of each structure MOS capacitors; all structures could not reduce sub-1 nm EOT after PMA.

3.4. Effect of La_2O_3 incorporation to HfO_2/Si interface

In figure 3.11, V_{fb} shift model was shown. To confirm that V_{fb} can be controlled between that of HfO_2 and La_2O_3 single layer MOS capacitors, I fabricated HfO_2/La_2O_3 (0.4nm~0.6nm) stacked layer MOS capacitors using W gate electrode. Figure 3.14 shows cross sectional TEM image of HfO_2/La_2O_3 (0.4nm). A SiO_x IL layer was observed after PMA 500 ^oC, which means that the directly connected interface of high-k and Si could not be realized in this structure. Figure 3.15 shows C-V curves of HfO_2, La_2O_3 single layer and HfO_2/La_2O_3 stacked MOS capacitors. HfO_2 has high V_{fb} and as the amount of incorporated La_2O_3 increased, V_{fb} shifted forward that of La_2O_3. This result shows that V_{fb} can be tuned between the value of HfO_2, La_2O_3 single layer MOS capacitors by controlling the amount of incorporated La_2O_3.

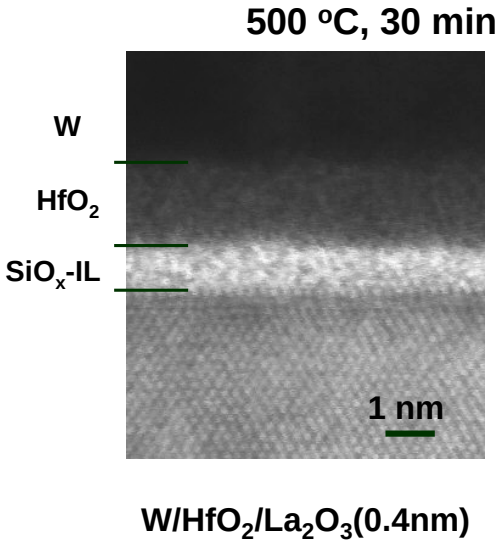

Figure 3.14 TEM image of HfO_2/La_2O_3 (0.4nm) MOS capacitor; after PMA 500^oC, SiO_x IL grow.

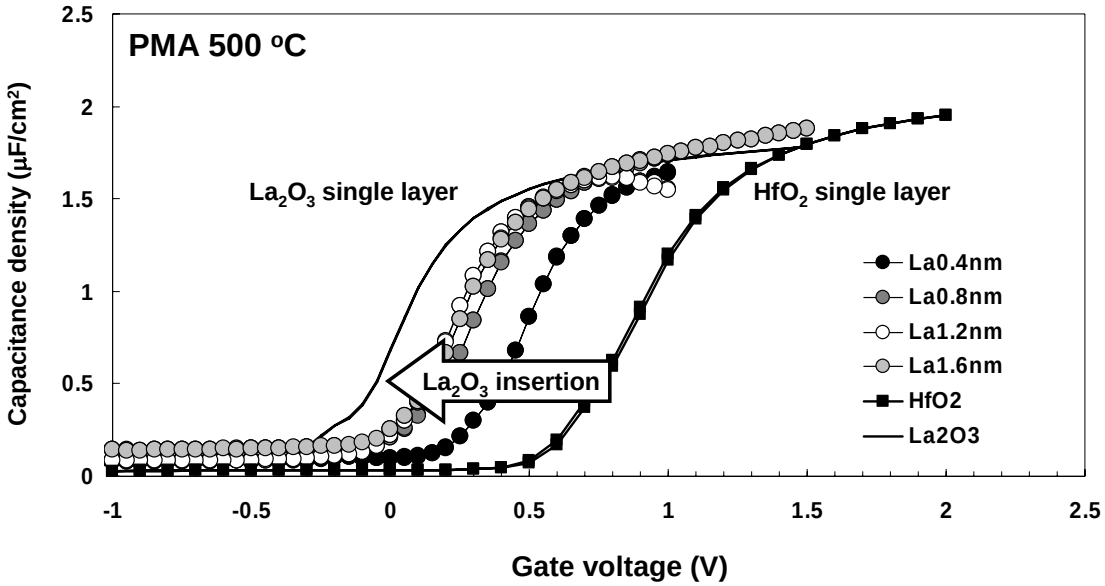

Figure 3.15 C-V curves of HfO_2, La_2O_3 single layer and HfO_2/La_2O_3 stacked MOS capacitors; HfO_2 has high V_{fb} and as the amount of incorporated La_2O_3 increased, V_{fb} shifted to La_2O_3.

Figures 3.16 and 3.17 show La_2O_3 thickness vs. V_{fb} plot of the MOS capacitors, V_{fb} shift started to saturate when inserted La_2O_3 reached to about 1 nm and the V_{fb} value is almost the same as those of La_2O_3/SiO_2 MOS capacitors. Considering that V_{fb} is determined by a proportion of La and Hf compositional ratios at the high-k/Si or high-k/SiO_2 interface, all MOS capacitors with La_2O_3 incorporation had SiO_2 IL after PMA and V_{fb} decreased until La_2O_3 formed one mono layer. Once one mono layer La_2O_3 was formed, the compositional ratios of HfO_2 and La_2O_3 at the interface do not change. However, in order to further reduce V_{fb}, the SiO_2 IL must be removed or another high-k material which could reduce V_{fb} of HfO_2 should be introduced.

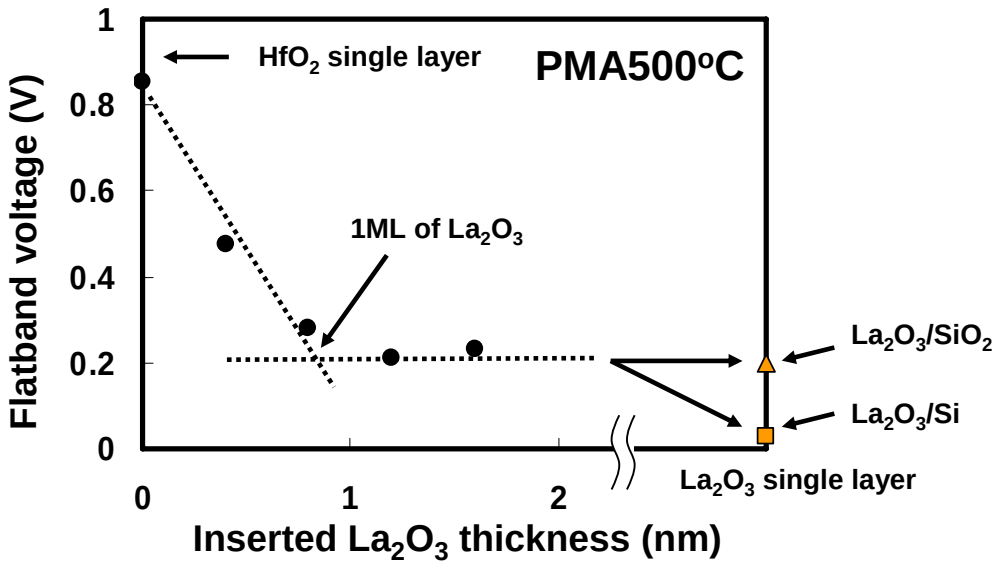

Figure 3.16 La_2O_3 thickness vs. V_{fb} plot; V_{fb} shift to negative side as the inserted La_2O_3 increased.

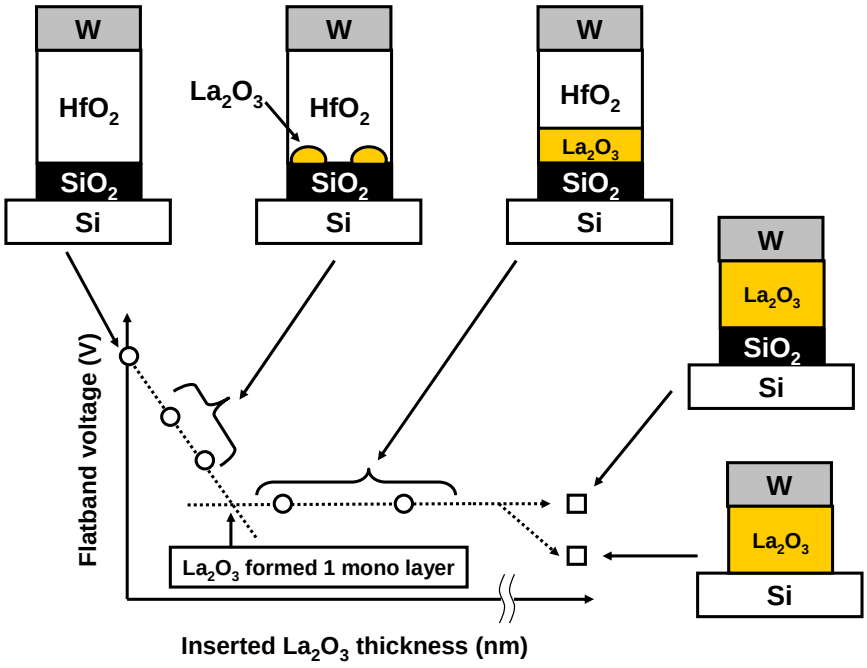

Figure 3.17 V_{fb} shift by La_2O_3 incorporation; existence of SiO_2 IL has important roll in V_{fb} shift.

3.5. Summary

In chapter 3, HfO_2 or La_2O_3 single-layer capacitors and HfO_2/La_2O_3 stacked layer MOS capacitors were fabricated using W as a gate electrode, it is important that high-k materials are directly connected with Si substrate to realize 0.5 nm EOT even after annealing. Figure 3.18 shows Si 1*s* spectrum analysis using XPS, only La_2O_3 single layer MOS structure could realize high-k/Si interface. This IL reaction after PMA was considered to be caused by oxygen supply from the W gate electrode that contains oxygen (shown in chapter 5). So, in order to achieve small EOT even after PMA, another high-k material or gate metal introduction is necessarily.

On the other hand, V_{fb} of each capacitor was measured and it was revealed that La_2O_3 incorporation to HfO_2/Si interface is effective to reduce V_{fb}. So with the W, La_2O_3 single layer is effective both for small EOT and low V_{th} (shown in fig. 3.19).

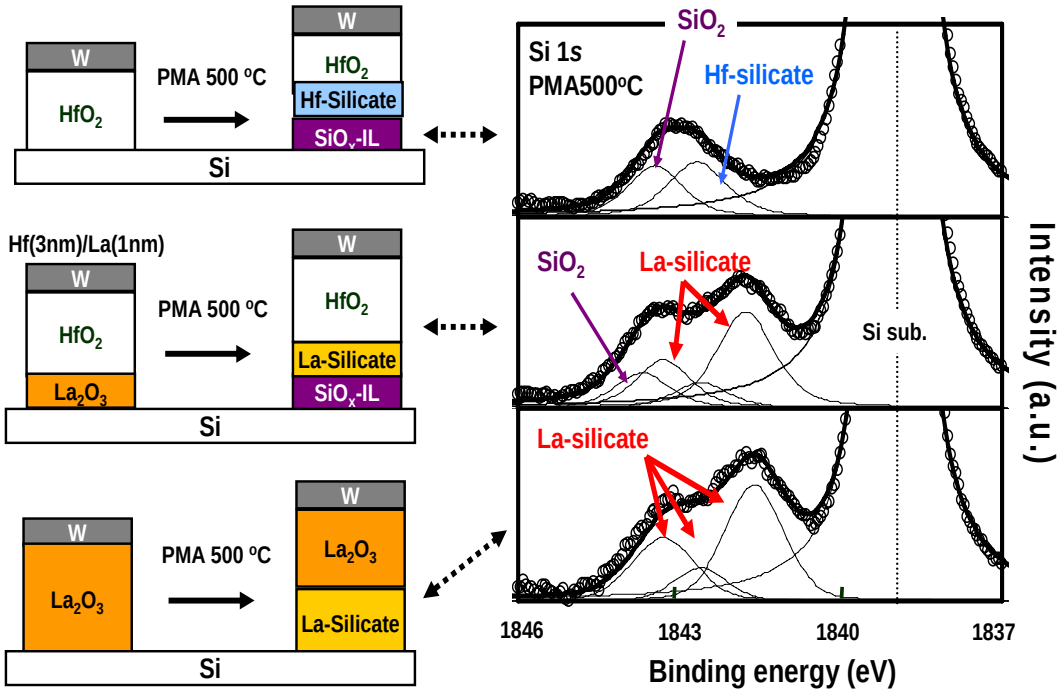

Figure 3.18 Si 1*s* spectrum analysis using XPS; only La_2O_3 single layer MOS structure could realize high-k/Si interface.

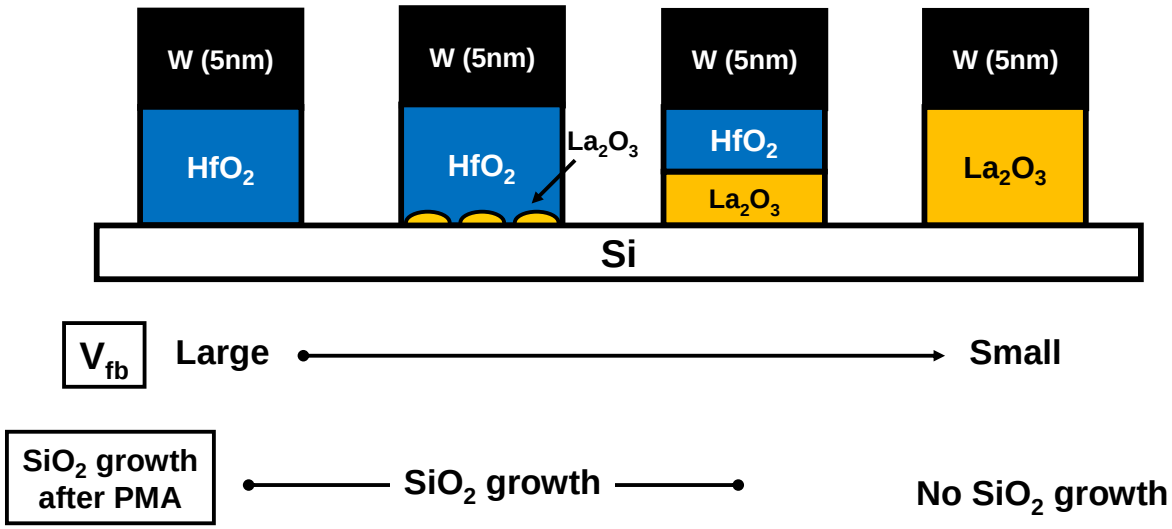

Figure 3.19 V_{fb} of each structure MOS capacitor and SiO_2 growth after PMA 500 ^oC; only La_2O_3 single layer capacitor could realize high-k/Si interface.

3.6. References

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Chapter 4. n-channel MOSFET with W gate electrode

4.1 Electrical characteristics of W/HfO_2 MOSFET

In this chapter I fabricated MOSFETs with W gate electrode to investigate electrical characteristics by changing the gate stack structures.

Firstly, I fabricated HfO_2 single layer MOS transistors with various HfO_2 thicknesses (shown in fig. 4.1) in gate-last-process and measured the threshold voltage (V_{th}), interface states (D_{it}) and effective electron mobility (μ_{eff}). All MOSFETs consist a SiO_2 IL because they were annealed at 500 ^oC (chapter 3).

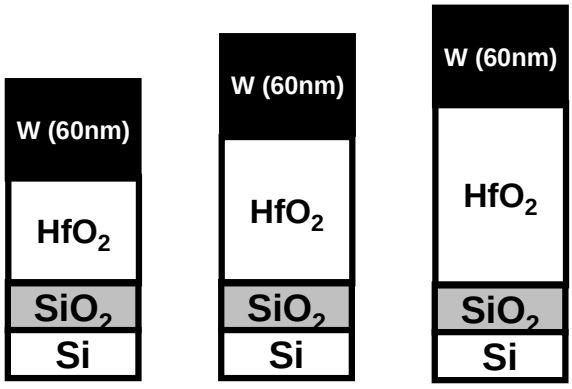

Figure 4.1 Schematic illustration of fabricated W/HfO_2 MOSFETs. Because all transistors were fabricated through gate-last-process, and annealed at 500 ^oC.

Figure 4.2 shows μ_{eff} -E_{eff} plot of the MOSFETs, the EOT values were changed from 1.1 nm to 1.4 nm after PMA 500 ^oC. From fig. 4.2, we can see that as EOT deceased, effective electron mobility decreased in all electric field values. This mobility degradation along with EOT reduction is widely observed in many reports (figure 4.3) [1-6]. In this structure, the smallest EOT after PMA 500 ^oC was 1.1 nm. This mobility reduction is caused by remote-coulomb-scattering (RCS), which is shown in chapter 5.

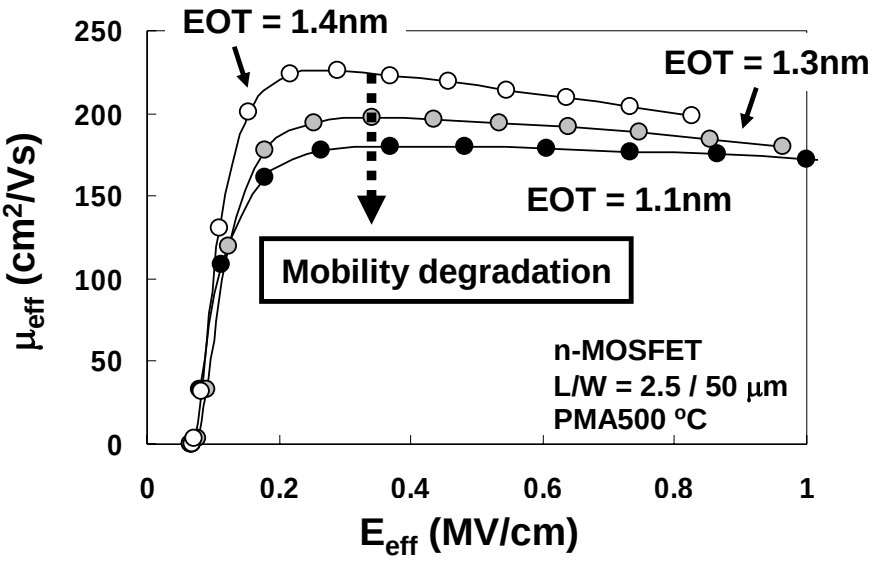

Figure 4.2 E_{eff}-μ_{eff} plot of the W/HfO_2 MOS transistors; mobility decreased along to EOT scaling.

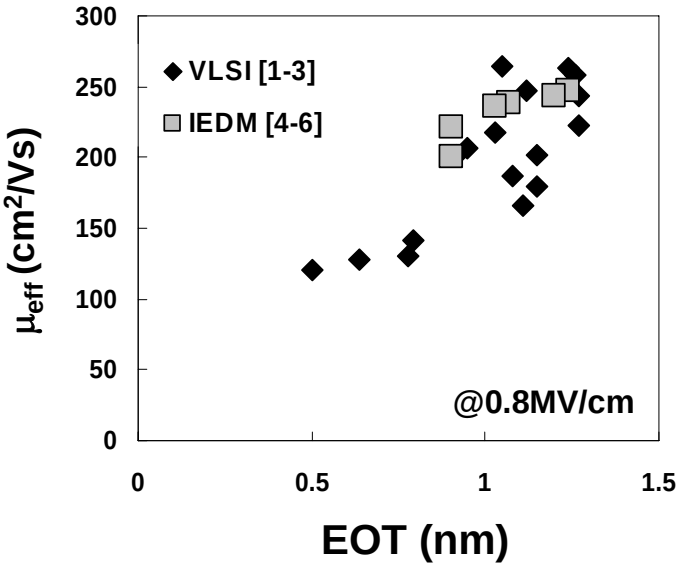

Figure 4.3 EOT- μ_{eff} plot reported in recent VLSI and IEDM; electron mobility decreased along to EOT scaling.

4.2 Electrical characteristics change by inserted La_2O_3

4.2.1 Introduction

I fabricated HfO_2 single layer MOS capacitors using W as gate electrode and measured the electrical characteristics. In this chapter, various thickness La_2O_3 was incorporated to HfO_2/Si interface and the electrical characteristic changes were investigated. I measured threshold voltage, interface states density and electron mobility of all the MOS transistors. All transistors were annealed at 500 ^oC, after PMA 500 ^oC, SiO_2 IL is formed (shown in chapter 3) though high-k was directly deposited on Hf-last Si substrate (shown in fig. 4.4).

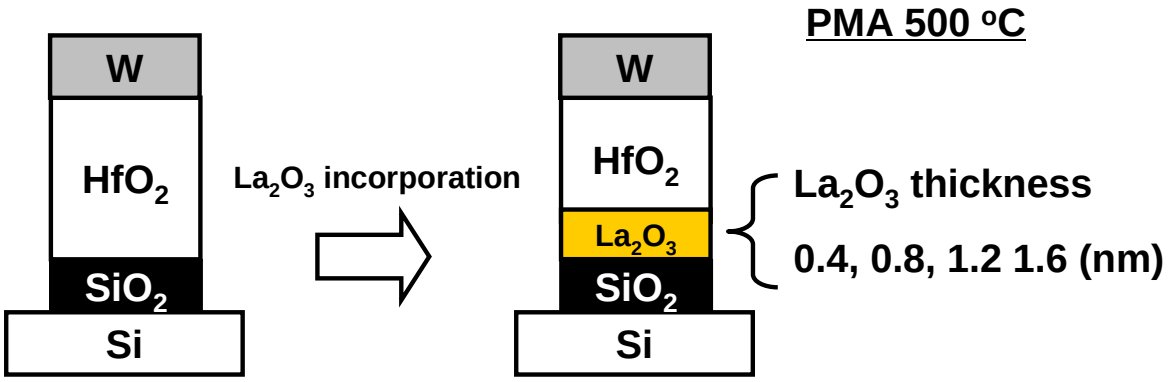

Figure 4.4 Fabricated MOS transistors; La_2O_3 (0.4 ~ 0.6 nm) was incorporated to HfO_2/Si interface. After PMA 500^oC, SiO_2 IL grew.

4.2.2 V_{th} change by La_2O_3 insertion

First of all, I measured V_{th} of each MOS transistor. In chapter 3, I found that La_2O_3 incorporation to HfO_2/Si interface was effective to reduce V_{fb} of HfO_2/Si MOS capacitor, this tendency is also expected to be observed in V_{th}. Figure 4.5 shows inserted La_2O_3 thickness vs. V_{th} plot, V_{th} shifted to negative side as the amount of incorporated La_2O_3 increased. This tendency can be expressed using the model shown in figure 3.16.

Because La_2O_3 single layer MOSFET has no SiO_2 layer, the V_{th} is smaller compared with HfO_2/La_2O_3 structure MOSFET which has SiO_2 IL. V_{th} of HfO_2 single layer was about 0.5 V and V_{th} of HfO_2/La_2O_3 is 0.15 V in the V_{th}-saturated-region shown in fig. 4.5. This result shows that HfO_2/La_2O_3 structure is better compared with HfO_2 single layer for small V_{th} .

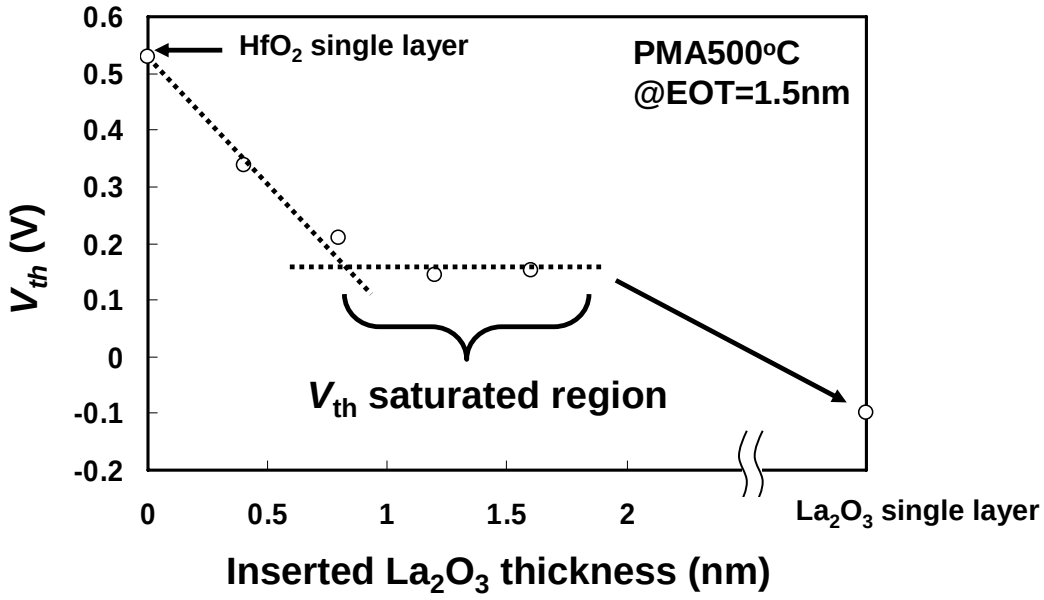

Figure 4.5 V_{th} -Inserted La_2O_3 thickness plot; V_{th} shifted to negative side as the amount of incorporated La_2O_3 increased.

4.2.3 D_{it} change by La_2O_3 insertion

I also measured interface state density (D_{it}) by using the charge pumping method.

Figure 4.6 shows an inserted La_2O_3 thickness vs. D_{it} plot after PMA 500 ^oC, HfO_2 single layer and HfO_2/La_2O_3 stacked layer MOSFET have almost the same values except MOSFET with 1.2 nm La_2O_3 insertion (This too small D_{it} might be due to a measurement error caused by large leakage current). On the other hand, La_2O_3 single layer MOSFET has larger D_{it} than that of other MOSFETs. This is because HfO_2 single layer and HfO_2/La_2O_3 stacked layer MOSFET formed SiO_2 IL after PMA 500 ^oC, this SiO_2/Si interface has small D_{it}. On the other hand, La_2O_3 single-layer MOSFET does not have SiO_2 IL and forms La-silicate/Si interface, so the interface has larger D_{it}. This D_{it} change is considered to have an effect on effective mobility and reliability of MOSFET.

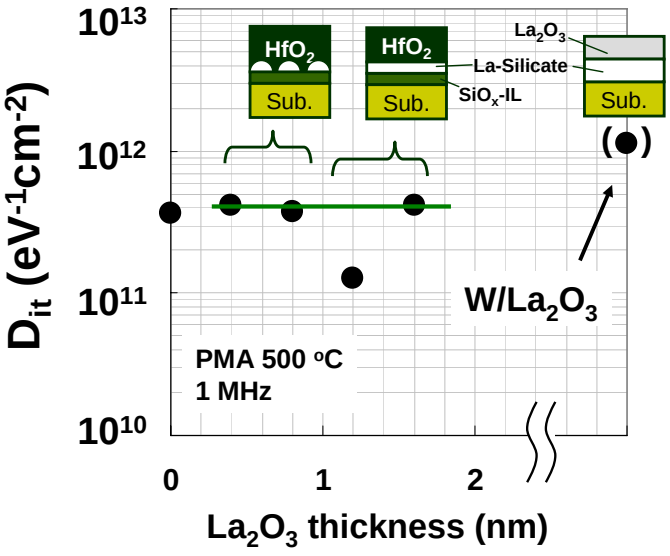

Figure 4.6 Inserted La_2O_3 thickness - D_{it} plot (PMA 500 ^oC); HfO_2 single layer and HfO_2/La_2O_3 stacked layer MOSFET has SiO_2 IL and its reduce D_{it}.

4.2.4 μ_{eff} change by inserted La_2O_3

In figure 4.2 and 4.3, we can see that effective mobility decreases along with an EOT scaling. So, to compare μ_{eff} values of various gate structures MOSFET, we should choose the same EOT transistors. Figure 4-7 shows electron mobility plot of HfO_2 single layer and HfO_2/La_2O_3 stacked layer MOSFET, from the figure, we can see that μ_{eff} increased largely by La_2O_3 incorporation to HfO_2/Si interface in the whole range of electric field. The mobility dependency on inserted La_2O_3 thickness was shown in Figure 4.8, no μ_{eff} dependency on La_2O_3 thickness was observed in this experiment. La_2O_3 of which thickness is from 0.4 to 1.6 nm had almost the same mobility and the same EOT after PMA and only 0.4 nm insertion of La_2O_3 could improved μ_{eff} dramatically in both large and small electric fields, in addition, La_2O_3 single layer MOSFET has larger mobility. This result indicates that La_2O_3 has advantage in μ_{eff} compared with HfO_2 single layer when high-k is directly deposited on Si-substrate.

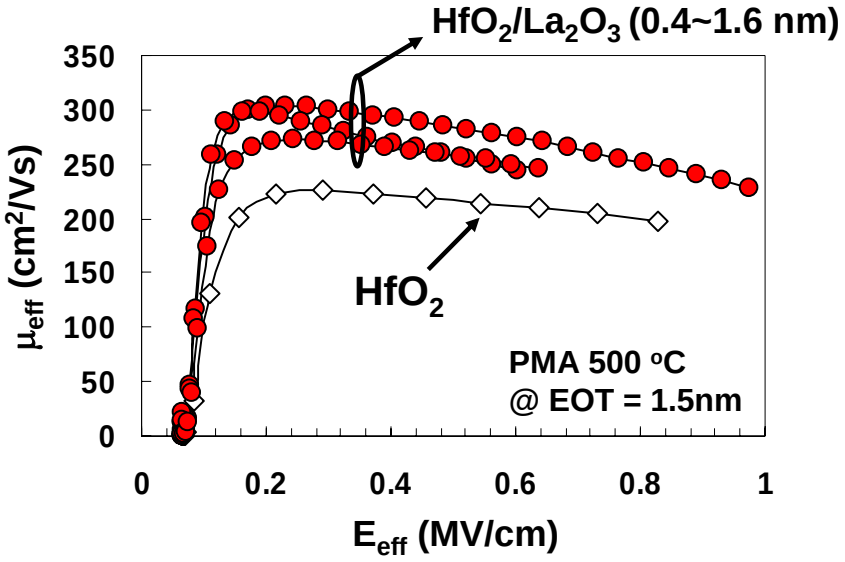

Figure 4.7 Electron mobility plot of HfO_2 single layer and HfO_2/La_2O_3 stacked layer MOSFET.

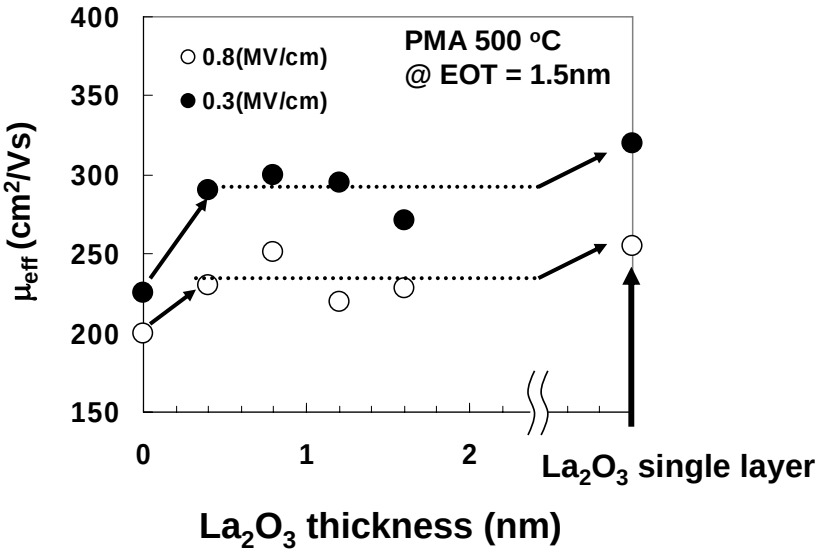

Figure 4.8 μ_{eff} – La_2O_3 thickness plot; only 0.4 nm insertion of La_2O_3 could improved m_{eff} dramatically in both large and small electric fields

4.3 References

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Chapter 5. Introduction of oxygen control gate electrode

5.1 $TaSi_2$ introduction in HfO_2/La_2O_3 MOS capacitors

To achieve further EOT scaling, IL growth after annealing should be reduced, however with W gate electrode, IL growth after PMA is a serious problem (shown in chapter 3 and 4). There are two ways to overcome this EOT growth, one is to change high-k materials, and the other is to change the gate electrode. In this chapter, we introduce new gate electrode $TaSi_2$. From the result of chapter 3, without oxygen supply in annealing, no interfacial reactions occurs. Considering that O impurity in W has an impact on the EOT increase with RTA conditions [1], this IL growth is caused by oxygen supply from W (shown in fig. 5.1).

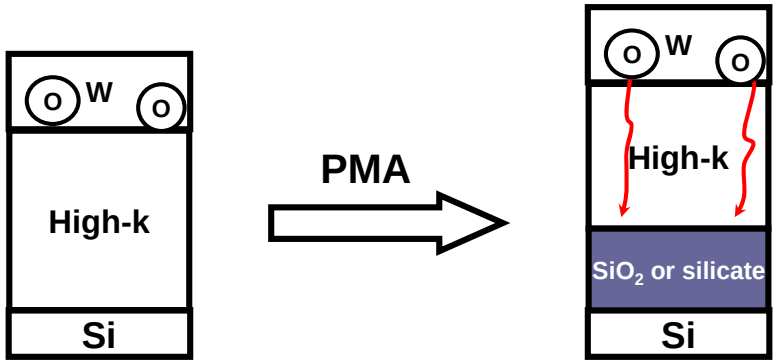

Figure 5.1 IL growth model; W deposited by RF sputtering essentially contains large amount of oxygen and causes interfacial reaction.

In this experiment, I introduced $TaSi_2$ gate electrode to prevent oxygen diffusion expecting the same effect as $TaSi_xN_y$ electrode which has been reported to be an excellent oxygen diffusion barrier up to 900 ^oC [2]. To confirm the model of figure 5.1, we fabricated HfO_2/La_2O_3 stacked MOS capacitors with $TaSi_2$(60nm)/W gate electrode.

The thickness of W film was varied from 5 nm to 60 nm while gate insulator structures were all the same HfO_2(2.5nm)/La_2O_3(1nm) (shown in figure 5.2). In this experiment, $TaSi_2$ was deposited on W film through the *in-situ* process to avoid any oxidation of W. If W gate electrode intrinsically contains oxygen, to change inserted W thickness might change the amount of oxygen supply and EOT growth after PMA.

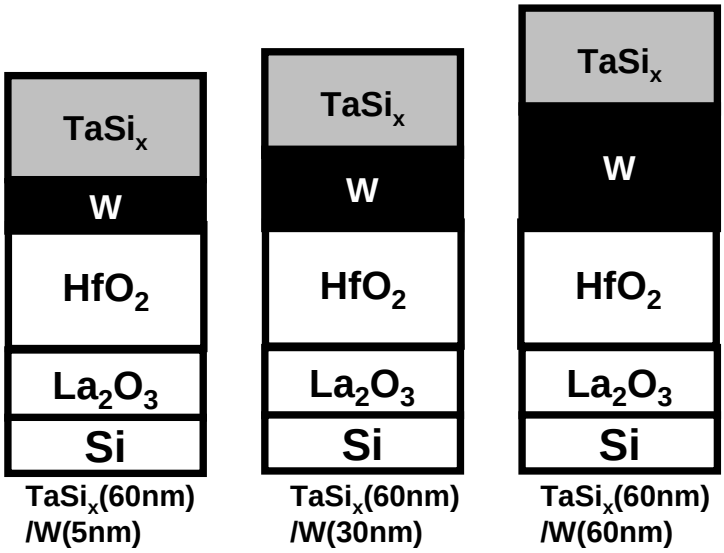

Figure 5.2 Fabricated MOS capacitors; gate electrode was $TaSi_2$(60nm)/W and gate oxide was HfO_2/La_2O_3 stacked structure.

Figure 5.3 shows C-V characteristics of fabricated MOS capacitors before and after PMA 500 ^oC. Before PMA, all capacitors had almost the same EOT (= 0.6 nm), this is because gate oxide structure was all the same (shown in fig. 5.2) and no oxygen diffusion had occurred yet. On the other hand, EOT after PMA 500^oC changes among each capacitor. As the thickness of inserted W increased, EOT after PMA increased. C-V hysteresis that is observed in as-deposited capacitors decreased after PMA. This

result shows that oxygen supply from the W gate electrode in PMA can recover defects in the dielectric layer or interface and reduce C-V hysteresis.

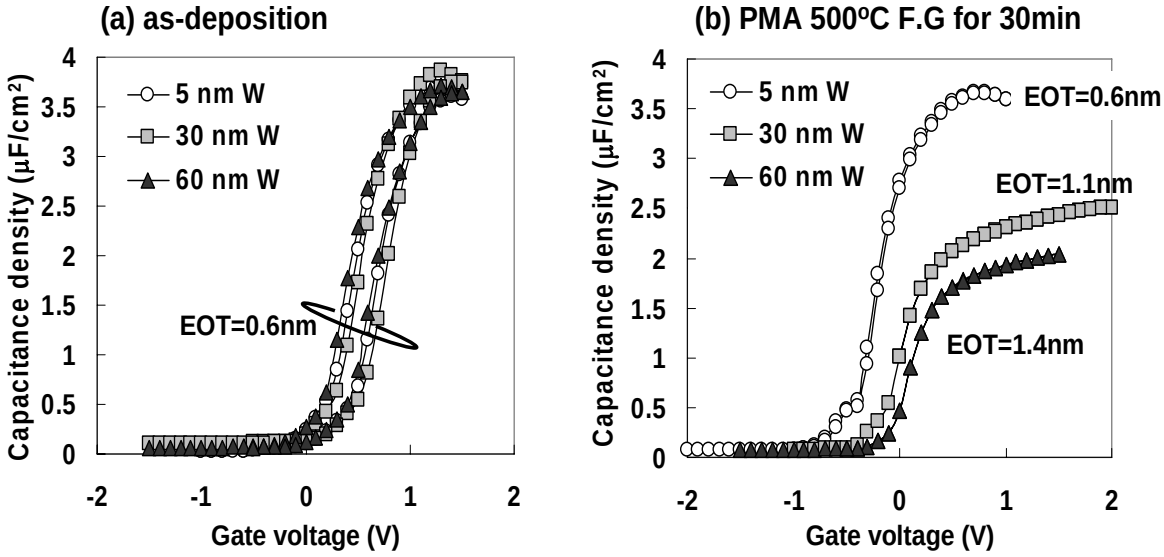

Figure 5.3 C-V characteristics of MOS capacitors (a) before annealing and (b) after PMA.

Figure 5.3 shows that EOT growth after PMA had largely been dependent on the insertion thickness of W. As the thickness of inserted W increased, EOT after PMA increased. Figure 5.4 shows EOT vs. annealing temperature plot. EOT before annealing was about 0.6 nm, after PMA, each capacitor had different EOT. Especially, in $TaSi_2$(60nm)/W(5nm) electrode, EOT increase after PMA was less than 0.1 nm. From this result, we can see that W intrinsically contains large amount of oxygen that causes EOT growth after PMA, so thinner W insertion can achieve small EOT even after PMA. To confirm the fact that W deposited by RF sputtering certainly contains oxygen, I measured the amount of oxygen using SIMS (shown in fig. 5.5). The measured sample had W/La_2O_3 MOS structure, the top of W gate formed WO_x because it was exposed to

the air. This figure shows that the amount of oxygen density contained in the W gate electrode is 10 % of the oxygen density in La_2O_3 thin film. Considering that La_2O_3 thickness was from 2 to 4 nm and W thickness was 60 nm, gate metal contains 1.5 to 3.0 times larger amount of oxygen compared with oxygen in La_2O_3 gate oxide layer. I also measured C-V hysteresis (shown in table 5.1). Before annealing C-V hysteresis was large (> 0.2 V), on the other hand, the hysteresis after PMA became small. The W (5 nm) capacitor has a little larger hysteresis (0.01 V) but it is negligibly small. Figure 5.6 shows a schematic illustration of the effect of W buffer layer insertion of different thickness. In this chapter I used $TaSi_2$(60nm)/W(5nm) gate electrode in the following experiment.

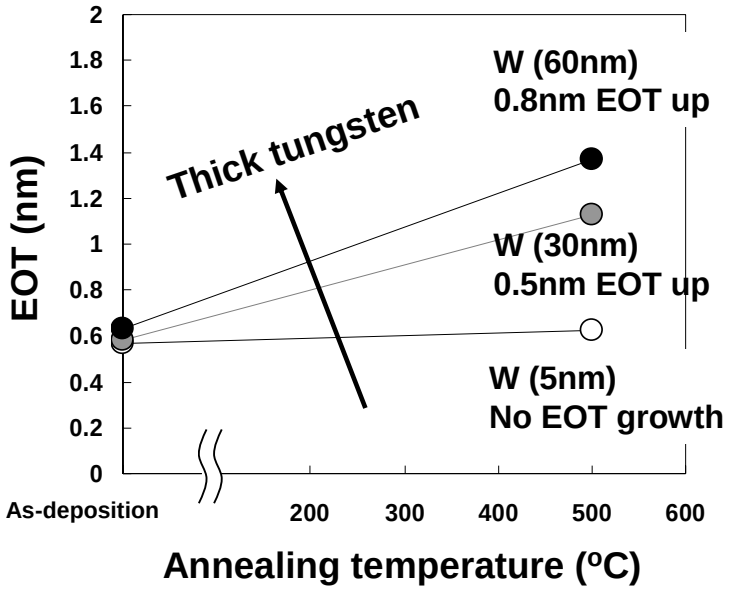

Figure 5.4 EOT vs. annealing temperature plot of each capacitor; as the thickness of inserted W increased

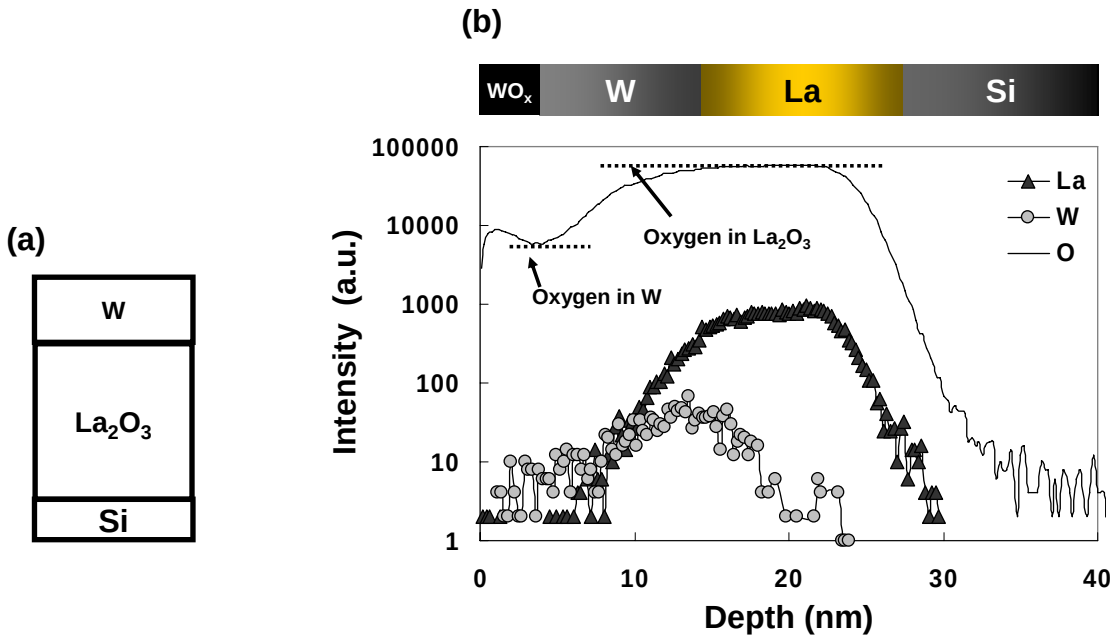

Figure 5.5 (a) W/La_2O_3 MOS capacitor and (b) its SIMS analysis; the amount of oxygen contained in W gate electrode is enough to form IL after PMA.

Table 5.1 EOT growth and C-V hysteresis change before and after PMA 500^{o}C

	W (60nm)	W (30nm)	W (5nm)
EOT growth	+ 0.8 nm	+ 0.5 nm	+ 0 nm
CV hysteresis red: before PMA Blue :after PMA	 0.25 V 0.00V	 0.30 V 0 .00V	 0.20 V 0.01 V

Large amount of oxygen supply (Thick Tungsten)

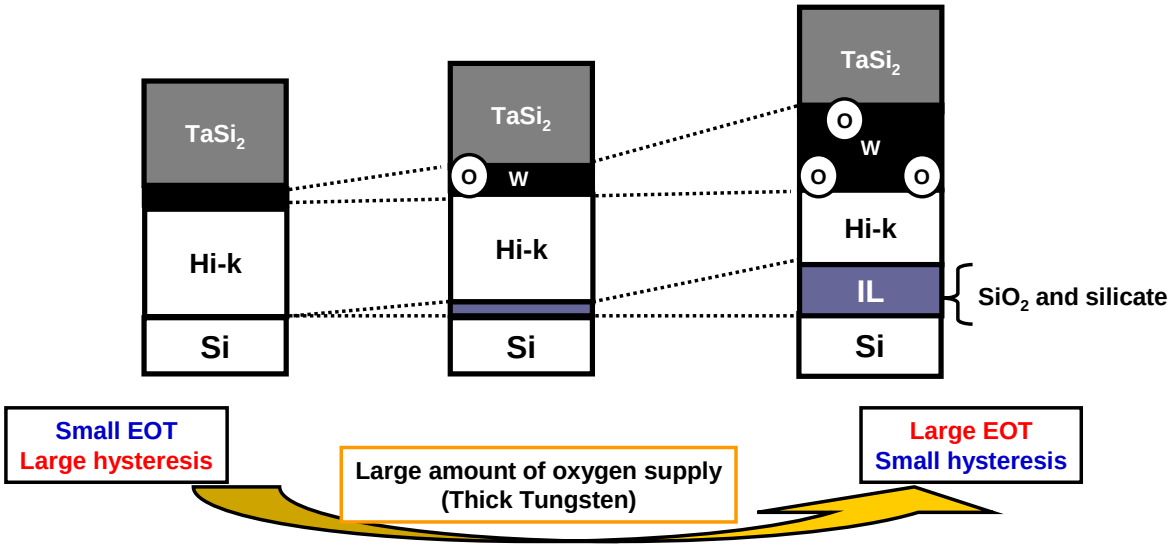

Figure 5.6 Effect of W buffer layer; as inserted W thickness increased, IL growth after PMA increased.

5.2 HfO_2 single layer MOSFET with $TaSi_2$/W(5nm)

To investigate whether $TaSi_2$/W(5nm) is effective in other oxide structures, I fabricated HfO_2 single layer MOS capacitor using $TaSi_2$/W(5nm). Figure 5.7 shows CV characteristics of HfO_2 single layer MOS capacitor, no EOT growth after PMA 500^{o}C was observed from its EOT change. This result shows that $TaSi_2$/W(5nm) stacked gate electrode is also effective in HfO_2 single layer MOS capacitors. In this experiment, the smallest EOT after PMA 500 ^{o}C was estimated to be 0.80 nm.

To investigate EOT scaling limit of HfO_2 MOSFET with $TaSi_2$/W(5nm) gate electrode, we fabricated HfO_2 single layer MOSFET. Figure 5.8 shows I_{ds}-V_g and I_{ds}-V_{ds} characteristic of 0.63 nm EOT n-MOSFET after PMA 500 ^{o}C. Figure 5.9 shows its C_{gc} and inversion density vs. mobility plot.

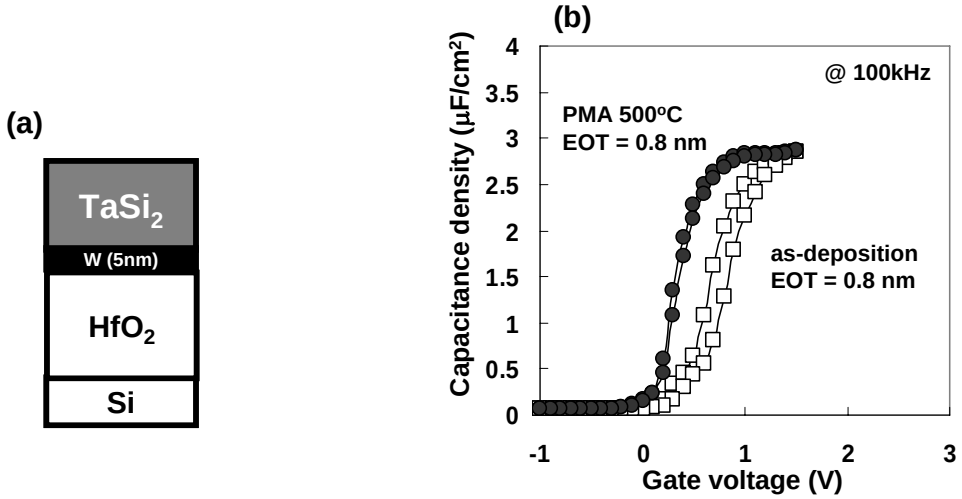

Figure 5.7 (a) Fabricated HfO_2 single layer MOS capacitor, (b) the C-V characteristics

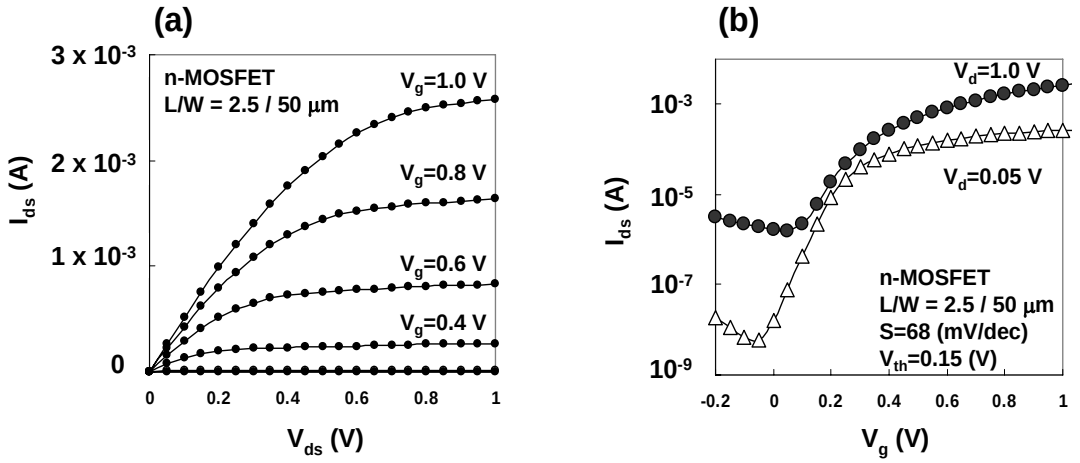

Figure 5.8 (a) I_{ds}-V_g and (b) I_{ds}-V_{ds} characteristic of 0.63 nm EOT HfO_2 single layer n-MOSFET after PMA 500 ^oC.

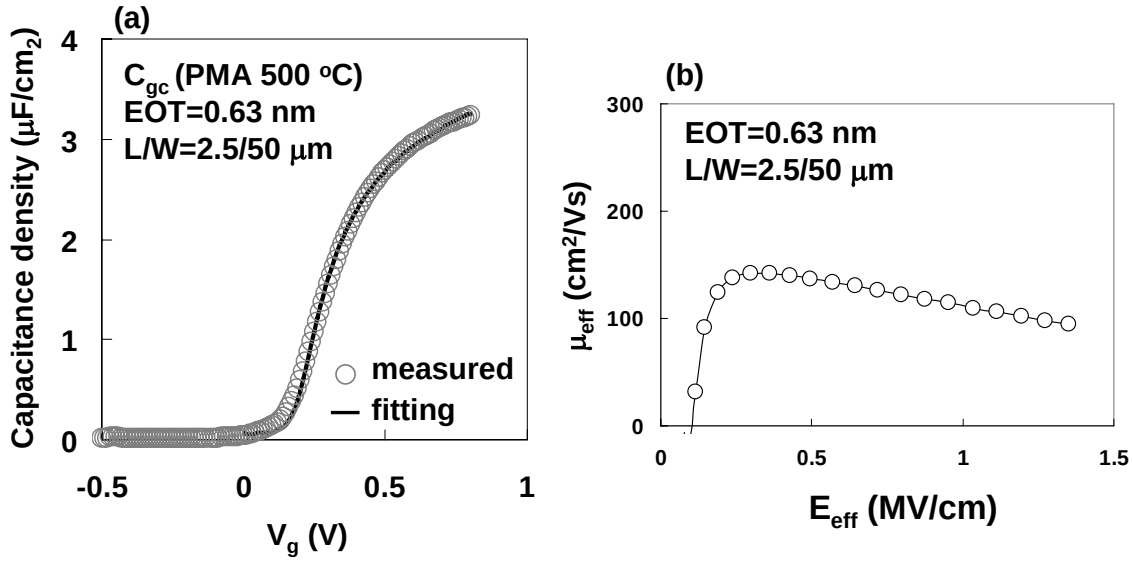

Figure 5.9 (a) C_{gc} and (b) E_{eff} vs. μ_{eff} plot of 0.63 nm EOT HfO_2 single layer n-MOSFET after PMA 500 ^oC.

5.3 MOSFET characteristics changes by $TaSi_2$/W introduction

Firstly I investigated a cause of mobility degradation along with EOT scaling using HfO_2 single layer MOSFET with W and $TaSi_2$/W gate electrodes. Schematic illustrations of the fabricated transistors are shown in figure 5.8, EOT values of the transistors are also shown in the figure. All transistors were annealed at 500 ^oC. After PMA, SiO_2 IL grew in MOSFET with W, which was shown in chapter 3. Among these MOSFETs, the smallest EOT values are 0.64 and 1.1 nm each. Figure 5.9 shows μ_{eff} on inversion density plot of W/HfO_2 transistors, as the EOT values decreased, μ_{eff} decreased in all electric field region. But, especially in low electric field region, μ_{eff} degradation was large. In this chapter, the cause of this μ_{eff} degradation is discussed.

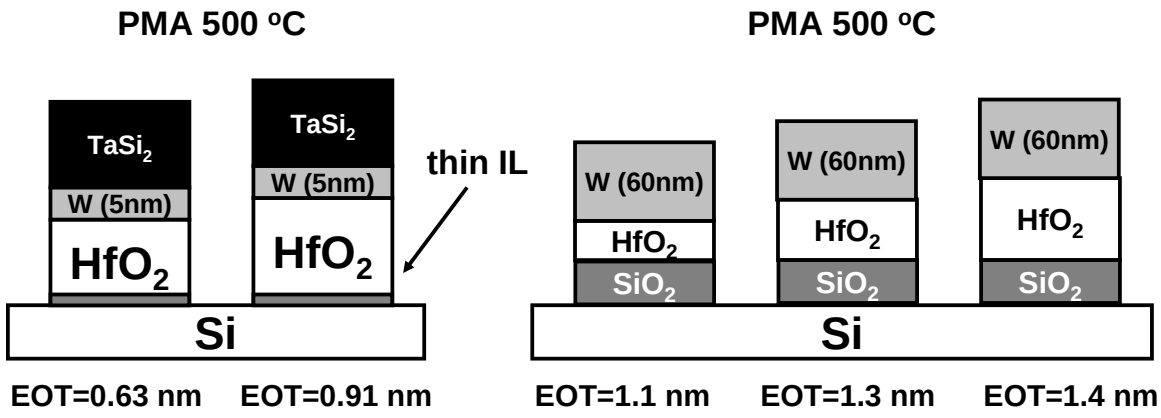

Figure 5.8 Fabricated n-channel MOS transistors; Their EOT values after PMA 500 ^oC.

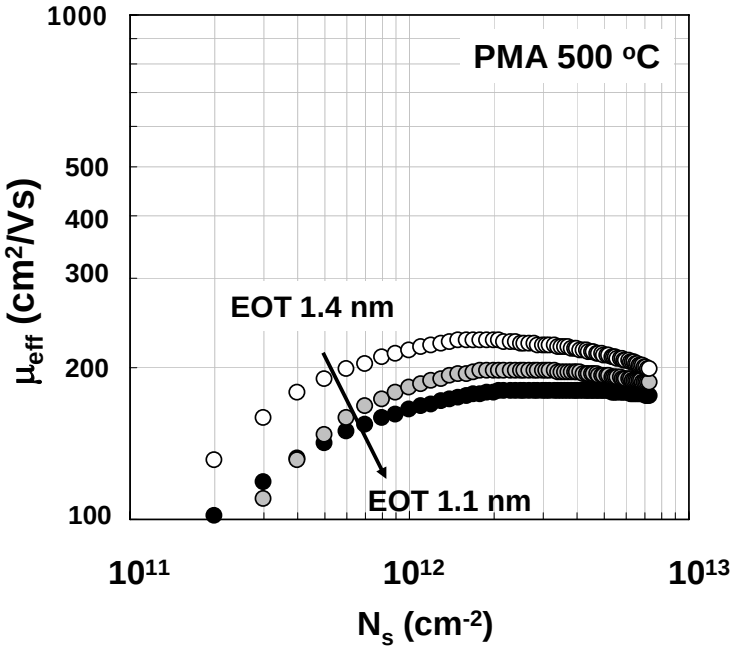

Figure 5.9 μ_{eff} on inversion density plot of W/HfO_2 MOSFET, as the EOT values decreased, μ_{eff} degradation is conspicuous in low electric field region.

In general, μ_{eff} degradation in low electric field region is caused by remote coulomb scattering (RCS). I extracted the additional scattering component using the Matthiessen's rule and compared with the 1.4 and 1.3 nm EOT n-MOSFETs. Figure 5.10 shows each μ_{eff} and the extracted component. A relation of μ_{add}~$N_s^{0.5}$ is observed at low N_s region, suggesting an additional Coulomb scattering. This result shows that mobility degradation along with EOT scaling is caused by RCS. In $TaSi_2$/W gate electrode, we also confirmed that mobility degradation along with EOT scaling is caused by RCS (shown in Figure 5.11). One of the origins of the RCS is considered to be gate metal defects in gate oxide [3]. Gate metal diffusion and mobility degradation model is shown in fig. 5.12.

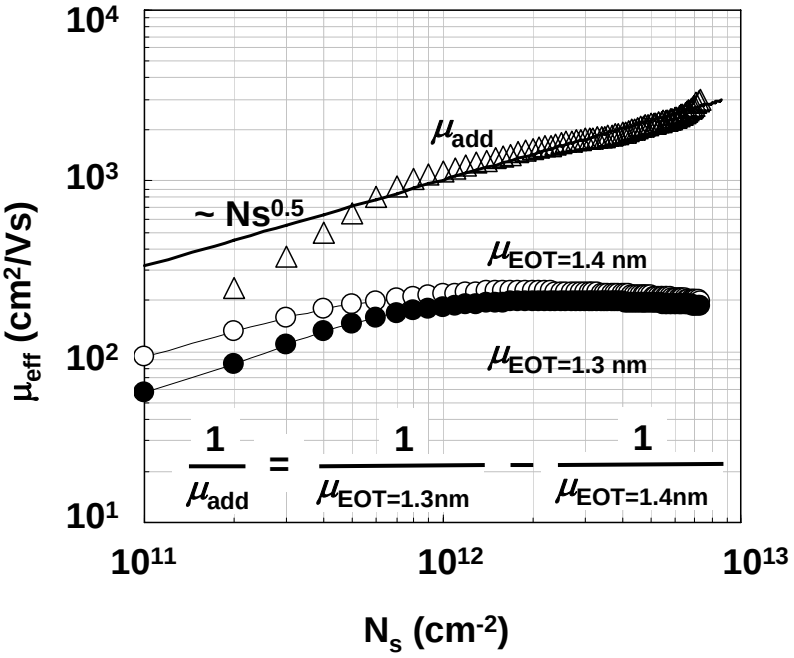

Figure 5.10 μ_{eff} comparison and the extracted component of W/HfO_2 MOSFET. A relation of μ_{add}~$N_s^{0.5}$ is observed at low N_s region, suggesting an additional Coulomb scattering.

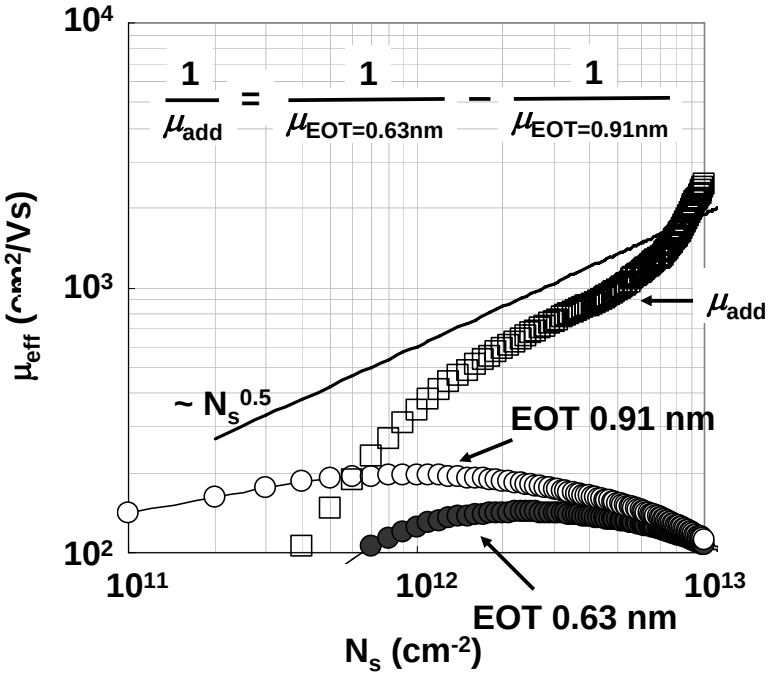

Figure 5.11 μ_{eff} comparison and the extracted component of $TaSi_2$/W/HfO_2 MOSFET. A relation of μ_{add}~$N_s^{0.5}$ is observed at low N_s region.

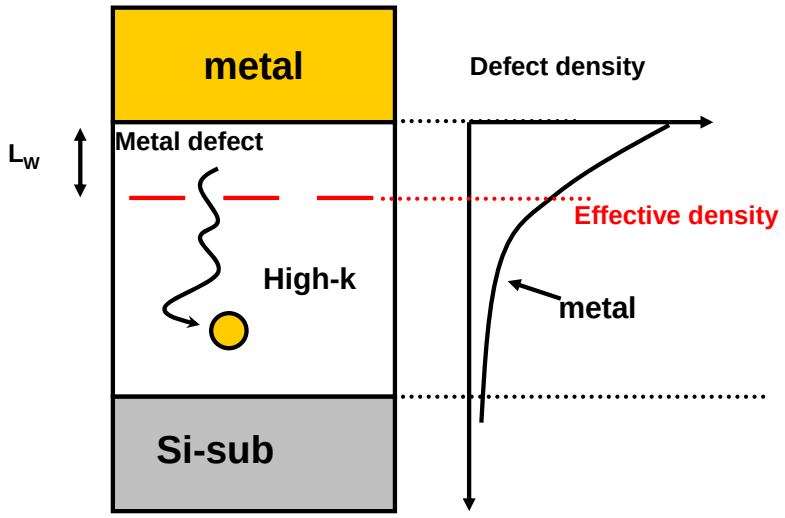

Figure 5.12 Gate metal diffusion and mobility degradation model.

In this model, gate metal diffuses to gate oxide and generates metal defects (fixed charge) and the metal defect generated in gate oxide is considered to be a scattering center which causes mobility degradation. Because the center of the effective density of this metal defect is placed at close to Si channel as the thickness of gate oxide becomes thin, electron mobility decreased as the EOT scaling. In this experiment, I fabricated two types of MOSFETs and found that in both electrodes, mobility decreased along with EOT downsizing.

I also compared electrical characteristics of MOS transistors with two different gate metals (shown in fig. 5.13). The EOT values are 1.1 nm in the W gate metal and 0.91 nm in the $TaSi_2$/W(5nm) gate each. Electron mobility of $TaSi_2$/W(5nm) gate is higher than that of W in small E_{eff} range although the EOT is smaller. This result shows that in the same EOT, $TaSi_2$/W(5nm)/HfO_2 MOS structure has an advantage in mobility compared with W. Considering that μ_{eff} degradation in small E_{eff} region is originated in

RCS, the difference of μ_{eff} in the different gate electrodes is caused by different amount of fixed charges in gate oxide.

Each MOS structure is shown in fig. 5.14. In the same EOT, MOSFET with $TaSi_2$/W(5nm) gate has thinner IL and thick HfO_2 film because the electrode supplies smaller amount of oxygen after PMA. There are two possibilities of the source of the mobility degradation. One is fixed charge in SiO_2 IL generated by PMA, thick IL could have larger amount of fixed charge. The other possibility is density of metal defects, in MOSFETs with different gate metals, the amount of metal defects might be changed. However I could not separate these two types of scattering centers.

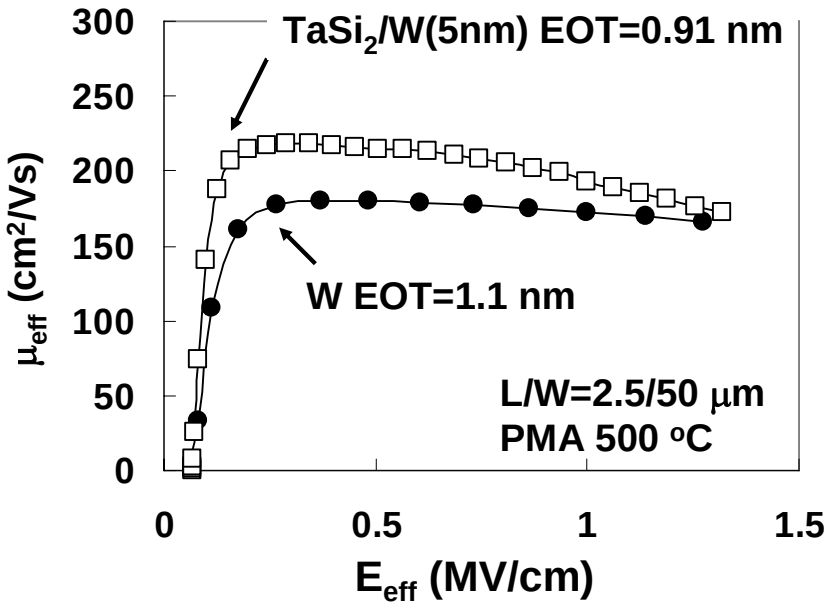

Figure 5.13 Electrical characteristics of MOS transistors with 2 different gate metals

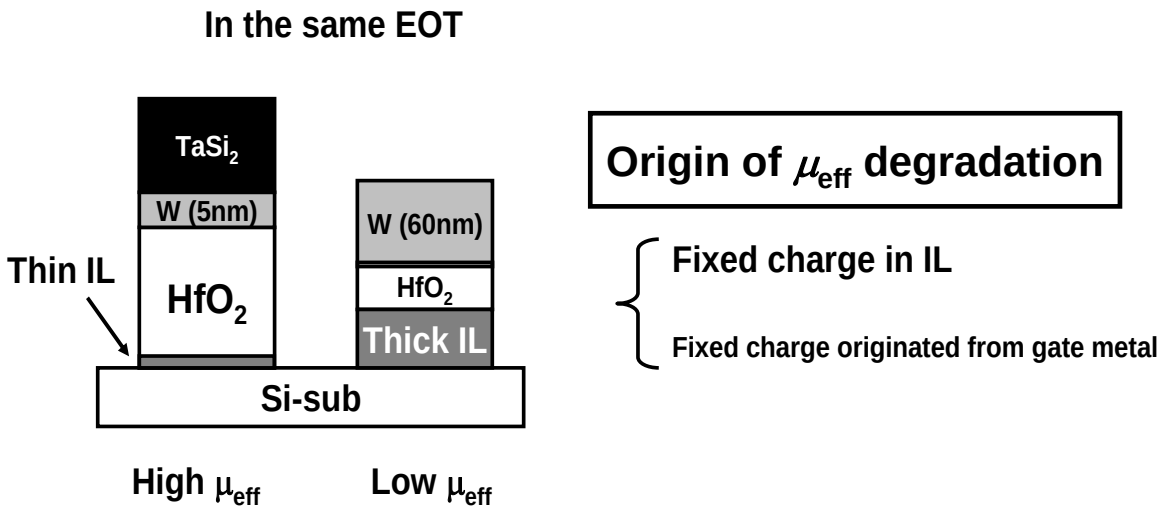

Figure 5.14 The same EOT HfO_2 MOSFET with different gate electrodes, W and $TaSi_2$/W (PMA 500 ^oC).

5.4 La_2O_3 single layer MOS capacitor with $TaSi_2$/W(5nm)

To investigate the limit of EOT downsizing, we fabricated La_2O_3 single layered MOS capacitor since La_2O_3 has advantage in leakage current compared with HfO_2. With $TaSi_2$(60nm)/W(5nm) gate electrode, EOT increase after PMA at 500 ^oC was not observed like experiments shown above. Figure 5.15 (a) shows CV characteristics of the MOS capacitor, 0.5 nm EOT was achieved even after PMA at 500 ^oC. However C-V hysteresis did not decrease after PMA. Figure 5.15 (b) shows J_g-V_g plot of the same EOT MOSCAPs with $TaSi_2$(60nm)/W(5nm)/La_2O_3 gate stack, gate leakage current varied widely although the EOT of these capacitors have almost the same values. This result implied that from the top electrode, Ta diffused to La_2O_3 and the amount of diffusion varied in each capacitor, the Ta diffusion was confirmed by EDX analysis (shown in fig 5-16(b)). We also confirmed that no SiO_2 IL was formed in this MOS structure by TEM image (shown in fig. 5.16(a)). To decrease C-V hysteresis keeping EOT 0.5 nm, I have to introduce Ta diffusion-blocking layer to W/La_2O_3 interface. Considering HfO_2/La_2O_3 stacked MOS capacitors had small C-V hysteresis, HfO_2 is one of the candidates for the Ta diffusion-blocking layer.

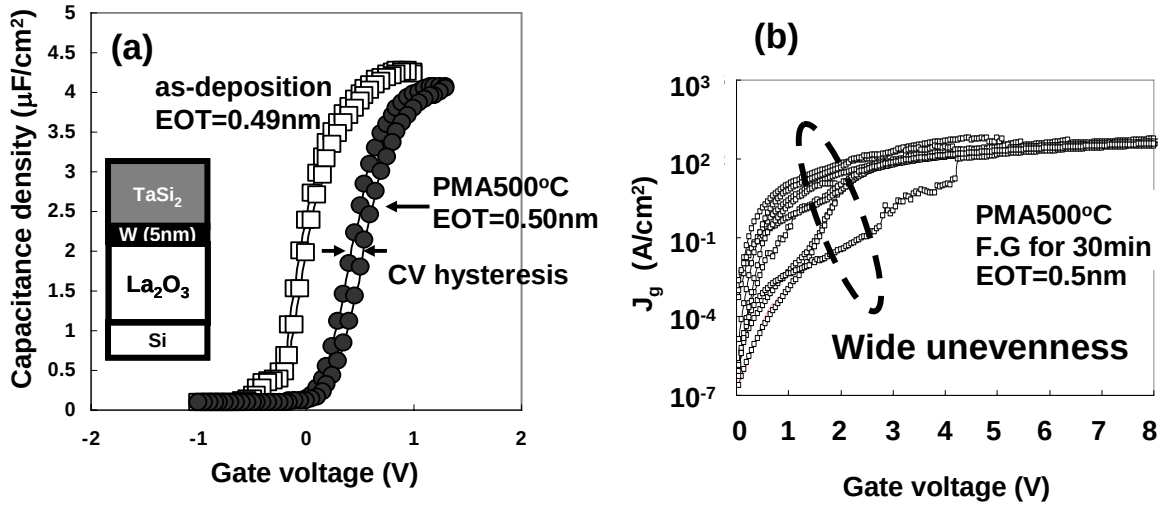

Figure 5.15 Electrical characteristics of La_2O_3 MOS capacitors with $TaSi_2$ (60nm)/W (5nm) gate electrodes. (a) C-V characteristics of the MOSCAPs before and after PMA. (b) J_g-V_g plot of the capacitors after PMA at 500 ^oC.

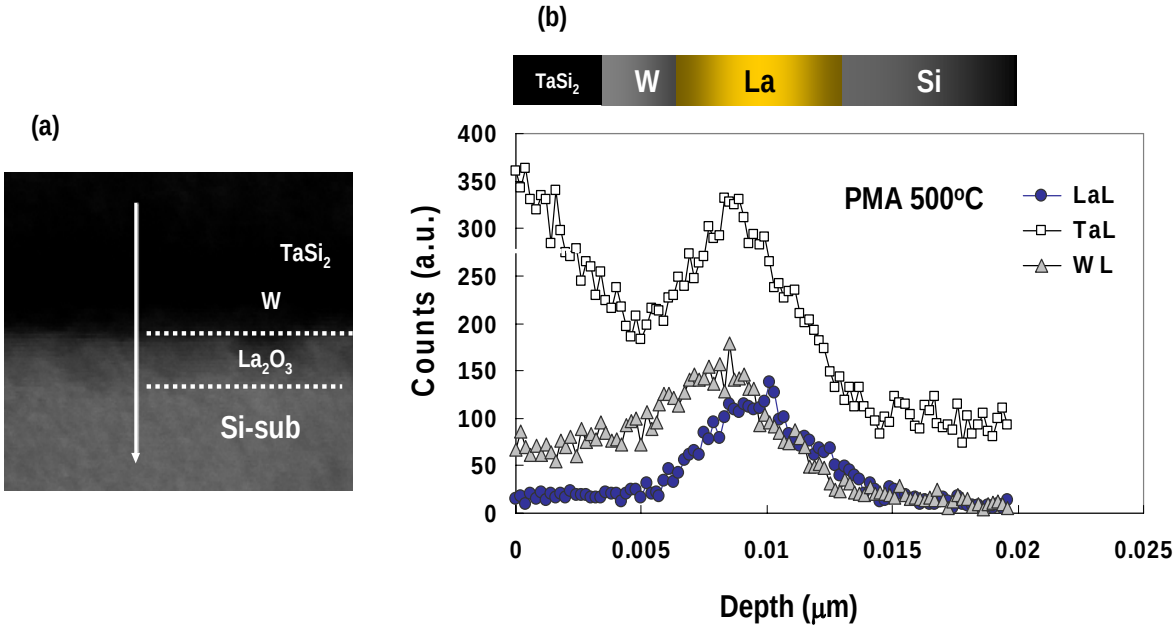

Figure 5.16 (a) TEM image and (b) EDX analysis; we can see that W and Ta diffused into La_2O_3 layer from gate electrode after PMA500 ^oC.

5.5 Summary

In chapter 5, I experimentally found that oxygen supply control by proper selection of gate electrode is one of the effective ways for small EOT and small C-V hysteresis in the gate-last-MOSFET. EOT increase (SiO_2 IL growth) after PMA is caused by oxygen supply from the W gate electrode deposited by RF sputtering and the amount of oxygen included in the W gate electrode revealed to be enough to grew IL from SIMS analysis. It revealed that thin W gate and $TaSi_2$ capping layer could dramatically reduce EOT growth after PMA and 5 nm W insertion was thin enough to suppress EOT growth. Figure 5.17 shows the summary of $TaSi_2$(60nm)/W(5nm) with various gate oxide structures. Because La_2O_3 has an advantage in leakage current, La_2O_3 could achieve the smallest EOT (= 0.5 nm). On the other hand, C-V hysteresis caused by Ta diffusion from $TaSi_2$ is serious problem in this stacked structure.

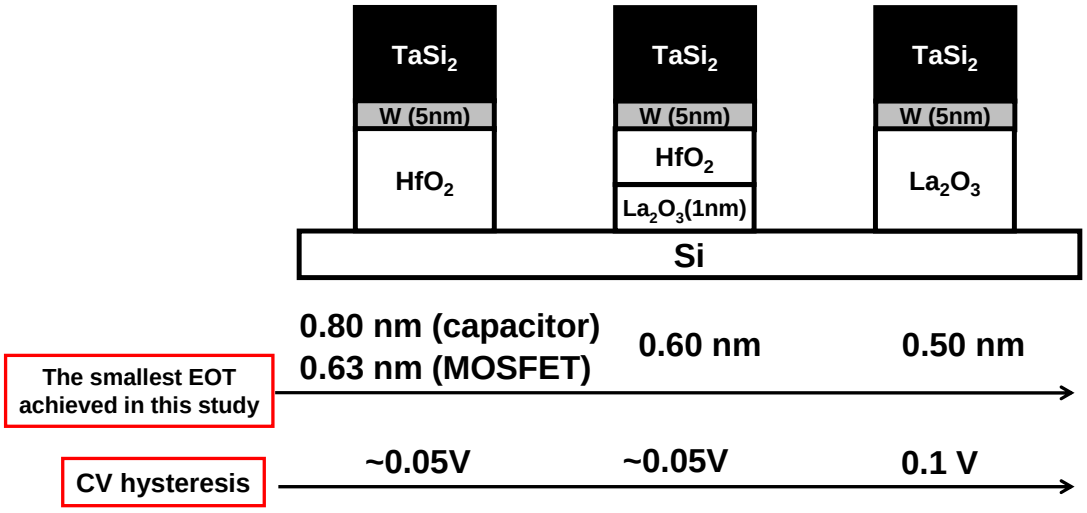

Figure 5.17 Summary of the $TaSi_2$(60nm)/W(5nm) with various gate oxide structures.

5.6 References

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Chapter 6. Introduction of high-k with higher κ value

6.1 Introduction

In chapter 5, I proposed oxygen control gate electrode using W and $TaSi_2$ and fabricated sub-1nm MOSFET with HfO_2 gate insulator in gate-last-process and found that we can achieve 0.5 nm EOT MOS structure with La_2O_3 by proper choice of gate metal.

In this chapter another approach for 0.5 nm EOT transistors is proposed, introduction of CeO_2 and SrO which have high dielectric constant compared with HfO_2 or La_2O_3 [1]. High dielectric constant insulator could achieve small EOT keeping its oxide physical thickness thick with reduction of direct tunneling gate leakage current and the small J_g MOSFET can achieve small EOT MOSFET. In this experiment, we fabricated La_2O_3/CeO_2 and $SrO/La_2O_3/CeO$ stacked layer nMOSFET and investigated its electrical characteristics.

6.2 Electrical characteristics of La_2O_3/CeO_2 MOSFET

In this experiment, I fabricated La_2O_3/CeO_2 stacked nMOSFET in gate-last-process. Fabricated transistors were shown in fig. 6.1. 1 nm thick CeO_2 film was deposited on Si and 1 nm to 3 nm La_2O_3 was deposited on CeO_2. W was used as gate electrode, because CeO_2 has large dielectric constant (= 30), EOT after PMA might be small even W gate supply oxygen to the insulator. Figure 6.2 and 6.3 shows the MOSFET characteristics of the smallest EOT transistor. In La_2O_3/CeO_2 stacked structure we achieved 0.51 nm EOT in gate-last-process. Considering that the EOT is 0.5 nm after PMA 500 ^oC, no IL seems to be formed in the interface and aftrer PMA, the MOS structure may be La_2O_3/Ce-silicate stack. In addition, from C_{gc} curves, no C-V hysteresis was observed thanks to oxygen supply from the W gate.

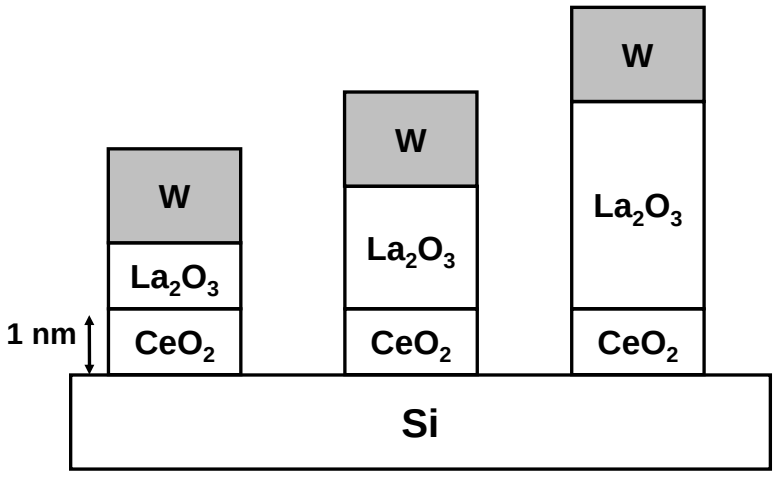

Figure 6.1 Schematic illustration of fabricated La_2O_3/CeO_2 stacked MOSFET. All MOSFETs were annealed at 500 ^oC.

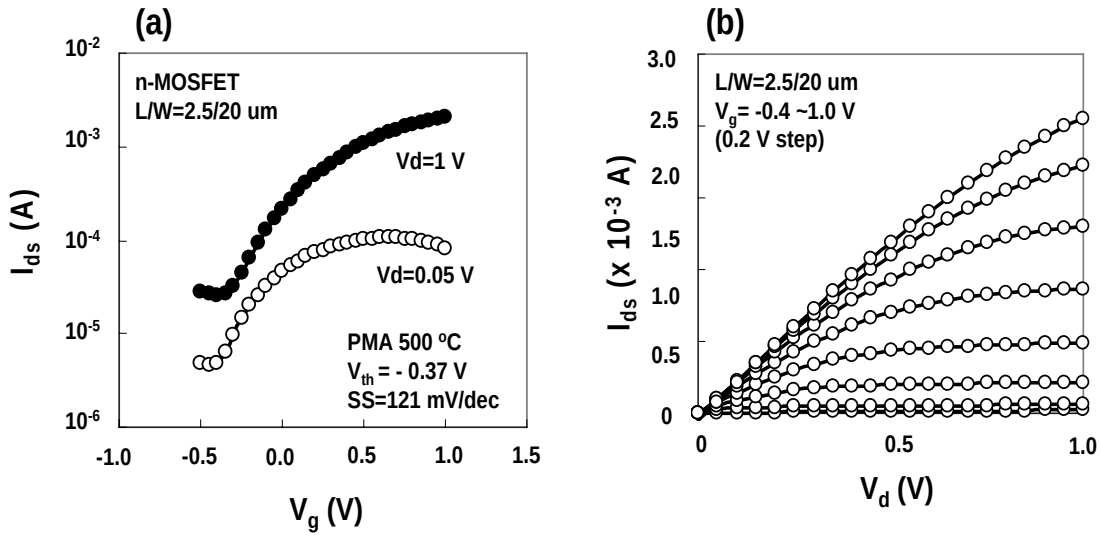

Figure 6.2 Electrical characteristics of La_2O_3/CeO_2 stacked nMOSFET (a) I_d-V_g plot and (b) I_d-V_d plot.

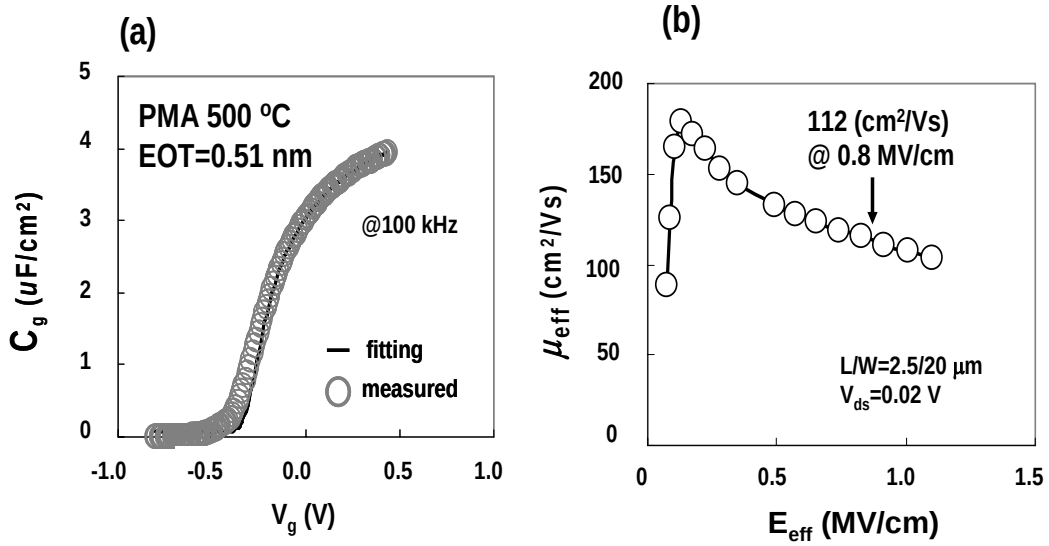

Figure 6.3 Electrical characteristics of La_2O_3/CeO_2 stacked nMOSFET (a) C_{gc} plot and (b) mobility plot.

Figure 6.4 shows J_g-EOT plot of La_2O_3/CeO_2 and La_2O_3 nMOSFET. Clearly the leakage current of La_2O_3/CeO_2 stacked MOSFET is smaller compared with La_2O_3 single layer FET. This is because La_2O_3/CeO_2 MOS structure could keep physical thickness thick thanks to high dielectric constant of CeO_2, at the same time wide band gap of La_2O_3 also reduce J_g [1]. So, to reduce J_g and achieve small EOT, La_2O_3/CeO_2 stacked structure is effective. Figure 6.5 shows μ_{eff}-EOT plot of La_2O_3/CeO_2 and La_2O_3 nMOSFET, the mobility decreased along with EOT scaling. (written in Chapter 5).

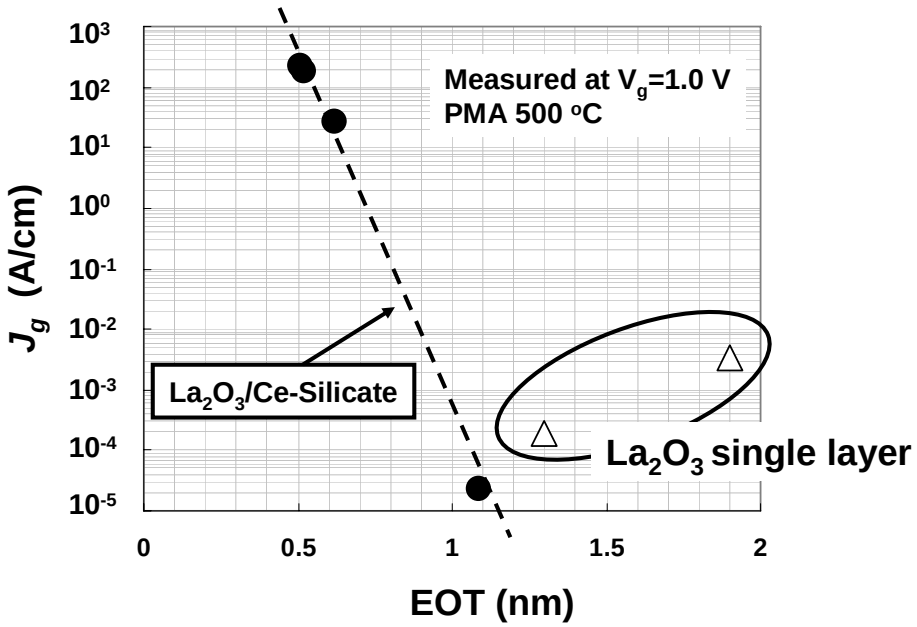

Figure 6.4 J_g-EOT plot of La_2O_3/CeO_2 and La_2O_3 nMOSFET; J_g was measured at V_g=1 V

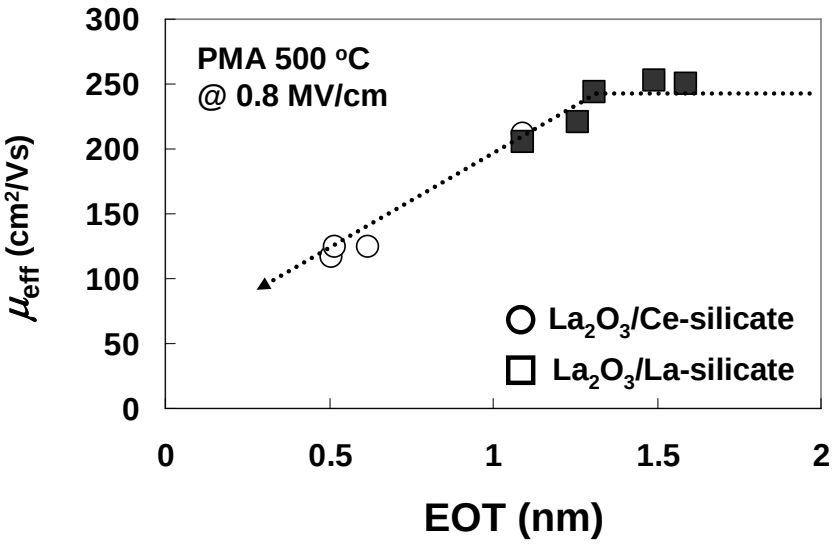

Figure 6.5 μ_{eff}-EOT plot of La_2O_3/CeO_2 and La_2O_3 nMOSFET; mobility decreased along to EOT scaling

6.3 MOSFET characteristic change by SrO capping

SrO is one of the candidates for gate insulators because it has large dielectric constant by mixing with Ti (dielectric constant of $SrTiO_3$ is over 100). In this chapter, I capped SrO on La_2O_3/CeO_2 stacks for further scaling. Figure 6.6 shows fabricated transistors. The thickness of CeO_2 bottom layer was set to 1 nm and capped SrO layer was 1 nm, La_2O_3 thickness was changed from 0.5 nm to 1 nm. All MOSFETs were annealed at 500 ^oC to confirm thermal endurance in gate-last-process. Figure 6.7 and 6.8 shows the MOSFET characteristics of the smallest EOT transistor. In $SrO/La_2O_3/CeO_2$ stacked structure we achieved 0.49 nm EOT in gate-last-process. In this structure, no C-V hysteresis was observed from its C_{gc} curve.

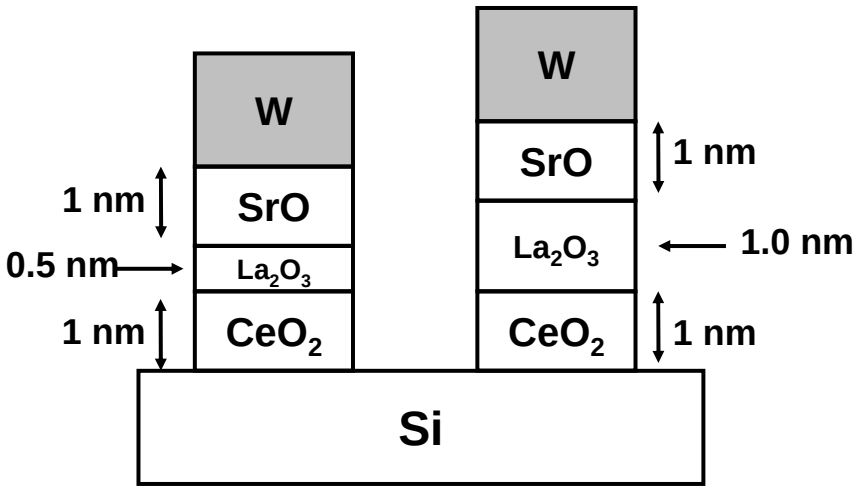

Figure 6.6 Schematic illustration of fabricated La_2O_3/CeO_2 stacked MOSFET with SrO cap. All MOSFETs were anneled at 500 ^oC.

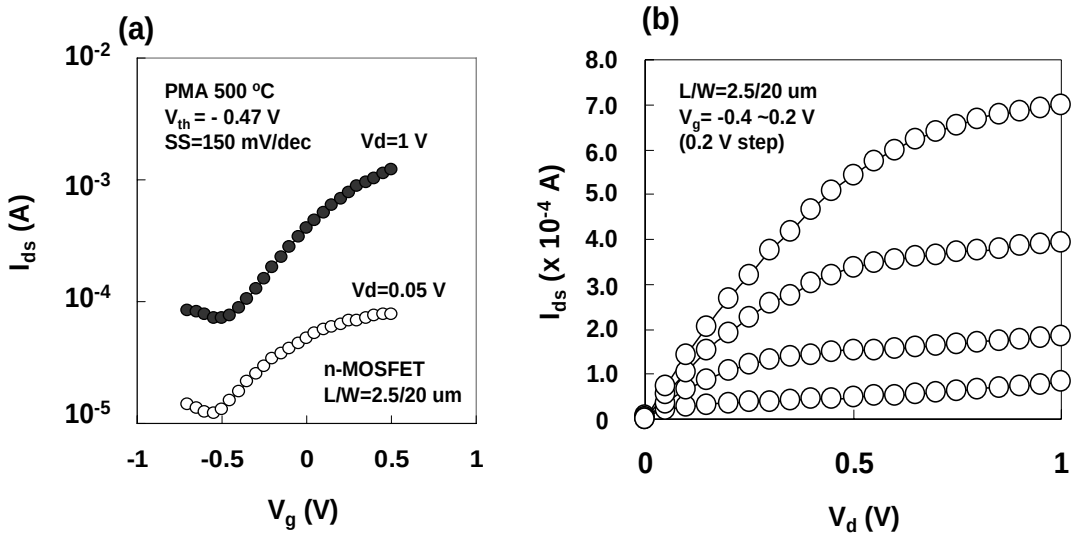

Figure 6.7 Electrical characteristics of $SrO/La_2O_3/CeO_2$ stacked nMOSFET (a) I_d-V_g plot and (b) I_d-V_d plot.

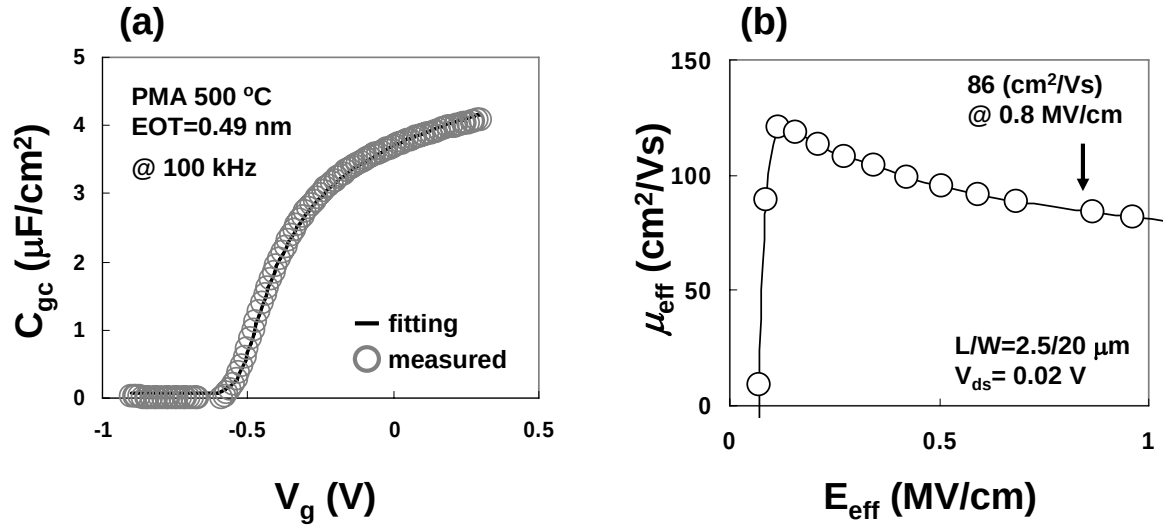

Figure 6.8 Electrical characteristics of $SrO/La_2O_3/CeO_2$ stacked nMOSFET (a) C_{gc} plot and (b) mobility plot.

6.4 Summary

In this chapter, CeO_2 and SrO were introduced as MOSFET gate insulators and it was found that both high-k materials could achieve EOT around 0.5 nm even after PMA 500 ^oC. So, to increase effective dielectric constant by introducing CeO_2 or SrO is an effective way to achieve small EOT because we can reduce direct tunneling current. Figure 6.9 shows cross sectional TEM image and EDX analysis of SrO/CeO_2 MOS capacitor with W gate electrode. We can see that no SiO_2 layer grown at the IL and Sr diffused to the interface. Figure 6.10 shows schematic illustration of gate oxide structure change before and after PMA 500 ^oC. In W/La_2O_3, La-silicate layer (k = 9) grew after PMA. On the other hand, La_2O_3/CeO_2 and $SrO/La_2O_3/CeO_2$ MOS structures have silicate layer with higher dielectric constant compared with La-silicate. So, Ce-silicate and Sr doped Ce-silicate can make physical thickness of gate oxide thick compared with La_2O_3 single layer MOS structure and have an advantage in decreasing leakage current. So, as the dielectric constant of gate oxide increase, we can achieve smaller EOT MOSFET.

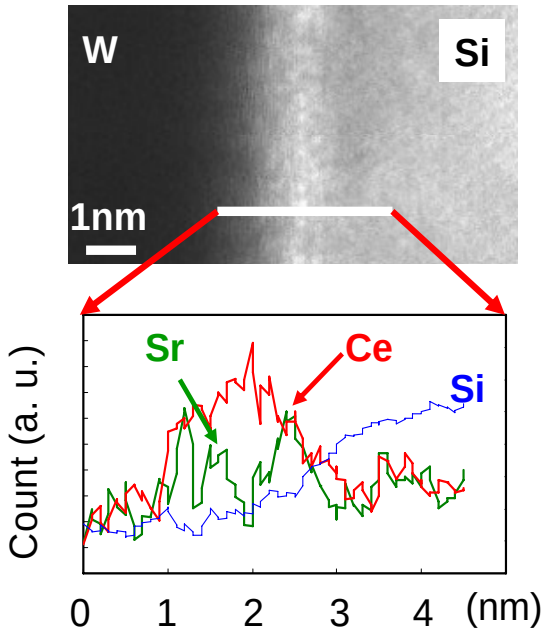

Figure 6.9 TEM image and EDX line profile of SrO/CeO_2 MOS capacitor.

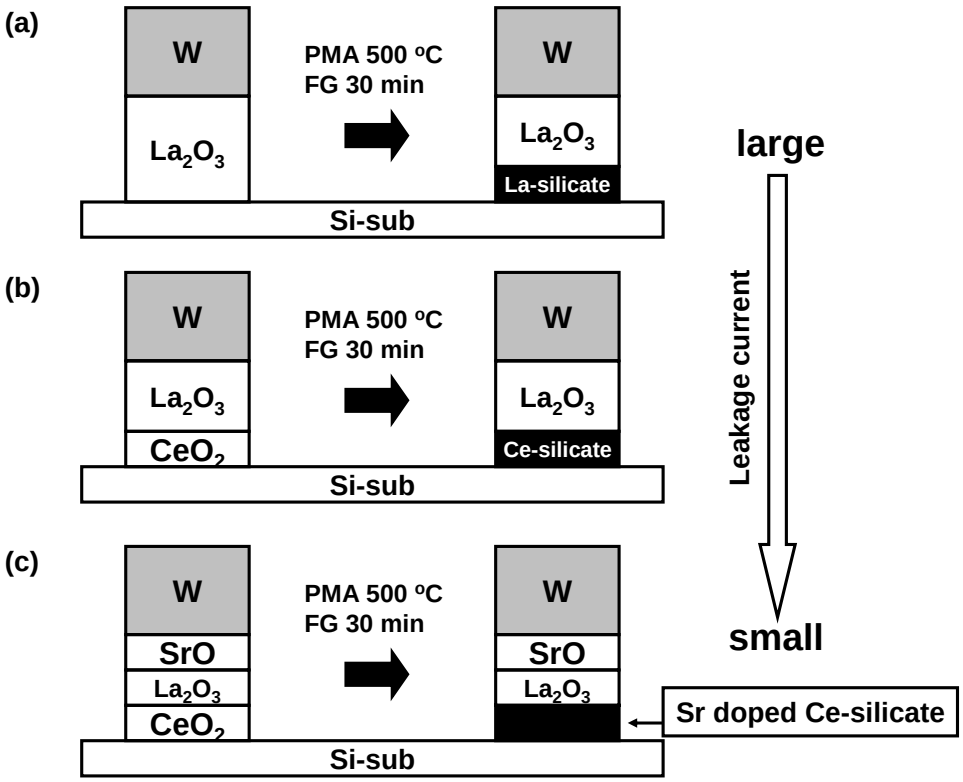

Figure 6.10 Schematic illustration of gate oxide structure changes before and after PMA.

I also fabricated sub-1nm MOSFET using CeO_2 and SrO. Figure 6.11 shows J_g-EOT plot of each structure MOSFET. As can be seen, CeO_2 and SrO have an advantage in leakage current and realize small EOT after PMA 500 ^oC. Figure 6.12 shows mobility-EOT plot of these structures compared with transistors reported in IEDM symposium. From the figure, MOSFET with SrO capping have smaller electron mobility compared with MOSFET without SrO cap. This result shows that SrO which was diffused to Si interface could be a scattering center and reduce its electron mobility. So, proper control of the thickness of SrO cap is important for small leakage current and high mobility MOSFET.

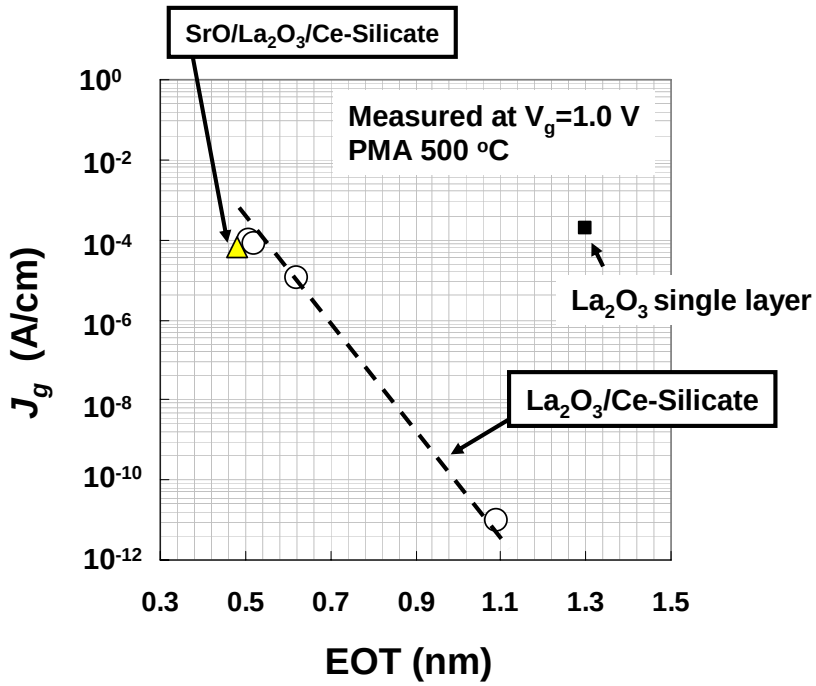

Figure 6.11 J_g-EOT plot of each structure MOSFET; CeO_2 and SrO have advantage in leakage current.

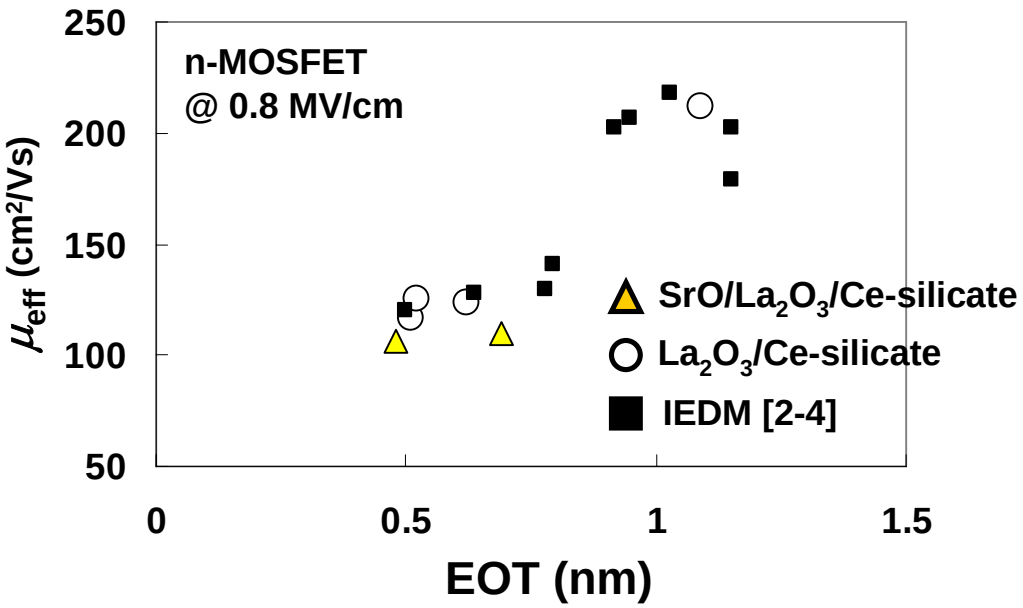

Figure 6.12 Electron mobility-EOT plot of this work and transistors reported in IEDM symposium.

6.5 References

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Chapter 7. Conclusion

7.1 Conclusion

In this work, the ways to fabricate sub-1nm EOT n-channel MOSFET with gate-last-process are proposed. Figure 7.1 shows a guideline for gate metal and gate insulator selection. Proper choice of gate metal and gate insulator is important for 0.5 nm EOT MOSFET with small leakage current and small C-V hysteresis.

In the gate metal, I used $TaSi_2$, W and found that oxygen supply from W causes IL formation in PMA. However, without W, C-V hysteresis becomes large. From this result, oxygen supply and silicate growth are important for gate-insulator-defect recovery. So, proper control of the oxygen supply by changing W thickness is necessary to achieve small EOT and small C-V hysteresis at the same time. On the other hand, gate insulator selection is also important for sub-1nm EOT transistors. As HfO_2 easily forms SiO_2 IL after PMA 500 ^oC with W gate electrode. Rare earth oxide such as La_2O_3 and CeO_2 which form no SiO_2 layer is one of the promising candidates for high-k/Si directly contacted MOSFET gate insulator. Considering that CeO_2 has large dielectric constant compared with La_2O_3, high-k film on a Si-substrate should be Ce-silicate because Ce-silicate could achieve small EOT keeping its physical thickness thick thanks to its higher κ value compared with La-silicate. In this study, I also confirmed that SrO capping on rare earth oxide can make silicate layer dielectric constant high.

I fabricated sub-1nm n-MOSFETs using the guideline and carefully examined the electron mobility. Figure 7.2 shows mobility-EOT plot in sub-1nm region. The mobility degradation along with EOT scaling is observed in all transistors. In Chapter 5, I found that the mobility degradation is due to remote coulomb scattering (RCS) and one of the sources which make the mobility small is metal defects. And the choice of gate metal

and insulator could reduce the fixed charge and suppress mobility degradation.

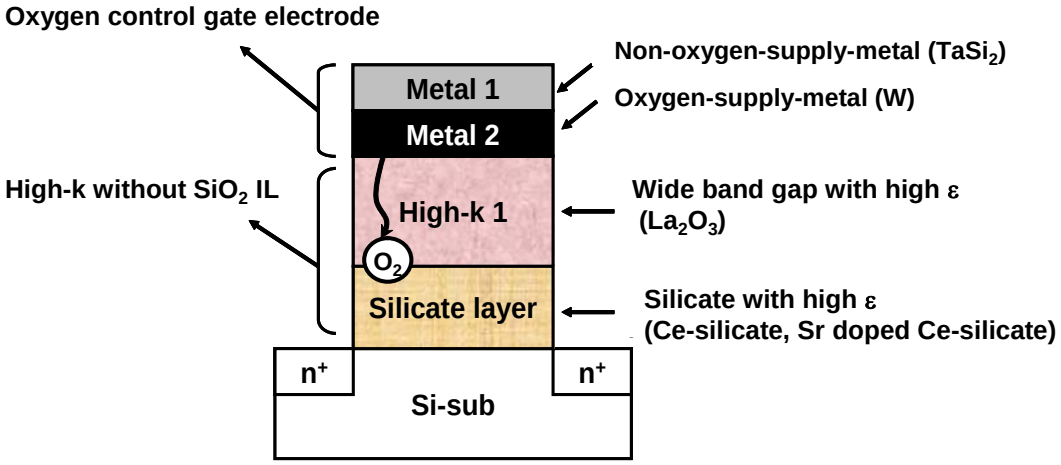

Figure 7.1 Guideline for gate metal and gate insulator selection for 0.5 nm EOT MOSFET.

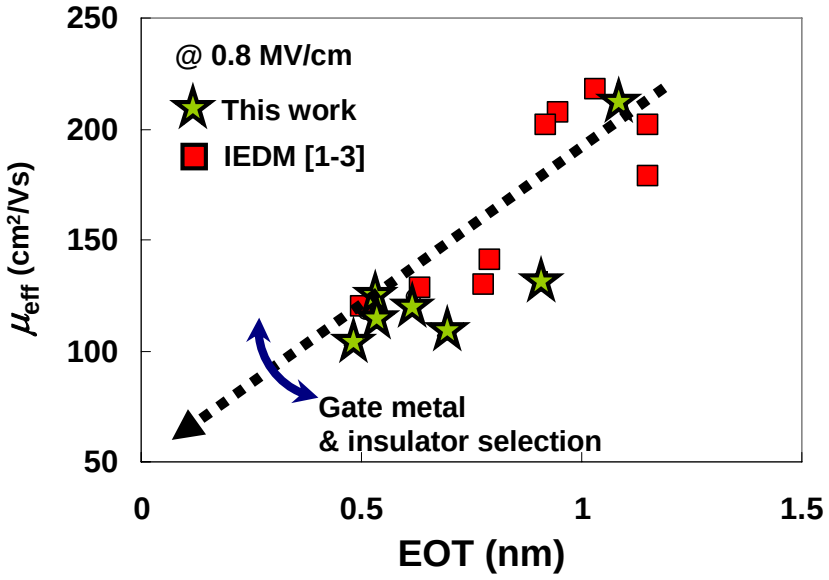

Figure 7.2 Electron mobility-EOT plot in sub-1nm region. Mobility degradation can be tuned by the selection of metal and insulator.

7.2 Recommendation for future work

In this study, I proposed the materials guideline for sub-1nm EOT MOSFET and mainly focused on J_g and CV-hysteresis. However there are many obstacles to overcome, one is the V_{th} control. In the small EOT MOSFETs of my study using rare earth oxide such as $SrO/La_2O_3/CeO_2$ and La_2O_3/CeO_2 has negative V_{th}, -0.47 V and -0.37 V each. Considering the gate length is 2.5 μm in this study, V_{th} values decreased further with L_g scaling due to the short channel effect. Gate metal selection based on work function is one of the solutions. I think new high-k material introduction with proportion of interface dipoles (shown in chapter 3) is the key to realize proper V_{th} control.

7.3 References

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