Master Thesis

A Study of Schottky Barrier Height Modulation by Metal Insertion and Its Application to SB-MOSFETs

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Chapter 1

INTRODUCTION

1.1 Background of This Study

About a half century ago, W. Brattain, J. Bardeen and W. Shockley succeeded in inventing the first transistor in 1947. Then, an integrated circuit (IC) is made by J. Killby in 1948. After the invention of the IC, the numbers of transistors included in a chip have increased according to Moore's law and the semiconductor technologies have accomplished wonderful development.

CMOS (Complementary Metal Oxide Semiconductor) technology evolution in the past years has followed the path of device scaling for achieving density, speed, and power improvements. MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) scaling was propelled by the rapid advancement of lithographic techniques for delineating fine lines of 1μm width and below.

In the constant-field scaling theory, it was proposed that one can keep short-channel effects under control by scaling down the vertical dimensions (gate insulator thickness, junction depth, etc.) along with the horizontal dimensions, while also proportionally decreasing the applied voltages and increasing the substrate doping concentration (decreasing the depletion width). This is shown schematically in Fig. 1.1. The principle of constant-field scaling lies in scaling the device voltages and the device dimensions (both horizontal and vertical) by the same factor, $\kappa(>1)$, so that the electric field remains unchanged. This assures that the reliability of the scaled device is not worse than that of the original device. Table 1.1 shows the scaling rules for various device parameters and circuit performance factors. The doping concentration must be increased by the scaling factor κ in order to keep Poisson's equation invariant with respect to scaling.

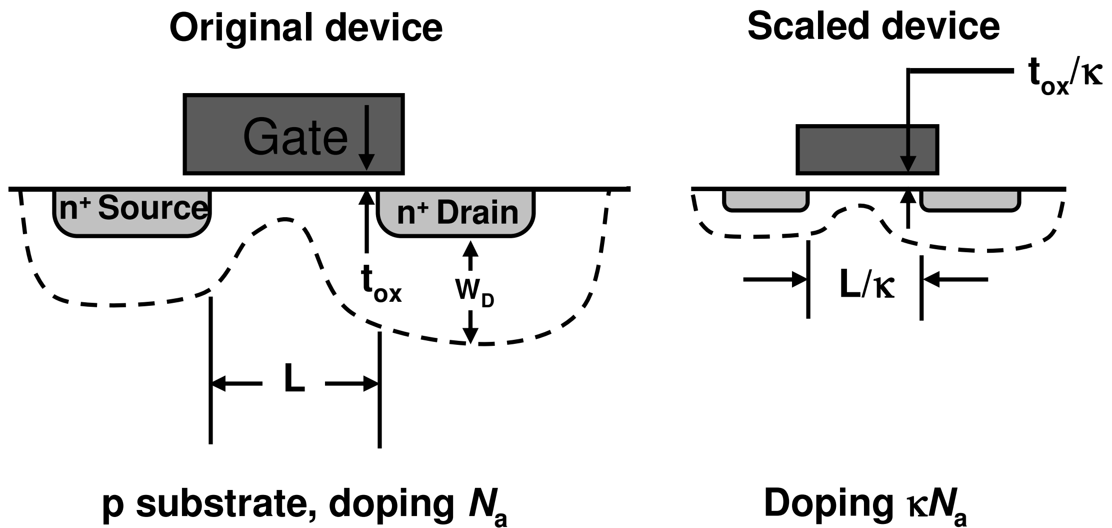


Fig. 1.1 Principles of MOSFET constant-electric-field scaling

Table 1.1 Scaling of MOSFET Device and Circuit Parameters

	MOSFET Device and Circuit Parameters	**Multiplicative Factor (κ>1)**
Scaling assumptions	Device dimensions(tox, L, W, χj)	$1/\kappa$
	Doping concentration (Na, Nd)	κ
	Voltage (V)	$1/\kappa$
Derived scaling behavior of device parameters	Elecric field (ξ)	1
	Carrier velocity (υ)	1
	Depletion –layer width (Wd)	$1/\kappa$
	Capacitance (C=εA/t)	$1/\kappa$
	Inversion-layer charge density (Qi)	1
	Current, drift (I)	$1/\kappa$
	CRchhannel resistance (Rch)	1
Capacitance behavior of circuit Power parameters	Circuit delay time (τ~CV/I)	$1/\kappa$
	Power dissipation per circuit (P~VI)	$1/\kappa^2$
	Power-delay product per circuit (Pτ)	$1/\kappa^3$
	Circuit density (∞ 1/A)	κ^2
	Power density (P/A)	1

The gate length of MOSFET came to be smaller than 100nm since the year of 2000 and 32nm for the year of 2005 as shown in Fig. 1.2 according to the ITRS roadmap 2007 update [1]. With continuous scaling of device dimensions, IC performance is becoming more and more dependent upon the parasitic series resistance of the source/drain junctions and their contacts.

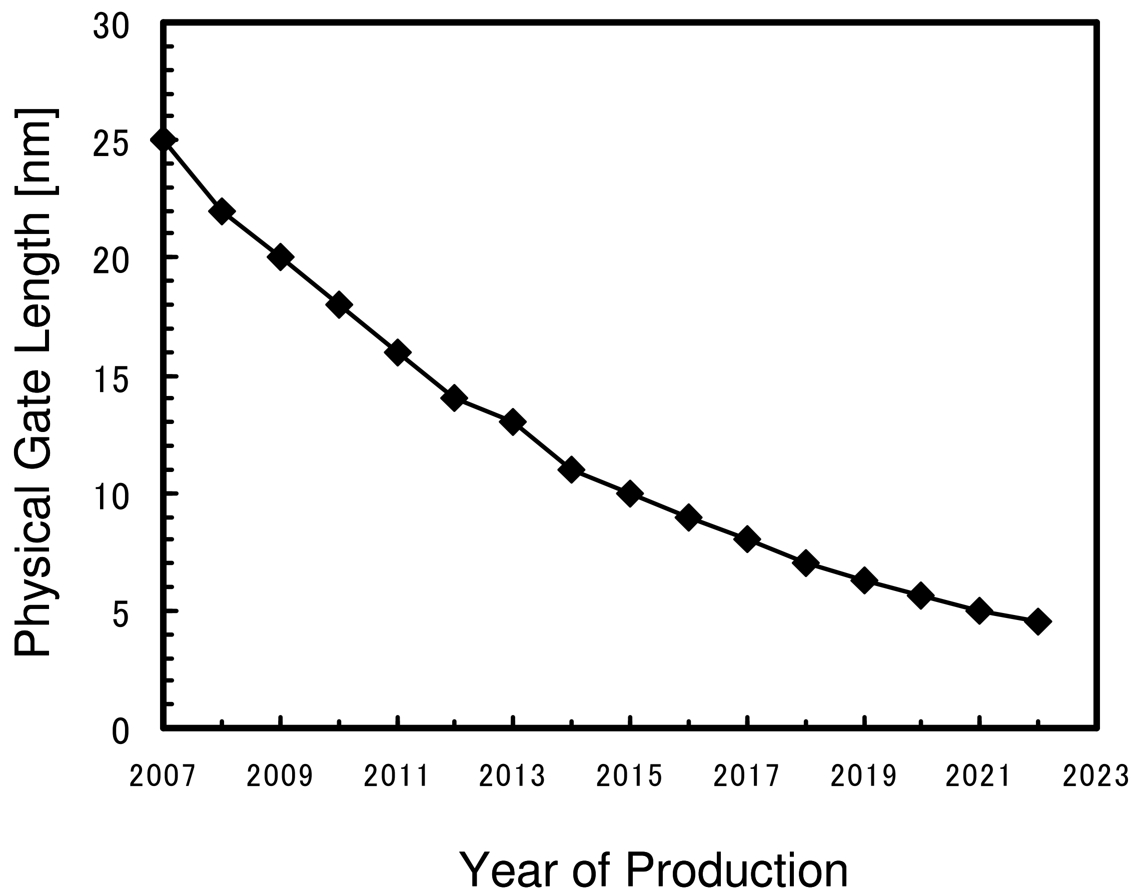


Fig. 1.2 the International Technology Roadmap for Semiconductors (2007 update)

1.2 Problem of Transistors in The Future VLSI

The physical limit comes for the scaling. Now, the biggest problem is the scaling of the gate oxide. The scaling of gate oxide for improving MOSFET performance is required. A few nm gate oxide technique is required, but the present SiO_2 range doesn't suppress the gate leakage current. This limit is said to be 1.2-1.5nm. The recent research for this problem uses high-k dielectric which k value is higher than that of the conventional SiO_2. If we use the material which k value is five times lager, we can obtain the same capacitance with the physical oxide thickness five times larger. However, we require that k is higher than 10, the band is higher than 1eV and the thermal stability, single crystal or amorphous, and small defect density are needed. The scaling of gate oxide is proceeding, it is not ignored that capacitance. That is to say, it is inversion capacitance of the channel surface and depletion conductance of polysilicon for the gate electrode. The inversion capacitance is not ignored. The problem of the depletion capacitance of the gate electrode is controlled the high gate impurity concentration. However, its limit comes up. Thinking for the measure is to use the polysilicon gate in stead of metal gate. The scaling has the problem of thin junction depth in source and drain range. The junction depth in source and drain for the scaling requires shallower junction depth. But the shallow junction profile has high resistance. The source and drain high impurity concentration makes the resistance low. This problem's limit also comes up.

1.3 Schottky Barrier MOSFET

In the previous section, it is explained that the VLSI is forced with various problems. In order to solve the problems, the various methods have been proposed so far. In these proposals, the schottky barrier MOSFET is suggested by S.M.Sze in 1968 [2]. The conventional MOSFET and schottky barrier MOSFET are compared in Fig. 1.3.

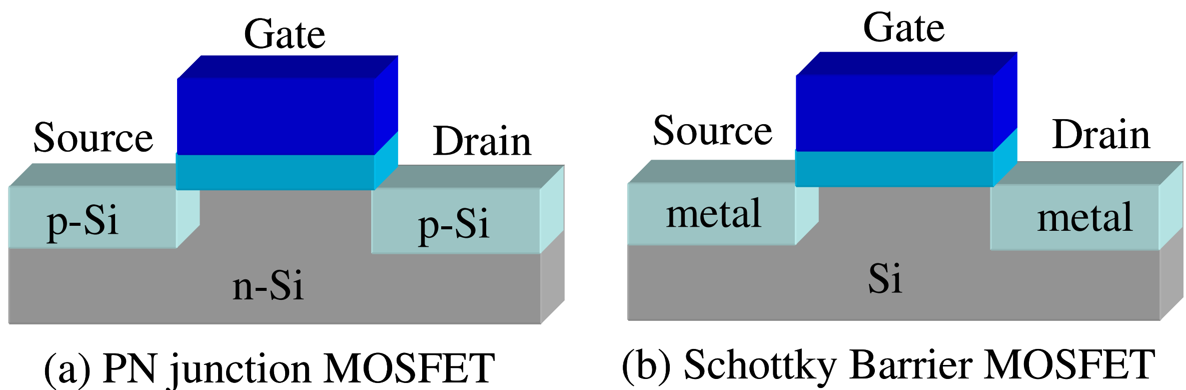


Fig. 1.3 The conventional n-MOSFET and schottky barrier MOSFET

The schottky barrier MOSFET adopts alloy of Si and metal that called silicide in source and drain region. The schottky barrier MOSFET formed schottky contacts in Si and silicide interfaces and operates as well as the conventional MOSFET. The next paragraphs show advantages and issues of the schottky barrier MOSFET.

Advantages

1. As the junction depth becomes smaller, the sheet resistance becomes higher. However, in terms of scaling, we need to have lower sheet resistance as well as smaller junction depth. For the solution of this problem, Schottky barrier MOSFET is considered. [3,4]

2. The schottky barrier MOSFET can be fabricated with a low temperature process compared with the conventional MOSFET.

3. The schottky barrier MOSFET does not require to form diffusion region in source and drain. That can permit scaling down the device area. The integration of circuit can be raised.

4. The doping in channel region does not need to increase in order to reduce depletion length as in the conventional MOSFET. The problem that means diffusion of impurity by short channel effect is avoided.

Issues

1. The drive current is limited by schottky barrier height. Because higher schottky barrier height rapidly increases parasitic resistance. [5,6]

2. The schottky barrier MOSFET has a higher leakage current than the conventional MOSFET because of tunneling current between Si the substrate and the silicide layer.

1.4 Silicide for Schottky Barrier MOSFET

Silicide materials I using for schottky barrier MOSFET are listed table 1.2.

Table1.2 Silicide material for schottky barrier MOSFET

Silicide	Schottky Barrier Height (eV)
NiSi	0.65～0.75
ErSi	0.27～0.36
HfSi	0.46～0.50

The Er silicide has been proposed for n-channel schottky barrier MOSFET because of very low schottky barrier height of 0.27-0.36eV for electrons. [7] And the reported schottky barrier height of Hf silicide is 0.46-0.50eV for electrons. [8] On the other hand, the schottky barrier height of Ni silicide is around middle gap of Si. It's 0.65-0.75eV for electron and hole. Though Ni silicide has a middle gap of Si, it has advantages for schottky barrier MOSFET. Ni silicide has a very low resistance compared with other materials as shown Fig. 1.4. And the other characteristics of Ni silicide are low Si consumption, low temperature for silicidation and lack of narrow-width effect.

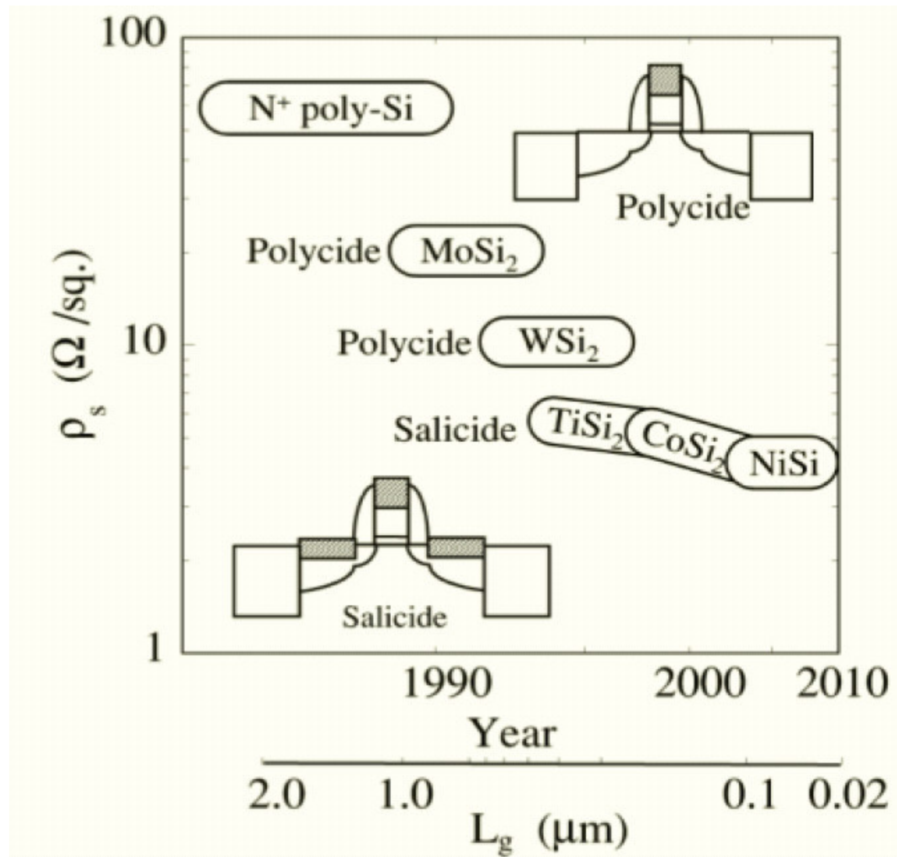


Fig. 1.4 resistance of various silicide [9]

1.5 Purpose of This Study

In this work, we investigated Φ_b modulation of Ni silicide which has good characteristics (Low Si consumption, Low temperature for silicidation and lack of narrow-width effect) by inserting an Er or Hf interlayer at the Ni/Si interface before silicidation, and applied the technique to n-channel SB-MOSFETs fabrications.

Chapter 2

SCHOTTKY BARRIER DIODE AND MOSFET

2.1 Schottky Diode

In the case of metal and silicon contact, the potential that is called schottky barrier height is formed metal and silicon interface that is the same commutation characteristics of pn junction. The work function of metal and semiconductor is ϕ_m and ϕ_σ ,respectively, and the electron affinity is χ . When the relationship $\phi_m > \phi_\sigma > \chi$ among ϕ_m,ϕ_σ and χ is defined $\phi_m > \phi_\sigma > \chi$, the schottky barrier height is

$$\phi_B = \phi_m - \chi \,. \quad (2.0)$$

The commutation is appeared from this potential. But, in fact the schottky barrier height is measured that dose not depend against metal work function ϕ_m. In generalization, the dependence on work function is small against ideal it. That reason is existence interfacial trap and interfacial layer. A lot of model are suggested in relationship among Fermi level pinnning. In this case, the only ideal case is considerd. The transportation structure pass through thermal electron emission obtains over the potential and tunneling structure pass through schottky potential as shown in Fig. 2.1.

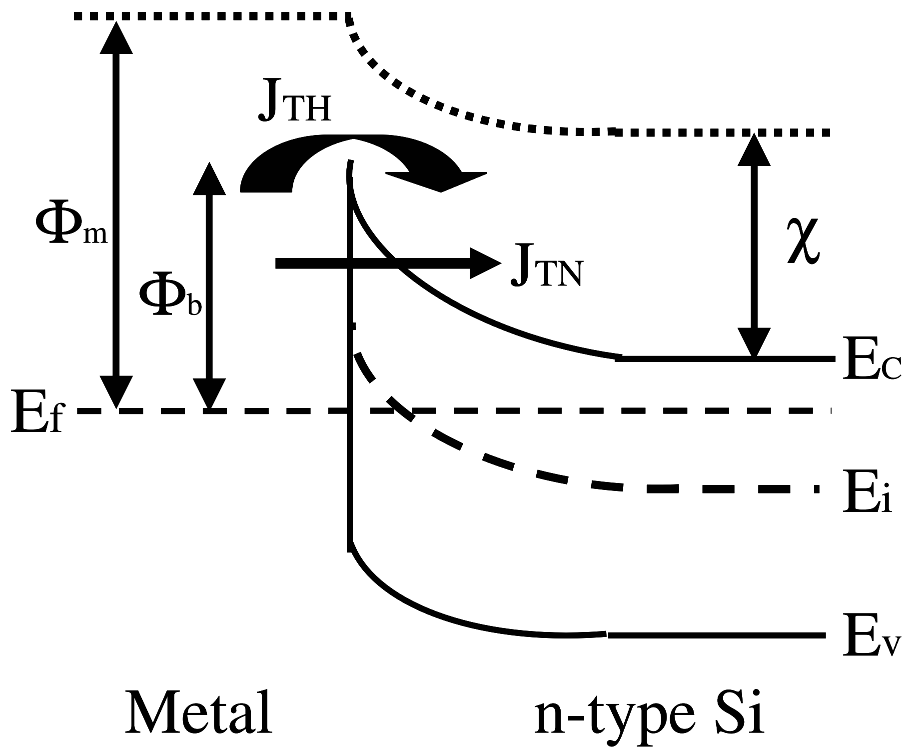


Fig. 2.1 schematic illustration of schottky diode band diagram [10]

2.1.1 Thermal Electron Emission Structure

It is mentioned thermal emission structure. First of all, the electron current j_2 is considered about from semiconductor to metal as shown in Fig. 2.2. The electron does not collision in distance of space electron charge layer. The electron current pass over this layer to metal. The electron emission metal is higher electron energy than E_0 as shown Fig. 2.2.

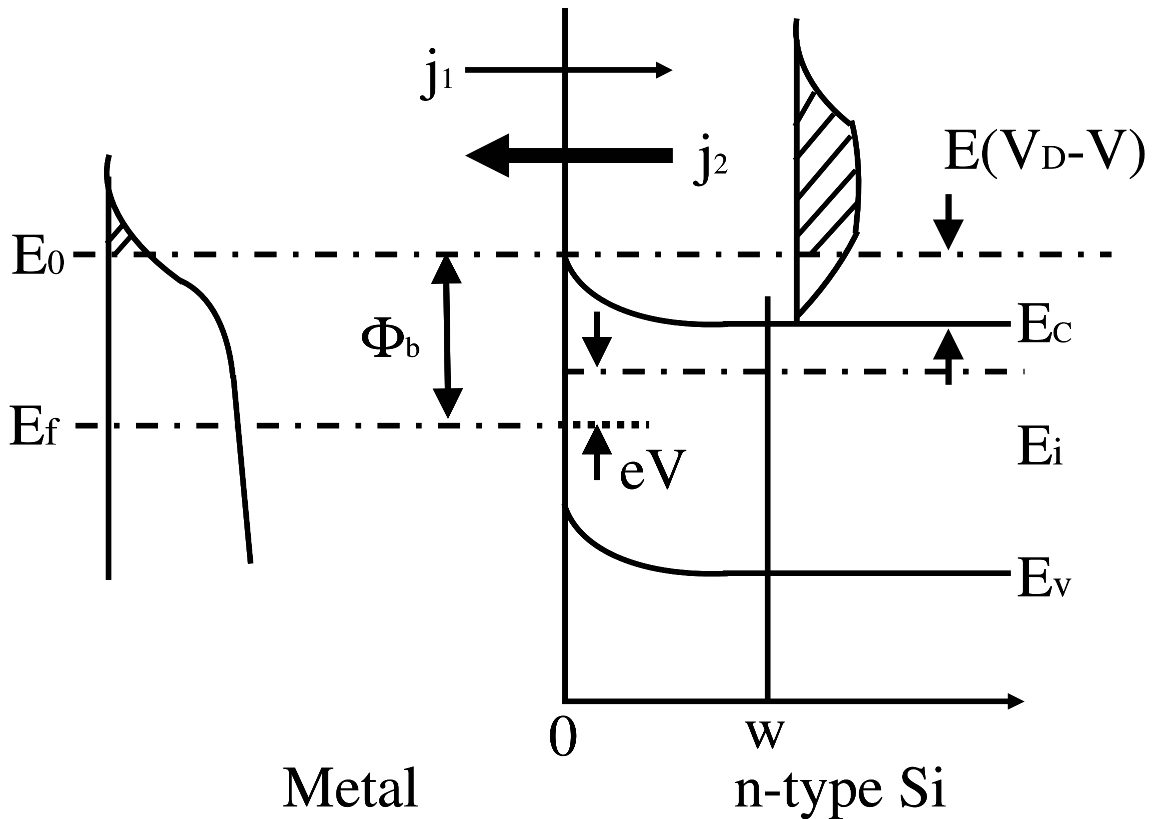


Fig. 2.2 schematic illustration of rectification of schottky contact [10]

$$j_2 = -\int v_x dn = -\int_{j_x>0} V_x \cdot Z(E) f(E) dE$$

$$= -\int_0^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} v_x \cdot 2\frac{1}{8\pi^3} \cdot f(E) dk_x dk_y dk_z$$

$$= -\frac{1}{4\pi^3}\int_0^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} v_x \left\{\exp\left(-\frac{E-E_f}{kT}\right)\right\} dk_x dk_y dk_z \quad (2.1)$$

But, Z(E) is state density of electron, f(E) is distribution function of electron, v_x is velocity element of x direction of electron, and m_e* is actual mass of electron in semiconductor. The v_x is written

$$v_x = \frac{\hbar k_x}{m_e^*}. \ (2.2)$$

$$E = E_0 + \frac{\hbar}{2m_e^*}(k_x^2 + k_y^2 + k_z^2) \quad (2.3)$$

The equation (2.1) is equal to

$$j_2 = -\frac{1}{4\pi^3}\int_0^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \frac{\hbar k_x}{m_e^*} \exp\left\{-\frac{\hbar^2\left(k_x^2 + k_y^2 + k_z^2\right)}{2m_e^* kT}\right\}\left\{\exp\left(-\frac{E_0 - E_f}{kT}\right)\right\} dk_x dk_y dk_z$$

$$= -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{E_0 - E_f}{kT}\right) \quad (2.4)$$

The semiconductor side is defined

$$E_0 - E_f = \phi_m - \chi - qV \quad (2.5)$$

$$\phi_B = \phi_m - \chi. \quad (2.6)$$

The current pass through from semiconductor to metal is

$$j_2 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B - qV}{kT}\right) \quad (2.7)$$

And, the current from metal to semiconductor is $\phi_m - \chi - qV$ replaced by $\phi_m - \chi$.

$$j_1 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \quad (2.8)$$

The net current is

$$j_2 - j_1 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \exp\left\{\left(\frac{qV}{kT}\right) - 1\right\}. \quad (2.9)$$

and current density is

$$j_{TH} = -\frac{4\pi q m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \exp\left\{\left(\frac{qV}{kT}\right) - 1\right\}. \quad (2.10)$$

The current about thermal emission structure is

$$j_{TH} = J_0 \exp\left\{\left(\frac{qV}{nkT}\right) - 1\right\} \quad [8]. \ (2.11)$$

$$j_0 = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \quad (2.12)$$

$$A^* = \frac{4\pi q m_e^* k^2}{h^3}. \quad (2.13)$$

A* is Richardson constant, k is Bltzmann's constant, h is Planck's constant and T is absolute temperature. The n that is called ideal factor is n=1 in ideal schottky contact, but in fact n>1. The reason of it is transport current in diffusion current, bias dependence of schottky barrier height in image force, injection of minority carrier, and dependence of schottky barrier in interfacial trap. The ϕ_b is written as

$$\phi_B = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_0}\right). \quad (2.14)$$

The ϕ_b can be looked for I-V measurement of schottky diode. The other method for look for schottky barrier height is relationship depletion capacitance and bias current.

2.1.2 Tunneling Structure

Next, it is considered about Tunneling structure. The tunneling is gave next equation [11]

$$J_{TN} = \frac{q^2 F^2}{8\pi h \phi_B} \exp\left[-\frac{8\pi}{3hqF} \sqrt{2m_e^* (q\phi_B)^3} \right]. \ (2.15)$$

But, F is field electric of vertical direction of semiconductor surface. The image of the image charge is added in schottky barrier ϕ_b

$$\phi_B = \phi_{B0} - \sqrt{\frac{qF}{4\pi\varepsilon}}. \ (2.16)$$

The ϕ_b is schottky barrier height when the field electric is not added, and the ε is silicon permittivity. The phenomenon that is lowered schottky barrier height in electric field is called schottky effect. The current in schottky interface expresses the sum of thermal emission current and tunneling current

$$J_{total} = J_{TH} + J_{TN}. \ (2.17)$$

2.1.3 Space Charge capacitance of Schottky Contact

The space charge capacitance of schottky contact can be considered a kind of capacitor as well as pn junction. That has electric capacitance. If the potential in paint x is φ(x), Poisson's equation is

$$\frac{d^2\varphi(x)}{dx^2} = -\frac{qN_D}{\varepsilon_0 \varepsilon_S}. \ (2.18)$$

The (2.18) is done integral is

$$\frac{d\ \varphi(x)}{dx} = -\frac{qN_D}{\varepsilon_0 \varepsilon_S} x + C_1 \quad (2.19)$$

$$\varphi(x) = -\frac{qN_D}{\varepsilon_0 \varepsilon_S} x^2 + C_1 + C_2. \ (2.20)$$

The x axis express Fig. 2.2,and beginning condition is φ(x)= φ_0=0 when x is equal to 0.

$$C_2 = 0 \quad (2.21)$$

x=w, and dφ(x)/dx=0

$$C_1 = -\frac{qN_D}{\varepsilon_0 \varepsilon_S} w. \ (2.22)$$

The potential is

$$\varphi(x) = \frac{qN_D}{\varepsilon_0 \varepsilon_s}\left(wx - \frac{x^2}{2}\right). \ (2.23)$$

x=w, and φ(w)=V_D-V

$$w = \left\{\frac{2\varepsilon_0 \varepsilon_s (V_0 - V)}{qN_D}\right\}^{\frac{1}{2}}. \ (2.24)$$

The electrostatic capacitance is

$$C = \frac{\varepsilon_0 \varepsilon_s}{w} = \left\{\frac{q\varepsilon_0 \varepsilon_S N_D}{2(V_D - V)}\right\}^{\frac{1}{2}} \quad (2.25)$$

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_0 \varepsilon_s N_D}(V_D - V). \ (2.26)$$

The N_D and V_D can be search, if the function of $1/C^2$ versus bias V.

2.2 Schottky Barrier MOSFET

2.2.1 The Principle of The Schottky Barrier MOSFET

The schottky barrier MOSFET works a different principle of the conventional pn junction MOSFET. Schottky barrier height has two mechanism; thermal electron emission structure and tunneling structure. The working MOS transistor is concerned closely with these structures.

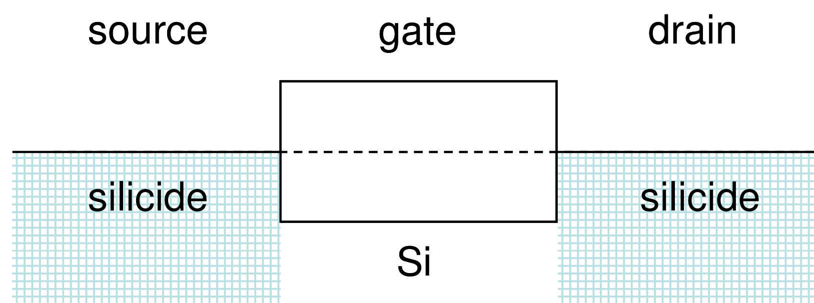
Fig. 2.3 shows a band structure of SB-MOSFET in the case of using middle gap silicide for source and drain. Fig. 2.3 (a) shows the case that there are no bias applied for gate and drain electrode. In this state, the thermal emission current obtaining over schottky barrier height flow as a leak current. A transistor is off state.

Fig. 2.3 (b) shows the case that there are drain bias (Vds>0) and no gate bias (Vgs=0). In this state, electron and hole cannot tunnel for the schottky barrier width of the edge of source and drain. A major current is a thermal emission current and a transistor is still off state.

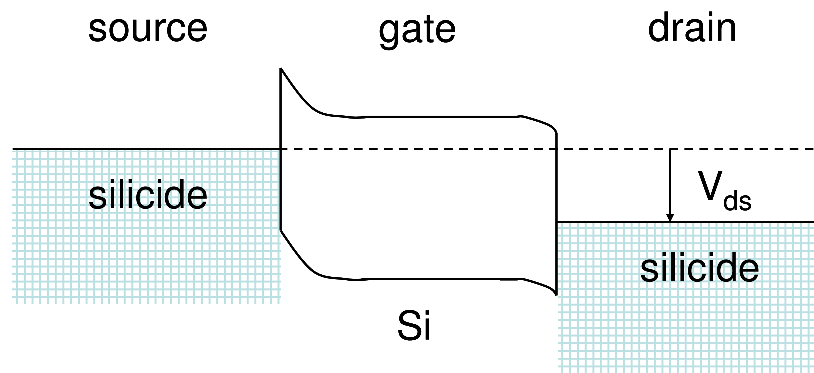
Fig. 2.3(c) shows the case that there are plus bias applied for gate and drain electrode. In this state, it's enough to flow a tunneling current because schottky barrier width become very thin at the edge of source. The schottky barrier width becomes more thickness at the edge of drain, so thermal emission current flow. Then, transistor is on state and a dependence of a on current is stronger by tunneling current.

Fig. 2.3 (d) shows the case that there are plus drain voltage (Vds>0) and minas gate voltage (Vgs<0). In this state, transistor is also on. SB-MOSFET can work for both p-type and n-type with one structure. In the case of using middle gap silicide, MOSFET especially work like that. This means that a leak current always flows.

On current of SB-MOSFET is controlled by a tunneling current at the source edge. The tunneling current depends on schottky barrier height, so it's so important to select materials. SB-MOSFET is need to be controlled by not middle gap silicide but also n-metal or p-metal. In this study, Er or Hf (n-metal) was inserted between Ni (middle gap) and Si and schottky barrier height was modulated by this technique.

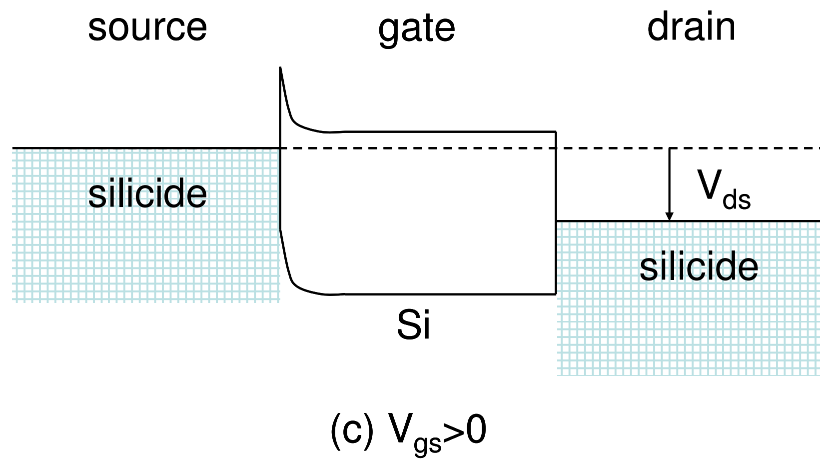


(a) V_{gs}=0

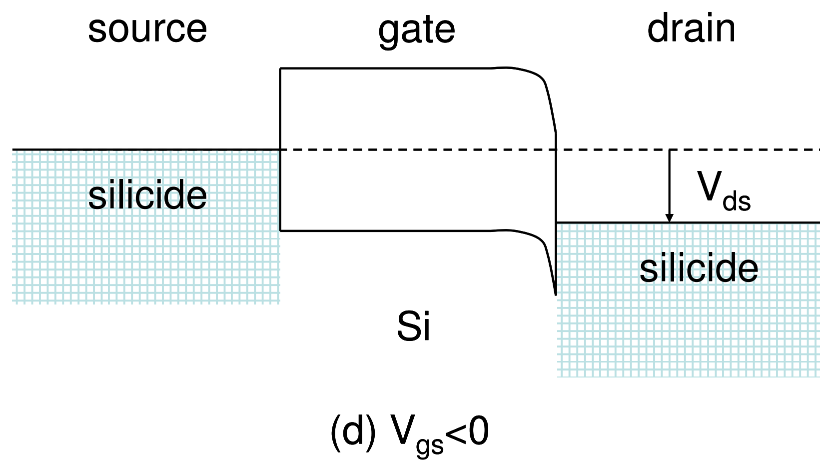


(b) V_{ds}>0

Fig. 2.3 The band structure of SB-MOSFET [10]



(c) $V_{gs}>0$



(d) $V_{gs}<0$

Fig. 2.3 The band structure of SB-MOSFET [10]

Chapter 3

FABRICATION AND CHARACTERIZATION METHODS

3.1 Experimental Procedure

3.1.1 Si Substrate Cleaning Process

High quality thin films require ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. It's considered that this substrate cleaning process is very important to realize desirable device operation and its reproducibility.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩcm at 25°C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩcm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the Si substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The steps are shown in Fig. 3.1. The first step, which use a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4: H_2O_2=4:1, called by SPM), was performed to remove any organic material and metallic impurities. After that, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:99). Then the cleaned wafer was dipped in DI water. Finally, the cleaned Si substrate was loaded to chamber to deposit as soon as it was dried by air gun.

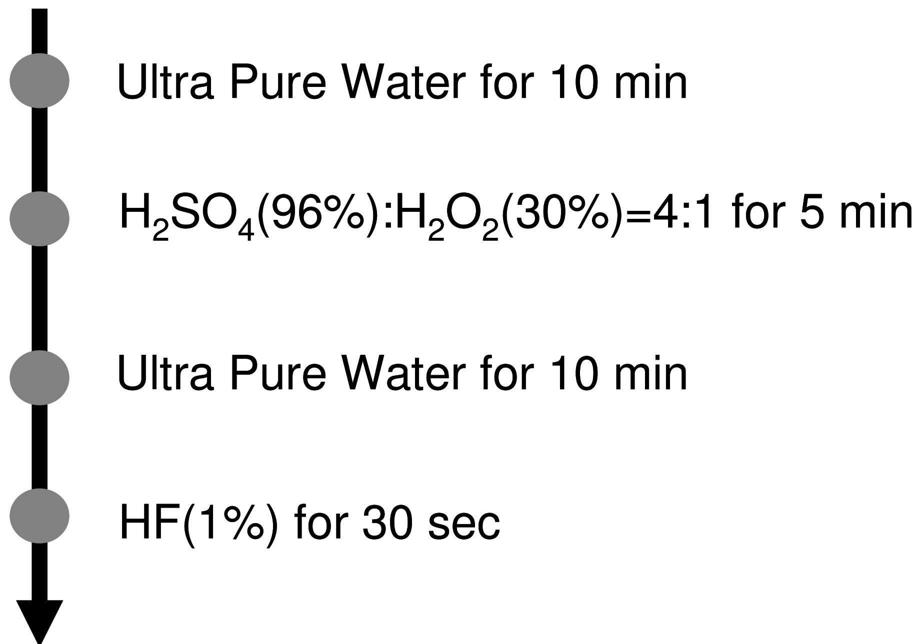


Fig. 3.1 Si Substrate Cleaning Process Flow

3.1.2 UHV-Sputtering System

After cleaned by chemicals, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive except Ni.) and Ni/Si were formed by an UHV-sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. It is performed by applying a high voltage across a low-pressure gas (usually argon at about 5 millitorr)to create a "plasma," which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike a "target," composed of the desired coating material, and cause atoms from that target to be ejected with enough energy to travel to, and bond with the substrate.

An UHV-sputtering system is used for thin film formations of electronic devices, for experiments of GMR, and for creating new materials of high temperature superconductors. In this study, UHV Multi Target Sputtering System ES-350SU shown as Fig. 3.2 was conducted. structure of UHV sputtering system is shown as Fig.

3.3. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. As for other details, Table 3.1 is attached for reference.

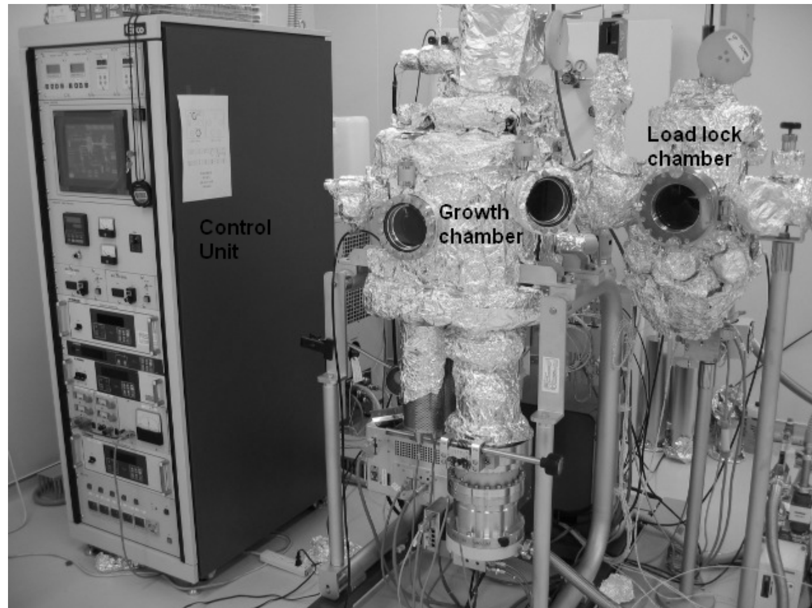


Fig. 3.2 Photo of UHV Multi Target Sputtering System ES-350SU

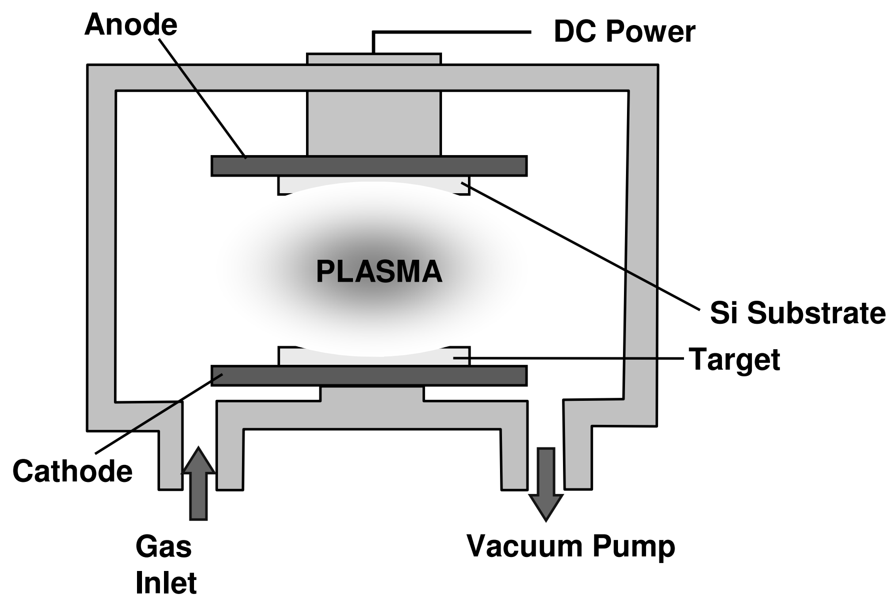


Fig. 3.3 structure of UHV sputtering system

Table 3.1 Specifications for UHV Multi Target Sputtering System ES-350SU

Growth chamber	1. Ultimate pressure	1.5 x 10^{-6}Pa
	2. Substrate size	2 inch in diameter
	3. Heating temperature	600ºC
	4. Heater type	Lamp type heater
	5. Target	3 inch x 5 pieces (motor-driven)
Load lock chamber	6. Vacuum pumps	TMP 500L/sec and RP 250L/min
	7.Ultimate pressure	6.6 x 10^{-5}Pa
	8. Vacuum pumps	TMP60L/sec and RP90L/min
	9. Substrate holder with cooling function / Substrate holder with heating function /Cleaning function / Radical beam source	

3.1.3 Infrared Annealing Furnace

After formation from UHV sputtering system, thin films of Ni/Si, Ni/M/Si, M/Ni/Si were moved to annealing furnace to hold thermal process.

In order to obtain high quality films, annealing process after deposition is required. The annealing after deposition is considered to bring the suppression of leakage current because of the defects in the films and surface roughness. In this study, thermal process leads to the reaction of Ni with Si.

The equipment for annealing used in this investigation was QHC-P610CP (ULVAC RIKO Co. Ltd). Fig. 3.4 is the photo of the infrared annealing furnace, whose schematic illustration was shown as Fig. 3.5. The annealing was performed by six infrared lamps surrounding the sample stage which were made of carbon and coated by

SiC. The heating temperature was controlled by thermocouple feedback.

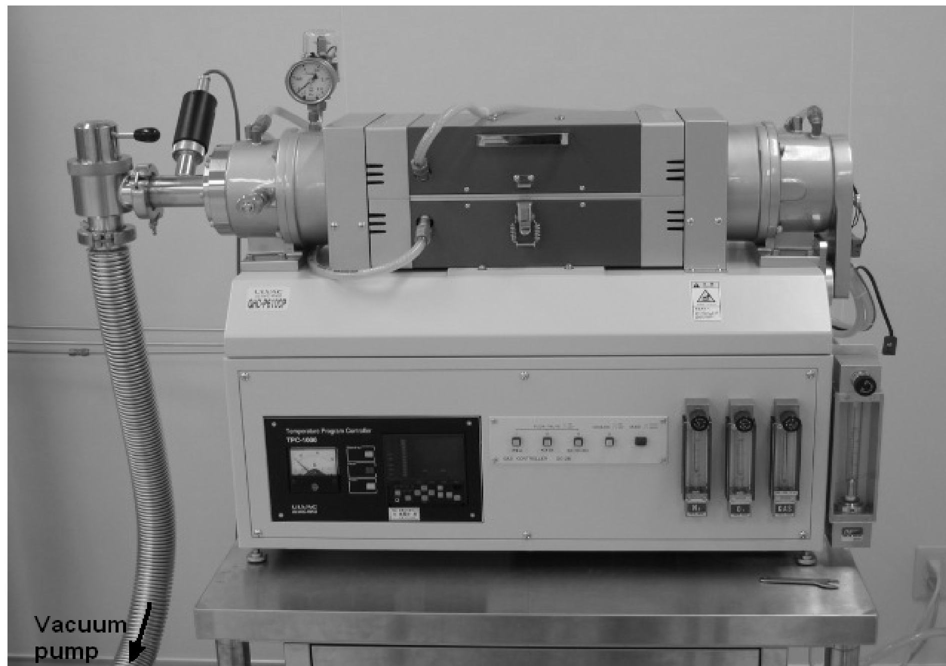


Fig. 3.4 Photo of infrared annealing furnace

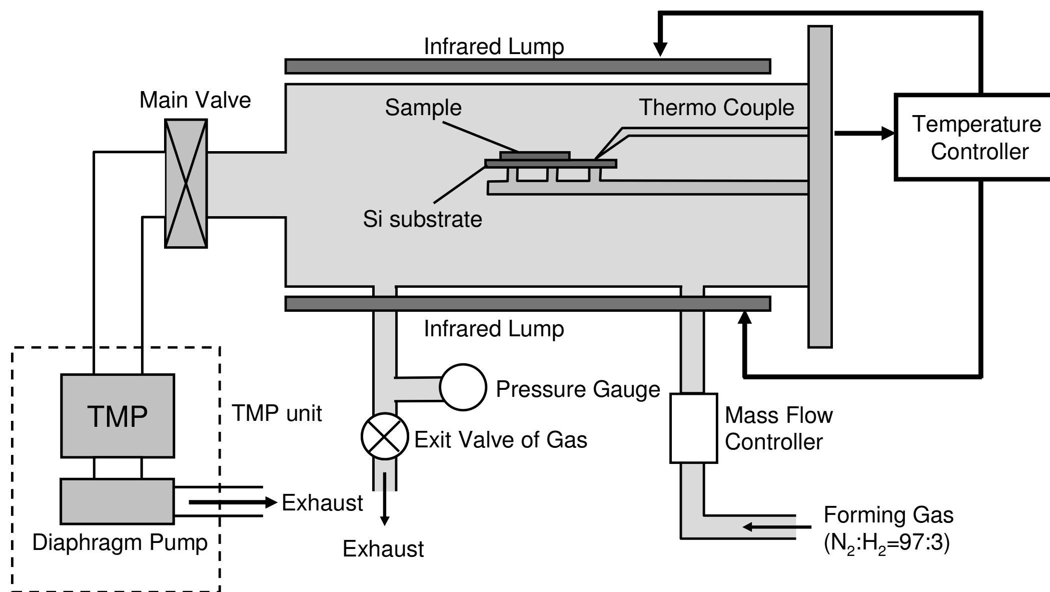


Fig. 3.5 schematic image of infrared annealing furnace

3.1.4 Vacuum Thermal Evaporation Method

All of Al metals in this work were obtained from deposition with bell jar vacuum thermal evaporation shown as Fig. 3.6. Fig. 3.7 illustrates a schematic drawing for vacuum thermal evaporation system. Filament is made of tungsten, was used for heating the Al source up to its vapor temperature. Both filaments and Al sources are made of Nilaco, inc. with material purity of 99.999%.

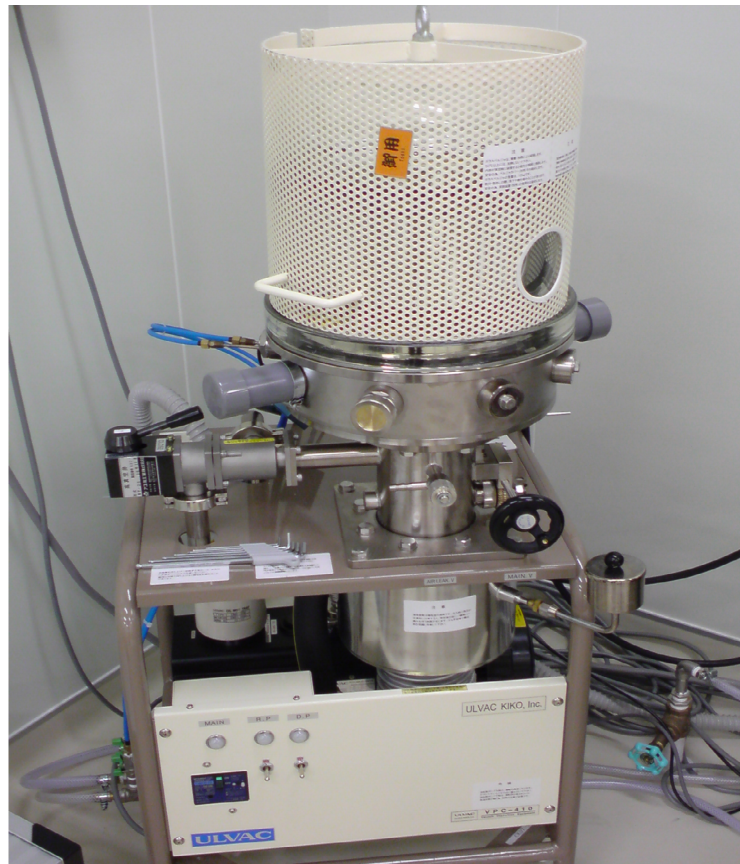


Fig. 3.6 Photo of bell jar

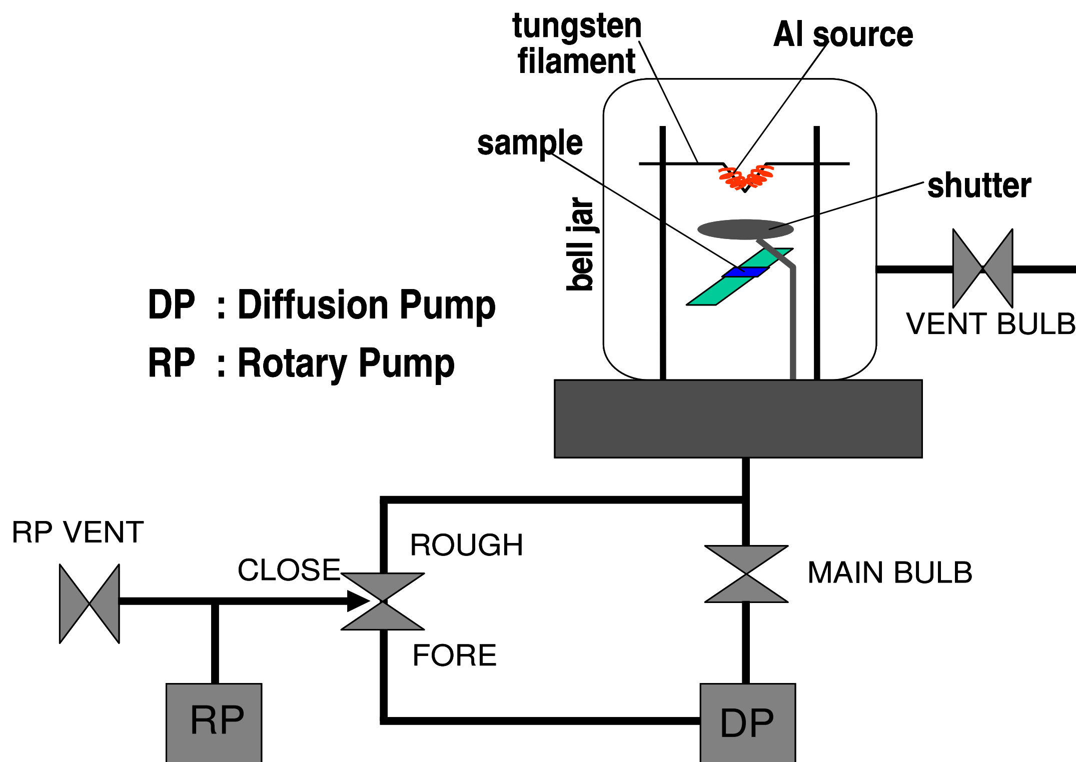


Fig. 3.7 Schematic drawing for vacuum thermal evaporation system.

The physics of vacuum thermal evaporation is based on thermodynamics of the evaporated materials. There have been experiments performed for evaluating the thermodynamic properties of material. Careful evaluation may reveal that the vapor pressure of liquid Al is given by the following.

$$\log P_{torr} = \frac{15{,}993}{T} + 12.409 - 0.999 \log T - 3.52 \times 10^{-6} T \quad (3.1)$$

Neglecting the last two terms, the Arrhenius character of log P vs. 1/T can be essentially preserved. Fig. 3.8 presents thermal equilibrium for metal evaporations in form of Arrhenius plots. The dot marks are the metal melting points. Two modes of evaporation can be distinguished in practice, depending whether the vapor effectively emanates from liquid or solid source. Usually, a melt will be required if the element in

question does not achieve a vapor pressure greater than 10^{-3} torr at its melting point. Most metals, like Al, Ag, Au, and so on, fall into this category, and effective film deposition is attained only when the source is heated into the liquid phase. On the other hand, elements such as Cr, Ti, Mo, Fe, and Si reach sufficiently high vapor pressures of 10^{-2} torr some 500°C below the melting point.

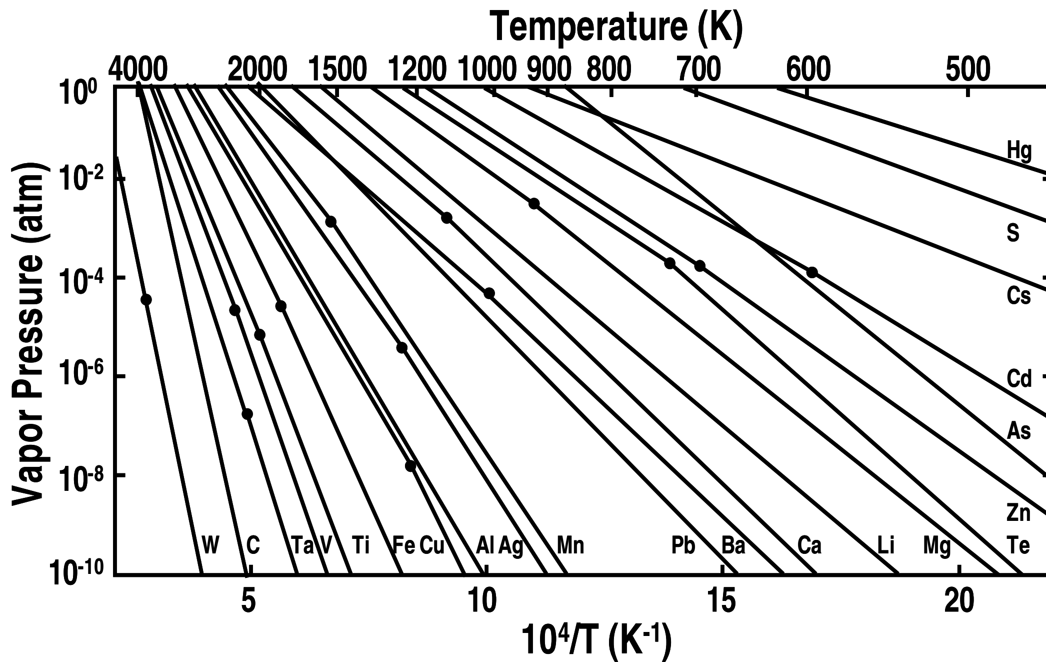


Fig. 3.8 Thermal equilibrium for metal evaporations in form of Arrhenius plots. The dot marks are the metal melting points.

3.1.5 Photolithography

The process flow of photolithography that used throughout this study is shows in Fig. 3.9. Electrical hotplate is used for baking purposes. The spin-coated layer photoresist was aligned and exposed through tungsten coated e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. MJB4 of Karl Suss contact-type mask aligner as shown Fig. 3.10 was used for aligning and exposition purposes. The exposure duration was set to 2.8 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.) after dipped into the solvent for 2 minute and baked at 130 ˚C for 5 minutes.

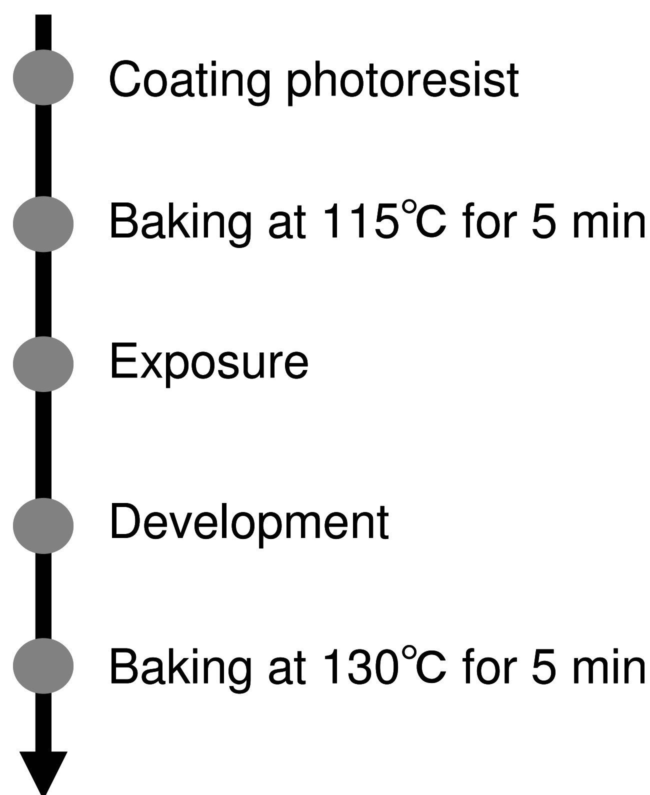


Fig. 3.9 The process flow of photolithography

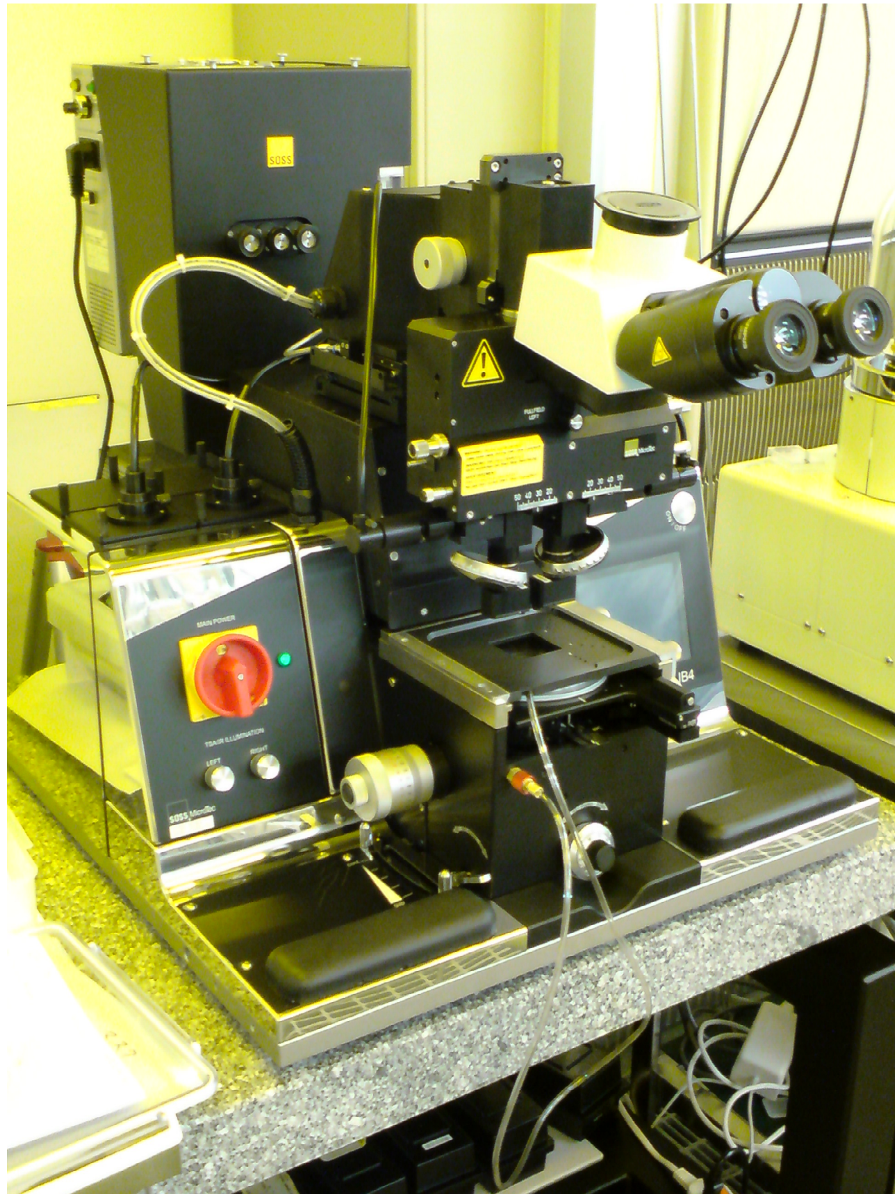


Fig. 3.10 Photo of mask aligner

3.2 Measurement Methods

3.2.1 Scanning Electron Microscope (SEM)

The Scanning Electron Microscope (SEM) as shown Fig. 3.11 is a microscope that uses electrons rather than light to form an image. There are many advantages to using the SEM instead of a light microscope. The SEM has a large depth of field, which allows a large amount of the sample to be in focus at one time. The SEM also produces images of high resolution, which means that closely spaced features can be examined at a high magnification. Preparation of the samples is relatively easy since most SEMs require the sample to be conductive. The combination of higher magnification, larger depth of focus, greater resolution, and ease of sample observation makes the SEM one of the most heavily used instruments in research areas today. The SEM uses electrons instead of light to form an image. A beam of electrons is produced at the top of the microscope by heating of a metallic filament. The electron beam follows a vertical path through the column of the microscope. It makes its way through electromagnetic lenses which focus and direct the beam down towards the sample. Once it hits the sample, other electrons (backscattered or secondary) are ejected from the sample. Detectors collect the secondary or backscattered electrons, and convert them to a signal that is sent to a viewing screen similar to the one in an ordinary television, producing an image.

Fig. 3.11 Photo of SEM

3.2.2 Transmission Electron Microscope (TEM)

Cross-section TEM image is the most important analysis method to characterize physical thickness, film quality and interface condition.

Fig. 3.12 Shows TEM system. First, focus lenses change convergent angle and beam size. The electron beam transmitted through the thin fragment sample passes objective lens and projective lens, and finally projected on fluorescent screen. Recording oh the image is performed by direct exposure on exclusive film for electron microscope set lower part of the fluorescent screen.

Electron interacts strongly with lattice by scattering. Thus, sample has to be very thin fragment. Required thickness of the sample is 5 to 500 nm at 100 kV. TEM images are obtained in very high resolution such as 0.2 to 0.3 nm at 200 kV.

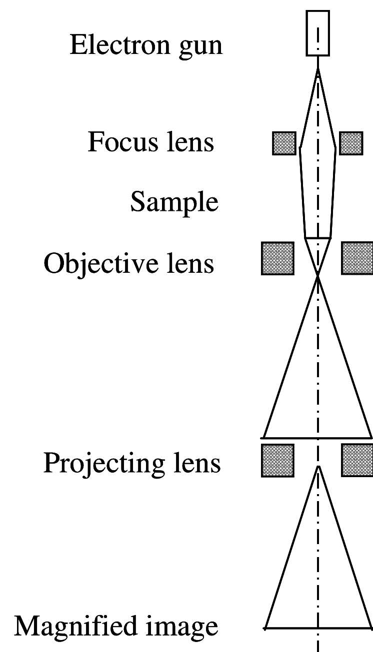


Fig. 3.12 schematic diagram for TEM (Transmission Electron Microscopy) observation. Several magnetic lenses are used to magnify the object image

3.2.3 Four-Point Probe Technique

The sheet resistance of Ni silicide was measured by four-point probe technique. The phase of Ni can be ascertained according to the sheet resistance of Ni silicide thin film, because the sheet resistance of $NiSi_2$ is greatly different from that of Ni monosilicide (NiSi) or other phase such as Ni_2Si.

The four-point probe technique is one of the most common methods for measuring the semiconductor resistivity because two-point probe method is difficult to interpret. The sheet resistance is calculated form potential difference between inside 2 terminals (between B probe and C probe) after applying the current between outside 2 terminals (between A probe and D probe) as shown in Fig. 3.13. The resistance by two-probe technique is higher than accurate resistance because it includes the contact resistance (R_C) between metal probe and semiconductor surface and spreading resistance (R_{SP}) of each probe. Neither R_C nor R_{SP} can be accurately calculated so that semiconductor resistance (R_S) cannot be accurately extracted from the measured resistance. On the other hand, four-probe technique can neglect these parasitic resistances because the current value which flows between terminals is very small and potential drop can be disregarded. In this study, sheet resistance was measured by four-probe technique.

For an arbitrarily shaped sample the sheet resistance (ρ_{sh}) is given by

$$\rho_{sh} = V/I * CF \qquad (3.2)$$

where *CF* is correction factor that depends on the sample geometry. If the distance among probes (s; in this study, s=1 mm) is greatly shorter than the width of a sample (d), *CF* equals to $\pi/\ln(2)=4.53$.

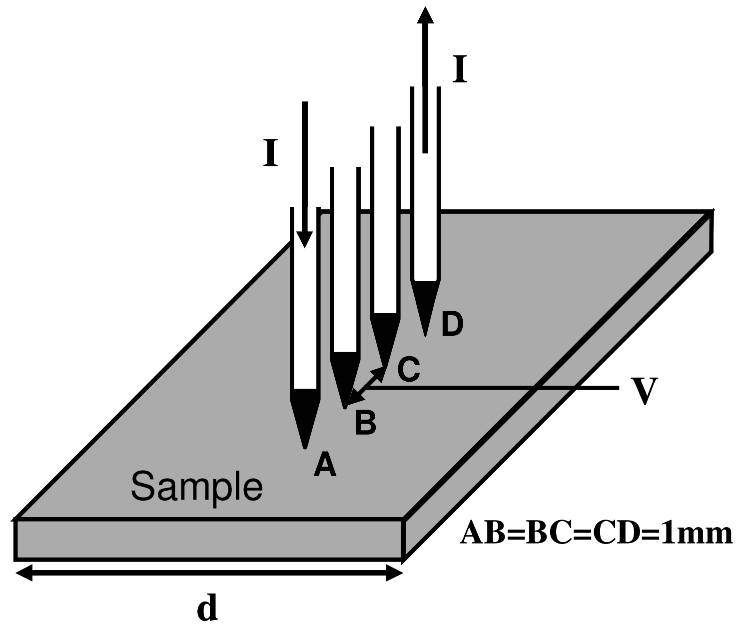


Fig. 3.13 illustration of four point probe system

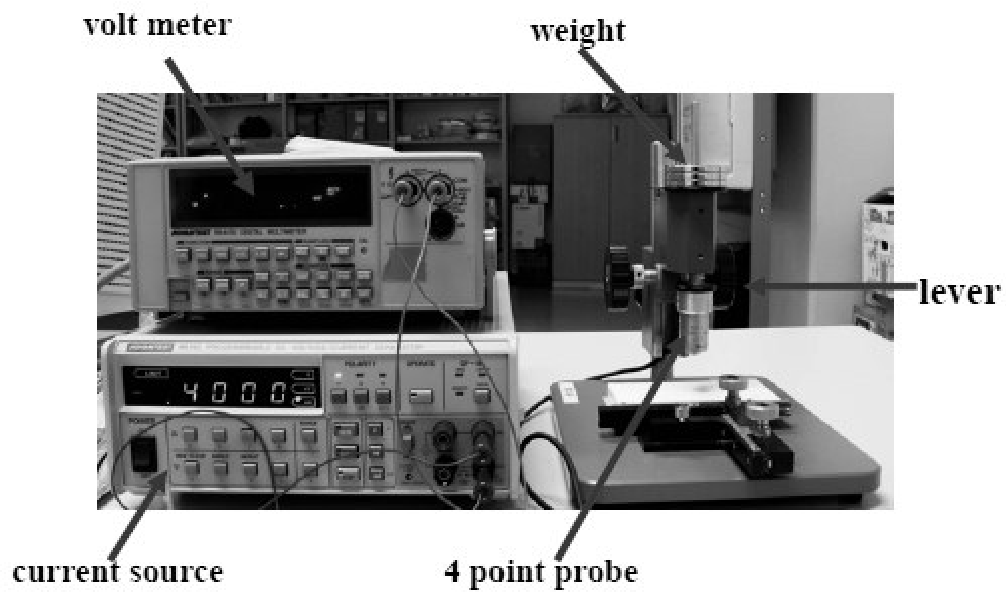


Fig. 3.14 Photo of four probe system

3.2.4 J-V (Leakage Current Density – Voltage) Measurement

To estimate the leakage current density, *J-V* characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard.).

3.2.5 Evaluation of Schottky Barrier Height Based J-V Characteristics

When, the case of V>>kT/q, the index term is more larger than 1, it can be ignored. The current density (***J***) of schottky contacts is defined

$$J = J_0 e^{qV/kT} \qquad (3.3)$$

However, the current density of obtaining actual characteristics increases the index function against bias voltage. The increasing rate is less than (3.3). Therefore, the ideal factor (***n***) is used as same as pn junction

$$J = J_0 e^{qV/nkT} \qquad (3.4)$$

If n is equal to 1, (3.4) accords with (3.3), and the current density flows along theory, but usually n>1.

Another, J_0 is expressed

$$J_0 = A^* T^2 e^{-\phi_B/nkT} = \frac{4\pi q m_e^* k^2 T^2}{h^3} e^{-\phi_B/kT} \qquad (3.5)$$

A^*, k and m^*_e are Richaldson constant, Boltman's Constant and effective mass. From (3.5), ϕ_B can be got from J_0.

3.2.6 C-V (Capacitance – Voltage) Measurement

C-V characteristic measurements were performed with various frequencies (1kHz ~ 1MHz) by precision LCR Meter (HP 4284A, Agilent). The energy band diagram of an MOS capacitor on a p-type substrate is shown in figure 3.15 [12]. The intrinsic energy level E_i or potential φ in the neutral part of device is taken as the zero reference potential. The surface potential φ_s is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \quad (3.6)$$

It is the change of charge due to a change of voltage and is most commonly given in units of farad/units area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS capacitor from the gate, $C = dQ_G / dV_G$, where Q_G and V_G are the gate charge and the gate voltage. Since the total charge in the device must be zero, assuming no oxide charge, $Q_G = (Q_S + Q_{it})$, where Q_S is the semiconductor charge, Q_{it} the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \varphi_s$, where V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and φ_s the surface potential, allowing Eq. (3.6) to be rewritten as

$$C = \frac{dQ_s + dQ_{it}}{dV_{ox} + d\phi_s} \quad (3.7)$$

The semiconductor charge density Q_S, consists of hole charge density Q_p, space-charge

region bulk charge density Q_b, and electron charge density Q_n. With $Q_S = Q_p + Q_b + Q_n$, Eq. (3.7) becomes

$$C = -\frac{1}{\dfrac{dV_{ox}}{dQ_s + dQ_{it}} + \dfrac{d\phi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \qquad (3.8)$$

Utilizing the general capacitance definition of Eq. (3.6), Eq. (3.8) becomes

$$C = -\frac{1}{\dfrac{1}{C_{ox}} + \dfrac{1}{C_p + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_{it}} \qquad (3.9)$$

The positive accumulation Q_p dominates for negative gate voltages for *p*-substrate devices. For positive V_G, the semiconductor charges are negative. The minus sign in Eq. (3.8) cancels in either case.

Eq. (3.9) is represented by the equivalent circuit in figure 3.16 (a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_p is very high approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in figure 3.16 (b) and the overall capacitance is C_{ox}. For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = .\ qN_AW$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} as shown in figure 3.17 (c). In weak inversion C_n begins to appear. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (figure 3.17 (d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in figure 3.17 (e) applies in inversion, with $C_b = K_s\,\varepsilon_o / W_{inv}$ with W_{inv} the inversion space-charge region width. The flatband voltage V_{FB} is determined by the metal-semiconductor work function difference

φ_{MS} and the various oxide charges through the relation

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{tox} \rho_m(x)dx - \frac{1}{C_{ox}}\int_0^{tox} \frac{x}{t_{ox}}\rho_{ot}(x)dx \quad (3.10)$$

where $\rho(x)$ = oxide charge per unit volume. The fixed charge Q_f is located very near the Si-SiO_2 interface and is considered to be at that interface. Q_{it} is designated as Q_{it} (φ_s), because the occupancy of the interface trapped charge depends on the surface potential.

Mobile and oxide trapped charges may be distributed throughout the oxide. The x-axis is defined in figure 3.16. The effect on flatband voltage is greatest, when the charge is located at the oxide-semiconductor substrate interface, because then it images all of its charge in the semiconductor. When the charge is located at the gate-insulator interface, it images all of its charge in the gate and has no effect on the flatband voltage. In the study, principally, EOT values and flatband voltage were extracted from C-V characteristics by using the NCSU CVC modeling program [13]. EOT values were calculated with taking quantum effect into account.

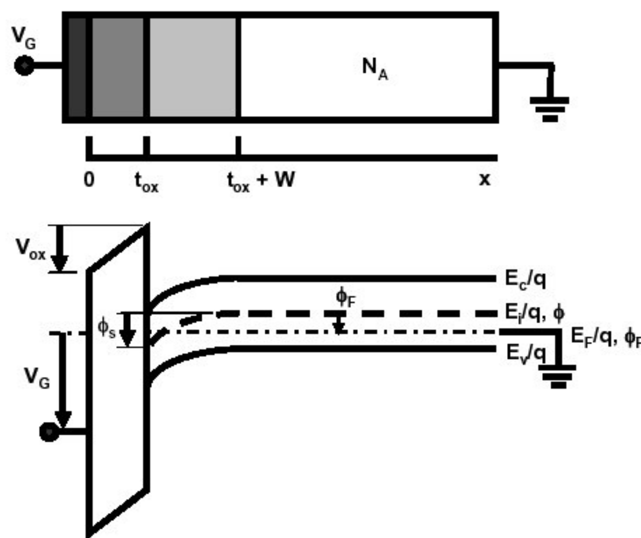


Fig .3.15 The energy band diagram of an MOS capacitor on a p-type substrate

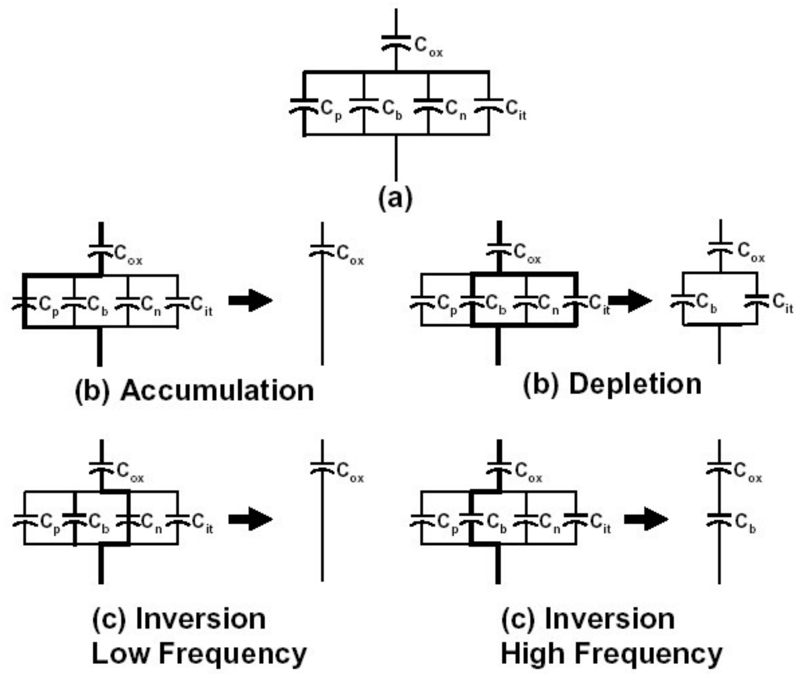


Fig .3.16 Capacitances of an MOS capacitor for various bias conditions.

3.2.7 Evaluation of Schottky Barrier Height Based C-V Characteristics

Schottky barrier height biased reverse voltage work as capacitance against small AC signal because the charge in depletion region changes if depletion-layer width is changed by bias voltage. The charge in depletion region is expressed Eq. (3.11)

$$Q = qN_D d = \sqrt{2q\varepsilon_s\varepsilon_o N_D (V_D + V)} \qquad (3.11)$$

Depletion capacitance is defined

$$C = \frac{dQ}{dV} = \sqrt{\frac{q\varepsilon_s\varepsilon_o N_D}{2(V_D + V)}} \qquad (3.12)$$

$1/C^2$ is calculated by Eq.(3.12)

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s\varepsilon_o N_D}(V_D + V) \qquad (3.13)$$

$1/C^2$ can be lined straight against reverse voltage V as shown Fig. 3.17. Diffusion voltage V_D is got from the point of $1/C^2=0$. The slope is $\frac{2}{q\varepsilon_s\varepsilon_o N_D}$ and εs is a constant defined by a material of semiconductor, so N_D is calculated by the slope. Eq. (3.13) is defined per a unit area and divided by a sample space A equals Eq. (3.14)

$$\frac{\Delta(1/C^2)}{\Delta V} = \frac{2}{A^2 q\varepsilon_s\varepsilon_o N_D} \qquad (3.14)$$

N_D is

$$N_D = \frac{2}{A^2 q\varepsilon_s\varepsilon_o \frac{\Delta(1/C^2)}{\Delta V}} \qquad (3.15)$$

E_C-E_F is got from Eq. (3.16)

$$n = N_C \exp\{-(E_C - E_F)/kT\} \qquad (3.16)$$

Schottky barrier height is expressed Eq. (3.17)

$$\phi_B = qV_D + (E_C - E_F) \qquad (3.17)$$

The band structure of schottky contact was shown as Fig. 3.18.

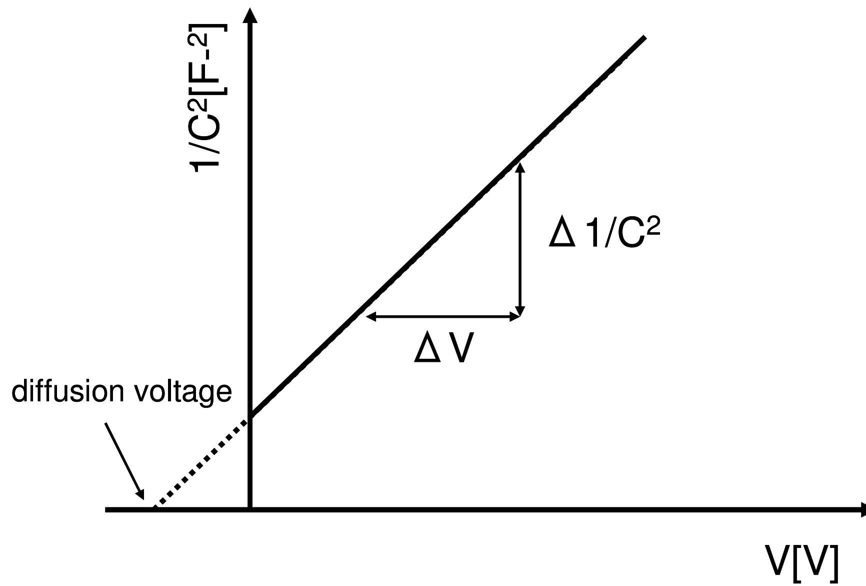


Fig. 3.17 $1/C^2$-V graph of schottky contact

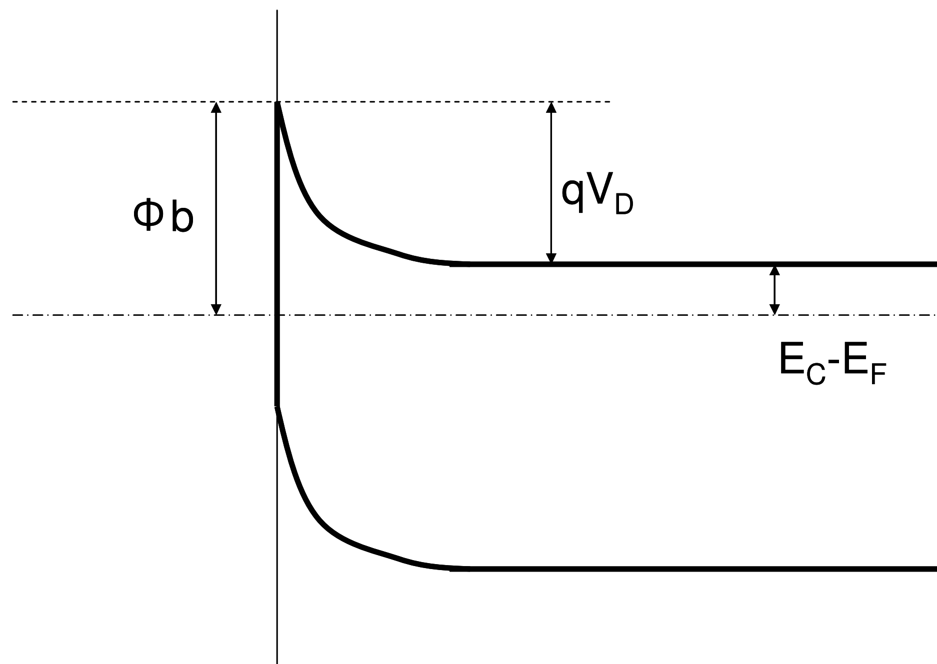


Fig. 3.18 The band structure of schottky contact

Chapter 4

CHARACTERISTICS OF Ni Silicide SCHOTTKY DIODE

4.1 Ni Silicide Schottky Diode with Er or Hf Interlayer

4.1.1 Introduction

As stated in chapter 2, it's so important for schottky barrier MOSFET to select materials because on current of SB-MOSFET is controlled by a tunneling current at the source edge and a tunneling current depends on schottky barrier height. NiSi has an experimental SBH of 0.65 eV on n-Si(100). This high SBH value hinders the application of NiSi in SB-MOSFETs. If we can lower the SBH of silicides to very low value, the device exhibits the same intrinsic performance as conventional MOSFET but also benefits from the advantages of SB-MOSFETs as mentioned chapter 1.

In this chapter, we report a new Schottky-barrier-height modulation method for Ni silicide by inserting an thin Er or Hf interlayer between Ni and Si before silicidation process.

4.1.2 Fabrication Process of Schottky Diode

Schottky diode was formed on SiO_2 isolated n- and p-type bulk (100) Si wafers, as shown in Fig. 1. The patterned wafers were cleaned in mixed solution of H_2SO_4 and H_2O_2 followed by chemical oxide removal by diluted HF. Pure metals of Er or Hf and Ni were deposited subsequently on to the substrates by DC sputtering in Ar gas at a pressure of 5.5×10^{-1} Pa. The layered structures of Ni/Er/Si and Ni/Hf/Si consisting of 12-nm-thick Ni layer and Er or Hf layer of various thicknesses ranging from 1.8 to 12 nm were deposited. The samples were annealed in forming gas (FG) (3% H_2 + 97% N_2) at various temperatures from 400°C to 700°C for 1 min. After the removal of un-reacted metals by chemical etching, Al back contacts were formed. The Schottky barrier heights of the fabricated diodes with Er interlayer were evaluated from current voltage (*I*-*V*) characteristics and the schottky barrier heights of the fabricated diodes with Hf interlayer were evaluated from capacitance voltage (*C*-*V*) characteristics. The silicide films formed from the 100nm-Ni/3.6nm-Er/Si layered structure were also analyzed by transmission electron microscope (TEM) and energy dispersive X-ray spectroscopy (EDX).

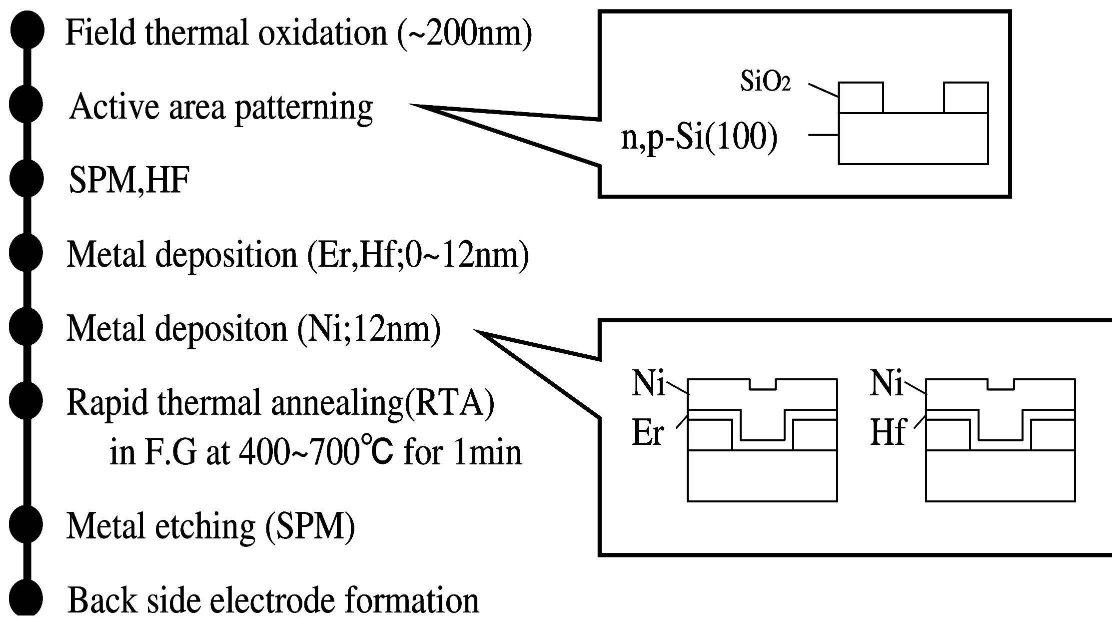
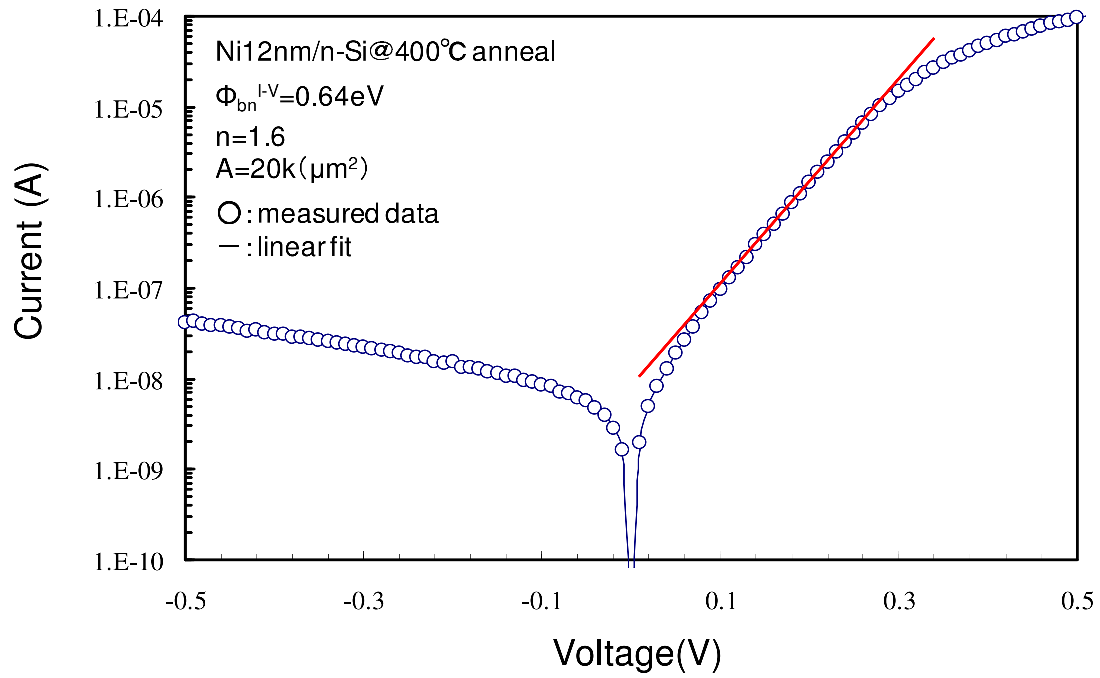


Fig. 4.1 Fabrication process of the Schottky barrier diodes from the initial structures of Ni/Er/Si and Ni/Hf/Si

4.1.3 Characteristics of Ni Silicide Schottky Diode

Φ_b of the Ni(12nm)/p-Si and Ni(12nm)/n-Si structures were evaluated from the *I*-*V* and *C*-*V* characteristics in the forward bias region. Typical current-voltage (*I*-*V*) and capacitance-boltage ($1/C^2$-V) curves of Schottky diodes of annealing temperature from 400°C to 700°C are shown in Figs. 4.2-4.7. Φ_b obtained by *I*-*V* characteristics were plotted against the annealing temperatures in Fig. 4.8 (a) and (b). The observed Φ_b for holes were 0.44-0.46eV and Φ_b for electron were 0.64-0.67eV in the annealing temperature range of 400-700°C. Φ_b obtained by *C*-*V* characteristics were plotted against the annealing temperatures in Fig. 4.9. The observed Φ_b for holes were 0.446-0.457eV in the annealing temperature range of 400-700°C.



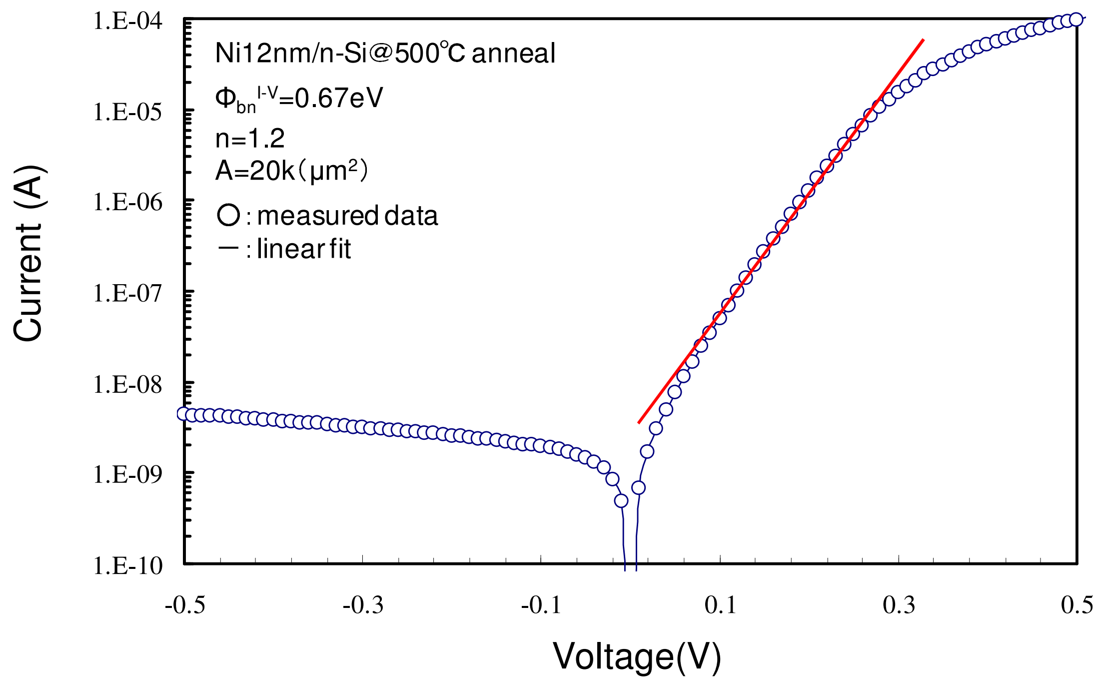
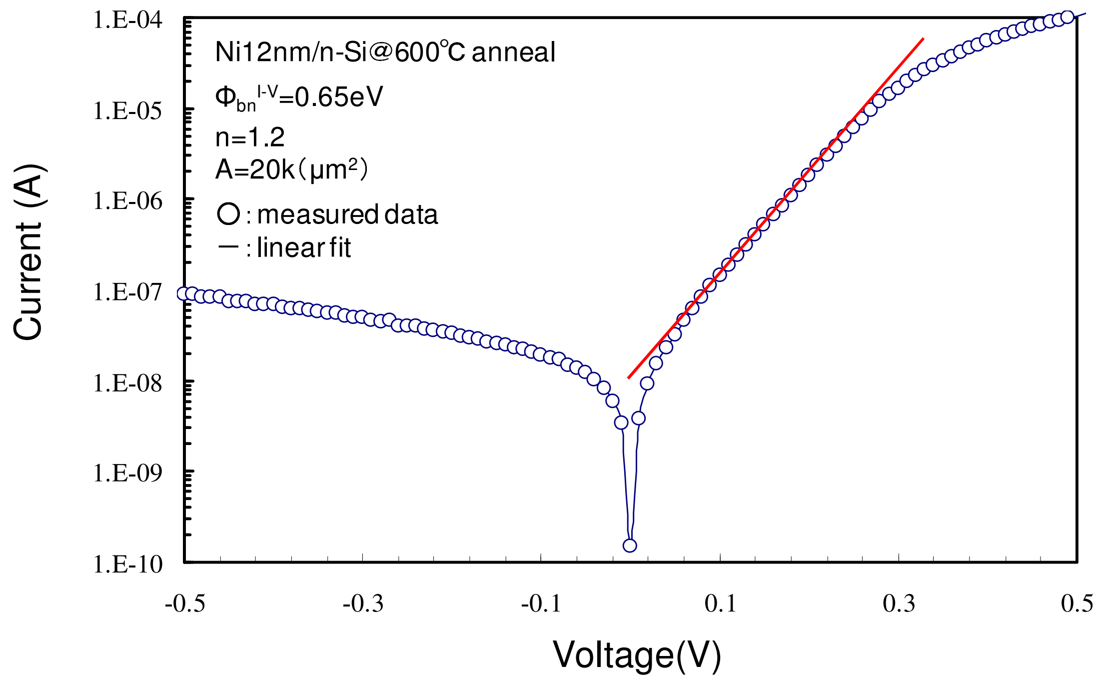


Fig. 4.2 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



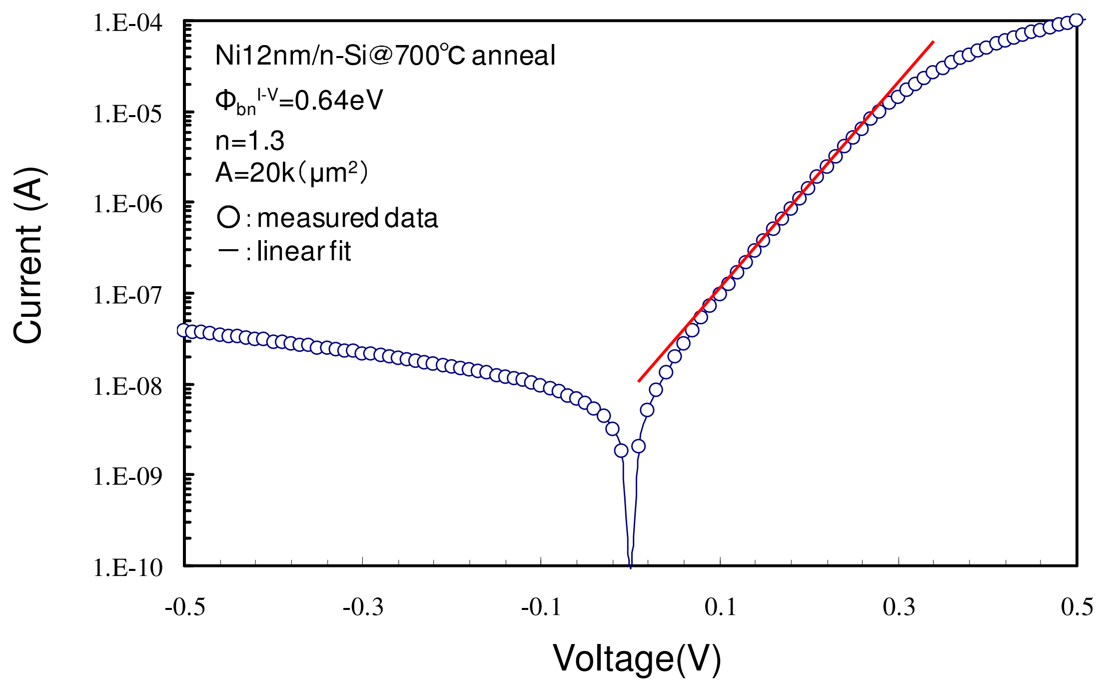
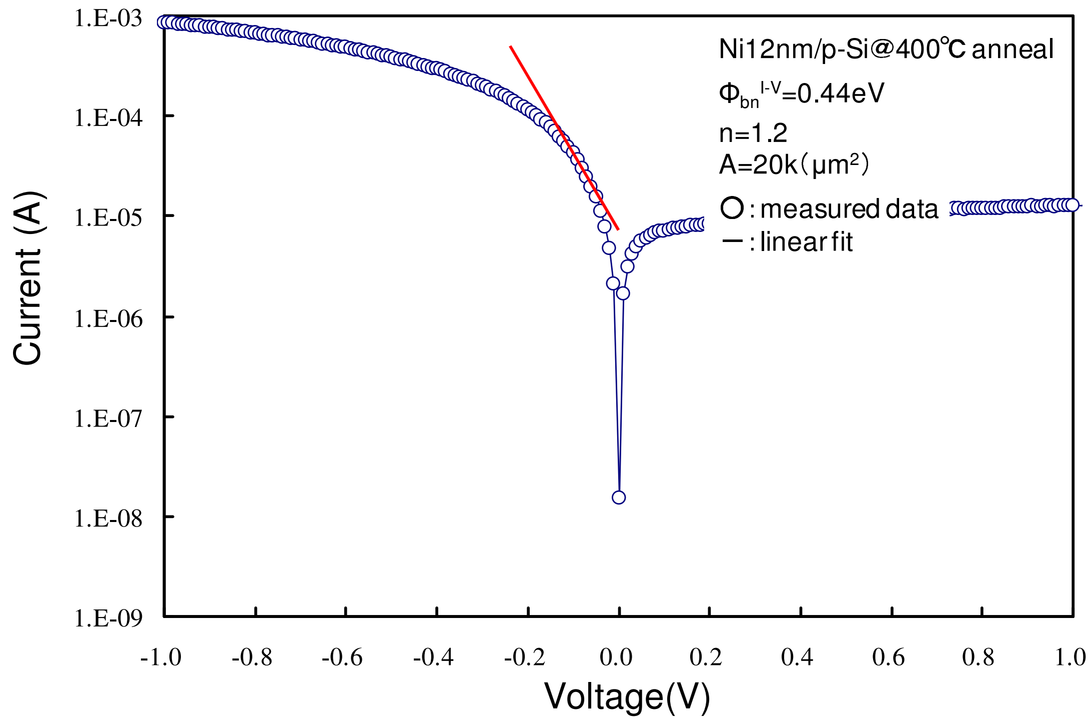


Fig. 4.3 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



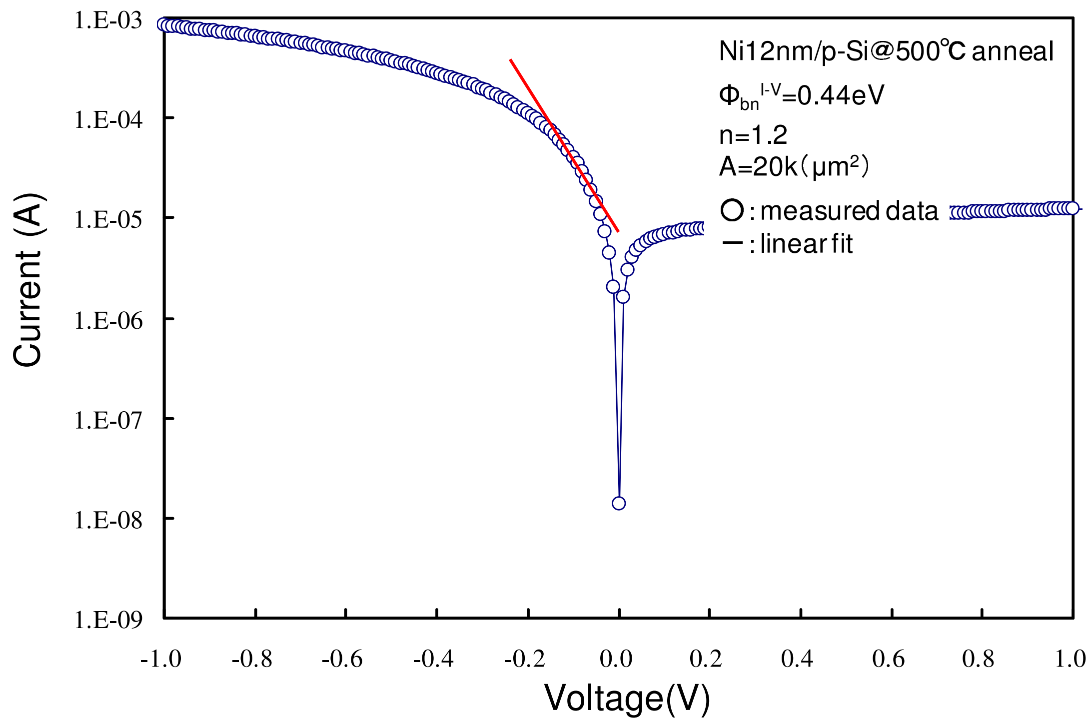
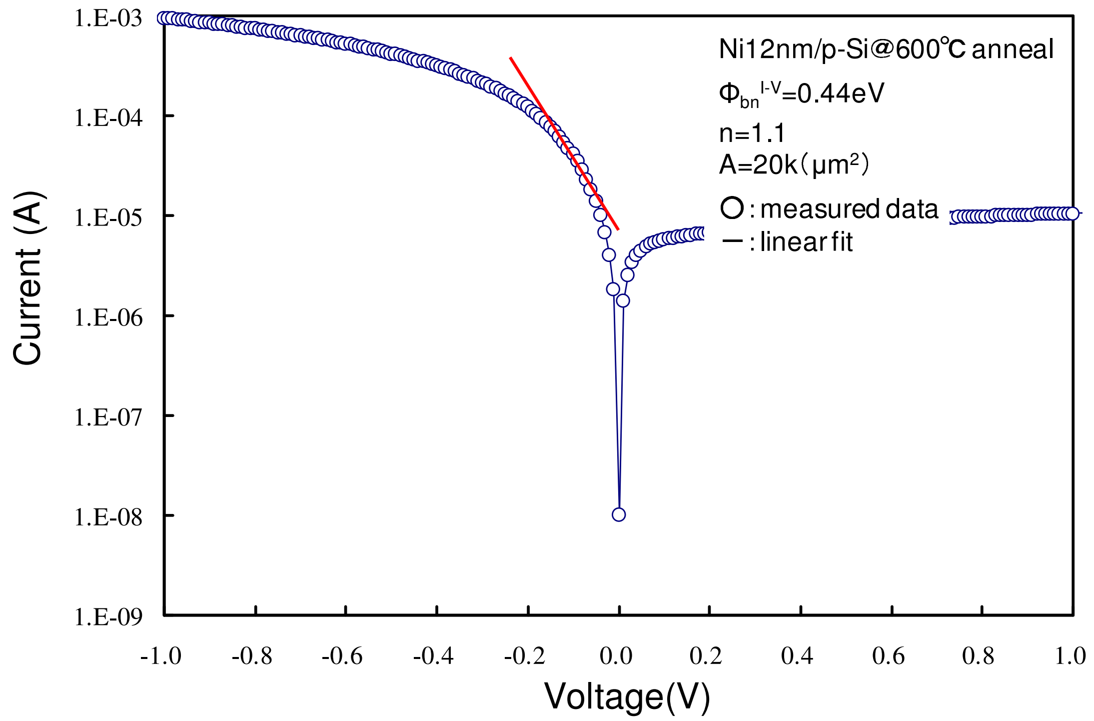


Fig. 4.4 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



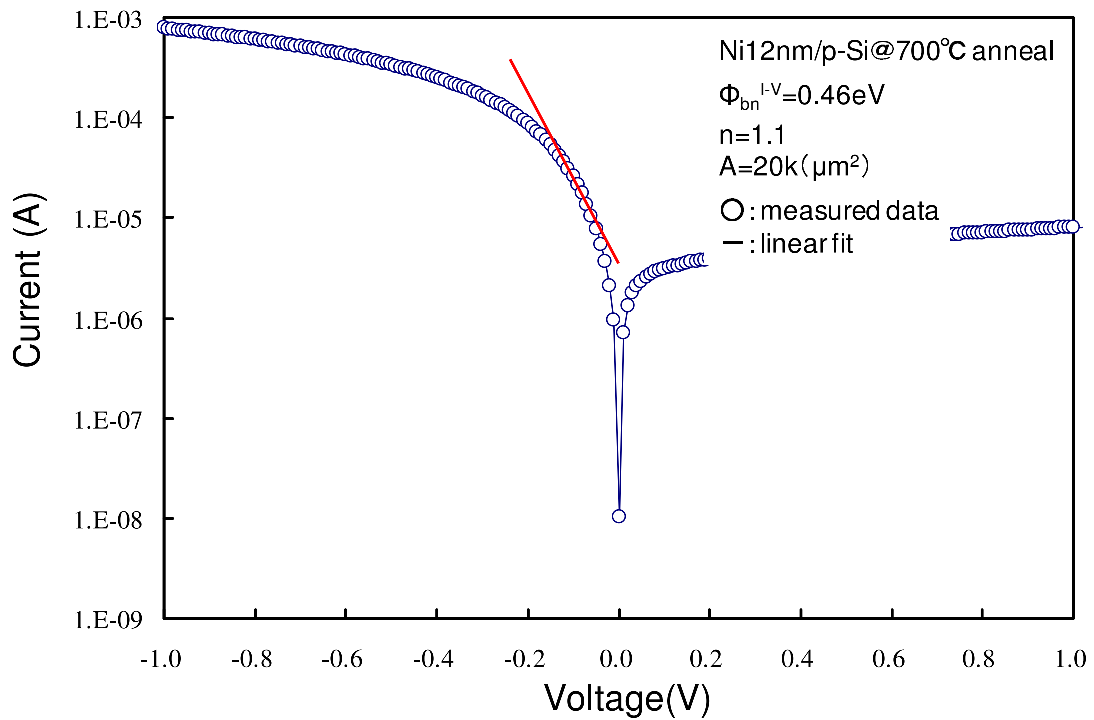
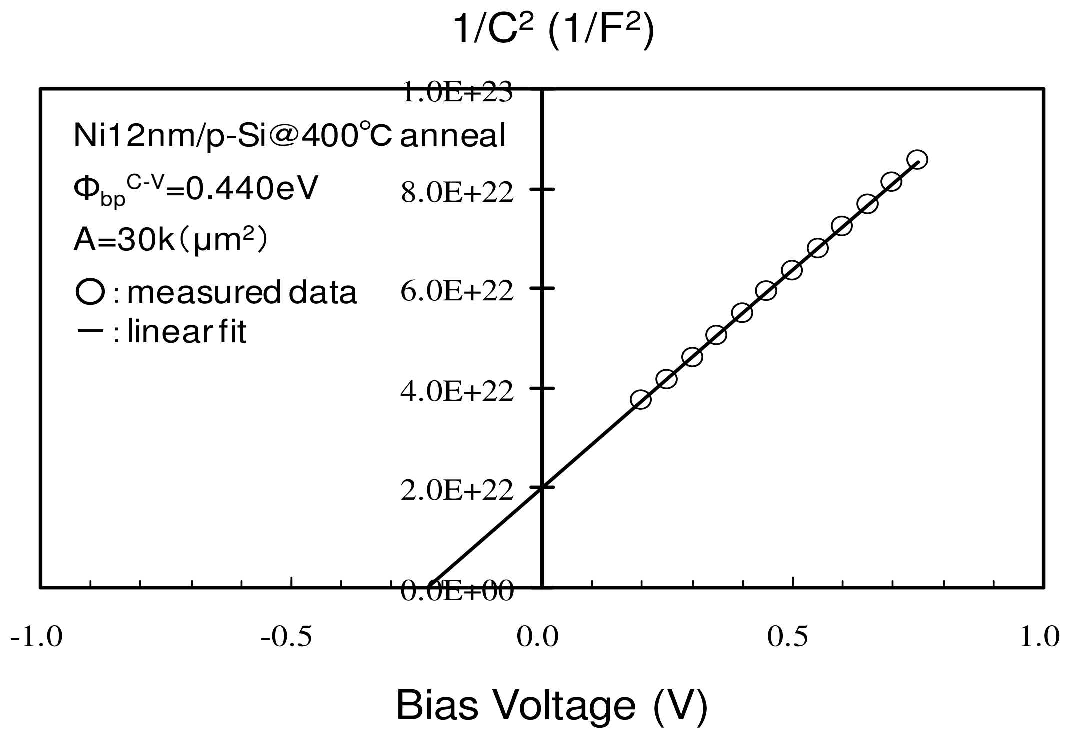


Fig. 4.5 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



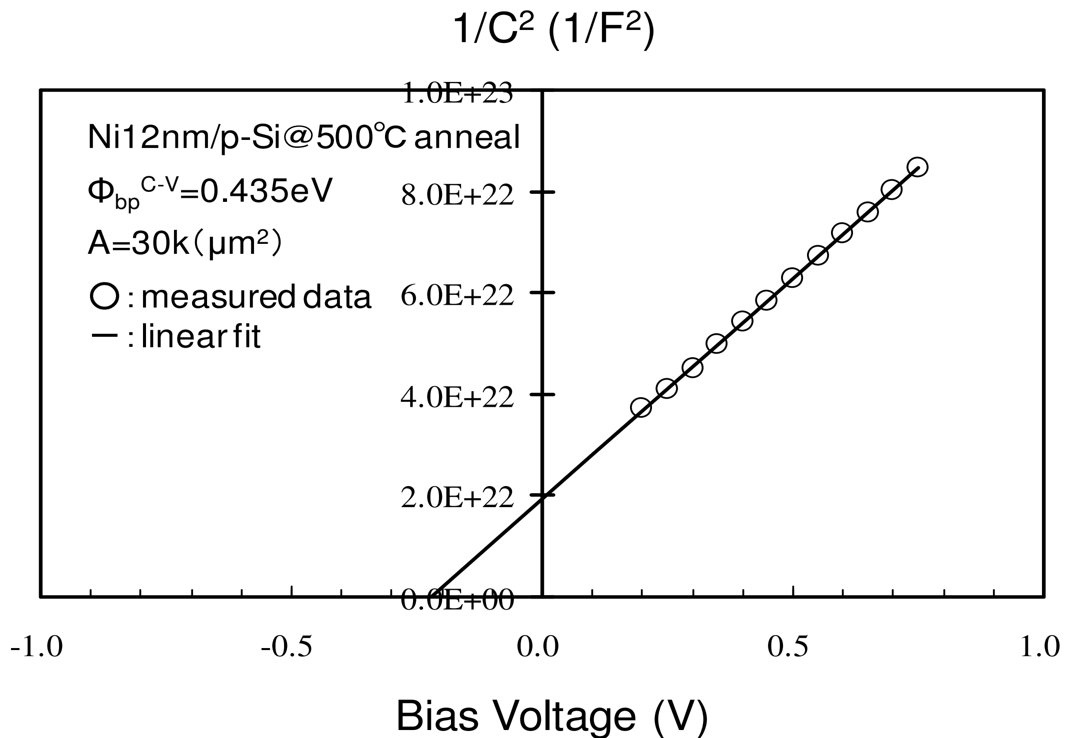
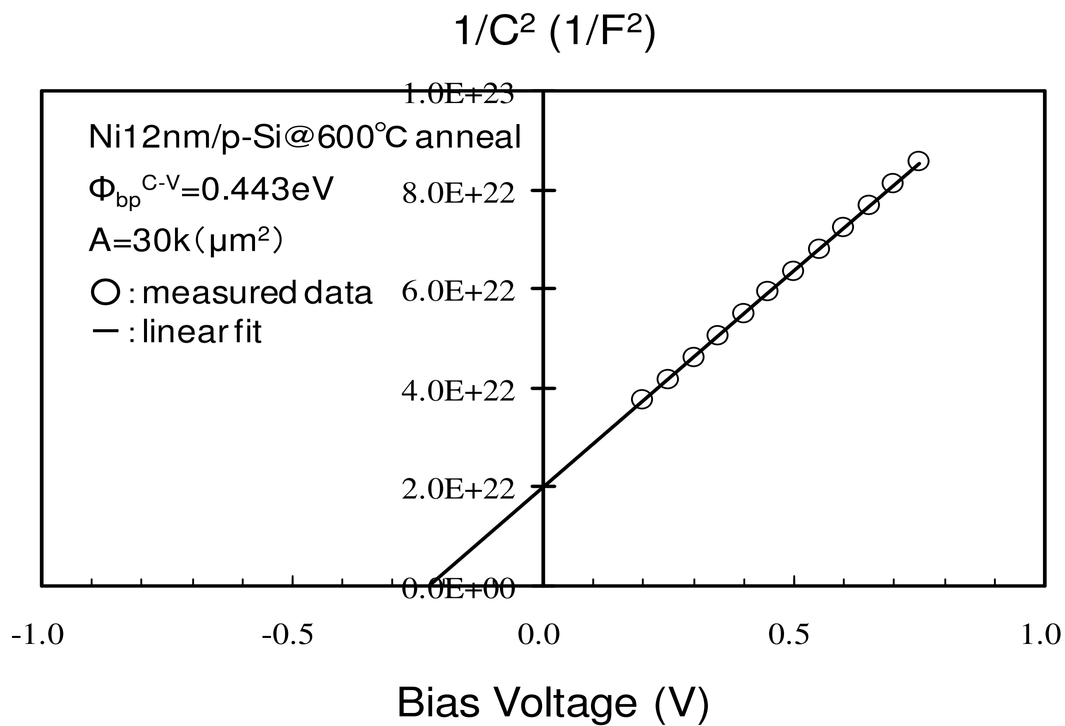


Fig. 4.6 $1/C^2$-V characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



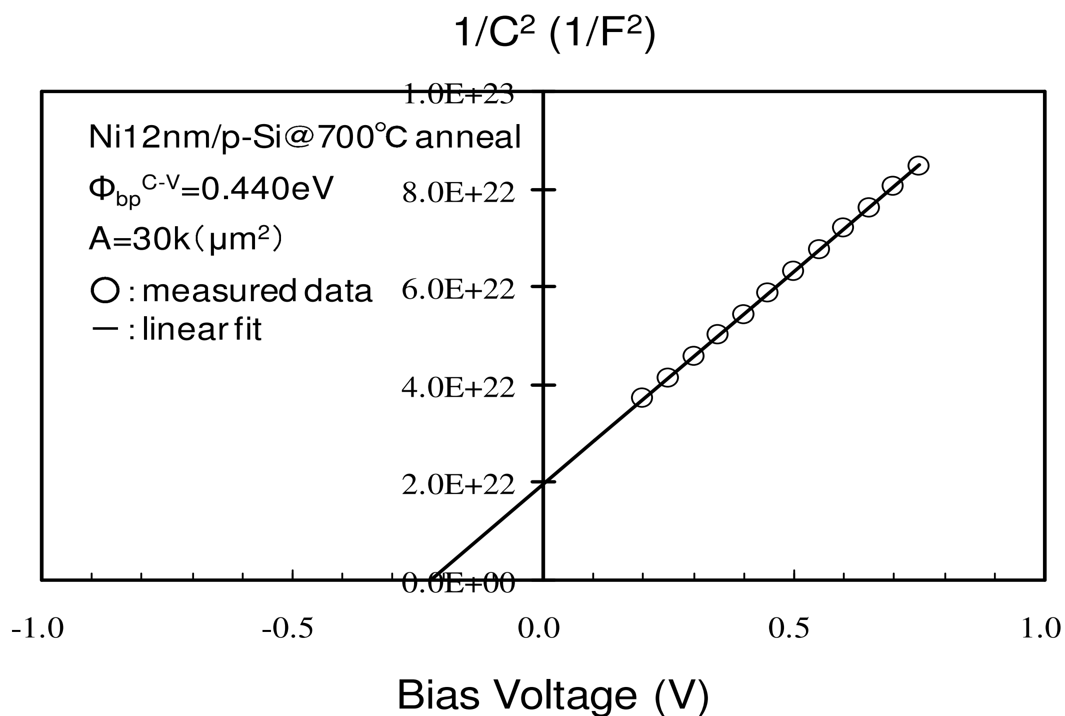


Fig. 4.7 $1/C^2$-V characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C

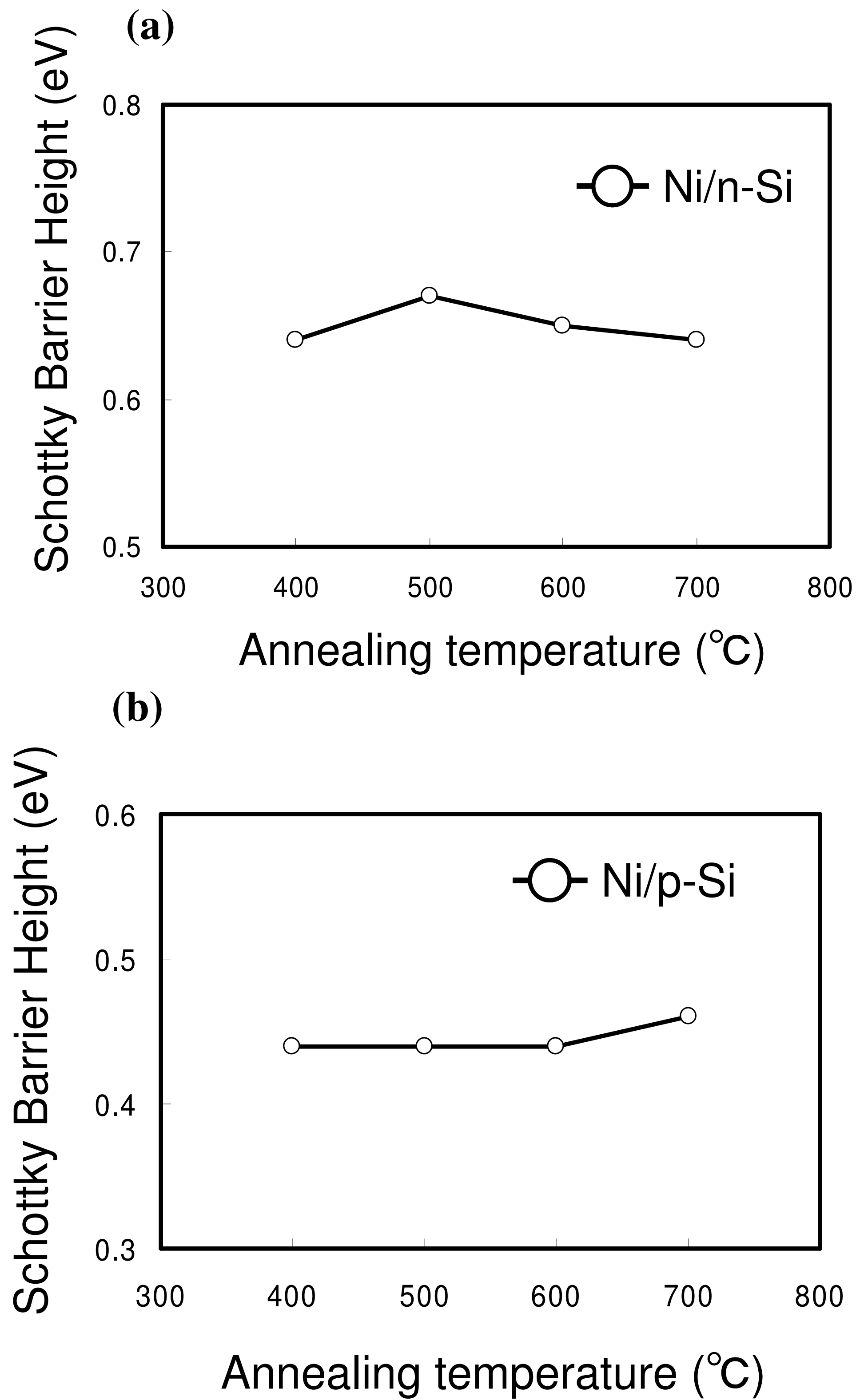


Fig. 4.8 Annealing temperatures dependence of Scottky barrier heights measured by I-V characteristics formed from the initial structures of Ni/n-Si and Ni/p-Si.

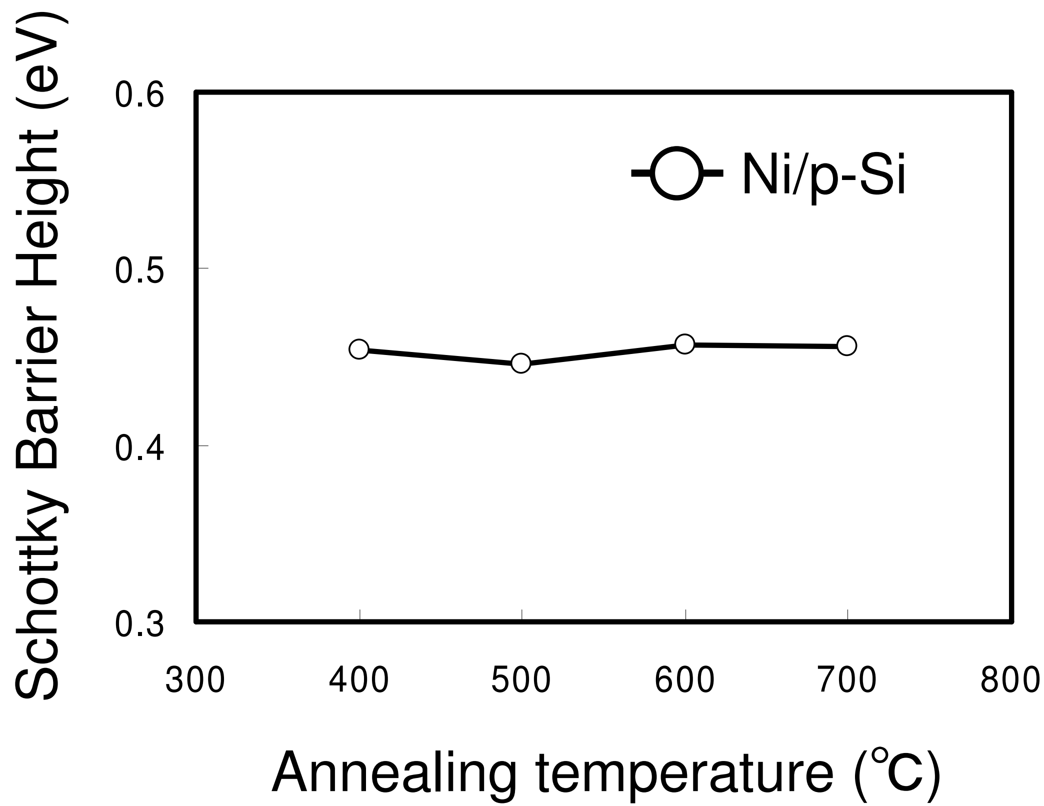
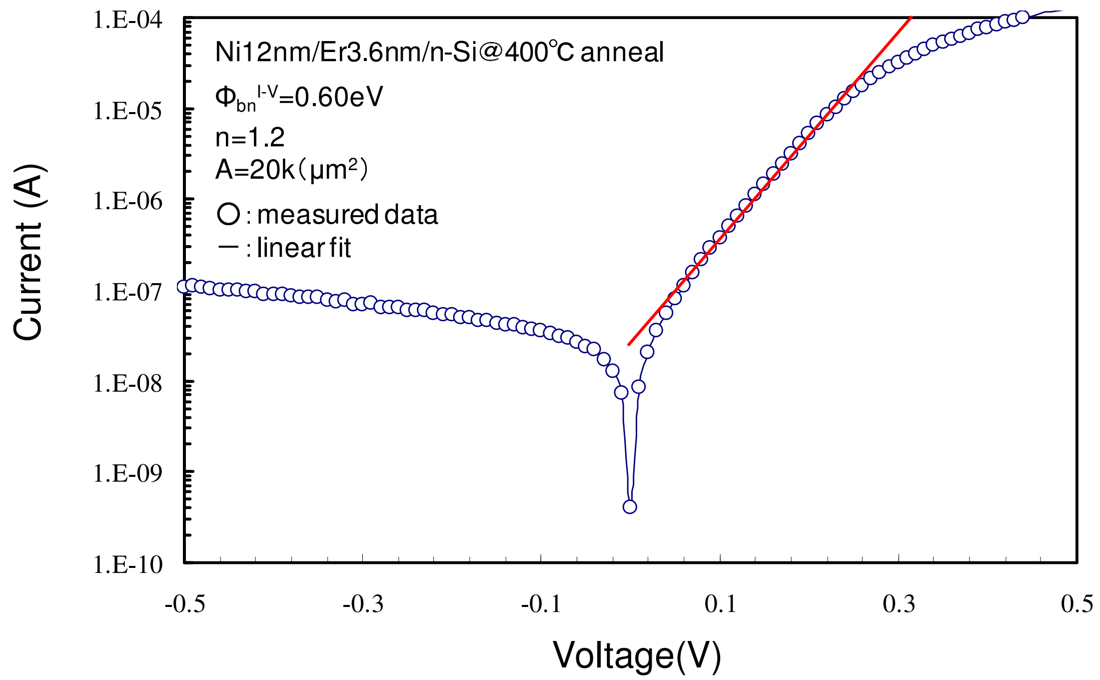


Fig. 4.9 Annealing temperatures dependence of Scottky barrier heights measured by C-V characteristics formed from the initial structures of Ni/n-Si.

4.1.4 Characteristics of Ni Silicide Schottky Diode with Er Interlayer

Typical current-voltage (*I-V*) curves of Schottky diodes of annealing temperature from 400°C to 700°C fabricated from the Ni/Er/n-Si and Ni/Er/p-Si structures are shown in Figs. 4.10-4.25. The Φ_b values for electrons evaluated from the *I-V* corves in the forward bias region are plotted as a function of the annealing temperature as shown in Fig. 4.26. The values of Φ_b observed from the layered deposition structures with the Er interlayer were lower by 0.02-0.22eV compared with those without the Er interlayer, and the lowest Φ_b of 0.42 eV was achieved for the sample with 12-nm-thick Er interlayer annealed at 700°C. For the constant annealing temperature of 700°C, the Φ_b decreased with increasing the thickness of the Er interlayer, and by 0.22 eV lowering was obtained for 12-nm-thick Er, as shown in Fig. 4.27.



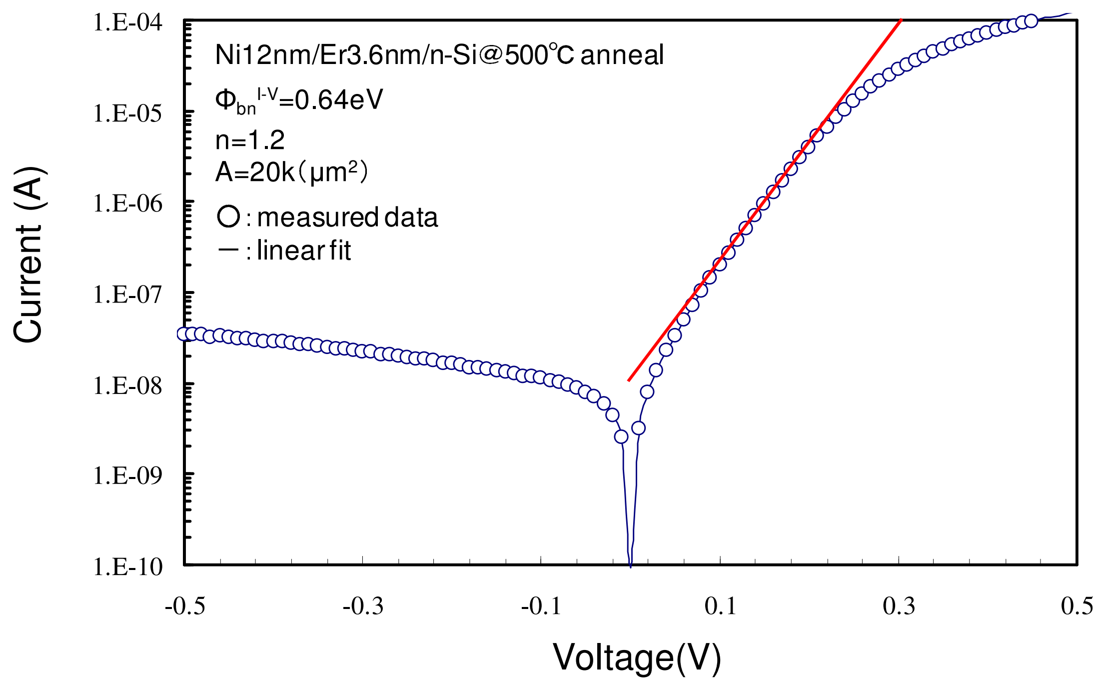
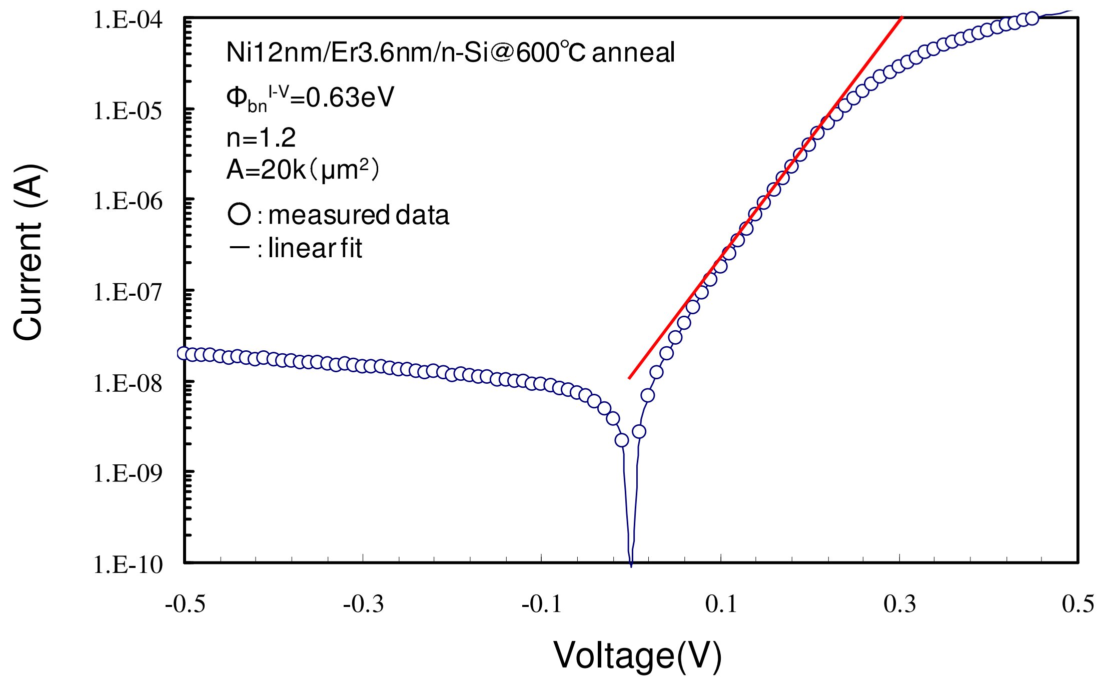


Fig. 4.10 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



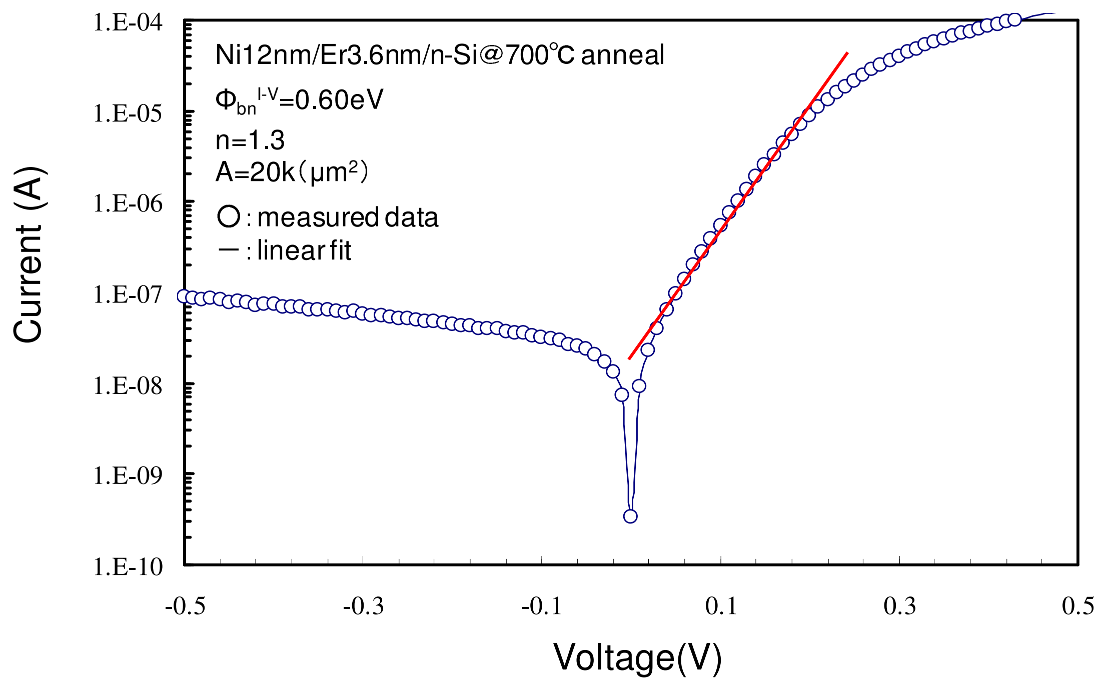
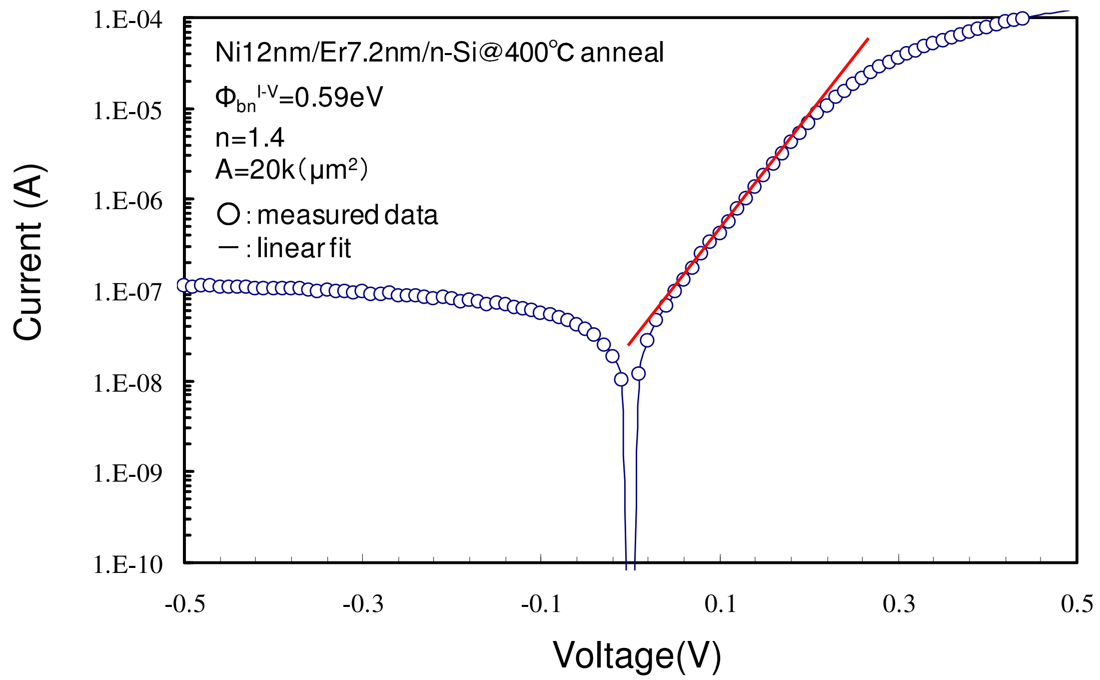


Fig. 4.11 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



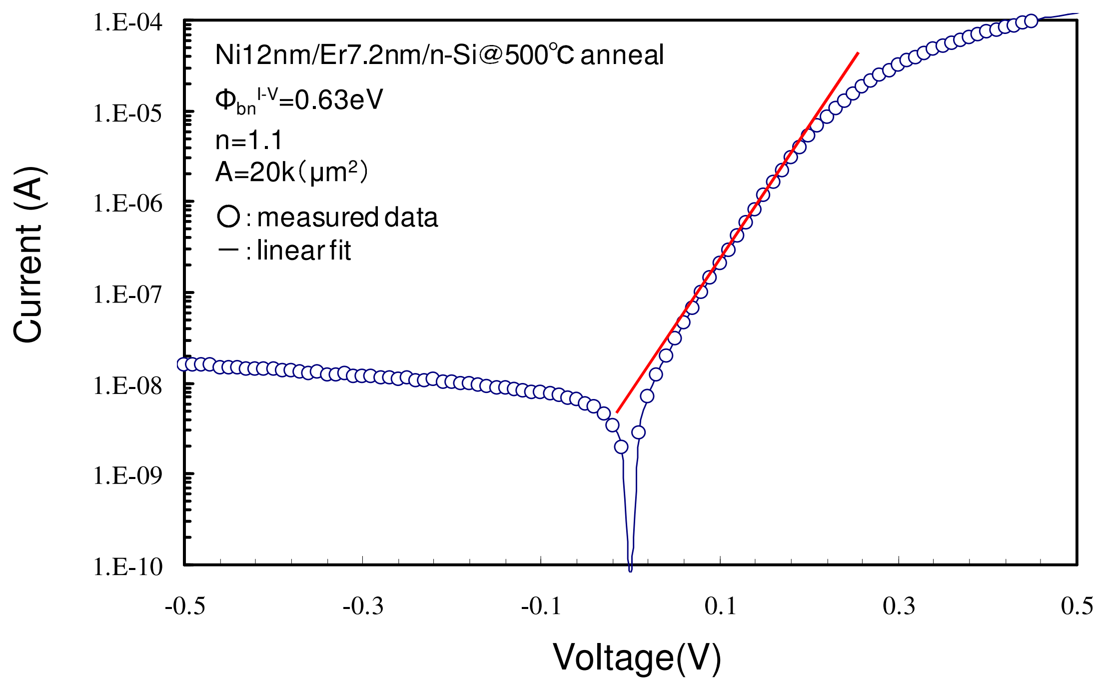
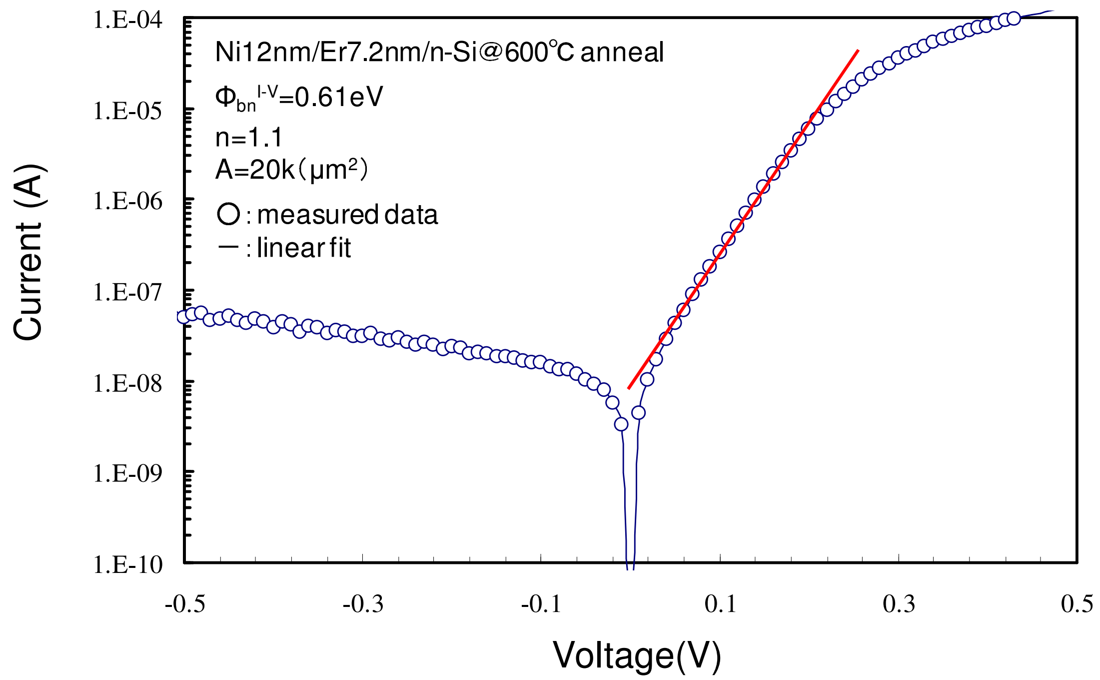


Fig. 4.12 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



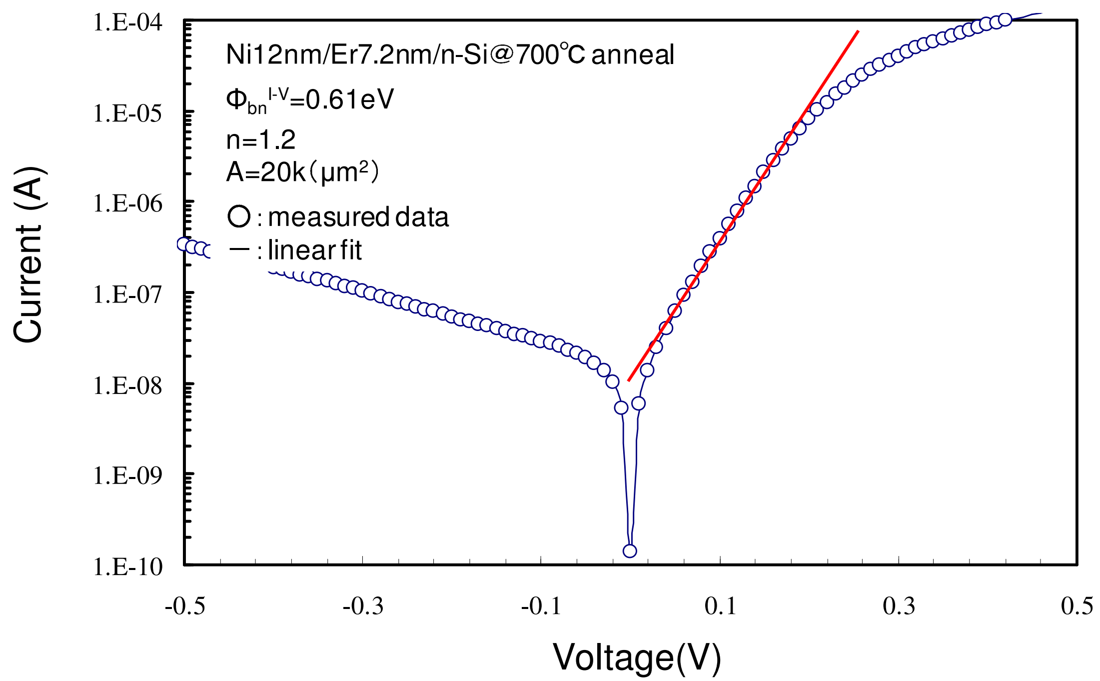
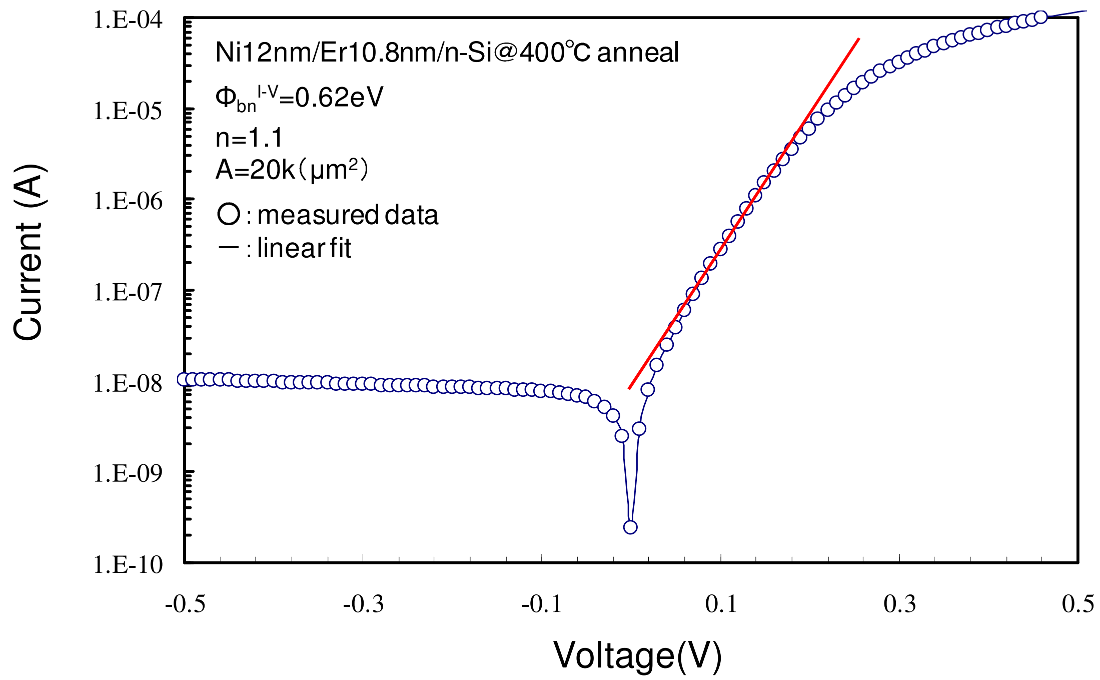


Fig. 4.13 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



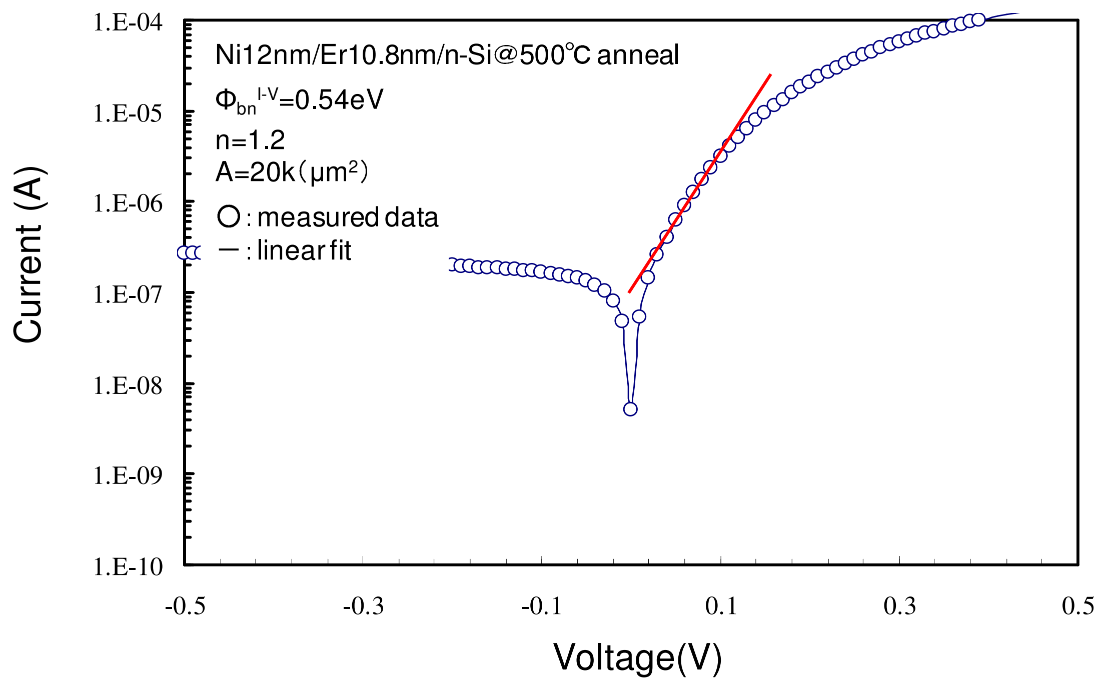
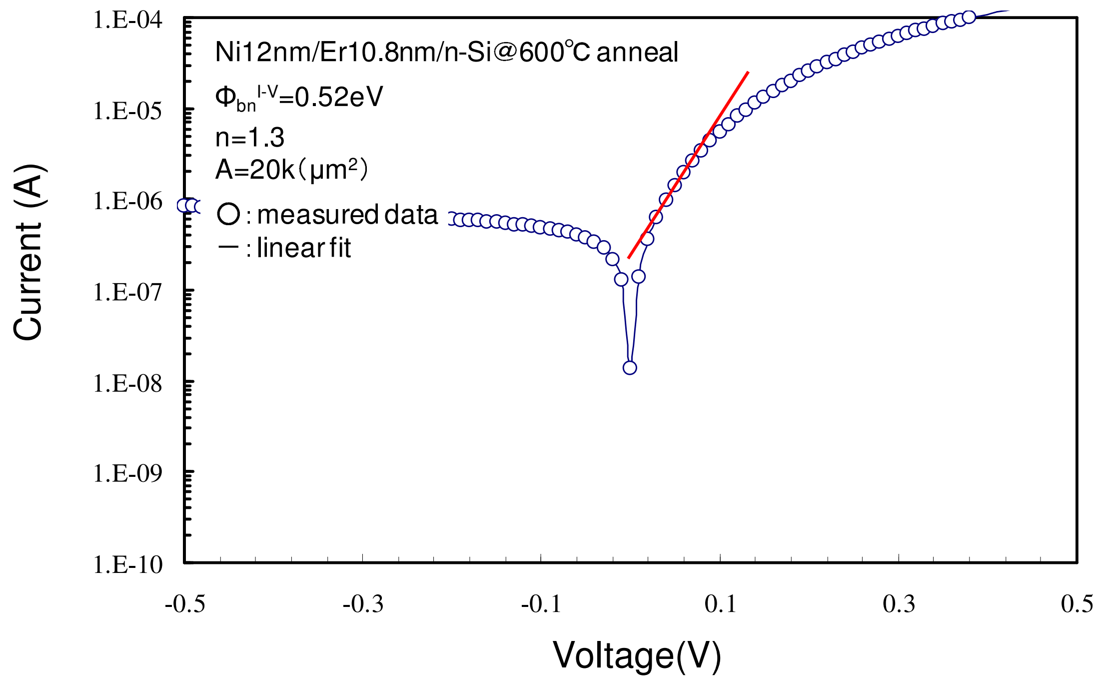


Fig. 4.14 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



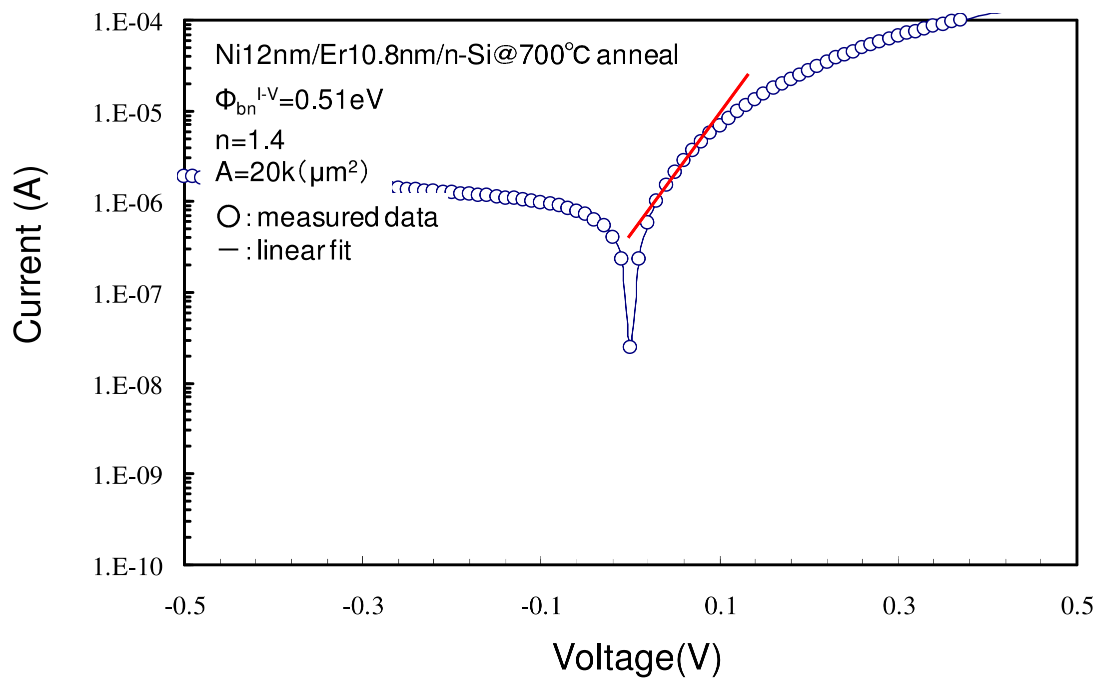
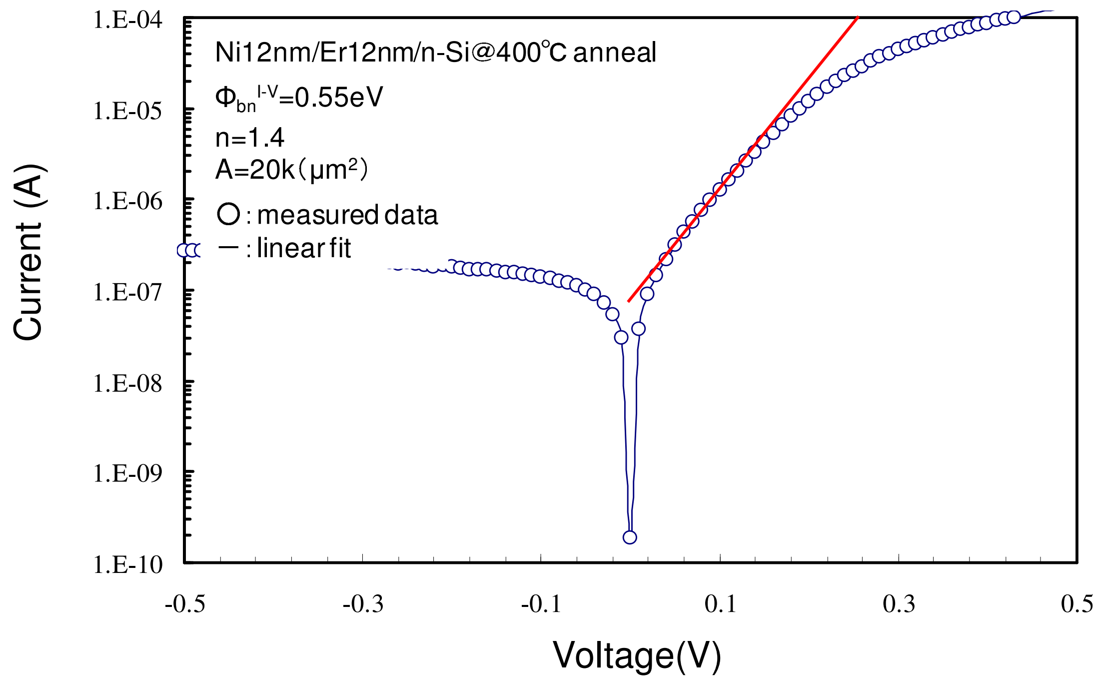


Fig. 4.15 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



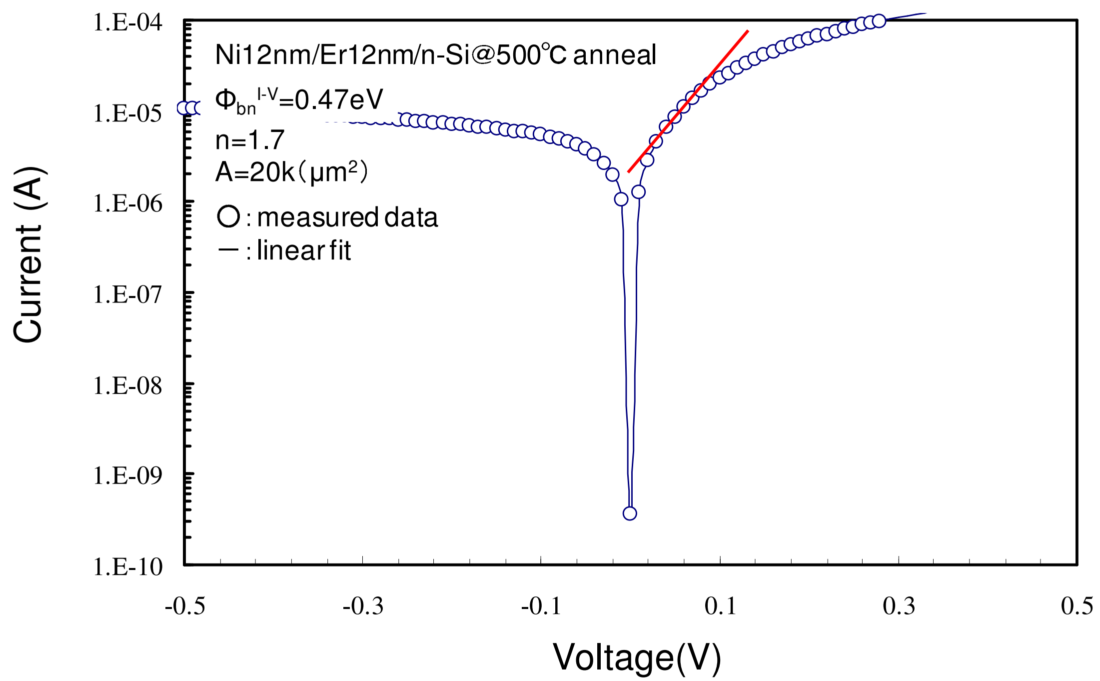
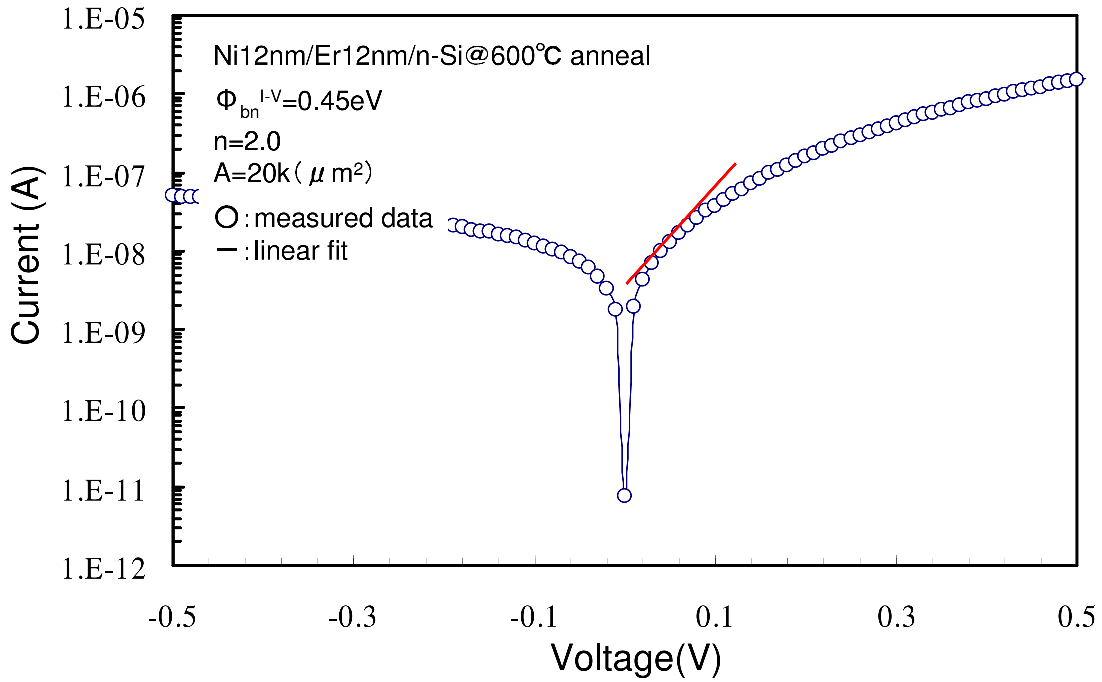


Fig. 4.16 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



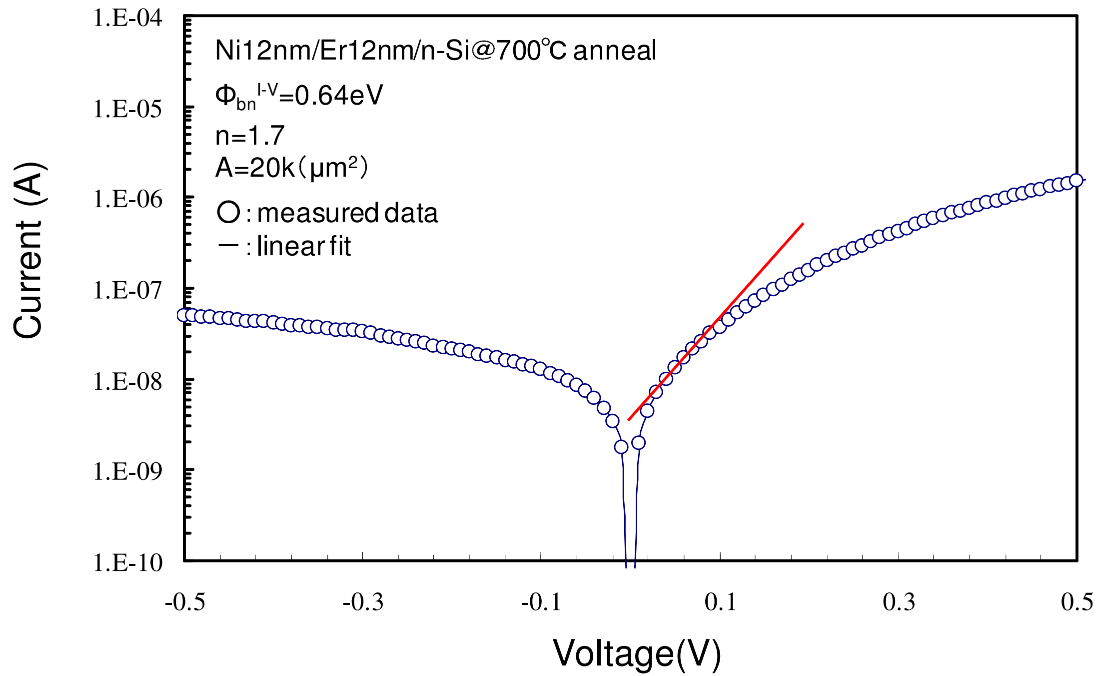
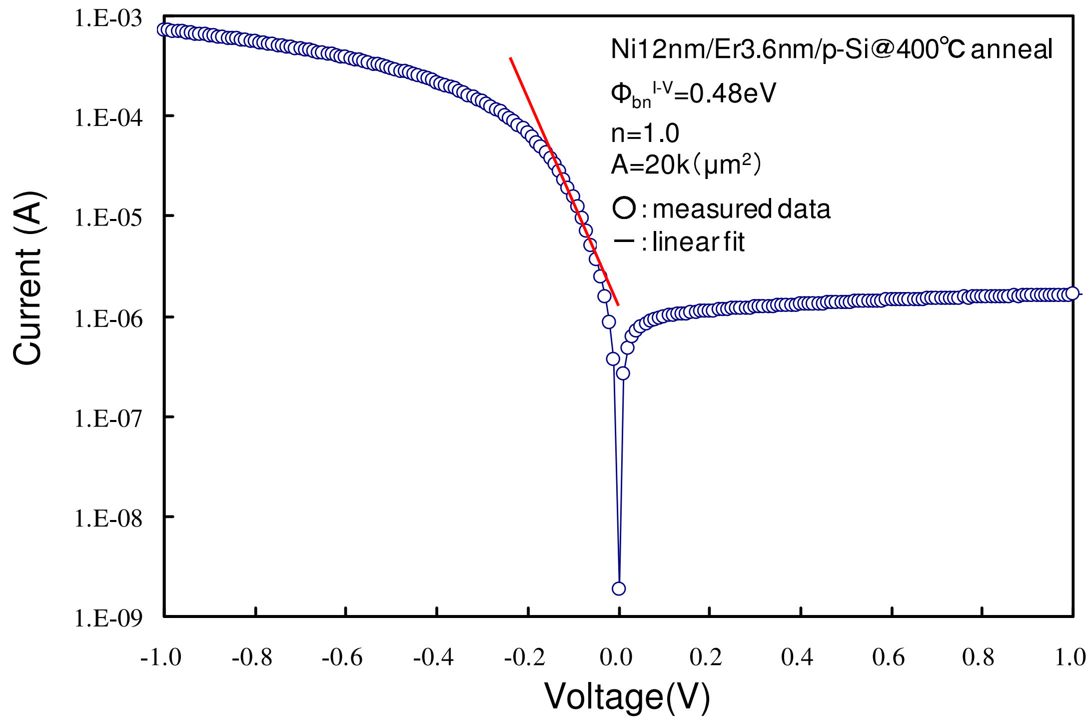


Fig. 4.17 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



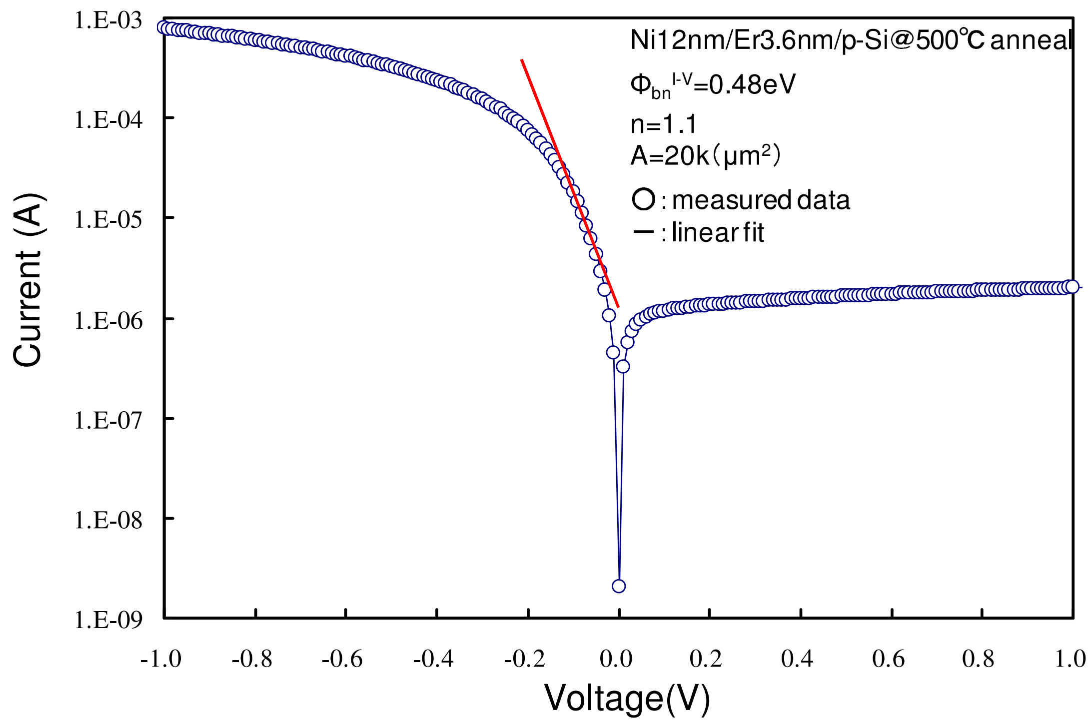
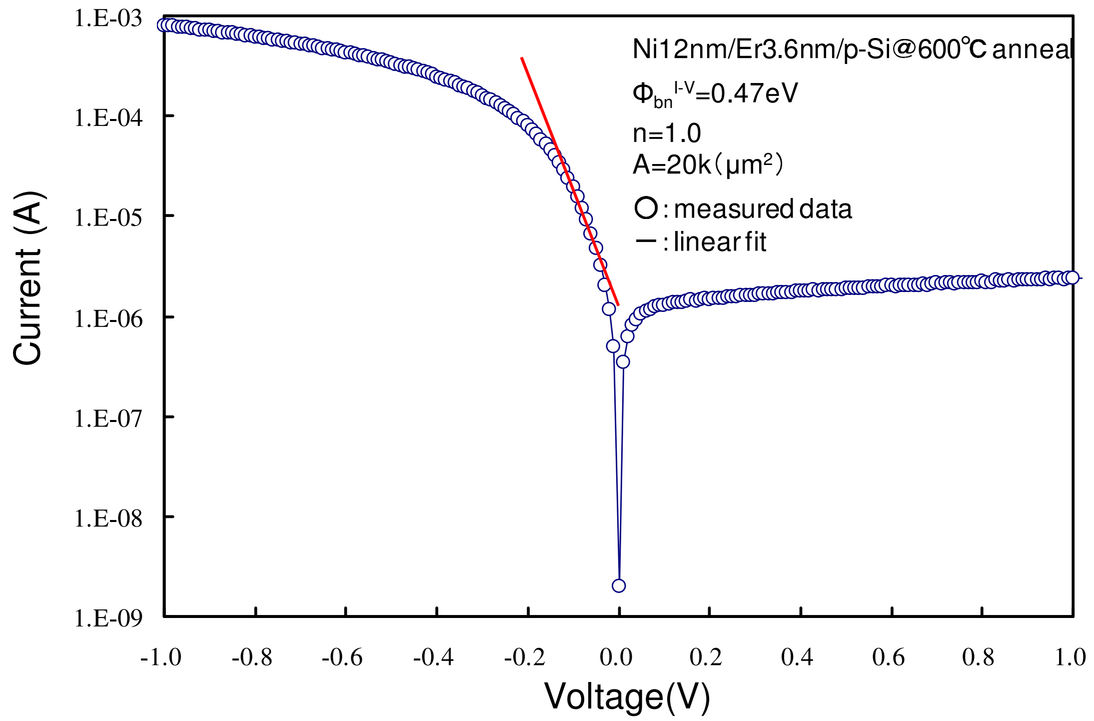


Fig. 4.18 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



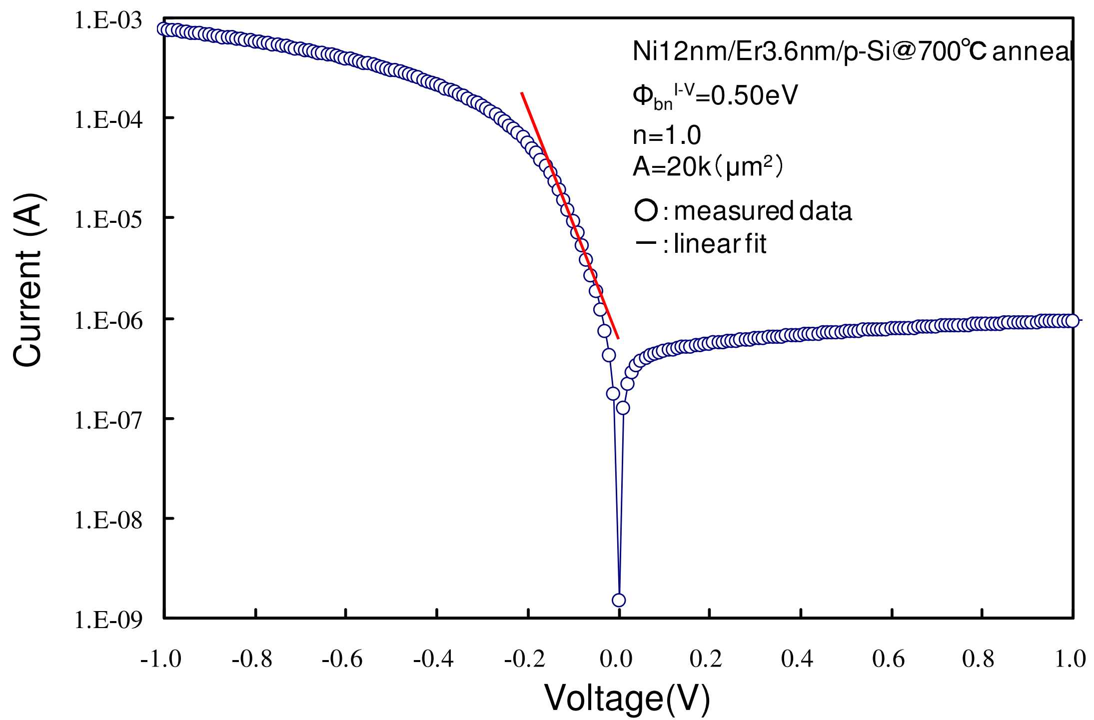
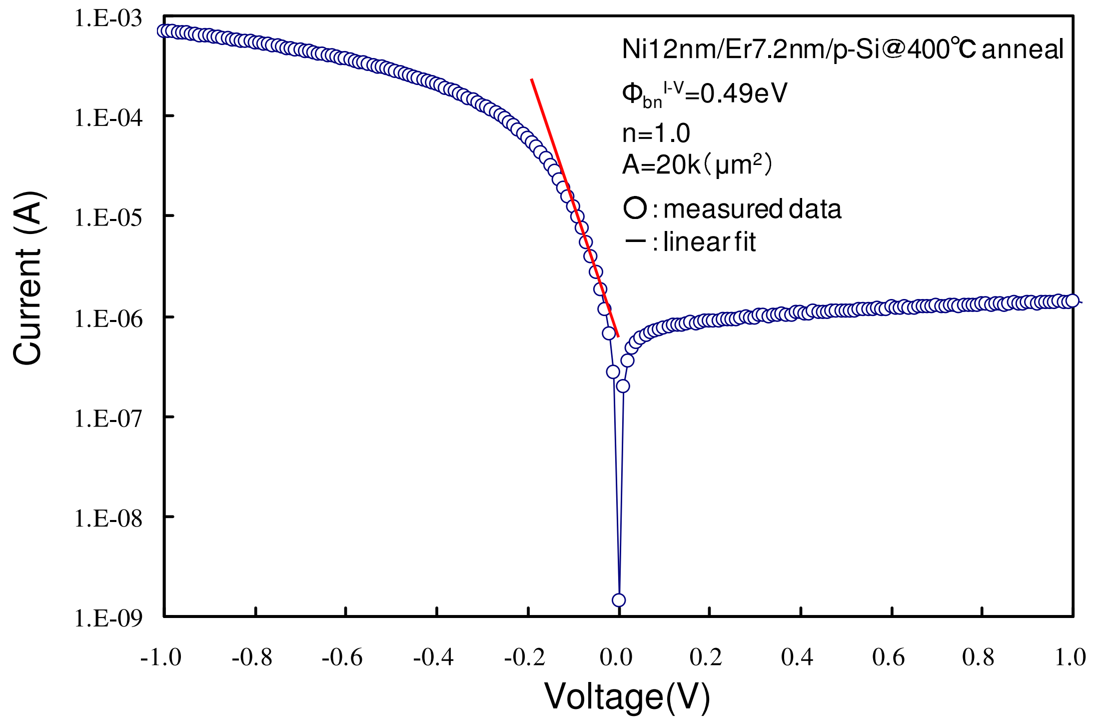


Fig. 4.19 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



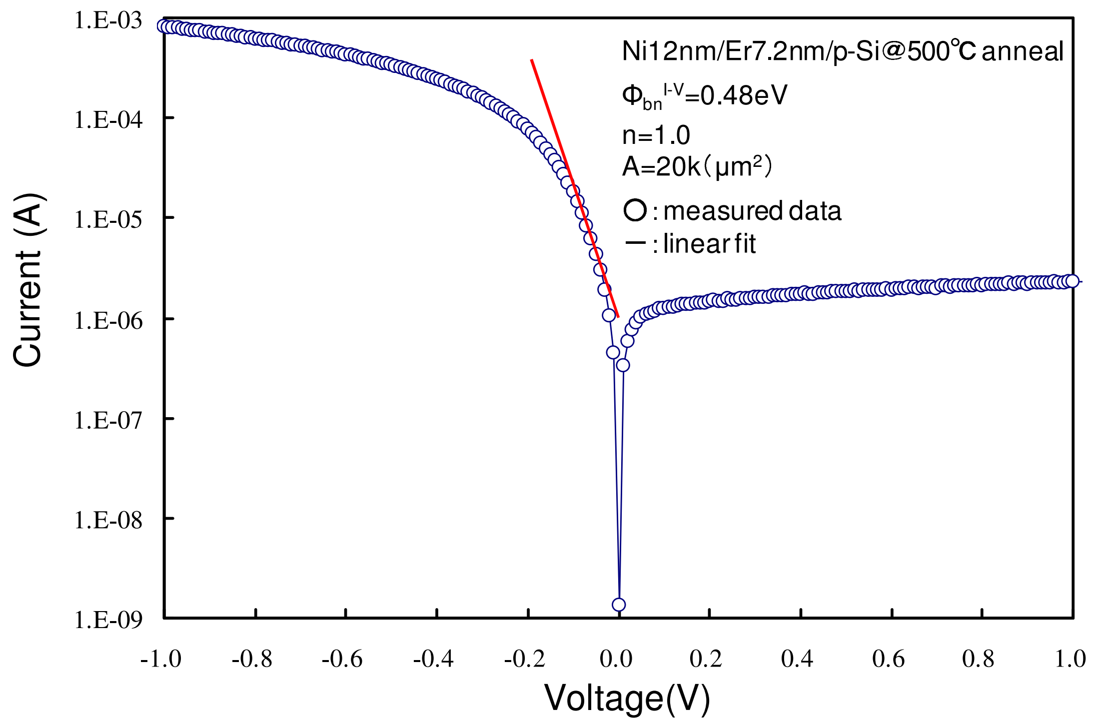
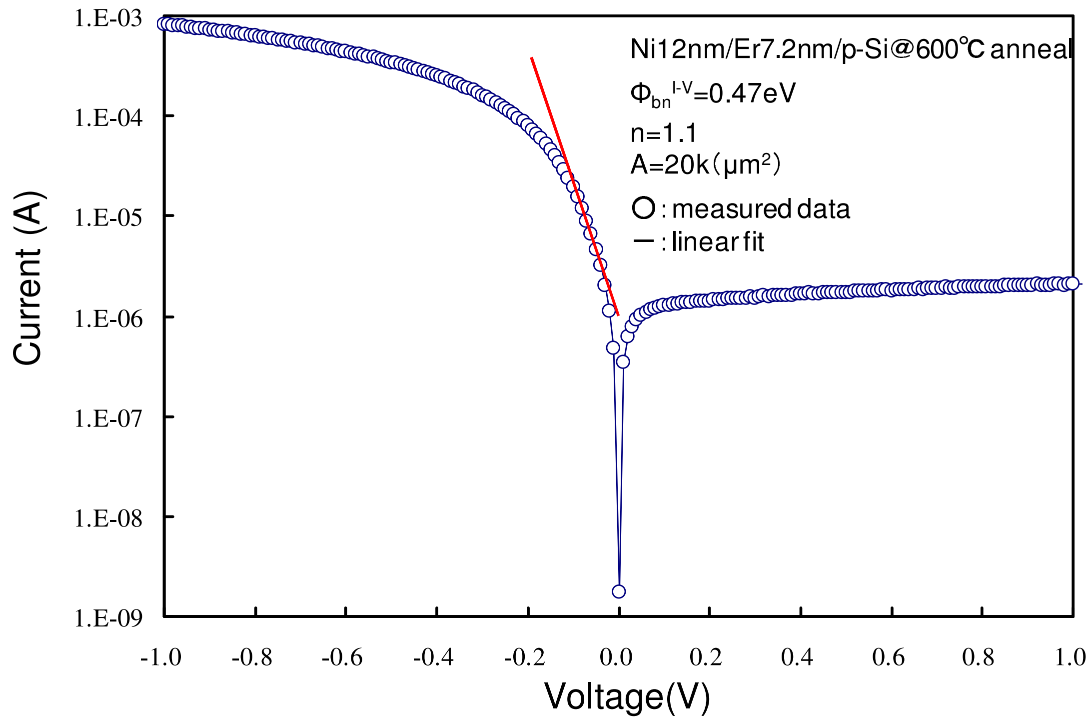


Fig. 4.20 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



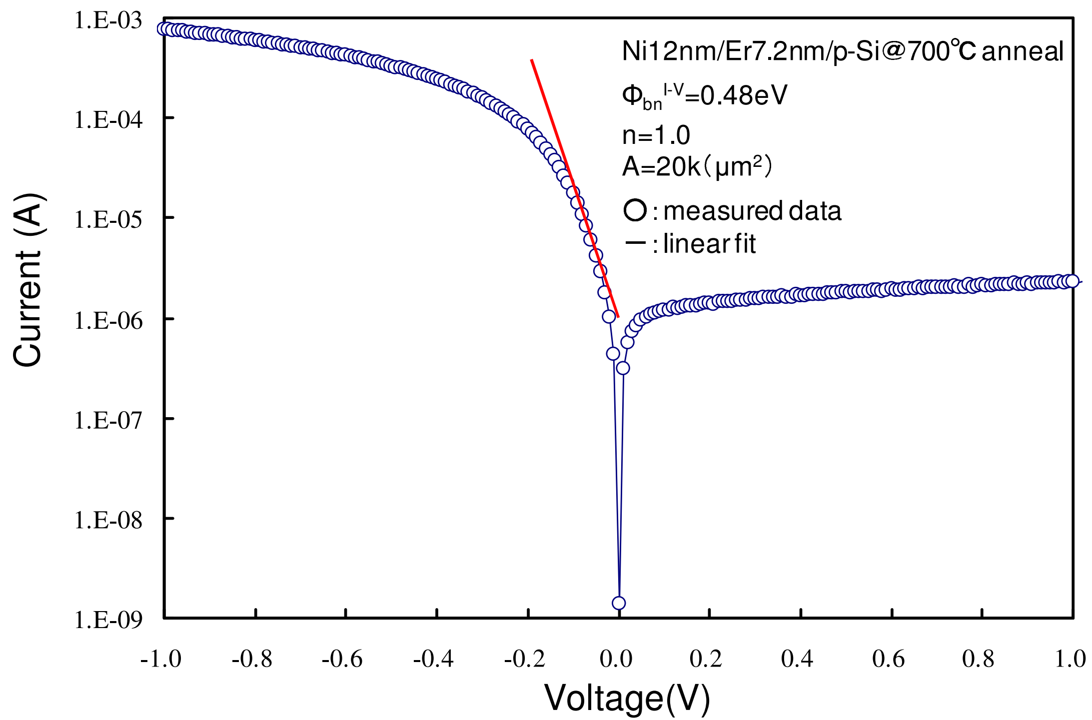
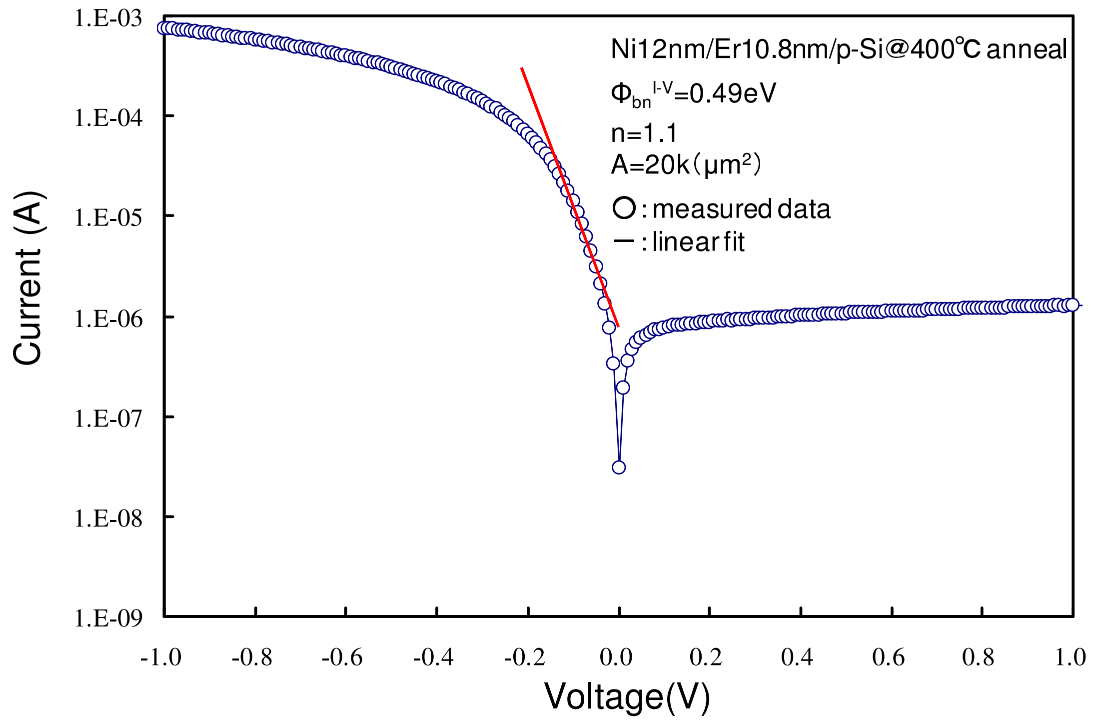


Fig. 4.21 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



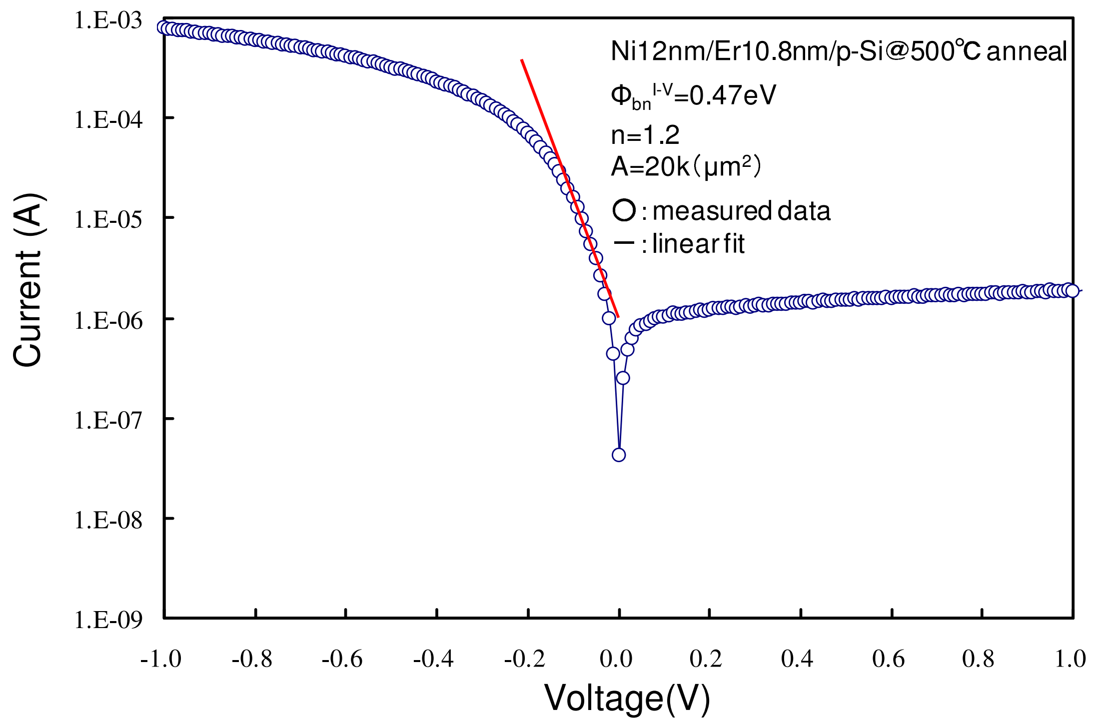
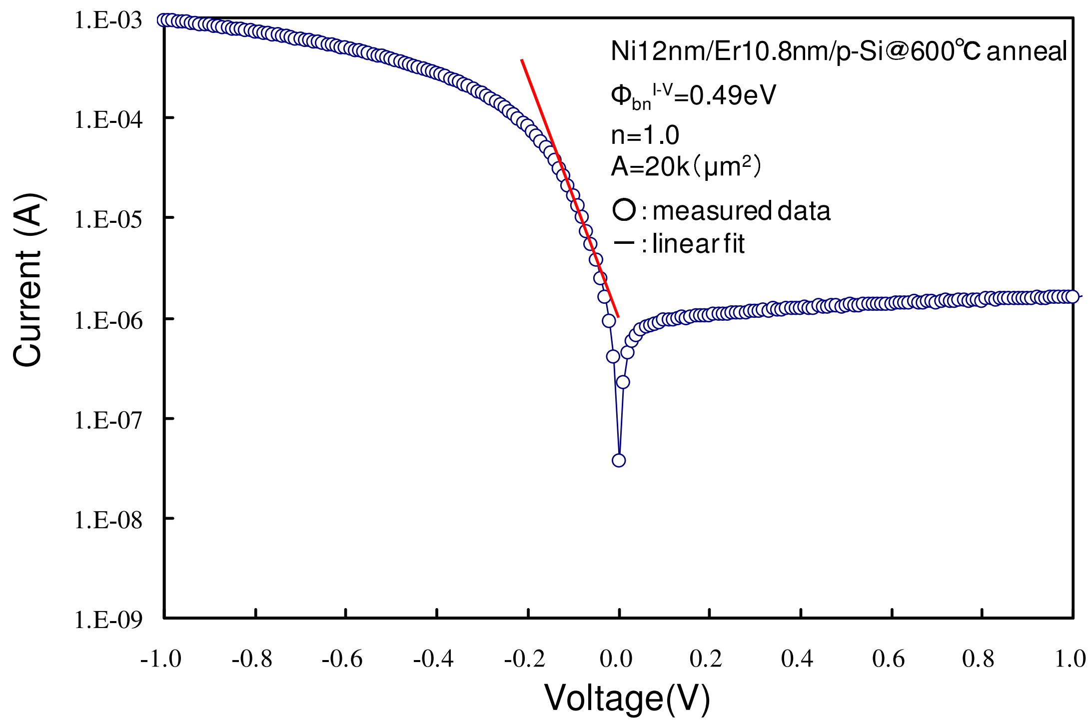


Fig. 4.22 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



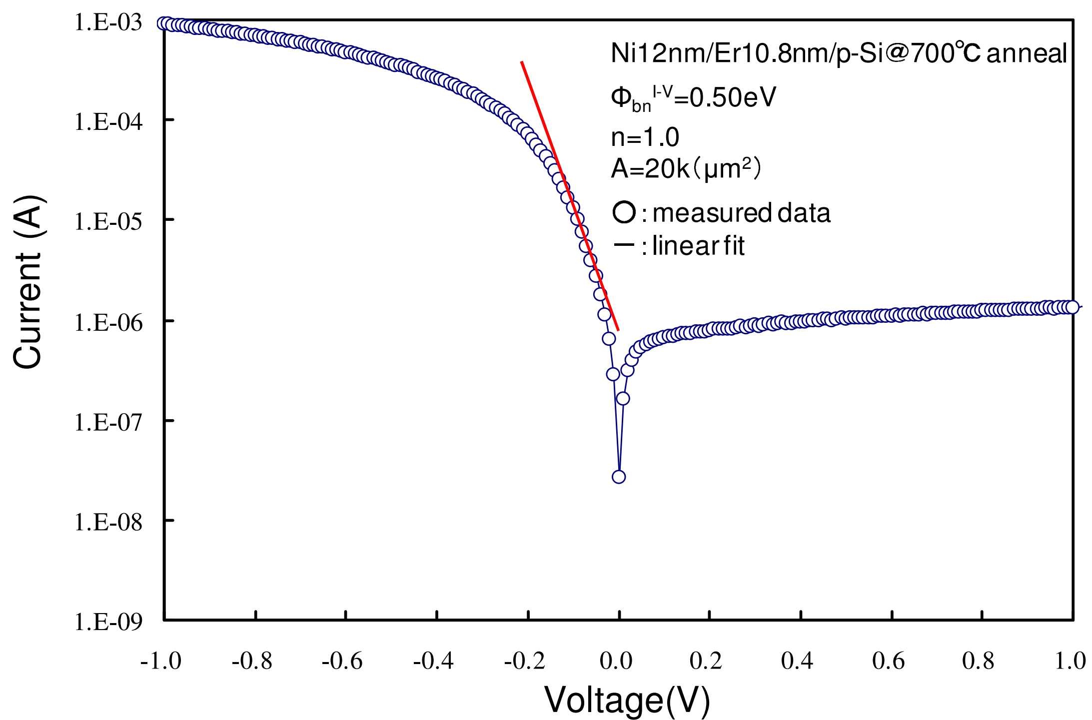
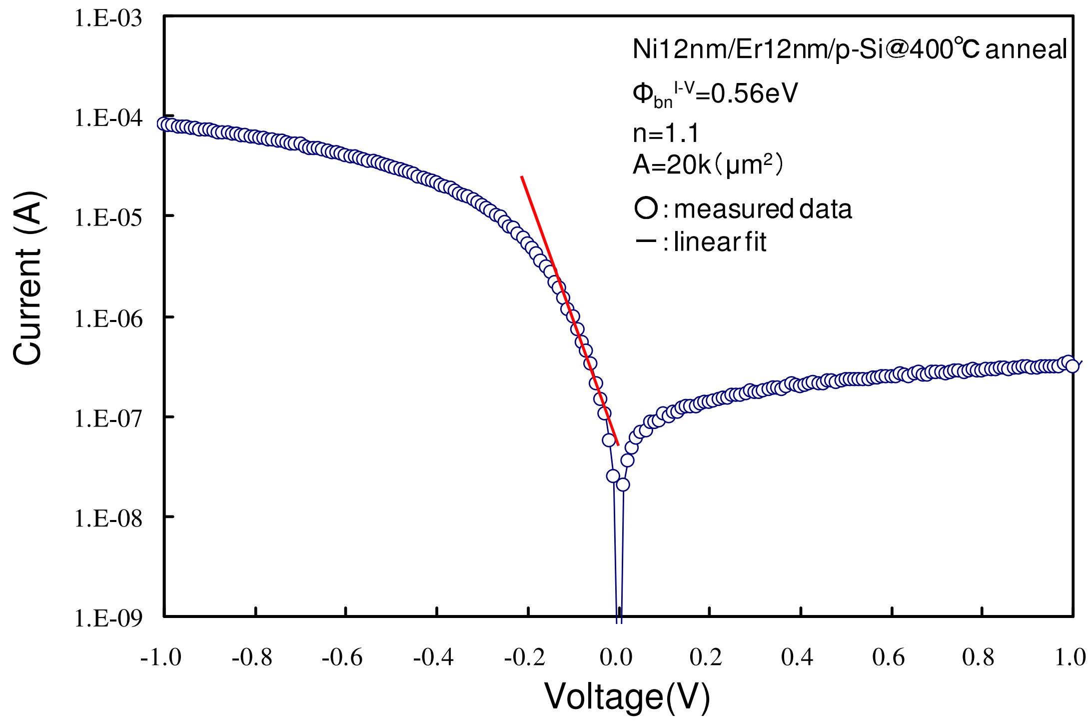


Fig. 4.23 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



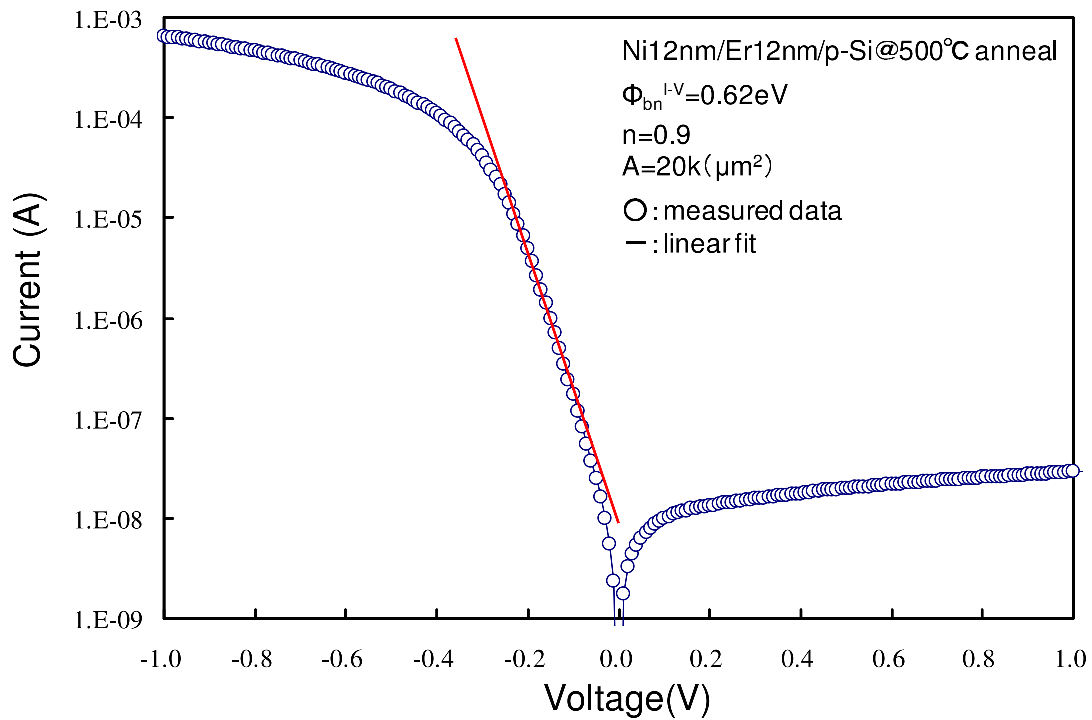
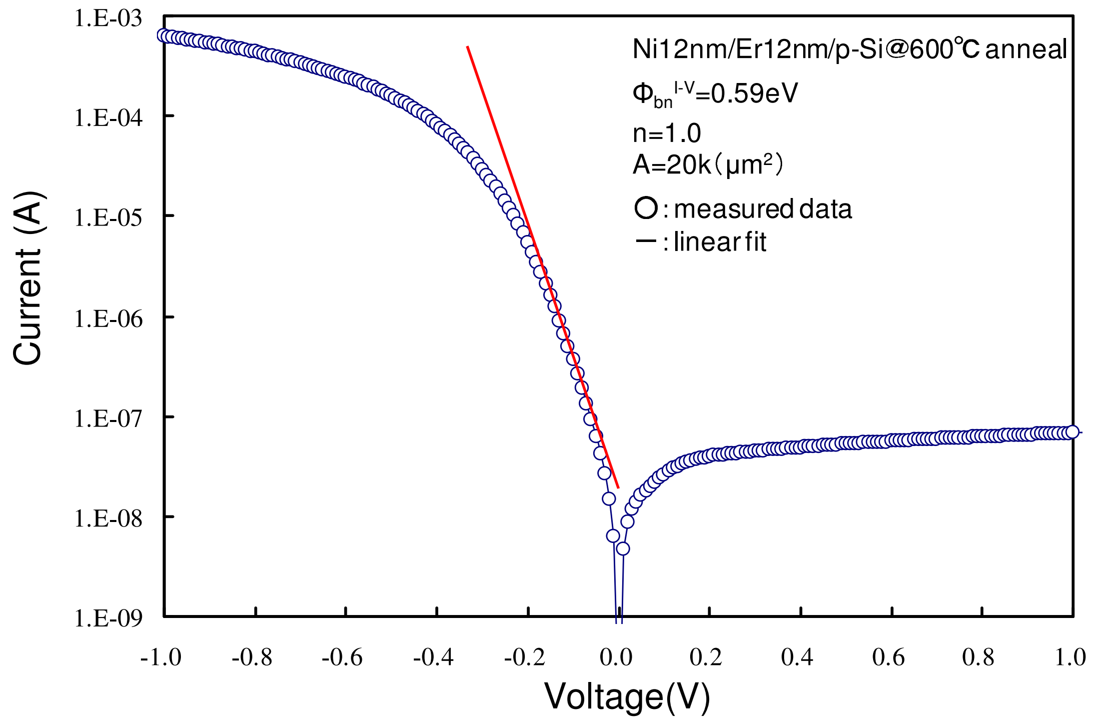


Fig. 4.24 Current-voltage (*I*-*V*) characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



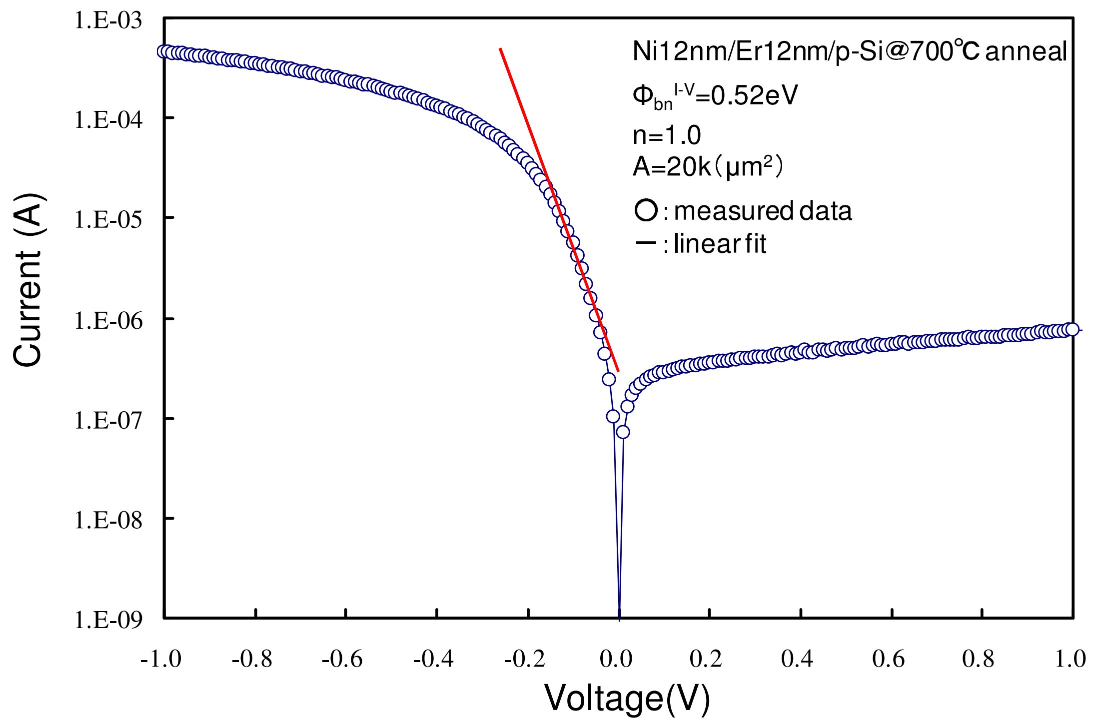


Fig. 4.25 Current-voltage (*I-V*) characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C

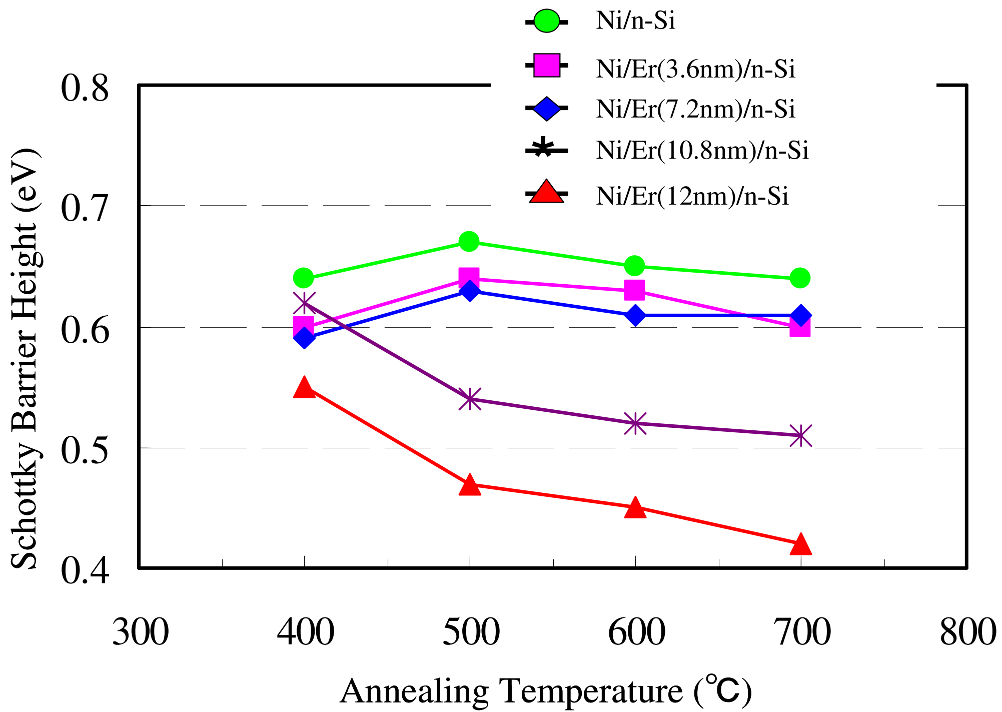


Fig. 4.26 Schottky barrier height for electrons depending on annealing temperatures with various thicknesses of Er interlayer.

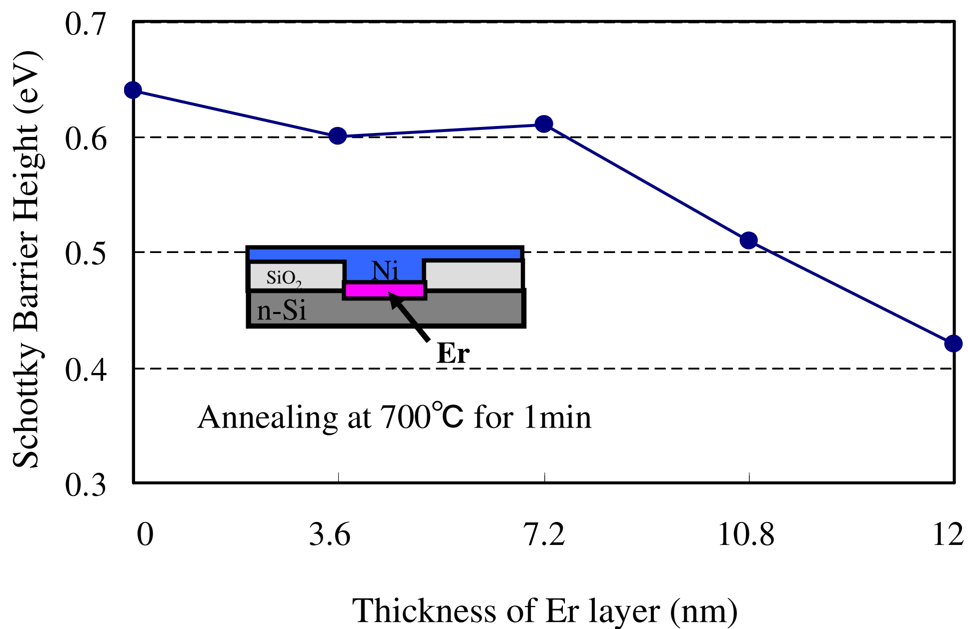
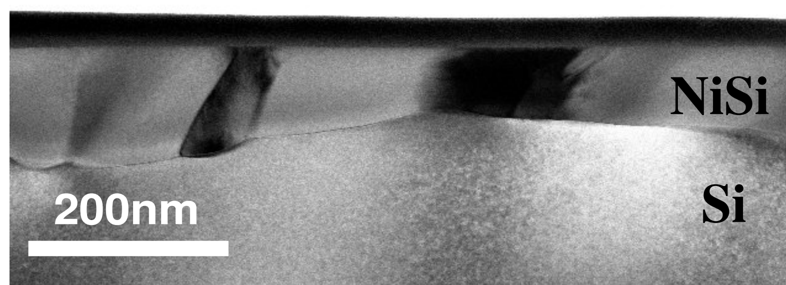


Fig. 4.27 Schottky barrier height of electrons after annealing at 700°C depending on thickness of Er interlayer in the initial layered structure.

4.1.5 Analysis of Schottky Barrier Modulation Er Interlayer

Cross sectional TEM and EDX images are shown in Fig. 4.28. A thin layer was found on the surface of Ni silicide layer in the TEM image. The EDX analysis revealed that the surface layer was mainly composed of segregated Er, however, some amount of Er were contained in the Ni silicide layer below. Origin of the observed Φ_b modulation effect is attributed to the residual Er in the Ni silicide layer.



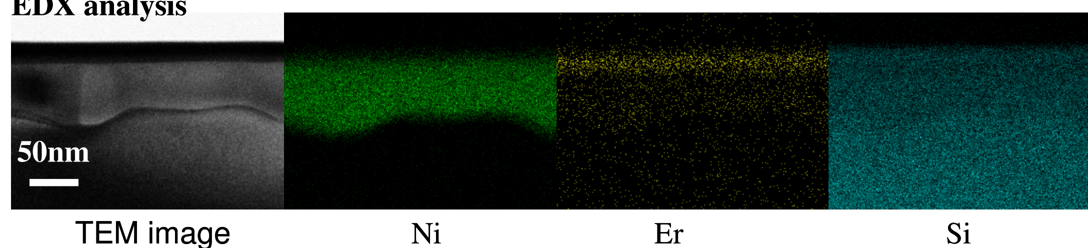


Fig. 4.28 Cross sectional TEM and EDX images of Ni silicide layer formed from the initial layered structure of Ni(100nm)/Er(3.6nm)/Si.

The Φ_b values for electrons evaluated from the *I-V* curves in the forward bias condition are plotted as a function of the annealing time as shown in Fig. 4.29. The values of Φ_b observed were almost same regardless of annealing time. This means that some amount of Er contained in the Ni silicide layer didn't move away after annealing for a long time. Er maybe remains in Ni silicide after silicidation.

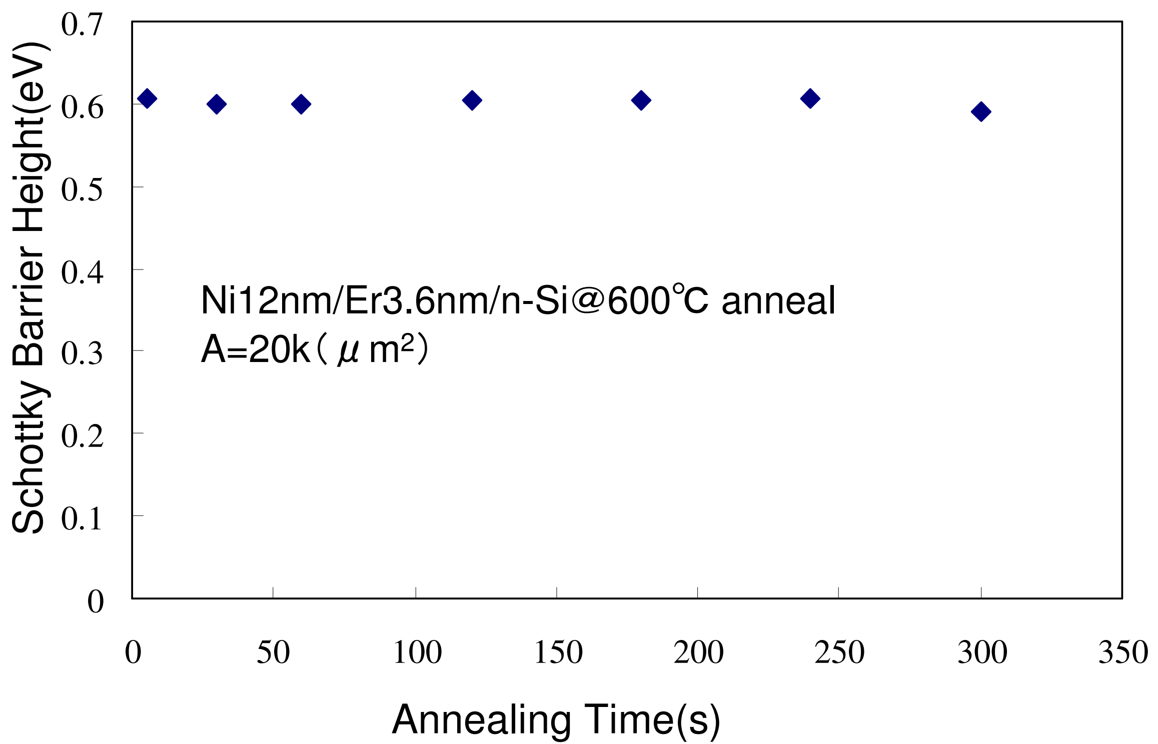
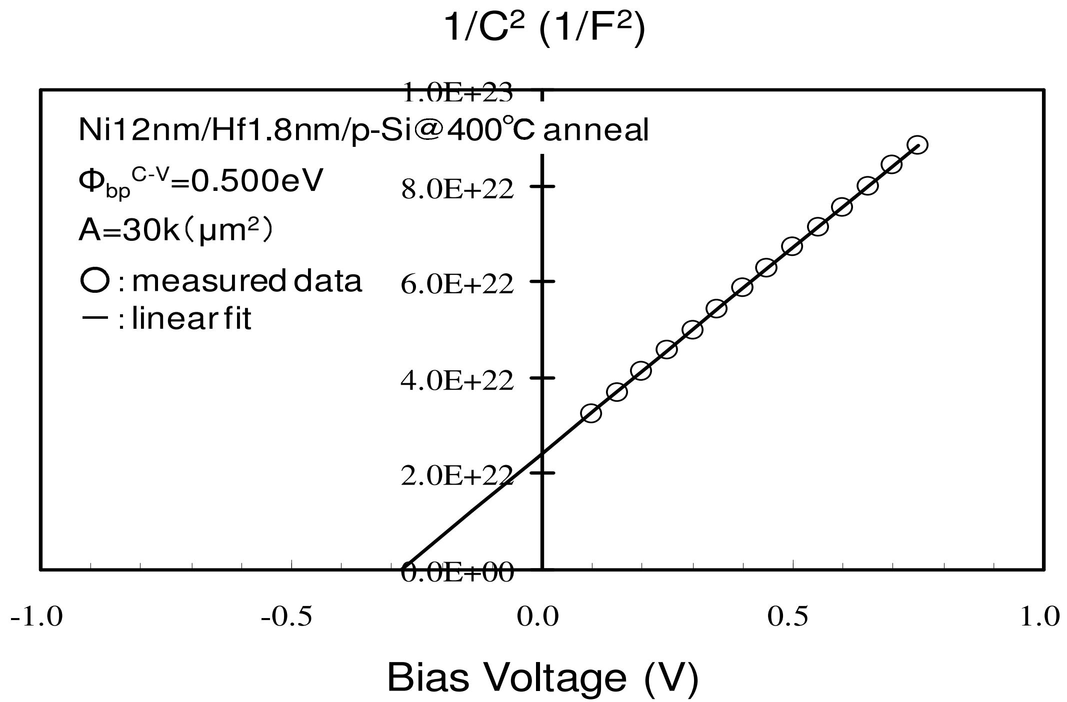


Fig. 4.29 Schottky barrier height of electrons depending on annealing time in the initial layered structure.

4.1.6 Characteristics of Ni Silicide Schottky Diode with Hf Interlayer

Typical capacitance-voltage ($1/C^2$-V) curves of Schottky diodes of annealing temperature from 400°C to 700°C fabricated from the Ni/Hf/p-Si structure are shown in Fig. 4.30-4.35. The Φ_b values for holes evaluated from the $1/C^2$-V corves in the reverse bias region are plotted as a function of the annealing temperature as shown in Fig. 4.36. The values of Φ_b observed from the layered deposition structures with the Hf interlayer were lower by 0.04-0.21eV compared with those without the Hf interlayer, and the highest Φ_b of 0.663 eV was achieved for the sample with 7.2-nm-thick Hf interlayer annealed at 700°C. For the constant annealing temperature of 700°C, the Φ_b value increased with increasing of the Hf interlayer thickness, and 0.21 eV increasing was obtained for 7.2-nm-thick Hf, as shown in Fig. 4.37.



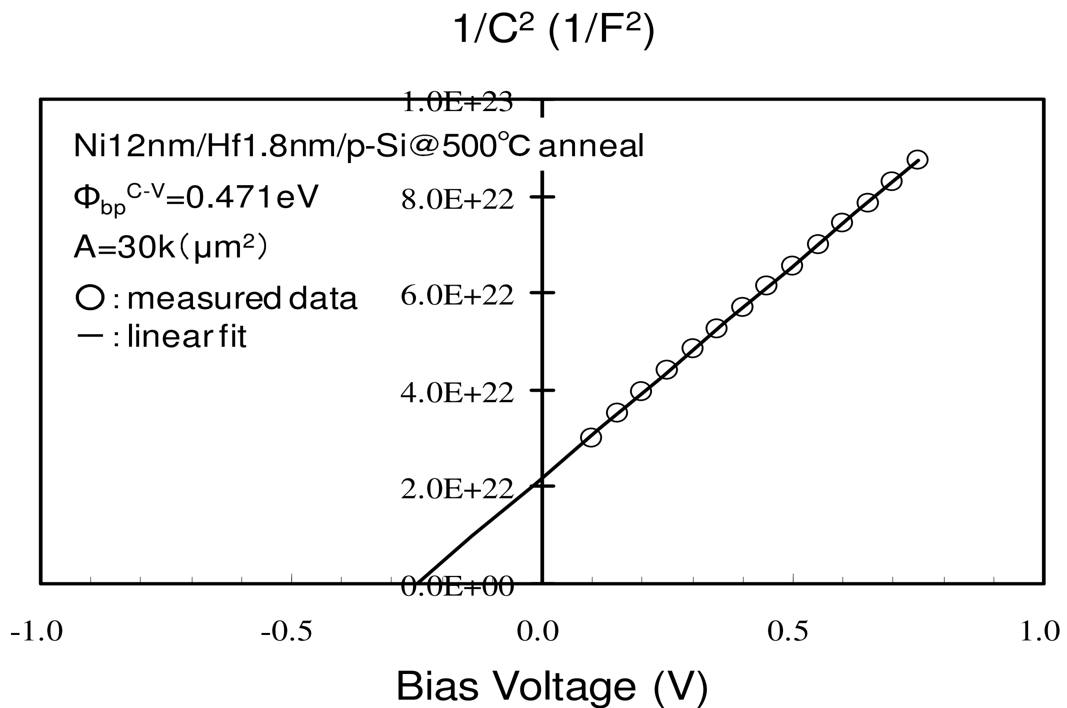
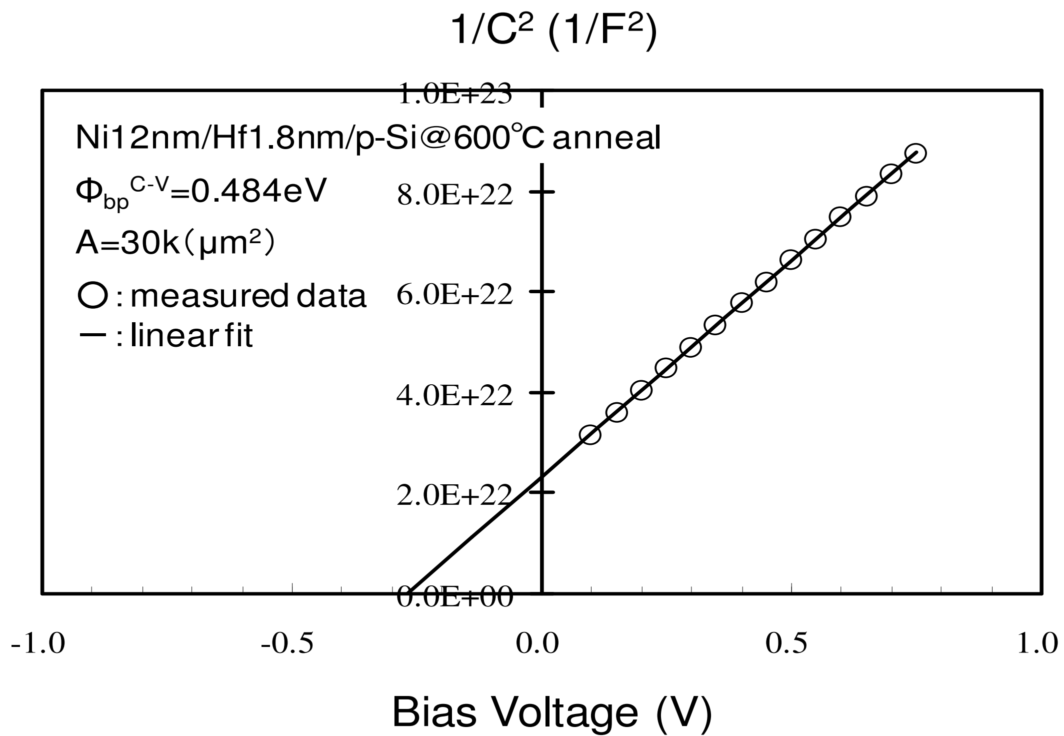


Fig. 4.30 $1/C^2$-V characteristics of Schottky diodes at annealing temperatures of 400^oC and 500^oC



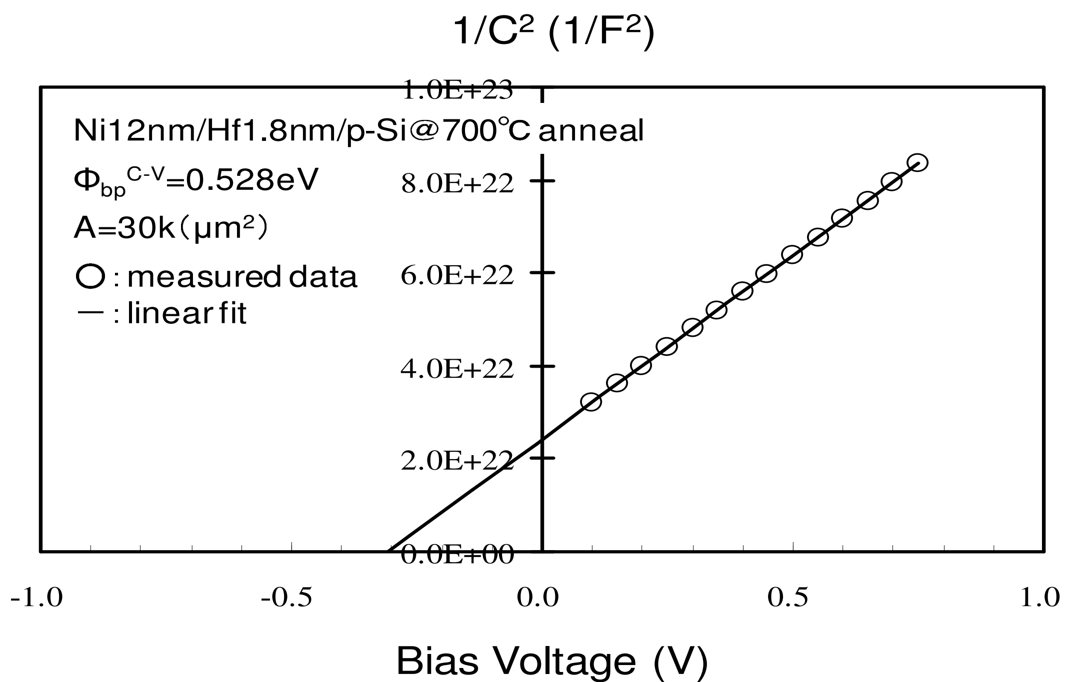
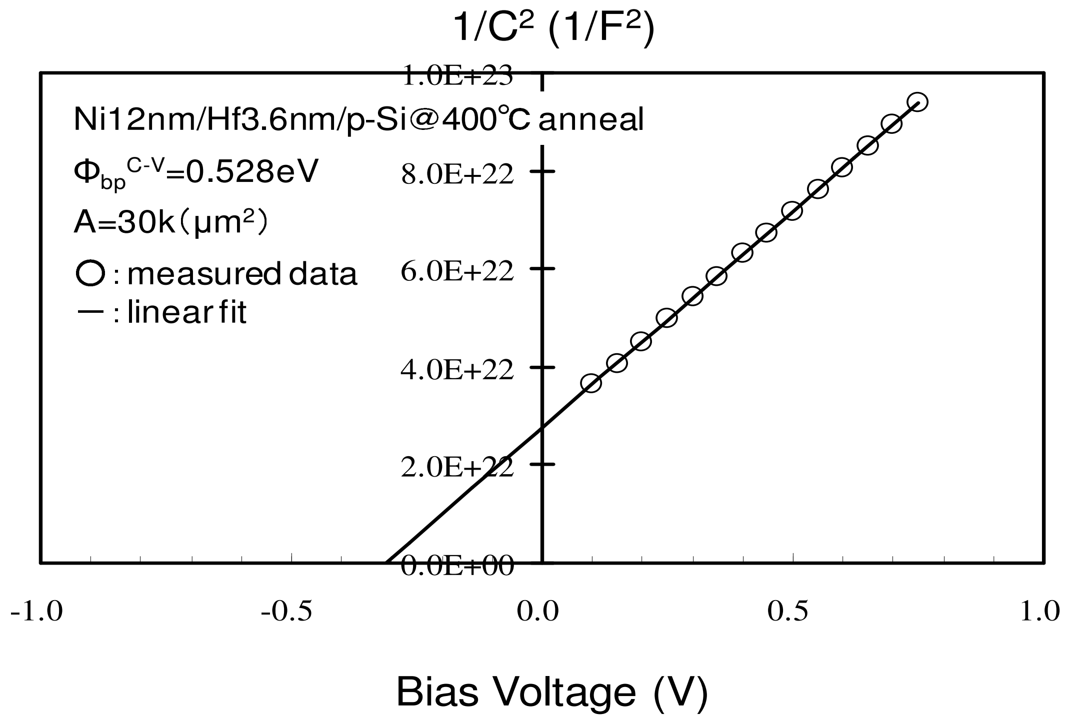


Fig. 4.31 $1/C^2$-V characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



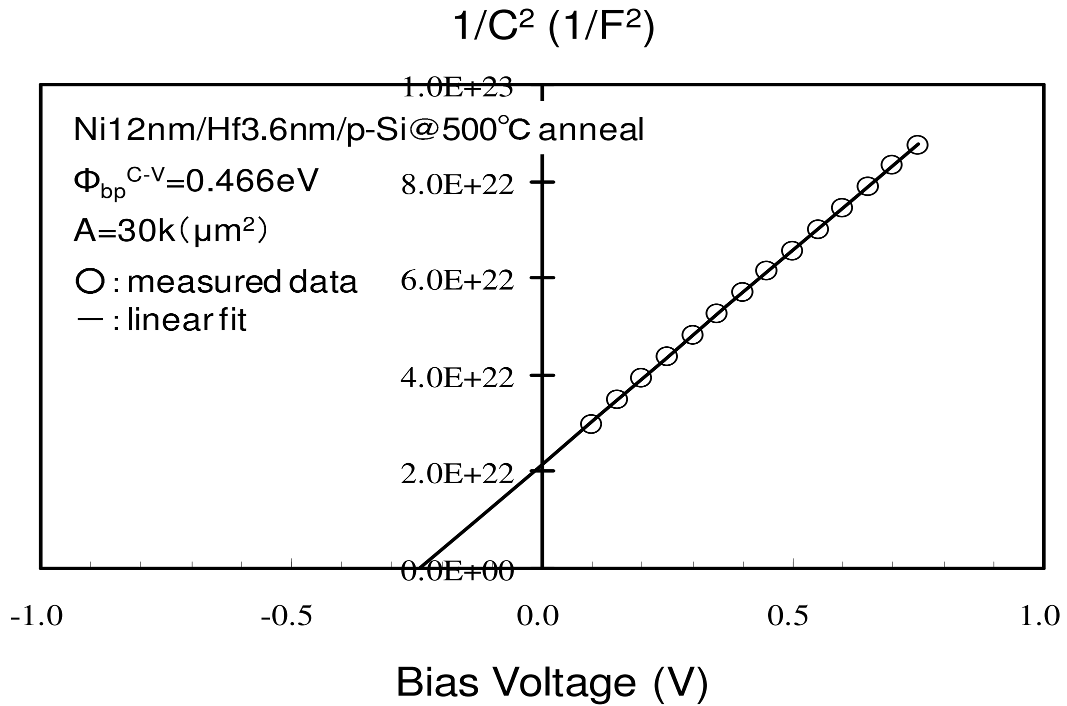
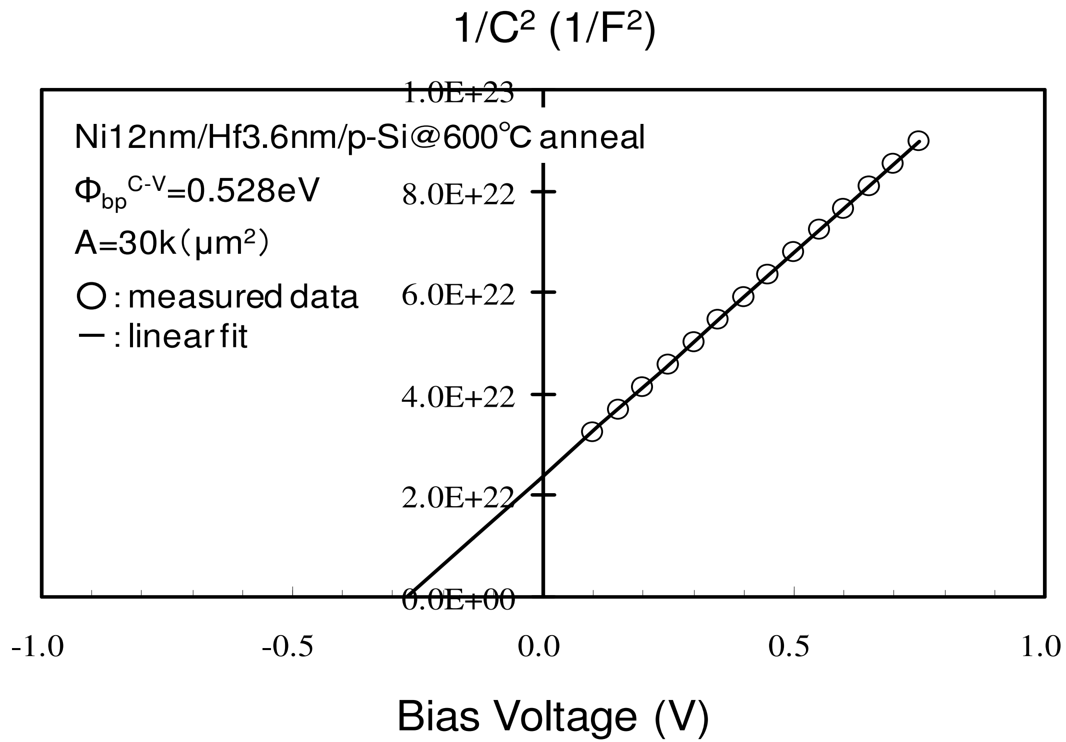


Fig. 4.32 $1/C^2$-*V* characteristics of Schottky diodes at annealing temperatures of 400°C and 500°



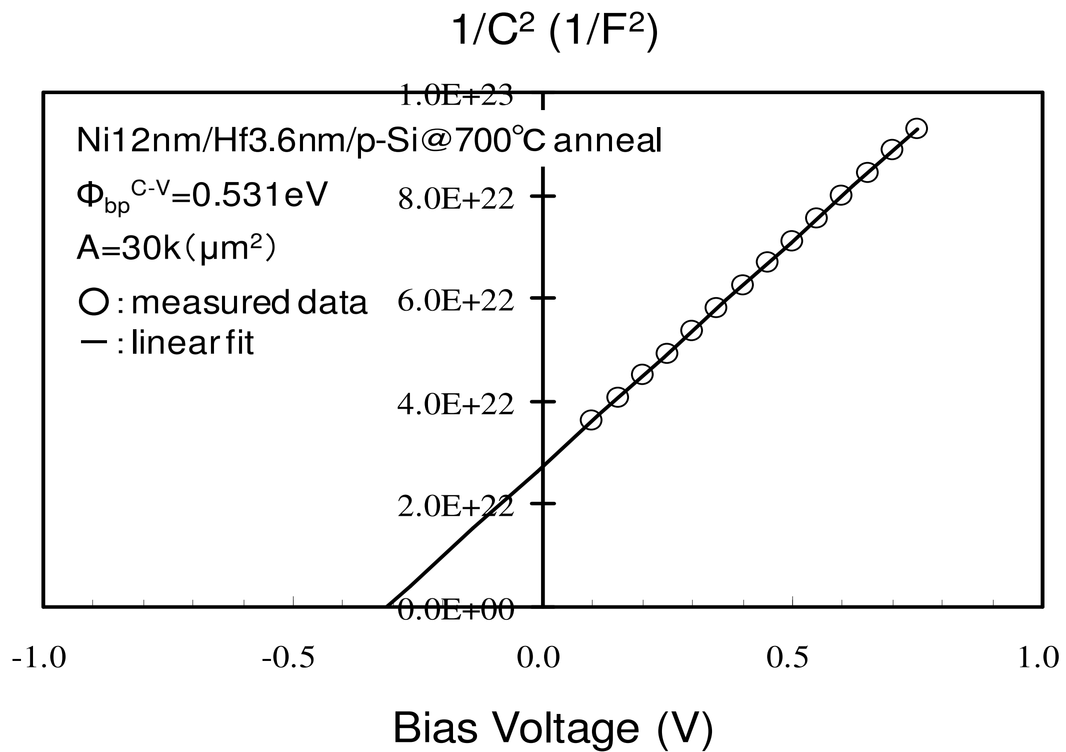
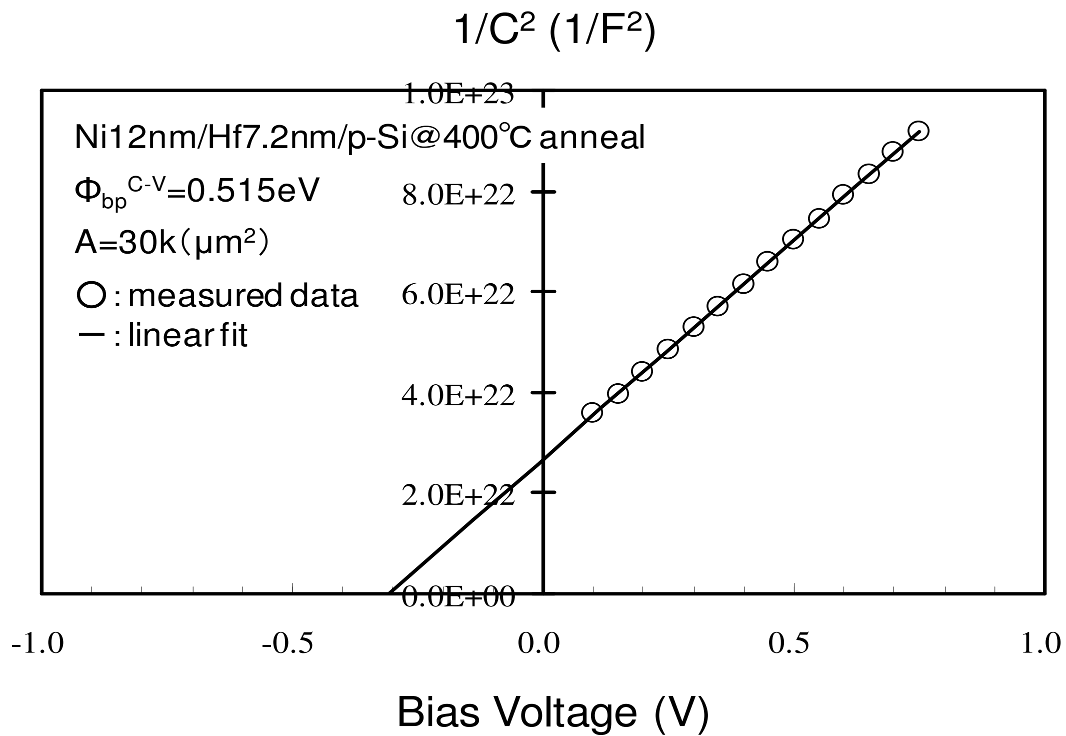


Fig. 4.33 $1/C^2$-V characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C



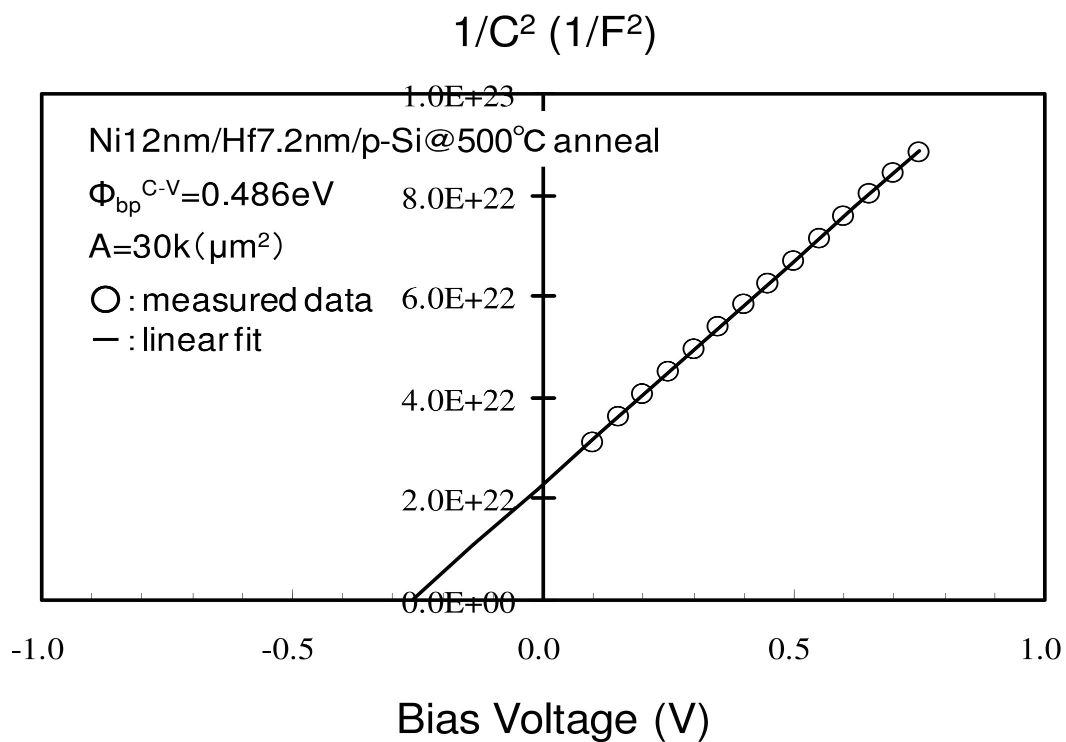
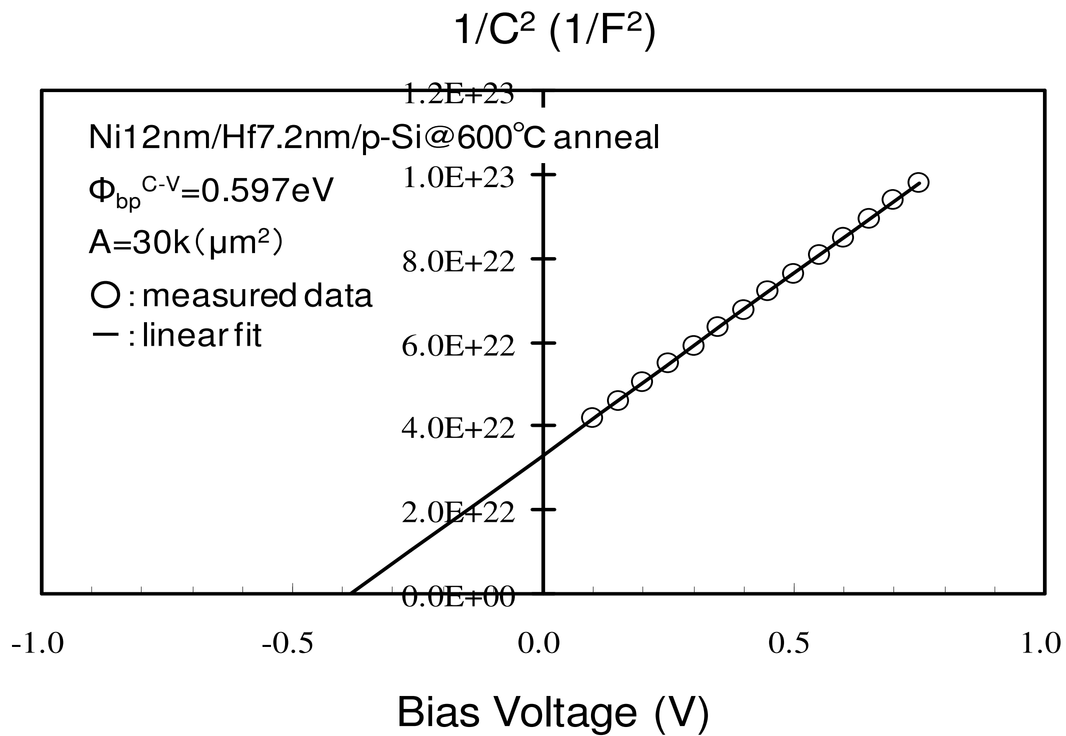


Fig. 4.34 $1/C^2$-V characteristics of Schottky diodes at annealing temperatures of 400°C and 500°C



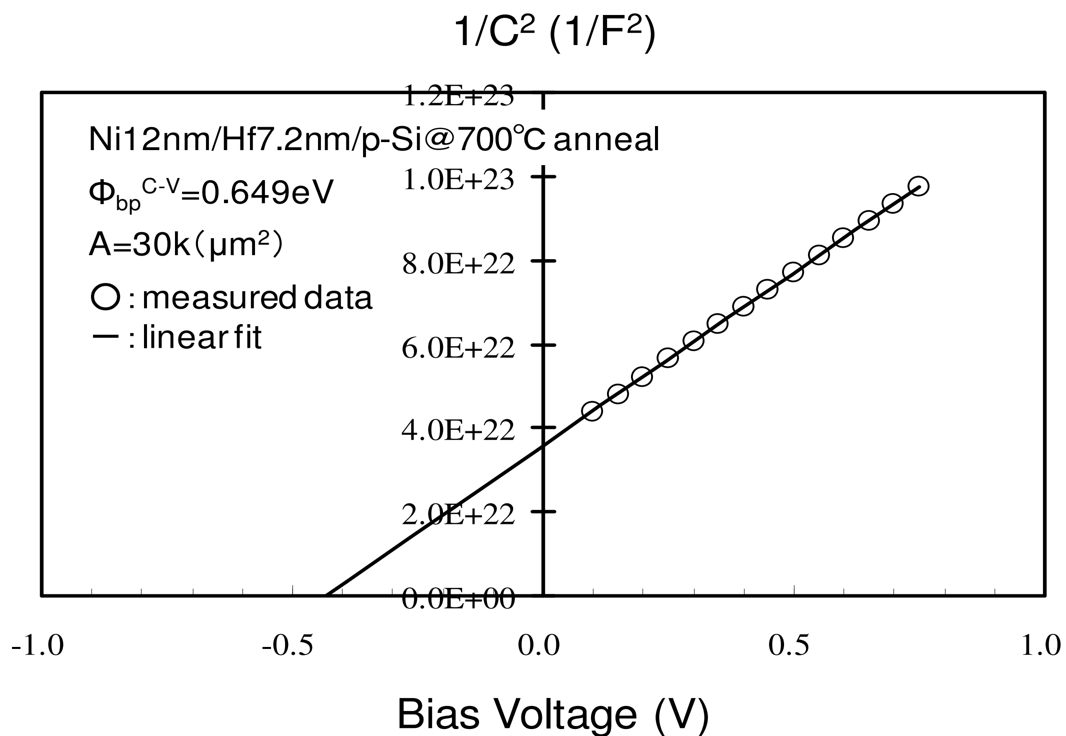


Fig. 4.35 $1/C^2$-V characteristics of Schottky diodes at annealing temperatures of 600°C and 700°C

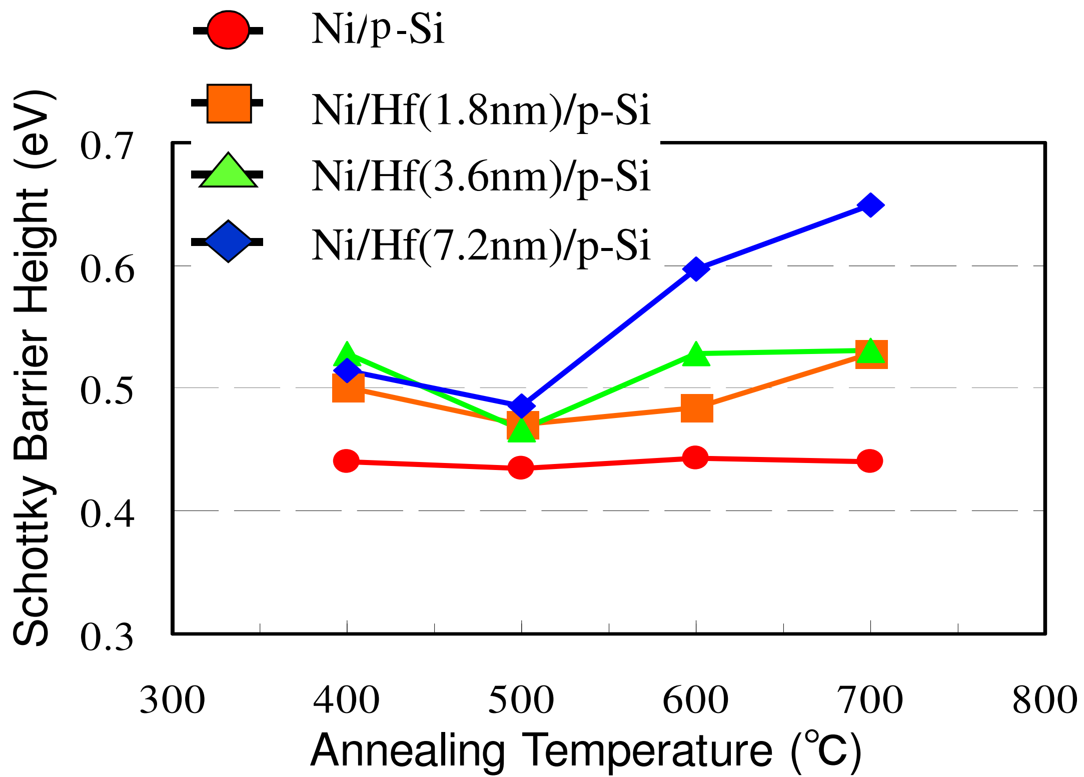


Fig. 4.36 Schottky barrier height for electrons depending on annealing temperatures with various thicknesses of Hf interlayer.

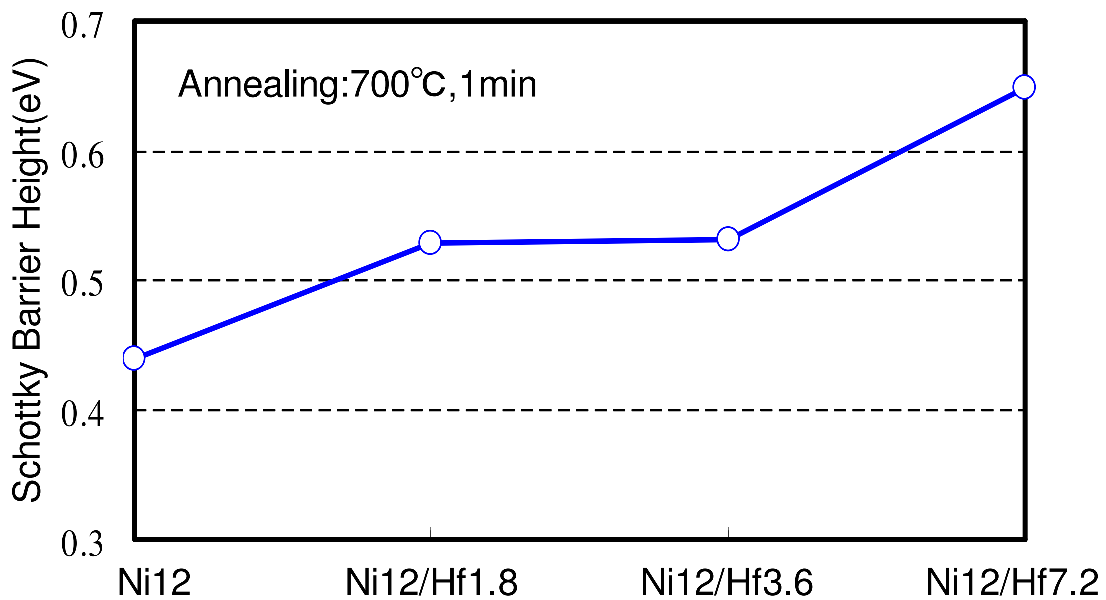


Fig. 4.37 Schottky barrier height of electrons after annealing at 700°C depending on thickness of Hf interlayer in the initial layered structure.

4.1.7 Analysis of Ni Silicide with Hf Interlayer

The annealing temperature dependence of the sheet resistances of Ni/p-Si, Ni/Hf1.8/p-Si and Ni/Hf7.2/p-Si structures was shown in Fig. 4.38. In the case of Hf insertion, the sheet resistance increased compared with Ni/p-Si structure because Hf interlayer was blocked a silicidation from NiSi to $NiSi_2$. Hf interlayer blocked a supply of Ni for silicidation, then the $NiSi_2$ phase was easily forwed. The sheet resistance increases sharply from Ni mono silicide (NiSi) to Ni dai silicide ($NiSi_2$) at about 750℃ though, in the case of Hf insertion, the sheet resistance was constant. This means that a thermal stability of silicide is improved by Hf insertion. The sheet resistance of the structures with Hf interlayer was so high under 600℃. This maybe because the silicidation of Hf did not start yet at this temperature.

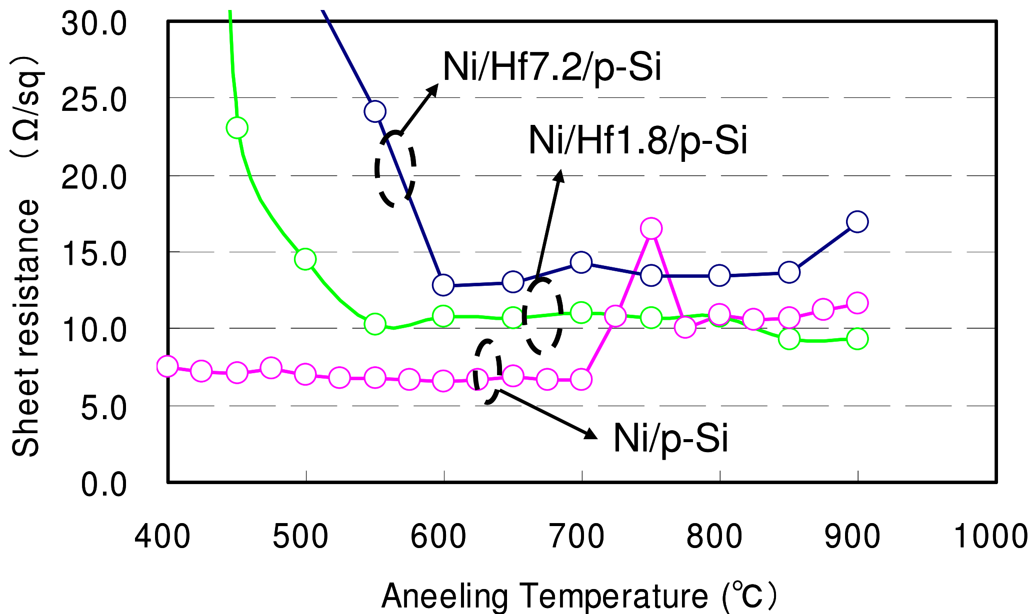


Fig. 4.38 The sheet resistances of silicides depending on the annealing temperature

Chapter 5

SCHOTTKY BARRIER MOSFET WITH Er INTERLAYER

5.1 Introduction

The Schottky barrier source/drain MOSFET (SB-MOSFET) is one of promising candidates for next generation devices, thanks to its shallow junction depth with low electrode resistance and low process temperature [3,4]. However, the high barrier height (Φ_b) severely limits the drive current of SB-MOSFETs [14,15]. The Er silicide has been proposed for n-channel SB-MOSFETs because of very low Φ_b of 0.27-0.36 eV for electrons [7]. However, previous reports indicated that middle gap materials such as NiSi also had the great possibility for applications to SB-MOSFETs by employing the Φ_b modulation techniques [5].

In this chaper, we applied the technique of the Φ_b modulation by Er interlayer to n-channel SB-MOSFETs fabrications.

5.2 Ni Silicide Schottky Barrier MOSFETs by With Er Interlayer

5.2.1 Fabrication Process and The Structure of SB-MOSFET

A fabrication process of n-channel SB-MOSFETs is shown in Fig. 5.1. The source/drain pre-formed p-Si(100) substrates covered with SiO_2 layer were used in this work. The gate stack of W/SiO_2 was formed by W deposition and etching of the W/SiO_2 layer. Then, 12nm-Ni/7.2nm-Er layers or 12nm-Ni layers as a reference were deposited and annealed at 600°C in the same manner as that employed in the Schottky diode fabrication process. After the un-reacted metals were etched, an Al back contact was formed. Finally, annealing in FG at 420°C for 30 minutes was carried out.

Schematic cross section of the fabricated SB-MOSFET is shown in Fig. 5.2. At the extensions regions of source and drain, the Schottky junction were placed so that the operation of SB-MOSFET is realized. The n^+ regions under the silicide source/drain are formed to reduce leakage current between source/drain and substrate due to the underlying pn junctions. The SEM image of SB-MOSFET is shown in Fig. 5.3. The SiO_2 layer was side etched a little by the etching process. But it was not strongly effected to characteristiecs of SB-MOSFETs. The thicknesses of W, SiO_2, and silicide were 60nm, 40nm and 20nm, respectively.

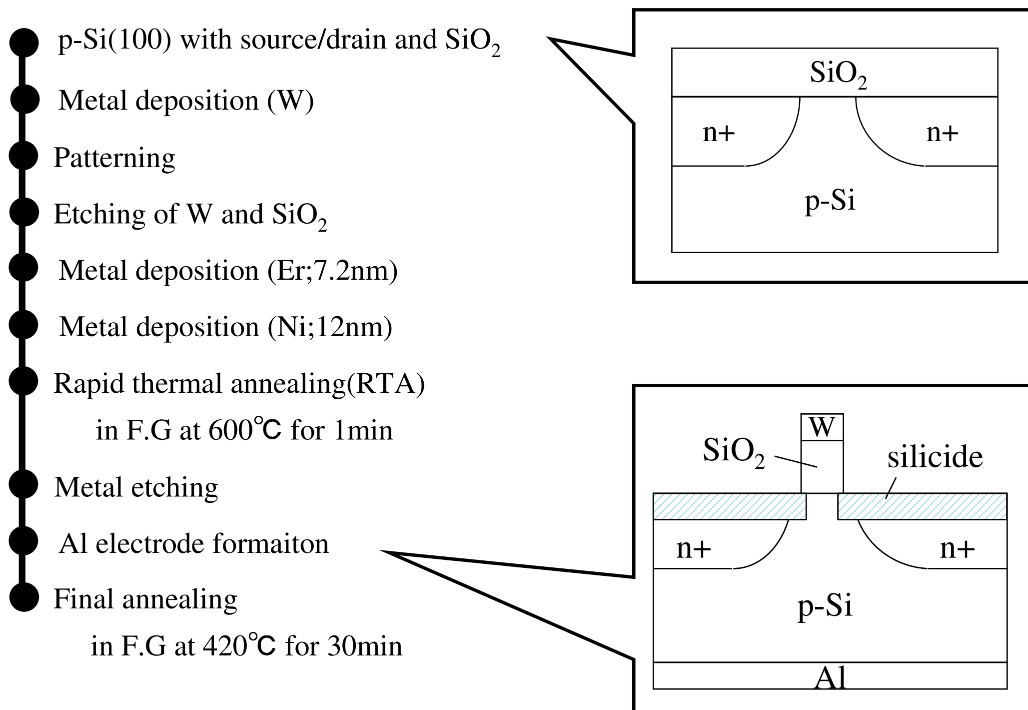


Fig. 5.1 Fabrication process of the n-channel SB-MOSFETs.

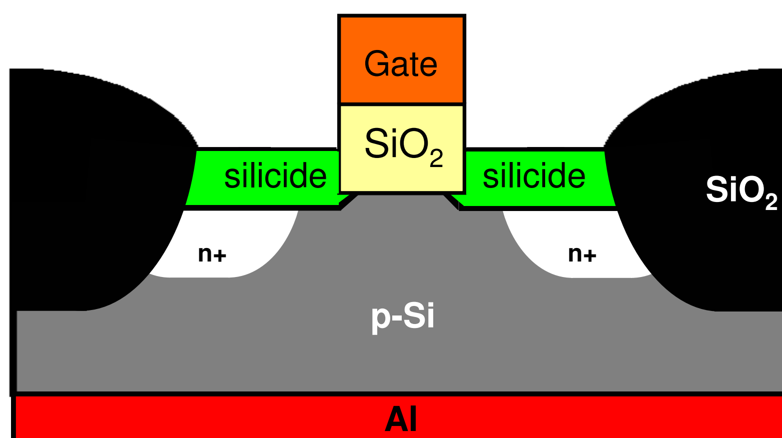


Fig. 5.2 Structure of n-channel SB-MOSFETs fabricated

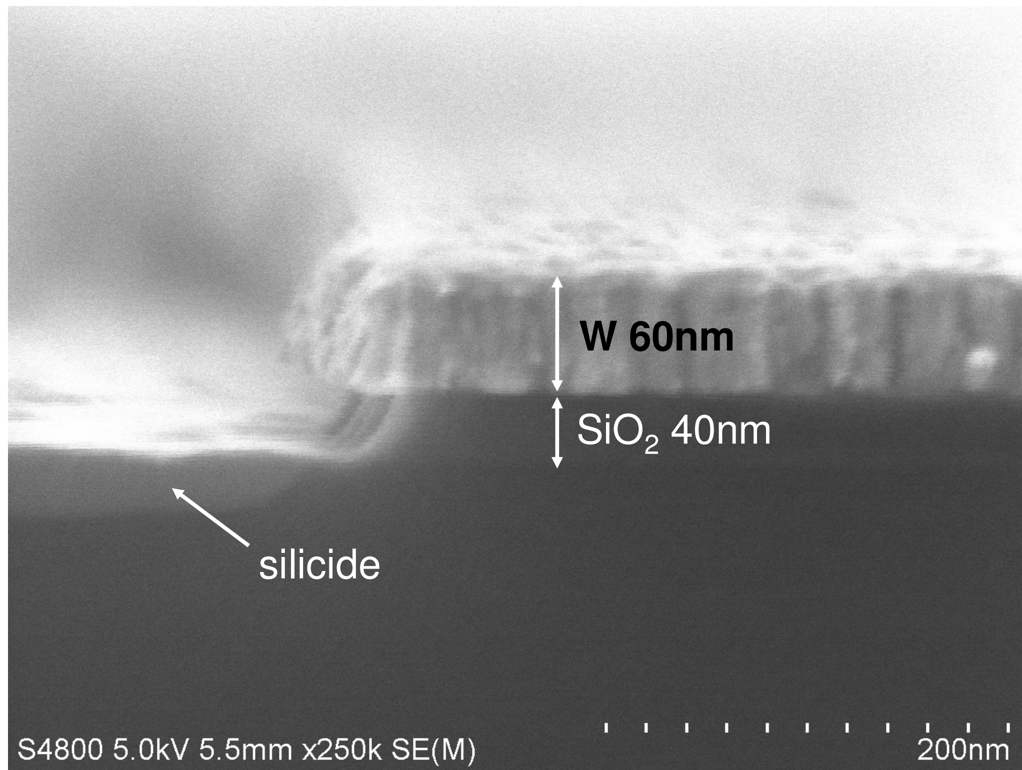


Fig. 5.3 SEM image of a part of n-channel SB-MOSFET fabricated

5.2.2 Characteristics of Ni Silicide Schottky Barrier MOSFETs with Er Interlayer

Fig. 5.4 shows I_d-V_g characteristics of the fabricated n-channel Ni silicide SB-MOSFETs. Threshold voltage (V_{th}) was shifted by 0.72V in the case of Er insertion. The schottky barrier height measured by schottky diode was lower by 0.04 eV with Er interlayer. Two reasons of V_{th} shift are considered. First, one is that the Er layer segregated to the surface reacted with SiO2 and Er oxide was formed. Second one is that Er reacted with W during the silicidation annealing process.

Fig. 5.5 shows I_d-V_d characteristics of the fabricated n-channel Ni silicide

SB-MOSFETs. I_d was increased by 20% in the case of Er insertion. As stated above, the Φ_b value was lower by 0.04eV, so it became easier for electrons to flow from the source.

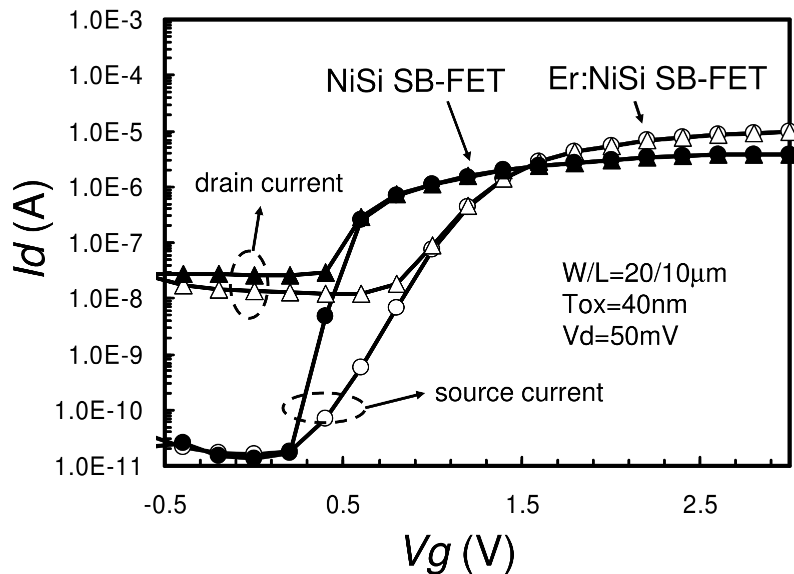


Fig. 5.4 I_d-V_g characteristics of the fabricated n-channel Ni silicide SB-MOSFETs.

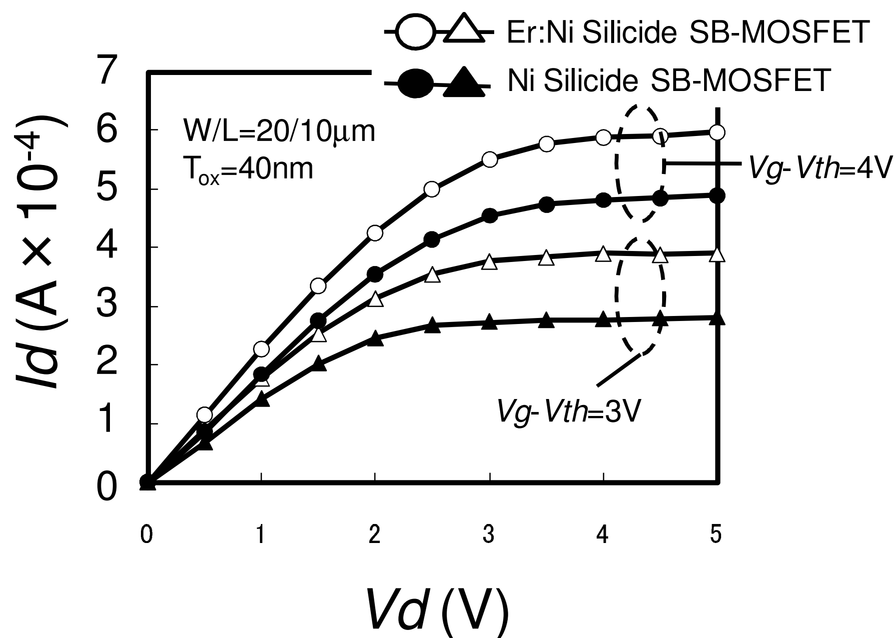


Fig. 5.5 I_d-V_d characteristics of the fabricated n-channel Ni silicide SB-MOSFETs

The contact resistance is determined by the schottky barrier height through

$$R_c = \frac{k}{qA^*T}\exp(\frac{q\phi_b}{kT}) \qquad (5.1)$$

where k is Boltzmann's constant, q is the electron charge, A* is the effective Richardson's constant, and T is temperature (Kelvin). A small reduction in the schottky barrier height has a large effect in reducing the contact resistance. So, the reduction by 0.04eV is so effective for the drain current. The resistance of NiSi SB-MOSFET and one with Er interlayer was compared in Fig. 5.6. A sum of the contact resistance and sheet resistance was reduced by 75.6% in the case of the Er inserted SB-MOSFET. This was so effective for increasing the drain current.

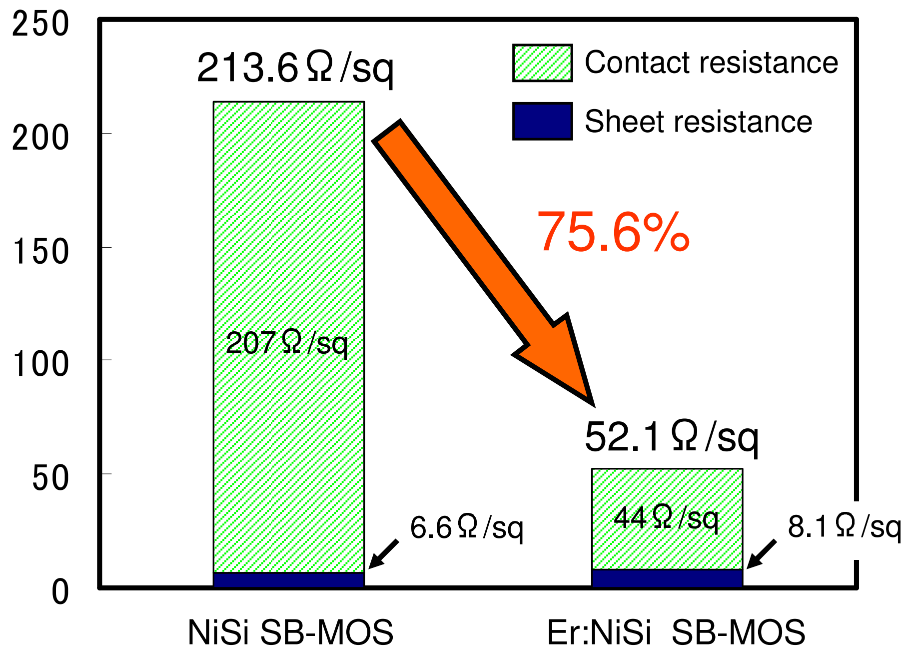


Fig. 5.6 the contact and sheet resistances of n-channel Ni silicide SB-MOSFETs

Chapter 6
CONCLUSION

6.1 Summary of This Study

A new technique of Φ_b modulation, in which an Er or Hf layer was inserted between Ni layer and Si substrate before silicidation process, was proposed. In the case of Er insertion, the value of Φ_b for electrons was lowered down to 0.22 eV and in the case of Hf insertion, the one of Φ_b for hole was increased by 0.21eV in this work. This technique was applied to the n-channel SB-MOSFETs fabrication. The SB-MOSFETs fabricated with the Er interlayer exhibited larger I_d than that observed for devices without the Er interlayer, due to the lowering of Φ_b for electrons.

6.2 Future Issues

In this work, we have proposed a new Φ_b modulation method for Ni silicide by inserting Er or Hf layer to Ni/Si interface and n-channel Ni Silicide Schottky barrier source/drain MOSFET was fabricated using Er insertion technique. I_d was increased by Er insertion, though, V_{th} was shifted. In the case of changing the silicide of source/drain, it's not possible for V_{th} to be shifted. So, tuning the process adopted for SB-MOSFET is needed.

In this work, we assumed that the value of Φ_b in the SB-MOSFET was the same as in the Schottky diode. In the SB-MOSFET, we need to consider the value of Φ_b of the SB-MOSFET in the horizontal direction. Because a silicide depth was very thin and the direction of the current was from silicide to channel.

The Φ_b value was decreased by 0.22eV with Er interlayer. We have a room for improvement. We need to search the other metals and the new process for silicide. And p channel SB-MOSFET are also considered.

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