

Master Thesis

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**Nickel silicide contact for**  
**Silicon Nanowire FET**

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# Chapter 1

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## *Introduction*

*1.1 Background of This Study*

*1.2 CMOS Downsizing limit and after that*

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## ***1.1 Background of This Study***

Nowadays, CMOS Large Scale Integrated circuits (LSIs), are really indispensable components for our human society. Needless to say, but almost all the human activities, living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc. cannot work without the help of the CMOS LSI operation. For example, all the bank activities immediately stop without CMOS computation. Cellular phones do not exist without CMOS technology. Also, it should not be forgotten that CMOS semiconductor industry is one of big driving force of world economy, which is not limited to semiconductor fields but also includes many different kinds industries of materials, equipments, and software's required for the integrated circuits. From now on, the continuous progress of CMOS technologies in terms of high-performance operation and low power consumption is still very important because of the following three reasons.

At first, under the rapid progress of aging population and falling birth rate, we need to accelerate the replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example. For the penetration of such intelligent robots to the daily family use, much higher intelligence and much lower power consumption than those of today are required, and the development of CMOS integrated circuits with much more high performance and low power consumption are indispensable.

Secondly, our society is now facing the global warming. The reduction of the CO<sub>2</sub> gas release is a critically urgent issue for the earth. Continuous progress of CMOS technologies contributes to the 'cooling of the earth' in two ways. One is direct

contribution to the power reduction for IT (Information Technology) devices. Explosive increase of energy consumption at office and home are demanded to be suppressed by so called 'Green IT' procedure. This can be done by the development of low power and high performance CMOS devices such used to data centers, routers and terminals, together with the high-efficient DC power feeding technology. Another contribution of the CMOS technology is to save the total power consumption of any kinds of systems – from those for entire city transportation traffic to those for individual car operation – by the optimum power saving control of the operation by intelligent CMOS processors.

Thirdly, continuous progress of CMOS technology is critically important from the semiconductor industry point, and thus, from the global economical point of view. Because of the merits in performance and power consumption from 65 to 45 nm node logic devices, and because of the high-density or cost merit from 8 to 16 Gbit flash memories, LSI products are sold well in the market every 2 or 3 years to replace the products of previous generations. In case if there is no more progress in the CMOS technologies, semiconductor industry will face a disaster, and hence, the world economy will be in a crisis.

It is well known that the progress of CMOS LSI has been accomplished by the downsizing of MOSFETs. In the past, there were many downsizing limits predicted already from the 0.8 micron-meter generation since 1970's. It was fortunate, however, that those limits were proven not to be true by the fabrication of smaller dimension MOSFETs and confirmation of their excellent electric characteristics. However, it has been predicted by most of the engineers now, that the downsizing would reach its limit probably about the gate length of 5 nm around the year of 2020. 2020 is not too far, but there is no sufficiently clear image for the world after CMOS reaches its scaling limit.

## ***1.2 CMOS downsizing limit and after that***

Why it is expected that about 5 nm is the limit of the downsizing? There are four main reasons; A) Difficulty on off-current suppression, B) Difficulty on increase in on-current, C) Difficulty on decrease in gate capacitance, D) Production and development cost increase.

### ***A. Difficulty on off-current suppression***

With decrease in gate length, off-current – the subthreshold and direct-tunneling leakage currents between source and drain – becomes significant at the gate length of 5~3 nm. From the consideration of the integration of huge number of MOSFETs in a chip, and resulted huge entire off-leakage current, probably, around 5 nm could be regarded as the limit of the gate length reduction. It might be even 10 nm or 3 nm, depending on the number of MOSFET integrations. Below 3 nm, the direct-tunneling leakage current increases very significantly and it is almost impossible to suppress the off-leakage current.

### ***B. Difficulty on increase of on-current***

Already the conduction of the drain current enters in the semi-ballistic region and thus, no significant increase of the drain saturated current or on-current is expected by reducing the gate length below 5 nm. Also, increase in source/drain resistance of small geometry MOSFETs tends to suppress the on-current.

### ***C. Difficulty on increase of on-current***

One of the scaling merits is to reduce the gate capacitance,  $C_g$ , because the switching time of MOSFETs is defined by  $C_g/I_d$ , where  $I_d$  is the drain on-current. However,  $C_g$  will

not decrease in proportion to the gate length because of gate electrode sidewall capacitance component and that of drain/ source-to-gate electrode overlap. These capacitance components are very difficult to be reduced because the gate electrode thickness and source/drain depth are very difficult to be further reduced.

#### ***D. Production and development cost increase***

It is expected that the structure and manufacturing process of such small dimension MOSFETs with huge number of integration on a chip becomes very complicated and the development and production cost of the CMOS LSI would become too expensive to retain the profit for the production.

#### ***E. Possible solution after that***

It is not sure exactly at what gate length and exactly at what year, the downsizing of MOSFETs reach its limit, but most of the engineers are expected that it would be happen around at the gate length of 5 nm and around in the year of 2020, although it could be 10 nm in 2015 or 3 nm in 2030.

Then, what will be the world after we reached the limitation. Unfortunately, at this moment, there are no candidates among the so-called 'beyond CMOS' or 'Post Si' new devices, which are believed to really replace CMOS transistors usable for the products of highly integrated circuits within 20 years. Our opinion is that we need to still continue CMOS based transistors with 'More Moore' approach with combining that of 'More than Moore.' Then, what is 'More Moore' approach after we reached the downsizing limit or with no more decrease in gate length? Because the number of the transistors in a chip is limited by the power consumption, we could continue the 'More



Moore's law for certain period by replacing current CMOS transistors by nanowire or nanotube MOSFETs with which the suppression of off-leakage current and increase of on-current under low voltage could be realized because of its nature such as quasi-one-dimensional conduction, multi-quantum channel per wire/tube and high-density integration of wire/tube in multi-layers. Figure 1 shows our roadmap for wire and tube MOSFETs after 2020.

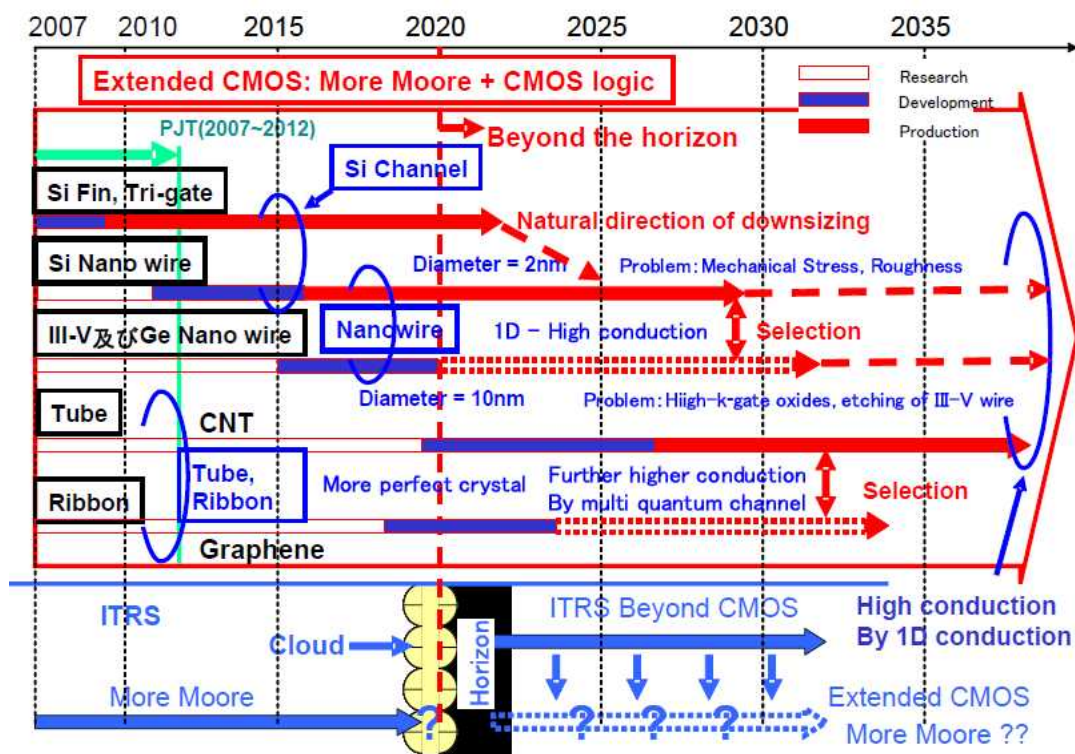


Fig.1.1 Roadmap for wire and tube

### 1.3 Silicon Nanowire Field Effect Transistors

Si nanowire FET is considered as one of the promising candidates for further extending the device downsizing, owing to its gate-all-around(GAA) structure which enables better gate control capability than planar transistors [1,2]. Figure.1.2 shows schematic and SEM image of GAA structure. Therefore, high  $I_{on}/I_{off}$  ratio can be achieved . Figure.1.3 shows comparison of the requirement to the bulk Si ,the ultra-thin body fully depleted(UTB FD) SOI and the double-gate(DG) MOSFET in 2008 in ITRS2008 with previously reported data on SiNW FET fabricated using CMOS compatible processes.[3-9] Si naowire FETs have already been obtained higher  $I_{ON}/I_{OFF}$  ratio than any planer transistors.

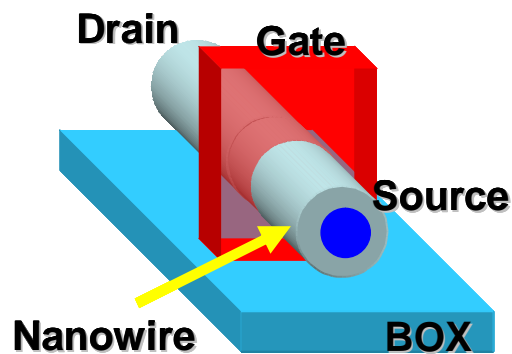
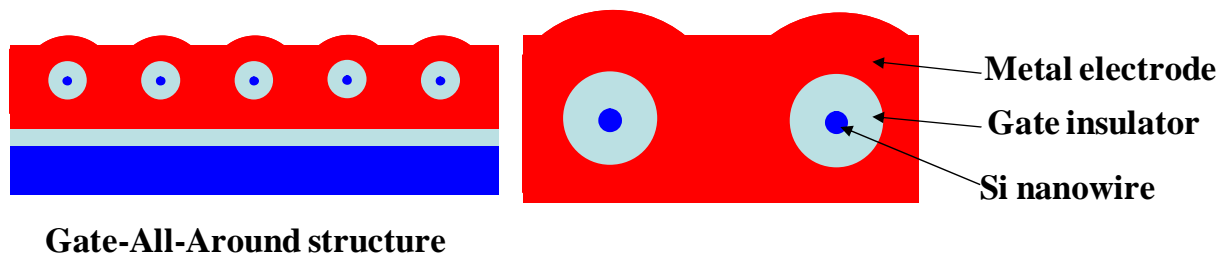


Figure.1.2 Schematic of GAA structure

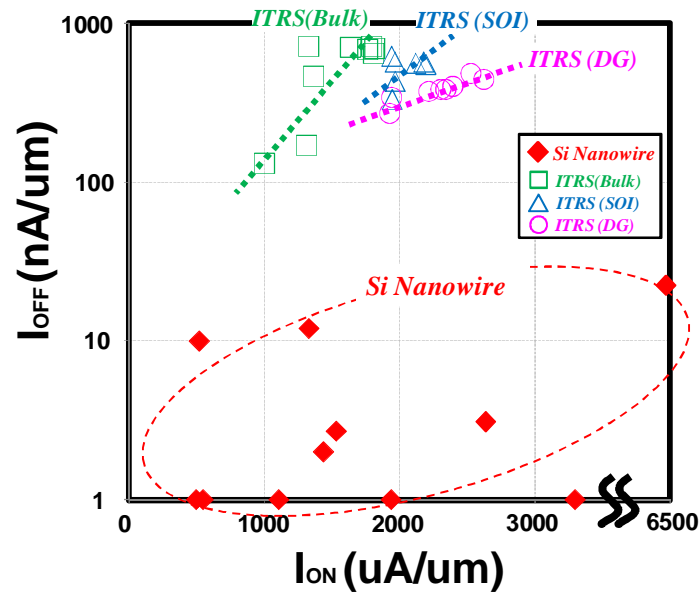


Figure 1.3 Comparison of the requirement to the bulk Si, UTB FD SOI and DG MOSFET in 2008 in ITRS2008 with previously reported data on Si nanowire FET fabricated using CMOS compatible processes.

Si nanowire FET has been fabricated by several techniques including, Si Fins are patterned by lithography and etching followed by the oxidation (Figure 1.4(a) shows Top-down method) or Methods using CVD, MBE and other processes to grow Si nanowire with better controllability of the size of the wire (Figure 1.4(b) shows Bottom-up method) [10,11].

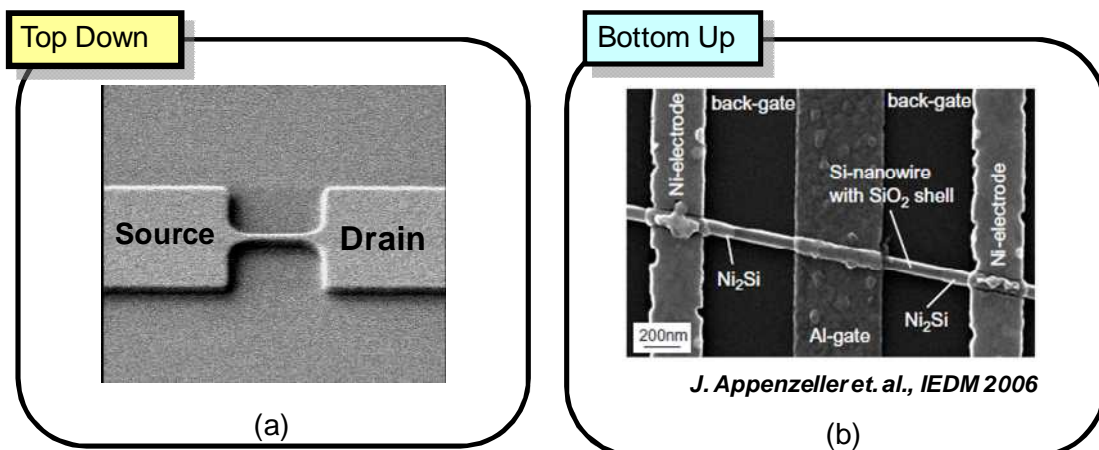


Figure 1.4 Fabrication methods of Si nanowire FET, (a) Top-down, (b) Bottom-up.

Si nanowire FET is not yet completely understood. There is a problem that the shape control of Si nanowire, the interface characteristic of the insulator, the geometry intolerances and surface roughness created by the Top-down processing, the strain etc. influence the transistor characteristic (mobility and threshold). In addition, One of the concerns in Si nanowire FET is the increase in access resistance at source/drain region, which eventually reduces the on-state current. And Si nanowire FET has some problems anything other than the above issue yet.

#### ***1.4 Advantage of Nickel silicide used as self-aligned silicide***

In the previous section 1.3, we showed that one of the concerns in SiNW-FET is the increase in access resistance at source/drain region. Commonly, metal silicides have been widely used as self-aligned silicide (salicide) contacts on source, drain and polycrystalline silicon gate regions of CMOS devices to reduce contact and series resistances.[12] And metal silicide contacts will be used in Si nanowire FETs as well as planar CMOS FETs. Currently, the most commonly used silicides (salicides) are  $\text{TiSi}_2$ ,  $\text{CoSi}_2$ , and  $\text{NiSi}$ . For  $\text{TiSi}_2$ , the transformation from the metastable high resistivity C49 phase to the thermodynamically stable low resistivity C54 phase is nucleation limited, causing linewidth dependence of sheet resistance for linewidths narrower than  $0.35\mu\text{m}$ .[13] Although  $\text{CoSi}_2$  has very good electrical properties, its high Si consumption and junction spiking problems limit its application to deep sub-micrometer devices.[14] Nickel mono-silicide( $\text{NiSi}$ ), without these drawbacks, has been shown to be a suitable silicide material for future nano-scale devices because of its advantages of lowest resistivity, absence of line-width effect, low Si consumption rate( $\sim 1\text{nm}$  of Ni

reacts with 1.84nm of Si to form 2.22nm of NiSi), low film stress, and it needs only low temperature, one-step annealing.[15,16]

### ***1.5 Purpose of this study***

Si Nanowire field effect transistors (SiNW-FET) have attracted much attention for future device, owing to its ability to suppress the off-state leakage current. One of the concerns in SiNW-FET is the increase in access resistance at source/drain region, which eventually reduces the on-state current. Commonly, metal silicide contacts, especially NiSi, have been used to reduce the resistance for bulk and SOI FET. However, the lateral diffusion of Ni to form NiSi in SiNW is still unknown. In this study, evaluation of lateral Ni diffusion into SiNW has been conducted.

In addition, one of the important problems in the nanowire process is the difficulty in controlling the cross-section shape of the nanowire fabricated by thermal oxidation, as the shape strongly affects the electrical property. In order to calibrate the oxidation rate to control Si nanowire for Sub-10nm cross-sectional shape optimization, different process temperatures and different oxidation times were therefore tested on Si nanowires.

This thesis reports the solutions for the above issues with experimental results.

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# Chapter 2

## *Fabrication and Characterization Methods*

### **2.1 *Experimental Procedure***

- 2.1.1 *Si Substrate Cleaning Process*
- 2.1.2 *Oxidation Furnace*
- 2.1.3 *Photolithography*
- 2.1.3 *UHV-Sputtering System*
- 2.1.4 *Infrared Annealing Furnace*

### **2.2 *Measurement Methods***

- 2.2.1 *Scanning Electron Microscope (SEM)*
- 2.2.2 *Transmission Electron Microscope (TEM)*

## ***2.1 Experimental Procedure***

### ***2.1.1 Si Substrate Cleaning Process***

At first, high quality thin films require ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩcm at 25°C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩcm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the Si substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The first step, which use a solution of sulfuric acid (H<sub>2</sub>SO<sub>4</sub>) / hydrogen peroxide (H<sub>2</sub>O<sub>2</sub>) (H<sub>2</sub>SO<sub>4</sub>: H<sub>2</sub>O<sub>2</sub>=4:1), was performed to remove any organic material and metallic impurities. After that, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H<sub>2</sub>O=1:99). Then the cleaned wafer was dipped in DI water. Finally, the cleaned Si substrate was loaded to chamber to deposit as soon as it was dried by air gun.



### ***2.1.2 Oxidation Furnace***

Thermal oxidation is accomplished using an oxidation furnace (or diffusion furnace, since oxidation is basically a diffusion process involving oxidant species), which provides the heat needed to elevate the oxidizing ambient temperature. A furnace typically consists of: 1) a cabinet; 2) a heating system; 3) a temperature measurement and control system; 4) fused quartz process tubes where the wafers undergo oxidation; 5) a system for moving process gases into and out of the process tubes; and 6) a loading station used for loading (or unloading) wafers into (or from) the process tubes.

The heating system usually consists of several heating coils that control the temperature around the furnace tubes. The wafers are placed in quartz glassware known as boats, which are supported by fused silica paddles inside the process tube. A boat can contain many wafers. The oxidizing agent (oxygen or steam) then enters the process tube through its source end, subsequently diffusing to the wafers where the oxidation occurs. In this study, Figure.2.1 shows a photo of Oxidation Furnace.

Depending on which oxidant species is used ( $O_2$  or  $H_2O$ ), the thermal oxidation of  $SiO_2$  may either be in the form of dry oxidation (wherein the oxidant is  $O_2$ ) or wet oxidation (wherein the oxidant is  $H_2O$ ). The reactions for dry and wet oxidation are governed by the following equations:

1) for dry oxidation:  $Si$  (solid) +  $O_2$  (vapor)  $\rightarrow$   $SiO_2$  (solid); and

2) for wet oxidation:  $Si$  (solid) +  $2H_2O$  (vapor)  $\rightarrow$   $SiO_2$  (solid) +  $2H_2$  (vapor).

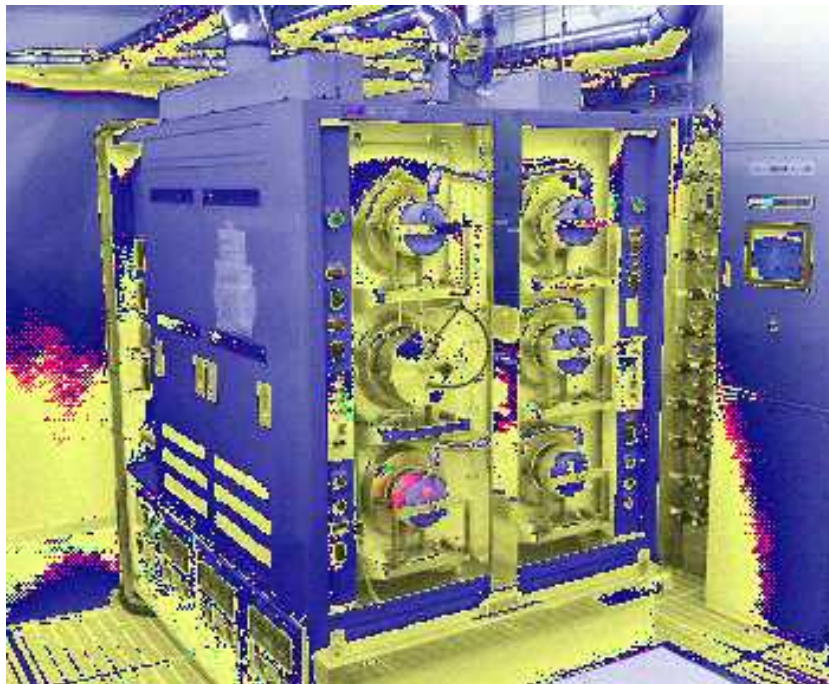


Figure.2.1 Photo of Oxidation Furnace

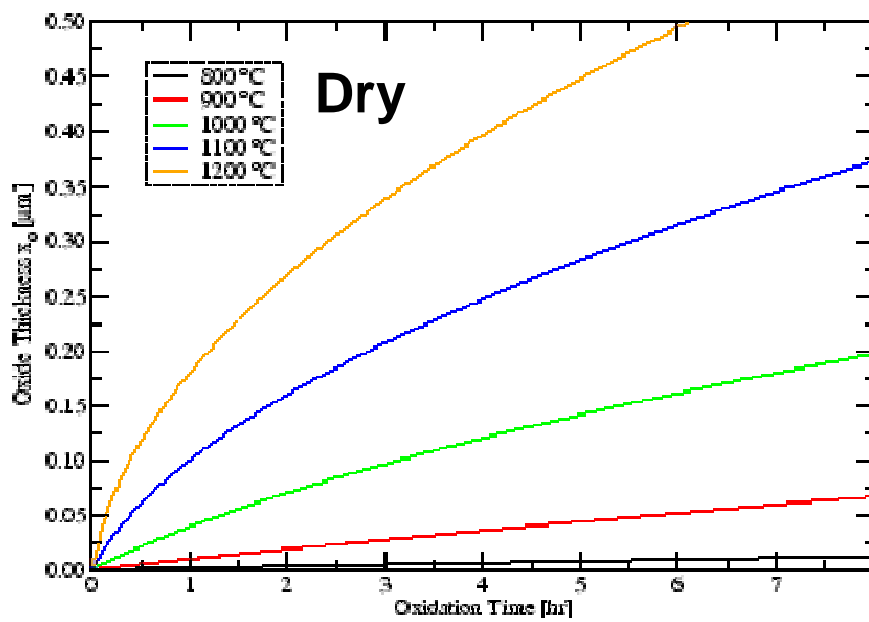


Figure.2.2 Oxide rate of dry oxidation

### ***2.1.3 Photolithography***

The process flow and the photo of photolithography used throughout this study is shown in Figure.2.3. Electrical hotplate is used for baking purposes. The spin-coated layer photoresist was aligned and exposed through tungsten coated e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. MJB4 of Karl Suss contact-type mask aligner as shown Figure.2.3 was used for aligning and exposition purposes. The exposure duration was set to 2.8 sec. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.) after dipped into the solvent for 2 minute and baked at 130 °C for 5 minutes.

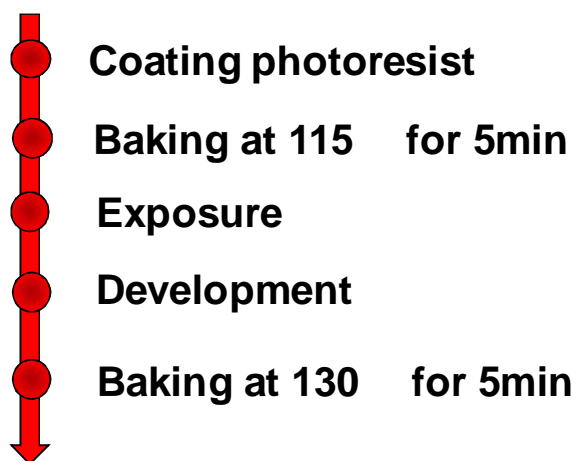


Figure2.3 The process flow and the photo of photolithography

### ***2.1.3 UHV-Sputtering System***

After cleaned by chemicals, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive except Ni.) and Ni/Si were formed by an UHV-sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. It is performed by applying a high voltage across a low-pressure gas (usually argon at about 5 millitorr) to create a “plasma,” which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike a “target,” composed of the desired coating material, and cause atoms from that target to be ejected with enough energy to travel to, and bond with the substrate.

An UHV-sputtering system is used for thin film formations of electronic devices, for experiments of GMR, and for creating new materials of high temperature superconductors. In this study, UHV Multi Target Sputtering System ES-350SU shown as Figure.2.5 was conducted. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. As for other details, Table 2.1 is attached for reference.

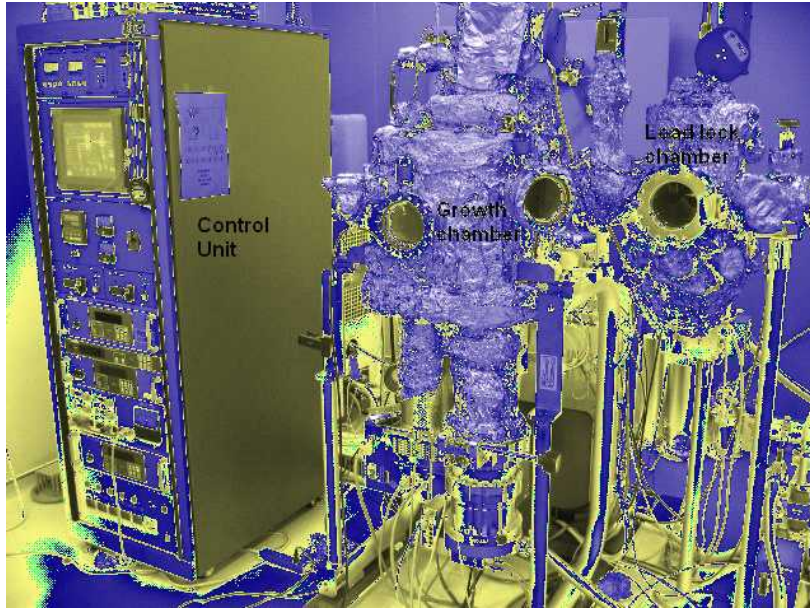


Figure.2.4 Photo of UHV Multi Target Sputtering System ES-350SU

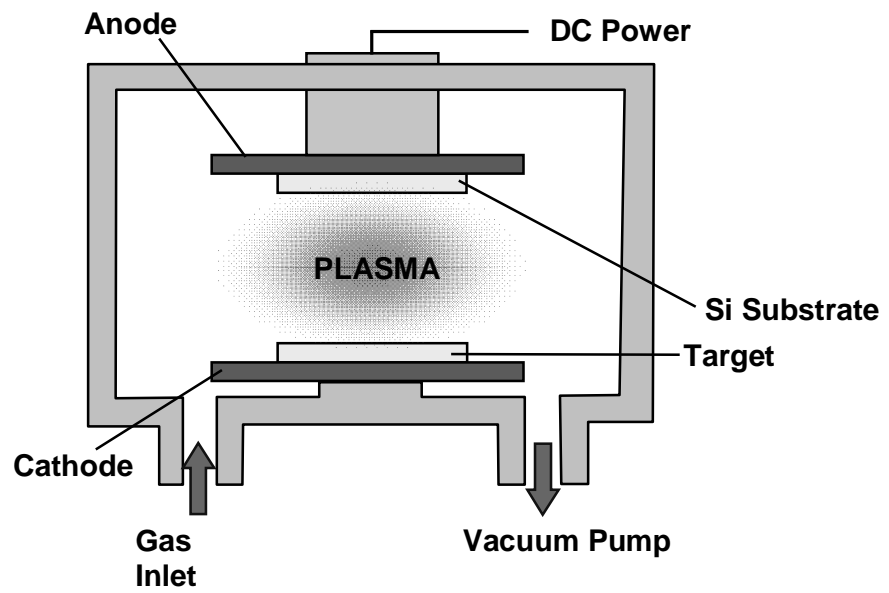


Figure.2.5 Structure of UHV sputtering system

<b>Growth chamber</b>	<b>1. Ultimate pressure</b>	<b>1.5 x 10<sup>-6</sup>Pa</b>
	<b>2. Substrate size</b>	<b>2 inch in diameter</b>
	<b>3. Heating temperature</b>	<b>600°C</b>
	<b>4. Heater type</b>	<b>Lamp type heater</b>
	<b>5. Target</b>	<b>3 inch x 5 pieces (motor-driven)</b>
<b>Load lock chamber</b>	<b>6. Vacuum pumps</b>	<b>TMP 500L/sec and RP 250L/min</b>
	<b>7. Ultimate pressure</b>	<b>6.6 x 10<sup>-5</sup>Pa</b>
	<b>8. Vacuum pumps</b>	<b>TMP60L/sec and RP90L/min</b>
	<b>9. Substrate holder with cooling function / Substrate holder with heating function /Cleaning function / Radical beam source</b>	

Table 2.1 Specifications for UHV Multi Target Sputtering System ES-350S

### ***2.1.4 Infrared Annealing Furnace***

After formation from UHV sputtering system, thin films of Ni/Si, Ni/M/Si, M/Ni/Si were moved to annealing furnace to hold thermal process.

In order to obtain high quality films, annealing process after deposition is required. The annealing after deposition is considered to bring the suppression of leakage current because of the defects in the films and surface roughness. In this study, thermal process leads to the reaction of Ni with Si.

The equipment for annealing used in this investigation was QHC-P610CP (ULVAC RIKO Co. Ltd). Figure.2.6 is the photo of the infrared annealing furnace, whose schematic illustration was shown as Figure.2.7. The annealing was performed by six infrared lamps surrounding the sample stage which were made of carbon and coated by SiC. The heating temperature was controlled by thermocouple feedback.

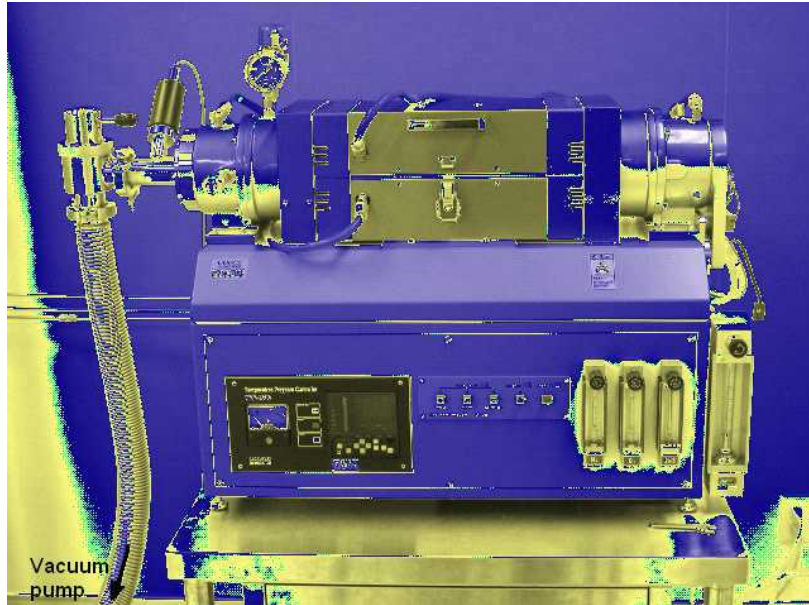


Figure.2.6 Photo of infrared annealing furnace

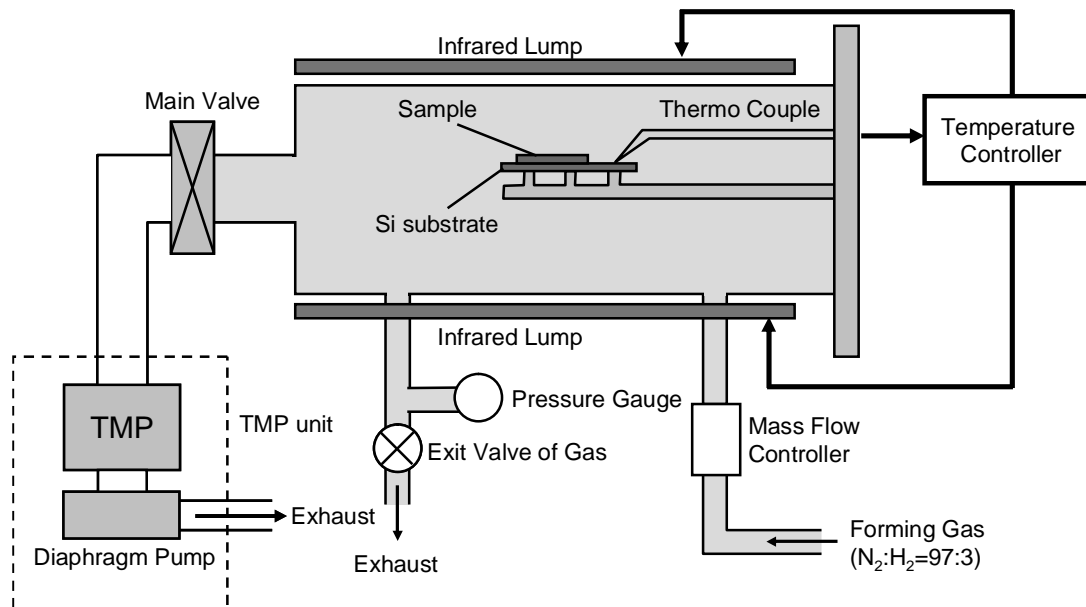


Figure.2.7 Schematic image of infrared annealing furnace



## ***2.2 Measurement Methods***

### ***2.2.1 Scanning Electron Microscope (SEM)***

Figure.2.9 shows Scanning Electron Microscope (SEM) system. The Virtual Source at the top represents the electron gun , producing a stream of monochromatic electrons. The stream is condensed by the first condenser lens. This lens is used to both form the beam and limit the amount of current in the beam. It works in conjunction with the condenser aperture to eliminate the high-angle electrons into a thin , tight , coherent beam. A user selectable objective aperture further eliminates high-angle electrons from the beam. A set of coils then scan or sweep the beam in a grid fashion , dwelling on points for a period of time determined by the scan speed. The final lens, the Objective , focuses the scanning beam onto the part of the specimen desired. When the beam strikes the sample , interactions occur inside the sample and are detected with various instruments interactions. Before the beam moves to its next dwell point these instruments count the number of interactions and display a pixel on a CRT whose intensity is determined by this number. This process is repeated until the grid scan is finished and then repeated , the entire pattern can be scanned 30 times per second.

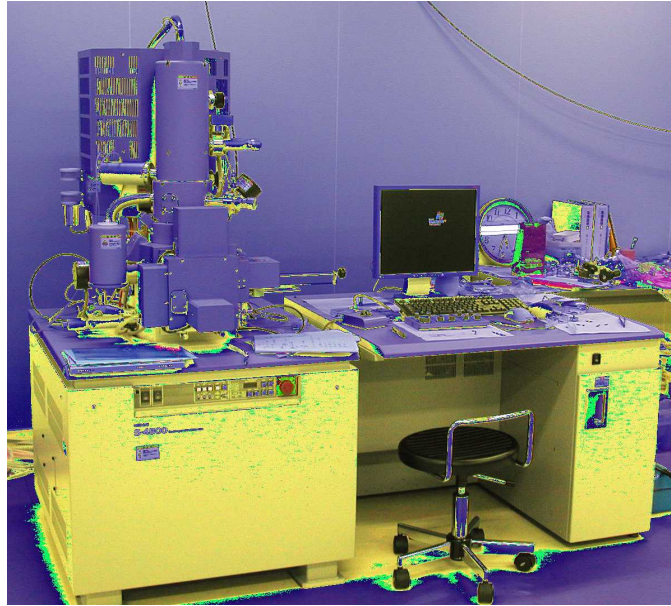


Figure.2.8 Photo of SEM equipment

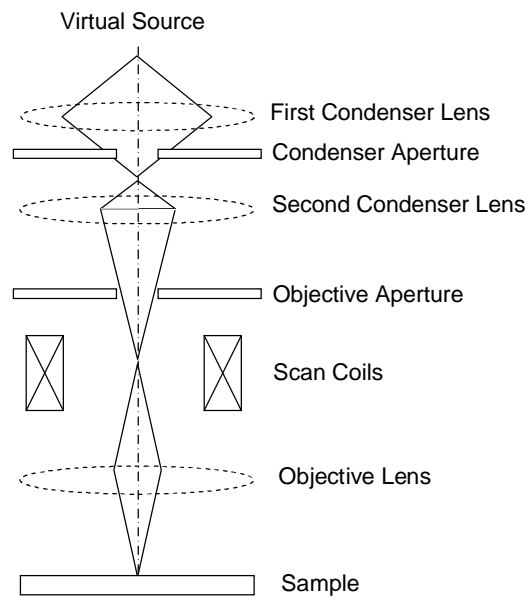


Figure.2.9 Schematic drawings of SEM equipment

### 2.2.2 Transmission Electron Microscope (TEM)

Cross-section TEM image is the most important analysis method to characterize physical thickness, film quality and interface condition.

Figure.2.10 Shows TEM system. First, focus lenses change convergent angle and beam size. The electron beam transmitted through the thin fragment sample passes objective lens and projective lens, and finally projected on fluorescent screen. Recording on the image is performed by direct exposure on exclusive film for electron microscope set lower part of the fluorescent screen.

Electron interacts strongly with lattice by scattering. Thus, sample has to be very thin fragment. Required thickness of the sample is 5 to 500 nm at 100 kV. TEM images are obtained in very high resolution such as 0.2 to 0.3 nm at 200 kV.

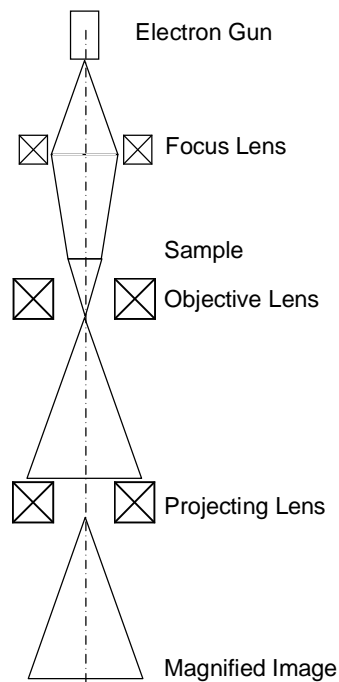


Figure.2.10 Schematic drawings of TEM equipment

# Chapter 3

## *Oxidation of Si Nanowire for Sub-10nm cross-section shape optimization*

*3.1 Introduction*

*3.2 Experimental*

*3.3 Observation of shapes of Si Nanowire with Si Fin Aspect Ratio*

*3.4 Fabrication process of SiNanowire for Sub-10nm diameter*

*3.5 Summary*

*3.6 References*

### ***3.1 Introduction***

In this chapter, we report fabrication of planar Si nanowires on silicon-on-insulator using thermal oxidation[1-6]. The important problems in the nanowire process are the difficulty in controlling the nanowire shape and diameter. The shape strongly affects the electrical property. The diameter must obtain well-controlled diameters down to 10nm, opening sub-5nm gate length opportunities for MOSFETs downscaling. Therefore, it is essential to find a process which enables us to round the nanowires for the optimal  $I_{OFF}$  value and to reduce the Si nanowires dimensions to the values below 10nm. However the oxidation of the structure having a large curvature such as Si nanowires is not yet completely understood. In order to calibrate the oxidation rate to round the corners of Si nanowire and to reduce the size of Si nanowire to values below 10nm, different methods of thermal oxidation, different process temperatures and different oxidation times were therefore tested on Si nanowires.

### 3.2 Experimental

Fabrication process flow of Si nanowire is shown Figure.3.1. Si Fins with different width ranging from 60 to 100nm were formed on a SOI substrate(SOI and BOX thickness of 61 and 145nm,respectively) by dry etching. Figure.3.2 shows a cross sectional SEM image of Si Fins. Wafer was then subjected to thermal Oxidation in dry O<sub>2</sub>. We focused on high temperatures for the oxidations in order to let the oxide flow around the nanowire and thus round the nanowire section. A cross sectional SEM image of Si nanowires fabricated by thermal oxidation is shown Figure.3.3.

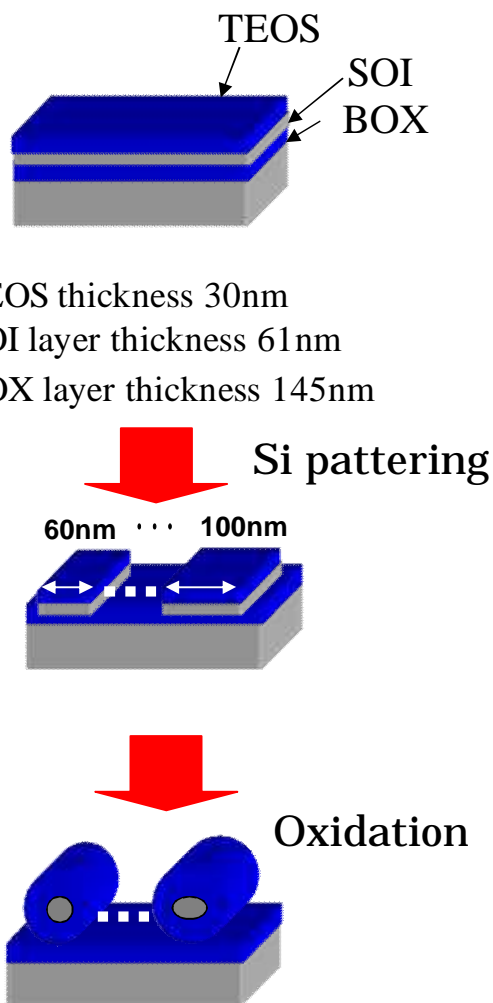


Figure.3.1 Process flow of Si nanowire

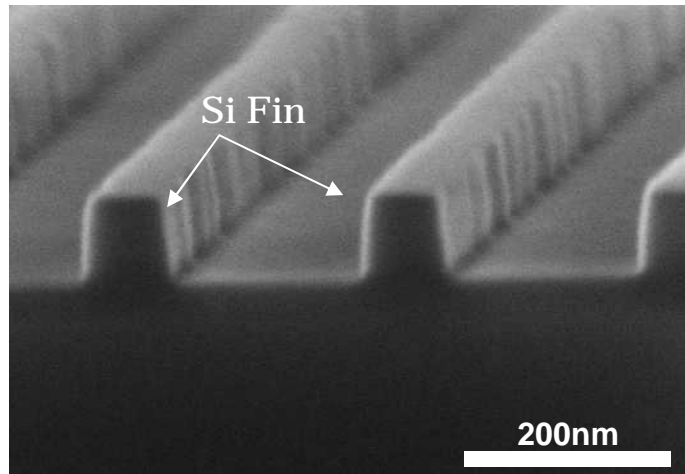


Figure.3.2 A cross sectional SEM image of Si Fins

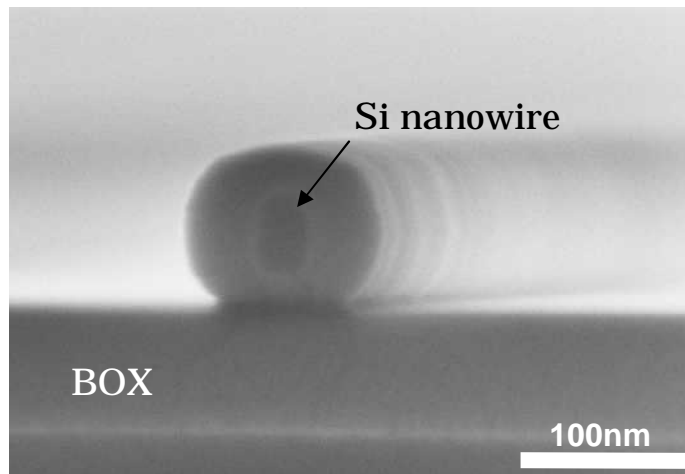


Figure.3.3 A cross sectional SEM image of Si nanowire

### 3.3 Observation of shapes of Si Nanowire with Si Fin Aspect Ratio

After 60min and 90min of 1000 °C oxidation , the shapes of Si nanowires on Si fin aspect ratio are measured. Figure.3.4 shows the results .In the case of Si fin aspect ratio between 0.95 and 1.05, the shape of the nanowire become round or square. In other cases, the shapes of the nanowires are oval with some convex corner. These corners are considered that turn off characteristics will be deteriorated as the electric field is increased at the corner. At this point, The effect of the shape on the electrical characterization on the shapes have not been investigated yet. However I anticipate the optimal shape to be circle.

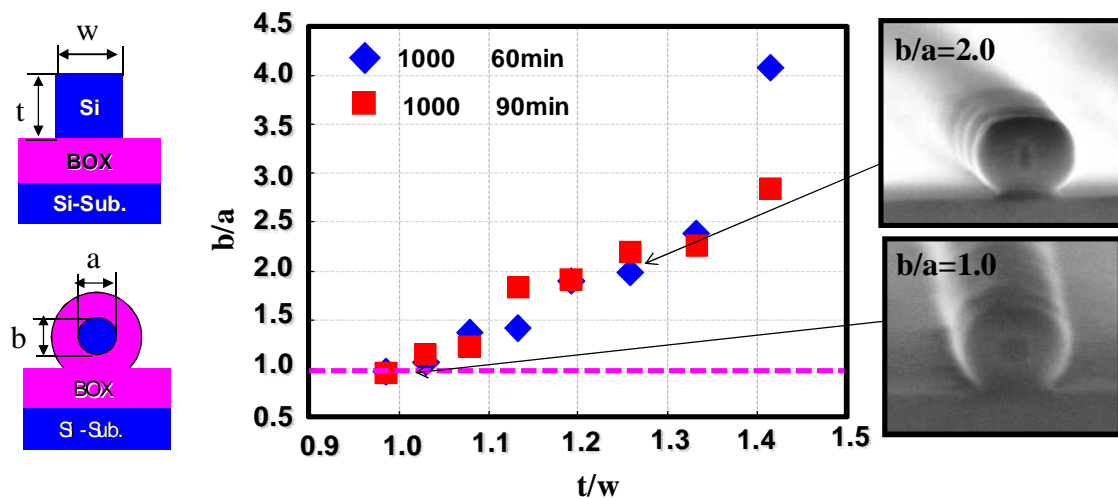


Figure.3.4 Shapes of Si Nnanowire with Si Fin Aspect Ratio



### ***3.4 Oxidation of Si Nanowire for Sub-10nm diameter***

Dry oxidation( at 1000°C and at 1100°C , respectively) has been investigated. Cross sectional transmission electron microscopy (TEM) images of Si nanowires after 1000 °C dry oxidation for 60min and 1100 °C dry oxidation for 30min are shown Figure.3.6. In the case of Si fin aspect ratio about one, oxidation at 1000 °C did not round the nanowire enough and could not reduce the size of Si nanowire to values below 10nm even after the long time oxidation. By contrast, Si nanowire oxidized at 1100 °C is very circular and can be fabricated Si nanowire of 9nm in diameter. Indeed, for temperature above the viscous flow point ( 950 °C) , the oxide can be considered as viscous fluid and will flow to relax the stress. The higher the oxidation temperature is, the easier the oxide will flow.

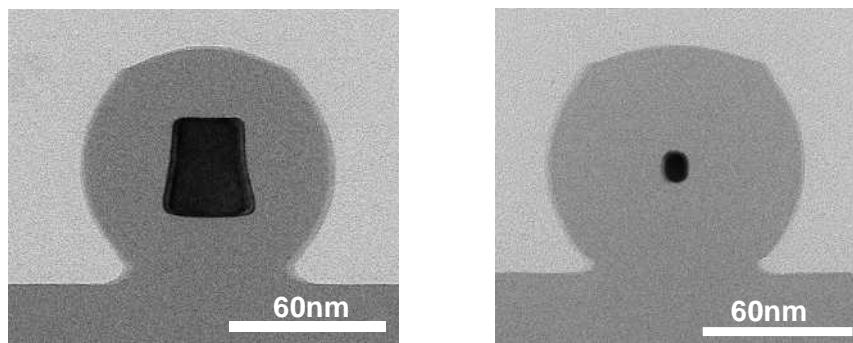


Figure.3.5 Cross sectional TEM image of Si nanowires (a) after 1000 °C for 60min, (b) after 1100 °C for 30min. Si nanowire oxidized at 1100 °C is very circular and can be fabricated Si nanowire of 9nm in diameter.

The dependence of a diameter on Si nanowire after 1000 °C dry oxidation for different durations is shown Figure.3.6. After 60 min, the nanowire oxidation rate a little reduced. For this temperature and oxidation durations, the oxide can be considered as an incompressible viscous fluid. To better understanding of the oxidation mechanisms occurring on our nanowires, the extension of the Deal and Grove model [7] to 2D cylindrical geometry developed by Kao et al [8]. can be used. The model takes into account the viscous nature of the oxide at this temperature with the definition of a normal stress at the interface. This stress greatly impacts the surface reaction rate at the Si/SiO<sub>2</sub> interface. Which controls the oxidation rate. The higher the stress at the interface is, the more the surface reaction drops. As the oxide grows around the nanowire, the stress in the oxide near the Si/SiO<sub>2</sub> interface considerably increases because of the volume expansion required by the formation of the new oxide layer, thus slowing the oxidation of the structure. A consequence of this oxidation rate reduction on convex structures such as nanowires is that, the oxidation will stop by itself when a high enough oxide layer thickness is reached.

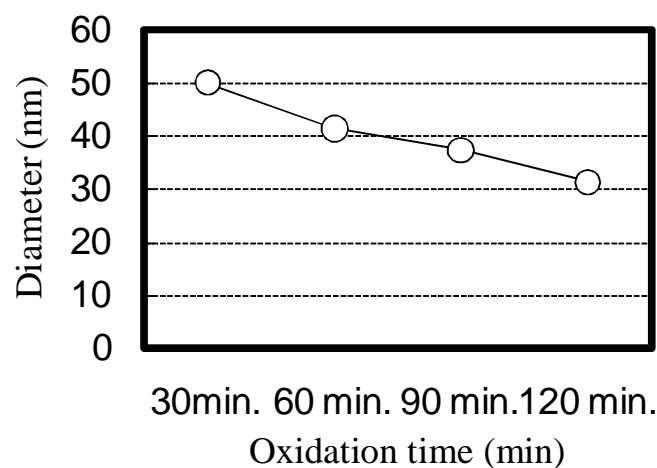


Figure.3.6 The dependence of a diameter on Si nanowire after 1000 °C dry oxidation for different durations. After 60 min, the oxidation tends to saturate.

In order to reach the Si nanowire diameter of under 10nm, we conducted reoxidation after removing the oxide layer formed by dry oxidation at 1000 °C for 60min. Figure.3.7 shows the process flow of reoxidation. This method means to break down the stress of the Si/SiO<sub>2</sub> interface. As a result, Si core of the nanowire could be fabricated by reoxidation at 1000 °C for 90min formed 10nm tall and 7nm wide.

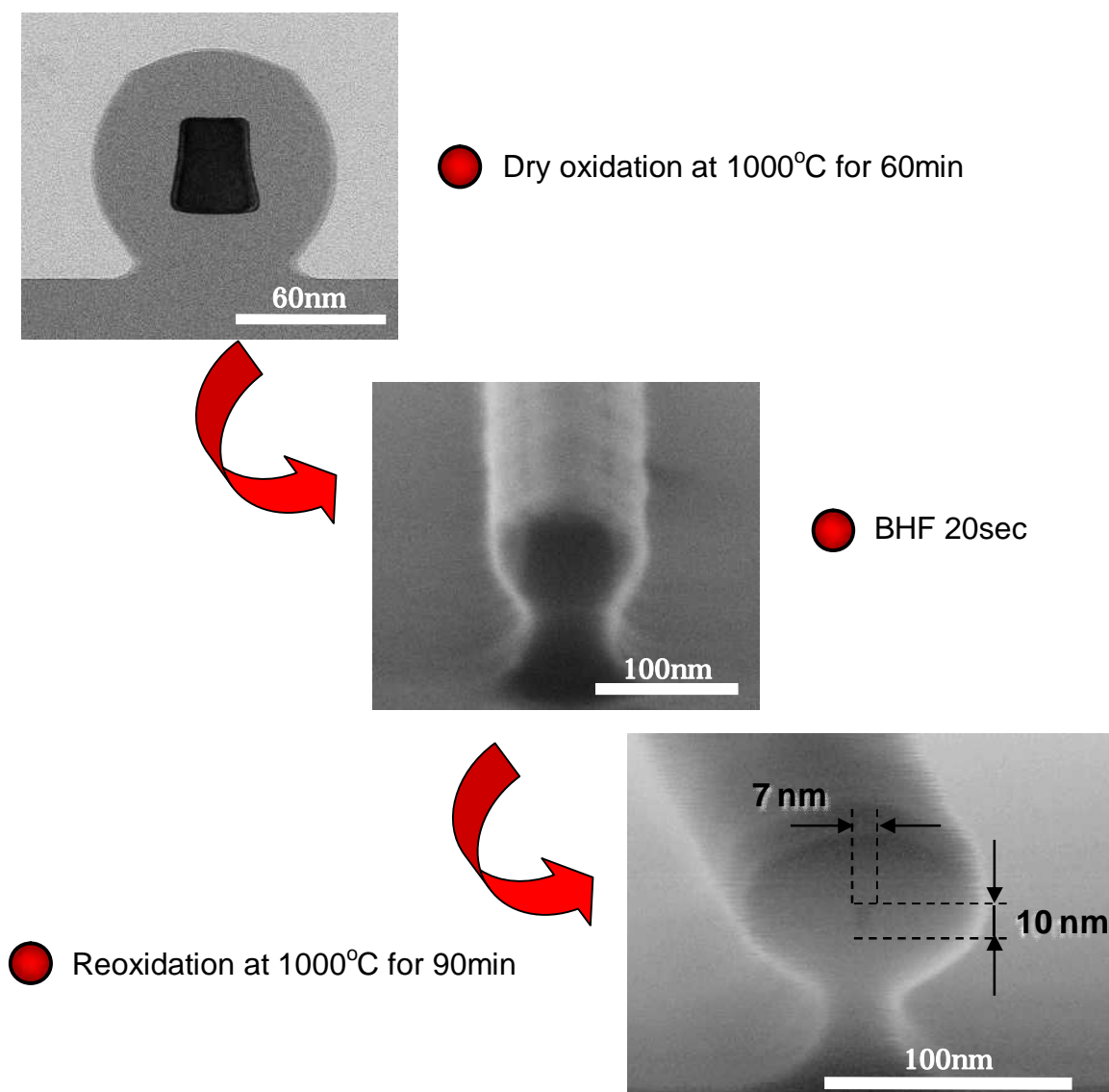


Figure.3.7 Process flow of reoxidation after removing the oxide layer formed by dry oxidation at 1000 °C for 60min.

### ***3.5 Summary***

In this chapter, Si nanowire has been fabricated by top-down method. In order to calibrate the oxidation to round and to reduce the size of Si nanowire to values below 10nm, different methods of thermal oxidation, different process temperatures and different oxidation times were tested on Si nanowires.

In the case of Si fin aspect ratio about one, Si nanowire oxidized at 1100 °C is very circular and can be fabricated Si nanowire of 9nm in diameter. After 1000 °C dry oxidation for 60 min, the nanowire oxidation is strongly reduced. A consequence of this oxidation rate reduction on convex structures such as nanowires is that, the oxidation will stop by itself when a high enough oxide layer thickness is reached. To reach the Si nanowire of under 10nm, we conducted reoxidation after removing the oxide layer formed by dry oxidation at 1000 °C for 60min. This method means to relax the stress of the Si/SiO<sub>2</sub> interface. As a result, Si core of the nanowire fabricated by reoxidation at 1000 °C for 90min is Si nanowire of under 10nm in diameter.

### 3.6 References

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# Chapter 4

## *Evaluation of Lateral Nickel Diffusion in Si Nanowire Schottky Contact*

*4.1 Introduction*

*4.2 Experimental*

*4.3 Results and Discussion*

*4.4 Summary*

*4.5 References*

## ***4.1 Introduction***

Si Nanowire field effect transistors (SiNW-FET) have attracted much attention for future device, owing to its ability to suppress the off-state leakage current. One of the concerns in SiNW-FET is the increase in access resistance at source/drain region, which eventually reduces the on-state current. Commonly, metal silicide contacts, especially NiSi, have been used to reduce the resistance for bulk and SOI FET. However, the lateral diffusion of Ni to form NiSi in Si nanowire is still unknown [1-4]. In this study, evaluation of lateral Ni diffusion into Si nanowire has been conducted.

## 4.2 Experimental

Figure.4.1 shows the process flow. Si lines with different widths ranging from 60 to 100 nm along <100> were formed on a SOI substrate (SOI and BOX thickness of 61 and 145 nm, respectively) by dry etching. Wafer was then subjected to thermal oxidation in dry O<sub>2</sub> at 1100 °C for 30min, resulting in formation of Si nanowires surrounded by SiO<sub>2</sub>. After striping a part of the formed SiO<sub>2</sub> with buffered HF to expose Si nanowires, 10-nm-thick Ni film was deposited by magnetron sputtering in Ar gas at a pressure of 5.5×10<sup>-1</sup> Pa. Silicidation annealing was performed by rapid thermal annealing (RTA) apparatus in a forming gas (N<sub>2</sub>/H<sub>2</sub>=97%/3%) ambient at annealing temperatures range from 400 to 700 °C . The unreacted Ni was removed by H<sub>2</sub>SO<sub>4</sub>/H<sub>2</sub>O<sub>2</sub> mixture. The formed NiSi was observed and measured by field-emission scanning electron microscope (SEM) at a high acceleration voltage (10 keV) so that the secondary electrons from NiSi can be collected through 50-nm-thick SiO<sub>2</sub> shell.

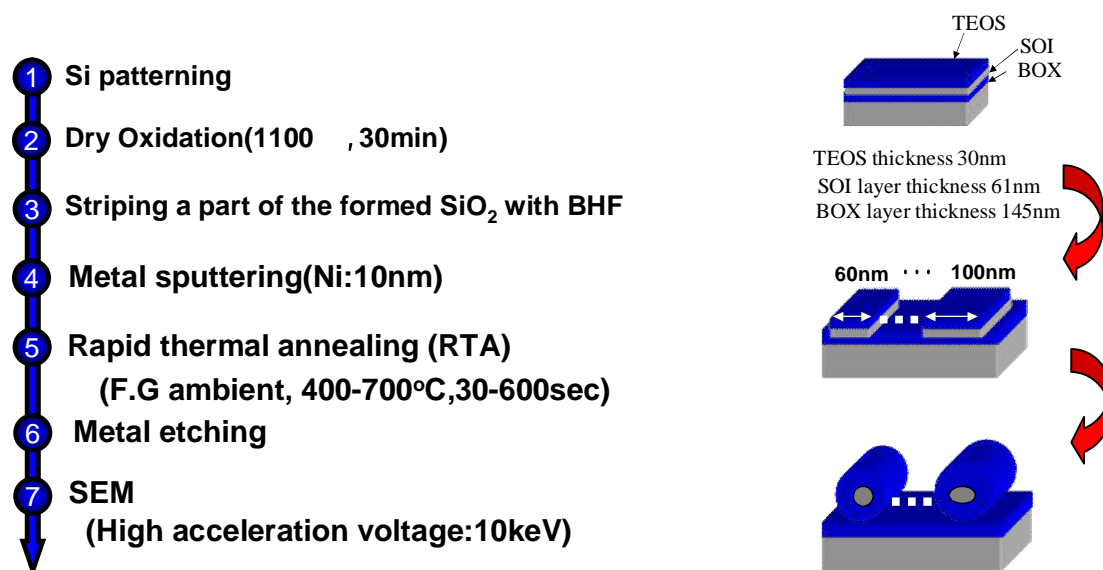
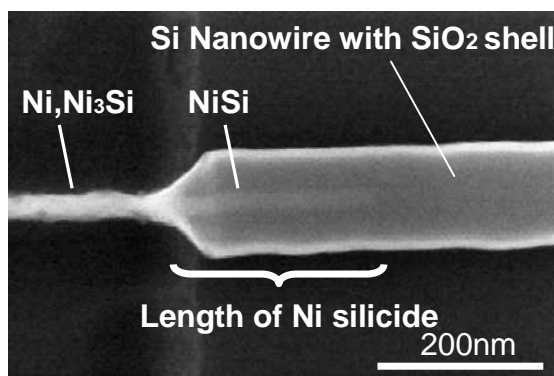


Figure.4.1 Process flow

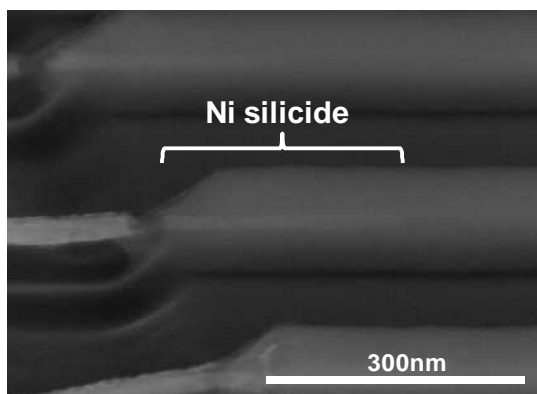


### 4.3 Results and Discussion

Figure.4.2 shows a typical SEM image of a lateral NiSi formation in a Si nanowire. This sample was fabricated at an annealing temperature of 450 °C for 30 sec. A bright contrast in the Si nanowire indicates the formation of NiSi by lateral Ni diffusion. The length ( $\lambda$ ) of the formed NiSi wire was measured from the edge of the Si nanowire.



(a)



(b)

Figure.4.2 SEM image of NiSi formed by lateral Ni diffusion into Si nanowire.

Figure.4.3 shows a flat-screen TEM image of laterally silicied Si nanowire after silicidation at 450°C for 30sec. NiSi/Si interface in Si nanowire might be flat, and there was almost no volume change by NiSi formation in Si nanowire.

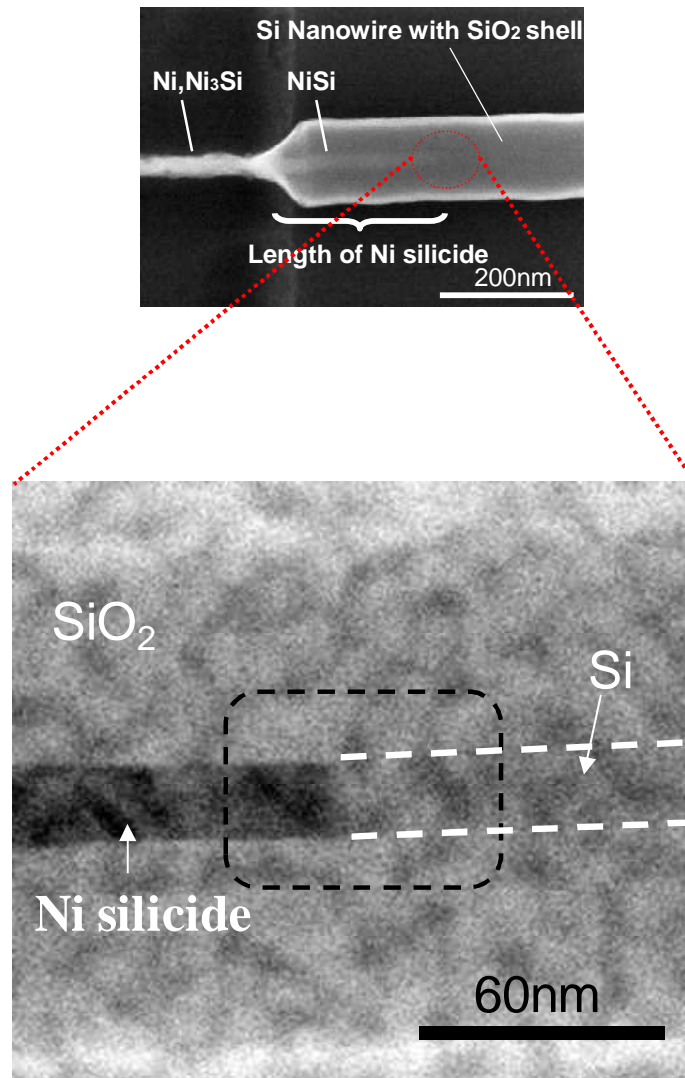


Figure.4.3 A flat-screen TEM image of laterally silicied Si nanowire after silicidation at 450°C for 30sec. NiSi/Si interface in Si nanowire might be flat, and there was almost no volume change by NiSi formation in Si nanowire.

Figure 4.4 shows the length of NiSi formed at 400, 450 and 500 °C on a Si nanowire with a cross section of  $7.5 \times 12 \text{ nm}^2$ . Higher temperature annealing results in longer NiSi formation and the length of NiSi increases with the annealing time. Therefore, it can be speculated that NiSi formation on Si nanowire is a thermally activated process. However, after annealing for 300 sec, the formation seems to saturate.

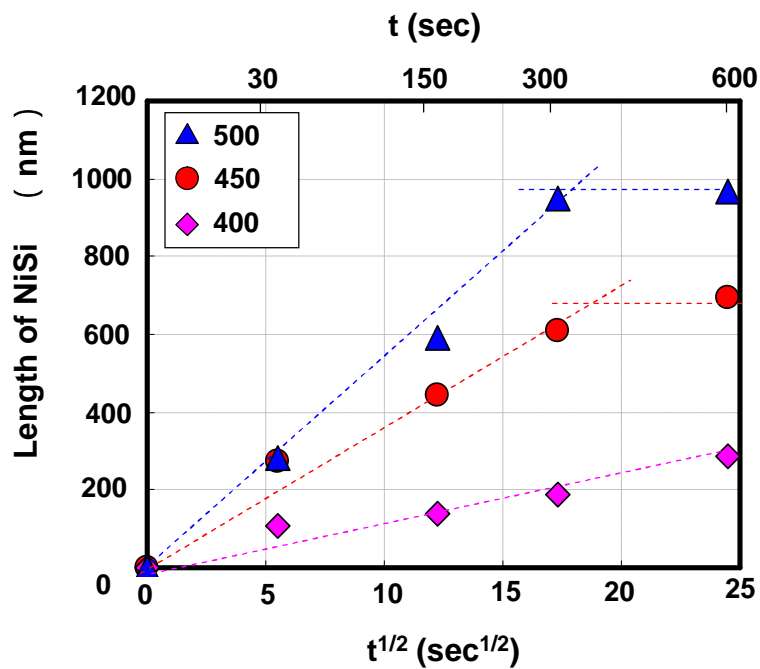


Figure .4.4. Length of NiSi on square root of the annealing time.

The dependence of the length of NiSi on annealing temperature is shown in figure 4.5. A monotonic relationship was observed up to a temperature of 600 °C, however, a progressive formation over 3 μm was observed above 650 °C. Generally, the temperature required for phase transition from NiSi to NiSi<sub>2</sub> for thin film case is known to be 700 °C [5]. As the cross section is nanometer size and also that the direction of Ni diffusion is one dimensional for our experiment, a lowering of phase transition temperature down to 650 °C might happen.

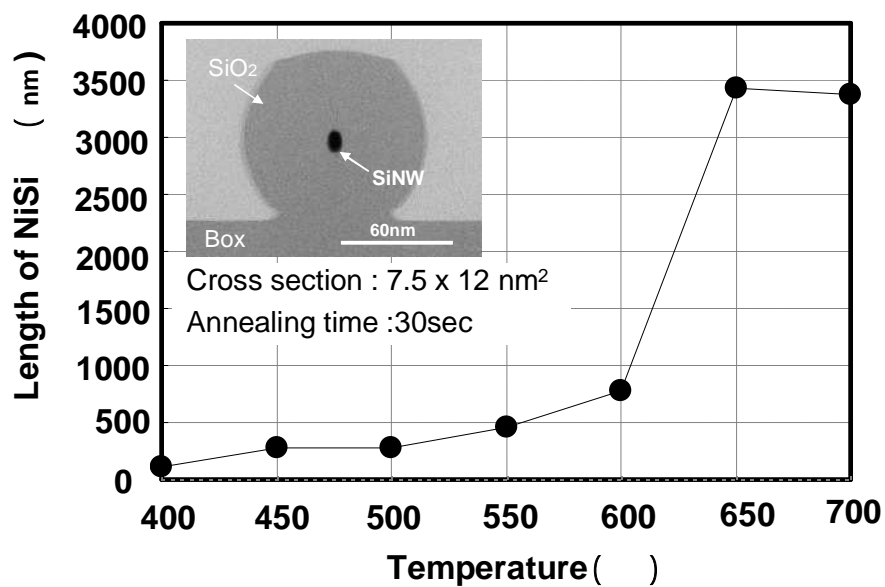


Figure.4.5. Diffusion length of Ni in <100> Si nanowire versus temperature range 400-700 °C.

Figure.4.6(a)-(c) show SEM images of a sample annealed at 650 °C for 30 sec at the edge of exposed region. Grains with a size of 80 nm were observed at the entrance of NiSi wire. These grains were also observed for the samples annealed at a temperature of 500 °C for 600 sec although the size is much smaller. Considering that there was almost no volume change by NiSi formation in Si nanowire, the lateral diffusion of Ni may be accompanied with a lateral diffusion of Si in the opposite direction. As these grains were observed at the entrance of the NiSi wire, the Si atoms may diffuse along the NiSi/SiO<sub>2</sub> interface. Therefore, it can be speculated that both Ni and Si are the diffusing species for NiSi formation in Si nanowire. Figure.4.7 shows the model on the lateral diffusion of Ni in Si nanowire.

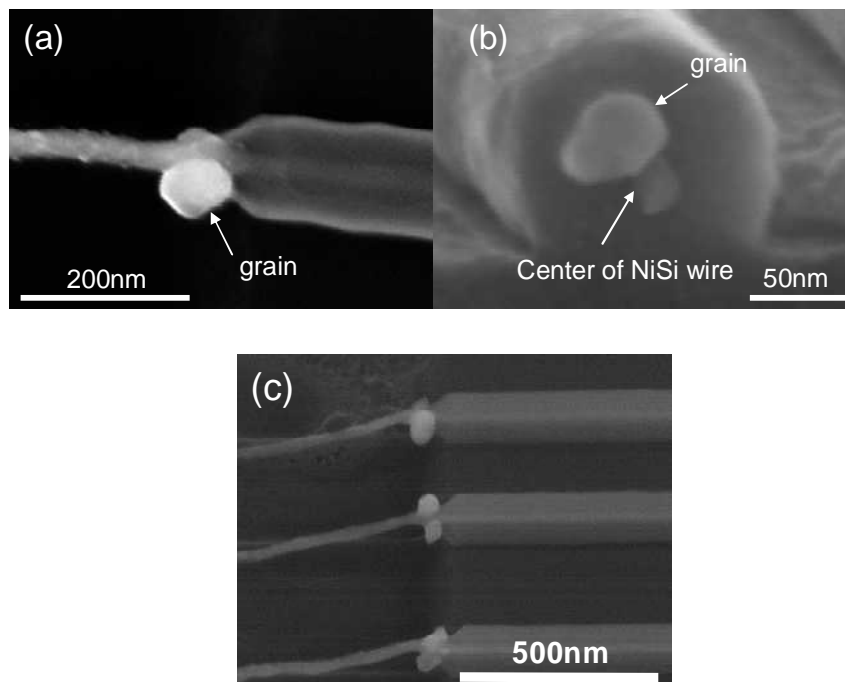
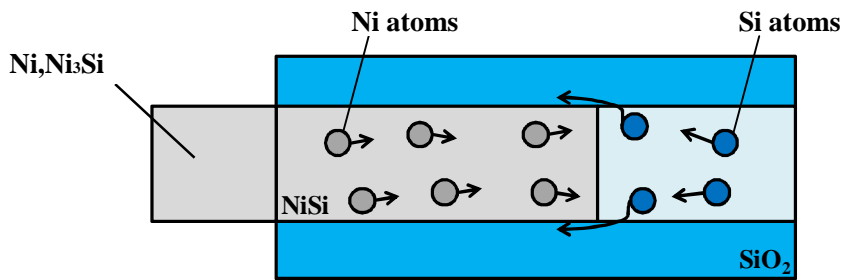


Figure .4.6 SEM image of (a) top view , (b) cross section ,(c) oblique of Ni diffusion in Si nanowire after annealing at 650 °C for 30 sec.

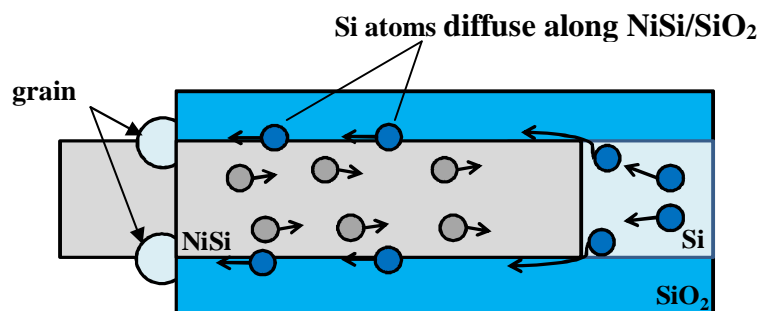


- (a) After striping a part of the formed  $\text{SiO}_2$  with buffered HF to expose Si nanowires, Ni film is deposited by magnetron sputtering.

RTA



- (b) NiSi in Si nanowire is formed by lateral Ni diffusion. Due to interstitial diffusion, Ni atoms diffuse through Si than through silicide. Si atoms diffuse along NiSi/SiO<sub>2</sub>.



- (c) As Si atoms diffuse along NiSi/SiO<sub>2</sub>, Grains occur at the entrance of NiSi. In other words, both Ni and Si are the diffusing species for NiSi formation in Si nanowire.

Figure.4.7. The model about the lateral diffusion of Ni on Si nanowire

The cross-sectional area dependence on the length of NiSi formed at annealing temperatures of 400-600°C for 30sec is shown Figures.4.8-4.12. As a cross-sectional area on the Si nanowire is smaller, the length of NiSi formed at annealing temperature ranging from 400 to 600°C increases. On the contrary, The length of NiSi decreases as a cross-section area on Si nanowire is larger. In other words, a cross-section area or a diameter dependence on the lateral diffusion of Ni was observed.

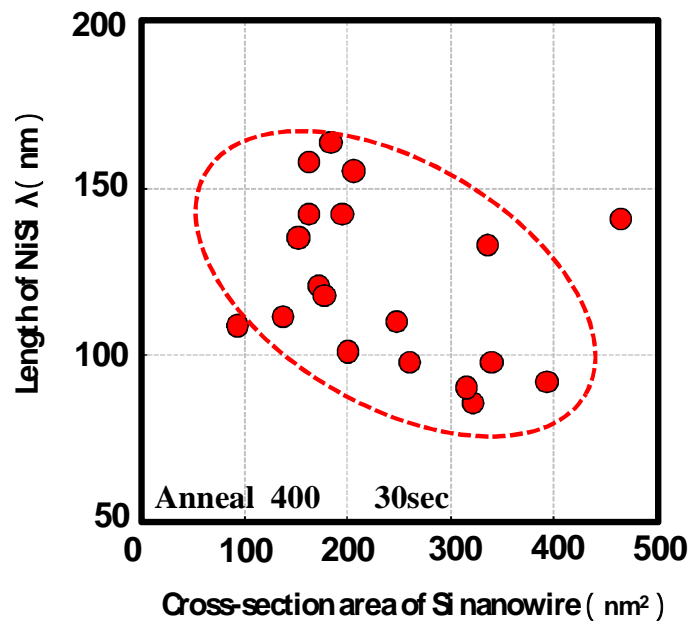


Figure.4.8. The cross-section area dependence on the length of NiSi formed at annealing temperature at 400°C for 30sec

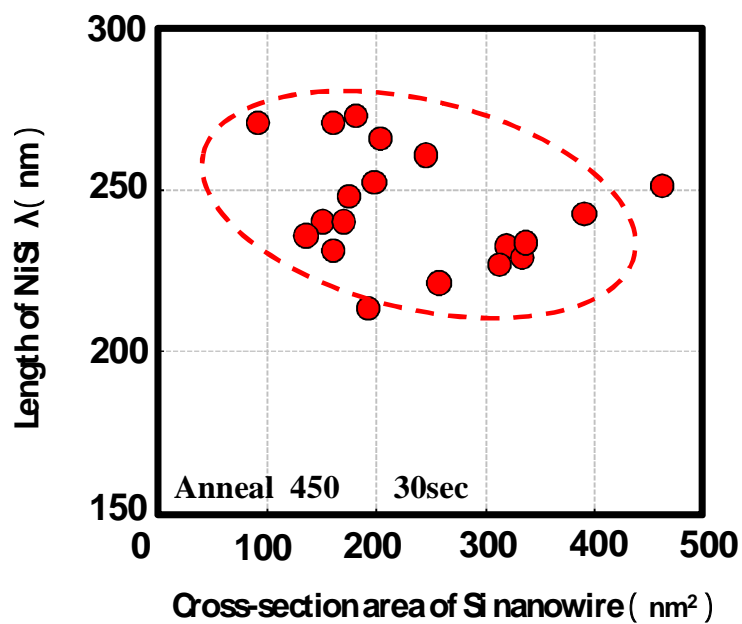


Figure.4.9. The cross-section area dependence on the length of NiSi formed at annealing temperature at 450°C for 30sec

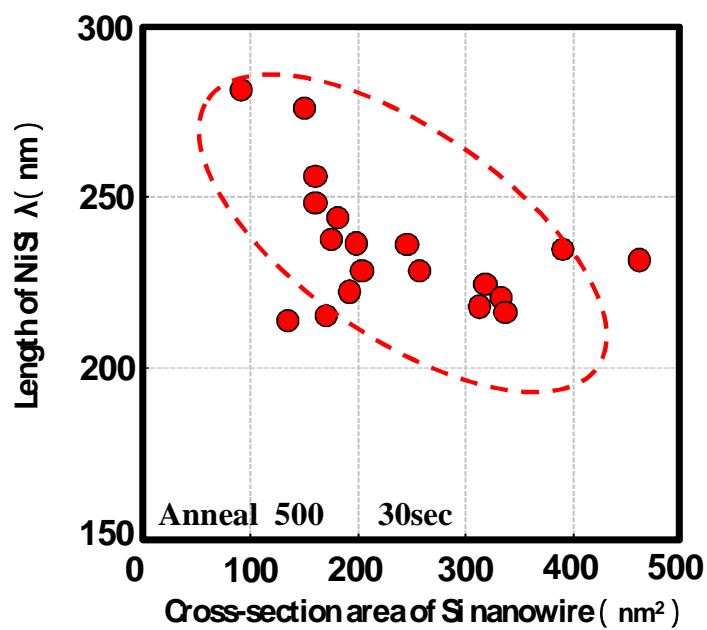


Figure.4.10. The cross-section area dependence on the length of NiSi formed at annealing temperature at 500°C for 30sec



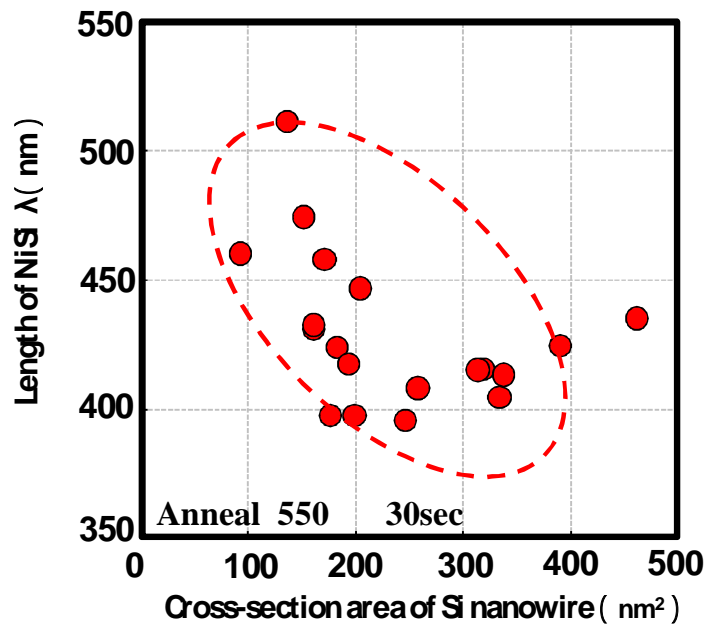


Figure.4.11. The cross-section area dependence on the length of NiSi formed at annealing temperature at 550°C for 30sec

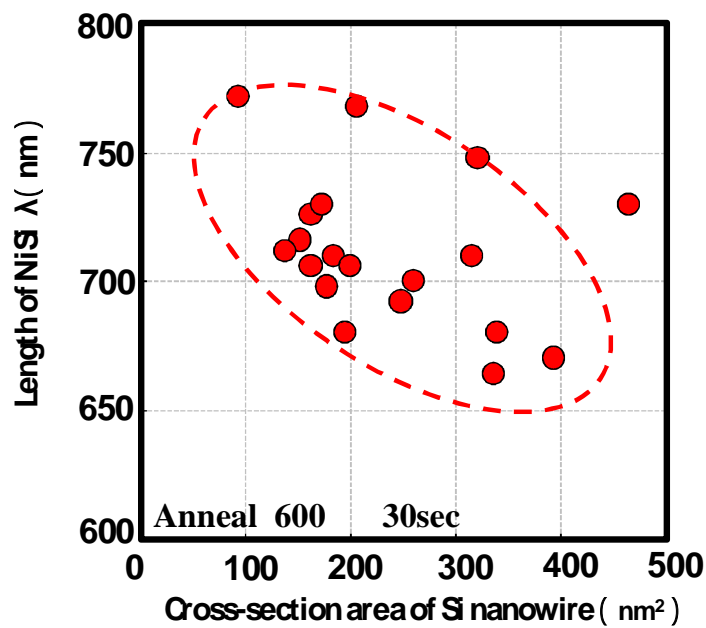


Figure.4.12. The cross-section area dependence on the length of NiSi formed at annealing temperature at 600°C for 30sec

The rate of growth  $\lambda^2/t$  on a Si nanowire with a cross section of  $7.5 \times 12 \text{ nm}^2$  is plotted in Figure.4.13. The straight line represents an activation energy of about 0.9 eV. The activation energies dependence of NiSi formation to Si nanowire of different cross sectional areas are shown Figure.4.14. An average activation energy of 0.9 eV has been obtained irrespective to the cross sectional area. The activation energies of the Ni diffusion in  $\langle 100 \rangle$  Si nanowires are not depended on the cross-section area of Si nanowire. As the activation energy for NiSi formation on bulk Si(100) wafer is  $1.2 \pm 0.3 \text{ eV}$  [6], the smaller activation energy for Si nanowire might come from one dimensional direction during the diffusion.

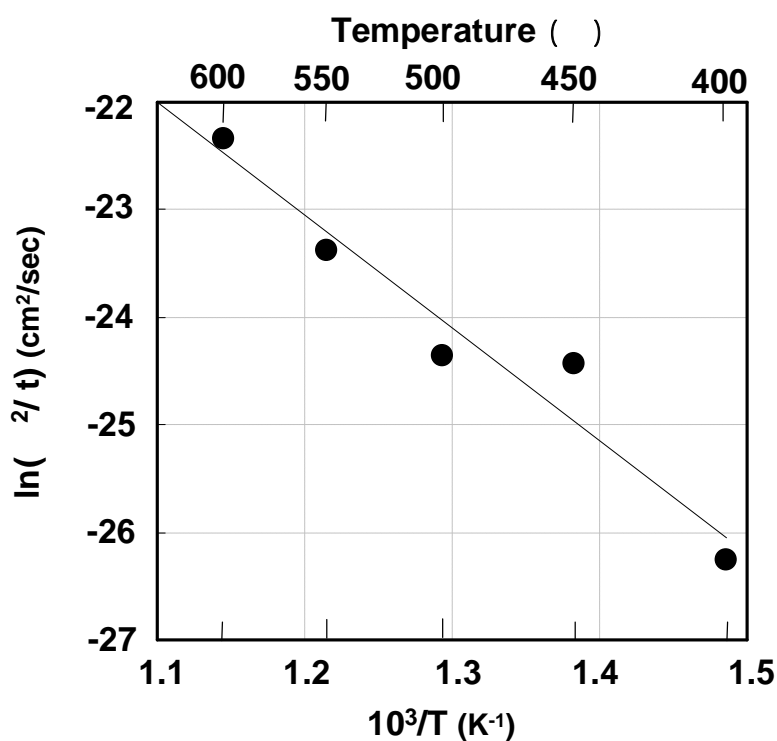


Figure.4.13. Arrhenius plot of  $\lambda^2/t$  on a Si nanowire with a cross section of  $7.5 \times 12 \text{ nm}^2$ .

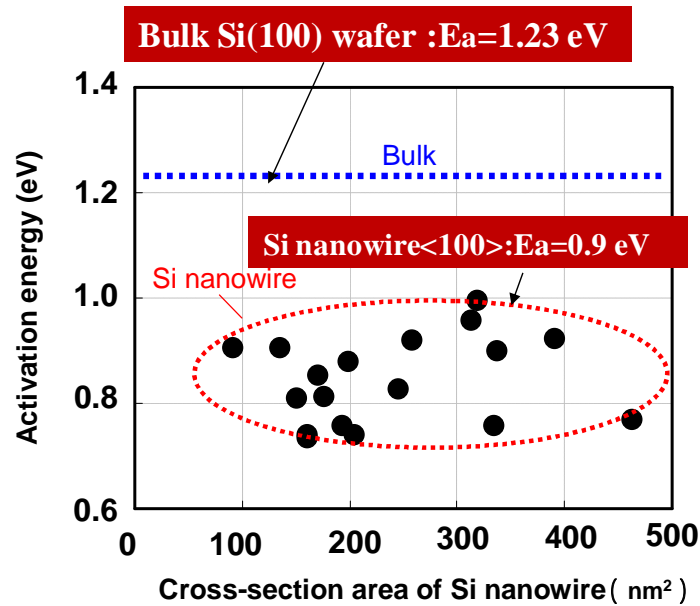


Figure.4.14 Plot of activation energy versus cross-section area of Si nanowire.

#### 4.4 Summary

Lateral Ni diffusion in Si Nanowire to form NiSi Schottky contact was characterized by scanning electron microscope (SEM) at temperatures range from 400 to 700 °C. Higher temperature annealing results in longer NiSi formation and the length of NiSi increases with the annealing time. A strong diameter dependence on the lateral diffusion of Ni was observed. The activation energy for NiSi formation on Si nanowires are found to be 0.9 eV which is lower than that on bulk case. One-dimensional diffusion of Ni with Si nanowire might be the reason for lowering the activation energy.

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# Chapter 5

## *Conclusion*

*5.1 Results of this study*

*5.2 Subject to the Future*

## ***5.1 Results of this study***

In this thesis, we investigated the nanowire thinning and rounding by oxidation and the Ni silicide contact formation for the Si nanowire FET. This chapter summarized the results of the studies referred to in this thesis .

### *Chapter3*

#### *Oxidation of Si nanowire for Sub-10nm cross-sectional shape optimization*

In the case of Si fin aspect ratio about one, Si nanowire oxidized at 1100 °C is very circular and can be fabricated Si nanowire of 9nm in diameter. After 1000 °C dry oxidation for 60 min, the nanowire oxidation rate is strongly reduced. A consequence of this oxidation rate reduction on convex structures such as nanowires is that, the oxidation will stop by itself when the oxide layer thickness reached large enough. To reduce the Si nanowire of under 10nm in diameter, we conducted reoxidation after removing the oxide layer formed by dry oxidation at 1000 °C for 60min. This method means to relax the stress of the Si/SiO<sub>2</sub> interface. As a result, Si nanowire oxidized at 1000 °C for 90min could be fabricated Si nanowire of under 10nm in diameter.

### *Chapter4*

#### *Evaluation of Lateral Nickel Diffusion in Si Nanowire Schottky Contact*

Lateral Ni diffusion in Si nanowire to form NiSi Schottky contact was characterized by scanning electron microscope at temperatures ranging from 400 to 700 °C. Higher temperature annealing results in longer NiSi formation at the same annealing time and the length of NiSi increases with the annealing time. The activation energy for NiSi formation on Si nanowires are found to be 0.9 eV which is lower than that on the bulk

case. One-dimensional diffusion of Ni with Si nanowire might be the reason for lowering the activation energy.

## ***5.2 Subject to the Future***

Ni silicide is a commonly used technology to reduce the access resistance for modern ULSI device and will still used for the future devices. However, it suffers from many difficulties such as composition and mechanical stress during the process, so that the process window to form Ni silicide is always small. In the highly scaled device, Si nanowire FET is becoming a strong the candidate among other devices and Ni silicide will be used as well. In this study, we found that it was difficult to control the diffusion of Ni in Si nanowire. But the parastic S/D resistances in extremely scaled GAA nanowire devices can pathologically limit the device current performance. In order to obtain high performance, it is imperative that to form low resistivity metallic nanowire contacts intruded Ni silicide reduces parasitic resistance. Thus, to control the diffusion of Ni in Si nanowire will be next investigation object.



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*January 2009*