Master Thesis

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New Stress Inducing Technique for UTBSOI

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Contents

Overview

Purpose of this study

Mechanism of SMT is studied in order to induce stress in the channel of the UTBSOI (Ultra-Thin-Body Silicon On Insulator) MOSFET (Metal Oxide Semiconductor Field Effective Transistor). The UTBSOI MOSFET is difficult to induce strain by the conventional methods because of problems caused by its structure made of ultrathin SOI substrate. The primary purpose of the study is thus investigating how to induce stress in the UTBSOI MOSFET with a very thin channel layer. In many stress including techniques, first of all in this study, SMT (Stress Memorization Technique) was investigated because this technique is promising in terms of scalability. The mechanism of SMT, however, has not been clarified yet. Therefore, the purpose of the study is to clarify the mechanism of SMT.

Results of this study

The experimental result of the planar sample revealed that, after annealing, the planar sample is in a compressively strained state caused by residual Ar. The experiments on the patterned sample revealed the following results.

I. Large strain distribution was observed corresponding to the step-like

pattern of SiN stress film and silicon substrate.

II. Ar implantation and annealing acted on wakening the strain contrast caused by the patterning.

III. Wafer bending measurements revealed that the Ar implantation and annealing decreased stress of the SiN film. Therefore, the above strain contrast weakening was caused both by Ar implantation and weakening the SiN film stress.

Through the above investigation, the method for evaluating strain distribution of patterned samples was established by using UV micro Raman spectroscopy.

Comments of the future work

SMT effect is thought to be occurred by including stress both from poly-Si gate electrode and S/D region by implanting dopant atoms and annealing with a capping stress film. For the investigation on stress distribution of such samples with complex structures, the analysis method established in this study can be useful. The major factors of SMT are considered to be an introduction of heterogeneous atoms by implantation, poly-grain growth of gate electrode by annealing, and/or

end-of-range-defect formation in a silicon substrate. And these phenomena can be enhanced by capping a stress film. Therefore, using this analysis method, the investigation of strain distribution for variety of samples with different structures and preparation conditions will be helpful to know what is a dominant factor for SMT.

Chapter 1

Introduction

1.1 Background of this study

1.2 Conventional booster technique

1.3 Problem on the implementation of strained-Si technology on UTBSOI.

1.4 Previous works on SMT

1.5 Purpose of the study

1.1 Background of this study

Until now, the more MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is downsizing with the scaling rule [1], the less cost per function has been achieved due to the increase in number of transistors in a chip, accompanied with improving performance and reducing power consumption per transistor. The scaling rule is based on reducing the device dimension in both lateral and vertical direction. A simple description of the scaling with the factor κ is shown in Figure 1 and Table I. Gate length(L), width(W), and oxide thickness(t_{ox}) are downsizing L/κ, W/κ, and t_{ox}/κ, respectively, while increasing κ-times impurity concentration(N_A) in order to decrease depletion width(X_D) to X_D/κ. To gain κ times increase of the device performance, the physical device dimensions should be reduced by a factor of κ, at the same time, voltage(V) should also be decreased by a factor of $1/\kappa$. However, further downsizing the CMOS (Complimentary MOSFET) is difficult to be done with improving both performance and power efficiency, because of the short channel effect, increasing leakage current and V_{th} fluctuation. For example, power consumption of the super computer is continuously increasing to reach maximum electricity that can

be generated from a single powerhouse. Therefore, CMOS needs to further remain improving both performance and power efficiency in order to continue downsizing. UTBSOI device has excellent short channel effect immunity due to thin body and also has small V_{th} fluctuation. Therefore, the UTBSOI device has an advantage in downsizing over bulk CMOS.
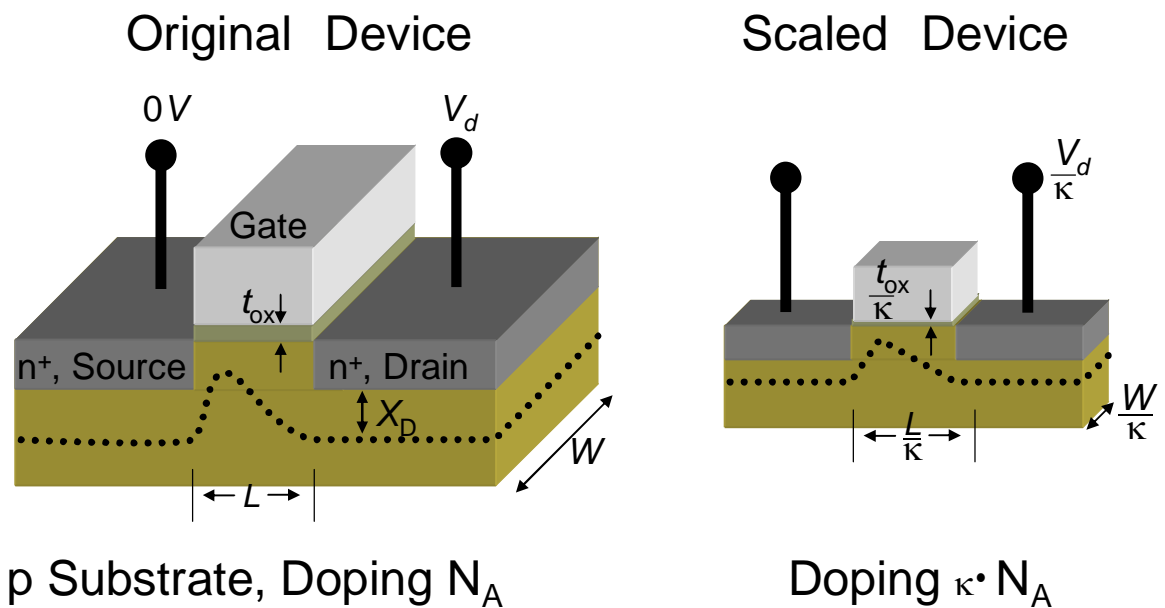
Original Device

0 V V_d

Gate

t_{ox}

n$^+$, Source   n$^+$, Drain

X_D

W

$\leftarrow L \rightarrow$

p Substrate, Doping N$_A$

Scaled Device

$\dfrac{V_d}{\kappa}$

$\dfrac{t_{ox}}{\kappa}$

$\dfrac{L}{\kappa}$

$\dfrac{W}{\kappa}$

Doping κ N$_A$

Fig. 1 Principles of constant-electric-field scaling for MOS transistors.

Table I. Generalized Scaling Factors

Physical Parameter	Scaling factor
Dimensions (W, L, t_{ox}, x_j)	$1/\kappa$
Impurity Concentration (N_A)	κ
Electric Field	1
Capacitance	$1/\kappa$
Current	$1/\kappa$
Voltage	$1/\kappa$
Power Density	1
Gate Delay	$1/\kappa$
Power-delay Product per circuit	$1/\kappa^3$
Circuit Density	κ^2

1.2 Conventional booster technique

The performance of the leading-edge CMOS is improving not only by miniaturizing the gate length but also by booster techniques. There are several techniques such as (110) substrate [2], metal source-drain [3], strained silicon [4], and so on. This study focuses on the strained-silicon technique. These strained-silicon techniques can be classified into two, global and local. In the global technique, strained-silicon substrates such as bulk [5], SGOI (Silicon Germanium on Insulator) [6], and so on, are used. But the global technique is difficult to improve both nMOS and pMOS at the same time [7]. On the other hand, in the local strain technique, many techniques such as stress liner [8], embedded SiGe [9], embedded SiC [10], STI-induced strain [11] and SMT (Stress Memorization Technique) [12] have been proposed. The combination of proper local techniques can apply different stress that is suitable for both nMOS and pMOS. That is, different stress liners can separately be used for nMOS and pMOS.

1.3 Issues on the implementation of strained-Si technology on UTBSOI.

Scalability of the strained-Si technique should be considered in order to use this technique for the extremely scaled CMOS. But it is reported that the conventional strain techniques such as stress liner have become inefficient with decreasing gate length [13], [14]. Figure 2 shows the effect of the stress-film thickness on stress with a constant gate pitch. The stress peak point moves upwards once the space is completely filled with the stress film, which decreases channel strain. Therefore, this result indicates that the more shrinking the space with the same stress film thickness, the weaker the stress in the channel region because of filling spaces with the stress film. As for the embedded SiGe technique, which is one of the effective stress techniques for the bulk pMOS, there is a problem: the thickness of the embedded SiGe layer which can be embedded in the UTBSOI structure is less than the bulk CMOS because of thin body.

As for the SMT, stress memorization can be caused by both S/D (source and drain regions) and gate electrode. When S/D and gate electrode are downsizing, memorized stress will probably become weak. But due to

downsized channel region, the effect might remain constant. Therefore, the amount of memorized stress cannot be reduced by scaling. SMT is thus considered to have scalability.
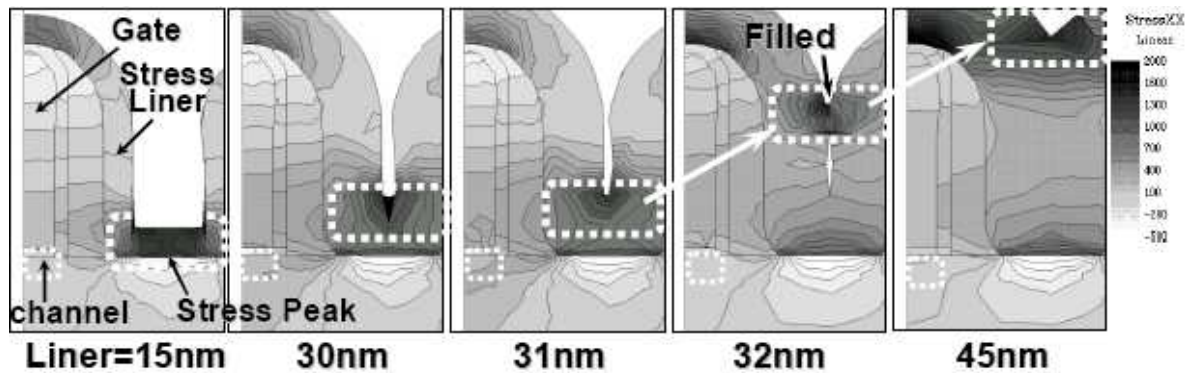

Fig. 2 Relationship between film thickness and stress distribution

1.4 Previous works on SMT

Concerning this technique, several methods have been proposed so far: annealing poly-Si gate electrodes with a capping layer after source and drain (S/D) implantation [12], implantation and annealing of S/D region capped with a stress film [15], annealing poly-Si gate electrodes capped with a stress film without a pre-implantation [16], Ge and/or F pre-doping and annealing [17, 18], and so on. The mechanism of stress "memorization", however, has not been clarified yet.

Table II: Previous Works

Strain source	Source material	Implantation	Cap	Ref.
Gate	Poly	Yes	SiO$_2$	[12]
Gate	Poly	Yes	SiO$_2$	[17]
Gate	Amorphous	Yes	SiO$_2$	[19]
Gate	Poly	Yes	SiN	[18]
S/D	Crystal	Yes	SiN	[15]
Gate	Poly	No	SiN (tens. > comp.)	[16]
Gate	Poly	No	SiN	[20]

1.5 Purpose of the study

The purpose of the study is to clarify the mechanism of SMT which is a powerful booster technique for downsizing UTBSOI devices. From the previous works, the "memorization" might occur with multiple causes such as (i) introduction of heterogeneous atoms by implantation, (ii) poly-grain growth of gate electrode by annealing, or (iii) end-of-range-defect formation in a silicon substrate by implantation, and these phenomena can be enhanced by capping a stress film.

As the first step of the investigation, the effect of Ar implantation and annealing of silicon substrates with and without a stress film was

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examined Ar was selected because it is inert, it can be desorped by annealing, and it can easily amorphize silicon. Stress measurement is done by micro Raman spectroscopy. In this study, for the first time, stress distribution was analyzed in the patterned samples through the spectral integration and deconvolution of each position in the pattern.

Chapter 2

Sample preparation and characterization

2.1 Sample preparation

2.1.1 Fabrication procedure of planar samples

2.1.2 Fabrication procedure of patterned samples

2.2 Characterization

2.2.1 UV Raman spectroscopy

2.2.2 Ar concentration measurement by SIMS

2.2.3 SiN film stress measurement by wafer bending

2.1 Sample preparation

2.1.1 Fabrication procedure of planar samples

Fabrication procedure of planar sample is shown in figure 4. After cleaning a p-type Si (100) wafer by SPM ($H_2SO_4+H_2O_2$), APM ($NH_3+H_2O_2$), and DHF (diluted HF), the wafer was oxidized to form a 10 nm thick SiO_2 layer. Ar ions were implanted perpendicular to the silicon substrate. Acceleration voltage was 100 keV and dose amount was 5×10^{14} cm^{-2}. Then, a silicon nitride film of 100 nm thick by a Plasma-Enhanced Chemical Vapor Deposition (PECVD) with stress of -1.7 GPa (strong) or 6 MPa (weak) was deposited on a silicon substrate at 400 ^{o}C in order to avoid recovery of damage caused by the Ar implantation during the deposition. Finally, the samples were subjected to rapid thermal annealing (RTA) at 900 ^{o}C for 30 s. A portion of samples was further annealed in a furnace at 950 ^{o}C for 25 min. Finally, the PECVD silicon nitride (PE-SiN) film was removed in hot phosphoric acid solution for some samples.
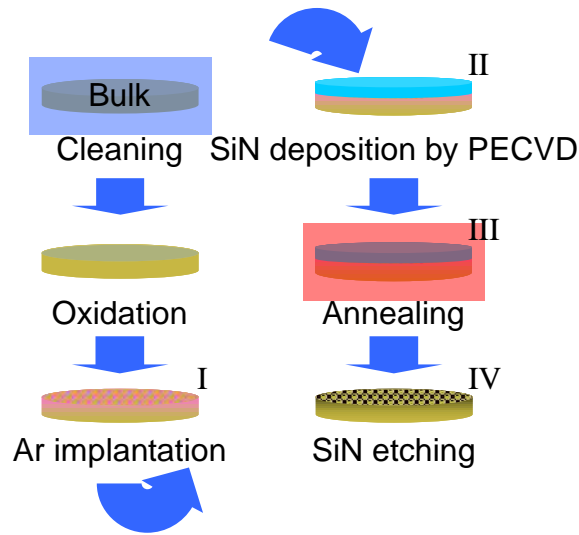
Fig. 4 Fabrication procedure of planar sample

2.1.2 Fabrication procedure of patterned samples

Figure 5 shows the fabrication procedure of patterned samples. After cleaning a silicon substrate, the surface was oxidized to form a 10 nm thick SiO_2 layer. Next, a 120 nm thick SiN film was formed by $\underline{L}$ow $\underline{P}$ressure $\underline{C}$hemical $\underline{V}$apor $\underline{D}$eposition (LPCVD). Then, trenches were formed by a dry etching. And a thermal CVD SiO_2 film of 20 nm thick was deposited. Next, Ar ions were implanted at a tilt angle of 25 degrees. Acceleration voltage was 100 keV and dose amount was 5×10^{14} cm^{-2}. This voltage was set so that the projected range of Ar implantation is about 120 nm in silicon substrate from the simulation result as shown in figure 6. The other side of the trench was also implanted by rotating the wafer as shown in figure 5. The LP-SiN layer worked as a hard mask for the Ar implant and

thus the dose amount of Ar on top of the silicon substrate through the SiN layer was negligibly smaller than 1×10^{18} cm^{-3}. Parts of samples were covered with a PE-SiN film of 100 nm thick on a whole area of the silicon substrate. Finally, the wafers were subjected to the annealing processes which are the same as the planar samples.
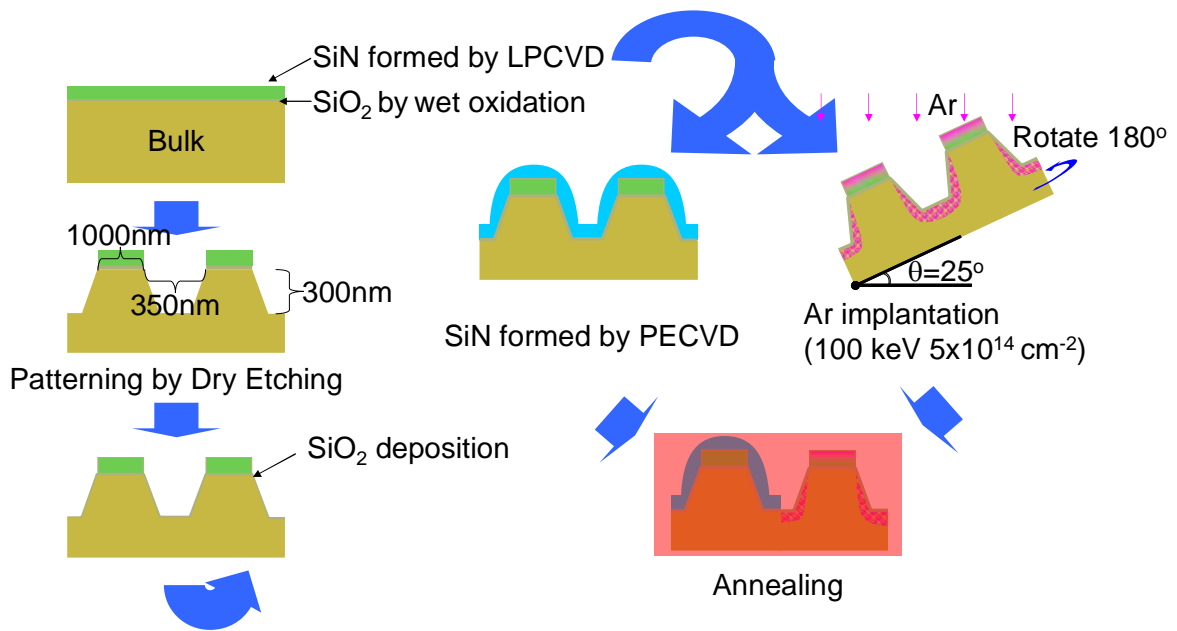

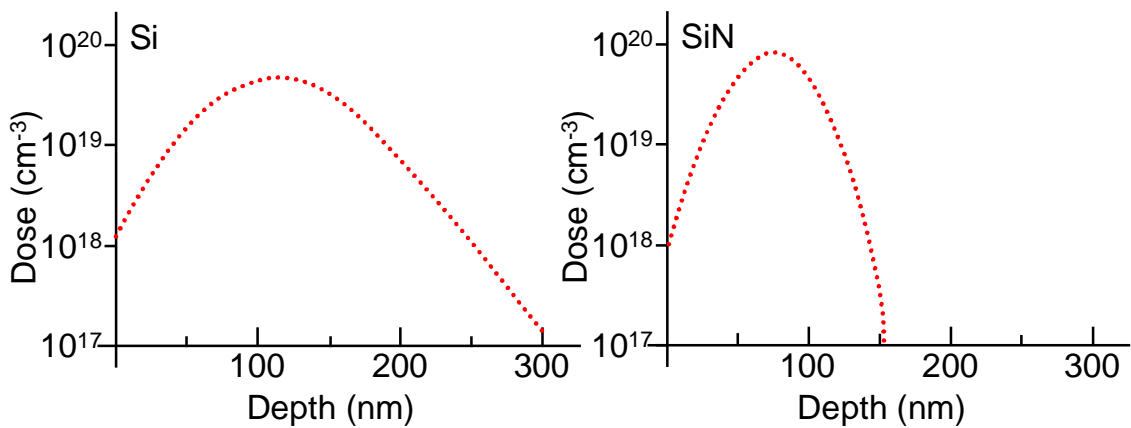**Fig. 5 Fabrication procedure for patterned sample**

Fig. 6 Depth profile of Ar in Si and SiN. Acceleration voltage and dose amount are 100 keV and 5×10^{14} cm^{-2}, respectively.

2.2 Characterization

2.2.1 UV Raman spectroscopy

Strain at the surface region of the samples was characterized by UV-Raman spectroscopy. Details of the measurement are described in Ref. [21]. UV laser of 364 nm in wavelength was used. Penetration depth of the light is only 5 nm. Strain is thus evaluated only at the surface of the sample. The Raman spectrometer has a resolution of 0.2 μm in position and 0.05 cm^{-1} in wavelength. Raman spectra corresponding to Si-Si vibration mode were collected. In this study, the deviation from the 520 cm^{-1} peak corresponding to bulk silicon was defined as the Raman shift value as shown in Fig. 7.
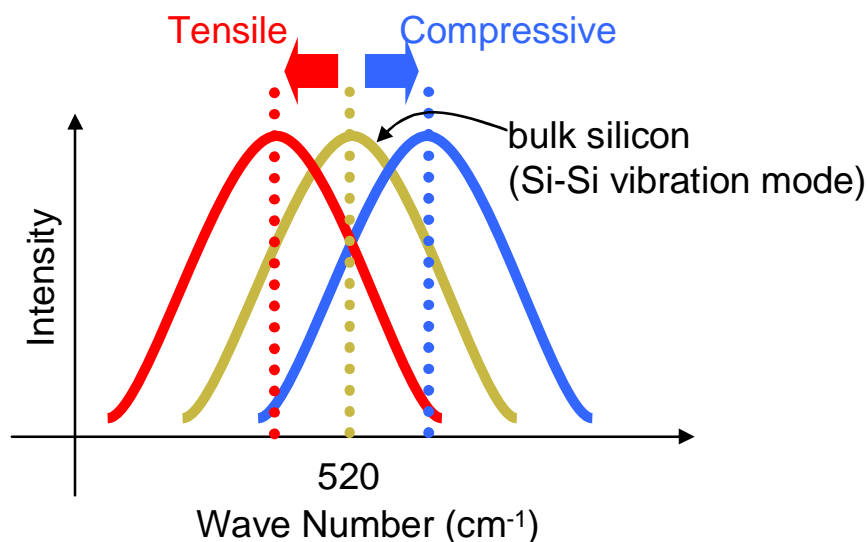

Fig. 7 Relation between stress and Raman spectra

That is, the positive value indicates compressive strain and vice versa. The shape of the light source for the conventional Raman spectroscopy is spot. In this study, by combining a line shape light source and a two dimensional CCD pixel array detector, the spectra along illumination line were simultaneously collected. The line shaped light with high homogeneity was obtained by using the high-frequency vibrating Galvano mirror as shown in figure 8. Figure 9 shows a typical Raman spectrum. Left and right peaks of the spectrum correspond to a Rayleigh and a Raman peak, respectively. The Raman and Rayleigh peaks were fitted with Lorentzian and Gaussian function, respectively. The value 'A' was defined which is a wave number difference between the Raman and the Rayleigh peaks for the sample to measure. On the other hand, the value 'B' is the difference from the reference sample. The B value can drift due to machine condition (temperature may be a major factor) as shown in figure 10, the Raman shift was thus calculated following the formula (1). Then the stress and strain values were calculated from the Raman shift value using the empirical formula (2) described in Ref. [22].
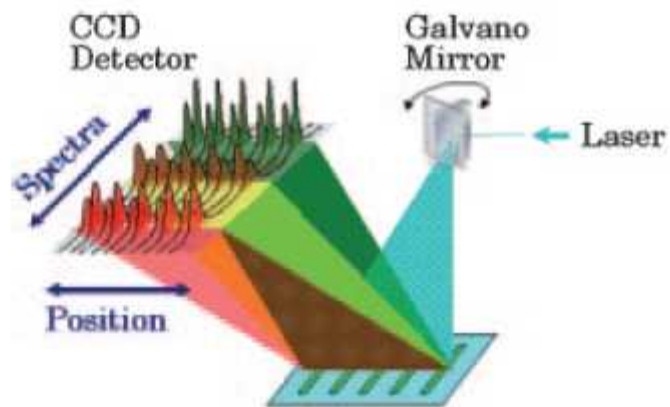
Fig. 8 One dimensional, high spatial resolution analysis using quasi-line shape light source with a Galvano mirror and CCD detector.
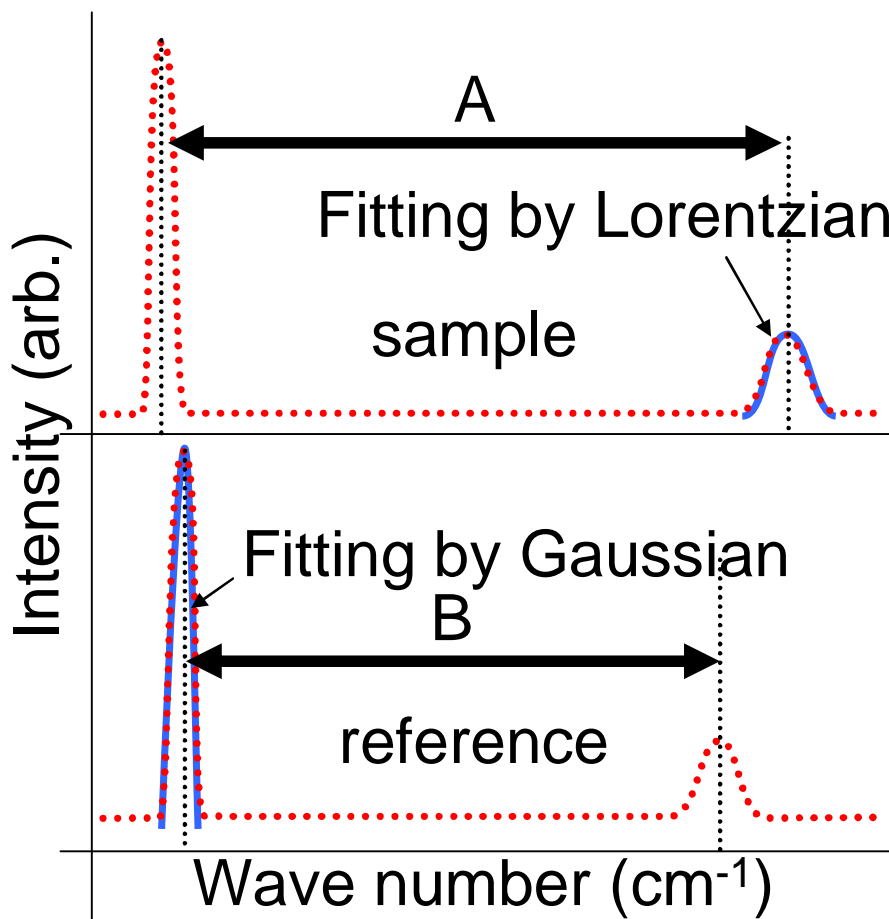

Fig. 9 Typical Raman peaks and Rayleigh peaks for sample and reference silicon

A=Raman peak$_{object}$-Rayleigh peak$_{object}$
B=Raman peak$_{reference}$-Rayleigh peak$_{reference}$
Raman Shift (cm^{-1})=A-B   (1)
Stress (MPa) = -461 x Raman Shift   (2)
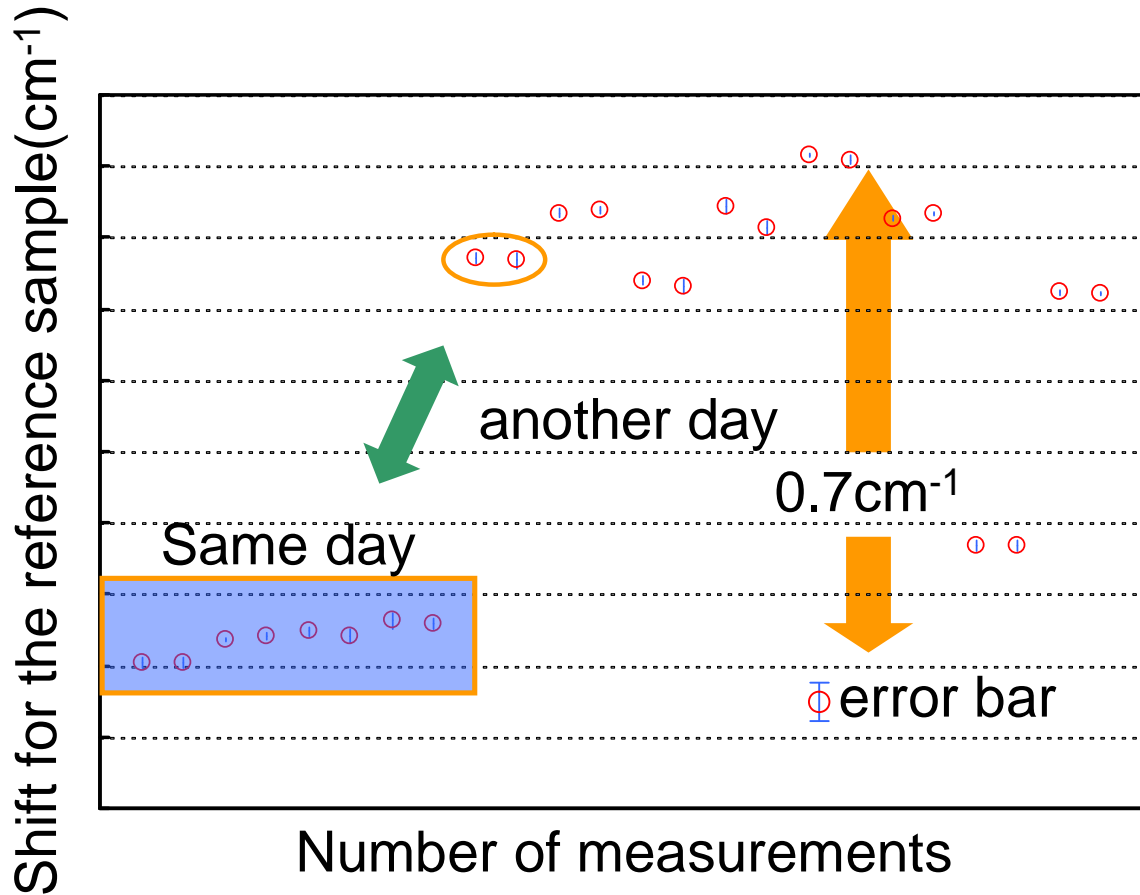**Strain=Stress/Young's modulus(GPa)**

Fig. 10 Drift of Raman shift for the reference sample

2.2.2 Ar Concentration measurement by SIMS

After annealing, depth profile of residual Ar concentration was measured by SIMS (secondary-ion mass spectrometry). Figure 13 shows schematic illustration of SIMS apparatus. Ion gun generates Cs^+ primary ion beam. By irradiating the primary ions to the sample, the secondary ions are emitted from the sample surface. During the measurement, the sample was etched by the primary ion beam. The depth profile can thus be obtained. Secondary ions are accelerated at 3.0 kV. The secondary ions, which go through filter, are selected by its velocity in the electrostatic sector. Following formulas (3) and (4), when both E and R are constant, and V is constant (5). Therefore, the ion only which has specific velocity passes the electrostatic sector which has both specific radius and electrical field. The electromagnetic sector separates the secondary ions by their mass (m/z). Following formula (3) and (6), when both B and R are constant, m is constant (7) (V was already made constant by the electrostatic sector.). Therefore, the ion, which has specific mass, passes the electromagnetic sector. Finally, the number of ions is counted by Faraday cup.

$$\frac{1}{2}mv^2 = zeV \qquad (3)$$

$$\frac{mv^2}{R} = zeE \qquad (4)$$

$$\frac{1}{2}ER = V \qquad (5)$$

$$\frac{mv^2}{R} = Bzev \qquad (6)$$

$$\frac{m}{z} = \frac{eB^2R^2}{2V} \qquad (7)$$

R :Radius, E :Electrical field, v :Velocity of secondary ion,

e :Elementary charge, V :Accelerating voltage,

z :Number of charges, m :Mass of secondary ion,
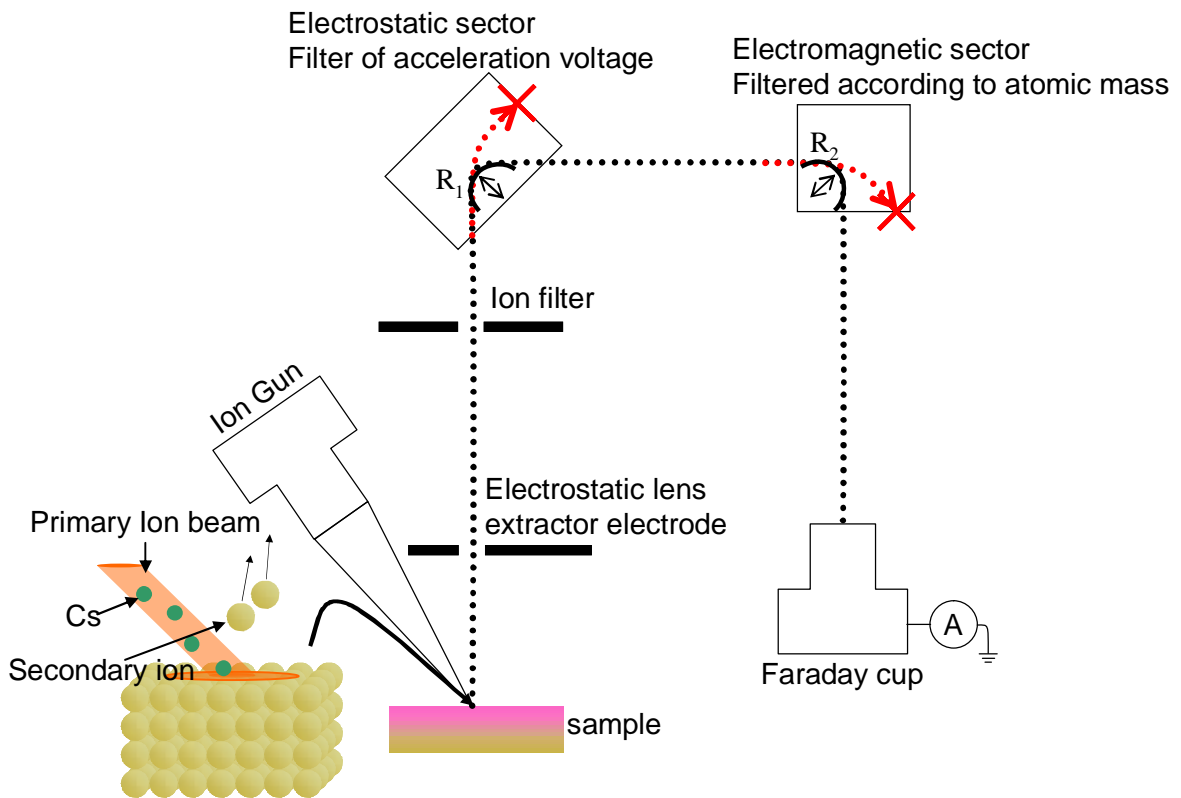
B :Magnetic field

Fig. 13 Schematic illustration of SIMS apparatus

2.2.3 SiN film stress measurement by wafer bending

Internal stress of a 120 nm thick LP-SiN film is evaluated by wafer bending. Figure 14 shows schematic of wafer bending measurement. Curvature radius of wafer with the film was measured by using a laser light. Radius values of wafers before and after deposition of the SiN film were compared. The stress of the film was them calculated with the formula (8).
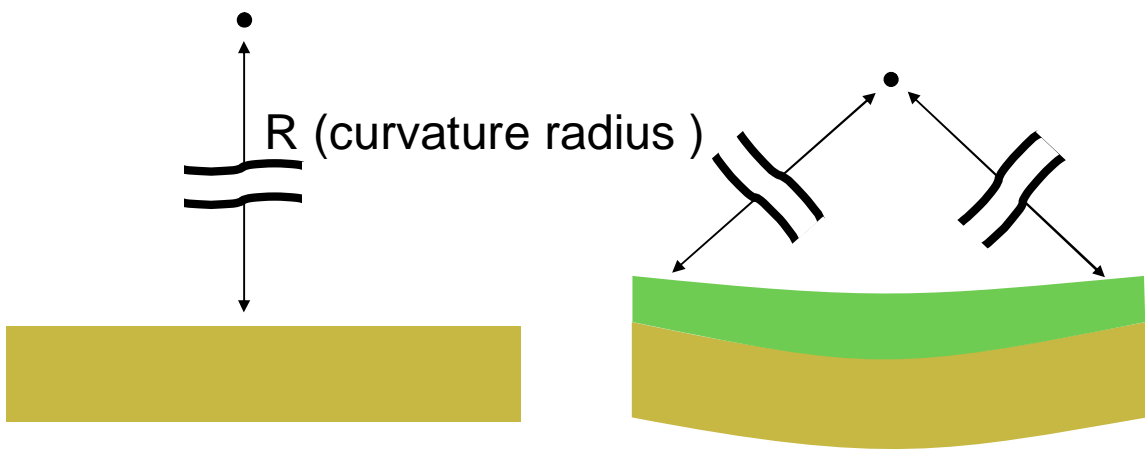

Fig. 14 Wafer bending

Stress (MPa)

$$z \cdot \dfrac{\cdot}{\cdot} \cdot f \cdot \dfrac{}{7} \cdots \dfrac{}{I} - - \dfrac{}{1 \cdot 9 \cdot 2} \Big) \qquad (8)$$

T Film thickness (130 nm in this work)

R ; Curvature radius

Chapter 3
Results and Discussion

3.1 Result of planar samples

3.1.1 Ar implantation and annealing effect

3.1.2 Effect of PE-SiN film on stress

3.2 Result of patterned samples

3.2.1 Ar implantation and annealing effect

3.2.2 Evaluation of LP-SiN film stress

3.3 Conclusion

3.4 Future works

3.1 Result of planar samples

3.1.1 Ar implantation and annealing effect

At first, implantation and annealing effect on planar samples is described. Table III describes samples of this experiment. Samples 1-3 are those without implantation and samples 4-8 are those with implantation. Figure 15 shows peak shift and FWHM of the samples. Note that there is no remarkable difference in peak shift and FWHM between the samples 7 and 8 with a capping SiN film during annealing but those values are smaller than those for the sample 5 (might be due to crystallization enhancement or temperature rise by SiN capping). In samples 4-8 with implantation, a remarkable red shift (<0) was observed for the samples with implantation. But the FWHM values were rather higher than the un-implanted bulk value (2.8 cm^{-1}). This shift might correspond to the incomplete damage recovery even after 900°C annealing (30 s) and not to tensile stress. Then, an additional annealing at 950°C was preformed on sample 5 in order to enhance re-crystallization.

Next, figure 16 indicates Raman shift and FWHM after a long-time annealing, Raman shift values around 0.2 cm^{-1} indicate compressive state and FWHM values are close to the bulk value. Ar concentration as a function of annealing time is shown in figure 17. After a long-time

annealing, Ar still exists in silicon [23]. Therefore, there is some possibility

that residual Ar causes stress.

Table III Sample description

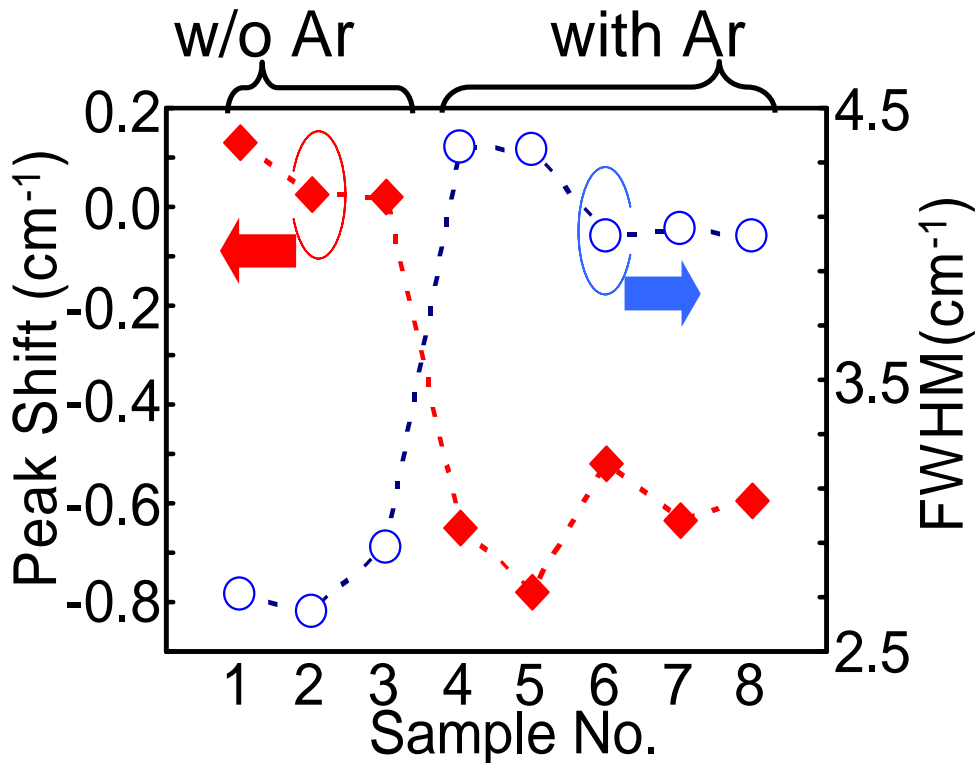| No.	SiN stress	Ar I/I	RTA	etch film
1	strong	no	no	no
2	strong	no	yes	no
3	strong	no	yes	yes
4	strong	yes	yes	yes
5	no film	yes	yes	no
6	weak	yes	yes	yes
7	weak	yes	yes	no
8	strong	yes	yes	yes

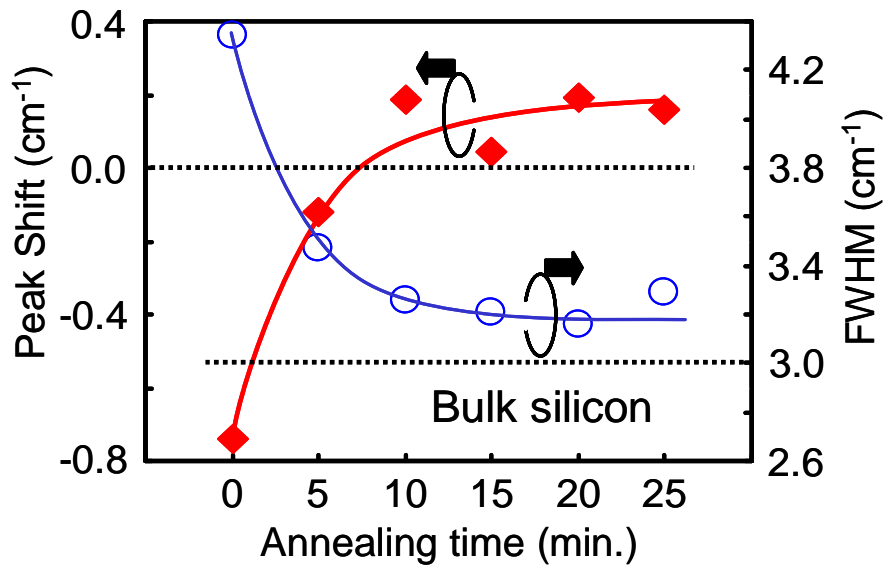**Fig. 15 Peak Shift and FWHM in planar samples**

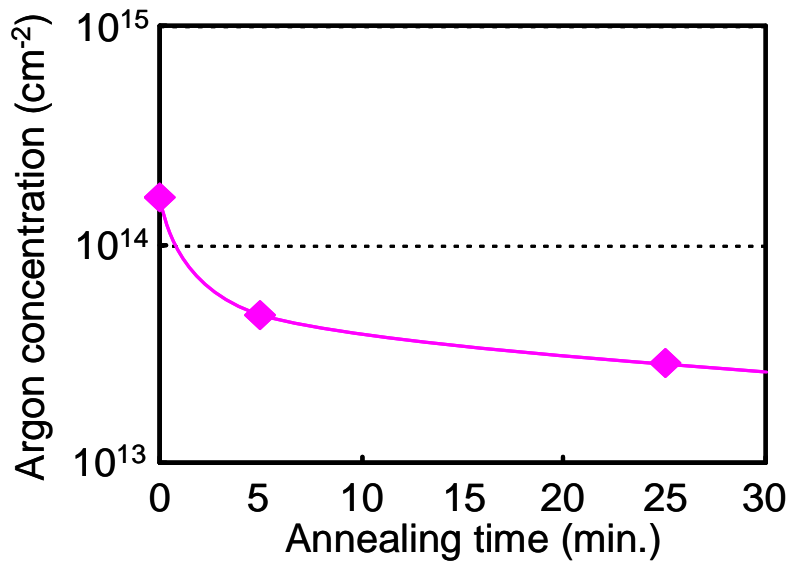**Fig. 16 Annealing-time dependence of Raman-peak shift and FWHM.**

Fig. 17 Annealing-time dependence of argon sheet concentration.

3.1.2 Effect of PE-SiN film on stress

Secondly, the effect of compressive SiN film for planar samples is described. In figure 15, samples 1-3 had nearly zero shift regardless of removing stress film. This result indicates that patterning the stress film is required to induce strain [24].

3.2 Result of patterned samples

3.2.1 Ar implantation and annealing effect

Figures 18 and 19 show peak shift and FWHM without and with Ar implantation, respectively. Annealing at 950 $^{\circ}$C for 25 min was performed for both sample. Position number indicates sample position of the measured area. At about 50-300, structure of the sample is line and space. Structure at around 350 in position number is similar to the planar samples. In the sample without Ar implantation in figure 18, zero shift was observed, likewise the planar sample, whereas in the Ar implanted sample in the figure 19, blue shift about 0.2 cm^{-1} was observed. In the line and space region (50-300), both Raman-shift and FWHM values periodically change with the pattern. The relationship between height (that is, line or space) and shift (or FWHM) is unclear. Thus, the peaks of Raman shift are temporarily called as high and low peaks, respectively. Difference between the high and low peaks in the sample without Ar implantation seems to be larger than

that in the Ar implanted sample. This large difference is due to strain distribution.

In order to clarify this behavior, spectra were integrated 16 times in order to increase signal to noise ratio and then peak deconvolution was performed. Figures 20 and 21 show Raman spectra at high-peak position for samples without and with Ar implantation, respectively. The Raman peak of the sample without Ar could be deconvoluted into two peaks. The major and minor peaks correspond to compressive and tensile state, respectively. This result will be discussed by using simulation.
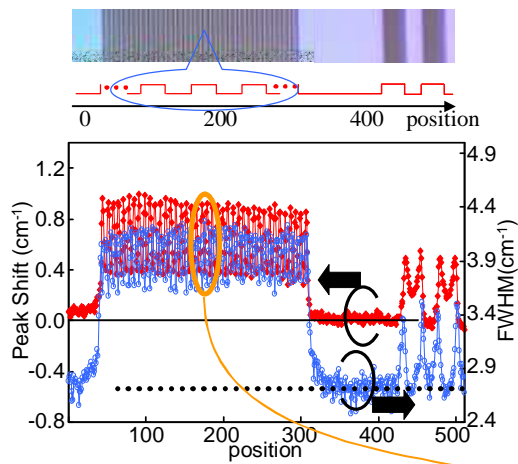

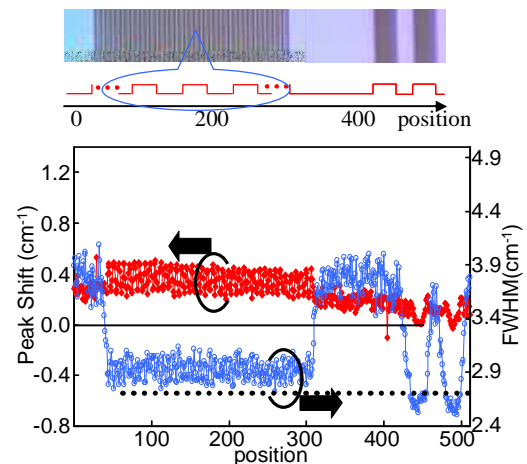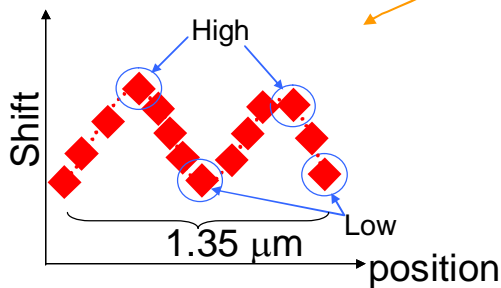**Fig. 18 Peak shift and FWHM of sample w/o argon implantation**

Fig. 19 Peak shift and FWHM of sample with argon implantation

L/S:1.0 μm/0.35 μm
depth:0.3 μm

	peak shift	strain	intensity
a	1.33 cm^{-1}	Comp.	78.1%
b	-0.74 cm^{-1}	Tens.	21.9%

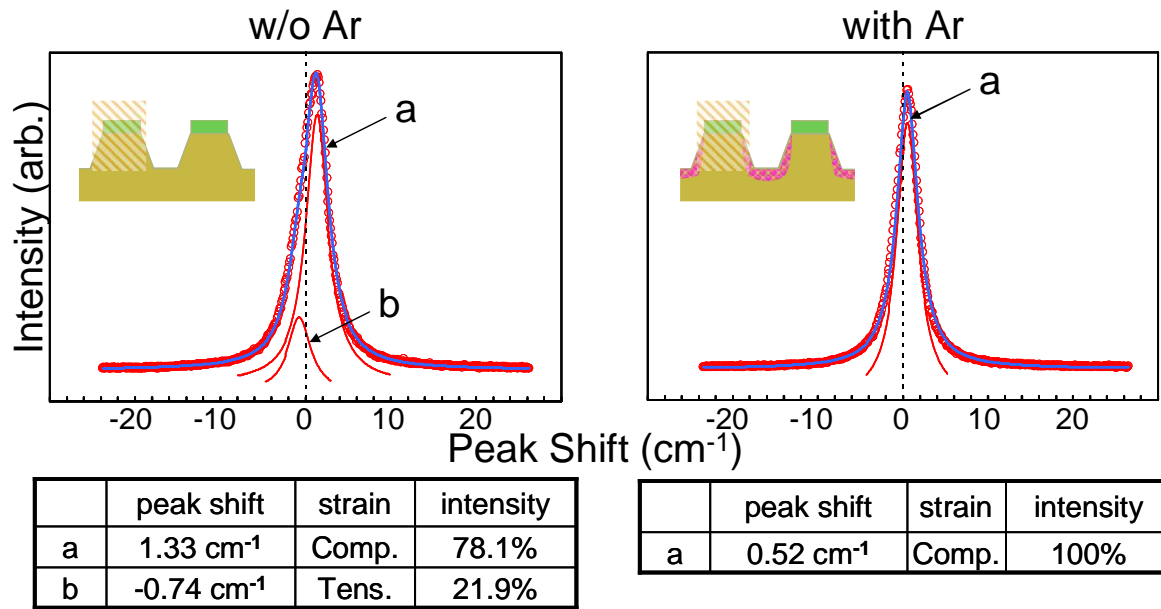|	peak shift	strain	intensity
a	0.52 cm^{-1}	Comp.	100%

**Fig. 20 Raman spectra
of w/o argon implantation**

**Fig. 21 Raman spectra
of with argon implantation**

Figure 22 shows simulation result of the same sample as in figure 20. In figure 22, points C, D, G, and H are in a highly compressive state. On the other hand, the points B, E, F, and I are in a tensile state. The two components in this figure, that is schematically shown D-E or F-G, can be attributed to these two states. This means that large contrast of strain can be induced in the pattered sample when silicon nitride stress film is attached on top of the line. By considering this simulation result, the compressive "a" peak in figure 20 can be attributed to top of the line (C, D, G, and H in figure 22) and the tensile "b" peak can be attributed to the edge (B, E, F, and I in figure 22), respectively. On the other hand, in the sample with Ar implantation, a single peak of compressive state is found in figure 21. It is considered that this "b" peak at the edge might move and coincide with the

"a" peak by Ar implantation. After Ar implantation and annealing, peak corresponding to tensile state might move to a compressive state due to residual Ar in Si. And at the same time, the stress induced by the silicon nitride film might be weakened by the implantation. The peak shift of Ar implantation thus seems to be decreased.
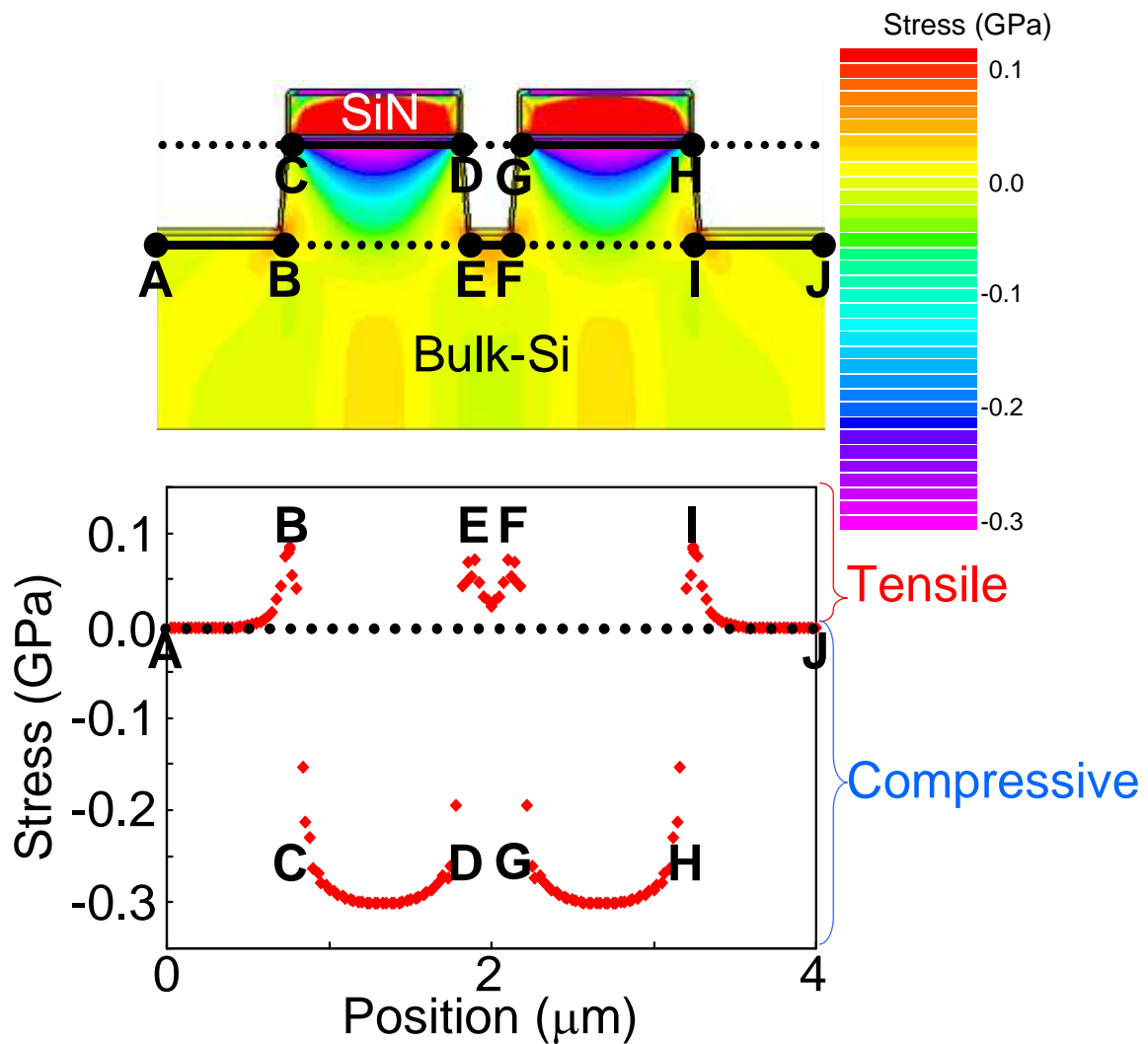

Fig. 22 Simulation of inducing stress to pattered sample by LP-SiN

3.2.2 Evaluation of LP-SiN film stress

In this section, the evaluation of stress in a 120 nm thick LP-SiN by a measurement of wafer bending is explained. Three SiN films, as-deposited state, with Ar implantation, and with Ar implantation and annealing, were prepared. Wafer bending and simulation results are shown in figure 23. After annealing at 950 ^{o}C for 25 min, stress of LP-SiN without Ar implantation did not change. On the other hand, after Ar implantation, stress of LP-SiN decreased to about 0.3 GPa. And after annealing, stress of the LP-SiN film with Ar implantation recovered to the stress level at about half of the initial state.

Figure 24 shows Raman shift and FWHM of the sample with Ar implantation without annealing (950 ^{o}C, 25 min). This sample corresponds to the state before annealing the sample in figure 19. Unlike the wafer bending results, the Raman results (in figures 19 and 24) seem to be similar with each other regardless of annealing. This means the behaviors in Figs. 19 and 24 cannot be explained only the change in by SiN film stress. The Raman data thus imply the effect of Ar incorporation.
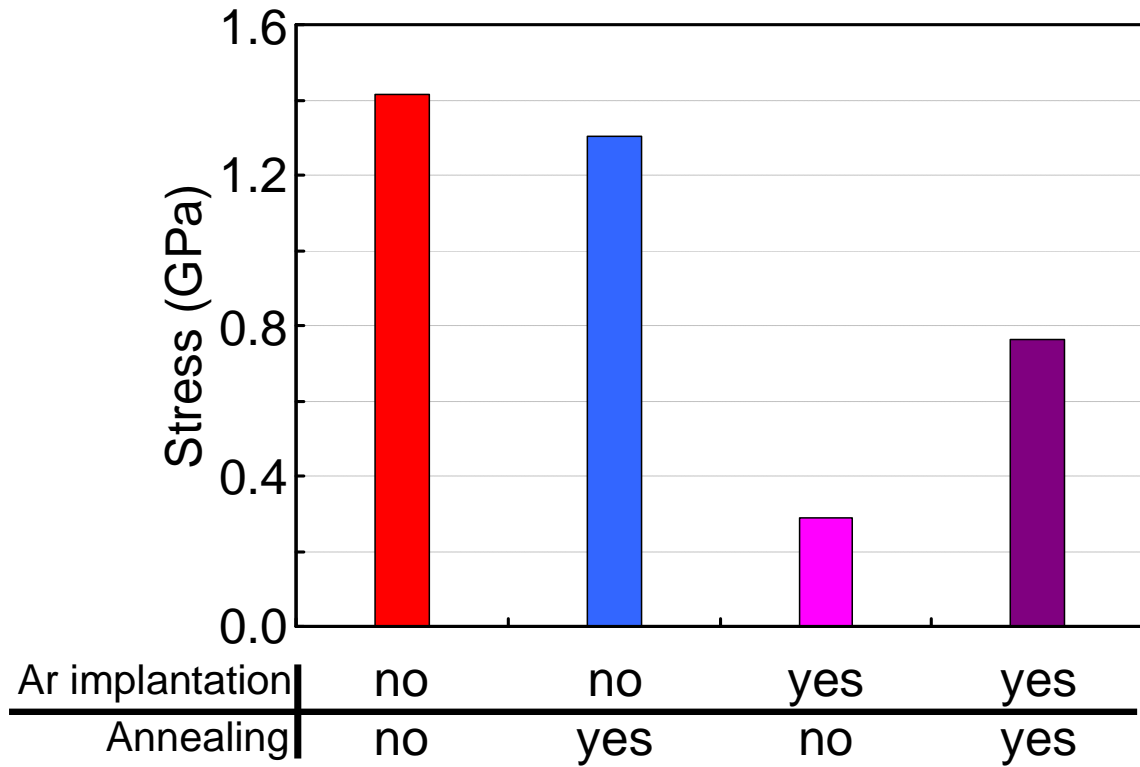
**Fig. 23 Variation of LP-SiN stress
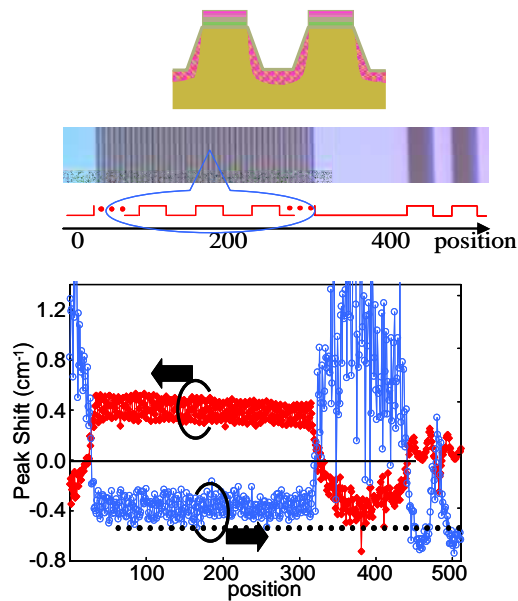caused by argon implantation and annealing.**

**Fig. 24 Peak shift and FWHM of samples
with argon implantation and without annealing**

3.3 Conclusion

In order to clarify the mechanism of SMT, as the first step of the investigation, the effect of Ar implantation and annealing of planar and line and space patterned silicon substrates with and without a stress film was examined.

I. After annealing at 950 $^{\circ}$C during 25 min, stress of Ar implanted silicon wafer was at -80 MPa that is caused by residual Ar atoms.

II. After forming line and space pattern, stress of the line region covered with the SiN film increased.

III. Stress decrease in the line and space pattern caused by Ar implantation and annealing can be attributed to both Ar incorporation in silicon and SiN stress decrease by Ar implantation.

IV. Result of wafer bending, stress of SiN film was weakened caused by Ar implantation before annealing, and stress of SiN film with Ar implantation recovered to the stress level at about half of the initial state. This result suggests that the stress variation in the line and space pattern is attributed to both the Ar incorporation and the SiN stress change.

V. For clarifying stress distribution of patterned sample, the analyzing

method was established by using micro Raman spectroscopy combined with signal integration and peak deconvolution.

3.4 Future works

In the next step, the effect of ion implantation and annealing should be investigated on the same structure as MOSFETs by using the stress measurement method that is established in this study.

The major factors of SMT are considered to be an introduction of heterogeneous atoms by implantation, poly-grain growth of gate electrode by annealing, and/or end-of-range-defect formation in a silicon substrate. And these phenomena can be enhanced by capping a stress film. Figure 25 shows structure of sample in the next investigation. The effect of gate electrode material (poly-grain effect), ion implantation on gate electrode and/or source/drain region, and capping film stress, can be investigated in these structures.

For the investigation on stress distribution of such samples with complex structures, the analysis method established in this study can be useful.
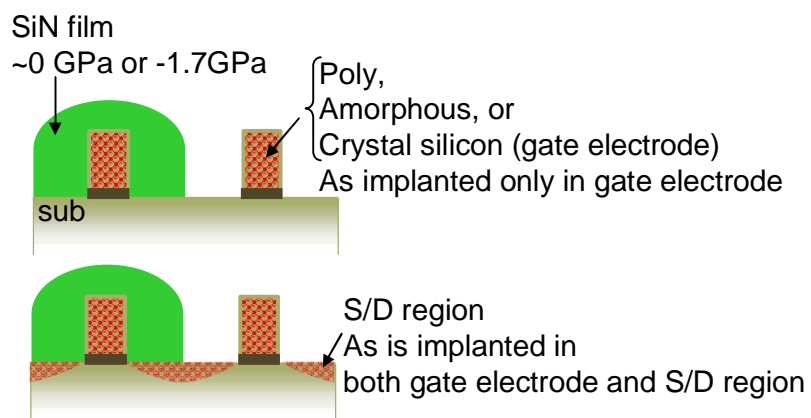
SiN film
~0 GPa or -1.7GPa

Poly,
Amorphous, or
Crystal silicon (gate electrode)
As implanted only in gate electrode

sub

S/D region
As is implanted in
both gate electrode and S/D region

Fig. 25 Structure of sample on next investigation

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IEDM; IEEE International Electron Devices Meeting

ISSCC; IEEE International Solid State Circuits Conference

VLSI; IEEE Symposia on VLSI Technology

SSDM; International Conference on Solid State Devices and Materials

J.S.A.P; The Japan Society of Applied Physics

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