Master thesis

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Electrical Characterization of W/HfO_2 MOSFET with La_2O_3 Incorporation

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【Chapter 1】

Introduction

1.1 Perspective on CMOS Technology

1.1.1 Back Ground of This Study

In recent years, our lives are becoming affluent with the global promotion of Information Technology (IT) as represented by computers, internets and cell-phones. As it is now, these are fundamental part of everyday life. These information equipments are realized by astonishing progress in silicon LSI (Large-Scale Integration) technology.

The performance of silicon LSI depends on the capability of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) that is a core part of LSI systems. In order to obtain high performance devises, it is necessary to miniaturize the MOSFET with the scaling method. The scaling method is based on reducing the device dimension in both lateral and vertical. The consensus scenario of how the device parameters are scaled for the next technology is provided in the International Technology Roadmap for Semiconductor (ITRS). A simple description of miniaturization with scaling factor of κ is shown in Figure 1.1 and Table 1.1. To gain κ times of the device performance, the physical device dimensions are reduced by k times, while the electrical parameters are increased by κ times.

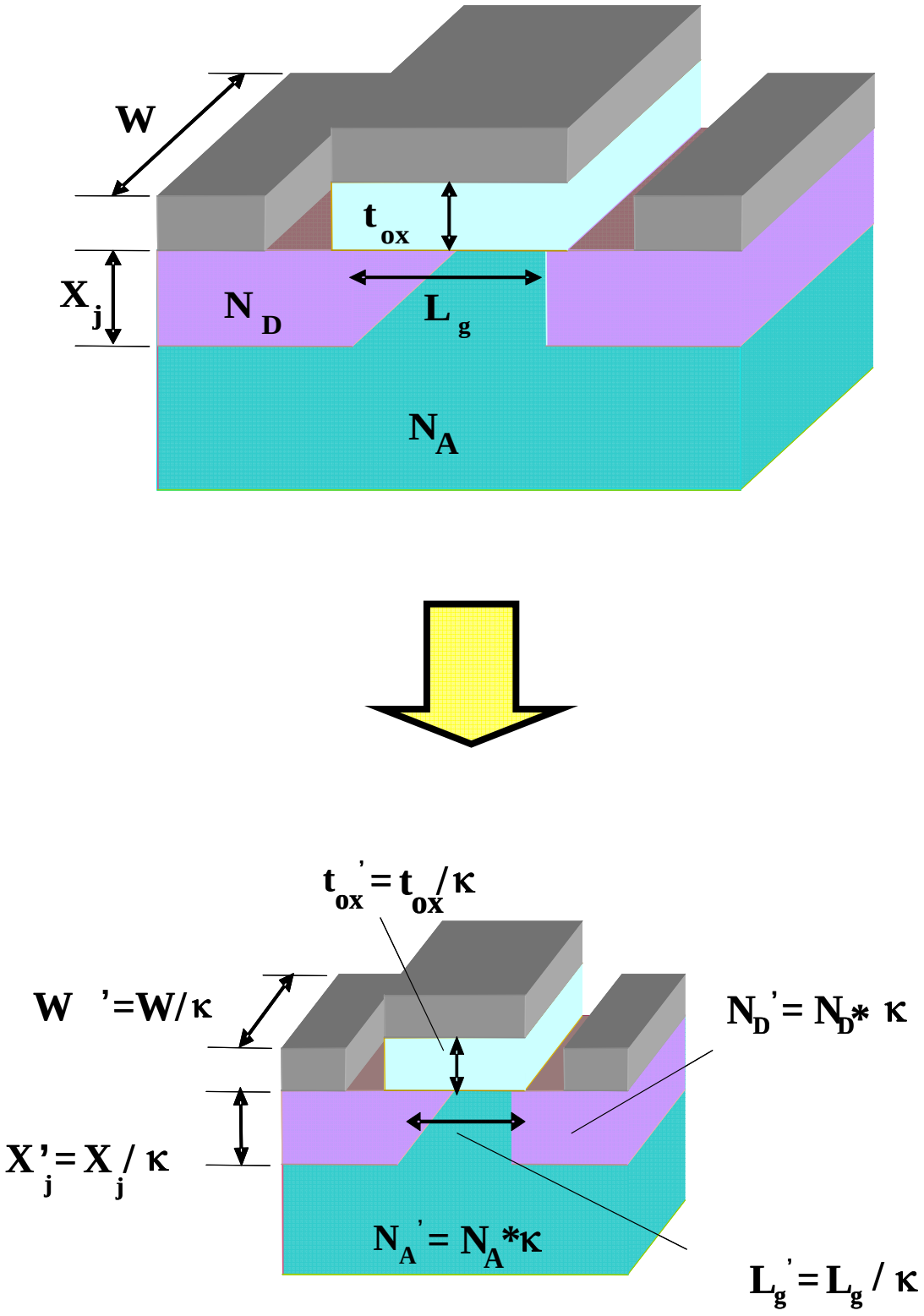

Figure 1.1 Scaling method

Table 1.1 Scaling of MOSFET by the scaling factor κ

Parameter	Inisial	Scaled
Channel Length	L	L/κ
Channel Width	W	W/κ
Total Device Area	A	A/κ^2
Gate Oxide Thickness	t_{ox}	t_{ox}/κ
Gate Capacitance	C_{ox}	$C_{ox}*\kappa$
Junction Depth	X_j	X_j/κ
Power Supply Voltage	V_{dd}	V_{dd}/κ
Threshold Voltage	V_{th}	V_{th}/κ
Doping Concentration	N_A	$N_A*\kappa$
	N_D	$N_D*\kappa$

1

1.1.2 The Limit of SiO_2 Gate Dielectric

Silicon dioxide film is the most common materials as the gate insulator film. However, a big hurdle is confronted to miniaturize the element size as in the past with keeping high performance and high integration. From ITRS 2007 up the date Table 1.2, Equivalent Oxide Thickness (EOT) will decrease the level below 1nm in near future [1]. On the other hand, the direct-tunneling leakage current is too increasing to be neglected as shown in figure 1.2. Therefore, SiO_2 gate insulator film must be replaced with an alternative material, which has high dielectric constant with leakage current as small as possible.

Table 1.2 ITRS 2007 up date

Year of Production	2008	2009	2010	2011	2014
Physical Gate length (nm)	22	20	18	16	11
EOT (nm)	0.9	0.75	0.65	0.55	0.5
Gate Leakage Current Density (A/cm^2)	9.09E+02	1.00E+03	1.11E+03	1.25E+03	1.82E+03

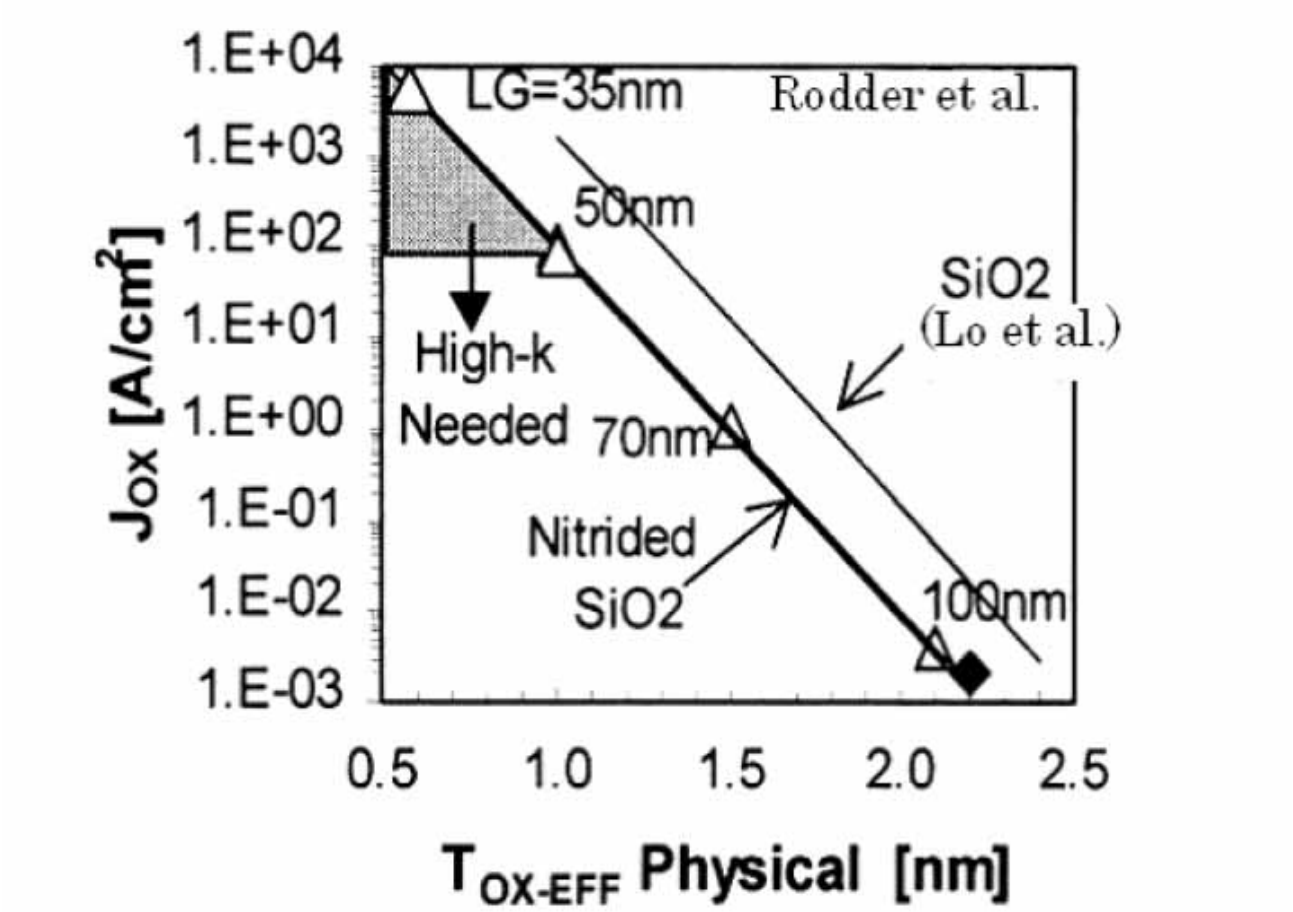

Figure 1.2 Relationship between gate leakage current and physical thickness of SiO2 film

1.1.3 Requirements in Gate Dielectrics

To decrease tunnel leakage current, high-k (high dielectric constant) materials have been attracted much attention. Replacing conventional SiO_2 with high-k materials for gate insulator, the required physical gate thickness for the same EOT becomes thicker, and thus, the leakage current could be suppressed. Figure 1.3 represents the schematic description of differences between the cases using SiO_2 and high-k material for gate

insulator.

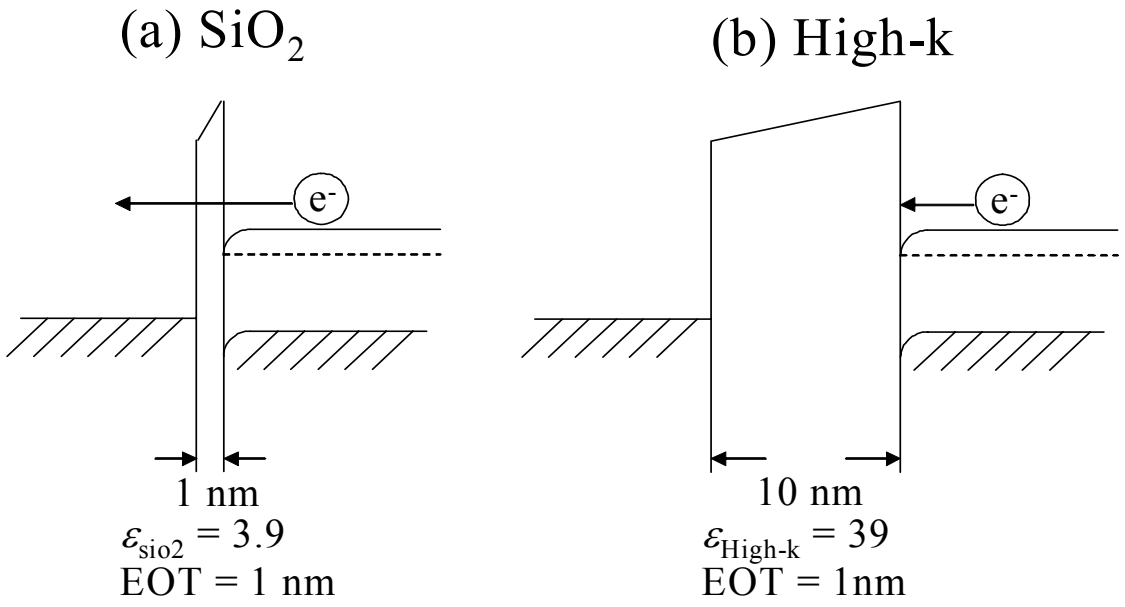

Figure 1.3 Schematic description of difference between the cases using (a) SiO_2 and (b) High-k for the gate insulator in the MOS structure.

The key guidelines for selecting an alternative gate dielectric material are high dielectric constant, large band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability. Among them, high dielectric constant and large band gap are the minimum required characteristics to suppress the gate leakage current. The direct-tunneling leakage current (J_{DT}) flow through a gate insulator film is determined by the tunneling probability of carrier. The tunneling probability of carrier (D_{DT}) is shown in below equation where physical thickness of insulator (d), electron effective mass in the gate insulator film (m^*) and barrier height of insulator (ϕ_b).

$$J_{DT} \propto D_{DT} \propto \exp\left\{-\frac{4\pi d\left(2m^{*}\phi_{b}\right)^{\frac{1}{2}}}{h}\right\} \qquad (1.1)$$

Relationship between physical thickness of SiO_2 (d_{EOT}) and physical thickness of high-k gate insulator (d) obtained by the same gate capacitance value (C) is shown in below equation where dielectric constant of SiO_2 (ε_{ox}) and high-k gate insulator ($\varepsilon_{high\text{-}k}$).

$$C = \frac{\varepsilon_{high-k}}{d} = \frac{\varepsilon_{ox}}{d_{EOT}} \qquad (1.2)$$

$$d = \frac{\varepsilon_{ox}}{\varepsilon_{high-k}} d_{EOT} \qquad (1.3)$$

Therefore, the gate leakage current can be suppressed by using high-k materials, which means that the physical thickness of high-k films can be thicken without changing EOT. In addition, the gate leakage current can also be suppressed by using large band gap materials.

1.1.4 High-k Gate Materials

The possible candidate of several metal oxides system for the use of gate dielectric materials is shown in white spaces of Table 1.3.

Table 1.3 Candidate of metal oxides that has possibility to be used as high-k gate insulator.

● H	●=Not a solid at 1000 K ○= Radioactive ①=Failed reaction 1: $Si + MO_x \rightarrow M + SiO_2$ ②=Failed reaction 2: $Si + MO_x \rightarrow MSi_x + SiO_2$ ⑥=Failed reaction 6: $Si + MO_x \rightarrow M + MSi_xO_y$															● He
Li	Be											● B	● C	● N	● O	● F	● Ne
① Na	Mg											Al	Si	● P	● S	● Cl	● Ar
K	Ca	Sc	② Ti	① V	① Cr	① Mn	① Fc	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr
● Rh	Sr	Y	Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe
● Cs	⑥ Ba	R	Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn
○ Fr	○ Ra	A	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt									

R	La	Ce	Pr	Nd	○ Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
A	○ Ac	○ Th	○ Pa	○ U	○ Np	○ Pu	○ Am	○ Cm	○ Bk	○ Cf	○ Es	○ Fm	○ Md	○ No	○ Lr

Among the candidate of high-k materials, Hf-based materials are the most promising candidate of them. As shown in Figure 1.4, many papers on high-k materials are submitted in the primary conferences up to 2002. However, from 2003 to now, the candidate of high-k materials have narrowed down to Hf-based materials. Therefore, Hf oxides (HfO_2) and Hf-based silicates or nitrides (HfSiON), with dielectric constants of 25 and 10 to 15 respectively, are among the promising materials for the 65 or 45-nm-technology nodes.

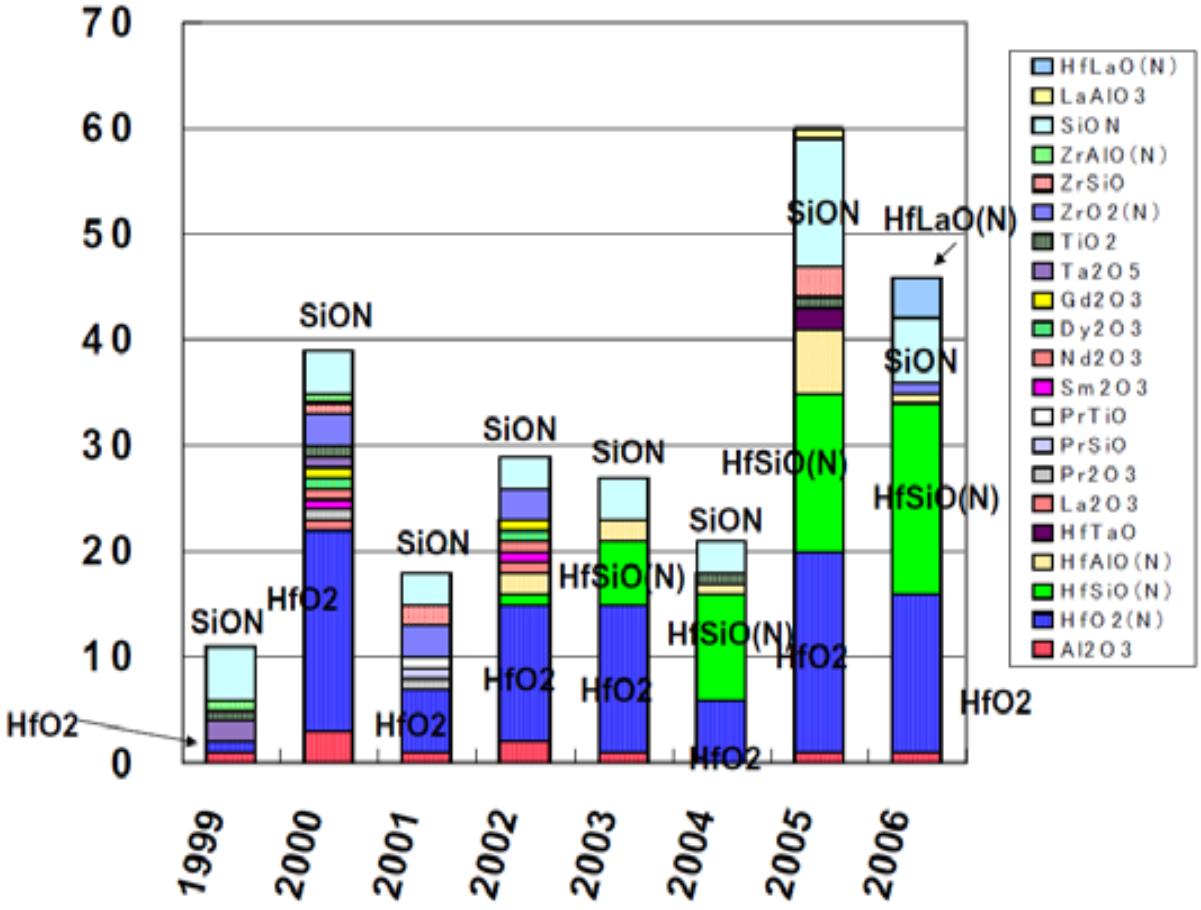

Figure 1.4 Reported High-k materials

1.2 Low-Frequency Noise in MOSFET

The CMOS technology, that possesses the advantage of low cost, high integration, and low power, is finding more and more important applications in the area of mixed mode and RF ICs. As compared with bipolar transistors, CMOS devices exhibit large noise, especially in the low-frequency (LF) region where flicker noise is dominant [2]. Flicker noise will affect the signal-to-noise ratio in operational amplifiers and analog/digital and digital/analog converters.

Low frequency noise have drawn much attention for the analog circuit designers since it is a major concern in analogue applications, but low frequency noise characterization is also a useful tool for the investigation of traps inside the gate dielectric. Accurate MOSFET noise models are therefore of high relevance for CMOS circuit designers as well as semiconductor manufacturers and device designers need to be concerned about reducing the *1/f* noise in the MOSFETs

1.3 Purpose of This Study

Hf-based-oxides have been used to replace SiO_2 gate insulator for advanced CMOS technologies and have been the most likely candidate to achieve EOT around 1nm. But, Hf-based-oxides require thin layer of SiO_2 or SiON to improve the relatively high interface state density and effective carrier mobility. Because the thin layer will increase the EOT, it reaches critical limit in terms of further scaling. Consequently, new process or additional material incorporation is strongly required. Recently, La_2O_3 has attracted

much attention as it has wide bandgap of 5.5eV and high dielectric constant of 24 with fairly nice interface property. Also, La_2O_3 has been used to control the threshold voltage to negative direction [3]. In this work, we studied the effect of La_2O_3 incorporation underneath the HfO_2 layer on electrical properties of MOSFETs.

【Chapter 2】

Theoretical Review

2.1 Fundamental Noise Mechanisms

2.1.1 Introduction

Currents and voltages in an electronic circuit are perturbed from their given values due to interference of noise. The desired signal becomes difficult to distinguish when the noise power is significant in relation to the signal power, why noise is unwanted in electronic. One could categorize noise originating from (i) external sources, for example adjacent circuits, AC power lines, radio transmitters disturbing the circuit of interest due to electrostatic and electromagnetic coupling, and (ii) internal random fluctuations in physical processes governing the electron transport in a medium..

The external disturbances can often be eliminated by appropriate shielding, filtering and layout design of the circuits. On the other hand, internal random fluctuations cannot be eliminated, but it is possible to reduce it by proper design of the devices and circuits.

2.1.2 Noise Definition

Figure 2.1 illustrates how an electronic signal fluctuates randomly due to noise. The current through a device can be written as

$$I(t) = \bar{I} + i_n(t) \qquad (2.1)$$

Where $\bar{I}$ is the average bias current and $i_n(t)$ is a randomly fluctuating current. The value of i_n is random at any point in time and cannot be predicted. Instead we

describe the noise with averages, for example the average of i_n measured over a long time should always equal zero. The study of noise is built on the mathematical methods from probability theory, which allows us to define appropriate averages for the random variables we are dealing with. A common and powerful method to characterize and describe noise is by converting the problem from the time domain to the frequency domain by Fourier transformation.

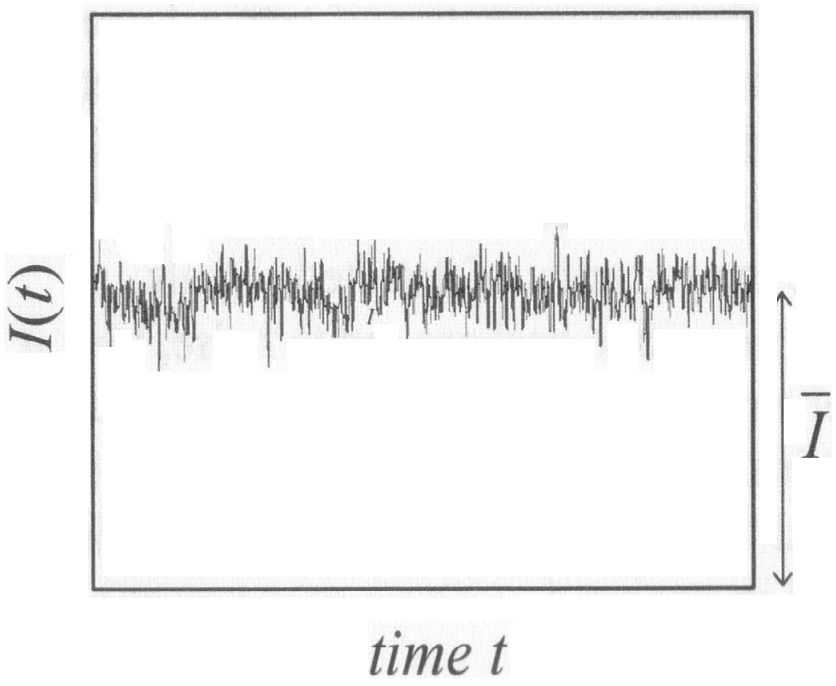

Figure 2.1 A typical noise waveform is illustrated [2].

2.1.3 Mathematical Treatment

Let us consider an electronic circuit and assume for the time being that we have a large number of identical copies of this circuit, an ensemble. At a chosen location in the circuit at a certain point in time there is a probability dP that the wanted signal will be disturbed by with an amplitude in the interval $[X, X+dX]$, where X is a random variable. One can define a probability density function $f(X)$ of X and write

$$dP = f(X)dX \qquad (2.2)$$

The probability density function should be normalized so that the integration over all allowed values of X yields 1.

For random variables, several ensemble averages are defined; mean value, variance, autocorrelation function, power spectral density etc. While one cannot know the exact outcome of random event, these averages give us adequate information about it. The mean value and variance are defined below in Eqs. (2.3) and (2.4), respectively:

$$\overline{X} = \int_{-\infty}^{+\infty} Xf(X) \qquad (2.3)$$

$$\operatorname{var} X = \int_{-\infty}^{+\infty} (X - \overline{X})^2 f(X)dX = \overline{X^2} - \overline{(X)}^2 \qquad (2.4)$$

The ensemble averages can be calculated when the probability density function is known. Practically all fluctuating currents and voltages in electrical devices follow the

normal distribution due to the central limit theorem stating that the sum of a large number of independent random variables has normal distribution. One important exception though is the switching of the signal between two levels, random-telegraph-signal noise, which is a Poisson process. The probability density function for the normal distribution is given as

$$f(X) = \frac{1}{\alpha\sqrt{2\pi}} \exp\left[-\frac{(X-m)^2}{2\alpha^2} \right] \qquad (2.5)$$

Where $\overline{X} = m$ and var $X = \alpha^2$ if X has a normal distribution.

However, the exact probability density function for the noise is seldom known. But, the time averages equal the ensemble averages for certain random processes. That is, the distribution for one ensemble element over time is equal to the distribution over the whole ensemble at a chosen point in time. Such processes are called stationary.

Currents and voltages are readily measured over time and used to gain information about the noise. The time average of the noise voltage or noise current just equal zero if integrated long enough and provides no interesting information; instead squared quantities are used to describe the noise. One such squared quantity is the power spectral density $S(f)$ which is given from the autocorrelation function $R(s)$ according to the Wiener-Khintchine theorem

$$S_x(f) = 4\int_0^\infty R(s)\cos(2\pi fs)ds \qquad (2.6)$$

$S(x)$ is a Fourier transformation of R(s), which is given by

$$R(s) = \overline{X(t)X(t+s)} = \lim_{T\to\infty}\frac{1}{T}\int_0^T X(t)X(t+s)dt \qquad (2.7)$$

or $$R(s) = \int_0^\infty S_x(f)\cos(2\pi fs)df \qquad (2.8)$$

Obviously, if $s = 0$ one obtains the variance or noise "power"

$$\overline{X^2(t)} = \int_0^\infty S_x(f)df = \lim_{T\to\infty}\frac{1}{T}\int_0^T X^2(t)dt \qquad (2.9)$$

Noise with a constant $S(f)$ for all frequency is said to be white. It is usually observed that the noise PSD is dependent on frequency at low frequencies, and becomes white thereafter. The corner frequency between frequency dependent noise and white noise is typically from a few Hz up to the MHz range and depends on the type and size of the device, bias conditions etc. A schematic diagram of the PSDs for the excess noise at low frequency, low frequency noise, and the white noise is shown Figure 2.2. The low-frequency noise may consist of superimposed $1/f$ noise and generation-recombination (g-r) noise.

Both white noise and low-frequency noise are important to consider in electronic circuits, their relative importance depends on the type of circuit and its application. The physical mechanisms behind the white noise sources are well known and the white noise level can usually be accurately predicted in electronic circuits. However, the origin of the low-frequency noise still raises many questions.

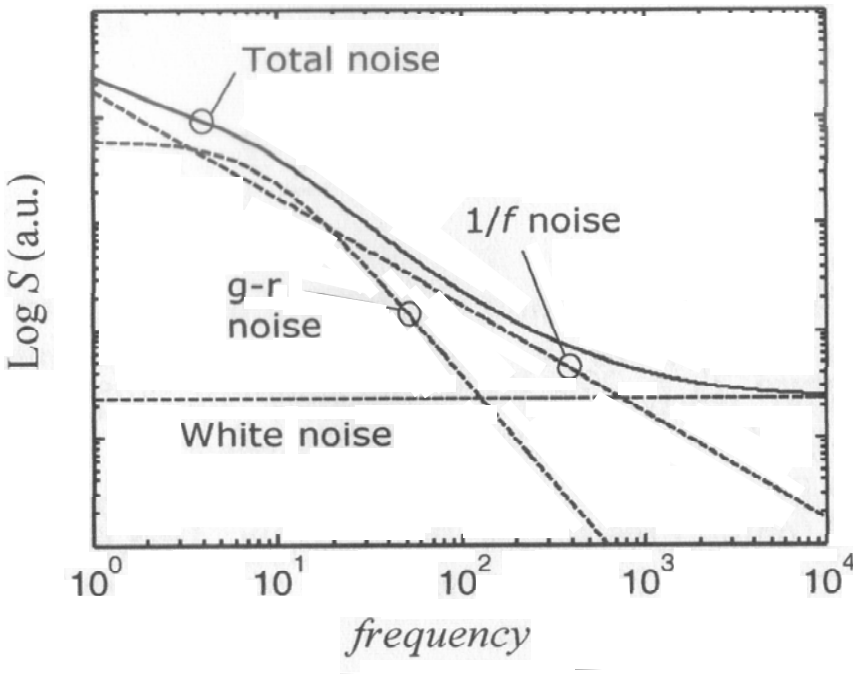

Figure 2.2 The PSD for low-frequency noise and white noise plotted vs. frequency. The excess noise above the white noise floor is called low-frequency noise and may consist of 1/*f* noise or generation-recombination (g-r) noise [2].

2.1.4 Fundamental Noise Sources

It is noted that there seem to be noise sources, thermal noise, shot noise, generation-recombination noise, random-telegraph-signal (RTS) noise and 1/*f* noise in semiconductor device.

(i) Thermal noise

The Thermal noise stems from the random thermal motion of electrons in a material.

Each time an electron is scattered, the velocity of the electron is randomized. Instantly, there could be more electrons moving in a certain direction than electrons moving in the other directions and a small net current is flowing. This current fluctuates in strength and direction, but the average over time is always zero. If a piece of material with resistance R and temperature T is considered, the PSD of the thermal noise current is found to be

$$S_I = \frac{4kT}{R} \qquad (2.10)$$

The thermal noise exists in every resistor and resistive part of a device and sets a lower limit on the noise in an electric circuit.

(ⅱ) Shot noise

The current flowing across a potential barrier, like the pn-junction, is not continuous due to the discrete nature of the electronic charges. The current across a barrier is given by the number of carriers, each carrying the charge q, flowing through the barrier during a period of time. A shot noise current is generated when the electrons cross the barrier independently and at random. The current fluctuates with a PSD

$$S_I = 2qI \qquad (2.11)$$

(ⅲ) Generation-recombination (g-r) noise

Generation-recombination (g-r) noise in semiconductors originates from traps that randomly capture and emit carriers, thereby causing fluctuations in the number of carriers available for current transport. If carriers are trapped at some critical spots, the

trapped charge can also induce fluctuations in the carrier mobility, diffusion coefficient, electric field, barrier height, space charge region width etc. The PSD of the fluctuations in the number of carriers is found to be

$$S_N(f) = 4\overline{\Delta N^2}\frac{\tau}{1+\tau^2\omega^2} \qquad (2.12)$$

Here, τ is the time constant of the transitions. The shape of the spectrum given by (2.12) is called a Lorentzian and is illustrated in Figure 2.3.

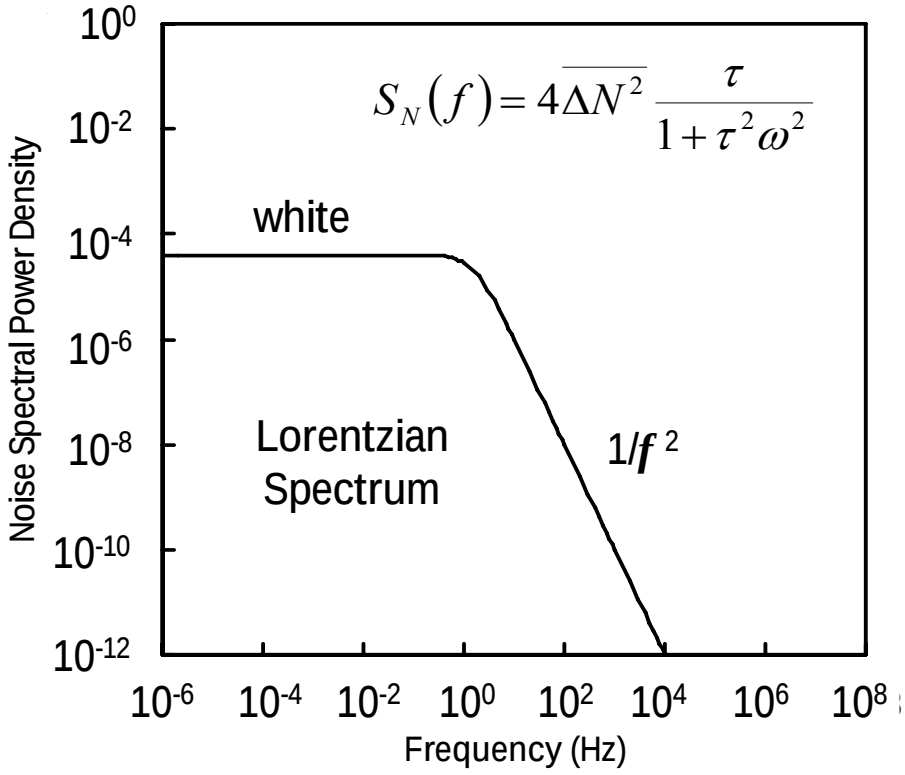

Figure 2.3 A Lorentzians shaped for the RTS

(ⅳ) Random-Telegraph-Signal (RTS) noise

A special case of g-r noise is the RTS noise, which is displayed as discrete switching events in the time domain. If only a few traps are involved, the current can switch between two or more states resembling a RTS waveform due to random trapping and detrapping of carriers. For two-level pulses with equal height ⊿I and Poisson distributed time durations in the lower state τ_i and in the higher state τ_h, the PSD of the current fluctuations is derived as

$$S_I(f) = \frac{4(\triangle I)^2}{(\tau_i + \tau_h)\left[(1/\tau_i + 1/\tau_h)^2 + (2\pi f)^2\right]} \qquad (2.13)$$

The PSD for the RTS noise and the g-r noise are both of the Lorentzian type.

(ⅴ) 1/*f* noise

1/*f* noise is the common name for fluctuations with a PSD proportional to $1/f^{\gamma}$ with γ close to 1, usually in the range 0.7-1.3. The PSD for 1/*f* noise takes the general form

$$S_I = \frac{K \cdot \mathrm{I}^{\beta}}{f^{\gamma}} \qquad (2.14)$$

Where K is a constant and β is a current exponent. 1/*f* fluctuations in the conductance have been observed in the low-frequency part of the spectrum (10^{-5} to 10^{7} Hz) in most conducting materials and a wide variety of semiconductor devices.

G-r noise from a large umber of traps (number fluctuations) can produce 1/*f* noise. An example is given in Figure 2.4 where g-r noise from four individual traps with different

time constants adds up to a $1/f^{\gamma}$ spectrum with γ close to 1.

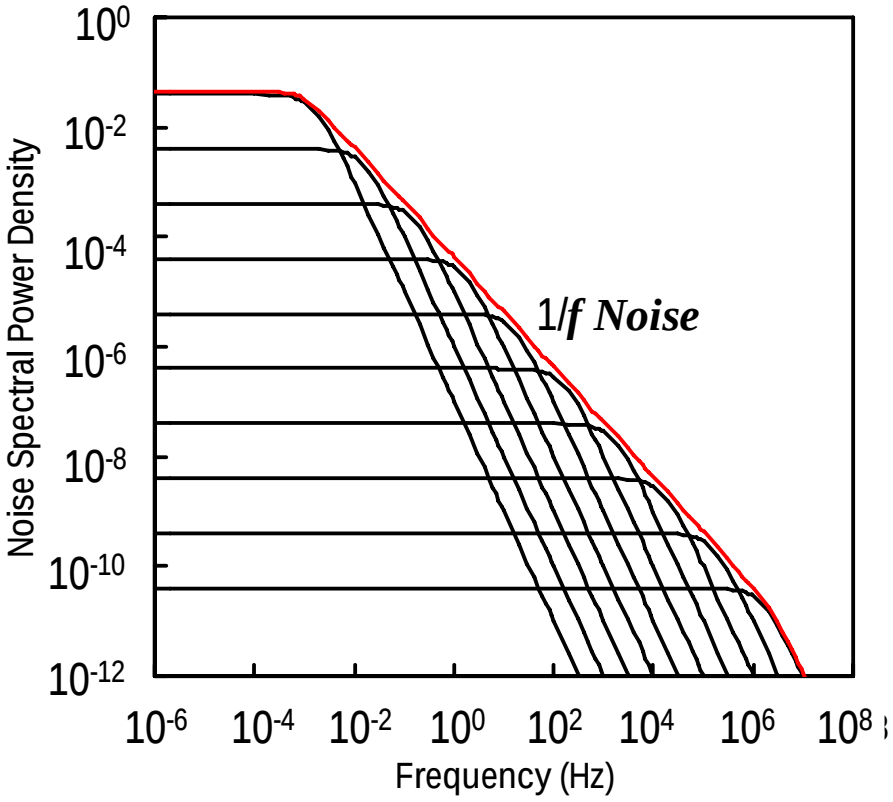

Figure 2.4 Superposition of 4 Lorentzians giving a total spectrum that approximately exhibits a $1/f$ dependence over several decades of frequency.

2.2 Low-Frequency Noise in MOSFET

2.2.1 Origin of 1/*f* noise in MOSFET

The origin of the 1/*f* noise in MOSFETs has been debated for several decades [4], whether number fluctuation noise due to traps in the gate oxide or bulk mobility fluctuations dominate the 1/*f* noise [5]. The drain current in a MOSFET is confined to a narrow surface channel under the gate oxide. The current transport is therefore sensitive to traps present at interface. Number fluctuation is generally believed to be the dominant 1/*f* noise mechanism in n-channel MOSFETs and commonly also in pMOSFETs [6]. However, the mobility fluctuation noise model tends to explain the 1/*f* noise in pMOSFETs [7]. In spite of extensive efforts to identify the physical origins of the current fluctuations, a consistent picture of the noise-generation mechanism has not yet emerged.

Generally the measured noise power in MOSFETs has more complicated dependence on the gate bias and oxide thickness than the number or mobility fluctuation theory predicts. Some authors have combined the number and mobility fluctuation models in order to explain their data.

2.2.2 Number Fluctuation Noise

In 1957, McWorther presented a 1/*f* noise model based on quantum mechanical tunneling transitions of electrons between the channel and traps in the gate oxide. The tunneling time varies exponentially with distance, thus the required distribution of time constants to produce 1/*f* noise is obtain a trap density that is uniform in both energy and

distance from the channel interface [8]. The physical mechanism behind the number fluctuation 1/*f* noise in MOSFETs is schematically illustrated in Figure 2.4. The oxide traps dynamically exchange carriers with the channel causing a fluctuation in the surface potential, giving rise to fluctuations in the inversion charge density.

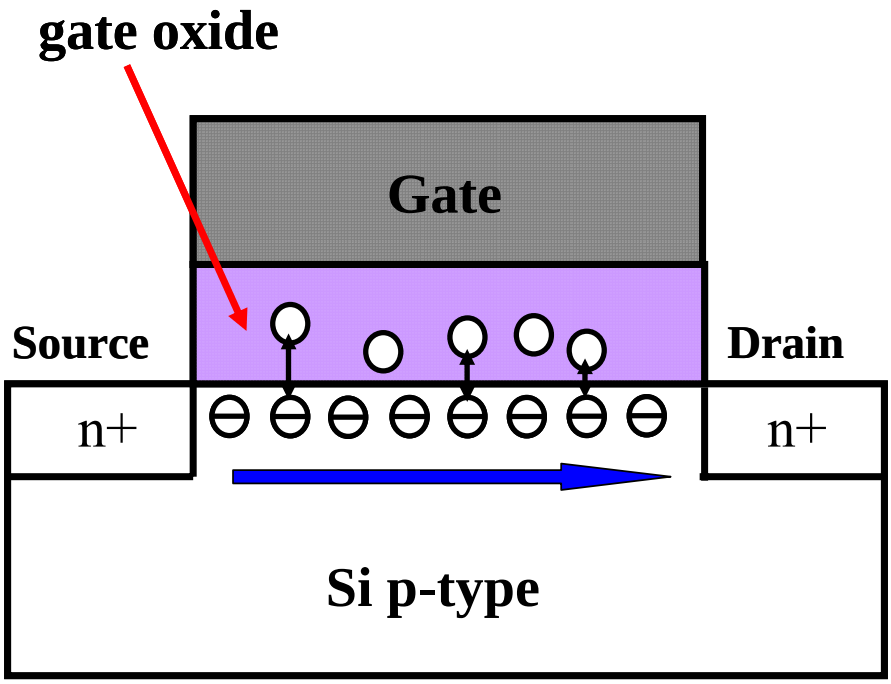

Figure 2.4 Schematic illustration of electrons in the channel of a MOSFET moving in and out of traps, giving rise to fluctuations in the inversion charge density and thereby the drain current. The carrier mobility is also affected by the oxide charge; mobility fluctuations correlated to the number fluctuations are therefore generated which may increase pr decrease the total low-frequency noise.

Mathematically it can be shown that a uniform spatial distribution of oxide traps near the interface will give raise to a distribution of time constants which add up to yield the 1/*f* noise spectrum. For a uniform oxide trap distribution in the energy gap, the theory predicts an input referred noise power which is independent of the effective gate voltage, $V_g - V_{th}$, but inversely proportional to the square of the gate capacitance, C_{ox}. The number fluctuation model is supported by the widely observed correlation between the flicker noise power and interface trap density [9].

2.2.3 Mobility Fluctuation Noise

The mobility fluctuation theory [10] considers the flicker noise as a result of the fluctuation in bulk mobility based on Hooge's empirical relation for the spectral density of flicker noise in a homogeneous sample. It was modeled base on a number of experiments in metal thin film. He found that the noise in film conductors could be characterized by

$$\frac{S^2}{I^2} = \frac{\alpha_{\mathrm{H}}}{fN_{total}} \qquad (2.15)$$

where α_H is a dimensionless Hooge's empirical parameter and I is the mean current flowing through the sample, S_I is the spectral density of the noise in the current, N_{total} is the total number of free carriers in the sample. It has been proposed that the fluctuation of bulk mobility in MOSFETs is induced by fluctuations in phonon population through phonon scattering [11]. Later, Hooge found that dimensionless α_H

parameter is due to electron phonon scattering that is related to the crystalline quality of film conductors. Hooge's theory gives a pure $1/f$ spectrum in all frequency range.

【Chapter 3】

Device Fabrication and Characterization Methods

3.1 Fabrication Process for N-MOSFETs

The fabrication process flow is shown in Figure 3.1 HfO_2 gated N-channel MOSFET (W/L=50μm/2.5μm) with La_2O_3 incorporation was fabricated on a p-Si (100) with LOCOS isolation. The source and drain were pre-formed prior to the high-k deposition. No interfacial layer was intentionally formed before high-k deposition. 2nm-thichness of HfO_2 and La_2O_3 with thickness 4nm were deposited by e-beam evaporation in an ultra high vacuum chamber. Tungsten metal electrode was deposited on top of the high-ks by sputtering. Annealing temperature was performed in forming gas ambient at 500℃ for 30 min. Al back side electrode was formed afterwards.

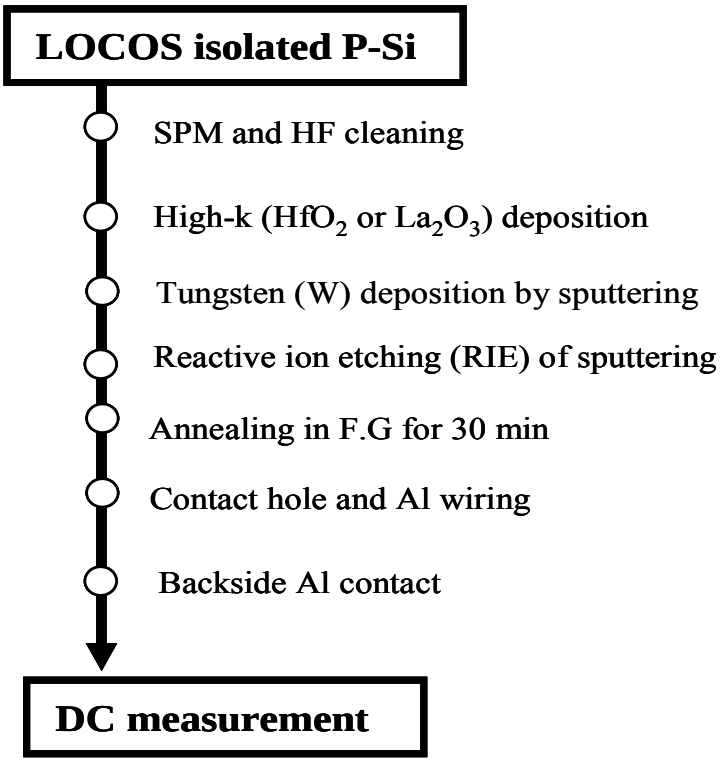

Figure 3.1 Fabrication process flow of high-k gated n-MOSFET

3.2 Characterization Methods of MOSFETs

3.2.1 Threshold Voltage (V_{th}) Measurement

One of the common threshold voltage (V_{th}) measurements is the linear extrapolation method with the drain voltage of typically 50-100 (mV) to ensure operation in the linear MOSFET region. The threshold voltage is determined from the extrapolated or intercepts gate voltage V_{GSi} by

$$V_T = V_{GSi} - \frac{V_{DS}}{2} \qquad (3.1)$$

where

$$V_{GSi} = V_{GS,\max} - \frac{I_{D,\max}}{g_{m,\max}} \qquad (3.2)$$

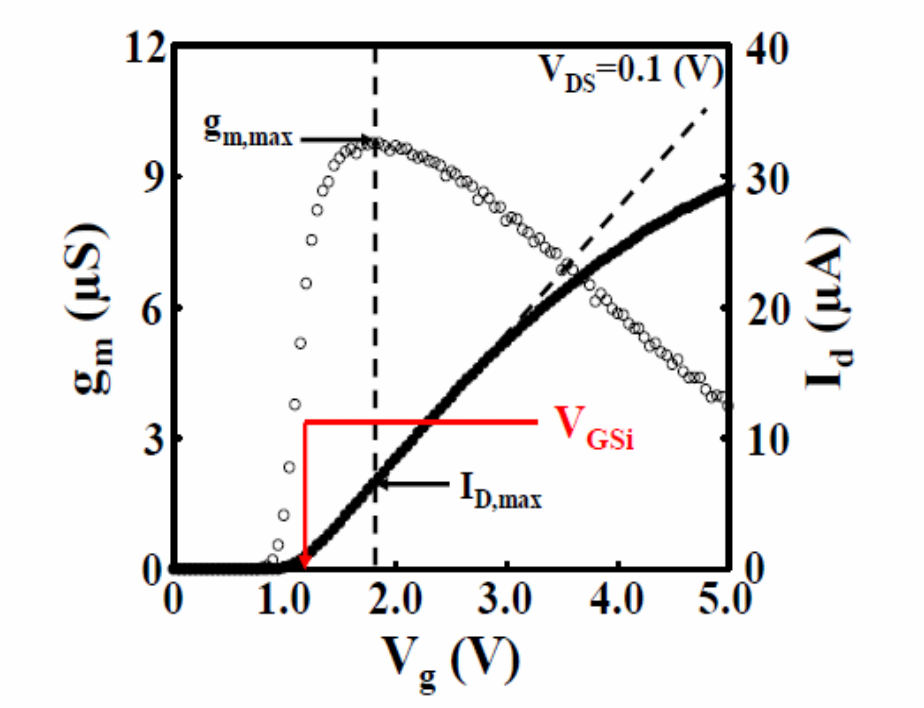

Figure 3.2 The linear extrapolation method

3.2.2 Subthreshold Slope (S.S) Measurement

The subthreshold slope (*S.S.*) is calculated from below equation.

$$S.S. = \left(\frac{d\left(\log_{10} I_{ds}\right)}{dV_g} \right)^{-1} \qquad (3.3)$$

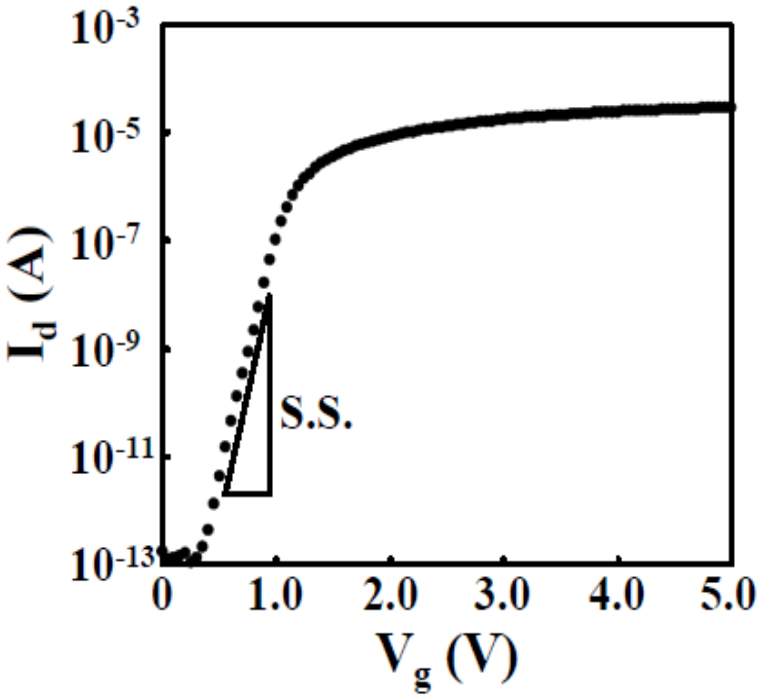

Figure 3.3 The subthreshold slope calculated from I_d-V_g characteristic

3.2.3 Split *C-V* Method

One of the most common measurements to obtain the effective mobility (μ_{eff}) is the split C-V method, which combines gate-to-channel capacitance (C_{gc}) and gate-to-bulk capacitance (C_{gb}). μ_{eff} is obtained from below equation,

$$\mu_{eff} = \frac{g_d L}{W Q_n} \qquad (3.4)$$

where the drain conductance g_d and the inversion charge density Q_n are defined as

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=constant} \qquad (3.5)$$

$$Q_n = \int_{V_{FB}}^{V_{GS}} C_{gc} dV_{GS}. \qquad (3.6)$$

E_{eff} is obtained from below equation,

$$E_{eff} = \frac{1}{\varepsilon_{Si}}\left(|Q_d| + |Q_n|\right) \qquad (3.7)$$

where ε_{Si}=11.9 and the depletion charge density Q_d are defined as

$$Q_d = \int_{V_{FB}}^{V_{th}} C_{gb} dV_{GS} \qquad (3.8)$$

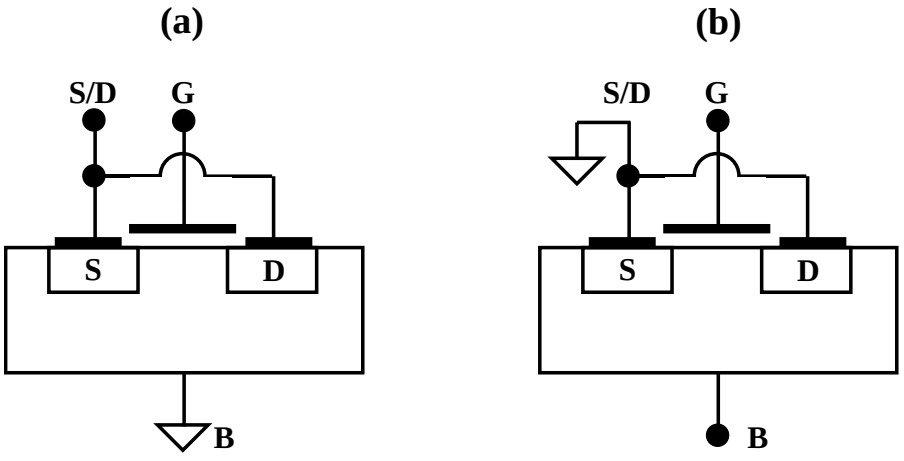

Figure 3.4 Configuration for (a) gate-to-channel, (b) gate-to-substrate capacitance measurements

3.3 Measurement Technique of Low-Frequency Noise

3.3 1 1/*f* noise measurement system

The noise signals of high quality devices are usually very small. To measure such signals, nearly noiseless and high sensitivity appliances are highly required. Figure 3.5 shows schematic diagram for 1/*f* noise measurement system. The grounding is very important to reject the outside signal interferences. Since long and very long wave radio frequencies, it is recommended to measure the low frequency noise under a shielded-chamber. The 1/*f* noise measurement system is utilized with several equipments, i.e., DC monitor, low-noise DC source, signal analyzer, low-noise amplifier, wafer probe, 1/*f* noise interface unit, and ground unit. The first tree equipments are automatically controlled with Personal Computer (PC) via *GPIB* network interface. 1/*f* noise measurement program running under Agilent VEE (Visual Engineering Environment) software is used to manipulate the complexity of noise measurements.

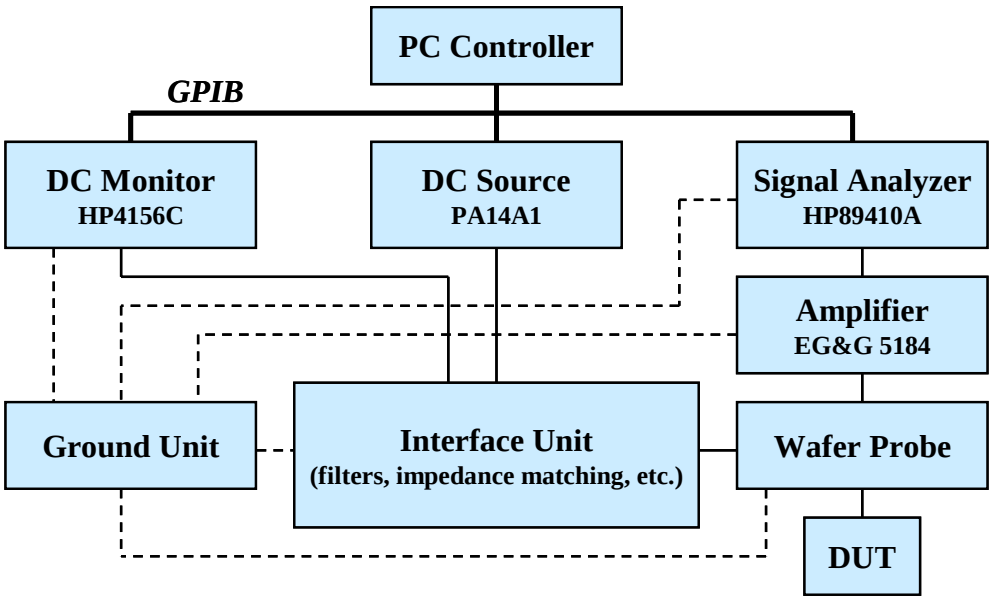

Figure 3.5 Diagram for 1/*f* noise measurement system

3.3 2 Vector Signal Analyzer

The noise power density of the device under test (DUT) is measured and analyzed with signal analyzer. In this experiment, we use Agilent HP89410A vector signal analyzer (VSA) as its photograph shown Fig. 3.6. To measure the noise signal, this equipment modulates signal in vector forms. We may measure noise signal as low as –160 dBv = 10 nVrms at 1kHz directly without pre-amplifier by setting the sensitivity of this equipment into the highest level. This equipment supports signal measurements over DC to 10 MHz frequency range, however, the 1/*f* noise measurement system allows 10 Hz to 10 MHz for measurement without pre-amplifier or 10 Hz to 100 kHz for measurement with amplifier.

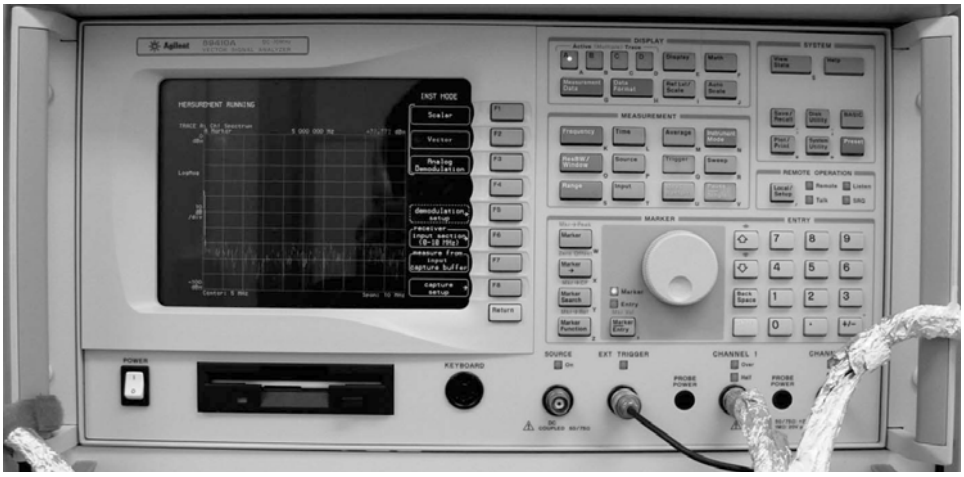

Figure 3.6 High sensitivity Agilent HP89410A vector signal analyzer (VSA)

3.3.3 Ultra-Low Noise DC Source

In 1/*f* noise measurements, DUT must be operated properly by DC biasing. Shibasoku PA14A1 ultra-low noise DC source shown in Figure 3.7 is used in this experiment to satisfy the requirements. This equipment is accommodated with 2 channels with sufficiently low enough noise, i.e., CH 1: -126 dBv = 0.5 μVrms and CH 2: -132 dBv = 0.5 μVrms at 1 kHz. Furthermore, these noise levels can be suppressed with RC Low-Pass (LP) filters that is utilized inside the 1/*f* noise interface unit. In case of nMISFET device, it is recommended to use CH 1 for biasing the gate and CH 2 for the drain, since the CH 2 has a half lower than CH 1 in noise power and the 1/*f* noise signal measured from the drain terminal. It is noted that PA14A1 DC source can not inverse its polarity and it should be done manually through the interface unit.

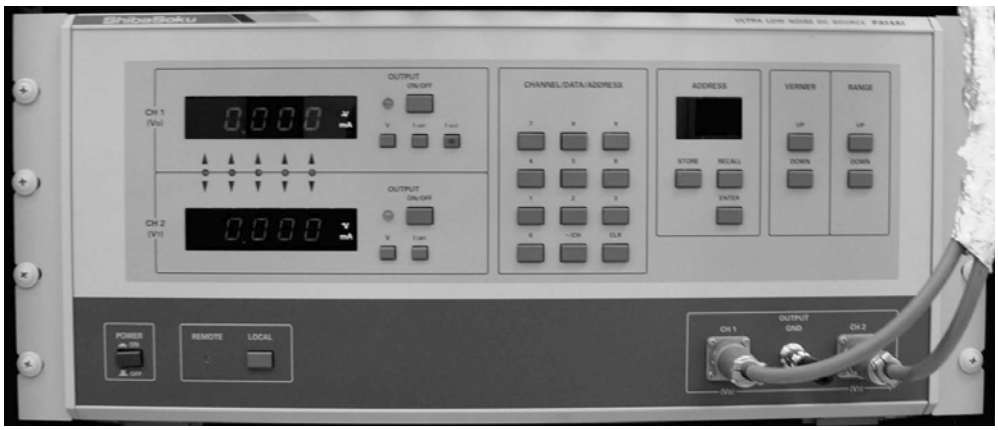

Figure 3.7 Shibasoku PA14A1 ultra-low noise DC source photograph

3.3.4 Ultra-Low Noise Pre-Amplifier

It is difficult to measure 1/*f* noise of high quality devices, since they have very low noise signals. To facilitate measurement of a very low noise, high gain ultra-low noise pre-amplifier is required to increase the measurement sensitivity. In this system, Pelkin Elmer EG&G 5184 ultra-low noise pre-amplifier is used to obtain noise floor as low as –178 dBv = 1.2 nVrms at 1 kHz as shown in Figure 3.8. This noise floor can be measured by shorting the pre-amplifier input with 50 Ω terminal stubs. As this equipment has flat gain of 60 dB along frequency range of 3 Hz to 300 kHz, it covers the supported frequency range of 10 Hz to 100 kHz of noise measurement. This pre-amplifier can be powered with either AC line or dry cell batteries. It is recommended to unplug the connector to the AC line, since it directly couple the AC line signal to the system.

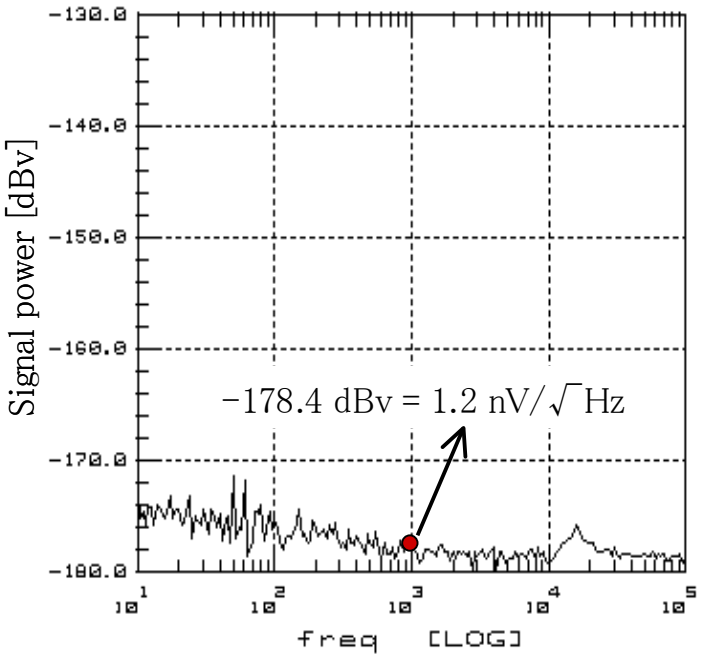

Figure 3.8 Noise floor of the 1/*f* noise measurement system after utilized by EG&G 5184 ultra-low noise pre-amplifier.

3.3.5 DC Source Monitor

Before 1/*f* noise measurement, the device DC characteristics, such as transconductance, input and output resistance, must be measured for setting the expected bias of PA141A and for calculating or converting input reference noise power. Agilent 4156C semiconductor parameter analyzer is used in this system. Long, medium and short integration are available depending on the measured current value. It is recommended to use long or medium for bias setting of the order of mA.

3.3.6 1/*f* Noise Interface Unit, Battery Unit and Ground Unit

1/*f* noise interface unit is specifically designed to coordinate and assist all of equipments to be practical for 1/*f* noise measurement. It contains low-pass filters, load impedances, impedance matching, switching, and substrate bias controller. Most of cable connectors are using triaxial BNC to isolate the signals. The substrate bias can be applied with rechargeable battery unit controlled with high precision variable resistors. The photograph of 1/*f* noise interface unit, battery unit and ground unit is shown in Figure 3.9.

Figure 3.9 Photograph of 1/*f* noise interface unit, battery unit and ground unit

3.3.7 Measurement Technique of the Low-Frequency Noise

Figure 3.10 depicts the equivalent circuit of the 1/*f* noise measurement system. The Device-Under-Test (DUT) is biased with two channels low noise DC source. The bias currents or voltages are filtered with RC low-pass filters to reject the interference noises coming from DC source. The current noises in MOSFET's channel influence the drain voltage fluctuations. As the drain noise signals are very small, the signals must be amplified properly. In this experiment, a typical 60 dB ultra low noise a pre-amplifier power-supplied by batteries is used. The amplified noise signals are measured and analyzed with vector signal analyzer (VSA). Performing measurements under a shielded chamber is highly recommended, as much of interferences from long wave radio frequency can be reduced.

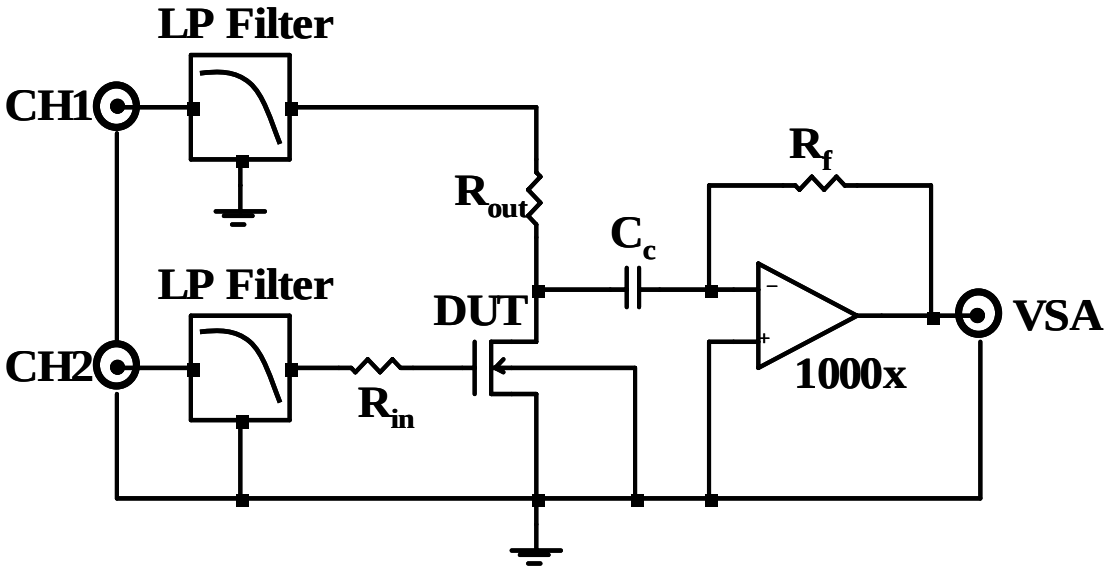

Figure 3.10 Equivalent circuit of 1/*f* noise measurement systems. RC low-pass filters are applied to reject noises coming from the DC source. The drain noise signals are amplified with a 60 dB pre-amplifier before measuring them with vector signal analyzer (VSA).

【Chapter 4】

Characterization of W/HfO_2/Si MOSFET Incorporating La_2O_3

4.1 Introduction

Optimizing high-k dielectrics for the next generations of deep-submicrometer CMOS transistors remains a challenging field. Issues that remain to be solved are the instability of the threshold voltage [12] and the significantly lower mobility compared with thermal SiO_2 gate devices. Hf-based materials are most likely replacement for SiO_2 in the future CMOS technology. However, various reliability [13] and gate-integration issues still persist. One of the issues of Hf-based oxides is the pining of threshold voltage (V_{th}) and mobility degradation [14]. On the other hand, it has been reported that La_2O_3 has been used to control the threshold voltage to negative direction. We investigated the effect of La_2O_3 incorporation underneath the HfO_2 layer in W/HfO_2/Si MOSFETs.

• Properties of La_2O_3

To perform a low EOT, high-κ gate dielectrics materials must have high enough dielectric constant. However, material with very high dielectric constant tends to have narrower band gap that allows higher Schottky conduction currents and tunneling currents. Figure 4.1 shows band gap energy of several metal oxide and silicate materials as a function of dielectric constants. La_2O_3 gives high dielectric constant of 25 and wide band gap of 5.5 eV that is suitable for the use of gate dielectrics.

To inhibit a low leakage current due to Schottky emission conduction mechanism, the high-κ gate dielectric materials must have wide band gap and high barrier of more

than 1 eV for both electrons and holes. Figure 4.2 Predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy. La_2O_3 has a good symmetrical band offset of more than 2 eV for both electrons and holes that is compatible for CMOS devices.

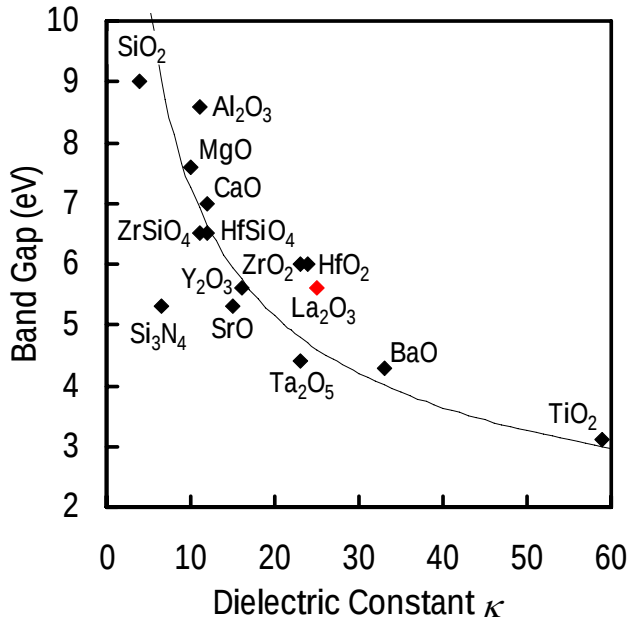

Figure 4.1 Band gap energy of several metal oxide and silicate materials as a function of dielectric constant. Material with very high dielectric constant has narrower band gap that is not suitable for the use of gate dielectrics.

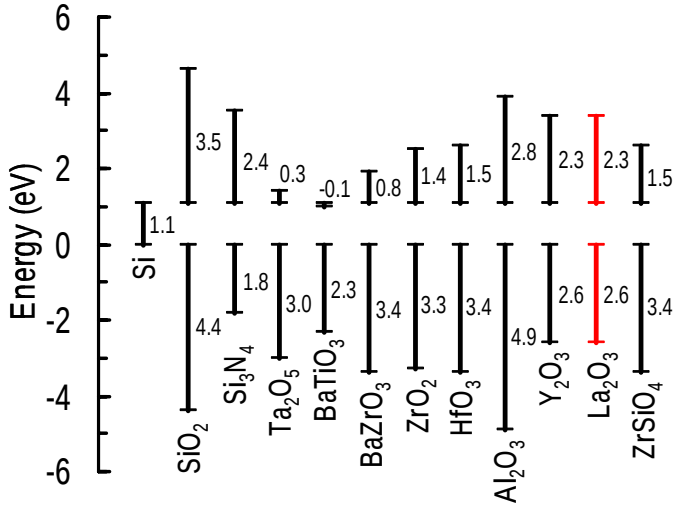

Figure 4.2 Predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy.

4.2 Electrical Characteristics of The Fabricated MOSFETs

The effect of La_2O_3 insertion for HfO_2 gated MOSFET is evaluated. The fabricated samples are (a) W/HfO_2(4nm)/Si and (b) W/HfO_2(2nm)/La_2O_3(4nm)/Si stacked structure as shown in figure 4.3. The gate length and the gate width of this transistor were 2.5 μm and 50μm, respectively. Samples have the same EOT of 1.6nm.

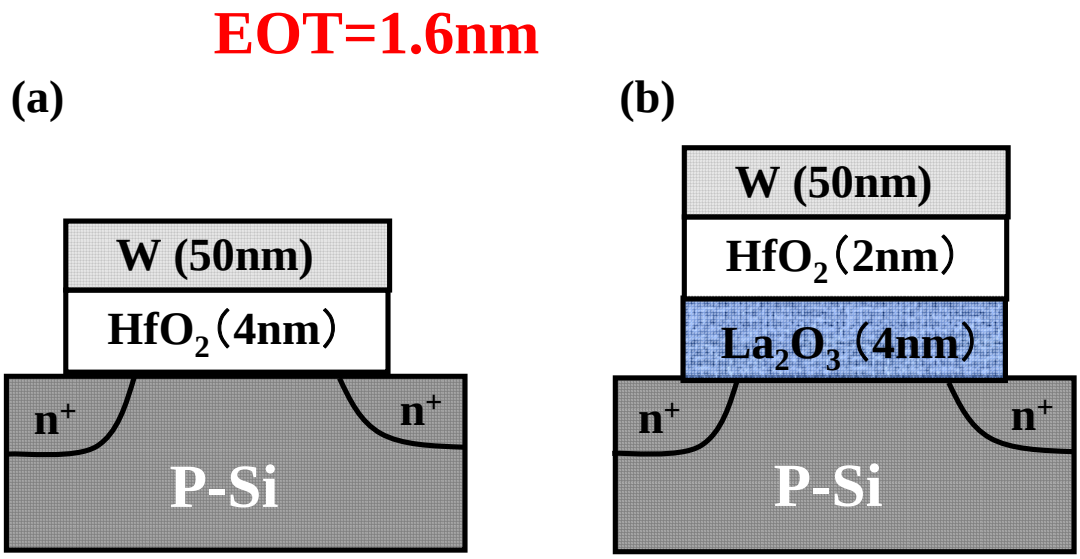

Figure 4.3 Schematic illustration of fabricated MOSFETs of (a) W/HfO_2(4nm)/Si and (b) W/HfO_2(2nm)/La_2O_3(4nm)/Si stacked structure

4.2.1 I_d-V_d Characteristics

We will show electrical characteristics of the MOSFET with W/HfO_2(2nm)/La_2O_3(4nm)/Si stacked dielectrics transistor with 500₀C PMA in F.G ambient for 30min. Figure 4.4 shows I_d-V_d characteristic of the W/HfO_2(2nm)/La_2O_3(4nm)/Si stacked structure .The gate length and the gate width of this transistor were 2.5μm and 50μm. From figure 4.4, we confirmed normal operation with well behaved I_d-V_d characteristic.

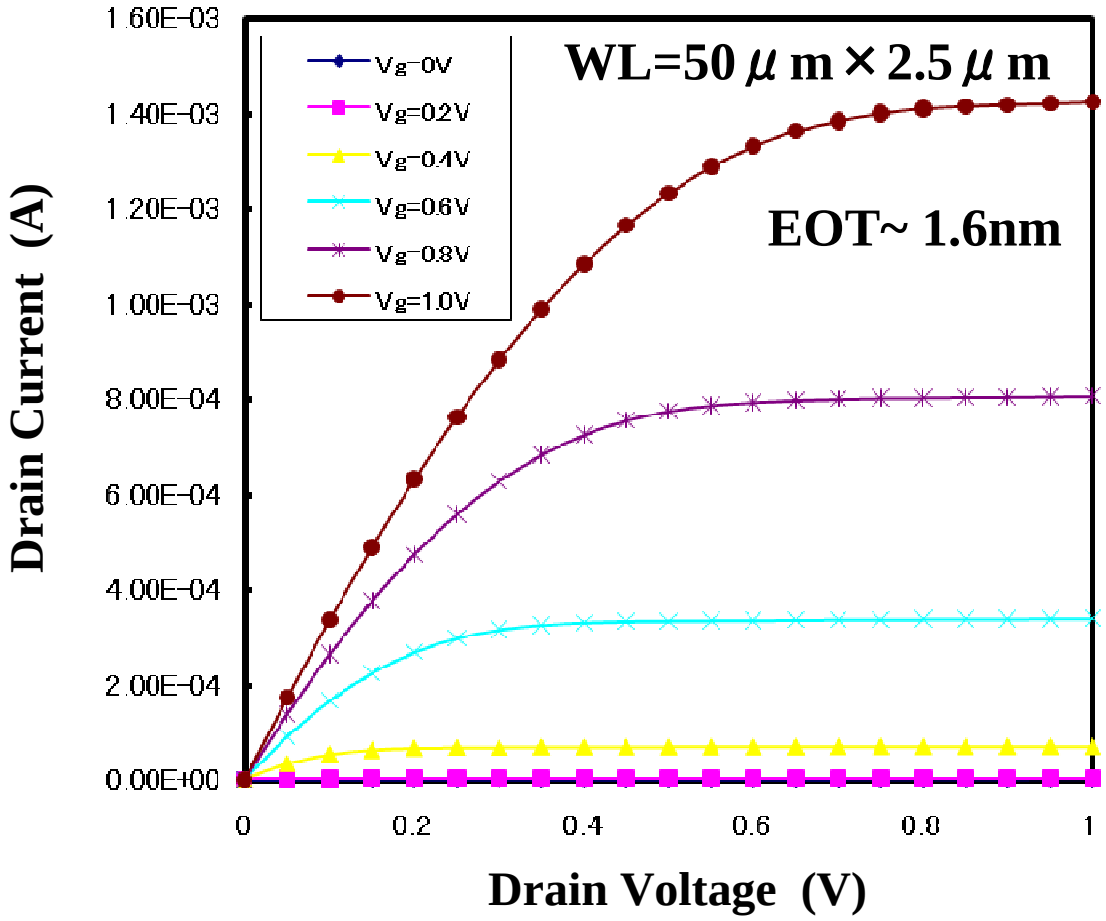

Figure 4.4 I_d-V_d characteristic of incorporation of La_2O_3 at HfO_2/Si interface

4.2.2 I_d-V_g and g_m-V_g Characteristics

Figure 4.5 and Figure 4.6 show I_d-V_g characteristics and g_m-V_g at V_d =50mV of the W/HfO_2(4nm)/Si and the W/HfO_2(2nm)/La_2O_3(4nm)/Si stacked structure, respectively. Subthreshold swing (*SS*) and threshold voltage are shown in table 4.1.

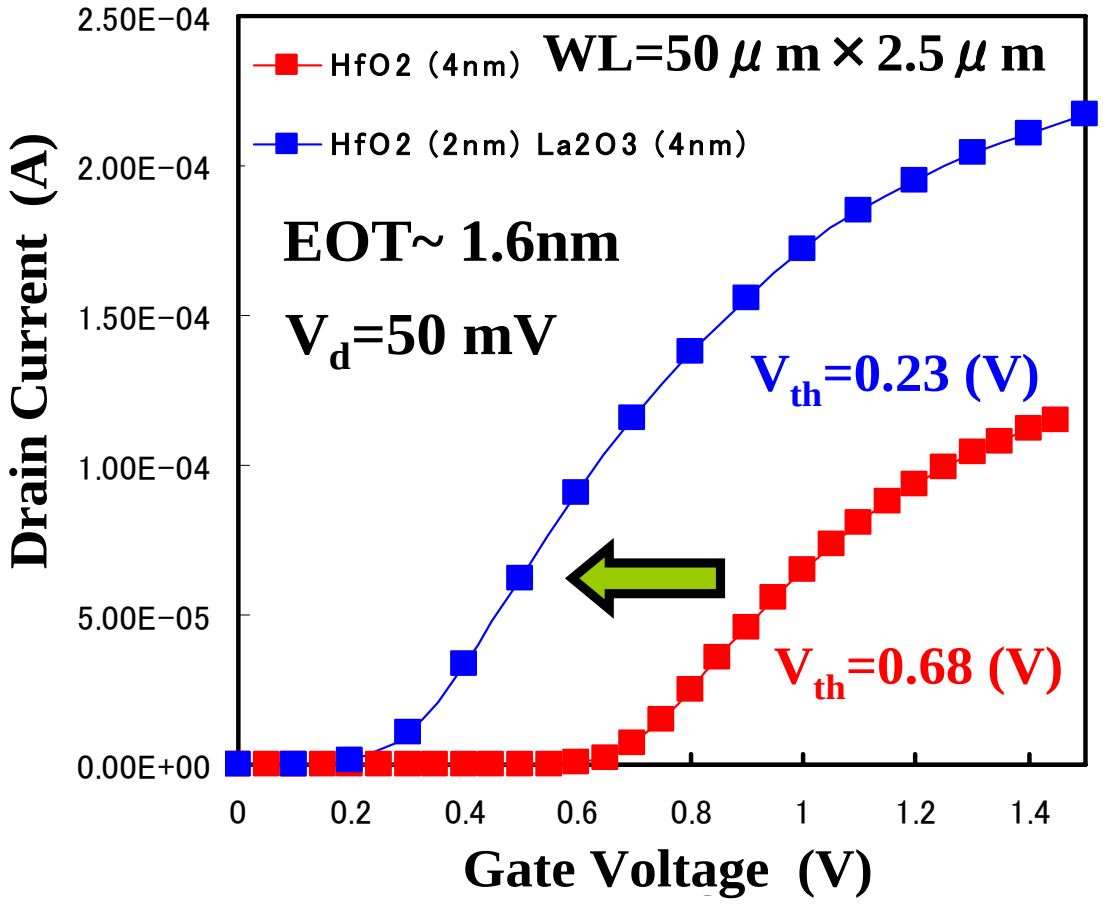

Figure 4.5 I_d-V_g Characteristics of W/HfO_2(4nm)/Si and W/HfO_2(2nm)/La_2O_3(4nm)/Si

Table 4.1 Subthreshold swing (*SS*) and threshold voltage of the fabricated samples

MOSFETs structure	V_{th} (V)	SS (mV/dec.)
HfO_2 (4nm)	0.68	94.6
Hf (2nm) La (4nm)	0.23	71.8

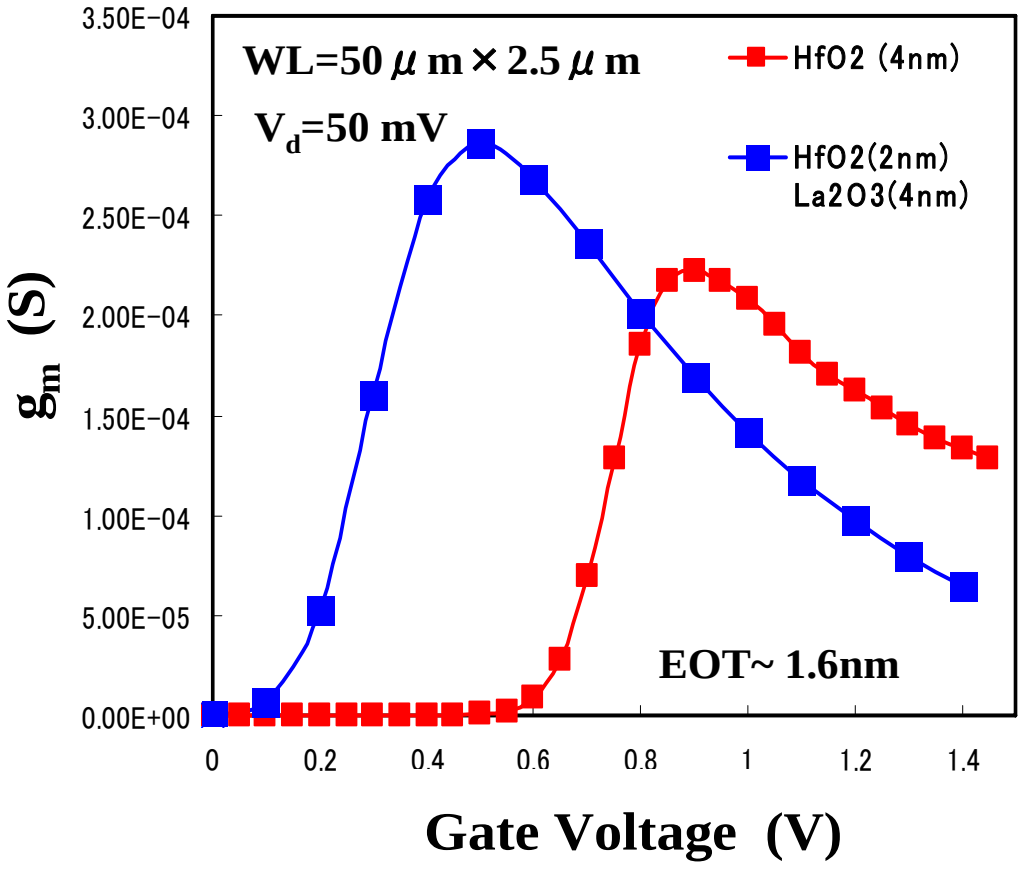

Figure4.6 g_m-V_g Characteristics of W/HfO_2(4nm)/Si and W/HfO_2(2nm)/La_2O_3(4nm)/Si

Value of the threshold voltage (V_{th}) and subthreshold swing (*SS*) is 0.68V and 94.6 mV/dec respectively in W/HfO_2(4nm)/Si structure. On the other hand, V_{th} and *SS* value is 0.23V and 71.8 mV/dec with incorporation of La_2O_3 at HfO_2/Si interface.

The threshold voltage shifted to negative direction by 0.45V with La_2O_3 incorporation. Subthreshold swing (*SS*) of 94.6 mV/dec was improved to 71.8 mV/dec with the incorporation of La_2O_3 presumably owing to better interfacial property.

4.2.3 Effective Electron Mobility

Effective electron mobility (μ_{eff}) of the fabricated MOSFET is evaluated by the split C-V method. Figure 4.7 shows the calculated μ_{eff} also W/HfO_2(4nm)/Si and W/HfO_2(2nm)/La_2O_3(4nm)/Si MOSFETs, that have the same EOT of 1.6nm. The peak mobility is 150 and 200 (cm^2/Vs), respectively.

We observed that the peak mobility was improved from 150 to 200 (cm^2/Vs) by incorporating La_2O_3 underneath the HfO_2 layer.

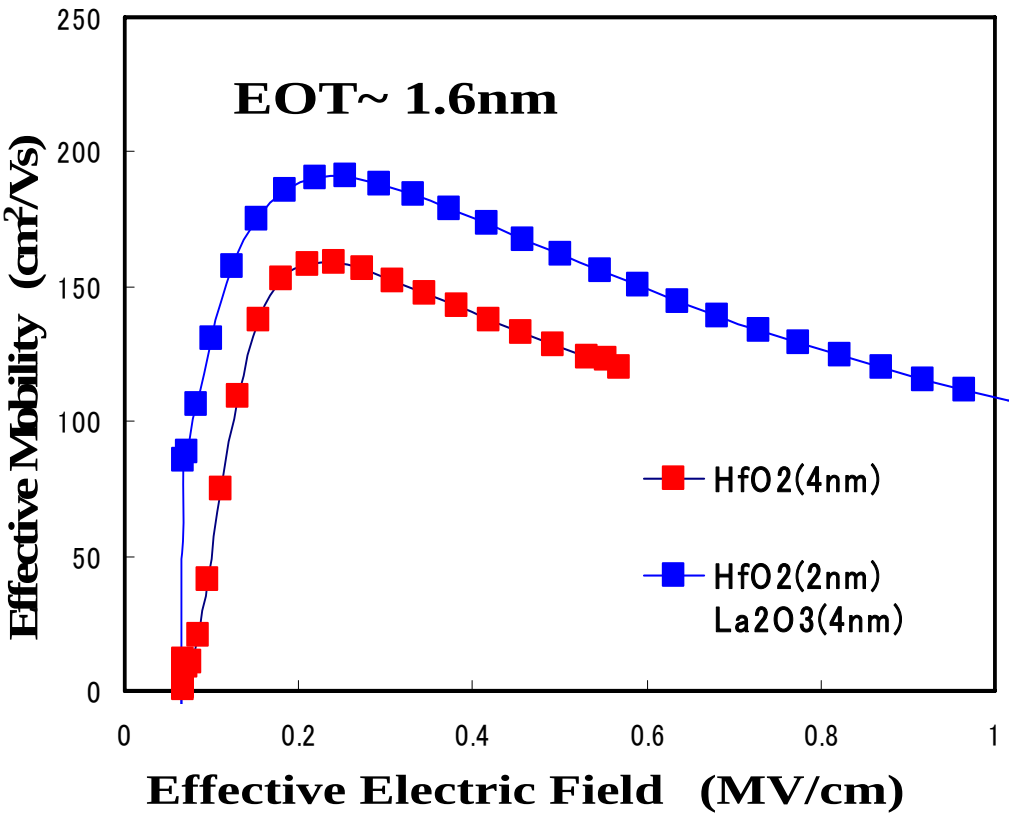

Figure 4.7 Effective electron mobility of La_2O_3 incorporated HfO_2 MOSFET. Samples are same EOT of 1.6nm

4.5 Low-Frequency Noise Characteristics

Figure 4.8 shows the drain current noise (S_{id}) characteristics of the devices at V_d=0.05V and $|V_g-V_t|$=0.2V for n-MOSFETs with W/HfO_2(4nm)/Si and W/HfO_2(2nm)/Si La_2O_3(4nm) /Si. The gate length and the gate width of this transistor were 2.5μm and 50μm, respectively.

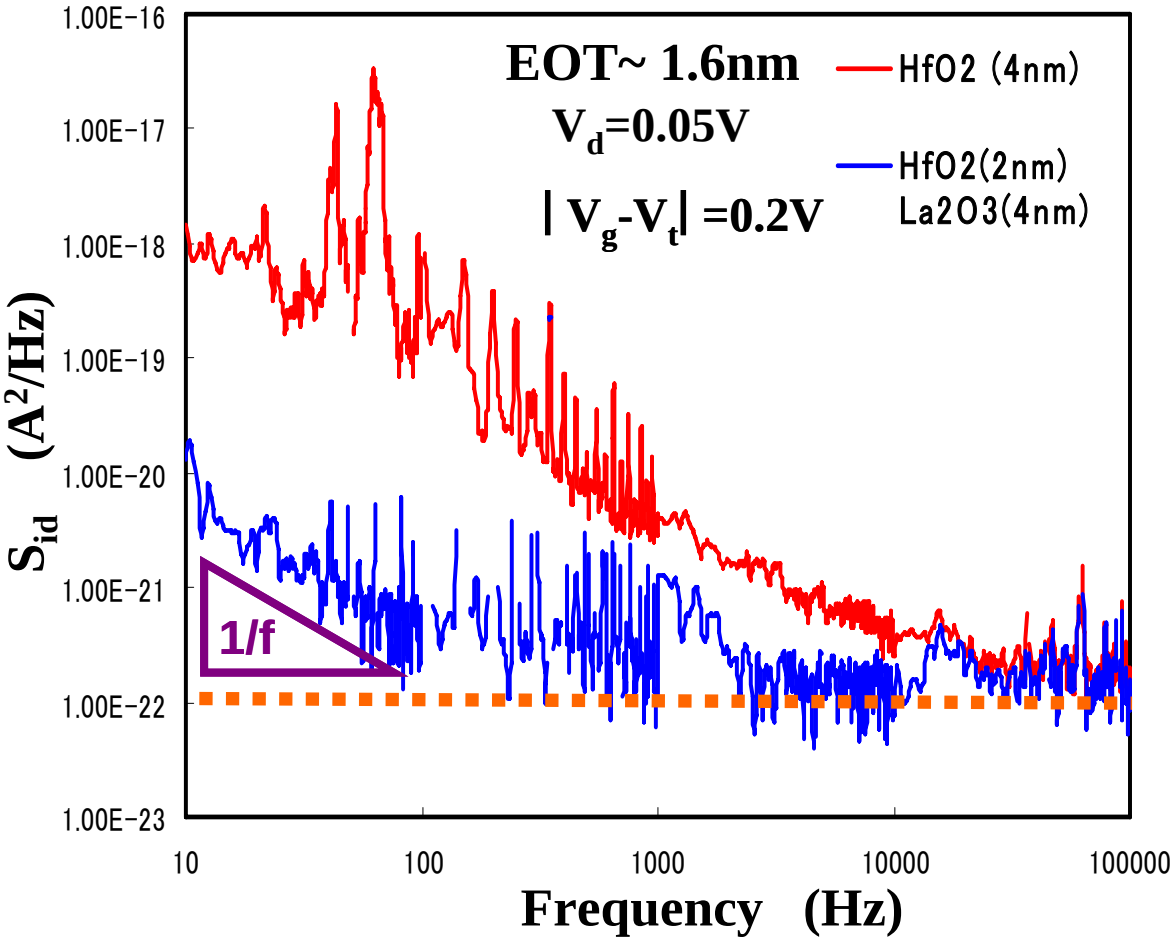

Figure 4.8 Drain current noise vs frequency at V_d=0.05V and $|V_g-V_t|$=0.2V

In this figure, 1/*f* noise was observed in all frequency region for the W/HfO_2(4nm)/Si transistor. On the other hand, 1/*f* noise was observed in 10 Hz~ 1KHz region and thermal noise was observed in 1K~100KHz for the W/HfO_2(2nm)/La_2O_3(4nm)/Si transistor. It is not known exactly why. But, in 10 Hz ~1KHz frequency region, where is dominant for the 1/*f* noise property, the drain current noise level was lower by 1~2 order of magnitude by incorporating La_2O_3. It is shown that the interface condition of the W/HfO_2(2nm)/La_2O_3(4nm)/Si structure is better than structure of W/HfO_2(4nm)/Si.

【Chapter 5】

Conclusion

5.1 Conclusion of This Study

We studied the effect of La_2O_3 incorporation underneath the HfO_2 layer on electrical properties of MOSFETs. By incorporating La_2O_3 underneath the HfO_2 layer, the threshold voltage shifted to negative direction by 0.45V. Subthreshold swing (SS) of 94.6 mV/dec was improved to 71.8 mV/dec with the incorporation of La_2O_3 presumably owing to better interfacial property. Moreover, the peak mobility was improved from 150 to 200 cm^2/Vs by the La_2O_3 incorporation with La_2O_3 underneath the HfO_2 layer.

We investigated 1/*f* noise measurement to make clear the interface condition. It was found that the drain current noise level was lower by 1~2 order of magnitude by incorporating La_2O_3 underneath the HfO_2 layer.

In this study, it was clear that electrical characteristics of the MOSFET using Hf-based oxides were improved by incorporating La_2O_3 underneath the HfO_2 layer.

5.2 Future Issues

Hf-based oxides have been the promising candidates for the next generation gate dielectric. We proposed the control of the threshold voltage and could improve effective mobility by incorporating La_2O_3 layer. However, only measurement of the DC characteristics are insufficient to elucidate the deep nature of the interface property as to the condition of interface. It is necessary to perform 1/*f* noise measurement to investigate the correlation of interfacial states and the noise level in the future of VLSI technologies.

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