

Electrical Characterization of La₂O₃-Gated MOSFET with Mg Incorporation

Tomotsune Koyanagi, Kiichi Tachi, Kouichi Okamoto, Kuniyuki Kakushima*, Parhat Ahmet, Kazuo Tsutsui*, Nobuyuki Sugii*, Takeo Hattori, and Hiroshi Iwai

Frontier Research Center, Tokyo Institute of Technology

*Interdisciplinary Graduate School of Science, Tokyo Institute of Technology,
4259 Nagatsua, Midori-ku, Yokohama 226-8502, Japan
Tel: +81-45-924-5847, Fax: +81-45-924-5846

1 Introduction

Mobility degradation of MOSFETs with high-k gate dielectrics has been one of the major issues for next generation CMOS technology. One of the solutions is to form a SiO₂ interfacial layer to keep the high-k layer and its related fixed charge away from the channel, however, the equivalent oxide thickness (EOT) will eventually increase. In terms of further scaled gate stack technology, high-k should be directly in contact to Si substrates. It has been reported that La₂O₃ can achieve an EOT below 1 nm by forming a La-silicate layer at the interface and showed fairly nice performance[1,2]. However, an additional mobility degradation has been observed in the range of EOT below 1.5 nm accompanied by a negative shift in flat band voltage (V_{fb}), indicating an accelerated generation of fixed charges in high-k. On the other hand, it has been reported that the incorporation of Mg into Hf-based dielectrics shows large improvement in mobility and reliability as well[3]. Therefore, it would be worth trying to incorporate Mg into La₂O₃ to suppress the generation of fixed charges. In this report, the improvement on electrical properties of La₂O₃ gated capacitors and MOSFETs with Mg incorporation is discussed.

2 Experiment

La₂O₃ layers ranging from 2 to 4 nm were deposited by e-beam evaporation on a HF-last SiO₂ isolated n-Si(100) wafer and source/drain preformed p-Si(100) wafer for capacitor and nFET, respectively. Then, 1-nm-thick Mg layer was *in situ* evaporated, followed by 60-nm-thick sputtered layer of W. W was patterned by reactive ion etching (RIE) using SF₆ chemistry to form gate electrodes. Wafers were then post-metallization annealed (PMA) in a rapid thermal annealing (RTA) furnace in forming gas (FG)(N₂ : H₂ = 97% : 3%) ambient at 500 °C for 30 min. Backside Al was finally deposited as a bottom electrode by thermal evaporation. Fig. 1 shows the schematic illustration of the as-deposited gate structure.

3 Results and Discussion

Fig. 2 shows a cross sectional TEM image of a fabricated MOS capacitor, where a slight bright contrast is observed at Si interface. EDX line-profile reveals the diffusion of Mg into La₂O₃ and further into grown La-silicate layer. The evolution of V_{fb} on EOT with and without Mg is shown in fig. 3. An aggressive V_{fb} shift below 1.7 nm is well controlled with the use of Mg, which may be either the effect of suppression of fixed charge generation or a dipole formation at Si interface. The incorporation of Mg also showed the same effect on threshold voltage (V_{th}), meanwhile little difference was observed on subthreshold swing (S. S.). The effective electron mobility (μ_{eff}) of both nFETs with EOT around 1.1 nm is shown in fig. 5. A large improvement in μ_{eff} , especially at low field is observed. It is known that mobility at low field is mainly limited by Coulomb scattering[4]. Therefore, because the doping densities in the two devices are the same, it can be concluded that charges in oxide is suppressed by the incorporation of Mg.

4 Conclusion

The effect of Mg incorporation into La₂O₃ gated MOSFET on electrical characteristics have been conducted. The aggressive shift in V_{fb} and V_{th} at small EOT can be effectively suppressed with the incorporation of Mg. Moreover, Mg incorporated La₂O₃-nFET has showed a large improvement in μ_{eff} mainly at low effective field. Future works is to optimize the amount of Mg into La₂O₃.

References

- [1] J.A. Ng, et al., *ELEX 3* (2006), pp. 316–321
- [2] H. Iwai et al., *IEDM Tech Dig* (2002), pp. 625–628.
- [3] N. Mise, et al., *IEDM Tech Dig.*(2007), p.527
- [4] S. Saito, et al., *Appl. Phys. Lett.* 81, 2391 (2002).

Acknowledgement

This work has been supported by NEDO.

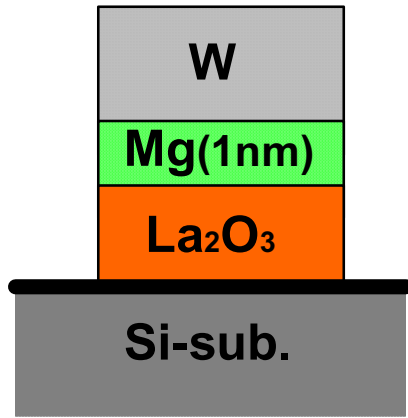


Figure 1 Schematic illustration of fabricated W/Mg(1nm)/La₂O₃(2~4nm)/Si structure.

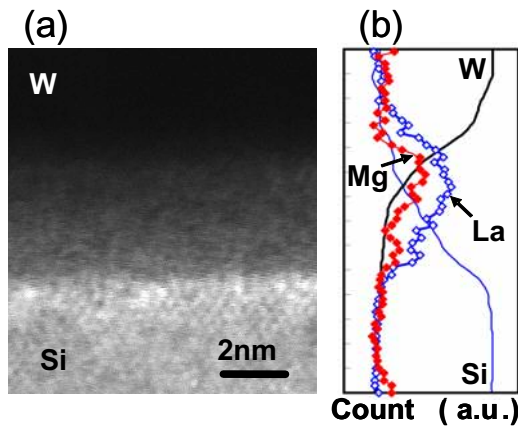


Figure 2 (a) Cross sectional TEM image of W/Mg(1nm)/La₂O₃/Si after PMA. (b) EDX line profile perpendicular to the gate stack reveals the diffusion of Mg into La₂O₃ and La-silicate.

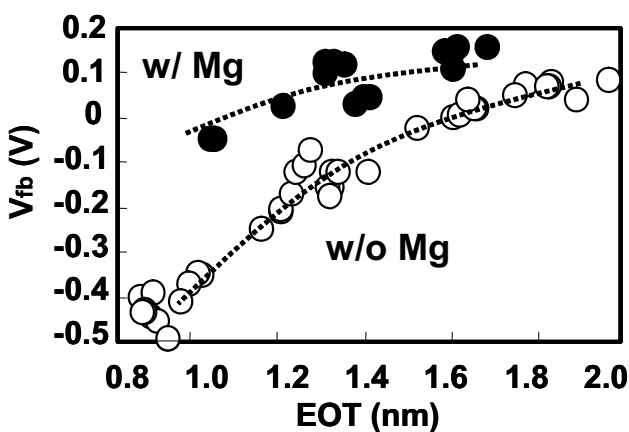


Figure 3 V_{fb} dependence on EOT. With Mg incorporation the aggressive V_{fb} shift can be suppressed.(PMA:500°C)

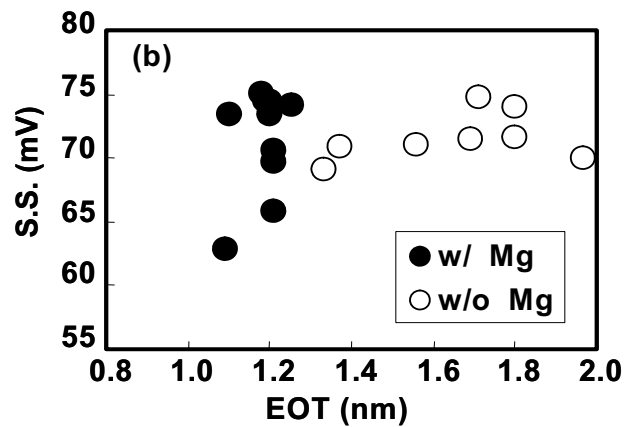
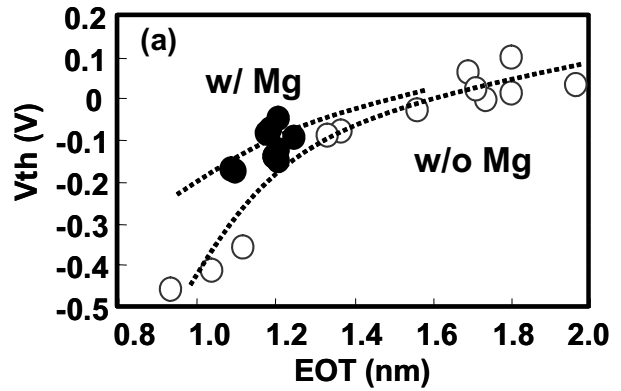


Figure 4 (a) Dependence of V_{th} on EOT also show the same trend to that of V_{fb}. (b) Little change was observed on S. S.

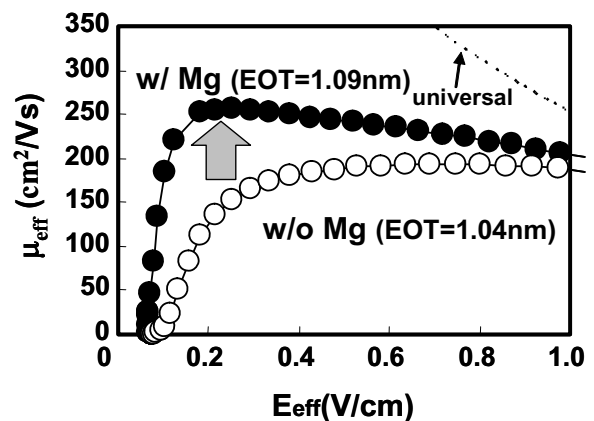


Figure 5 μ_{eff} of La₂O₃ gated MOSFET with and without Mg. An increase in μ_{eff} , especially at low field is obtained.