Effect of Ultrathin Si Passivation Layer for Ge MOS Structure with La_2O_3 Gate Dielectric

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Abstract

The effect of ultrathin Si passivation layer on Ge MOS characteristics with La_2O_3 gate dielectric has been examined. Hysteresis on C-V curve significantly reduced with Si passivation layer over 1nm due to suppression of Ge suboxide growth. However, positive flat-band voltage shift was observed with the interfacial Si layer. The excessive V_{fb} shift relieved with increasing Si layer thickness, which seemed to converge over 2.0 nm.

Introduction

Recently, Ge has drawn lots of attention for further performance improvement of MOSFETs thanks to its high carrier mobility. However, Ge metal-oxide-semiconductor (MOS) device has a critical problem on the selection of gate dielectric material. In addition, considering the process generation that Ge MOSFETs will be introduced to the semiconductor industry, small equivalent oxide thickness (EOT) is necessary. For these reasons, high dielectric constant (high-k) materials with superior interface quality on Ge are necessary for the Ge-MOSFETs [1]. In many high-k materials, La_2O_3, which possesses high bulk dielectric constant (~27) and large band-gap, is more attractive than other high-k materials [2]. On the other hand, it seems difficult to achieve satisfactory property in direct formation of high-k on Ge substrate, and better characteristics have been obtained with passivation layer such as GeON, Ge_3N_4 and Si on Ge substrate [3-5]. In this work, we studied the effects of ultrathin Si passivation layer on Ge substrate in La_2O_3/Ge MOS structure.

Experimental Details

n-type Ge wafers were cleaned by the NH_4OH/ H_2O_2/H_2O (1/2/20) treatment and then transferred into an ultrahigh-vacuum (UHV) chamber (~10^{-8} Pa) and annealed at 500°C to remove the remained Ge oxide. After that, ultrathin Si layer and La_2O_3 films were deposited by electron-beam evaporation under pressure of ~1×10^{-6} Pa at substrate temperature of 250°C. Tungsten (W) films were deposited *in situ* to avoid moisture absorption of La_2O_3 from air. Gate electrode structures were defined by lithography and dry etching.

Results

Figure 1 shows C-V characteristics of W/La_2O_3/Ge MOS capacitors with or without Si passivation layer on Ge substrate. The samples were annealed in N_2 at 500°C for 5 minutes. The initial thickness of Si passivation layer without PMA is about 1.5 nm. Hysteresis on C-V curve dramatically decreased with Si passivation layer of 1.5nm. In the La_2O_3/Ge stack, a large amount of hysteresis is considered to be caused by a Ge suboxide layer [2]. Therefore, the suppression of Ge-suboxide growth by Si passivation layer would reduce the hysteresis of La_2O_3/Ge system, as is indicated in Fig. 2. On the other hand, positive flat-band voltage (V_{fb}) shift was observed with Si passivation layer as shown in Fig. 1. Similar V_{fb} shift in high-k/Ge system with Si passivation layer was observed in *Ref* [5]. This positive shift of V_{fb} was observed only in samples sufficiently passivated by Si layer (>1.0 nm), which Ge oxide did not grow. The amount of positive V_{fb} shift decreased with increasing Si layer thickness, which seemed to become constant at 2.0 nm or thicker as shown in Fig. 3.

Conclusions

Ge suboxide growth was perfectly suppressed with Si passivation layer in La_2O_3/Ge structure, which reduced hysteresis on C-V curve. On the other hand, positive flat-band voltage shift was observed with the Si layer. The amount of V_{fb} shift decreased with increasing Si layer thickness, which seemed to become constant at 2.0 nm or thicker. Considering the control of threshold voltage (V_{th}), the Si layer of 2.0 nm thick or higher is required.

Acknowledgement

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Reference

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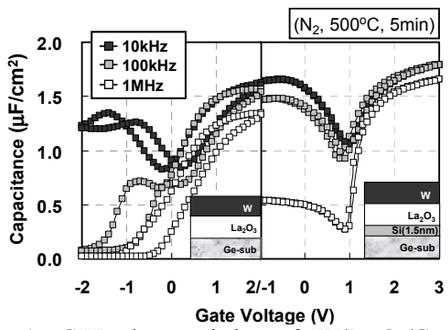

Figure 1. C-V characteristics of W/La_2O_3/Ge MOS capacitors with or without Si passivation layer.

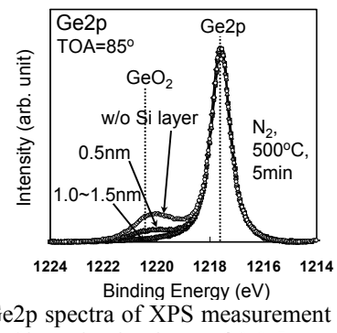

Figure 2. Ge2p spectra of XPS measurement in La_2O_3/Ge system with Si passivation layer of 0-1.5 nm.

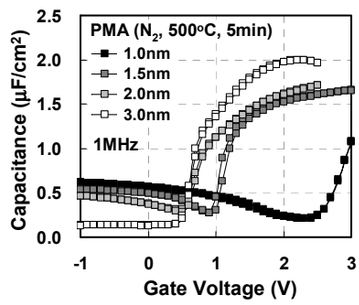

Figure 3. C-V characteristics of W/La_2O_3/Si/Ge MOS capacitors with Si passivation layer of 1.0-3.0 nm.