0.5 nm EOT MOS structure with $TaSi_x$/W stacked gate electrode

K. Okamoto[1], K. Kakushima[2], P. Ahmet[1], K. Tsutsui[2], N. Sugii[2], A. N. Chandorkar[1, 3] T. Hattori[1] and H. Iwai[1]
[1]FCRC, Tokyo Institute of Technology,
4259-S2-20, Nagatsuda-cho, Midoriku, Yokohama
226-8503, Japan
Tel:+81-45-924-5847 Fax:+81-45-924-5846
[2]IGSSE, Tokyo Institute of Technology
[3]Indian Institute of Technology Bombay
E-mail: okamoto.k.af@m.titech.ac.jp

Abstract

MOS structures using HfO_2, La_2O_3 and tungsten (W) electrode in gate-last-process was fabricated. However, surplus oxygen supply caused by W gate metal made it difficult to keep EOT small after annealing and promoted interfacial layer (IL) growth. In order to reduce EOT increase after annealing, $TaSi_x$ electrode was introduced and $TaSi_x$ (50 nm)/W (5 nm) stacked electrode was revealed to prevent IL growth dramatically. Thanks to $TaSi_x$ introduction, MOS capacitor (MOSCAP) with 0.5 nm could be fabricated using gate-last-process.

Introduction

Aggressive scaling of MOSFET devices requires a Metal gate/High-k gate stack [1-2]. HfO_2 based materials with SiO_2 interfacial layer stacks have been one of the promising candidate. However, to achieve 0.5 nm EOT, which is the ultimate specification in ITRS roadmap, high-k should be directly contacted on Si substrate and SiO_2 IL should be removed. In this study, we fabricated MOSCAPs with HfO_2 and La_2O_3 gate insulator using W and $TaSi_x$ as gate electrodes for SiO_x-IL-free gate stacks.

Experimental

HfO_2 and La_2O_3 films were deposited on HF-last, n-Si (100), the dopant density of which is $1.5\text{x}10^{15}$ cm^{-2} by e-beam evaporation in an ultra high vacuum chamber ($\sim10^{-6}$ Pa). And Gate electrode W and $TaSi_x$ were in-situ deposited by RF sputtering to avoid to any moisture absorption. Annealing was performed ex-situ using image furace assuming a gate-last-process at 500°C in F.G. ambient (N_2:H_2=97:3). Capacitance-Voltage (CV) characteristic of the MOSCAPs measured at 100 kHz using Agilent4284A precision LCR meter and EOT was calculated from CV characteristics using the NCSU CVC program.

Result and Discussion

We fabricated HfO_2/La_2O_3 MOSCAP which has relatively low V_{fb} compared to that of HfO_2 capacitors [3].Fig.1 shows sectional TEM image of W/HfO_2/La_2O_3 and schematic model of the MOS structure, we can find that SiO_x IL growth occurred after annealing. This IL growth was caused by surplus oxygen supplied from top W electrode. So, gate stacks with 0.5 nm EOT is difficult to be realized.

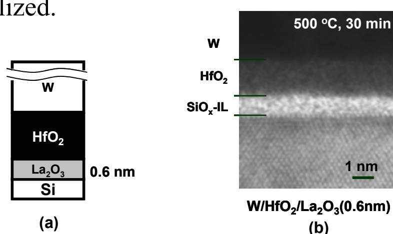

Fig.1 W/HfO_2/La_2O_3 MOSCAP; (a) schematic model and (b) cross sectional TEM image.

In order to choose gate electrodes which can maintain small EOT after annealing, we firstly fabricated HfO_2 (3 nm)/La_2O_3 (1 nm) stacked MOSCAPs with $TaSi_x$/W stacked top electrodes. The thickness of $TaSi_x$ on W electrode was all 50 nm and that of W was changed from 5 to 60 nm. Fig.2 shows CV characteristics and EOT increase-inserted W thickness plot. EOT increase corresponds to the difference between EOT after PMA 500°C and that of as-deposition. In this experiment, EOT of as-deposition MOSCAPs was all 0.6 nm. We can see that EOT after annealing increased as the inserted W became thick. When inserted W is as thin as 5 nm, EOT increase after annealing was under 0.1 nm. That is, as the thickness of inserted W film becomes thin, amount of oxygen included in W decreases and O_2 used in IL growth can not be supplied from outside.

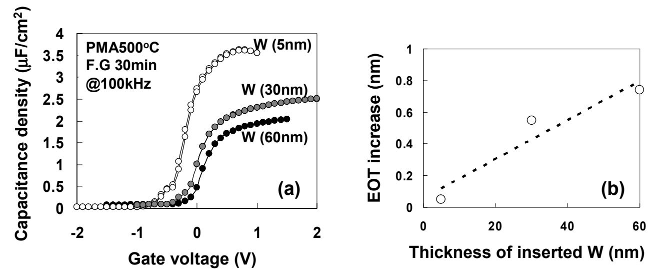

Fig.2 Electrical characteristics of HfO_2/La_2O_3 stacked MOSCAPs using $TaSi_x$(50 nm)/W(5~60 nm). (a) CV characteristics, and (b) EOT increase vs. W thickness.

Using the $TaSi_x$ (50nm)/W (5nm) electrode, we successfully fabricated a 0.5 nm EOT MOSCAP with La_2O_3 film only. The schematics of the MOSCAP and the CV characteristics are shown in Fig.3 (a). And we found that, after the annealing, frequency dispersion due to interface states at high-k/Si was reduced comparing to as-deposited sample, as shown in Fig. 3 (b) and (c). This result indicates that effect of Ta diffusion to Si interface after annealing is small.

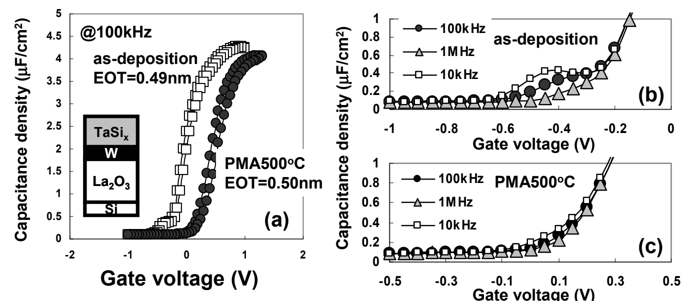

Fig.3 (a) CV curves of 0.5 nm EOT MOSCAP. (b) Frequency dispersion on CV curves for MOS capacitors of as-deposited and after annealing.

Conclusion

The reason of IL growth after annealing was revealed to be the surplus oxygen supply from the W electrode deposited by RF sputtering. To reduce the SiO_x IL growth, $TaSi_x$ should be capped on thin W film. It was confirmed that 5 nm W is enough to avoid IL formation. We succeeded in fabricating 0.5 nm EOT MOS capacitor using gate-last-process with $TaSi_x$ (50nm)/W(5nm) stacks as top electrode and La_2O_3 as gate insulator.

References

[1]P. D. Kirsch, *et al.*, *IEDM Tech Dig.*, p.629 (2006).
[2]S. K. Han, *et al.*, *IEDM Tech Dig.*, p.621 (2006).
[3]K. Okamoto, *et al.*, *ESSDERC*, p.199 (2007).