Schottky Barrier Height Modulation by Er Insertion and Its Application to SB-MOSFETs

K.Noguchi [1], W.Hosoda [1], K.Matano [1], K.Kakushima [2], P.Ahmet [1], K.Tsutsui [2], N.Sugii [2], A. N. Chandorkar [1,3], T.Hattori [1], and H.Iwai [1]
[1]FCRC, Tokyo Institute of Technology, 4259-S2-20, Nagatsuta-cho, Midori-ku, Yokohama 226-8503, Japan
Tel: +81-45-924-5847 Fax: +81-45-924-5846
[2]IGSSE, Tokyo Institute of Technology,
[3]Indian Institute of Technology Bombay
E-mail: noguchi.k.ab@m.titech.ac.jp

ABSTRACT

We investigated the modulation of Schottky barrier height (Φ_b) by inserting Er layer between Si (100) substrate and Ni layer before the silicidation annealing. Φ_b for electrons of NiSi was decreased by inserting an Er layer.

INTRODUCTION

The Schottky barrier source/drain MOSFET (SB-MOSFET) is one of the promising candidates for next generation devices, thanks to its shallow junction depth with lower electrode resistance and process temperature [1-2]. However, the high barrier height (Φ_b) severely limits the drive current of SB-MOSFETs [3-4]. The Er silicide has been proposed for SB-NMOS because of very low Φ_b of 0.27-0.36 eV for electrons [5]. However, the reports of middle gap materials such as NiSi also showed the great possibility of these materials for applications of the SB-MOSFET by employing the Φ_b modulation techniques [3].

In this work, we investigated Φ_b modulation of Ni silicide by inserting an Er interlayer at the Ni/Si interface before silicidation, and applied the technique to n-cannel SB-MOSFETs fabrications.

EXPERIMENTAL DETAILS

Schottky diode was formed on SiO_2 isolated n- and p-type bulk (100) Si wafers, as shown in Fig. 1. The patterned wafers were cleaned in mixed solution of H_2SO_4 and H_2O_2 followed by chemical oxide removal by diluted HF. Pure metals of Er and Ni were deposited subsequently on to the substrates by DC sputtering in Ar gas at a pressure of 5.5×10^{-1} Pa. The layered structures of Ni/Er/Si consisting of 12-nm-thick Ni layer and Er layer of various thicknesses ranging from 3.6 to 12 nm were deposited. The samples were annealed in forming gas (3% H_2 + 97% N_2) at various temperatures from 400°C to 700°C for 1 min. After the removal of un-reacted metals by chemical etching, Al back contacts were formed.

A fabrication process of SB-MOSFETs as shown in Fig. 2 was proposed, in which Er and Ni were deposited on the source/drain pre-formed P-Si (100) substrates and annealed in the same manner described above.

RESULTS

The Φ_b values evaluated from the *I-V* corves in the forward bias region are plotted as a function of the Er thickness as shown in Fig. 3. It was found that the insertion of 12-nm-thick Er followed by annealing at 700°C lowered the Φ_b for electrons by 0.22eV. This result indicates that the Er insertion is promising for N-channel SB-MOSFETs. The values of Φ_b were fond to depend also on the annealing temperature and the Er thickness.

Fabrication of N-channel SB-MOSFETs is in progress and the details will be discussed at the conference site.

CONCLUSION

The Φ_b modulation of Ni silicide on Si by the Er interlayer was investigated. We found that the Φ_b for electrons was lowed by 0.22eV, by using this technique.

ACKNOWLEGEMENTS

This work is supported by Grant-in-Aid for Scientific Research on Priority Areas by the Minister of Education, Culture, Sports, Science and Technology, Japan.

REFERENCES

[1] S. Zhu, *et al*., IEEE Electron Devices Lett, **25**, 565 (2004).
[2] M. Jang, *et al*., IEEE Electron Devices Lett, **26**, 354 (2005)
[3] A.Kinoshita, *et al*., Symp. VLSI Tech. 9A-3, (2005).
[4] J. Kedzierski, *et al.,* IEDM Tech Dig 57-60, (2000).
[5] J. M. Larson and J. P. Snyder., IEEE Trans. Electron Devices, vol. 53, 1048 (2006).

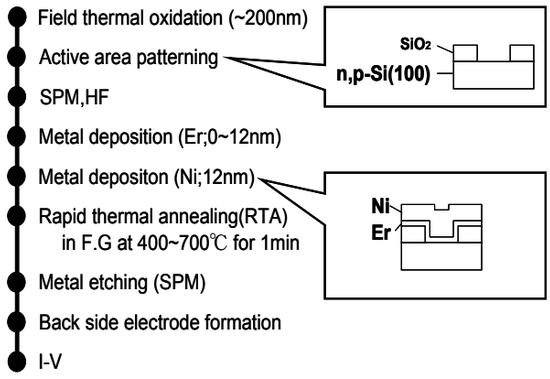

Fig. 1. Fabrication process of Schottky barrier diode.

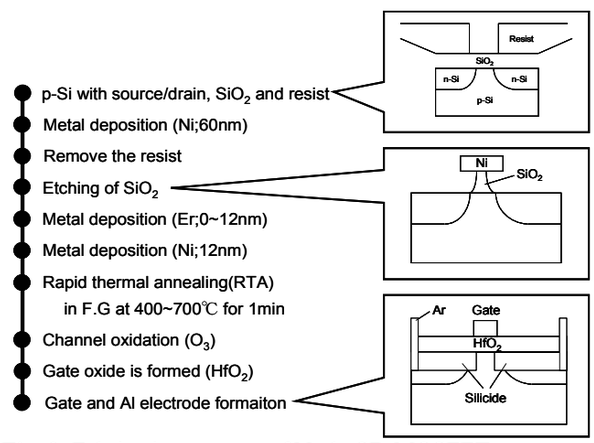

Fig. 2. Fabrication process of N-ch. SB-MOSFETs.

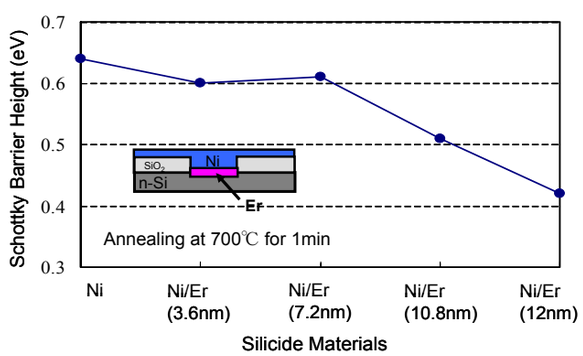

Fig. 3. Schottky barrier height for electrons depending on thickness of Er interlayer after annealing at 700℃.