Electronic Structure Analysis of Silicon Nanowires for High Conductivity in n- and p-channel Nanowire-FET

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Introduction

From the scaling limit issues in planer MOSFET, 3D-MOSFET including Fin or Tri-gate have been focused for future LSI devices, owing to its ability to reduce the off current (I_{off}), which eventually reduces the power consumption. These 3D-MOSFETs also provide larger on current (I_{on}) by adjusting the threshold voltage (V_{th}) to appropriate value. However, the total current required for driving the circuit would be limited due to its narrower cross section. This concern is also applied to Nanowire-FET which is the ultimate 3D-MOSFET. One way to improve the I_{on} at small cross section is to achieve 1-dimensional transport (Fig. 1). In order to investigate the properties of the Nanowire-FET, we analyzed the electronic structure of silicon nanowires (SiNWs), which are used as a channel for Nanowire-FET.

Method

The electronic structures of SiNWs are calculated by the first principles calculations with local density functional approximation (LDA) [1,2] using ultrasoft pseudo-potential proposed by Vanderblt [3]. All the calculations are done by Tokyo Ab-initio Program Package (TAPP) [4]. We analyzed the dependence of cross section side length (SL) on the band structure of <100> SiNWs having a square cross section. From these results, the SL dependence on bandgaps (E_g), electron effective masses (m^*) and the number of quantum channels were estimated. The obtained E_g are shifted by 0.5 eV, which is required to reproduce the bulk silicon E_g value.

Result and Discussion

SiNWs have a direct E_g at gamma point, which are in contrast to bulk Si. The E_g of SiNWs becomes wide as SL decreases and E_g of 3.1 eV is obtained with SL = 0.77 nm. When SL increases, the E_g becomes close to that of the bulk Si (1.12 eV). The m^* at conduction band minimum becomes light as the SL increases. Moreover, the m^* moves towards the bulk m^*, 0.2 m_0, when the SL of SiNWs increases.

When 1-dimensional ballistic conduction is achieved, the conductivity of SiNW MOSFET is basically determined by the number of quantum channels near conduction band minimum (CBM) in n-channel FET and valence band maximum (VBM) in p-channel FET. Here, the numbers of quantum channels within 50 meV (100 meV) from CBM and VBM are plotted in Fig. 2. Number of quantum channels within 50 meV (100 meV) from CBM increases from 2 to 4 (from 4 to 7), as the SiNW SL increases from 0.77 nm to 3.84 nm. Within 50meV (100 meV) from the VBM, number of channels increases from 2 to 7 (from 2 to 7). Therefore, larger SiNW SL can achieve higher conductivity from the viewpoint of the number of quantum channels near each edge.

However, as the density of bands increase, the spacing of each band becomes narrow, which will allows inter sub-band scattering and eventually reduces the conductivity [5]. Here, we propose a model that there exists a trade off between the quantum channel numbers and inter sub-band scattering and an optimum SL exists for the SiNW MOSFET application (Fig. 3).

Conclusions

In conclusion, the tendency of E_g, m_e and the number of quantum channels for different SLs in SiNWs has been calculated. A trade-off model for I_{on} is proposed for SiNW MOSFET.

Acknowledgement

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Reference

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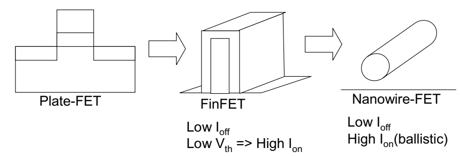

Fig. 1 The concept of device scaling for future MOSFET

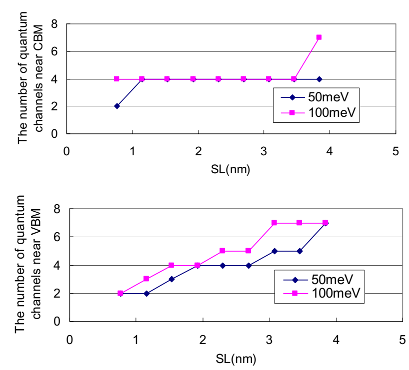

Fig. 2 The number of quantum channels versus SL. Diamond points indicate the numbers of quantum channels within 50 meV from the CBM (upper) and VBM (lower). And square points indicate the numbers of quantum channels within 100 meV.

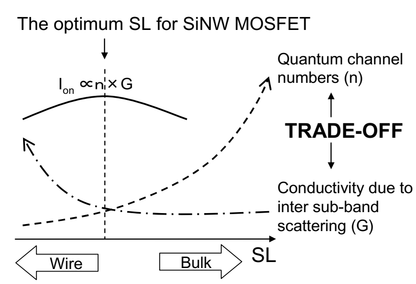

Fig. 3 The trade off model between the quantum channel numbers (n) and the conductivity (G) with inter sub-band scattering. The arrow of n and G curves points a direction to obtain a high I_{on}. An optimum SL exists for SiNW MOSFET application.