Electric properties of CeO_X /La_2O_3 stack as gate dielectric in advanced MOSFET technology

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Abstract

The dielectric properties of CeO_x/La_2O_3 gate stack was investigated. The leakage current at the EOT around 1.0 nm was suppressed by one order compare to the leakage current in La_2O_3 by introducing CeO_X/La_2O_3 stack.
MOSFETs with CeO_x/La_2O_3 stack as the gate dielectric were fabricated and its properties were studied.

Introduction

CeO_x has a high dielectric constant of ~ 26 [1], but is has a relatively narrow band gap of 3eV. On the other hand, La_2O_3 has a large band gap of ~5.4eV, however, EOT increases due to growth of silicate [2] at the interface of La_2O_3/Si during the thermal process. It was reported that the interfacial layer growth at the La_2O_3/Si interface strongly depend on the supplied oxygen to the La_2O_3 film[3] and CeO_x has a excellent oxygen storage properties thanks to the chemical properties Ce ion. Therefore, it is expected that a CeO_x / La_2O_3 stacked structure may improve the dielectric properties of La_2O_3. In this paper, we report the dielectric properties of CeO_x / La_2O_3 gate stack.

Experiments

MOS capacitors and MOSFET were fabricated on a n-type Si(100) wafers (resistivity 1~10 Ωcm). After chemical cleaning with H_2SO_4+H_2O_2 followed by HF dipping, the stacked structures consisting of La_2O_3 and CeO_x films were deposited by electron-beam deposition in ultrahigh vacuum (10^{-6} Pa) at 300 °C. Thicknesses of the materials were controlled by moving a mechanical shutter during the deposition. Single-layer capacitors of La_2O_3 and CeO_x were fabricated as references. Tungsten (W) metal gate electrode was *in-situ* deposited by RF sputtering in order to avoid any moisture or carbon-related contamination. Post-metallization annealing (PMA) was conducted in forming gas (H_2:3%, N_2:97%) at 500 °C for 30 min.

EOT values were derived by fitting capacitance-voltage (C-V) curves using the CVC program. Gate current density-voltage (J-V) properties were measured at the temperatures of 20 to 120°C

Results and Discussions

Figure 1 shows the J-V characteristics of the fabricated capacitors with CeO_X single layer, La_2O_3 single layer and CeO_X/La_2O_3 stack, respectively. All of these samples have similar EOT values. It was observed that the measured leakage current in CeO_X/La_2O_3 stack was the smallest among the three types of the measured samples; CeO_X single layer, La_2O_3 single layer and CeO_X/La_2O_3 stack. Figure 2 shows the relation between Leakage current and EOT in the fabricated capacitors at a gate voltage of 1 V. Compare to CeO_X and La_2O_3 single layer dielectrics, the leakage current at EOT around 1.0 nm was suppressed by two orders compare to former one and was suppressed by one order compare to later one by introducing the CeO_X/La_2O_3 stacked insulator, strongly suggests the practical advantages of the CeO_X/La_2O_3 in reducing the leakage current.

Conclusions

We have investigated the dielectric properties of CeO_x/La_2O_3 gate stack. It was observed that the leakage can be suppressed by introducing the CeO_X/La_2O_3 stacked insulator. Our results show that the advantages of the CeO_X/La_2O_3 in reducing leakage current and the superior properties as one of the promising candidate of new high-k materials.

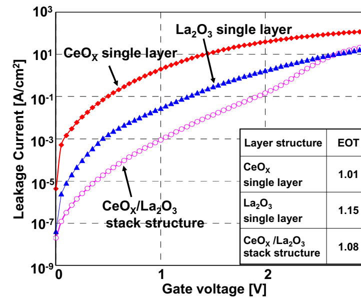

Figure 1 . J-V characteristics in the CeO_X, La_2O_3 single layer and CeO_X/La_2O_3 stack structure capacitors.

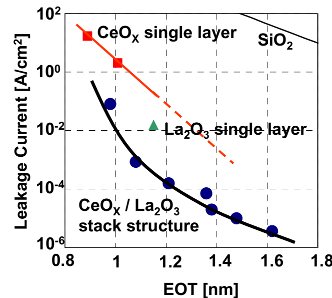

Figure 2. Jg－EOT plot in the all samples.

Reference

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