Master Thesis

A Study on Effective Barrier Height Control
with Metal Inserted Ni Silicide

Supervisor

Professor Hiroshi Iwai

Iwai Laboratory

Department of Electronics and Applied Physics

Tokyo Institute of Technology

06M36077

Yoshihisa Ohishi

LIST OF CONTENT

Chapter 4

Chapter 5

Chapter 6

Chapter 1
INTRODUCTION

1.1 Background of This Study

About a half century ago, Brattain, Bardeen and Shockley succeeded in inventing the first transistor. Then, an integrated circuit (IC) is made by killby in 1948. After the invention of the IC, the number of transistors included in a chip have increased according to Moore's law and the semiconductor technologies have accomplished   wonderful development.

CMOS (Complementary Metal Oxide Semiconductor) technology evolution in the past years has followed the path of device scaling for achieving density, speed, and power improvements. MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) scaling was propelled by the rapid advancement of lithographic techniques for delineating fine lines of 1μm width and below.

In constant-field scaling, it was proposed that one can keep short-channel effects under control by scaling down the vertical dimensions (gate insulator thickness, junction depth, etc.) along with the horizontal dimensions, while also proportionally decreasing the applied voltages and increasing the substrate doping concentration (decreasing the depletion width). This is shown schematically in Fig. 1.1. The principle of constant-field scaling lies in scaling the device voltages and the device dimensions (both horizontal and vertical) by the same factor, κ(>1), so that the electric field remains unchanged. This assures that the reliability of the scaled device is not worse than that of the original device.

Table 1.1 shows the scaling rules for various device parameters and circuit performance factors. The doping concentration must be increased by the scaling factor   κ in order to keep Poisson's

equation invariant with respect to scaling.
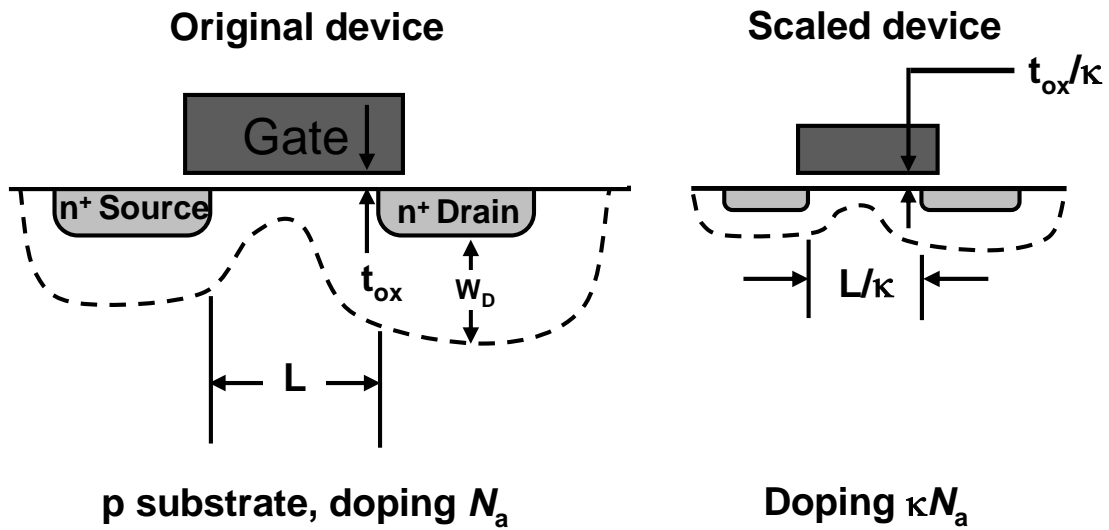
Fig. 1.1 Principles of MOSFET constant-electric-field scaling

Table 1.1 Scaling of MOSFET Device and Circuit Parameters

	MOSFET Device and Circuit Parameters	Multiplicative Factor (κ>1)
Scaling assumptions	Device dimensions(tox, L, W, χj)	$1/\kappa$
	Doping concentration (Na, Nd)	κ
	Voltage (V)	$1/\kappa$
Derived scaling behavior of device parameters	Elecric field (ξ)	1
	Carrier velocity (υ)	1
	Depletion –layer width (Wd)	$1/\kappa$
	Capacitance (C=εA/t)	$1/\kappa$
	Inversion-layer charge density (Qi)	1
	Current, drift (I)	$1/\kappa$
	CRchhannel resistance (Rch)	1
Capacitance behavior of circuit Power parameters	Circuit delay time (τ~CV/I)	$1/\kappa$
	Power dissipation per circuit (P~VI)	$1/\kappa^2$
	Power-delay product per circuit (Pτ)	$1/\kappa^3$
	Circuit density (∞ 1/A)	κ^2
	Power density (P/A)	1

The gate length of MOSFET came to be lower than 100nm since the year of 2000 and 32nm for the year of 2005 as shown in Fig.1.2 according to the ITRS roadmap 2006 update[1]. With continuous scaling of device dimensions, IC performance is becoming more and more dependent upon the parasitic series resistance of the source/drain junctions and their contacts.
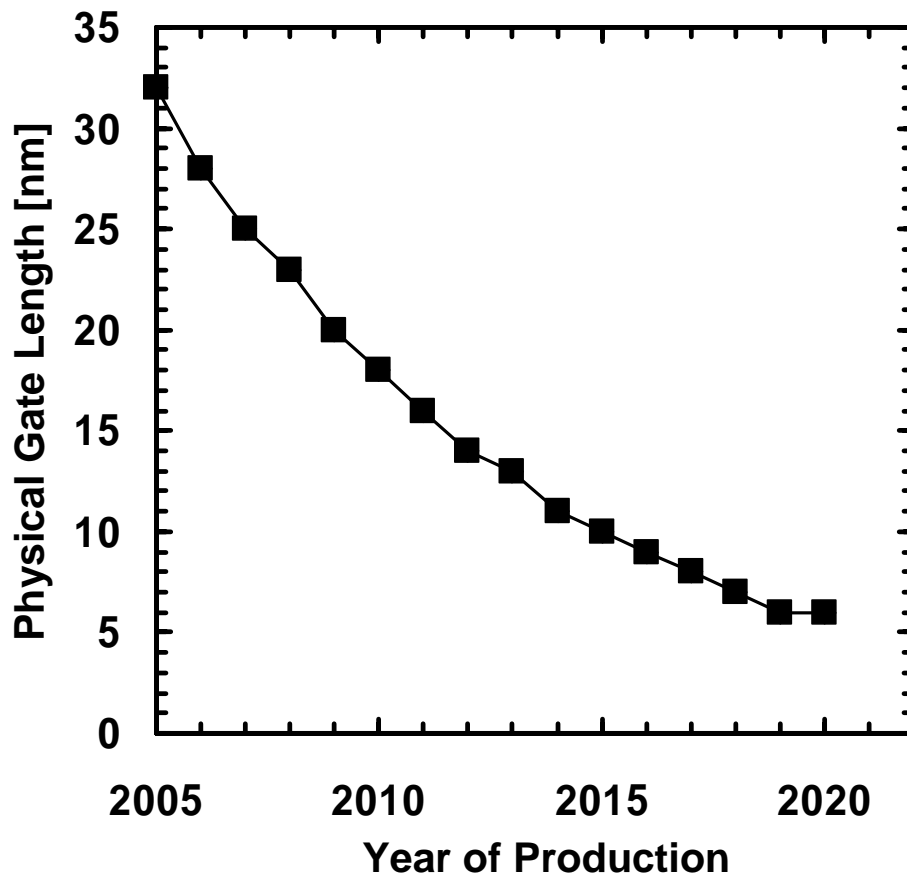

Fig.1.2 the International Technology Roadmap for Semiconductors (2006 update)

1.2 Problem of the VLSI

 The physical limit comes for the scaling. Now, the biggest problem is the scaling of the gate oxide. The scaling of gate oxide for improving MOSFET performance is required. A few nm gate oxide technique is required, but the present SiO_2 range doesn't suppress the gate leakage current. This limit is said 1.2-1.5nm. The recently research for this problem uses high-k dielectric that k is higher than the conventional SiO_2. If we use the material that k is five times, getting the same capacitance in five times oxide thickness. However, we require not only higher k but also k is higher than 10, the band is higher than 1eV, the thermal stability, single crystal or amorphous, and small defect density. The scaling of gate oxide is proceeding, it is not ignored that capacitance. That is to say, it is inversion capacitance of the channel surface and depletion conductance of polysilicon for the gate electrode. The inversion capacitance doesn't ignored. The problem of the depletion capacitance of the gate electrode is controlled the high gate impurity concentration. However, it's limit come up. Thinking for the measure is to use the polysilicon gate in stead of metal gate. The scaling has the problem of thin junction depth in source and drain range. The junction depth in source and drain for the scaling requires more shallow junction depth. But the shallow junction profile has high resistance. The source and drain high impurity concentration makes the resistance low. This problem's limit also come up.

1.3 Schottky Barrier MOSFET

 Before section, it explain that the VLSI is forced various problem and solution. For these problem

solution, the various methods suggest and experiment on. In these suggestion, schottky barrier

MOSFET is suggested by S.M.Sze in 1968 [2]. The conventional MOSFET and schottky barrier

MOSFET are shown in Fig.1.3.
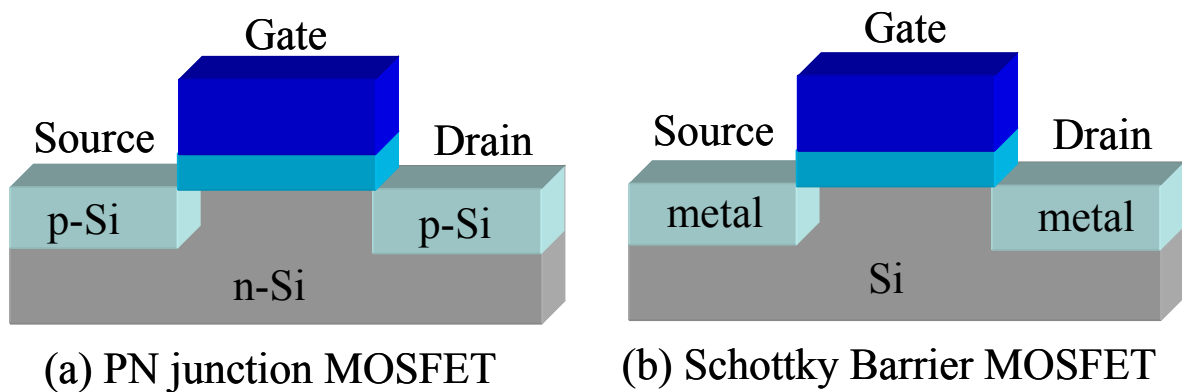
Fig.1.3 The conventional MOSFET and schottky barrier MOSFET

 The schottky barrier MOSFET adopts alloy of Si and metal that called silicide in source and drain

range. The schottky barrier MOSFET formed shottky contact in Si and silicide interface operate as

well as conventional MOSFET. The next paragraph shohws the advantages of schottky barrier

MOSFET.

 1. The scalling of MOS device is done along the Moore's low. The junction depth of the source

and drain is more thinner. However, the resistance of this part followed thin junction depth is

increase. That problem's solution is high doping concentration. However, while junction depthis

thin high doping concentration is very difficult technology. In terms of this problem, the schottky

barrier MOSFET can form thin junction for low resistivity by using silicide. High resistivity in the

source and drain renge is controled.

2. The schottky barrier MOSFET doesn't require to form diffusion range in source and drain. That

can permit scalling device area. The integration of circuit can be rised.

3. The doping in channel range don't need to control carrier by schottky barrier height. The

problem that means dispersion of impurity by short channel effect is avoided.

4. The usual CMOS has npn and pnp structures. For this reason, the parasitic transistor exists. But,

schottky barrier MOSFET is controled to inject minority carrier from drain to semiconductor, the

current gain of parasitic transistor is ignored and controlled CMOS latchup [3].

5. The usual pn junction occurs electric fields concentration in channel-drain interface. But,

schottky junction that comparable to pn junction is relaxation field effect to control impact ion. The

source range injection carrier that comparable pn junction is lowering barrier height to passage

carrier. That makes carrier injection.

6. The schottky barrier MOSFET uses wafer of SOI (Silicon On Insulto) structure to control

leakage current when off time. That is controlled the floating body effect that is problem using SOI

wafer [4].

The pn junction MOSFET is mentioned to change schottky barrier MOSFET to realize high drive

current and small consumption electric power. Now, Silicide materials for schottky barrier

MOSFET is listed table 1.2.

Silicide	Barrier height (eV)	Channel type
$ErSi_{2-x}$	0.27-0.32	N
$TiSi_2$	0.60	N,P
$CoSi_2$	0.64	N,P
NiSi	0.65-0.70	N,P
PtSi	0.87	P
IrSi	0.93	P

Table1.2 Silicide material for schottky barrier MOSFET

The characteristics of schottky MOSFET dominate the nature of peculiar to silicide called schottky barrier height. Now, different silicides such as platinum silicide for SB-PMOS and erbium silicide for SB-NMOS have been chosen for p- and n-Silicon. The reported barrier height of platinum silicide is around 0.15-0.27eV [5] for p-Si and that of erubiumu silicide is 0.27-0.36 [5]. In 2000 year, the reported schottky barrier MOSFET has 20nm gate length [6]. The schottky barrier MOSFET for adopting a conventional CMOS process required integrating p and n transistor in same wafers. To realize this request, the technology formed different kind of silicide in same wafers is required. However, that paper doesn't report.

1.4 Purpose of This Study

We report schottky barrier height moduration of NiSi with thin layer of Al, Er or Pt inter layer (0.9-3.6nm) have been examined under different annealing temperature and to evaluate the proposed barrier height modulation by fabricating schottky barrier MOSFET has SOI structure.

Chapter 2

SCHOTTKY BARRIER DIODE AND MOSFET

2.1 Schottky Diode

In the case of metal and silicon contact, the potential that is called schottky barrier height is formed metal and silicon interface that is the same commutation characteristics of pn junction. The work function of metal and semiconductor is ϕ_m and ϕ_σ ,respectively, and the electron affinity is χ . When the relationship ϕ_m ϕ_σ χ among ϕ_m, ϕ_σ and χ is defined ϕ_m ϕ_σ χ, the schottky barrier height is

$$\phi_B = \phi_m - \chi . (2.0)$$

The commutation is appeared from this potential. But, in fact the schottky barrier height is measured that doesn't depend against metal work function ϕ_m. In generalization, the dependence on work function is small against ideal it. That reason is existence interfacial trap and interfacial layer. A lot of model are suggested in relationship among Fermi level pinnning. In this case, the only ideal case is thinking. The transportation structure pass through thermal electron emission get over the potential and tunneling structure pass through schottky potential as shown in Fig. 2.1.
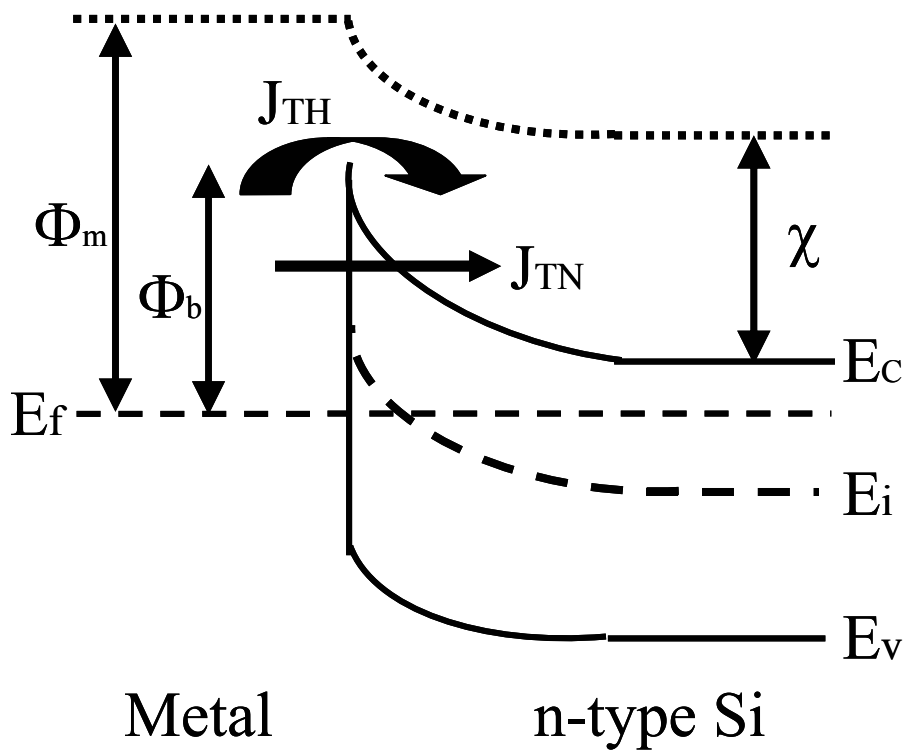
Fig2.1 schematic illustration of schottky diode band diagram [7]

2.1.1 Thermal electron emission structure

It is mentioned thermal emission structure. First of all, The electron current j_2 think about from semiconductor to metal as shown in Fig.2.2. The electron doesn't collision in distance of space electron charge layer. The electron current pass over this layer to metal. The electron emission metal is higher electron energy than E_0 as shown Fig. 2.2.
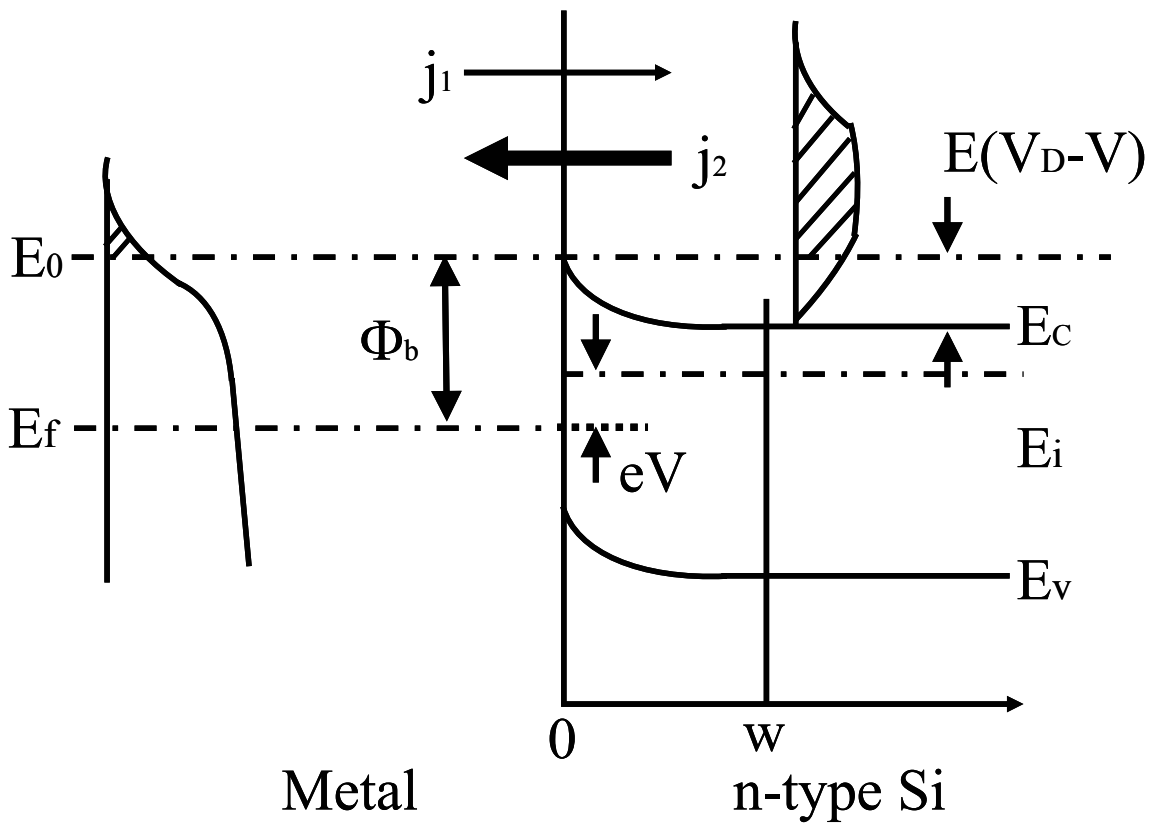
Fig 2.2 schematic illustration of rectification of schottky contact [7]

$$j_2 = -\int v_x \, dn = -\int_{j_x > 0} V_x \cdot Z(E) f(E) dE$$

$$= -\int_0^\infty \int_{-\infty}^\infty \int_{-\infty}^\infty v_x \cdot 2 \frac{1}{8\pi^3} \cdot f(E) dk_x dk_y dk_z$$

$$= -\frac{1}{4\pi^3} \int_0^\infty \int_{-\infty}^\infty \int_{-\infty}^\infty v_x \left\{ \exp\left(-\frac{E - E_f}{kT} \right) \right\} dk_x dk_y dk_z \quad (2.1)$$

But, Z(E) is state density of electron, f(E) is distribution function of electron, v_x is velocity element

of x direction of electron, and m_e* is actual mass of electron in semiconductor. The v_x is written

$$v_x = \frac{\hbar k_x}{m_e^*}. \quad (2.2)$$

$$E = E_0 + \frac{\hbar}{2m_e^*} (k_x^2 + k_y^2 + k_z^2) \quad (2.3)$$

The equation (2.1) is equal to

$$j_2 = -\frac{1}{4\pi^3} \int_0^\infty \int_{-\infty}^\infty \int_{-\infty}^\infty \frac{\hbar k_x}{m_e^*} \exp\left\{ -\frac{\hbar^2 (k_x^2 + k_y^2 + k_z^2)}{2m_e^* kT} \right\} \left\{ \exp\left(-\frac{E_0 - E_f}{kT} \right) \right\} dk_x dk_y dk_z$$

$$= -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{E_0 - E_f}{kT}\right) \quad (2.4)$$

The semiconductor side is defined

$$E_0 - E_f = \phi_m - \chi - qV \quad (2.5)$$

$$\phi_B = \phi_m - \chi. \quad (2.6)$$

The current pass through from semiconductor to metal is

$$j_2 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B - qV}{kT}\right) \quad (2.7)$$

And, the current from metal to semiconductor is $\phi_m - \chi - qV$ replaced by $\phi_m - \chi$.

$$j_1 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \quad (2.8)$$

The net current is

$$j_2 - j_1 = -\frac{4\pi m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \exp\left\{\left(\frac{qV}{kT}\right) - 1\right\}. \quad (2.9)$$

and current density is

$$j_{TH} = -\frac{4\pi q m_e^* k^2 T^2}{h^3} \exp\left(-\frac{\phi_B}{kT}\right) \exp\left\{\left(\frac{qV}{kT}\right) - 1\right\}. \quad (2.10)$$

The current about thermal emission structure is

$$j_{TH} = J_0 \exp\left\{\left(\frac{qV}{nkT}\right) - 1\right\} \quad [8]. \quad (2.11)$$

$$j_0 = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \quad (2.12)$$

$$A^* = \frac{4\pi q m_e^* k^2}{h^3}. \quad (2.13)$$

A* is Richardson constant, k is Bltzmann's constant, h is Planck's constant and T is absolute

temperature. The n that is called ideal factor is n=1 in ideal schottky contact, but in fact n>1. The

reason of it is transport current in diffusion current, bias dependence of schottky barrier height in

image force, injection of minority carrier, and dependence of schottky barrier in interfacial trap. The

ϕ_b is written as

$$\phi_B = \frac{kT}{q} \ln\left(\frac{A^* T^2}{J_0}\right). \quad (2.14)$$

The ϕ_b can be looked for I-V measurement of schottky diode. The other method for look for

schottky barrier height is relationship depletion capacitance and bias current.

2.1.2 Tunneling Structure

Next, it is thinking about Tunneling structure. The tunneling is gave next equation [9]

$$J_{TN} = \frac{q^2 F^2}{8\pi h \phi_B} \exp\left[-\frac{8\pi}{3hqF} \sqrt{2m_e^* (q\phi_B)^3} \right]. \ (2.15)$$

But, F is field electric of vertical direction of semiconductor surface. The image of the image charge is added in schottky barrier ϕ_b

$$\phi_B = \phi_{B0} - \sqrt{\frac{qF}{4\pi\varepsilon}}. \ (2.16)$$

The ϕ_b is schottky barrier height when the field electric is not added, and the ε is silicon permittivity. The phenomenon that is lowered schottky barrier height in electric field is called schottky effect. The current in schottky interface expresses the sum of thermal emission current and tunneling current

$$J_{total} = J_{TH} + J_{TN}. \ (2.17)$$

2.1.3 Space Charge capacitance of schottky contact

The space charge capacitance of schottky contact can think a kind of capacitor as well as pn junction. That has electric capacitance. If the potential in paint x is φ(x), Poisson's equation is

$$\frac{d^2\varphi(x)}{dx^2} = -\frac{qN_D}{\varepsilon_0\varepsilon_S} . \quad (2.18)$$

The (2.18) is done integral is

$$\frac{d\,\varphi(x)}{dx} = -\frac{qN_D}{\varepsilon_0\varepsilon_S}x + C_1 \quad (2.19)$$

$$\varphi(x) = -\frac{qN_D}{\varepsilon_0\varepsilon_S}x^2 + C_1 + C_2 . \quad (2.20)$$

The x axis express Fig.2.2,and beginning condition is φ(x)= φ₀=0 when x is equal to 0.

$$C_2 = 0 \quad (2.21)$$

x=w, and dφ(x)/dx=0

$$C_1 = -\frac{qN_D}{\varepsilon_0\varepsilon_S}w . \quad (2.22)$$

The potential is

$$\varphi(x) = \frac{qN_D}{\varepsilon_0\varepsilon_s}\left(wx - \frac{x^2}{2}\right). \quad (2.23)$$

x=w, and $\varphi(w)=V_D-V$

$$w = \left\{\frac{2\varepsilon_0\varepsilon_s(V_0 - V)}{qN_D}\right\}^{\frac{1}{2}}. \quad (2.24)$$

The electrostatic capacitance is

$$C = \frac{\varepsilon_0\varepsilon_s}{w} = \left\{\frac{q\varepsilon_0\varepsilon_S N_D}{2(V_D - V)}\right\}^{\frac{1}{2}} \quad (2.25)$$

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_0\varepsilon_s N_D}(V_D - V). \quad (2.26)$$

The N_D and V_D can be search, if the function of $1/C^2$ versus bias V.

Chapter 3

FABRICATION AND CHARACTERIZATION METHODS

3.1 Experimental Procedure

3.1.1 Si Substrate Cleaning Process

At first, high quality thin films require ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩcm at 25$^\text{o}$C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩcm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the Si substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The first step, which use a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4: H_2O_2=4:1), was performed to remove any organic material and metallic impurities. After that, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:99). Then the cleaned wafer was dipped in DI water. Finally, the cleaned Si substrate was loaded to chamber to deposit as soon as it was dried by air gun.

3.1.2 UHV-Sputtering System

After cleaned by chemicals, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive except Ni.) and Ni/Si were formed by an UHV-sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. It is performed by applying a high voltage across a low-pressure gas (usually argon at about 5 millitorr)to create a "plasma," which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike a "target," composed of the desired coating material, and cause atoms from that target to be ejected with enough energy to travel to, and bond with the substrate.

An UHV-sputtering system is used for thin film formations of electronic devices, for experiments of GMR, and for creating new materials of high temperature superconductors. In this study, UHV Multi Target Sputtering System ES-350SU shown as Fig.3.1 was conducted. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. As for other details, Table 3.1 is attached for reference.
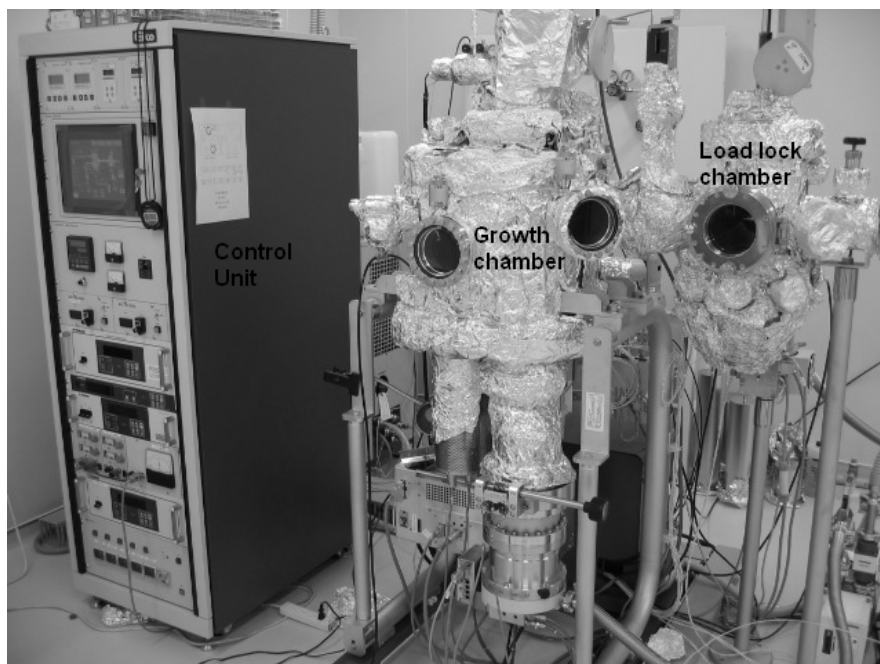
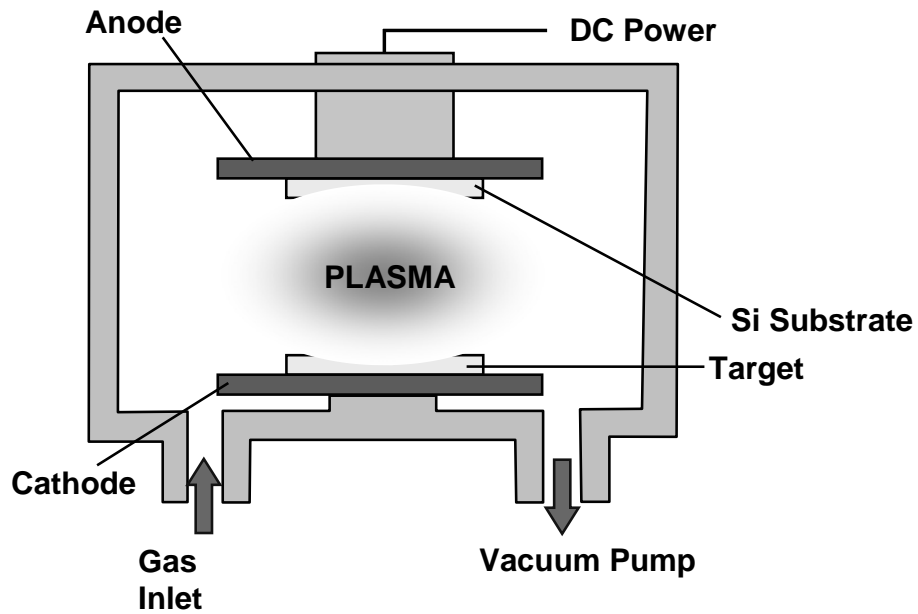Fig. 3.1 Photo of UHV Multi Target Sputtering System ES-350SU

Fig. 3.1 structure of UHV sputtering system

Table 3.1 Specifications for UHV Multi Target Sputtering System ES-350SU

Growth chamber	1. Ultimate pressure	1.5×10^{-6}Pa
	2. Substrate size	2 inch in diameter
	3. Heating temperature	600ºC
	4. Heater type	Lamp type heater
	5. Target	3 inch x 5 pieces (motor-driven)
Load lock chamber	6. Vacuum pumps	TMP 500L/sec and RP 250L/min
	7.Ultimate pressure	6.6×10^{-5}Pa
	8. Vacuum pumps	TMP60L/sec and RP90L/min
	9. Substrate holder with cooling function / Substrate holder with heating function /Cleaning function / Radical beam source	

3.1.3 Infrared Annealing Furnace

After formation from UHV sputtering system, thin films of Ni/Si, Ni/M/Si, M/Ni/Si were moved to annealing furnace to hold thermal process.

In order to obtain high quality films, annealing process after deposition is required. The annealing after deposition is considered to bring the suppression of leakage current because of the defects in the films and surface roughness. In this study, thermal process leads to the reaction of Ni with Si.

The equipment for annealing used in this investigation was QHC-P610CP (ULVAC RIKO Co. Ltd). Fig. 3.2 is the photo of the infrared annealing furnace, whose schematic illustration was shown as Fig. 3.3. The annealing was performed by six infrared lamps surrounding the sample stage which were made of carbon and coated by SiC. The heating temperature was controlled by thermocouple feedback.
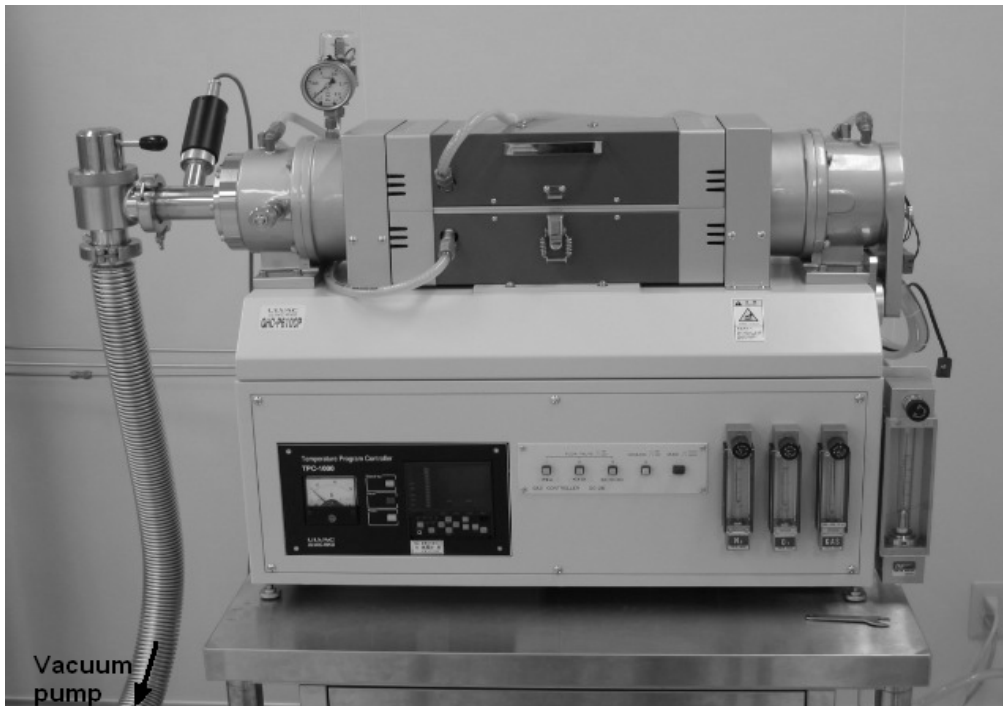
Fig. 3.2 Photo of infrared annealing furnace
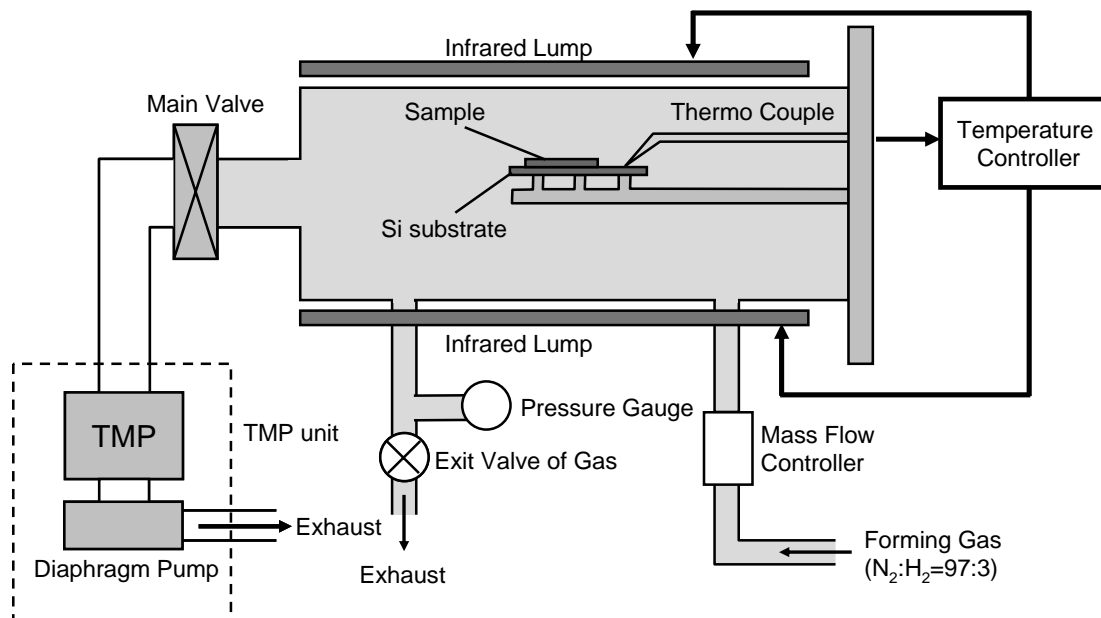
Fig. 3.3 schematic image of infrared annealing furnace

3.2 Measurement Methods

3.2.1 Transmission Electron Microscope (TEM)

Cross-section TEM image is the most important analysis method to characterize physical thickness, film quality and interface condition.

Fig.3.4 Shows TEM system. First, focus lenses change convergent angle and beam size. The electron beam transmitted through the thin fragment sample passes objective lens and projective lens, and finally projected on fluorescent screen. Recording oh the image is performed by direct exposure on exclusive film for electron microscope set lower part of the fluorescent screen.

Electron interacts strongly with lattice by scattering. Thus, sample has to be very thin fragment. Required thickness of the sample is 5 to 500 nm at 100 kV. TEM images are obtained in very high resolution such as 0.2 to 0.3 nm at 200 kV.

Electron gun

Focus lens

Sample

Objective lens

Projecting lens

Magnified image
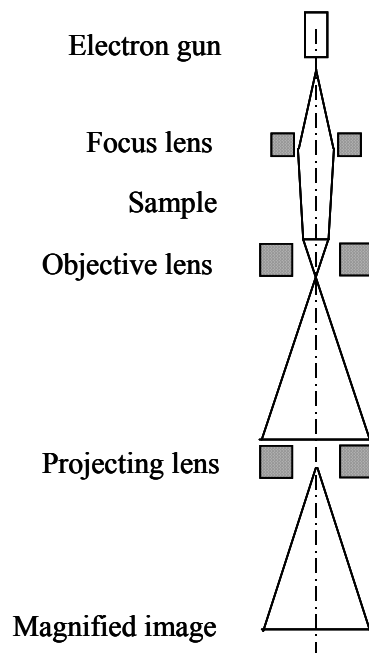
Fig.3.4 schematic diagram for TEM (Transmission Electron Microscopy) observation. Several magnetic lenses are used to magnify the object image

3.2.3 Rutherford Backscattering Spectroscopy (RBS)

Rutherford backscattering spectrometry (RBS) is based on bombarding a sample with energetic ions-typically He ions of 1 to 3 MeV energy-and measuring the energy of the backscattered ions. It allows determination of the masses of the elements in a sample, their depth distribution over distance from 100 angstrom to a few microns from the surface, and crystalline structure in a non-destructive manner.

Fig.3.5 shows RBS schematic. Ion of mass M_1, atomic number Z_1, and energy E_0 are incident on a solid sample or target composed of atoms of moss M_2 and atomic number Z_2. Most of the incident ions come to rest within the solid losing their energy through interactions with valence elements. The incident ions lose energy, traversing the sample until they experience a scattering event and then lose energy again as they travel back to the surface leaving the sample with reduced energy. For those incident ions scattered by surface atoms, conservation of energy and momentum leads to a relationship of their energy after scattering E_1 to the incident energy E_0 through the kinematic factor K

$$K = \frac{E_1}{E_0} = \frac{\left(\sqrt{1-(R\sin\theta)^2} + R\cos\theta\right)^2}{(1+R)^2} \approx 1 - \frac{2R}{(1+R)^2}(1-\cos\theta)$$

where R= M_1/M_2 is the scattering angle. The kinematic factor is a mesure of the primary ion energy loss. The unknown mass M_2 is calculated from the measured energy E_1 though the kinematic factor.
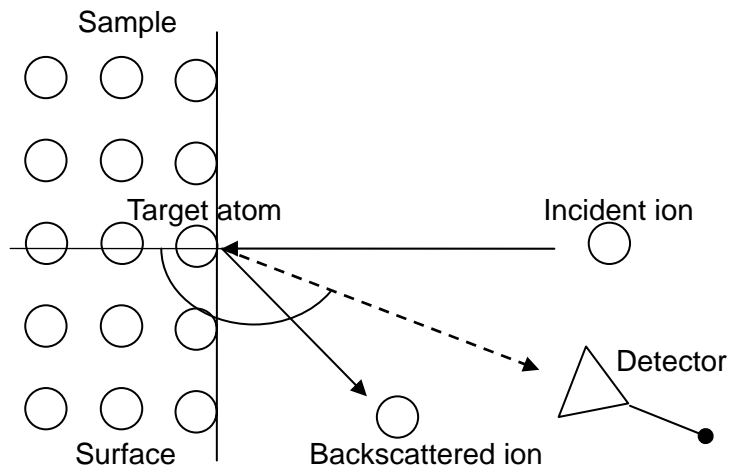
Fig. 3.5 Rutherford backscattering schematic

3.2.3 Auger Electron Spectroscopy (AES)

Auger Electron Spectroscopy (*Auger spectroscopy* or AES) is a surface specific technique utilizing the emission of low energy electrons in the *Auger process* and is one of the most commonly employed surface analytical techniques for determining the composition of the surface layers of a sample. The Auger electron is a secondary electron discharged to a vacuum by a process shown for Fig.3.6. The Auger effect occurs because the incident electrons can remove a core state electron from a surface atom. This core state can be filled by an outer shell electron from the same atom, in which case the electron moves to a lower energy state, and the energy associated with the transition is the difference in orbital energies. This energy must be released in some fashion. In some cases this energy is imparted to a second outer shell electron, which then is ejected from the atom. The characteristic energy of this ejected electron is

$$E_{Core\ State} = E_{S1} + E_{S2}$$

where S1 and S2 are the outer shell states. Because these orbital energies are determined by the element of the atom, the composition of a surface can be determined. When a primary electron beam was irradiated on the sample surface, an incidence electron activates an electron of an inner shell of a sample atom, and a cavity is made.
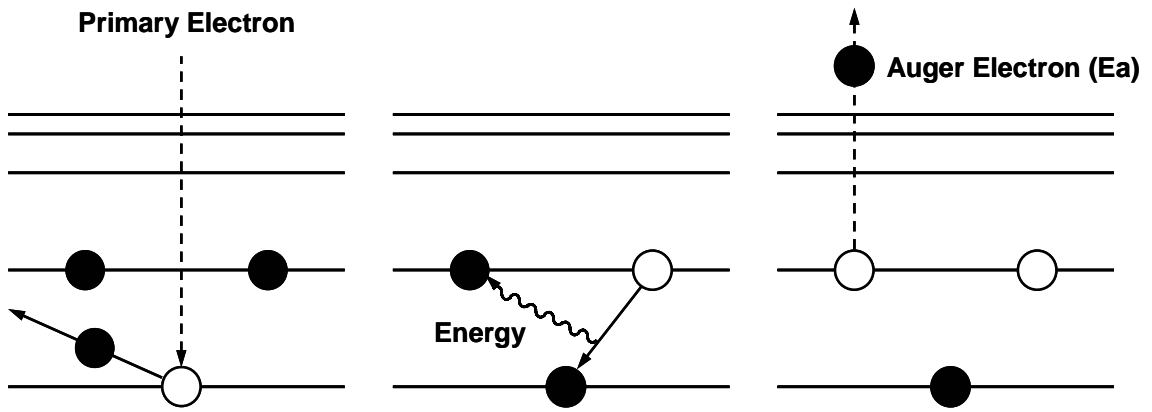
Fig. 3.6. Principle of AES

3.2.4 J-V (Leakage Current Density – Voltage) Measurement

To estimate the leakage current density, *J-V* characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard.).

3.2.5 Evaluation of Schottky Barrier Height Based J-V Characteristics

When, the case of V>>kT/q, the index term is more larger than 1, it can be ignored. The current density (**J**) of schottky contacts is defined

$$J = J_0 e^{qV/kT} . \text{(3.1)}$$

However, the current density of getting actual characteristics increases the index function against bias voltage. The increasing rate is less than (3.1). Therefore, the ideal factor (**n**) is used as same as pn junction

$$J = J_0 e^{qV/nkT} . \text{(3.2)}$$

If n is equal to 1, (3.2) accords with (3.1), and the current density flows along theory, but usually *n*>1.

Another, J_0 is expressed

$$J_0 = A^* T^2 e^{-\phi_B / nkT} = \frac{4\pi q m_e^* k^2 T^2}{h^3} e^{-\phi_B / kT}. \ (3.3)$$

A^*, k and m^*_e are Richaldson constant, Boltman's Constant and effective mass. From (3.3), ϕ_B

can be got from J_0.

Chapter 4

CHARACTERISTICS
OF
Ni Silicide SCHOTTKY DIODE

4.1 Ni Silicide Schottky Diode by Using Al, Pt or Er

4.1.1 Introduction

Self-aligned silicidation is one of the key technologies in the state-of-art complementary metal-oxide-semiconductor (CMOS) process to make Ohmic or Schottky contacts at source/drain and gate. Amongst of them, Ni silicide has emerged as a leading choice in Si nanometer electronics due to its low resistivity and high scalability. Recently, Schottky barrier source/drain metal-oxide-semiconductor field-effect transistors (MOSFETs) have been receiving a lot of attention because of the lower parasitic series resistance at source/drain, possible zero junction depth and simpler fabrication process [10-13]. However, for a typical Schottky barrier (SB) MOSFET, the on-current of SB-MOSFET could be increased substantially [13]. NiSi has an experimental SBH of 0.65 eV on n-Si(100). This high SBH value hinders the application of NiSi in SB-MOSFETs. If we can lower the SBH of silicides to very low value, the device exhibits the same intrinsic performance as conventional MOSFET but also benefits from the advantages of SB-MOSFETs mentioned above.

In this chapter, we report a new Schottky-barrier-height modulation method for Ni silicide by inserting a thin Al, Er or Pt and Pt and B interlayer before silicidation process.

4.1.2 Fabrication process of schottky diode

Schottky diodes were formed on SiO_2 isolated n- and p-type bulk (100) Si wafers (doping concentration: 1.0×10^{15} cm^{-3}), as shown in Fig. 4.1. Before metal deposition, the patterned wafers were cleaned in mixed solution of H_2SO_4 and H_2O_2 followed by chemical oxide removal by diluted HF. Metals were deposited subsequently by DC sputtering in Ar gas at a pressure of 5.0×10^{-1} Pa. The layered structures of Ni/Al/Si, Ni/Pt/Si and Ni/Er/Si with 100-nm-thick Ni layer and the Al,Pt or Er layer thicknesses ranging from 0.9 to 3.6 nm were deposited. Ni (100 nm)/Si, Er (100 nm)/Si and Pt (100 nm)/Si structures were also deposited as references. The samples were annealed in forming gas (3% H_2 + N_2) at various temperatures from 300°C to 700°C for 1 min. After the removal of un-reacted metals by chemical etching, Al back contacts were formed by thermal evaporation. The Schottky barrier heights of the fabricated diodes were evaluated form current voltage characteristics. The structures of the formed silicide films were also analyzed by Aujer Electron Spectroscopy (AES), transmission electron microscope (TEM), energy dispersive X-ray spectroscopy (EDX) and Rutherford backscattering spectroscopy (RBS).

● Field thermal oxidation (~200nm)

● Active area patterning

● SPM, HF-last

● Metal sputtering
(Ni:100nm, Al,Pt or Er :0.9-3.6nm)

● Rapid thermal annealing (RTA)
(F.G ambient, 300-700°C,1min)

● Metal etching

● Back side electrode formation
(Aluminum evaporation)
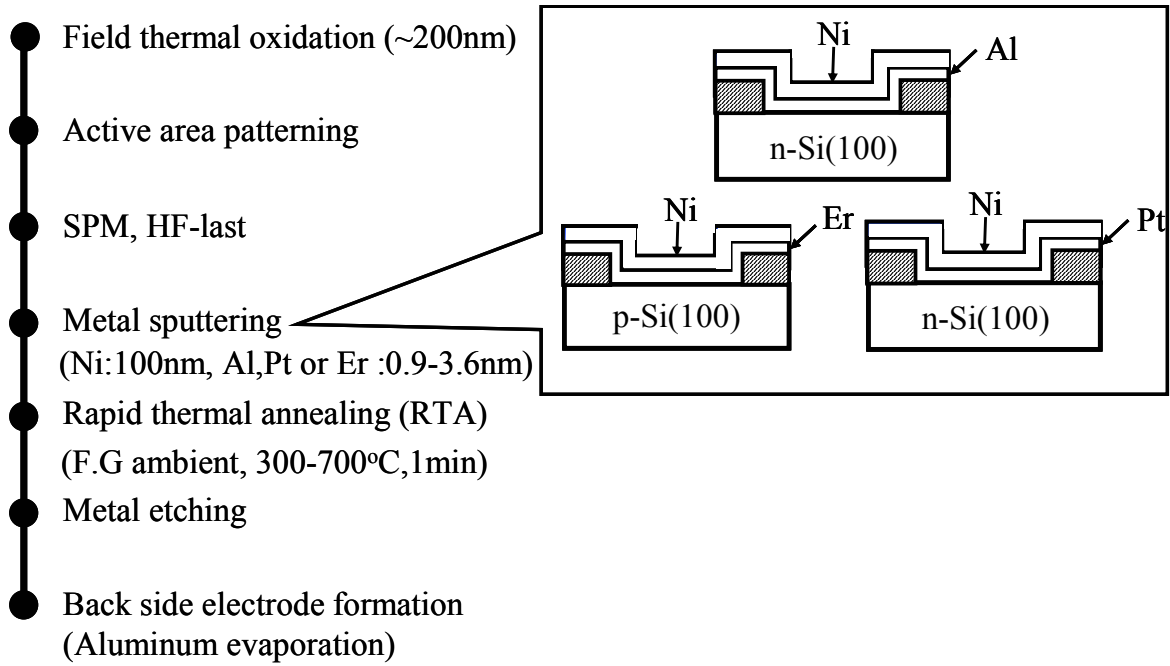
Fig.4.1 Fabrication process of the Schottky barrier diodes from the initial structures of Ni/Al/n-Si, Ni/Er/p-Si and Ni/Pt/n-Si.

4.1.3 Characteristics of Ni silicide schottky diode

Φ_b of the Ni(100nm)/p-Si and Ni(100nm)/n-Si structures Φ_b were evaluated from the *I-V* curves in the forward bias region. The obtained Φ_b values are plotted against the annealing temperatures in Fig. 4.2 (a) and (b). The observed Φ_b values for holes were 0.37-0.43eV in the annealing temperature range of 300-700°C. The observed Φ_b values for electrons were 0.55-0.62eV in the annealing temperature range of 300-700°C.

(a)

(b)
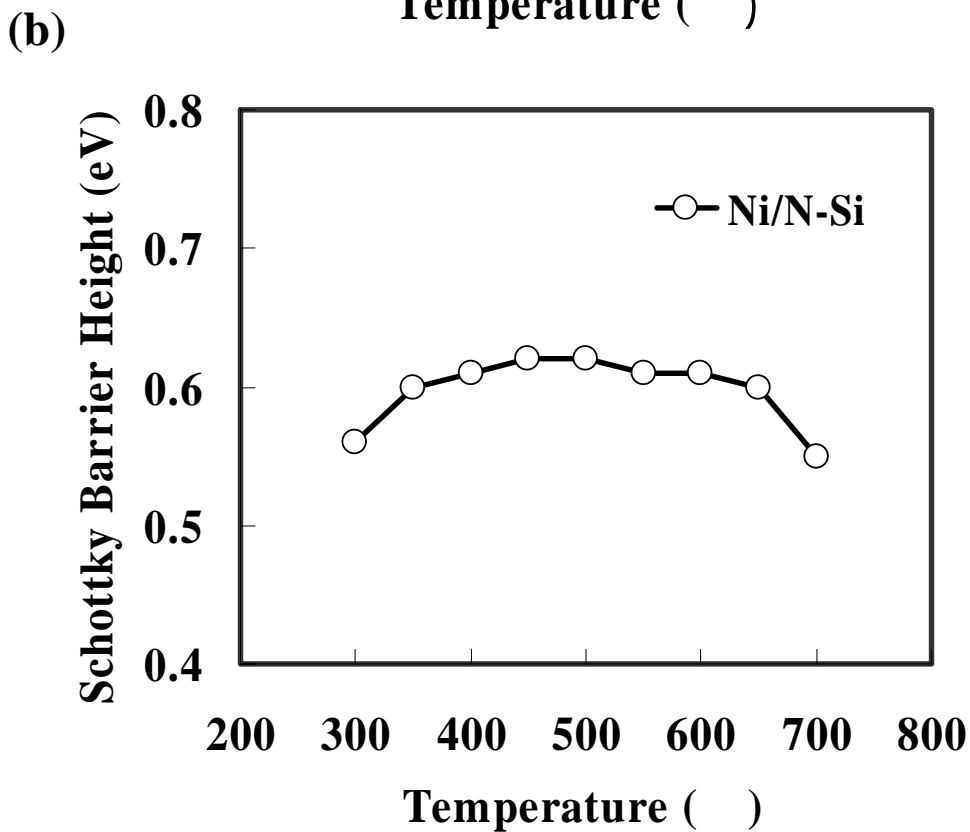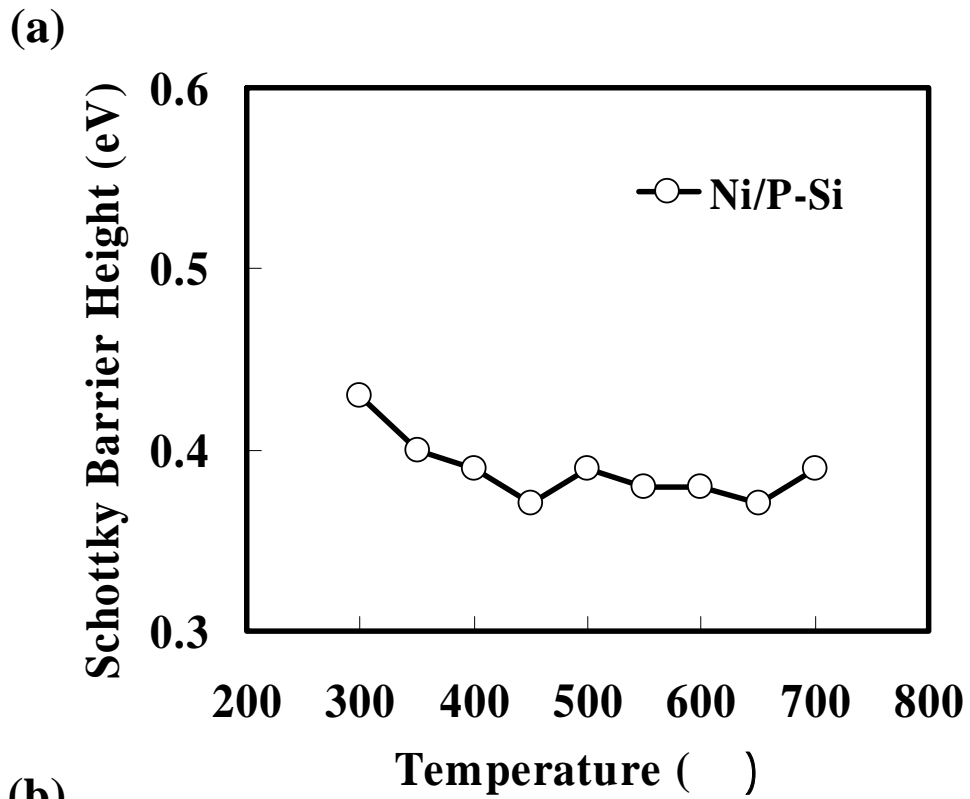
Fig.4.2 Annealing temperatures dependence of Scottky barrier heights for the diodes for the diodes formed from the initial structures of Ni/p-Si and Ni/n-Si.

4.1.4 Characteristics of Ni silicide schottky diode by using Pt or Er

Typical current-voltage (*I-V*) curves of Schottky diodes of annealing temperature from 300°C to 700°C fabricated from the Ni/Al/n-Si, Ni/Er/p-Si and Ni/Pt/n-Si structures are shown in Fig. 4.3-4.11. Φ_b was evaluated from the *I-V* curves in the forward bias region. The obtained Φ_b values are plotted against the annealing temperatures in Fig. 4.12.

In the case of the Al insertion, observed Φ_b values for holes were as the same value as the Ni silicide without the Al insertion, in the annealing temperature range of 300-700°C as shown Fig.4.12(a). This means that the Al t insertion is not favorable for n-type MOSFETs because the Φ_b for holes cannot be lowered.

In the case of the Er insertion, observed Φ_b values for holes were higher by 0.03-0.12eV from the value for the Ni silicide without the Er insertion, in the annealing temperature range of 300-700°C as shown Fig.4.12(b). This means that the Er insertion is favorable for n-type MOSFETs because the Φ_b for electrons can be lowered. The values of Φ_b depended on the annealing temperature while not on the inserted Er thickness.

In the case of Pt insertion, observed Φ_b values for electrons were higher by 0.08-0.2eV from the value for Ni Silicide without the Pt insertion, in the annealing temperature range of 300-700°C as shown Fig.4.12(c). This means that the Pt insertion is favorable for p-type MOSFETs because the Φ_b for holes can be lowered.
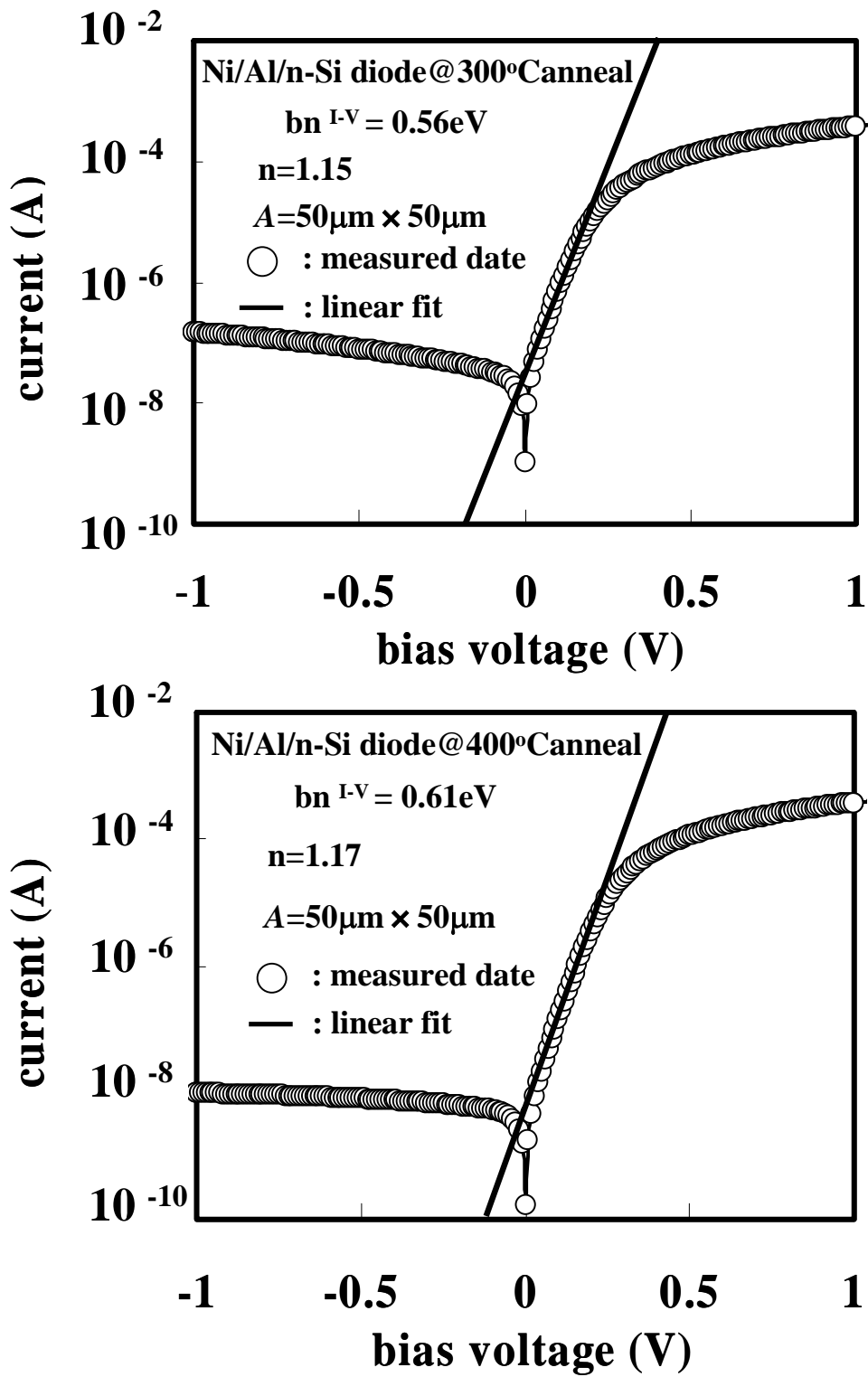
Fig.4.3 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Al(3.6nm)/n-Si at annealing temperatures of 300°C and 400°C.
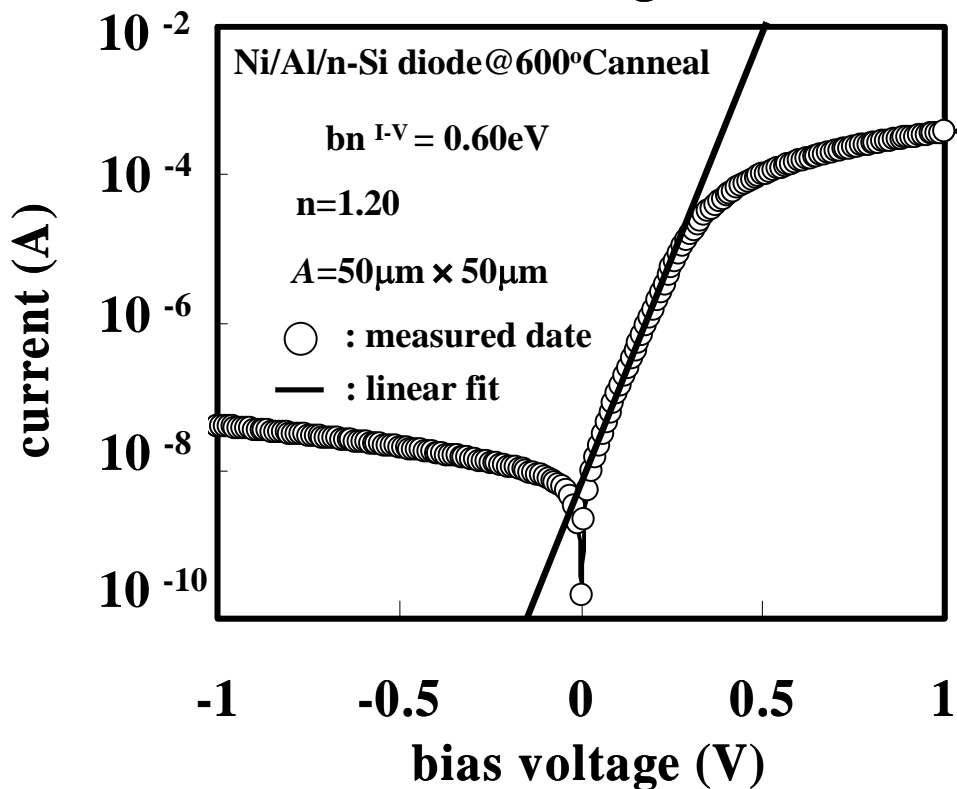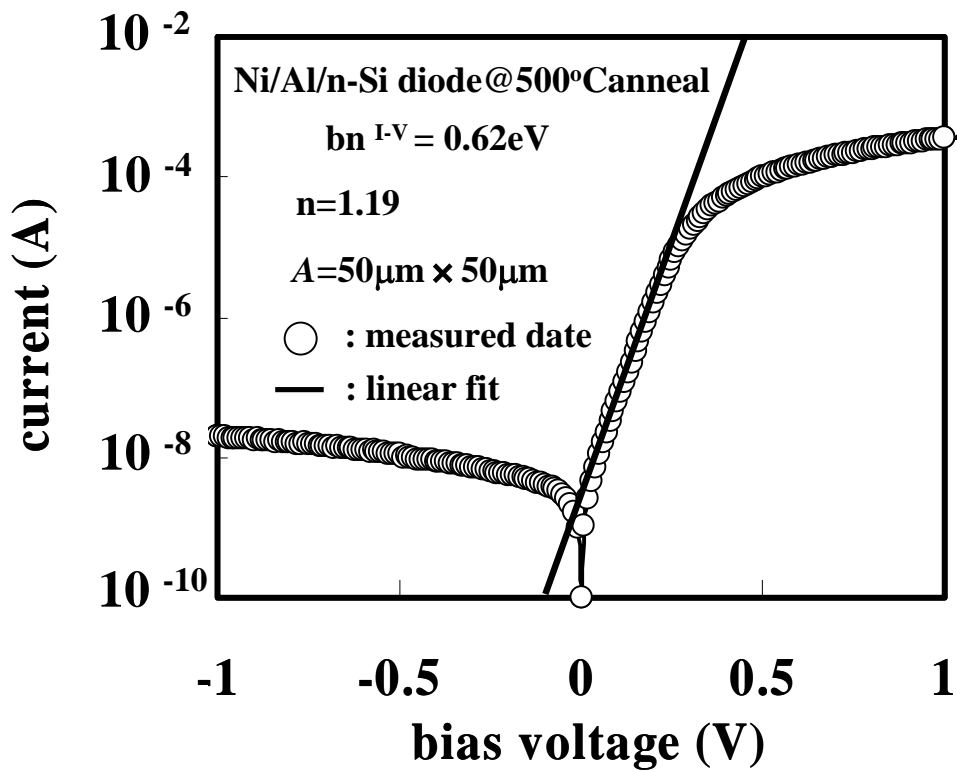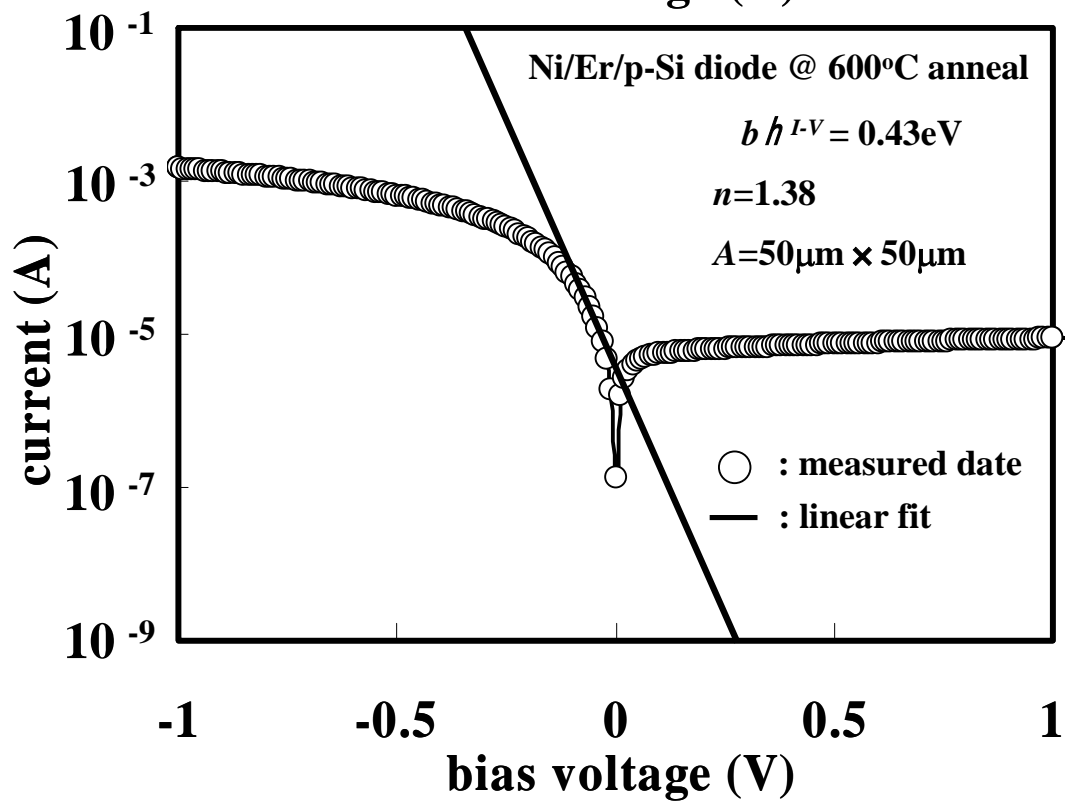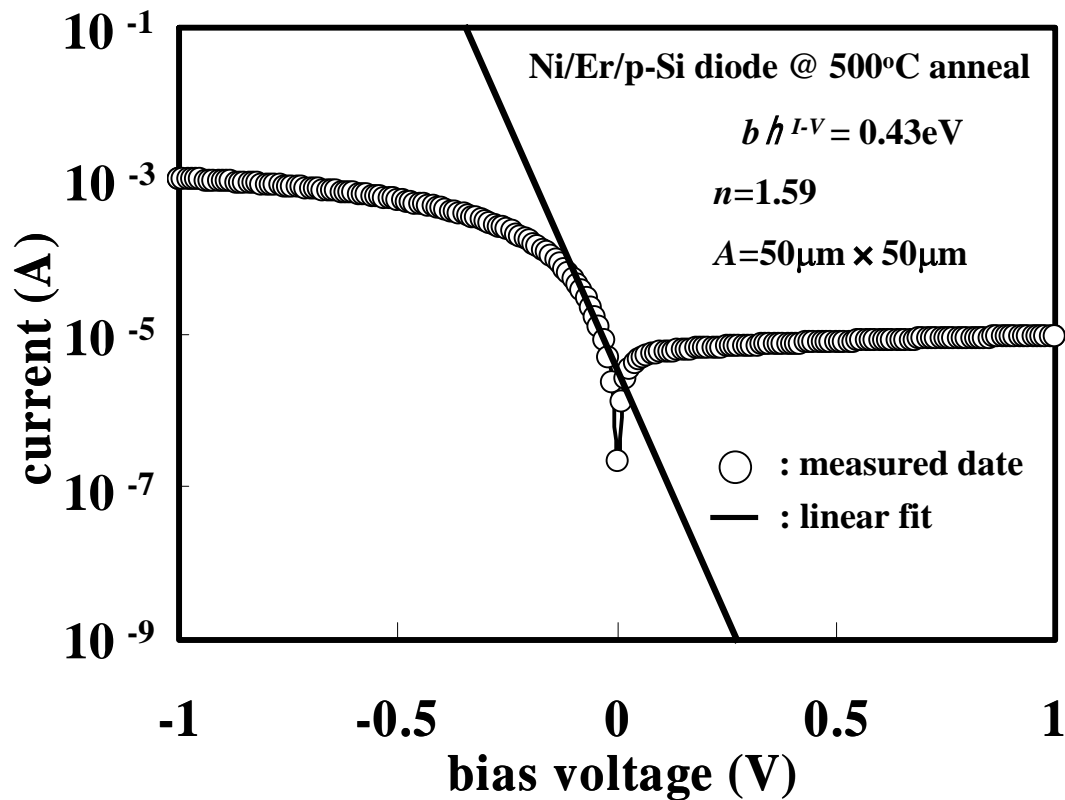
Fig.4.4 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Al(3.6nm)/n-Si at annealing temperatures of 500°C and 600°C.
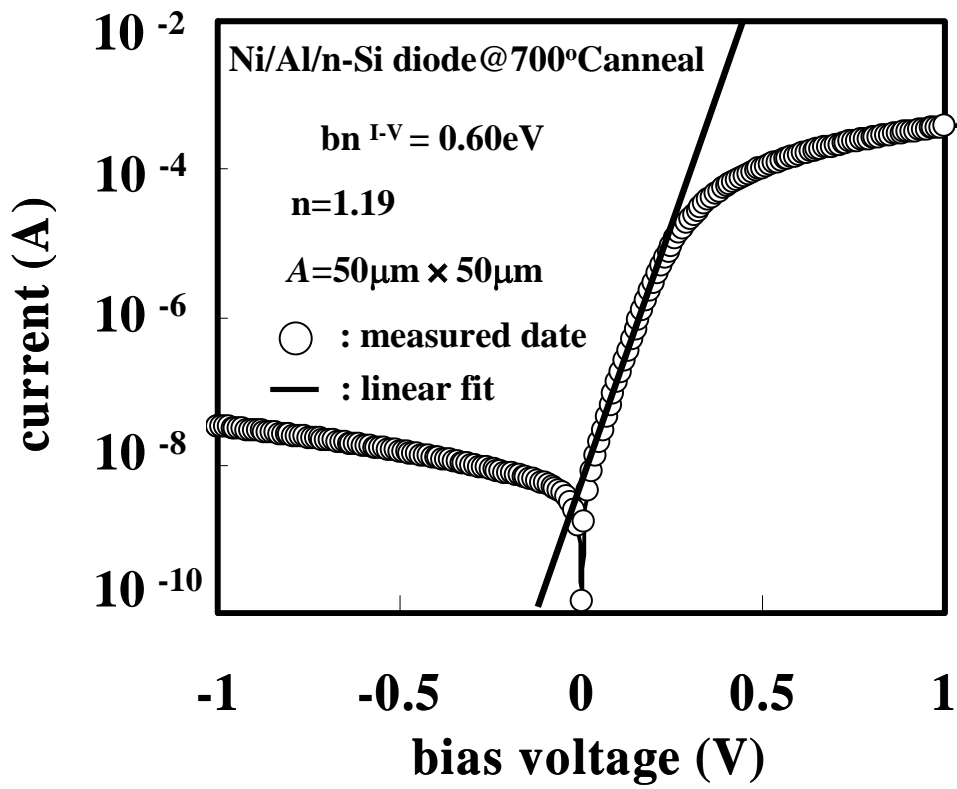
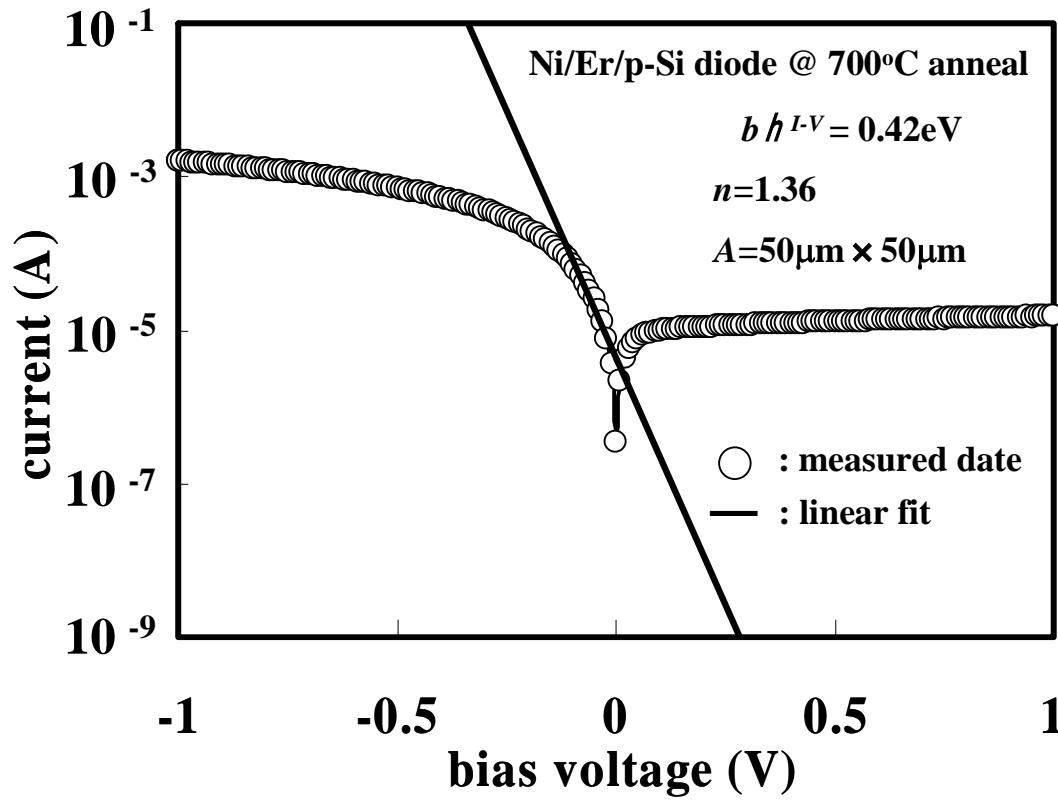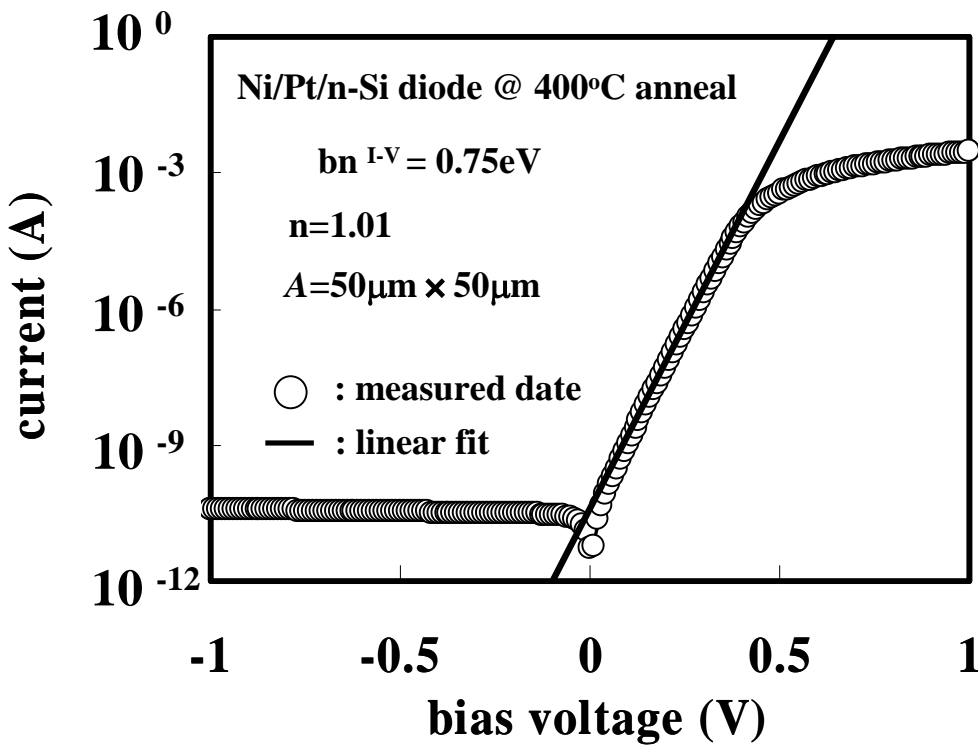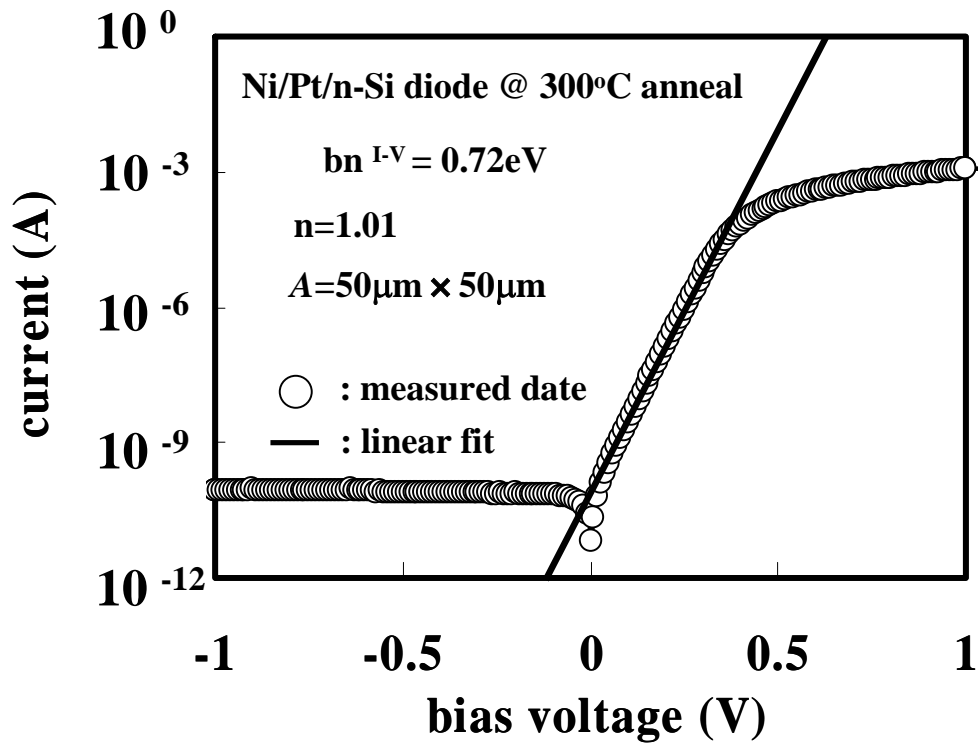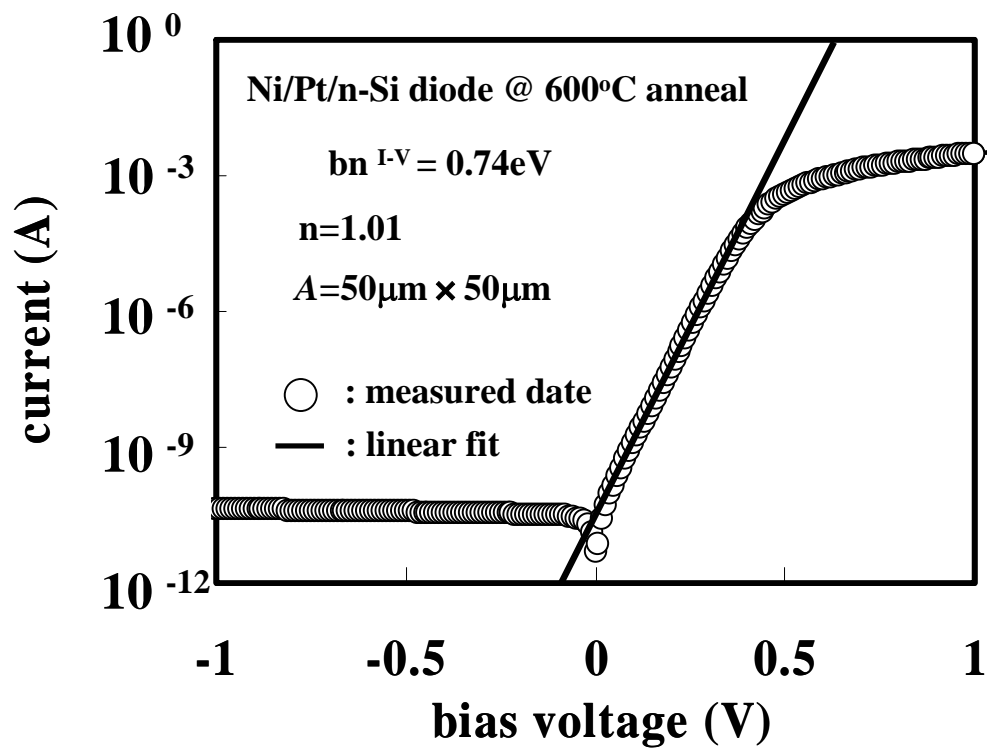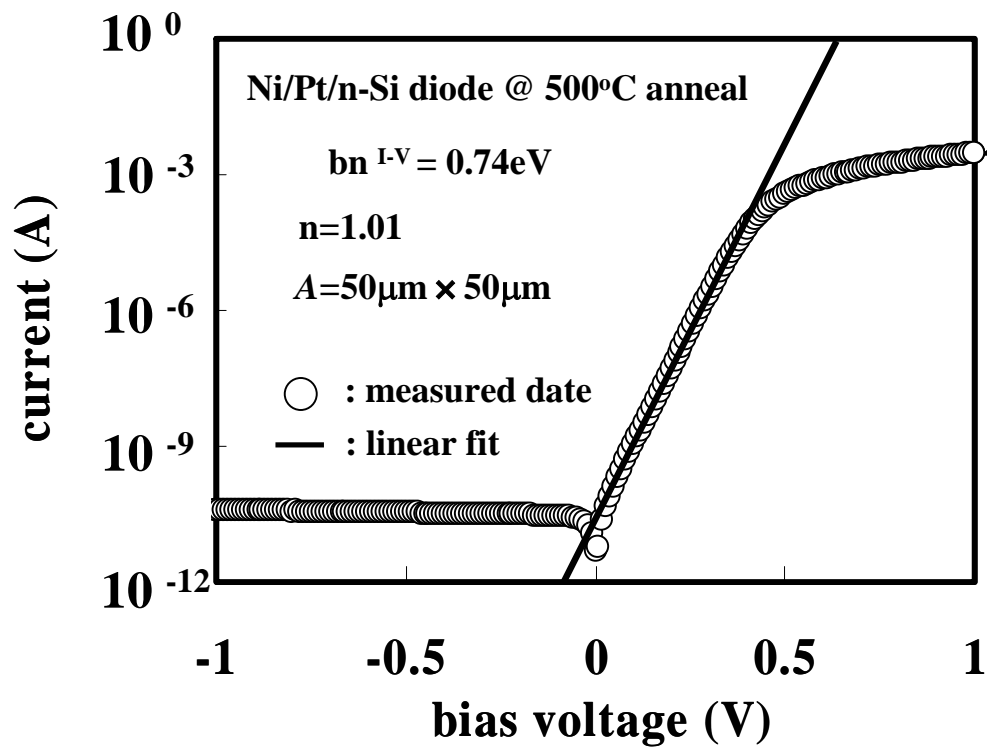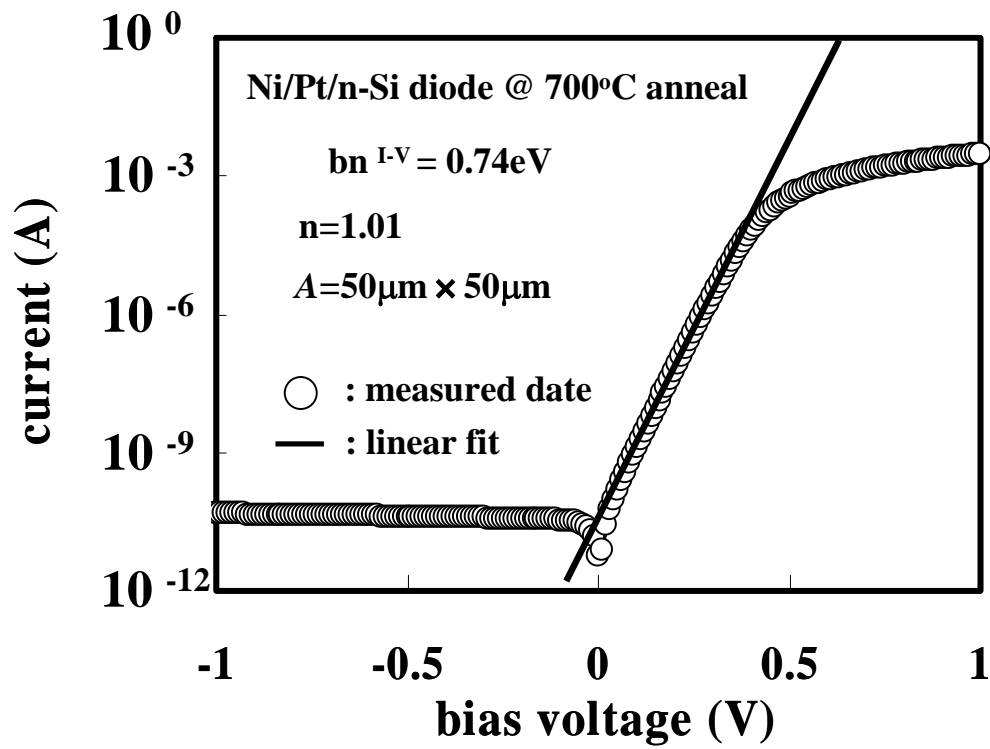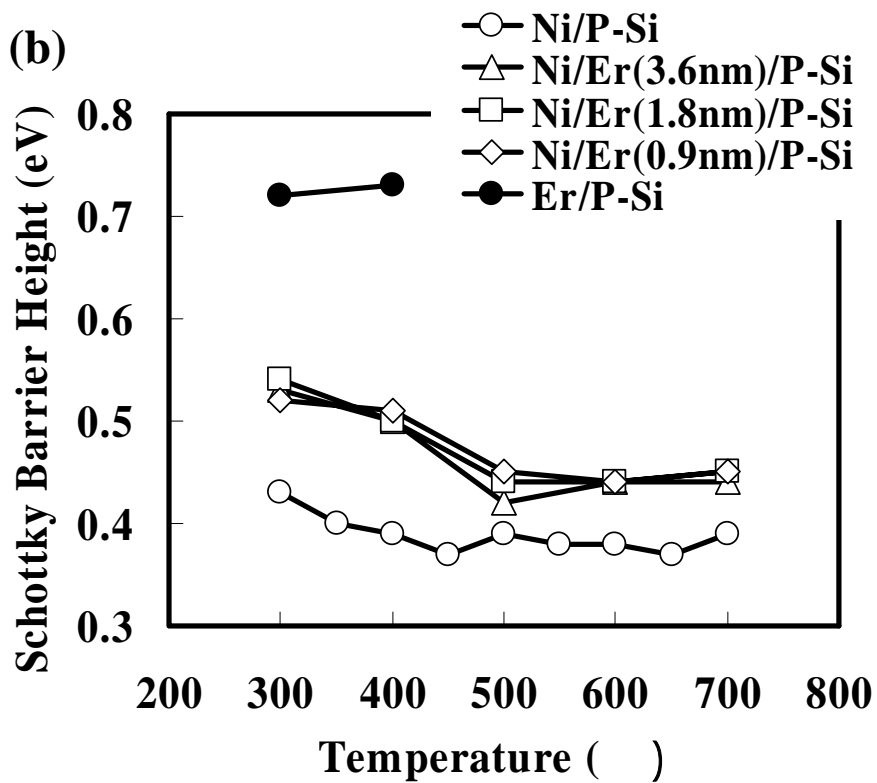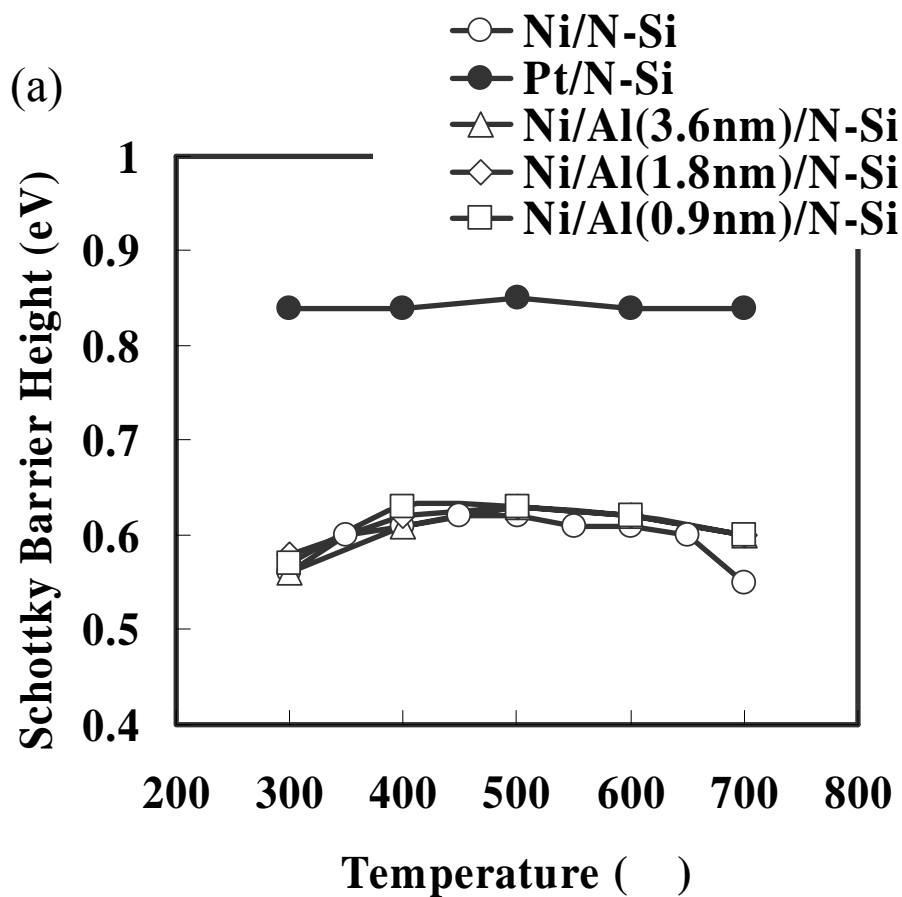Fig.4.5 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Al(3.6nm)/n-Si at annealing temperatures of 700°C.

Fig.4.6 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Er(3.6nm)/p-Si at annealing temperatures of 300°C and 400°C.

Ni/Er/p-Si diode @ 500°C anneal

$b^{I-V} = 0.43\text{eV}$

$n=1.59$

$A=50\mu\text{m}\times 50\mu\text{m}$

◯ : measured date
— : linear fit

current (A)

bias voltage (V)

Ni/Er/p-Si diode @ 600°C anneal

$b^{I-V} = 0.43\text{eV}$

$n=1.38$

$A=50\mu\text{m}\times 50\mu\text{m}$

◯ : measured date
— : linear fit

current (A)

bias voltage (V)
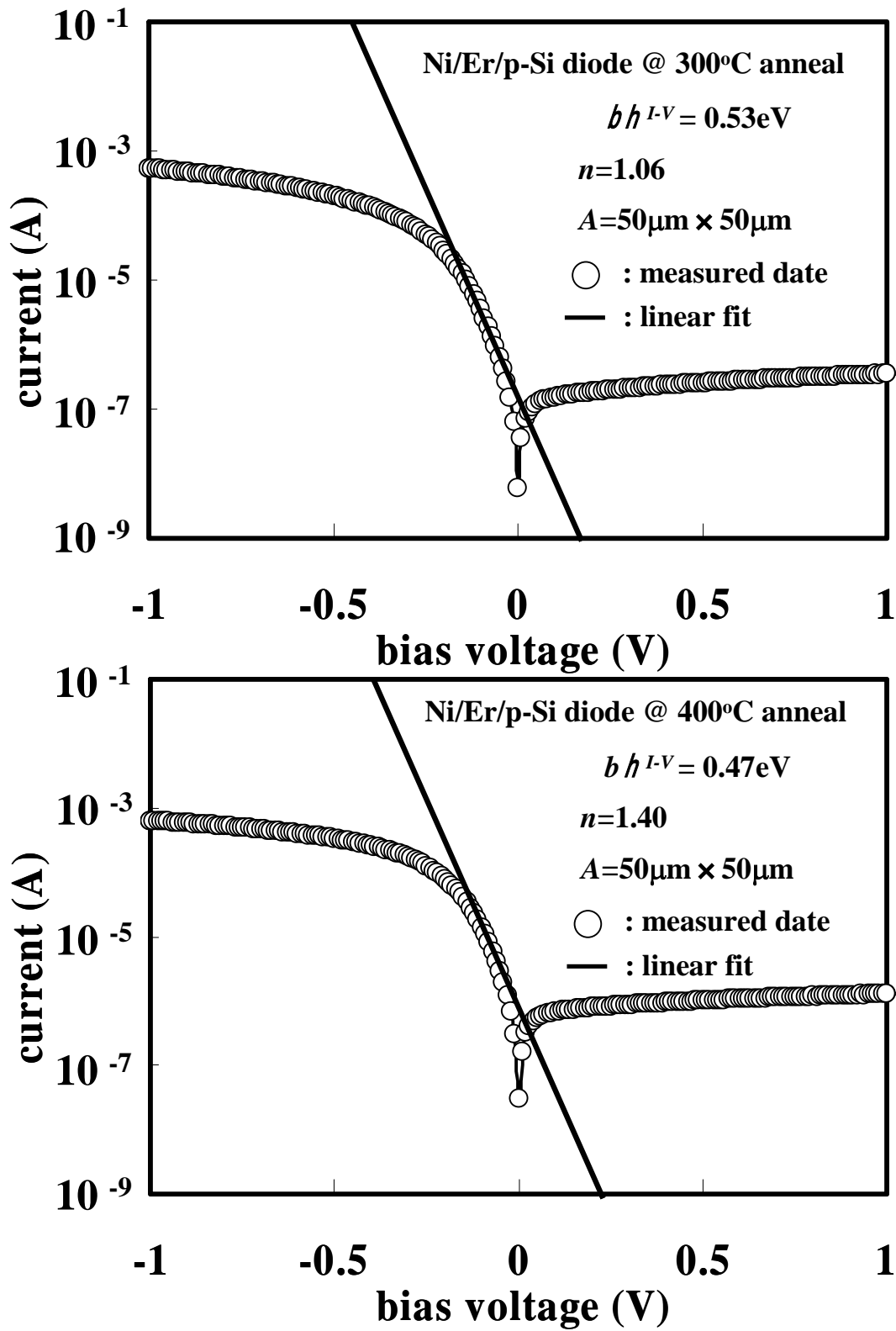
Fig.4.7 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Er(3.6nm)/p-Si at annealing temperatures of 500°C and 600°C.
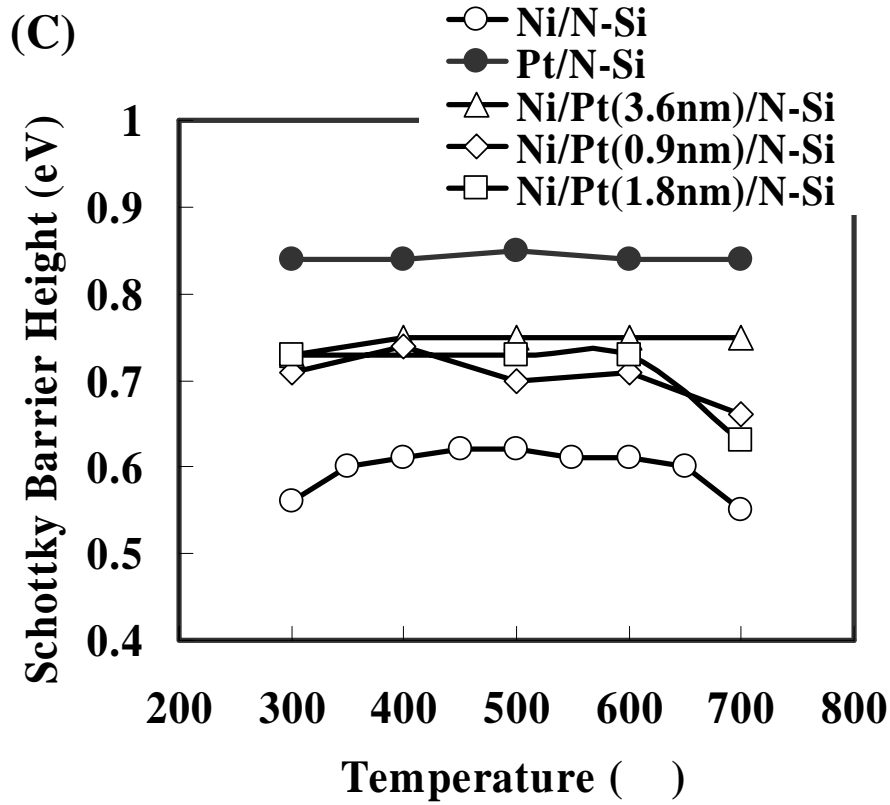
Fig.4.8 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Er(3.6nm)/p-Si at annealing temperatures of 700°C

Fig.4.9 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Pt(3.6nm)/n-Si at annealing temperatures of 300°C and 400°C.

Fig.4.10 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Pt(3.6nm)/n-Si at annealing temperatures of 500°C and 600°C.

Fig.4.11 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Pt(3.6nm)/n-Si at annealing temperatures of 700°C.

(a)

Ni/N-Si
Pt/N-Si
Ni/Al(3.6nm)/N-Si
Ni/Al(1.8nm)/N-Si
Ni/Al(0.9nm)/N-Si

(b)

Ni/P-Si
Ni/Er(3.6nm)/P-Si
Ni/Er(1.8nm)/P-Si
Ni/Er(0.9nm)/P-Si
Er/P-Si

Fig.4.12 Annealing temperatures dependence of Scottky barrier heights for the diodes for the diodes formed from the initial structures of Ni/Al/n-Si,Ni/Er/p-Si and Ni/Pt/n-Si with various thicknesses of Al, Er or Pt layers.

4.1.5 Analysis of Schottky Barrier Modulation by Using Al, Pt or Er

AES analysis, as shown Fig4.13, revealed that an Al layer was formed at the surface, and didn't remain at the Ni Silicide/Si interface, after the annealing at 500°C.

TEM and EDX analysis, as shown Fig.4.14, revealed that an Er silicide layer was formed at the surface, while small amount of Er was incorporated in the entire NiSi layer, after the annealing at 500°C.

RBS analysis, as shown Fig.4.15, revealed that most of the Pt remained at the Ni Silicide/Si interface, after the annealing at 500°C.

The non-remained Al at the Ni silicide/Si interface might not contribute to the Φ_b modulation. Otherwise, the remained Pt and Er at the Ni silicide/Si interface might contribute to the Φ_b modulation for both cases although the properties of segregation are apparently different in the Er inserted case and Pt inserted case.
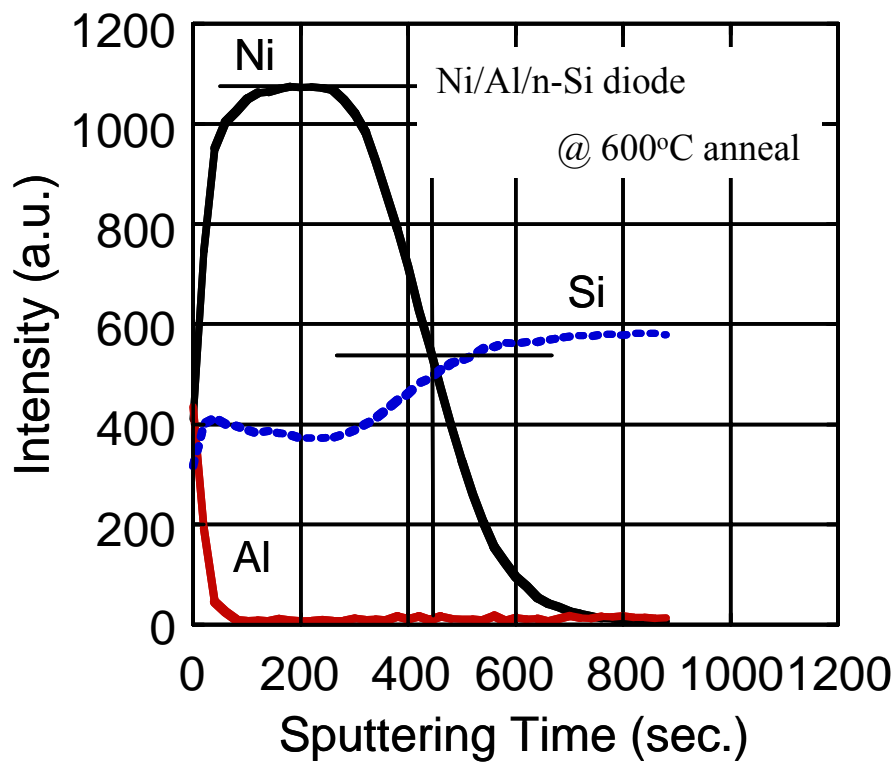
Fig.4.13 AES depth profile for Ni silicide formed from the Al-just interface with 1.2 nm Al layer at 600°C.
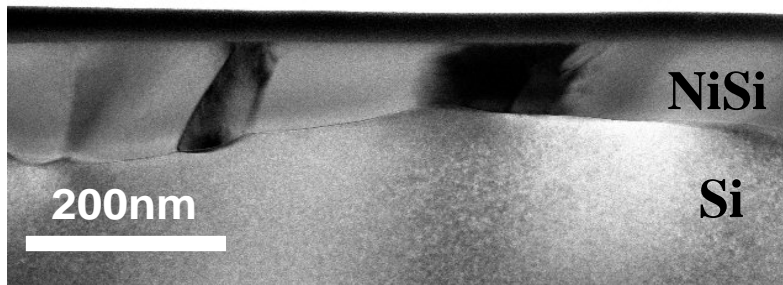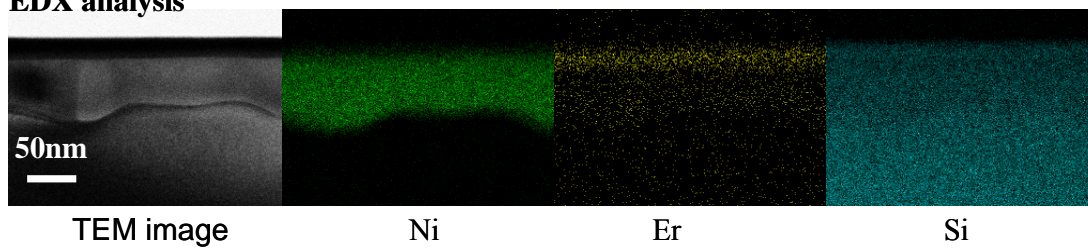
Fig.4.14 Cross-section TEM and EDX view of Ni/Er(3.6nm)/p-Si.

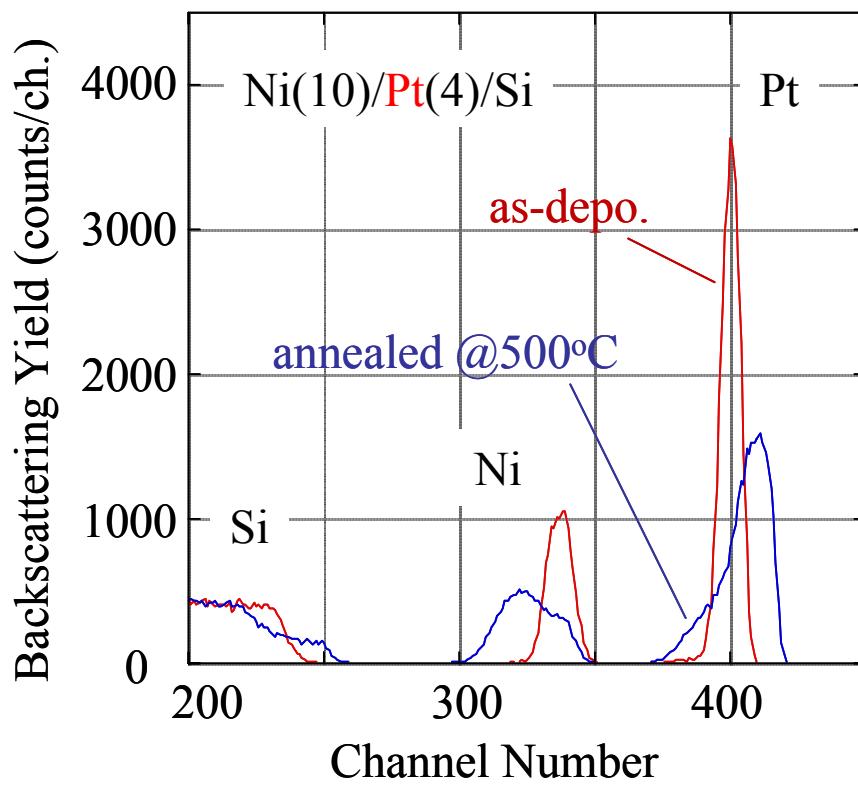Fig.4.15 RBS profile for Ni/Pt/Si diode at 500°C anneal.

4.2 Ni Silicide Schottky Diode by Using Pt and B

4.2.1 Fabrication process of schottky diode

Schottky diodes were formed on SiO_2 isolated n- bulk (100) Si wafers (doping concentration: 1.0×10^{15} cm^{-3}), as shown in Fig.4.16. Before metal deposition, the patterned wafers were cleaned in mixed solution of H_2SO_4 and H_2O_2 followed by chemical oxide removal by diluted HF. Metals were deposited subsequently by DC sputtering in Ar gas at a pressure of 5.0×10^{-1} Pa. The layered structures of Ni/Pt/B/Si with 12-nm-thick Ni layer and the Pt and B layer thicknesses 3.6 nm were deposited. The samples were annealed in forming gas (3% H_2 + N_2) at various temperatures from 300^oC to 700^oC for 1 min. After the removal of un-reacted metals by chemical etching, Al back contacts were formed by thermal evaporation. The Schottky barrier heights of the fabricated diodes were evaluated form current voltage characteristics.

- Field thermal oxidation (~200nm)

- Active area patterning

- SPM, HF-last

- Metal sputtering
  (Ni:100nm, Pt and B :3.6nm)

- Rapid thermal annealing (RTA)
  (F.G ambient, 300-700°C,1min)

- Metal etching

- Back side electrode formation
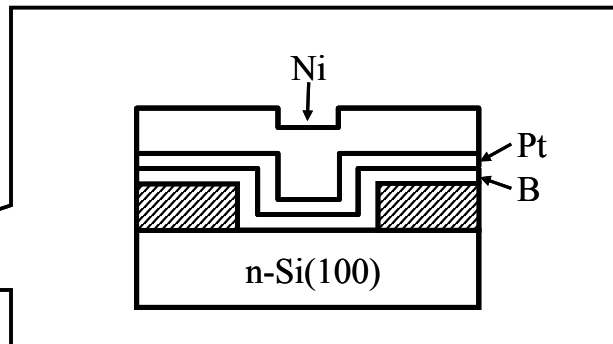 (Aluminum evaporation)

Ni

Pt

B

n-Si(100)

Fig.4.16 Fabrication process of the Schottky barrier diodes from the initial structures of Ni/Pt/B/n-Si.

4.2.2 Characteristics of Ni silicide schottky diode by using Pt and B

Typical current-voltage (*I-V*) curves of Schottky diodes of annealing temperature from 300$^{\text{o}}$C to 700$^{\text{o}}$C fabricated from the Ni/Pt/B/n-Si structures are shown in Fig. 4.17-4.19. Φ_b was evaluated from the *I-V* curves in the forward bias region. The obtained Φ_b values are plotted against the annealing temperatures in Fig. 4.20.

In the case of B and Pt insertion, observed Φ_b values for electrons were higher by 0.19-0.3eV from the value for Ni Silicide without the B and Pt insertion, in the annealing temperature range of 300-700$^{\text{o}}$C as shown Fig.4.12. This means that the B and Pt insertion is favorable for p-type MOSFETs because the Φ_b for holes can be lowered.
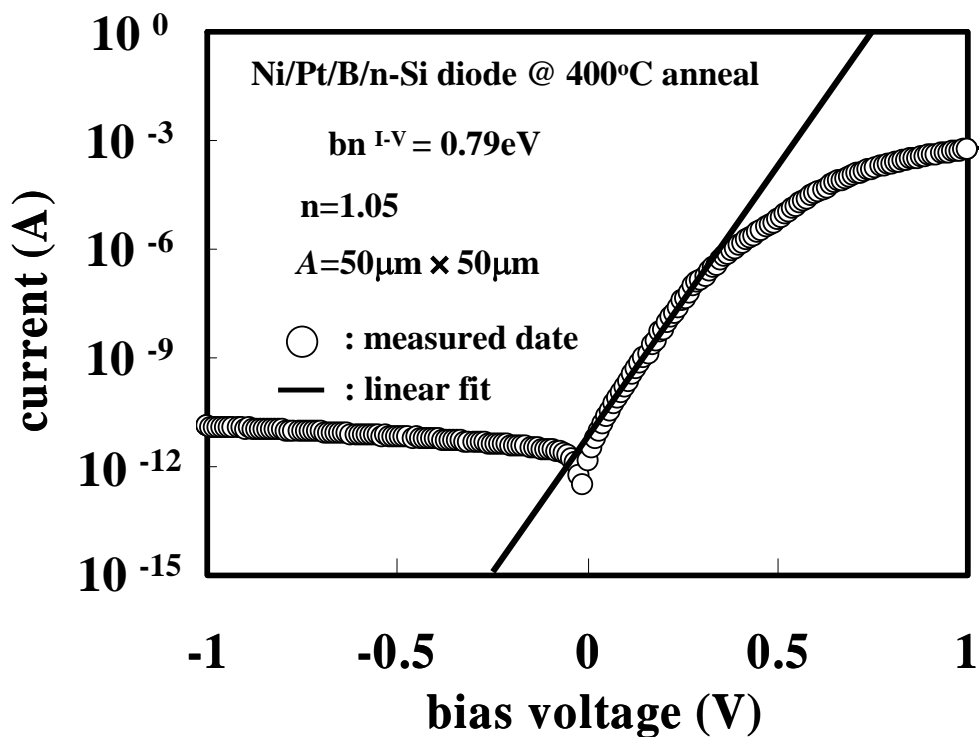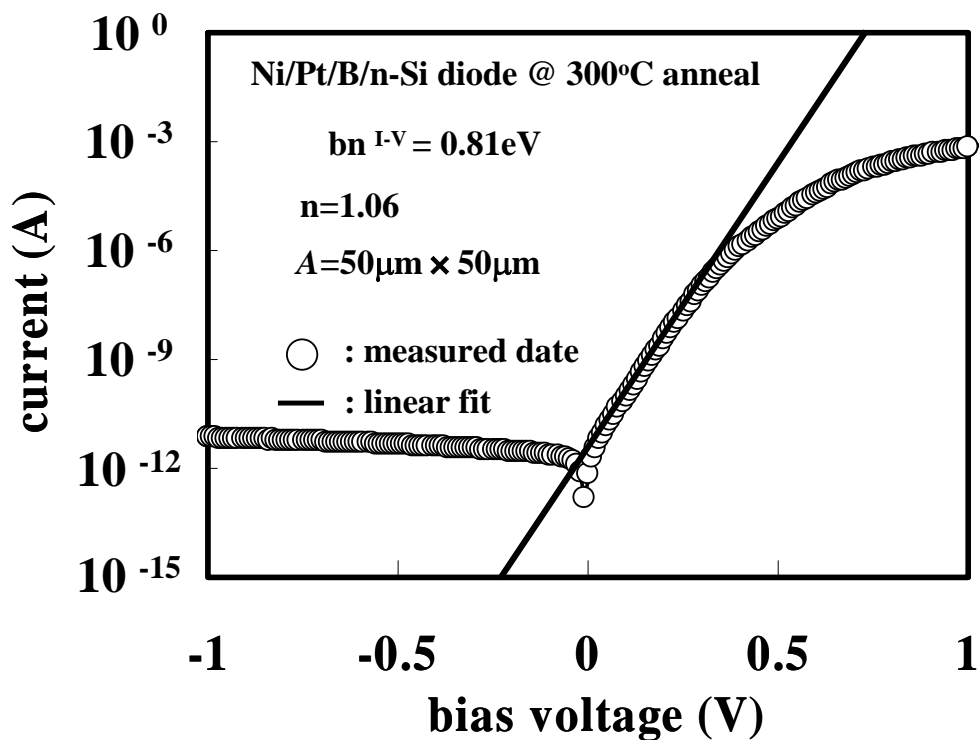
Fig.4.17 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Pt(3.6nm)/B(3.6nm)/n-Si at annealing temperatures of 300°C and 400°C.

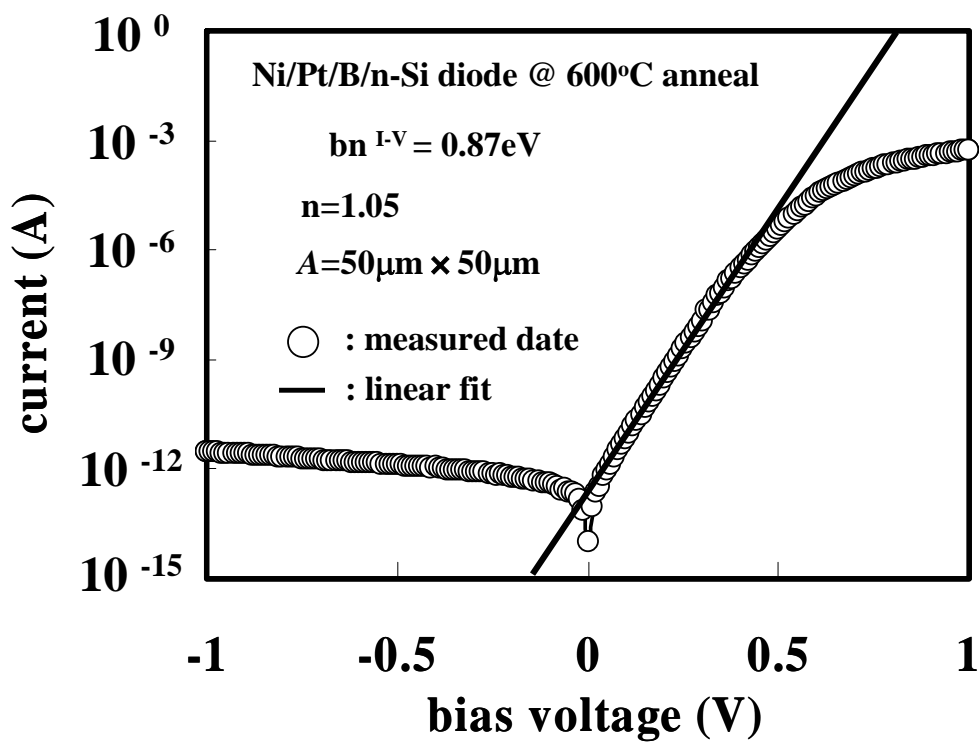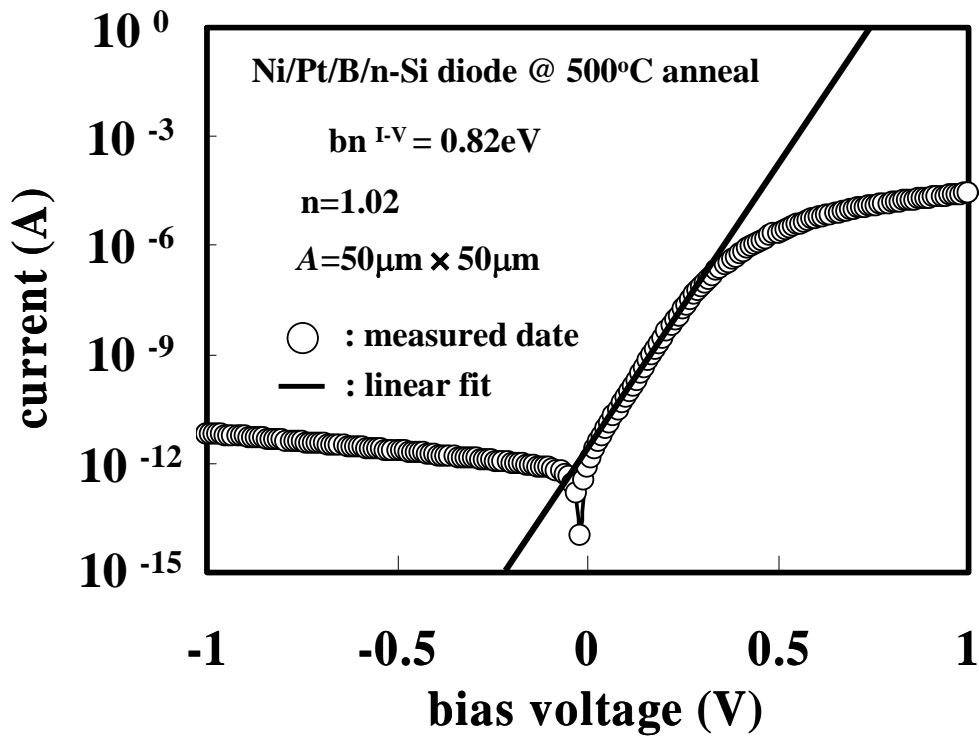Fig.4.18 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Pt(3.6nm)/B(3.6nm)/n-Si at annealing temperatures of 500°C and 600°C.
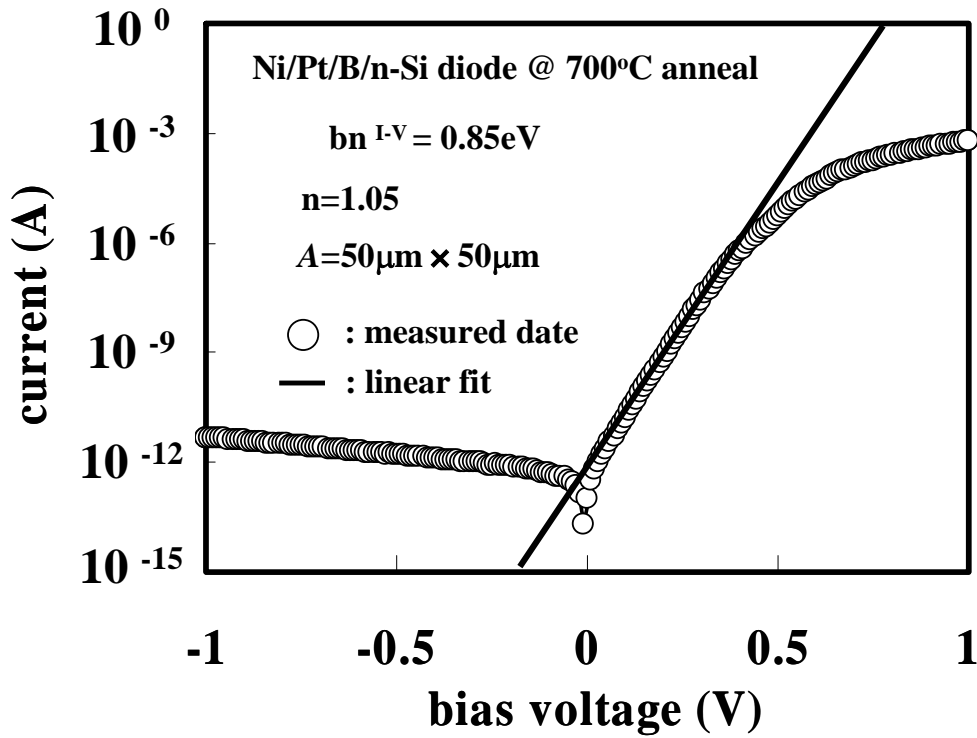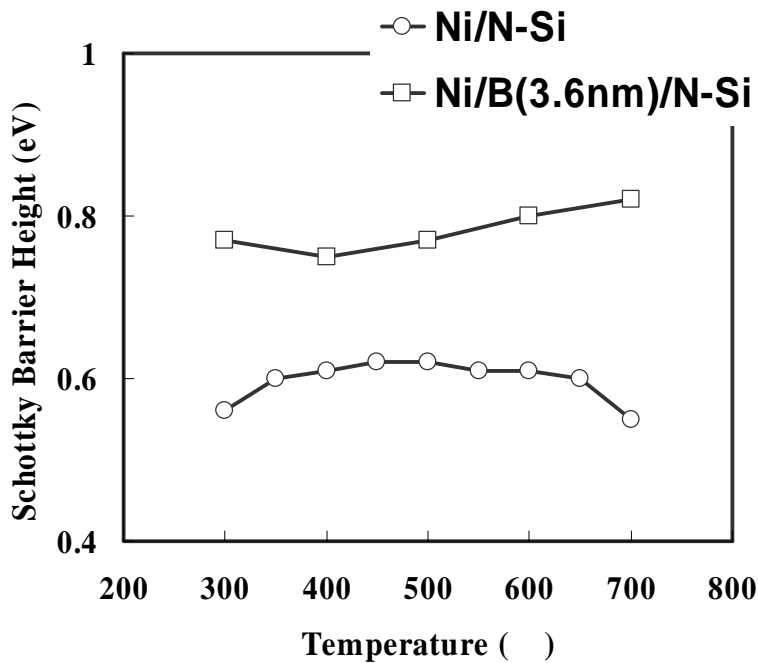
Fig.4.19 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initia structures of Ni/Pt(3.6nm)/B(3.6nm)/n-Si at annealing temperatures of 700°C.

Fig.4.20 Annealing temperatures dependence of Scottky barrier heights for the diodes for the diodes formed from the initial structures of Ni/Pt/B/n-Si with 3.6nm thicknesses of B or Pt layers.

4.2.3 Analysis of Schottky Barrier Modulation by Using Pt and B

  During the second rapid tharmall annealing, diffusion B layers are driven out of the silicides and

become piled up at the silicide/silicon interface. First-principles calculations suggest that the system

assumes its most stable state when B atoms occupy the substitutional sites within the first Si

monolayers in the close vicinity of the silicide/silicon interface. As a result, these substitutional B

atoms are charged by the interface states, forming electric dipoles across the interface. Fig.4.20

schematically illustrates how the deformation of the energy band is induced by the dipoles. In detail,

whether the dopants substitute Si atoms or not may also depend on the silicide used. Further

investigation is needed to confirm the mechanism. Based on the experimental results, substitutional

B atoms are expected to be negatively charged and to bend the energy band upward leading to an

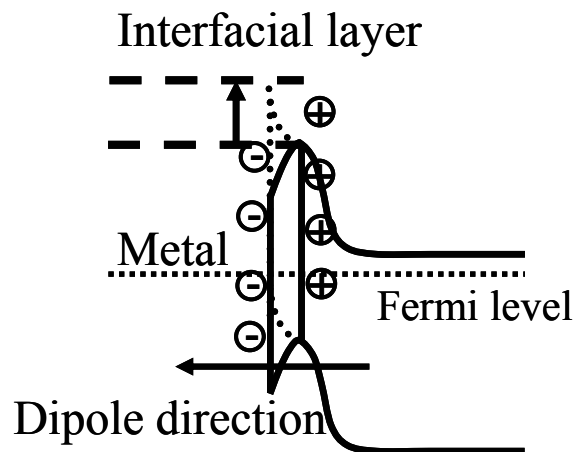increased electron SBH from the silicide to the Si [Fig.4.20].

Fig.4.20 Deformation of the energy band induced by negatively.

Chapter 5

SCHOTTKY BARRIER MOSFET BY USING Er

5.1 Introduction

The Schottky barrier source/drain MOSFET (SB-MOSFET) is one of the promising candidates for next generation devices, thanks to its shallow junction depth with lower electrode resistance and process temperature[16,19]. The major concern is, however, to reduce the Schottky barrier height (Φ_b) for electrons and holes, because the presence of large Φ_b severely limits the CMOS drive current [17]. Variety of silicides such as Pt silicide and Er silicide have been proposed for SB-PMOS and SB-NMOS use, and the Φ_b of 0.15-0.27eV in SB-PMOS using Pt silicide and that of 0.27-0.36 eV in SB-NMOS using Er silicide were reported [18]. Reports on middle gap materials such as NiSi and $CoSi_2$ also showed that the great possibility of those materials for applications of the SB-MOSFETs by employing Schottky-barrier-height modulation techniques [17].

In this chapter, we report a new Schottky-barrier-height modulation method for Ni silicide by inserting a thin Er or Pt interlayer before silicidation process.

5.2 Ni Silicide Schottky Barrier MOSFETs by Using Er

5.2.1 Fabrication Process

The back gate type -channel SB-MOSFETs were also fabricated on boron-doped (1.0×10^{15} cm^{-3}) p-type silicon on insulator (SOI) wafers (SOI thickness: 40nm), as shown in Fig.5.1. The buried oxide (BOX) layer of 140-nm-thick SiO$_2$ in the SOI structure was used as the gate oxide. Active regions were defined by lithography and reactive ion etching. Channel regions were covered with a 10-nm-thick thermal-oxide layer by the rapid thermal annealing in 5% O$_2$ at 1000°C for 9 min. Er and Ni layers of 3.6 and 100 nm thick, respectively, were subsequently deposited by DC sputtering in the same way as that described above. Then the samples were annealed in forming gas (3% H$_2$ + N$_2$) at 300°C for 1min. After the removal of un-reacted metals, Al back contacts were formed for a gate electrode.

Lithography and reactive ion etching

Active regions define

Rapid thermal annealing (RTA)
(F.G ambient, 300°C,1min)
SPM, HF-last

Metal sputtering
(Ni:100nm, Er :3.6nm)

Rapid thermal annealing (RTA)
(F.G ambient, 300°C,1min)

Metal etching

Back side electrode formation
(Aluminum evaporation)

SiO$_2$
SOI
BOX
Si
SOI layer thichness 40nm
BOX layer thichness 140nm
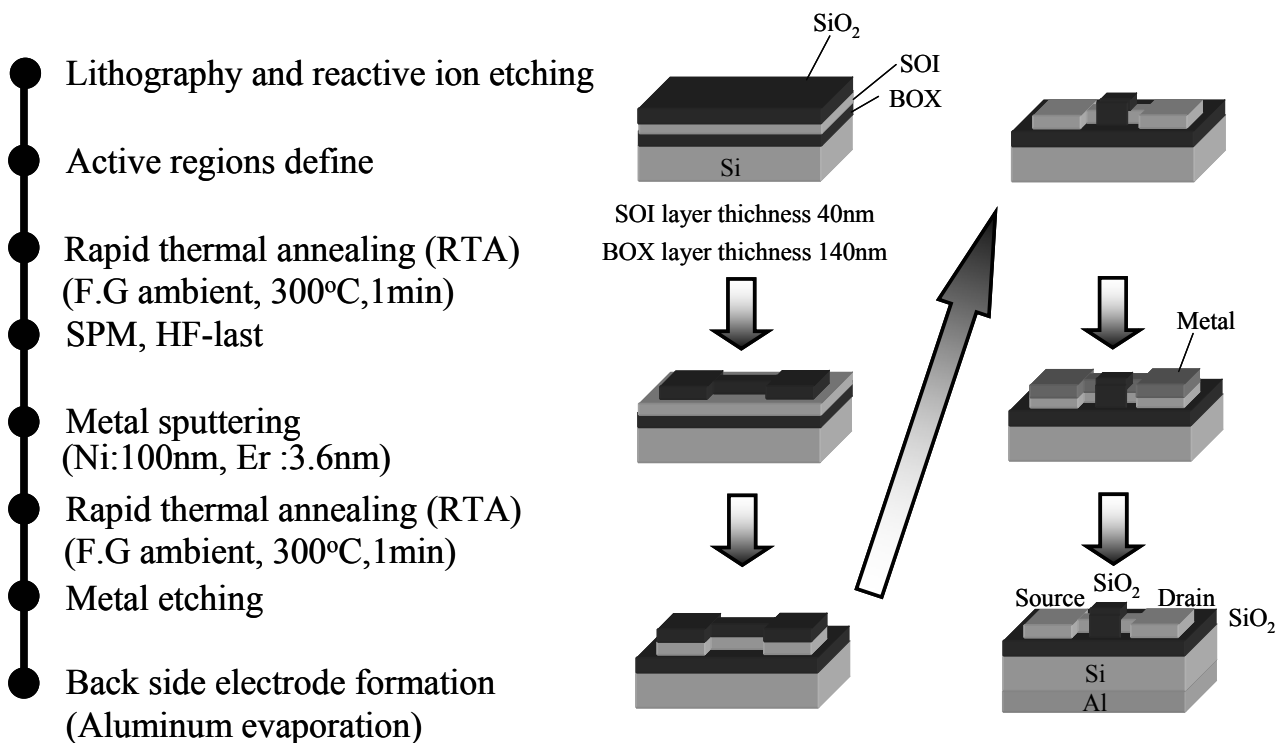
Metal

Source SiO$_2$ Drain
SiO$_2$
Si
Al

Fig.5.1 Fabrication process of the Schottky barrier MOSFET by Er layer insertion

5.2.2 Characteristics of Ni Silicide Schottky Barrier MOSFETs by Using Er

Fig.5.2 (a) and (b) show I_D-V_G and I_D-V_D characteristics of the fabricated n-type SB-MOSFET with 20 μm channel length. Because the 140-nm-thick SiO_2 BOX layer was used as the gate oxide, the obtained value of subthreshold slope was 235 mV/dec. This high value of subthreshold slope may improved by reducing the gate oxide thickness.
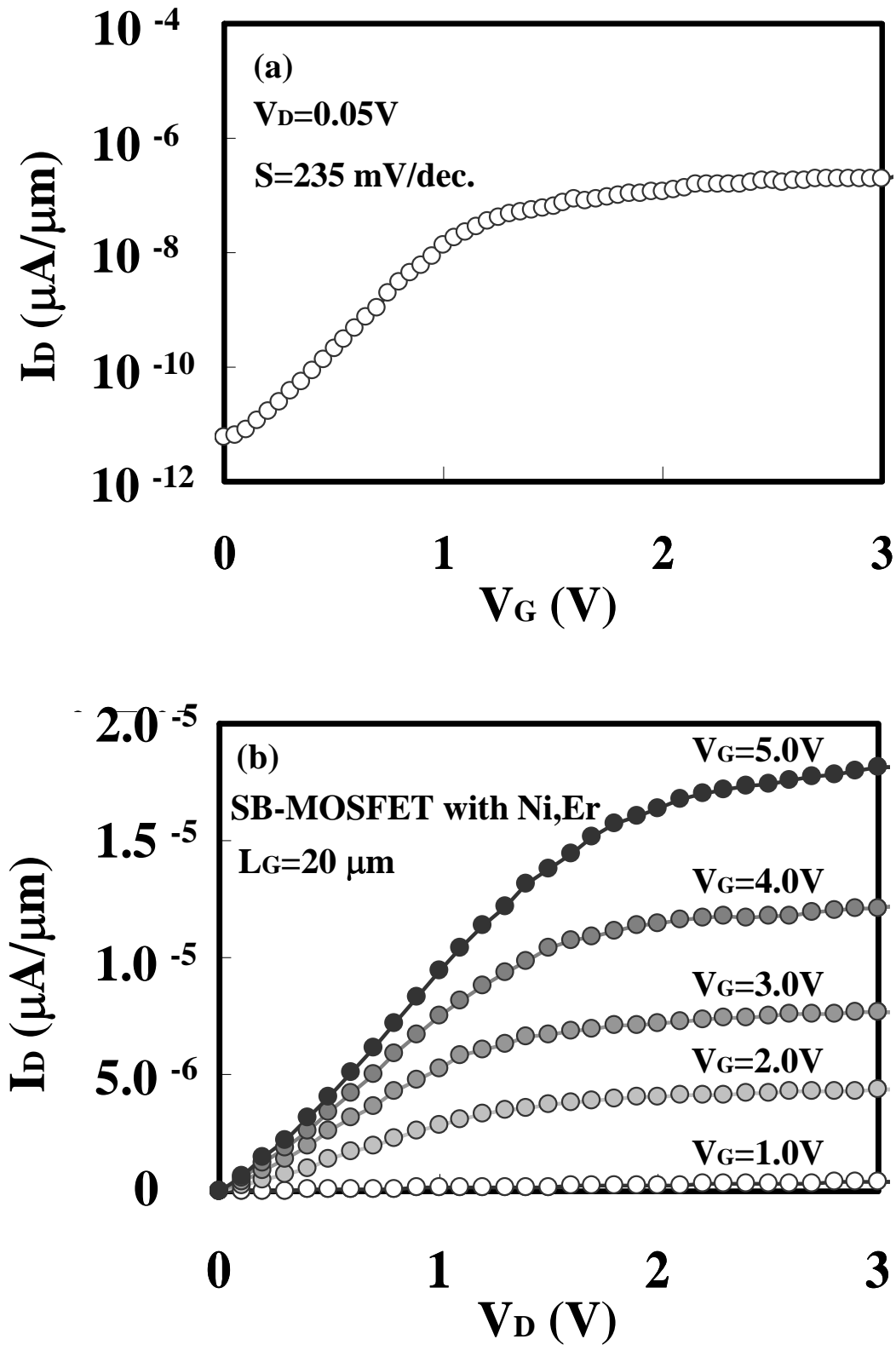
Fig.5.2 (a)I_D-V_G and (b)I_D-V_D characteristics of the fabricated N-channel SB-MOSFET.

Chapter 6
CONCLUSION

6.1 Result of this study

We have proposed a new Φ_b modulation method for Ni silicide by inserting Er or Pt and B and Pt layers to Ni/Si interface. The Φ_b modulation of 0.03-0.12eV lowering for electrons, 0.08-0.2eV lowering for holes, 0.19-0.3eV lowering for holes by the Er insertion, Pt insertion and B and Pt insertion, respectively, was performed. The modified values of Φ_b were insensitive to variation of the annealing temperatures employed in the experiments. n-type Schottky barrier source/drain MOSFET was successfully fabricated using Er insertion technique

6.2 Subject and forward view

In this work, we have proposed a new Φ_b modulation method for Ni silicide by inserting Er or Pt and B and Pt layers to Ni/Si interface and n-type Schottky barrier source/drain MOSFET was successfully fabricated using Er insertion technique. Hoevwr, enough characteristics doesn't get. From now on forward, the subject to overcome is found. First of all, it is proposed that Φ_b modulation method by using other materials and processes. The possibility more shchottky barrier modulation is investigated. Second, in the case of B and Pt insertion, schottky barrier height for holes is fairly lowering. On the other hand, in this work, the schottky barrier modulation method for electrons is only Er insertion. When this method is used for CMOS, schottky barrier lowering is reqired p and n-type silicon, respectively. Third, MOSFET having more thin gate oxide fabricate.

Reference

[1] International Technology Roadmap for Semiconductors (ITRS) 2006 update

[2] M. P. Lepselter and S. M. Sze, Proc. IEEE, vol. 56, PP. 1400-1402 (1968)

[3] F. J. Huang and K. K. O, Electron. Lett., vol. 33, pp. 1341-1342 (1997)

[4] M. Nishisaka and T.Asano, Jpn. J. Appl. Phys., vol. 37, pp. 1295-1299 (1998)

[5] W. Saitoh, S. Yamagami, A. Itoh and M. Asada, Jpn. J. Appl. Phys., vol. 38, pp.L629-631 (1999)

[6] J. Kedzierski, S. Xuan, E. H. Anderson, J. Bokor, T. J. King and C. Hu, IEDM, pp.57-60 (2000)

[7]   SOI MOSFET
(2002)

[8]   ,   ,   ,   , 1995.

[9] F. A. Padovani and R. Stratton, Solid State Electron, vol. 9, 695 (1966)

[10] J. Kedzierski, P. Xuan, E. Anderson, J. Boker, T.King, and C. Hu, IEDM Tech. Dig. 57 (2000)

[11] Q. T. Zhao, P. Kluth, S. Winnerl, and S. Mantl, Solid-State Electron. **47**, 1183 (2003)

[12] C. Wang, J. P. Snyder, and J. R. Tucker, Appl. Phys. Lett. **74**, 1174 (1999)

[13] C. Wang, J. P. Snyder, and J. R. Tucker, Appl. Phys. Lett. **74**, 1174 (1999)

[15] J. Guo and M. Lundstorm, IEEE Trans. Electron Devices **49**, 1897 (2002)

[16] Moongyu Jang et al., IEEE Electron Devices Lett, vol. 26, 354 (2005)

[17] A.Kinoshita, C. Tanaka, K.Uchida and J. Koga., Symp. VLSI Tech. 9A-3(2005)

[18] John M. Larson and John P. Snyder., IEEE Trans. Electron Devices, vol. 53, 1048 (2006)

[19] Shiyang Zhu et al., IEEE Electron Devices Lett, vol. 25, 565 (2004)

[20] Zhen Zhang, Zhijun Qui, Ran Liu, Mikael Ostling and Shi-Li Zhang., IEEE Electron Devices Lett, vol. 28, No.7 (2007)

Acknowledgements

Yoshihisa Ohishi
Yokohama, JAPAN
January 2008