Master thesis

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A Study on High-k Gage Stack Engineering for Improving Mobility

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Contents

Chapter 1 Introduction

1.1 Background of this study

Si-based large-scale-integrated circuits (LSIs) have developed rapidly in the last forty years and the Complementary Metal Oxide Semiconductor (CMOS) Field Effect Transistor (FET) which forms the basis of LSIs is the most important electronic device. The recent dramatic advances in information technology (mobile PC, cell- phone, Internet, etc.) owe to high speed, small, and low power consumption.

This progress has been accomplished with the downsizing of transistors in accordance with Moore's Law. This law notes that the device feature size decreases each year and the number of transistors on a LSI doubled every two years. The International Technology Roadmap for Semiconductor (ITRS) [1.1] defines how the device parameters are scaled for the next technology node. The scaling rule of MOSFET was published by R. Dennard [1.2]. Figure 1.1 shows the principle of scaling rule. According to this rule, the device dimension and supply voltage of MOSFET should be reduced by the same factor *k*. The doping concentration should be increased by the same

factor *k*. As a result, the electric field in MOSFET remains constant despite the technology node.

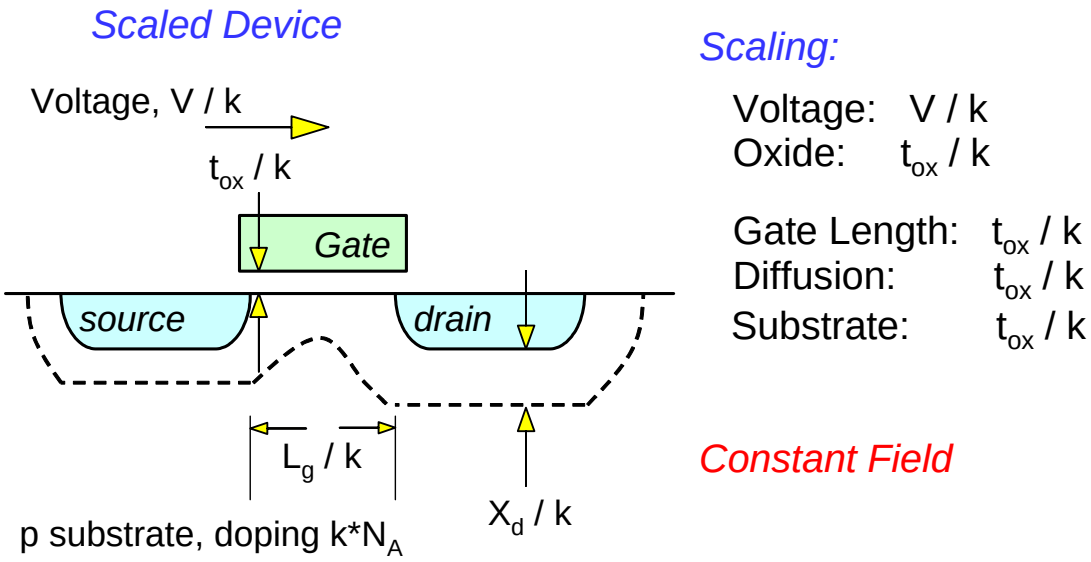

Fig. 1.1 *Scaling rule of MOSFET*

The drain current in MOSFET, I_d, can be written as [1.3]

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_g - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \quad \text{.....} \quad (1.1)$$

where μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance per unit area, W is the gate width, L is the gate length, V_g is the gate voltage, V_t is the threshold voltage, V_{ds} is the drain voltage. The C_{ox} is given by [1.3]

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \text{.....} \quad (1.2)$$

where ε_{ox} is the oxide permittivity, t_{ox} is the oxide thickness. From the Eq. (1.1) and Eq. (1.2), scaling the oxide thickness and the gate length result in higher drain current. Thus, the scaling is important and "golden rule" for improving the MOSFET performance. However, the scaling can not go on forever.

1.2 Limits of SiO_2

As mentioned previously, the MOSFET is the fundamental device in LSI circuit. According to Moore's Law, the transistor has been shrunk to get higher performance and reduce the costs. The changes of main parameters of LSIs in the last ten years are plotted in Figure 1.2 [1.4]. The gate oxide, which separates the gate electrode from the substrate, is the most important part of the MOSFET. Silicon dioxide (SiO_2) has been used as ideal gate dielectrics for forty years because SiO_2 is compatible with silicon substrate, namely low interface state density, good thermal stability, etc. Silicon dioxide (SiO_2) is usually formed by thermal oxidation of silicon substrate. SiO_2 has successfully scaled so far and SiO_2 physical thickness becomes thinner until 1.2nm which means a thickness of a few atomic layers.

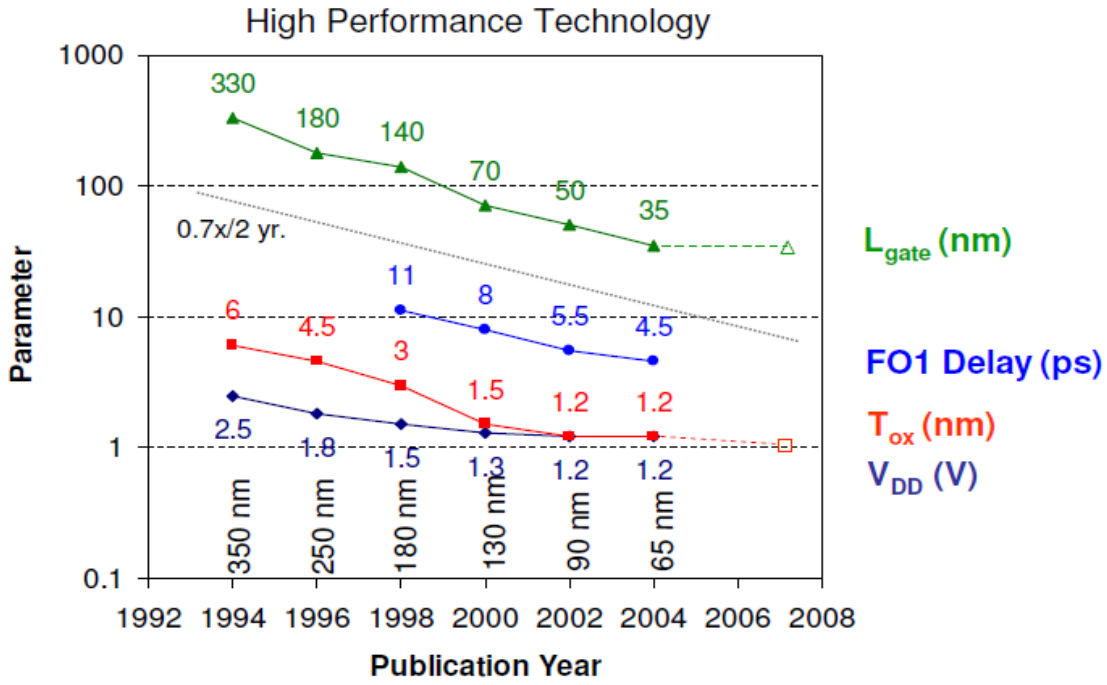

Fig. 1.2 *Inflection of main parameters of MOS LSIs*

The thickness of SiO2 is now so thin (under 1.5nm) that gate leakage current due to direct tunneling of electron through the SiO_2 becomes too high, exceeding $1A/cm^2$ at 1V shown in Figure 1.3 [1.5]. As a result, power consumption increases unacceptable level. In addition, it becomes extremely difficult to fabricate and measure accurately ultra thin gate oxide. Thus, SiO_2 is approaching its physically and electrically limits. To continue the scaling rule, it is necessary to replace SiO_2 with an alternative material as a gate oxide.

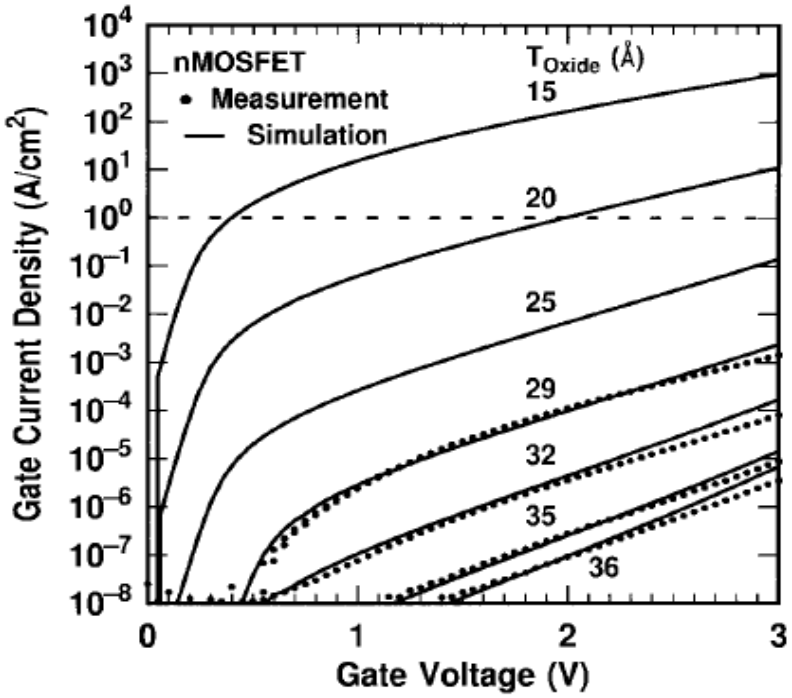

Fig. 1.3 *Leakage current versus voltage for various thickness of SiO_2*

1.3 Introduction of high-k materials

To balance competing goals ultra-thin gate dielectrics and low leakage current, high-k (high dielectric constant) gate dielectrics is essential technology. The guideline for selecting an alternative gate dielectrics materials are high dielectric constant, large band gap and high band offset to silicon, thermodynamic stability, interface quality, process compatibility, and reliability. The gate dielectrics which have high dielectric constant and large band gap can suppress the gate leakage current. Relationship between physical thickness of SiO_2 and high-k gate oxide obtained by same gate capacitance value (C) is written as,

$$C = \frac{\varepsilon_{high-k}}{t_{high-k}} = \frac{\varepsilon_{SiO_2}}{t_{EOT}} \qquad \text{.....} \quad (1.3)$$

where $\varepsilon_{high\text{-}k}$ is the dielectric constant of high-k materials, $t_{high\text{-}k}$ is the physical thickness of high-k gate oxide, ε_{SiO2} is the dielectric constant of SiO_2 (=3.9).

EOT (Equivalent-Oxide-Thickness) is expressed as,

$$T_{EOT} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} T_{phy} \qquad \text{.....} \quad (1.4)$$

where T_{phy} is the physical thickness of gate oxide.

Therefore, it is well established that gate leakage currents are reduced by using the high-k materials as a gate dielectric while maintaining a small equivalent oxide thickness (EOT).

The above requirement is that dielectric constant should be preferably 25~30, a very high dielectric constant is undesirable. Because there is the trade off between dielectric constant and band offset, which requires a reasonably large band gap. Figure 1.4 [1.6]

shows the dielectric constant of candidate oxides tends to vary inversely with the band gap.

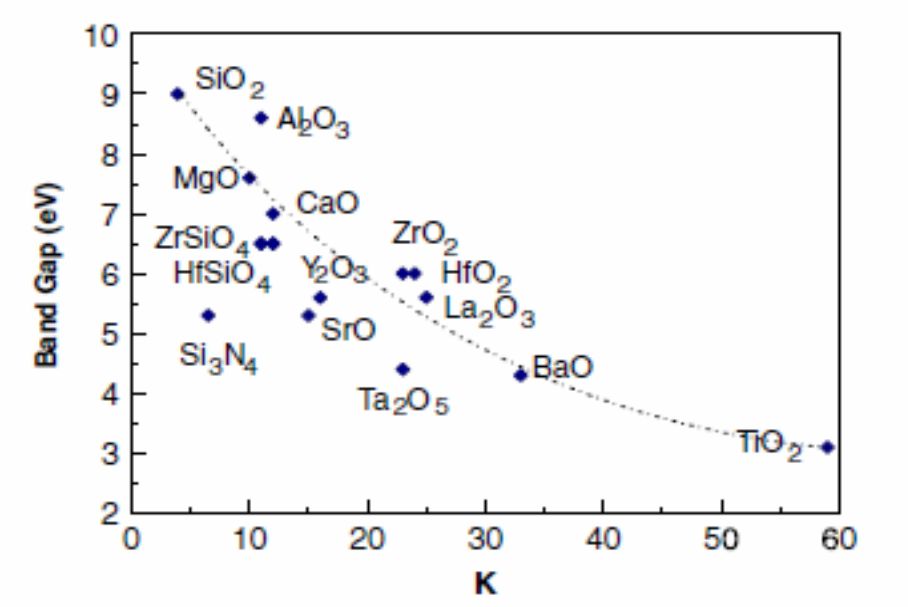

Fig. 1.4 *Dielectric constant versus band gap for candidate high-k gate oxide*

Among the candidate high-k materials, Hf-based materials are the most promising candidate. Figure 1.5 shows Hf-based gate oxide could reduce gate leakage current density almost three orders compared to SiO_2[1.7].

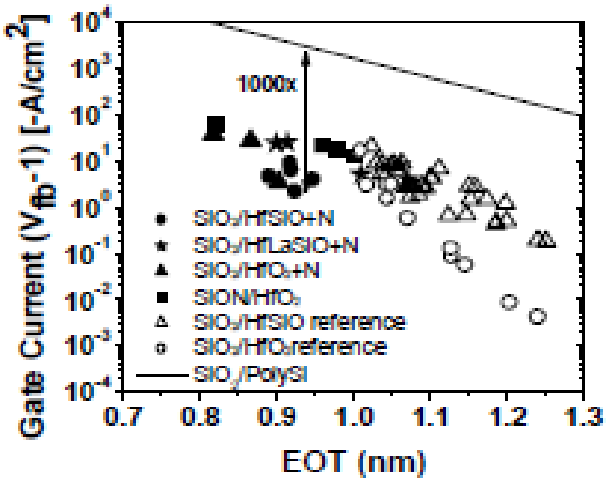

Fig. 1.5 *Gate leakage current density versus EOT compared with Hf-based oxide and SiO_2*

1.4 Problem of high-k gate dielectrics ~mobility degradation~

As stated already, it is possible to remarkably reduce the gate leakage current using high-k gate dielectrics. There is a major problem to be solved in MOSFET with high-k gate dielectrics. Figure 1.6 represents the effective mobility, μ_{eff}, of MOSFET with high-k gate dielectrics is lower than SiO_2 MOSFET [1.8, 1.9, 1.10].

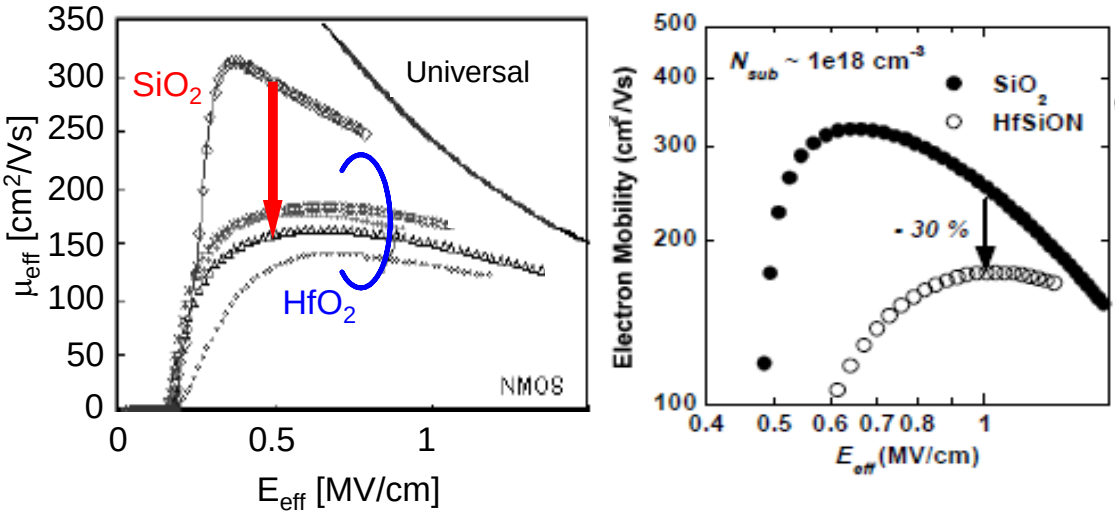

Fig. 1.6 *Comparison of effective mobility with Hf-based oxide and SiO_2*

The effective mobility which directly affects the drain current of MOSFET is significant device parameter written as Eq. (1.1). Although the gate leakage current is reduced by using the high-k gate dielectrics, the effective mobility of MOSFET with the high-k gate dielectrics also degrades compared to those of SiO_2. As a consequence, the performance of MOSFET cannot improve.

The mechanism of the effective mobility reduction has been intensively investigated by several groups [1.11, 1.12]. Several scattering sources have been identified as being

responsible for the reduced mobility. A model of MOSFET with high-k gate dielectrics is presented in Figure 1.7 [1.13]. One of the most serious problems is intrinsic mobility reduction by the remote phonon scattering due to the soft optical phonons inherent to high-k gate dielectrics [1.14]. Regardless of intrinsic mobility reduction, the effective mobility of MOSFET with high-k gate dielectrics may be reduced by extrinsic mechanisms as well, such as, fixed charges, interfacial dipoles, remote surface roughness, and crystallization, which could be avoided by improving the process.

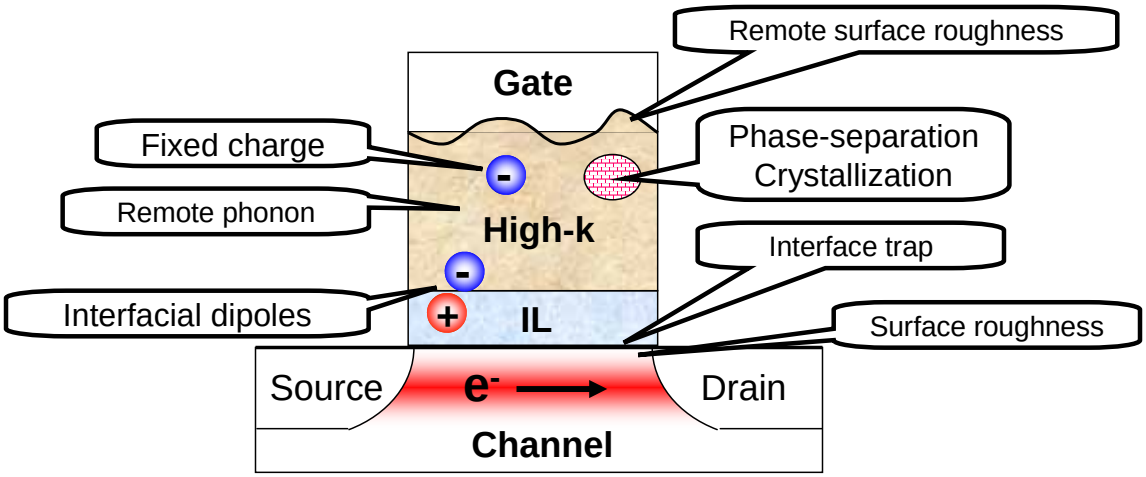

Fig. 1.7 *Possible sources for reduced mobility in high-k gate MOSFET*

It has reported that Hf-based oxide suppresses the reduced mobility to insert the SiO_2-based interfacial layer of 0.5-0.7 nm between the high-k gate dielectrics and silicon substrate. However, this attempt increases the EOT and it is easy to predict that the scaling limit is determined by the interfacial layer.

1.5 Purpose of this study

Continuing the gate oxide scaling, it is necessary to directly deposit the high-k gate dielectrics on the silicon substrate. Simultaneously, the choice of the high-k materials and the high-k gate stacks engineering become considerably important for improving the effective mobility of MOSFET.

La_2O_3 is the one of candidate for alternative gate dielectrics because of its high dielectric constant and large band offset shown in Figure 1.4. It has reported that there are many oxygen vacancies in high-k gate dielectrics compared to SiO_2 and considered that carriers may be trapped these oxygen vacancies [1.15]. Trapped charge scatters carriers and reduces inversion mobility. Therefore, high-k material which has great affinity with oxygen must be selected. According to the standard Gibbs free energy, the Sc_2O_3 has great affinity with oxygen shown in Table 1.1 [1.16]. However, there are few repots investigating the Si transitors with Sc_2O_3 gate insulator.

Table 1.1 *the standard Gibbs free energy of the rare earth oxide*

rare earth oxide	ΔG^o (kJ/mol)
Sc_2O_3(~13)	-1901+(0.287)T
Y_2O_3(~18)	-1895+(0.281)T
La_2O_3(~27)	-1785+(0.277)T

On the other hand, HfO_2 or Hf-based oxides are most candidate high-k material [1.15]. It has reported that incorporation of La_2O_3 into HfO_2 can increase the crystallization temperature [1.17]. In addition, the oxygen vacancy which is predominant defect can suppress by incorporation of La_2O_3 into HfO_2 [1.18]. It indicates that combination of La_2O_3 and HfO_2 can improve the inversion mobility.

The purpose of this study is experimentally to clarify the optimum the structure (stack or complex) and the combination of high-k materials for improving the effective mobility and to investigate the influence of the mobility due to various high-k gate stack engineering based on La_2O_3. Firstly, the basic properties of Sc_2O_3 are investigated. Subsequently, the electrical characteristics of complex oxide with changing the composition ratio are investigated. In addition, combination of La_2O_3 and HfO_2 are also investigated.

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Chapter 2 Fabrication and Characterization Methods

2.1 Experimental

2.1.1 Fabrication Procedure for MOS Capacitor

Figure 2.1 shows the device fabrication flow of high-k gate dielectrics MOS-capacitors. The high-k gate dielectrics MOS capacitors were fabricated on n-type (100)-oriented 2-5 Ω-cm Si substrate. To determine the capacitor area and avoid unexpected effect, 300nm thermal oxide was formed and patterned photolithography. After the substrates were cleaned with H_2SO_4/H_2O_2 mixture at 100^oC for 5min to remove resist-related organic contamination, diluted HF treatment. The high-k thin films were deposited on the substrate using e-beam evaporation at 300^oC in ultra-high vacuum chamber 10^{-7} Pa as shown in Figure 2.2. Tungsten (W) gate electrodes were formed by RF sputtering without breaking the ultra-high vacuum to avoid absorption of moisture from the air. The gate electrode was patterned by lithography and formed by RIE. Post-Metallization annealing (PMA) was performed. An Al films were evaporated on the backside of the substrate as a contact for electrical measurement.

Fig. 2.1 *Fabrication procedure for MOS-capacitor*

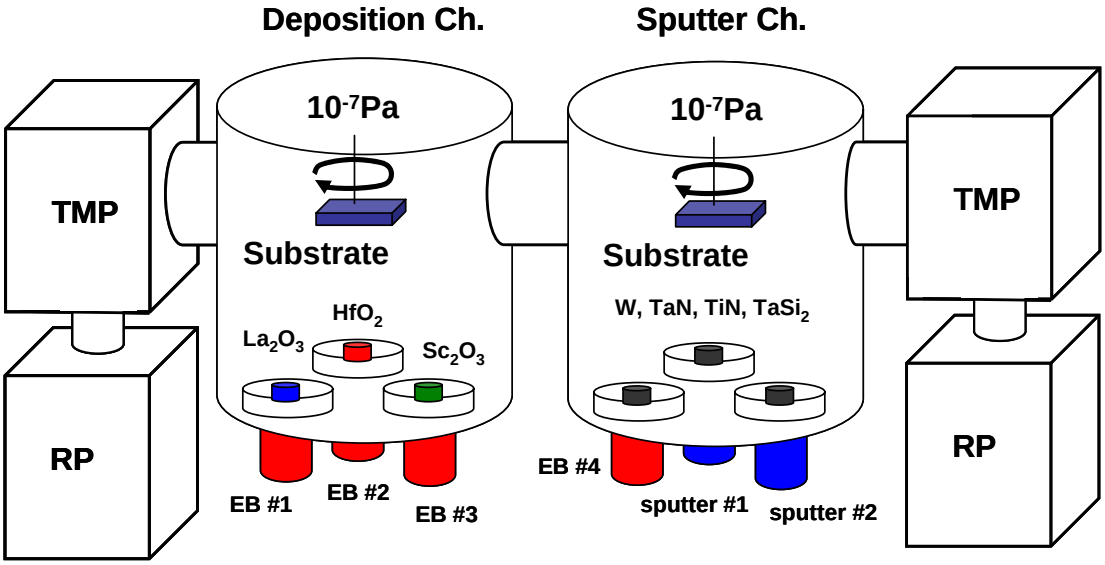


Fig. 2.2 *Schematic view of e-beam evaporation and RF sputtering system*

2.1.2 Fabrication Procedure for nMOSFET

Figure 2.3 shows the fabrication procedure for nMOSFET with high-k gate dielectrics. The high-k gate dielectrics were deposited on a HF-last, source and drain pre-formed Si wafer by e-beam evaporation in an ultra-high vacuum chamber same as the fabrication of MOS capacitors. The gate electrode was defined with photolithography followed by gate metal etching by RIE. An Al film was evaporated for source/drain contact.

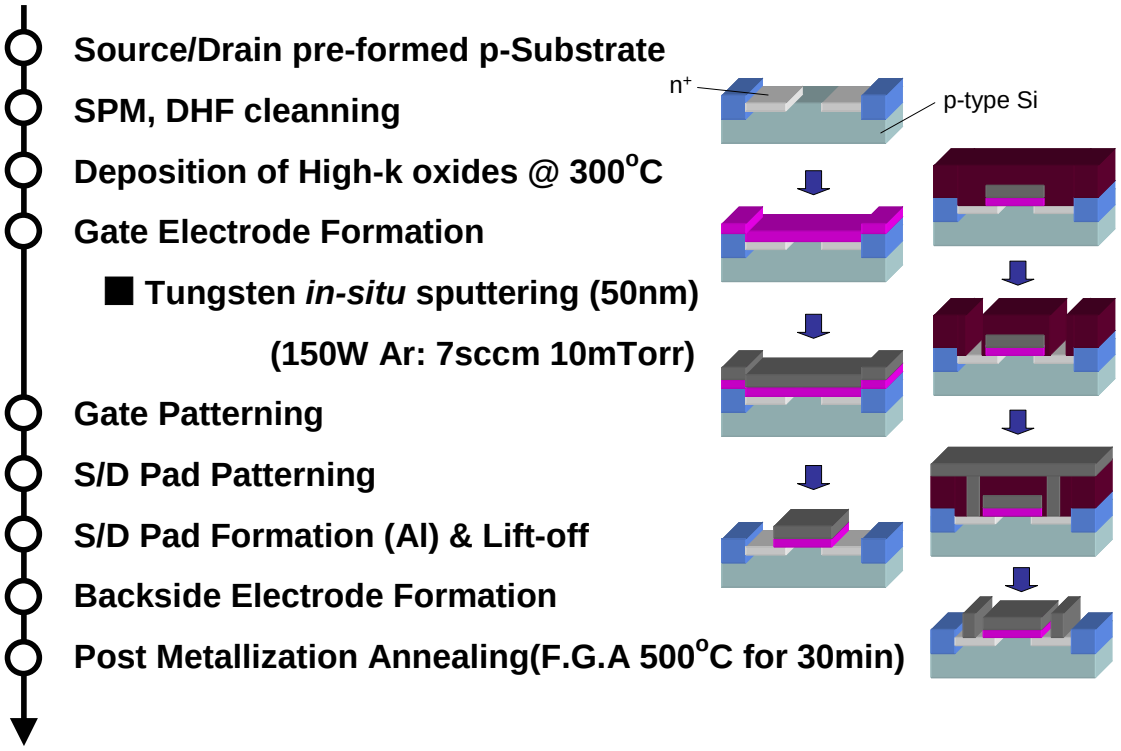


Fig. 2.3 *Fabrication procedure for nMOSFET*

2.2 Measurement Methods

2.2.1 Capacitance-Voltage (C-V) Characteristics

C-V characteristics or MOS capacitances are defined as small-signal capacitances and can easily be measured by applying a small ac voltage on top of a dc bias across the structure and sensing the out-of-phase ac current at the same frequency. In most cases, C-V characteristic measurement is performed with various frequencies (1kHz-1MHz) by precision LCR Meter (HP 4284A, Agilent). The energy band diagram of an MOS capacitor on a p-type substrate is shown in Figure 2.4 [2.1]. The intrinsic energy level E_i or potential ϕ in the neutral part of the device is taken as the zero reference potential. The surface potential ϕ_s is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \qquad \text{.....} \quad (2.1)$$

It is the change of charge due to a change of voltage and is most commonly given in units of farad/unit area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS-capacitor from the gate, $C = dQ_G / dV_G$, where Q_G and V_G are the gate charge and the gate voltage . Since the total charge in the device must be zero, $Q_G = -(Q_S + Q_{it})$ assuming no oxide charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \phi_s$, where V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and ϕ_s the surface potential, allowing Eq. (2.1) to be rewritten as

$$C = -\frac{dQ_S + dQ_{it}}{dV_{ox} + d\phi_s} \qquad \text{.....} \quad (2.2)$$

The semiconductor charge density Q_S, consists of hole charge density Q_P, space-charge region bulk charge density Q_b, and electron charge density Q_n. With $Q_S = Q_P + Q_b + Q_n$, Eq. (2.2) becomes

$$C = -\frac{1}{\frac{dV_{ox}}{dQ_S + dQ_{it}} + \frac{d\phi_s}{dQ_P + dQ_b + dQ_n + dQ_{it}}} \qquad \text{.....} \quad (2.3)$$

Utilizing the general capacitance definition of Eq. (2.1), Eq. (2.3) becomes

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_P + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_P + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \qquad \text{.....} \quad (2.4)$$

The positive accumulation charge Q_p dominates for negative gate voltage for *p*-substrate devices. For positive V_g, the semiconductor charges are negative. The minus sign in Eq. (6.3) cancels in either case.

Equation (2.4) is represented by the equivalent circuit in Figure 2.5 (a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_P is very high approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in Figure 2.5 (b) and the overall capacitance is C_{ox}. For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = -qN_A W$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} as shown in Figure.2.5 (c). In weak inversion C_n begins to appear. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (Figure 2.5 (d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in Figure 2.5 (e) applies in inversion, with $C_b = K_s \varepsilon_0 / W_{inv}$ with W_{inv} the inversion space-charge region width.

The flatband voltage is determined by the metal-semiconductor work function difference ϕ_{MS} and the various oxide charges through the relarion

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{t_{ox}} \frac{x}{t_{ox}} \rho_m(x)dx - \frac{1}{C_{ox}}\int_0^{t_{ox}} \frac{x}{t_{ox}} \rho_{ot}(x)dx \quad \ldots \quad (2.5)$$

where $\rho(x)$ = oxide charge per unit volume. The fixed charge Q_f is located very near the Si-SiO_2 interface and is considered to be at that interface. Q_{it} is designated as Q_{it} (ϕ_s), because the occupancy of the interface trapped charge depends on the surface potential. Mobile and oxide trapped charges may be distributed throughout the oxide. The *x*-axis is defined in Figure 2.4. The effect on flatband voltage is greatest, when the charge is located at the oxide-semiconductor substrate interface, because then it images all of its charge in the semiconductor. When the charge is located at the gate-oxide interface, it images all of its charge in the gate and has no effect on the flatband voltage. For a given charge density, the flatband voltage is reduced as the oxide capacitance increase, *i.e.*, for thinner oxides. Hence, oxide charges usually contribute little to flatband or threshold voltage shifts for thin-oxide MOS devices.

In this study, EOT value and flatband voltage were extracted from C-V characteristics by the NCSU CVC modeling program [2.2]. EOT values were calculated with taking quantum effect into account. Considering the quantum-mechanical confinement effects, the carriers concentration peaks below the Silicon-oxide interface and goes to nearly zero at the interface. As a result, the effective gate oxide thickness is slightly larger than the physical thickness.

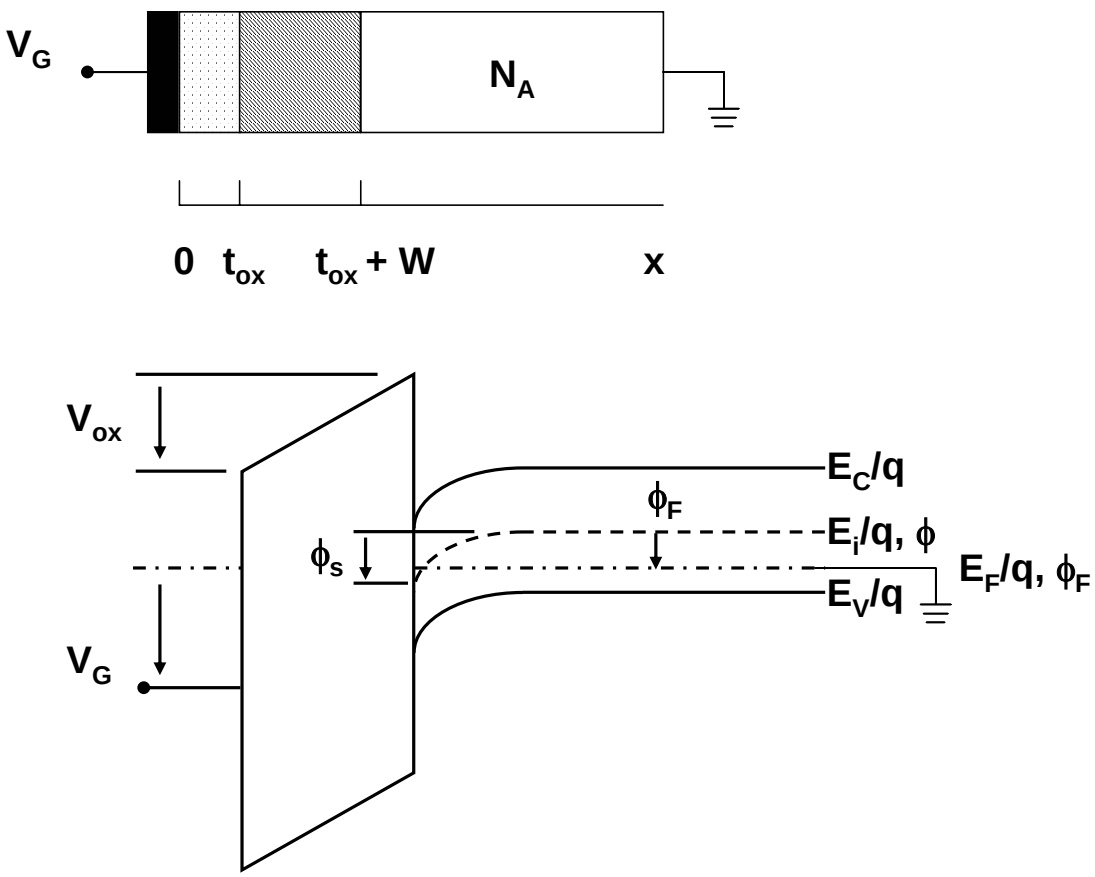


Fig. 2.4 *Cross-section and potential band diagram of an MOS capacitor*

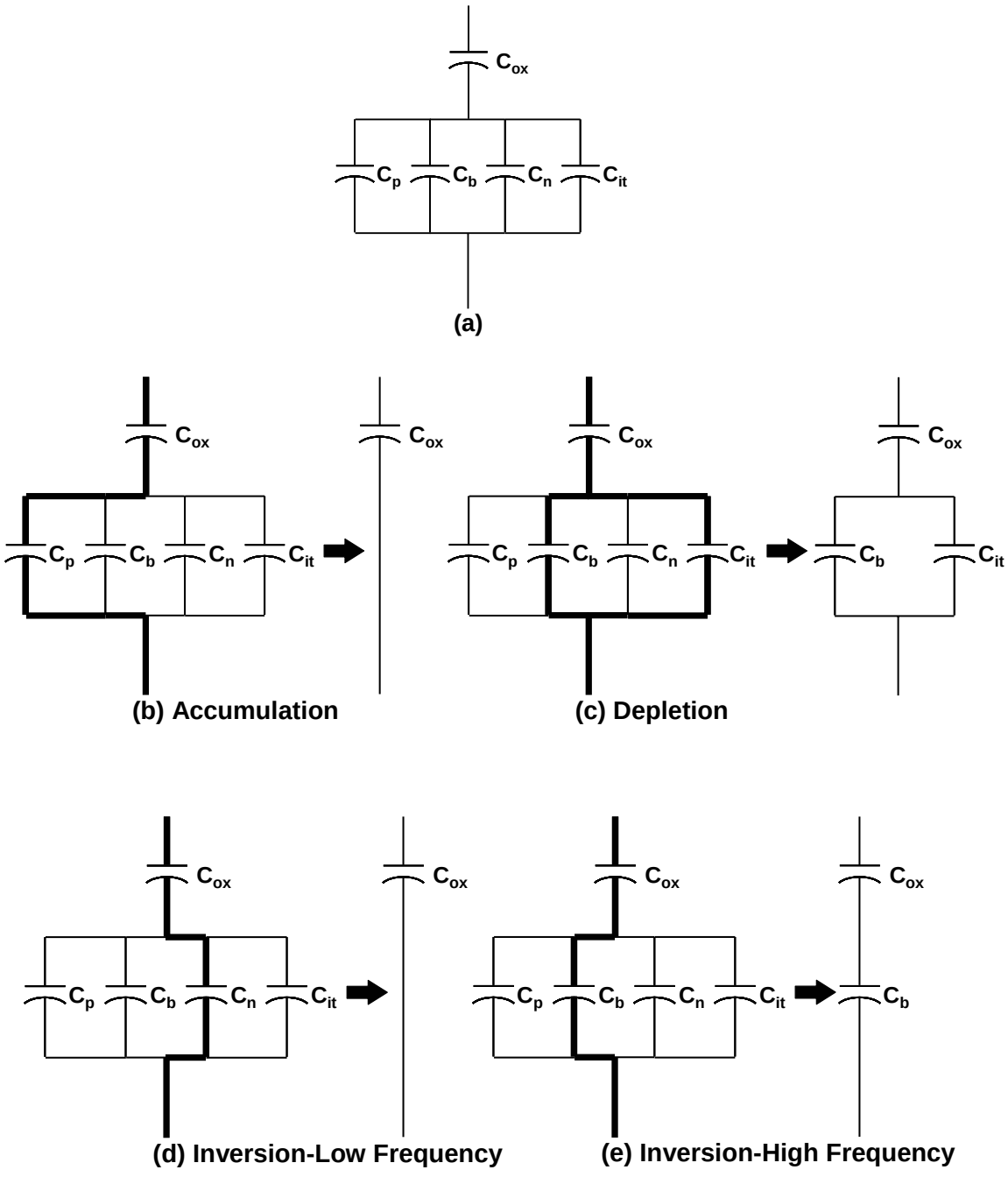


Fig. 2.5 *Capacitances of an MOS capacitor for various bias condition*

2.2.2 Conductance Method for Interface Trap Density

The conductance method, proposed by Nicollian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it}. Interface trap densities of 10^9 $cm^{-2}eV^{-1}$ and lower can be measured. It is also the most complete method, because it yields Dit in the depletion and weak inversion portion of the band gap, the capture cross-sections for majority carriers, and information about surface potential fluctuation. The technique is based on measuring the equivalent parallel conductance G_p of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in Figure 2.6 (a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_S, and the interface trao capacitance C_{it}. The capture-emission of carriers by D_{it} is a lossy process, represented by the resistance R_{it}. It is convenient to replace the circuit of Figure 2.6 (a) by that in Figure2.6 (b), where C_p and G_p are given by

$$C_P = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2} \qquad \text{.....} \quad (2.6)$$

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \qquad \text{.....} \quad (2.7)$$

where $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it}C_{it}$, the interface trap time constant, given by $\tau_{it} = [\upsilon_{th}\sigma_P N_A \exp(-q\phi_s/kT)]^{-1}$. Dividing G_p by ω makes Eq. (2.7) symmetrical in $\omega\tau_{it}$. Eq. (2.6) and Eq. (2.7) are for interface traps with a single energy level in the band gap. Interface traps at the SiO_2-Si interface, however, are

continuously distributed in energy throughout the Si band gap. Capture and emission occurs primarily by trap located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] \qquad \text{.....} \quad (2.8)$$

Equations (2.7) and (2.8) show that the conductance is easier to interpret than the capacitance, because Eq. (2.7) does not require C_s. The conductance is measured as a function of frequency and plotted as G_p/ω versus ω. G_p/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_p/q\omega$. For Eq. (2.8) we find $\omega \approx 2/\tau_{it}$ and $D_{it} = 2.5G_p/q\omega$ at the maximum. Hence we determine D_{it} from the maximum G_p/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis. G_p/ω versus f plots, calculated according to Eq. (2.7) and (2.8).

Experimental G_p/ω versus ω curves are generally broader than predicted by Eq. (6.49), attributed to interface trap time constant dispersion caused by surface potential fluctuations due to non-uniformities in oxide charge and interface traps as well as doping density. Surface potential fluctuations are more pronounced in *p*-Si than in *n*-Si. Surface potential fluctuations complicate the analysis of the experimental data. When such fluctuations are taken into account, Eq. (2.8) becomes

$$\frac{G_P}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] P(U_s)\, dU_s \qquad \text{.....} \quad (2.9)$$

where $P(U_s)$ is a probability distribution of the surface potential fluctuation given by

$$P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(U_s - \overline{U}_s)^2}{2\sigma^2}\right) \qquad \text{.....} \quad (2.10)$$

with $\overline{U}_S$ and σ the normalized mean surface potential and standard deviation,

respectively. An approximate expression giving the interface trap density in terms of the measured maximum conductance is

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{\max} \qquad \text{.....} \quad (2.11)$$

Capacitance meters generally assume the device to consist of the parallel C_m-G_m combination in Figure 2.6 (c). A circuit comparison of Figure 2.6 (b) to Figure 2.6 (c) gives G_p/ω in terms of the measured capacitance C_m, the oxide capacitance, and the measured conductance G_m as

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \qquad \text{.....} \quad (2.12)$$

assuming negligible series resistance. The conductance measurement must be carried out over a wide frequency range. The portion of the band gap probed by conductance measurements is typically from fratband to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50mV or less to prevent harmonics of the signal frequency giving rise to spurious conductance. The conductance depends only on the device area for a given D_{it}. However, a capacitor with thin oxide has a high capacitance relative to the conductance, especially for low D_{it} and the resolution of the capacitance meter is dominates by the out-of-phase capacitive current component. Reducing C_{ox} by increasing the oxide thickness helps this measurement problem.

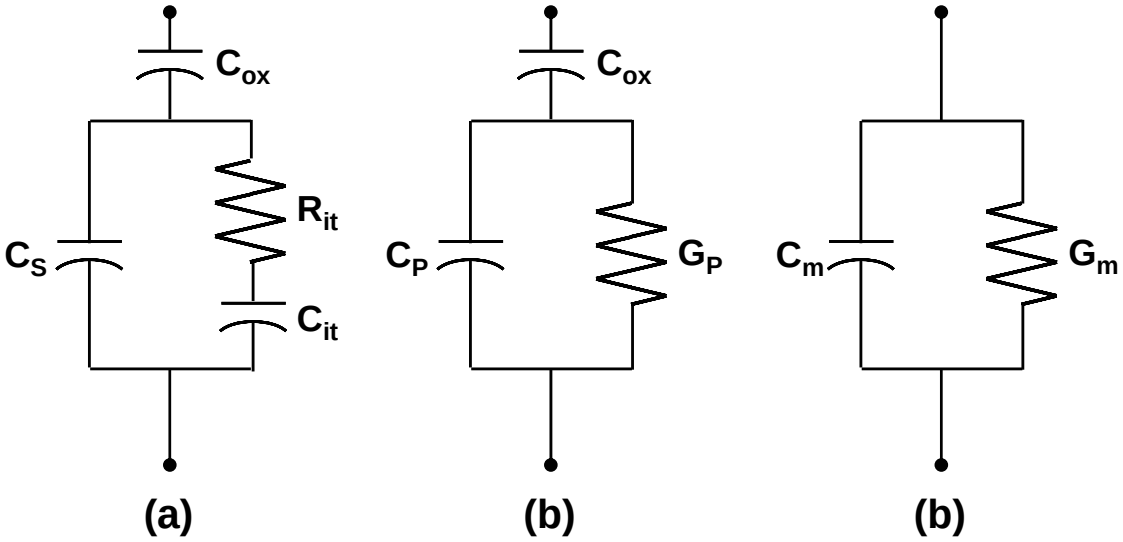


Fig. 2.6 *Equivalent circuits for conductance measurement; (a) MOS capacitor with interface trap time constant* $\tau_{it} = R_{it}C_{it}$*, (b) simplified circuit of (a), (c) measured circuit.*

2.2.3 Gate Leakage Current – Voltage (J-V) Characteristics

One of the main concepts of replacing the high-k gate dielectrics with SiO_2 is to suppress the gate leakage current. Thus, it is enormously important to measure the gate leakage current-voltage (J-V) characteristics. In addition, the properties of high-k films, such as the barrier height, effective mass, are obtained by analyzing the carrier transport mechanisms from the leakage current. To investigate the voltage and temperature dependence of gate leakage current, it is able to identify the carrier conduction mechanisms experimentally [2.3]. J-V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.).

2.3 Characterization of nMOSFET

2.3.1 Threshold Voltage

As the MOSFET is the fundamental switching devices in the LSI circuits, the threshold voltage V_{th} is an important parameter of the MOSFET. The threshold voltage can be determined by plotting I_{ds} versus V_g at low drain voltage, typically 50-100mV, as shown in Figure 2. 7. The extrapolated intercept of the linear portion of the I_{ds} versus V_g curve with the V_g –axis gives the V_g value. It needs to regard the point of slope because the threshold voltage varies the point of I_{ds} - V_g slope. It is commonly used the point of slope on the I_{ds} - V_g curve by a maximum in the transconductance, fit a straight line to the I_{ds} - V_g curve at that point and extrapolate to I_{ds} = 0, as shown in Figure 2. 7.

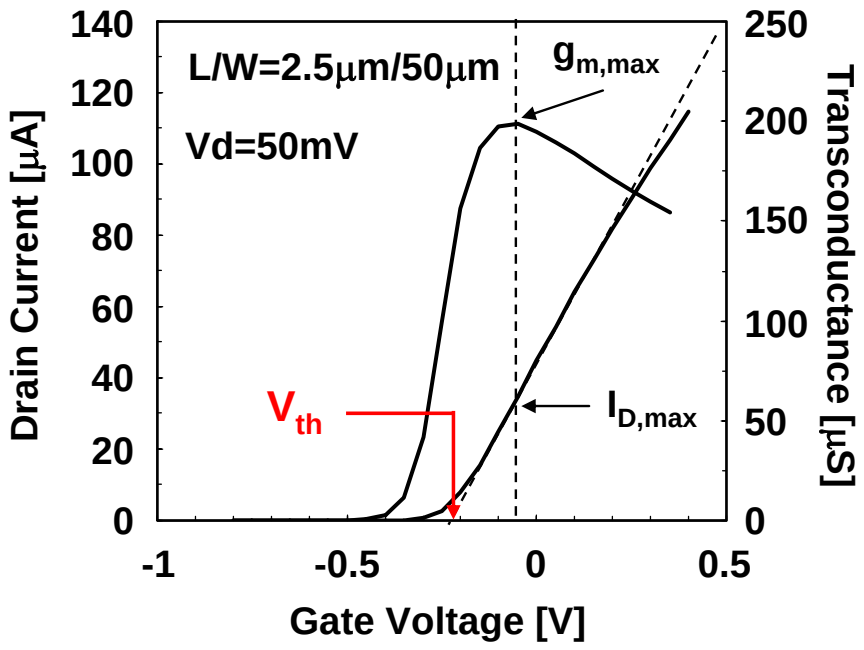


Fig. 2.7 *Threshold voltage determination by the linear extrapolation technique*

2.3.2 Subthreshold Slope

As shown in Figure 2.7, the drain current rapidly approach to zero below the threshold voltage on a linear scale. On a logarithmic scale, however, the drain current remains nonnegligible level even below the V_{th}. This is because the inversion charge abruptly does not to drop zero. The slope is usually expressed as the subthreshold slope *S.S.* in Figure 2.8. This value is that gate voltage necessary to change the drain current by one decade, and given by

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \quad \text{.....} \quad (2.13)$$

where k is a Boltzmann's constant, T is temperature, q is a electronic charge, C_{dm} is a depletion-layer capacitance. If the interface trap density is high, the subthreshold slope may be graded. Because the capacitance attributed to the interface trap is in parallel with the depletion-layer capacitance.

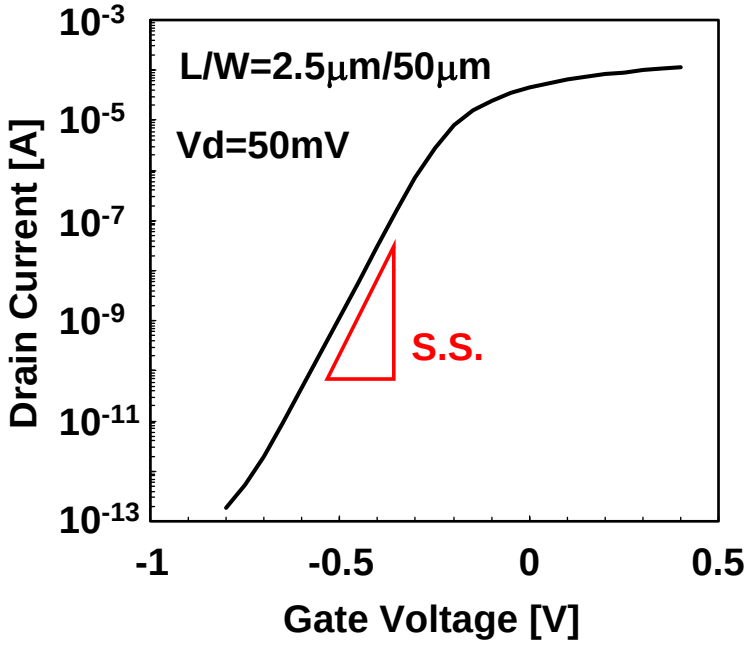


Fig. 2.8 *Threshold voltage determination by the linear extrapolation technique*

2.3.3 Mobility Extraction Technique ~Split C-V Measurement~

The effective inversion layer mobility in MOSFET is a very important parameter for device analysis, design and characteristics. As the effective inversion mobility shows sensitivity to device properties or interface properties, it can be also used to probe the high-k gate dielectrics properties.

The effective mobility, μ_{eff} , is defined in terms of the measurement of drain current, I_d, of a MOSFET at low drain voltage, V_d, in the linear region as [2.4]

$$\mu_{eff} = \frac{L}{W} \cdot \frac{I_d}{V_d} \cdot \frac{1}{Q_{inv}} = \frac{L}{W} \cdot g_d \cdot \frac{1}{Q_{inv}} \qquad \text{.....} \quad (2.14)$$

where $g_d = I_d/V_d$ is the channel conductance, Q_{inv} is the inversion layer charge. The channel conductance is calculated from differential I_d-V_g measurements at 20mV and 40mV as shown in Figure 2.9 to compensate the degradation of the channel conductance due to leakage current. For accurate extraction of effective mobility, accurate value of Q_{inv} must be used in Eq. (2.14). A Split C-V measurement is one of the extraction techniques for inversion layer charge accurately. Figure 2.10 represents the Split C-V measurement arrangement. The inversion layer charge is obtained from the voltage integral of a gate-channel capacitance as shown in Figure 2.11. The inversion layer charge Q_{inv} can be written as

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc}(V_g) dV_g \qquad \text{.....} \quad (2.15)$$

where C_{gc} is the gate-to-channel capacitance [2.5]. Similarly, the depletion layer charge Q_b is also obtained due to integrate the gate-body capacitance, C_{gb} , from flatband voltage toward the inversion as shown in Figure 2.12.

$$Q_b = \int_{V_{FB}}^{V_g} C_{gb}(V_g) dV_g \qquad \text{.....} \quad (2.16)$$

The effective electric field E_{eff} can be expressed as [2.4]

$$E_{eff} = \frac{1}{\varepsilon_{Si}}\left(\eta Q_{inv} + Q_b\right) \qquad \text{.....} \quad (2.17)$$

where η are 1/2 for electrons and 1/3 for holes.

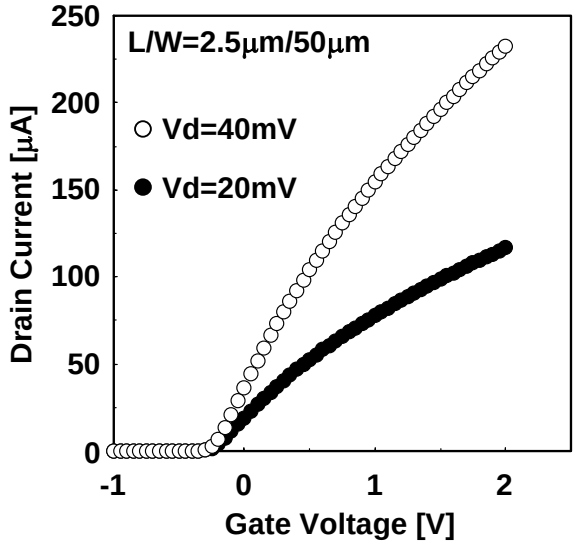


Fig. 2.9 *I_d-V_g measurements at 20mV and 40mV*

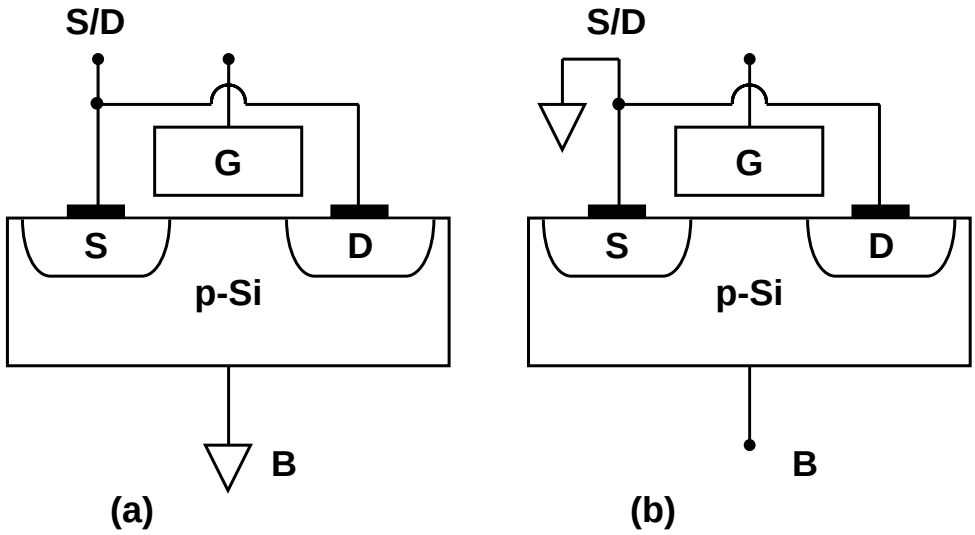


Fig. 2.10 *Configuration for (a) gate-to-channel, (b) gate-to-body capacitance measurements*

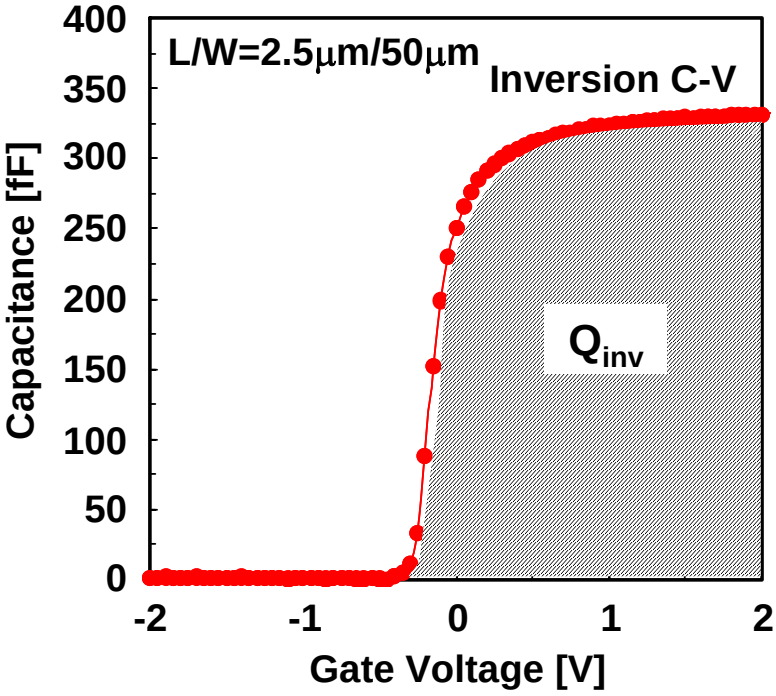


Fig. 2.11 *Gate-to-channel capacitance of nMOSFET*

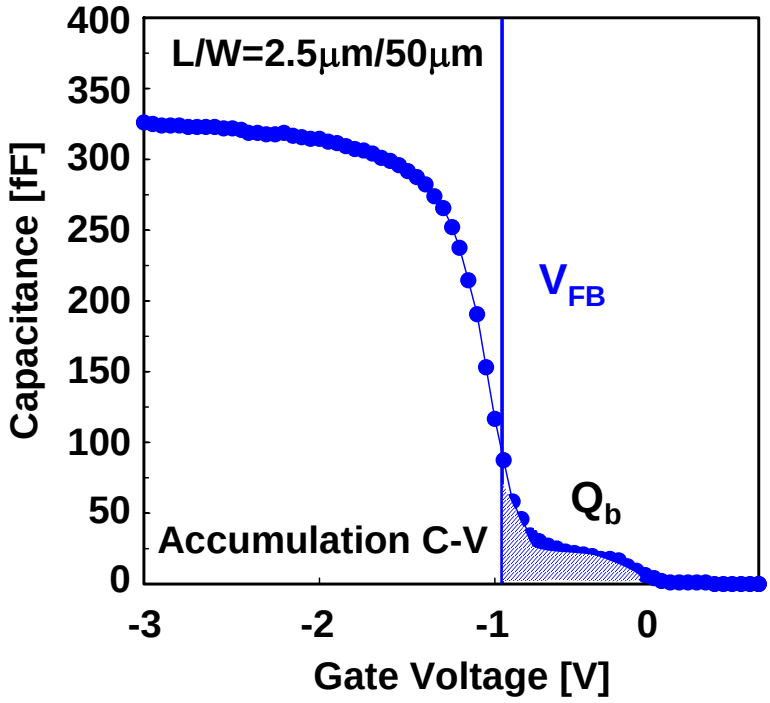


Fig. 2.12 *Gate-to-body capacitance of nMOSFET*

2.3.4 Charge Pumping methods

The surface region under the gate oxide between the source and drain is formed the inversion layer and is crucial for current conduction in a MOSFET. Hence, the carriers in the inversion layer are strongly affected by the gate oxide-Si substrate interface properties. In addition, as the high-k gate dielectrics is not thermally-oxidized film but deposited film, the evaluation of interface properties between the high-k gate dielectrics and Si substrate is crucially importance.

The charge pumping method is one of the sensitive methods for the characteristics of the interface trap density which is located at the high-k gate dielectrics-Si substrate interface [2.6]. Figure 2.13 shows the circuit diagram of the charge pumping measurement. The MOSFET gate is connected to a pulse generator. The MOSFET source and drain are tied together and slightly reverse biased. The time varying gate voltage is sufficiently amplitude for the surface under the gate to be driven into inversion and accumulation as shown in Figure 2.14. The rise and fall times t_r and t_f are fixed value, 100nsec. The Charge pumping current which due to recombination processes at the interface defects is measured at the substrate. The interface trap density, N_{it}, is written as

$$N_{it} = \frac{I_{cp}}{qfA} \qquad \text{.....} \quad (2.18)$$

where q is the elementary charge, f is the frequency, A is the channel area. The waveforms can be constant Vamp and pulsing with varying the base voltage from inversion to accumulation as in Figure 2.15 (a) and Figure 2.15 (b) represents the charge pumping current with varying the base voltage from inversion to accumulation. The I_{cp} in the Eq. (2.18) is used for the maximum I_{cp} value as show in Figure 2.15 (b).

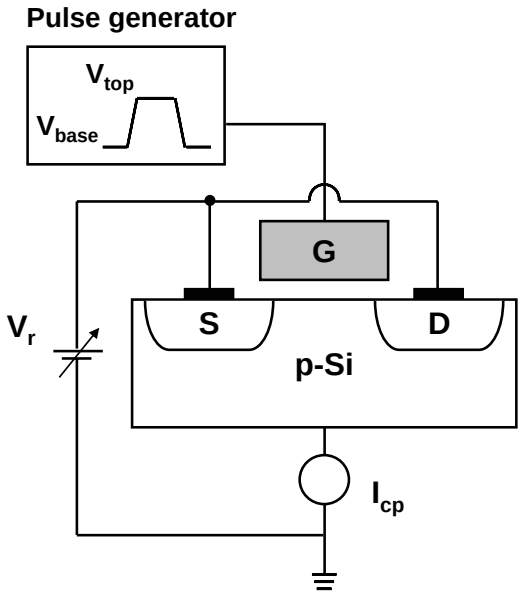


Fig. 2.13 *Measurement circuit diagram of charge pumping method*

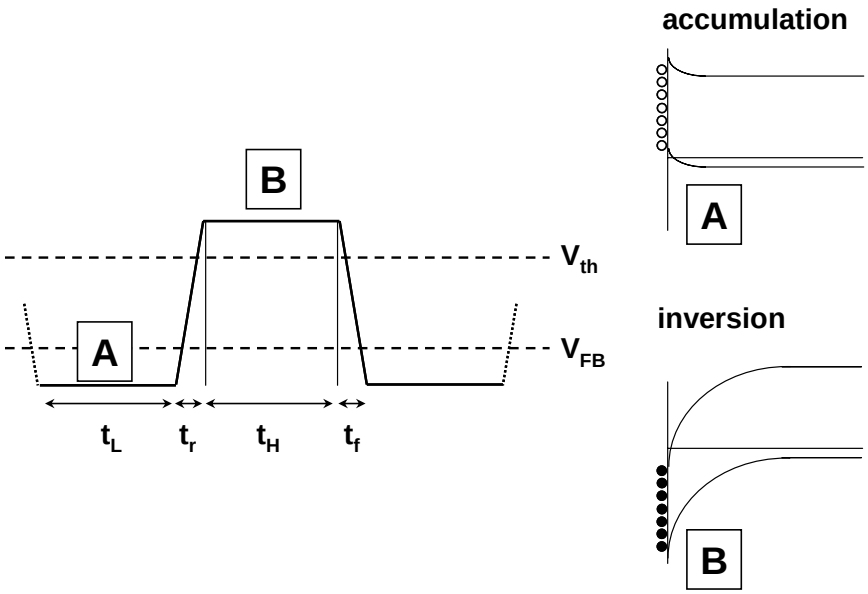
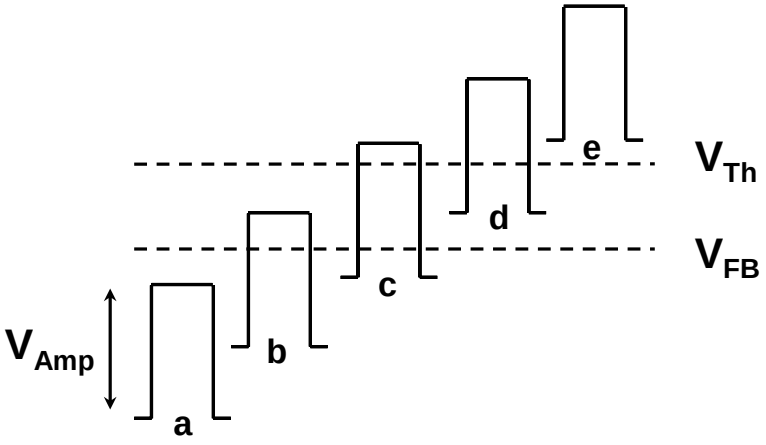
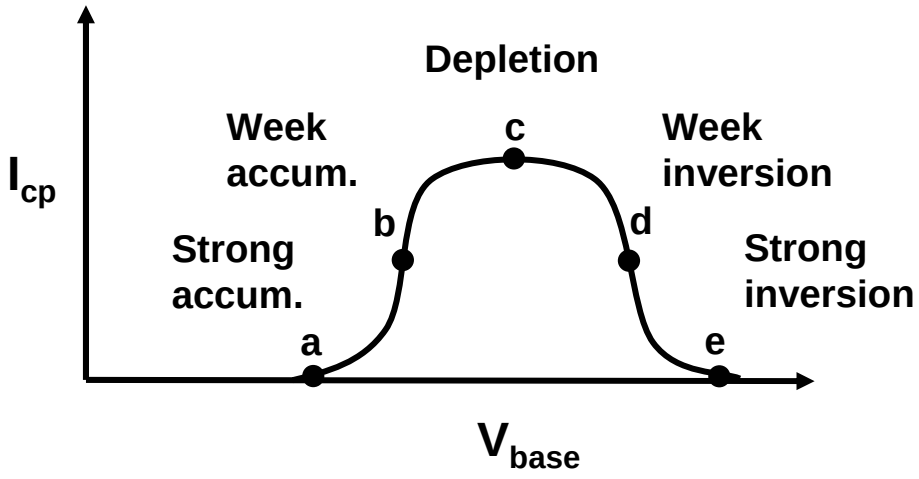


Fig. 2.14 *Sweeping between inversion and accumulation*



(a)



(b)

Fig. 2.15 (a) *Charge pumping waveform and* ***(b)*** *Charge pumping current versus base voltage*

Figure 2.16 shows the band diagrams for changing the interface from accumulation to inversion under the action of periodic gate pulses. The interface traps are filled with electrons from source/drain during t_r and the electrons in traps empty into substrate during t_f.

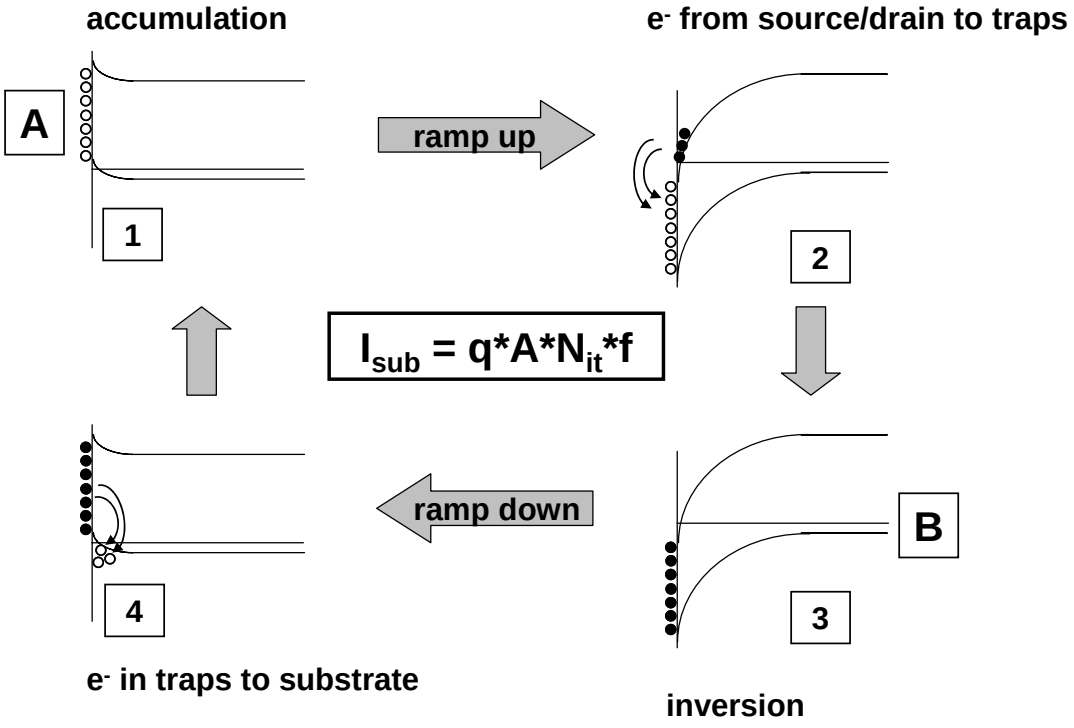


Fig. 2.16 *Band diagrams applied periodic gate pulses*

2.4 References

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Chapter 3 Characterization of Sc_2O_3 Single-Layer MOS capacitors

3.1 Introduction

As shown in Figure 1.7, there are many scattering sources in the MOSFET with high-k gate dielectrics. One of the most concerns is the defects in the high-k gate dielectrics. Electrically active defects are undesirable. Firstly, trapped charge in these defects causes the threshold voltage shift which means the LSI is inoperative. Secondly, trapped charge scatters the carriers in the inversion layer which means the reduced drain current. In addition, defects become the source of breakdown of oxide. Thus, few bulk defects are required. It has been reported that oxygen vacancies exist in large numbers in the high-k gate dielectrics compared to SiO_2 [3.1, 3.2]. It would appear that the oxygen vacancies in the high-k gate dielectrics are cause of defects. Thus, it is necessary to choice the high-k material which can suppress the oxygen vacancies.

According to the standard Gibbs free energy, the Sc_2O_3 has great affinity with oxygen as shown in Table 1.1 [3.3]. Firstly, it has to be determined the basic properties

of the Sc_2O_3 before the incorporation of Sc_2O_3 into host high-k dielectrics, In this section, the dielectric constant of Sc_2O_3, Thermal stability, carrier transport mechanisms are described. In addition, the barrier height of the Sc_2O_3 is estimated from electrical characteristics.

3.2 C-V Characteristics of Sc_2O_3 MOS Capacitors

It is very important to clarify the basic electrical properties of Sc_2O_3 single layer gate insulator. Firstly, Sc_2O_3 MOS capacitors were fabricated by e-beam evaporation at 300^{o}C in ultra-high vacuum chamber as shown in Figure 2.2. The physical thickness of the Sc_2O_3 film is about 5-6nm. Post Metallization Annealing (PMA) was performed at 300^{o}C, 500^{o}C and 700^{o}C in N_2 ambient for 5 min.

Figure 3.1 shows the C-V characteristics of the Sc_2O_3 MOS capacitors as a function of PMA temperature. The C-V curve of as-deposited sample was not measured due to high gate leakage current. PMA 300^{o}C sample shows large C-V hysteresis which indicates the large amount of defects at the high-k oxide/Si interface. Because the Sc_2O_3 has great affinity with oxygen, the reactivity of the Sc_2O_3 and the Si substrate is very low and sharp. As a result, it can be considered that a many trap sites are remained at the high-k oxide/Si interface. On the other hand, as the C-V hysteresis of PMA 500^{o}C and 700^{o}C are negligible small, the accumulation capacitance is drastically decreased with increasing the annealing temperature as shown in Figure 3.1. Figure 3.2 (a) represents the EOT (Equivalent-Oxide Thickness) change as a function of PMA temperature. The EOT values are estimated using NCSU CVC program. The EOT change of Sc2O3 is almost identical compared to La_2O_3. This increase of the EOT with increasing PMA temperature indicates the formation of the interfacial layer which is low dielectric constant. The formation of the low dielectric constant interfacial layer is one of the most important issues. It is important how to suppress the growth of interfacial layer [3.4]. It is speculated that the reduction of the C-V hysteresis and increasing the EOT are due to formation of the interfacial layer.

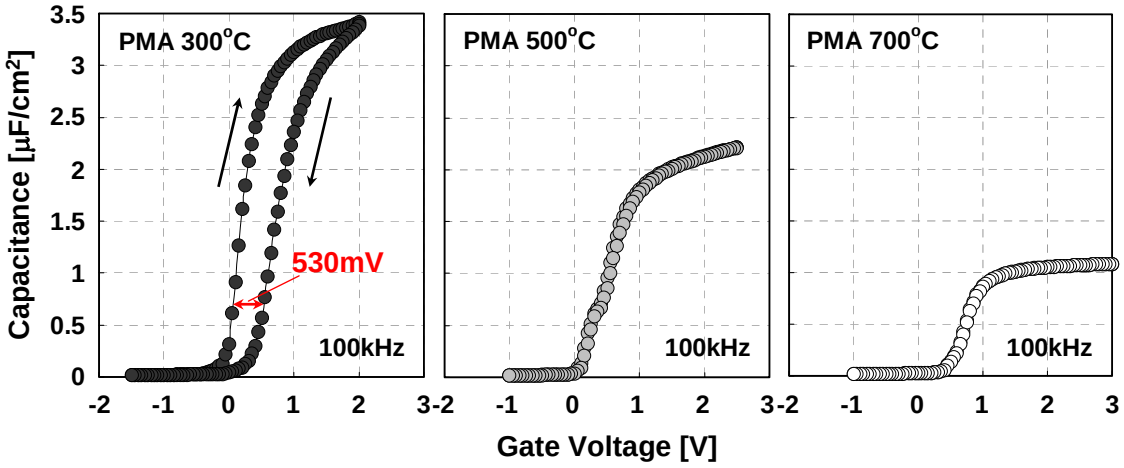
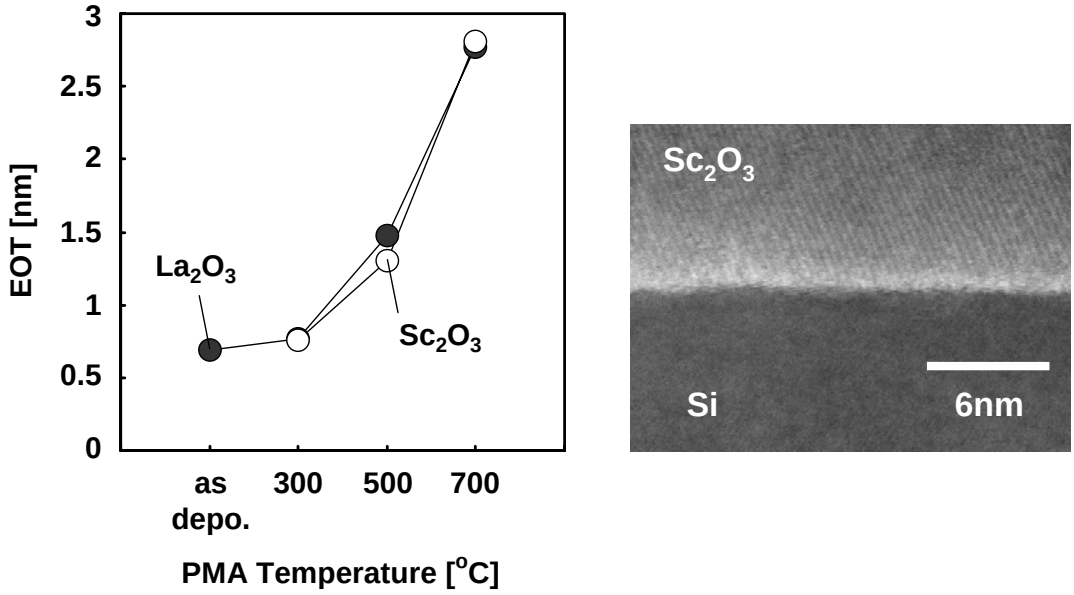


Fig. 3.1 *C-V characteristics of Sc_2O_3 MOS capacitors as a function of annealing temperature*



(a) **(b)**

Fig. 3.2 *C-V characteristics of Sc_2O_3 MOS capacitors as a function of annealing temperature*

(a) *EOT change as a function of annealing temperature*

(b) *Cross-section of TEM image of PMA 500°C sample*

In order to confirm the interfacial layer growth, the high-k/Si interface was investigating by Transmission-Electron Microscopy (TEM). Figure 3.2 (b) shows the cross-section TEM image of PMA 500^{o}C sample. No interfacial layer was confirmed from Figure 3.2 (b). It was reported that the reactivity between the scadium oxide and Si substrate is lower [3.5]. That is a great advantage of incorporation of Sc_2O_3 into host high-k materials because the Sc_2O_3 may be able to suppress the interfacial layer growth by incorporated into another high-k material. As the physical thickness can be determined by TEM image, the dielectric constant of the Sc_2O_3 was calculated using the following equation as written in section 1.

$$T_{EOT} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} T_{phy}$$

It was obtained the dielectric constant of the Sc_2O_3 , $\varepsilon_{Sc_2O_3}$, is about 15. This value is well coincident with previous report [3.6].

3.3 Carrier transport mechanisms in Sc_2O_3 Gate Oxide

In the previous section, it was mainly investigated the C-V characteristics and interface properties by TEM. In this section, the gate leakage current is mainly investigated. To analyze the gate voltage and temperature dependence with gate leakage current, it is able to identify the carrier transport mechanisms of the Sc_2O_3 gate oxide. In the previous section, the PMA 500^{o}C sample shows no interfacial layer formation. Thus the carrier transport mechanisms of the PMA 500^{o}C sample are described without interfacial layer.

Figure 3.3 (a) shows the gate current density-voltage (J-V) characteristics with various temperatures and Figure 3.3 (b) shows the Arrhenius plot of gate leakage current for gate voltages from 0.5V to 2.5V. As the Si substrate is n-type, the electrons were injected from Si substrate, namely the sample in accumulation mode. The gate leakage current is increasing with increasing temperature independent of gate voltage. It indicates that the thermal excitation process is dominant such as the Schottky emission or the Poole-Frenkel emission as shown in Figure 3.4 [3.7]. The Schottky emission process is thermoionic over the metal-insulator barrier or the insulator-semiconductor barrier is responsible for carrier transport. The Pool-Frenkel emission is due to emission of trapped electrons into the conduction band. The supply of electrons from the traps is through thermal excitation. For trap states with Coulomb potentials, the expression is similar to that of the Schottky emission. However, the barrier height is the depth of the trap potential well. In particular, it is considered that the Poole-Frenkel emission is dominant mechanism because there are many defects or trap states in the high-k dielectrics.

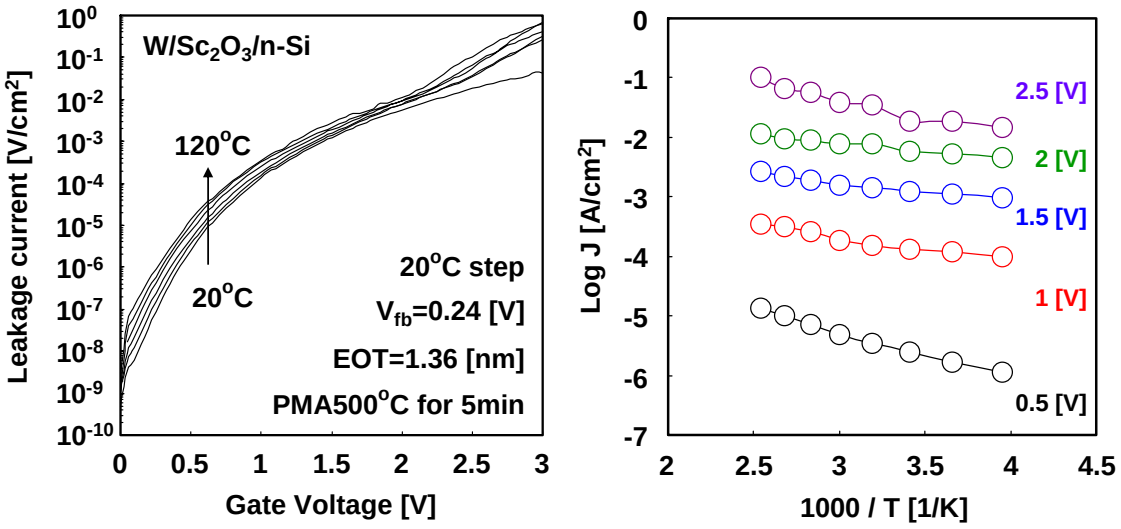


Fig. 3.3 *Temperature dependence of gate leakage current*

(a) *Current-voltage characteristics*

(b) *Arrhenius plot of gate leakage current*

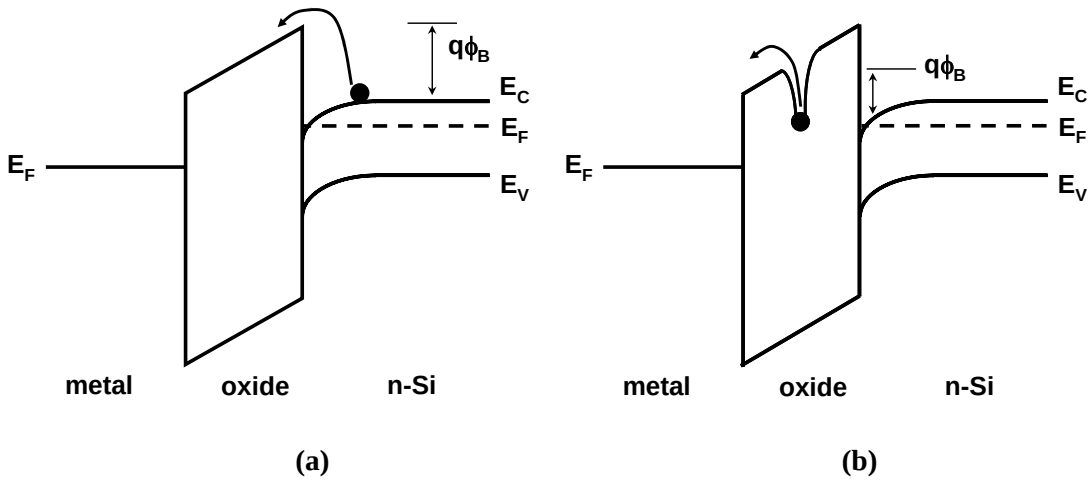


Fig. 3.4 *Energy band diagrams of conduction mechanisms*

(a) *Schottky emission*

(b) *Pool-Frenkel emission*

Figure 3.5 (a) and (b) represent the Schottky and Pool-Frenkel plots of the experimental value, respectively. The red curves are fitting lines calculated by following equation. The Schottky emission process is written as [3.8],

$$J = A^{*}T^{2}\exp\left(\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_i}\right)}{kT}\right) \quad \text{.....} \quad (3.1)$$

where A^{*} is the modified Richardson's constant, T is the temperature, q is the elementary charge, ϕ_B is the barrier height, E is the electric field in insulator, ε_i is the insulator permittivity, k is the Boltzmann's constant, and the Poole-Frenkel emission process is written as,

$$J = \sigma(0)E\exp\left(\frac{-q\left(\phi_B - \sqrt{qE/\pi\varepsilon_i}\right)}{kT}\right) \quad \text{.....} \quad (3.2)$$

where $\sigma(0)$ is the low field conductivity. The electric field in insulator, E, was extracted from C-V curve as shown in Figure 3.1 by following equation. The electric field in insulator is written as,

$$E = \left(V_g - \psi_S - V_{FB}\right)/T_{high-k} \quad \text{.....} \quad (3.3)$$

where V_g is the gate voltage, ϕ_S is the surface potential, V_{FB} is the flatband voltage, $T_{high\text{-}k}$ is the physical thickness of high-k gate dielectrics. In the case of the Schottky emission plots, the experimental results do not fit the Schottky emission theory very well, as shown in Figure 3.5 (a). In addition, the dielectric permittivity extracted from the Eq. (3.1) and the slope of the fitting line is about 7-10. This value is lower compared to the dielectric permittivity extracted from the C-V characteristics as shown in Figure 3.1. These results indicate that the Shottky emission process is not dominant mechanism for the Sc_2O_3 gate dielectrics at PMA 500^{o}C.

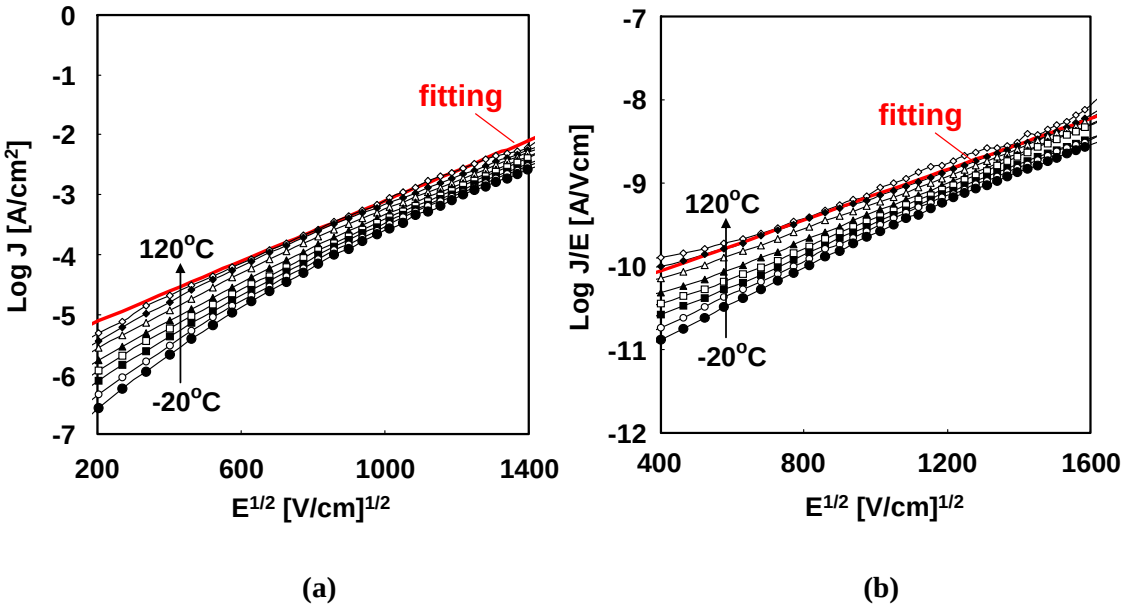


Fig. 3.5 *Theoretical and experimental plots of gate leakage current*

(a) *Schottky emission plots*

(b) *Pool-Frenkel emission plots*

On the other hand, for the case of the Poole-Frenkel emission process, the experimental results fit the theoretical plot compared to the Schottky emission process as shown in Figure 3.5 (b). The dielectric permittivity extracted from the Eq. (3.2) and the slope of the fitting line, however, is more than 25. This value is so high compared to the dielectric permittivity extracted from the C-V characteristics that the Poole-Frenkel emission process is also not the dominant transport mechanism. Neither the Schottky emission nor the Poole-Frenkel emission is dominant carrier transport mechanisms for the Sc_2O_3 gate dielectrics at PMA 500^{o}C. However, the experimental results show the temperature dependence. It was reported that the carrier transport mechanism of ZrO2

and Ta2O5 gate dielectrics was explained by the trap-assisted tunneling model which take into account the tunneling of electrons through traps located below the conduction band of the high-k gate dielectrics [3.9]. Figure 3.6 shows the schematic band diagram of trap-assisted tunneling and the trap-assisted tunneling model is given by,

$$J \propto N_t \exp\left[\left(qV_{ox} - \phi_1 + \phi_t\right)/k_B T\right] \qquad \text{.....} \quad (3.4)$$

where N_t is the trap density, V_{ox} is the voltage across the gate insulator, ϕ_1 is the barrier height, ϕ_t is the trap level energy.

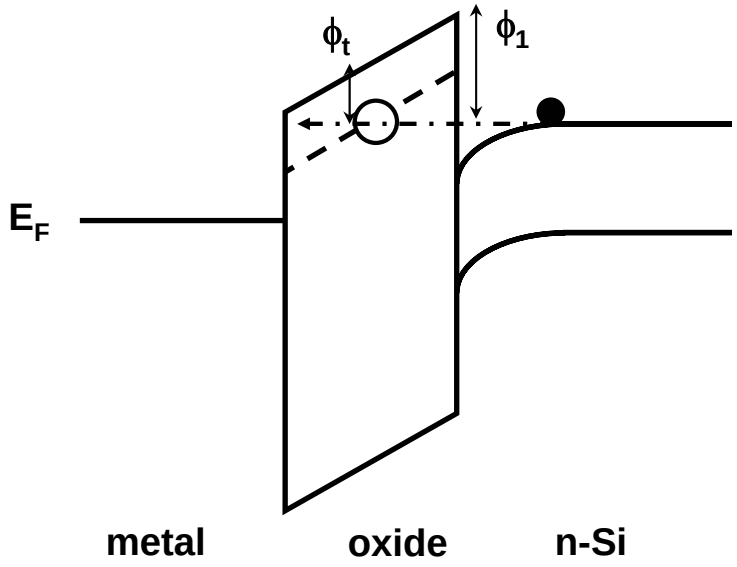


Fig. 3.6 *Schematic energy band diagram of the trap-assisted model*

As shown in Eq. (3.4), the barrier height ϕ_1 is necessary to obtain the theoretical plots using Eq. (3.4). At the high gate voltage region in Figure 3.3 (a), the gate leakage currents show the different behaviors compared to the low gate voltage region. It is considered that the Fowler-Nordheim tunneling may be occurred. Consequently, the barrier height ϕ_1 is evaluated from the Fowler-Nordheim plots. The Fowler-Nordheim

tunneling process is given by,

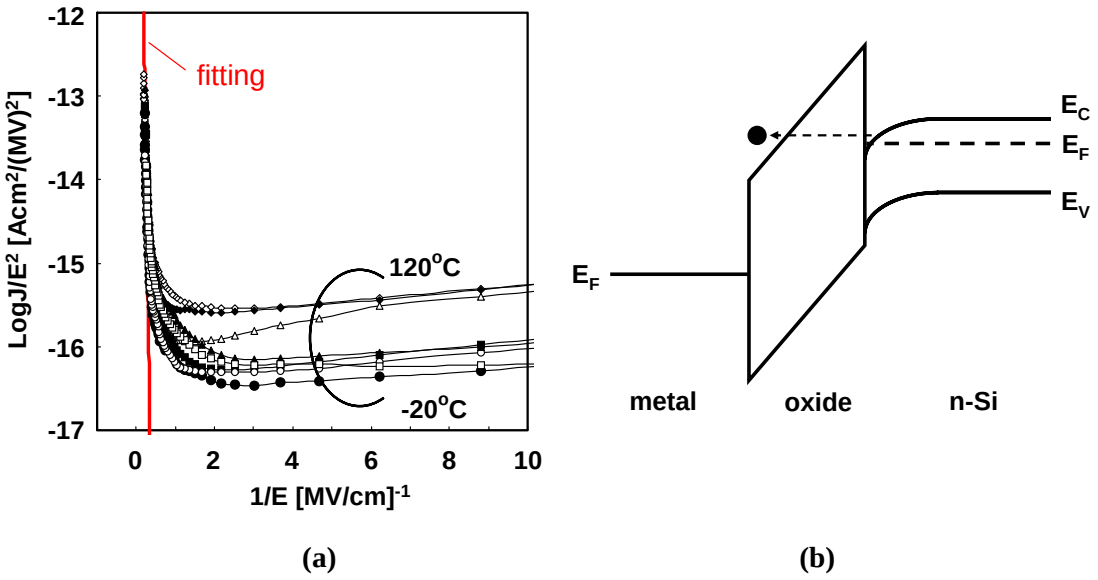
$$J = \frac{q^3}{16\pi^2 \hbar \phi_B} E \exp\left[-\frac{4}{3} \frac{\sqrt{2m_{ox}^*}\phi_B}{\hbar q} \frac{1}{E} \right] \quad \text{.....} \quad (3.5)$$

where $\hbar$ is Planck's reduced constant, ϕ_B is the barrier height at the semiconductor-oxide interface, m_{ox}^* is the electron effective mass in the insulator. Figure 3.7 (a) shows the theoretical and experimental plots of the Fowler-Nordheim tunneling current. The experimental plots show the same behaviors which are independent of temperature because the Fowler-Nordheim mechanism is not the thermal excitation but the tunneling process. Figure 3.7 (b) shows the energy band diagram of the Fowler-Nordheim tunneling. The electrons tunnel into the conduction band of the oxide layer. Hence, the Fowler-Nordheim tunneling occurs when the gate voltage is high and leakage currents do not depend on the temperature. The barrier height at the semiconductor-oxide interface and electron effective mass in the insulator can be extracted from Eq. (3.5) and fitting curve. The barrier height ϕ_B is 1.2eV and the electron effective mass is $0.45m_o$, where m_o is the free-electron mass from Eq. (3.5) and fitting curve. The above extracted barrier height ϕ_B = 1.2eV is not included in the Image-Force-Induced Barrier Lowering. Image-force-induced barrier lowering is not negligible and has to be included in the more accurate theories of Fowler-Nordheim tunneling [3.10]. The actual energy barrier to emission is $\phi_o - \Delta\phi$ and $\Delta\phi$ is given by,

$$\Delta\phi = \sqrt{\frac{q^3 E}{4\pi\varepsilon_i}} \quad \text{.....} \quad (3.6)$$

Thus, the calculated value by Eq. (3.6), $\Delta\phi$, is 0.21eV.

Figure 3.8 represents energy band diagram including in the image-force-induced barrier lowering and ϕ_o equals 1.41eV.



(a) **(b)**

Fig. 3.7 *The Fowler-Nordheim tunneling currents*

(a) *The theoretical and experimental plots of gate leakage current*

(b) *Energy band diagram of the Fowler-Nordheim tunneling*

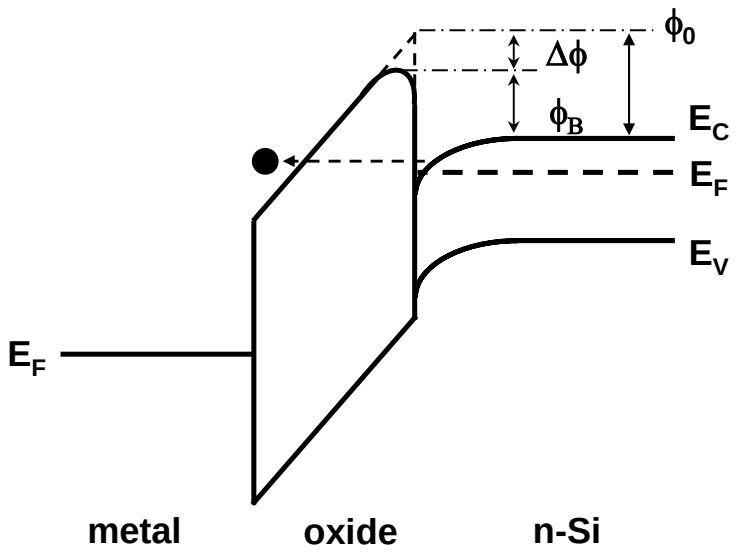


Fig. 3.8 *Schematic energy band diagram including in the Image-Force-Induced Barrier Lowering*

As the accurate barrier height can be extracted above, the leakage current characteristics are analyzed by trap-assisted tunneling model. Figure 3.9 (a) shows the leakage current as a function of the inverse of temperature. The red line is the theoretical plots using Eq. (3.4) where ϕ_1 is 1.41eV. Figure 3.9 (b) represents the trap energy levels estimated by Eq. (3.4) and the trap energy level ϕ_t is about 0.5-0.6eV below the conduction band. This value is shallow trap level compared to the HfO2 which equals 1.2eV below the conduction band [3.11]. This result indicates that the shallow trap states would easily trap carriers.

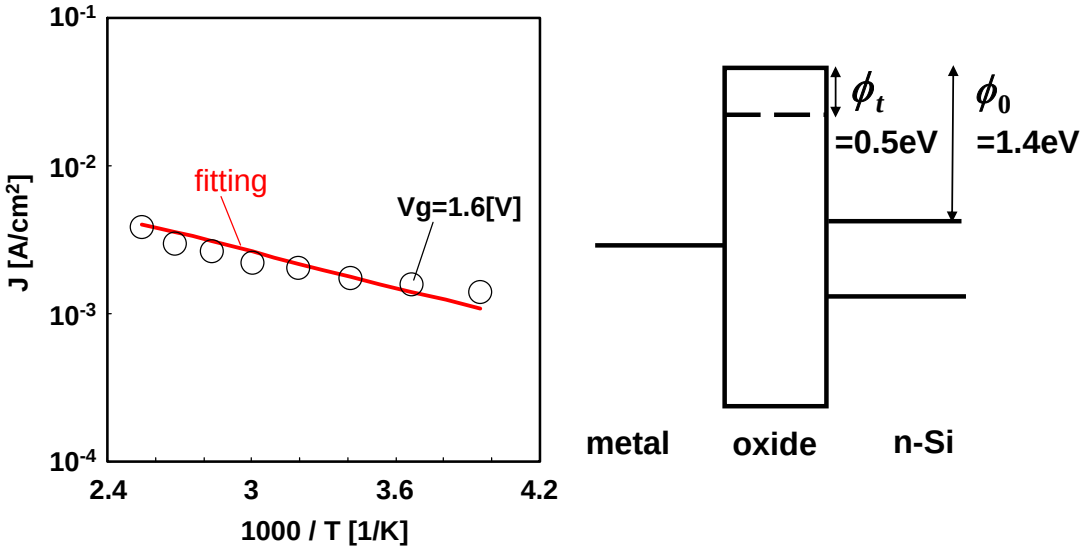


Fig. 3.9 *The trap-assisted tunneling mechanism*

(a) *The theoretical and experimental plots of trap-assisted tunneling current*

(b) *Estimated trap energy level. Trap states 0.5eV below conduction band*

3.4 Summary

In order to clarify the basic properties of Sc_2O_3 gate dielectrics, the electrical characteristics of MOS capacitor with Sc_2O_3 gate dielectrics were investigates.

From the C-V characteristics, Sc_2O_3 gate dielectrics showed the large C-V hysteresis at PMA 300^{o}C sample. On the other hand, the C-V hysteresis of PMA 500^{o}C and 700^{o}C samples was negligible small. It was confirmed that no interfacial layer was formed at PMA 500^{o}C sample. The EOT change with increasing the annealing temperature was almost identical compared to La_2O_3 gate dielectrics. Therefore, thermal stability of Sc_2O_3 films is same level as that of the La_2O_3. On the other hand, after PMA 500^{o}C, the formation of interfacial layer was not observed. This is a great advantage of Sc_2O_3 gate dielectrics. This result indicates that the incorporation of Sc_2O_3 has possibilities to suppress the interfacial layer growth.

The carrier transport mechanisms of Sc_2O_3 gate dielectrics were investigated from the temperature dependence of the gate leakage current. At the high electric field region, the Fowler-Nordheim tunneling was observed. It is considered that the trap-assisted tunneling is dominant mechanism at the low and middle electric field region. The barrier height at the semiconductor-oxide interface is 1.41eV including the image-force-induced barrier lowering. The trap energy level is 0.5eV below the conduction band which is easily trap carriers.

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Chapter 4 Characterization of La-Sc Oxides Complex Gate MOS capacitors

4.1 Introduction

In the chapter 3, the basic properties of Sc_2O_3 single-layer MOS capacitors were described. The dielectric constant of Sc_2O_3 is low about 15 and it is difficult to use a single-layer. On the other hand, no interfacial layer formation was observed after performed 500^{o}C annealing. This result is extremely informative because it may be suppressed the formation of interfacial layer due to incorporation of Sc_2O_3 into another high-k materials. It was reported that amorphous $LaScO_3$ thin films on silicon have a dielectric constant of 22-24 and a band offsets between semiconductor–oxide were more than 1eV for both the conduction and valence bands. In addition, the interface between semiconductor–oxide is atomically sharp [4.1]. All these parameters meet the requirements of gate dielectrics.

In this charter, the electrical characteristics of La-Sc oxides complex gate MOS capacitors.

4.2 Experimental

The concern of complex high-k oxides or ternary high-k dielectrics is how to control the composition ration of the films. As shown in the Figure 2.2, the source of e-beam evaporation is used oxide sintered compact. The periodically stacked LaO/ScO layers were deposited on the Si substrate using shutter during the evaporation shown in Figure 4.1 (a). Figure 4.1 (b) represents a schematic view of the complex film structure composed of LaO and ScO. The composition ratio of LaO to ScO can be controlled due to changing the physical thickness [4.2]. Two kinds of films with different composition ratio of LaO to ScO were prepared. The Post Metallization Annealing (PMA) was performed at 300^{o}C, 500^{o}C, and 700^{o}C in N_2 ambient for 5min after the gate electrode formation.

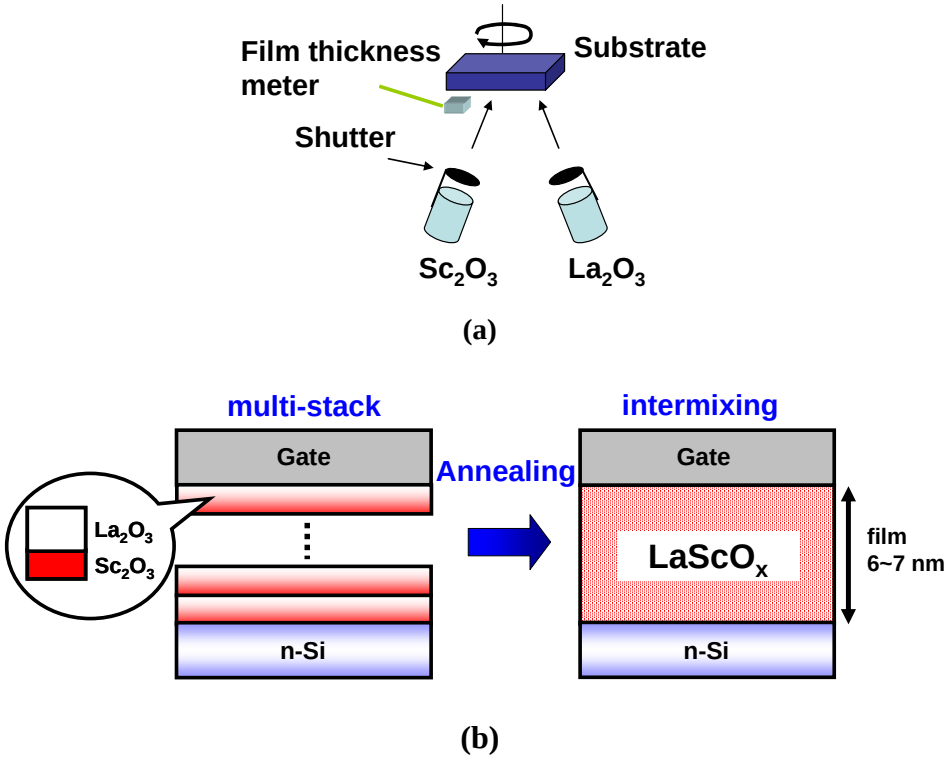

Fig. 4.1 *Sample fabrication method* ***(a)*** *deposition system* ***(b)*** *schematic view of high-k film*

4.3 C-V Characteristics of La-Sc Oxides Complex Gate MOS Capacitors

Firstly, the C-V characteristics of La-Sc oxides complex gate MOS capacitors were investigated. Prepared samples are Sc/(La+Sc) = 33% and 67%. Figure 4.2 shows the C-V characteristics of the La-Sc oxides complex gate MOS capacitors with (a) Sc/(La+Sc) = 33% and (b) Sc/(La+Sc) = 67% as a function of annealing temperature. Several C-V curves show the C-V hysteresis. The direction of all the C-V hysteresis was in the clockwise. Using the n-type Si substrate, these results suggest the carriers are injected from the substrate into the gate oxide. Large bumps, which indicate the large interfacial state density [4.3], were observed in the case of Sc/(La+Sc) = 33% sample. On the other hand, the C-V curves indicating the lower interfacial state density as well as small C-V hysteresis were obtained for the Sc/(La+Sc) = 67% case. Considering the large bump reported for the La_2O_3/Si capacitors [4.4], the incorporation of Sc into La_2O_3 can play a role to suppress the interfacial state density. The Sc_2O_3/Si capacitors with low annealing temperature showed large hysteresis of 0.5V as shown in Figure 3.1, therefore small amount of La incorporation to Sc_2O_3 can reduce the charge trapping. However, the PMA at higher temperature leads to lower capacitance value. The behavior of changing the capacitance value is similar to Sc_2O_3/Si capacitors as shown in Figure 3.1. Flatband voltage (V_{FB}) of the as PMA300^{o}C capacitors are summarized in Figure 4.3. Higher LaO concentration leads to negative flatband voltage shift, which is in good agreement with reported flatband voltage shift reported in [4.5], and it would be suitable for band edge threshold voltage (V_{th}) control.

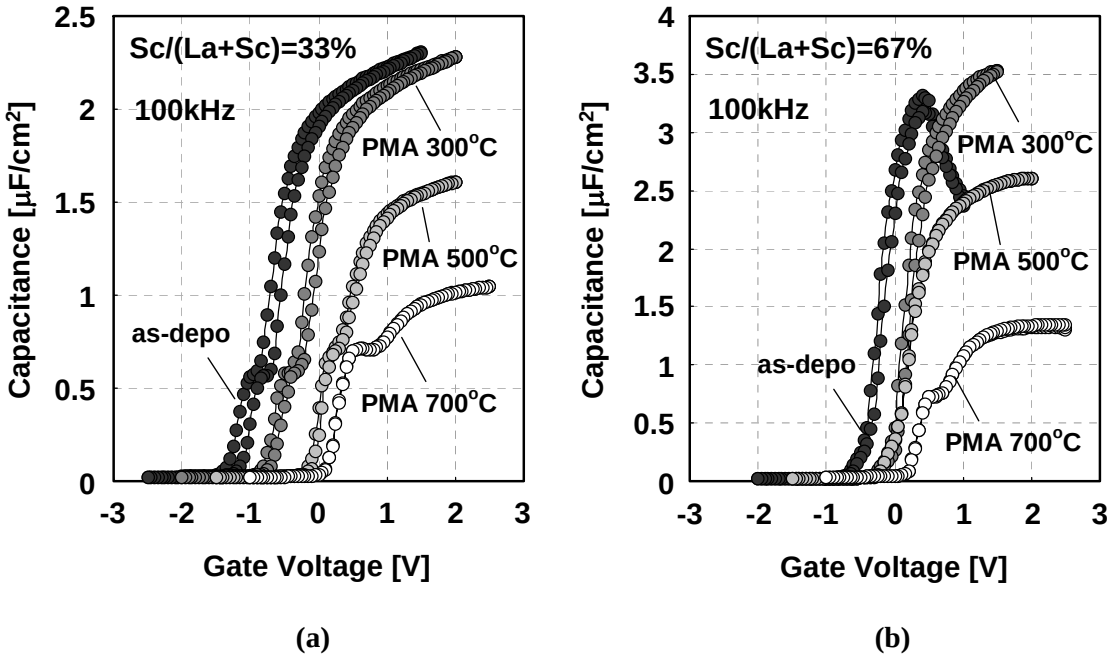

Fig. 4.2 *High-frequency C-V characteristics*
(a) *Sc/(La+Sc)=33% capacitors and* ***(b)*** *Sc/(La+Sc)=67% capacitors*

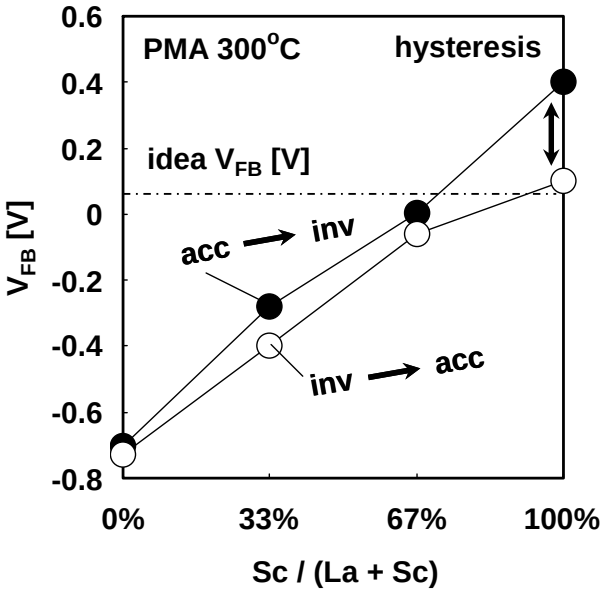

Fig. 4.3 *V_{FB} Shift as a function of Sc concentration observed from C-V curves exhibiting hysteresis*

However, excessively negative V_{FB} is not desirable for pMOSFETs as the V_{th} would be high. On the other hand, the Sc_2O_3 film induces positive V_{FB} shift even taking into account. Therefore, large negative V_{FB} shift induced by La_2O_3 can be controlled by incorporation of the ScO. Considering the ideal V_{FB} of 0.06V obtained on the $W/SiO_2/Si$, Sc/(La+Sc) = 67% concentration seems to be optimum to cancel the effect of La.

Figure 4.4 represents the V_{FB} with different composition ratio as a function of annealing temperature. The results of Sc_2O_3/Si and La_2O_3/Si capacitors are used as reference. It can be confirmed that the V_{FB} values are shifted between the Sc_2O_3/Si and La_2O_3/Si single-layer capacitors. In addition, the amount of V_{FB} shift increases with concentration of LaO.

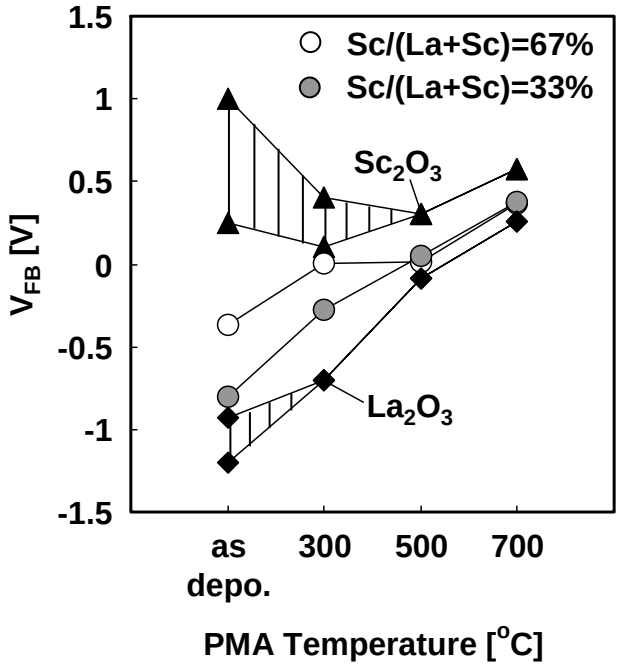

Fig. 4.4 *V_{FB} Shift as a function of annealing temperature*

Figure 4.5 shows the EOT change along PMA temperature. The behavior of EOT change of Sc/(La+Sc) = 33% sample is similar to that of Sc/(La+Sc) = 67% sample. On the other hand, complex films are suppressed the EOT increasing with higher annealing temperature even low Sc concentration compared to La_2O_3/Si single-layer capacitors. It is considered that incorporation of Sc into La suppressed the interfacial layer formation as described chapter 3. Thus, it is conceivable that incorporation of Sc into La is one of effective methods to control the EOT increase.

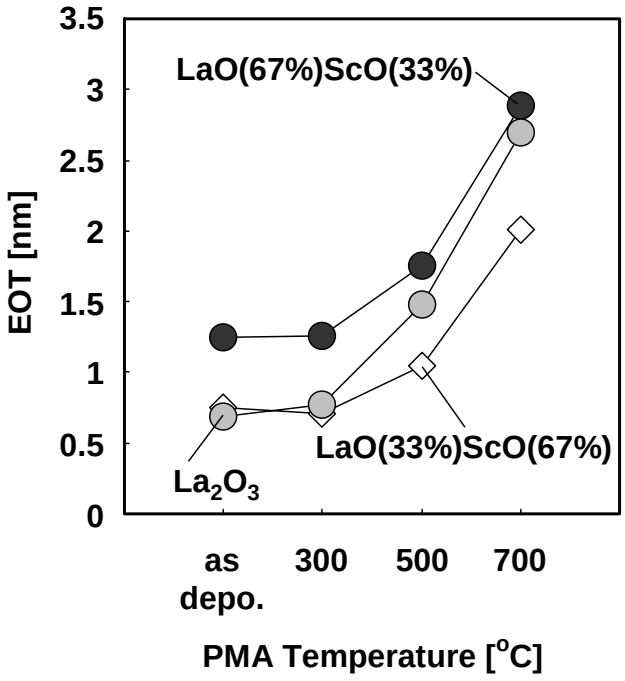

Fig. 4.5 *EOT change as a function of annealing temperature*

4.4 Model of V_{FB} Shift

In the previous section, it is clarified that changing the composition ration of La to Sc can tune the flatband voltage (V_{FB}). It was reported that large negative V_{FB} shift of La_2O_3 is due to positively charged oxygen vacancies [4.6]. The Si band bending is most influenced of charges located at the oxide/Si interface. Considering the large flatband voltage shift due to incorporation of Sc into La as shown in Figure 4.3, it is considered that positive charges at the high-k/Si interface were disappeared associated with ScO or negative charges were generated due to ScO incorporation as shown in Figure 4.6 (a).

On the other hand, in the case of $HfLaO_x$, it was reported that the origin of flatband voltage shift is an existence of the dipole at the high-k/SiO_2 interface [4.7, 4.8]. Figure 4.6 (b) represents the flatband voltage due to dipole associated with electronegativity difference [4.9]. The flatband voltage was determined the amount of atoms at the high-k/Si interface. The flatband voltage can be tuned by changing the number of bonds at the interface. It assumes that flatband voltage shift between La_2O_3 and Sc/(La+Sc) = 67% is due to fixed charges at Si interface. The difference fixed charges becomes more than $10^{13}cm^{-2}$ orders by ref [4.7], which seems to be too large in reality. Thus, a dipole is presented as a main origin of flatband voltage shift.

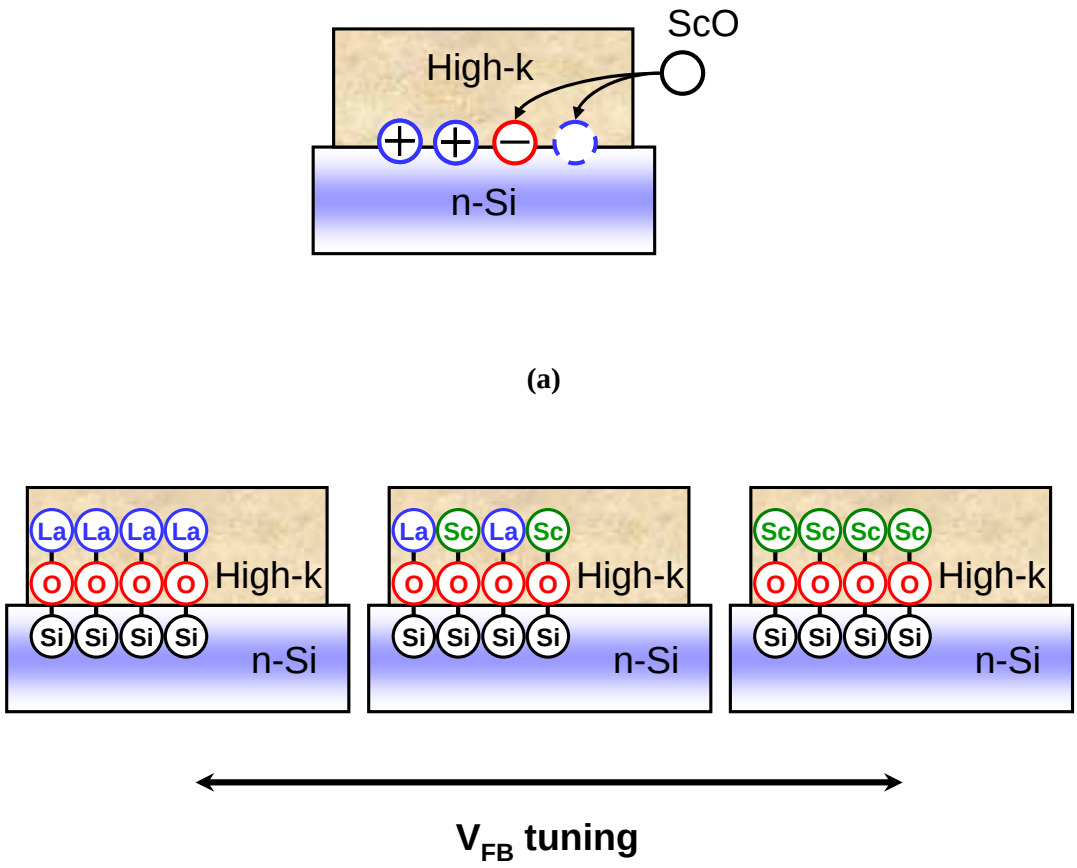

Fig. 4.6 *Flatband voltage shift model*

(a) *The interface located fixed charges model*

(b) *The interface dipole model*

4.5 Interface State Density

As shown in Figure 4.2, the incorporation of Sc into La_2O_3 can play a role to suppress the interfacial state density. In this section, accurate investigations of the interface state density by conductance method are described. Prepared samples are precisely same, Sc/(La+Sc) = 33% and 67%, making thicker compared to the samples which investigate the C-V characteristics. Because if the leakage current is high due to thin films, it is difficult to accurately extract the conductance value associated with interface state density. The Post Metallization Annealing (PMA) was performed at 300^{o}C and 500^{o}C in N_2 ambient for 5min after the deposition of complex films and gate electrode formation.

Figure 4.7 (a), (b) and (c) represent the frequency dispersion of C-V curves with Sc/(La+Sc) = 33% at PMA300^{o}C, Sc/(La+Sc) = 33% at PMA500^{o}C and Sc/(La+Sc) = 67% at PMA500^{o}C, respectively. As-deposited and Sc/(La+Sc) = 67% at PMA300^{o}C samples show a large C-V hysteresis (not shown). In the case of low frequency, carriers can react to its ac voltage and the bumps in C-V curves, which indicate high interface state density, were observed. On the other hand, the case of high frequency, carriers can react to its ac signal and bumps become small. It indicates that the large frequency dispersion means high interface state density. Figure 4.7 (a) and (b) show large frequency dispersion. However, these two C-V characteristics have very different shapes, which indicate that the energy distribution of interface states is differing [4.3]. It is considered that interface properties were varied due to high temperature annealing. Compared to these two C-V curves, few frequency dispersion was observed from Sc/(La+Sc) = 67% at PMA500^{o}C sample as shown in Figure 4.7 (c).

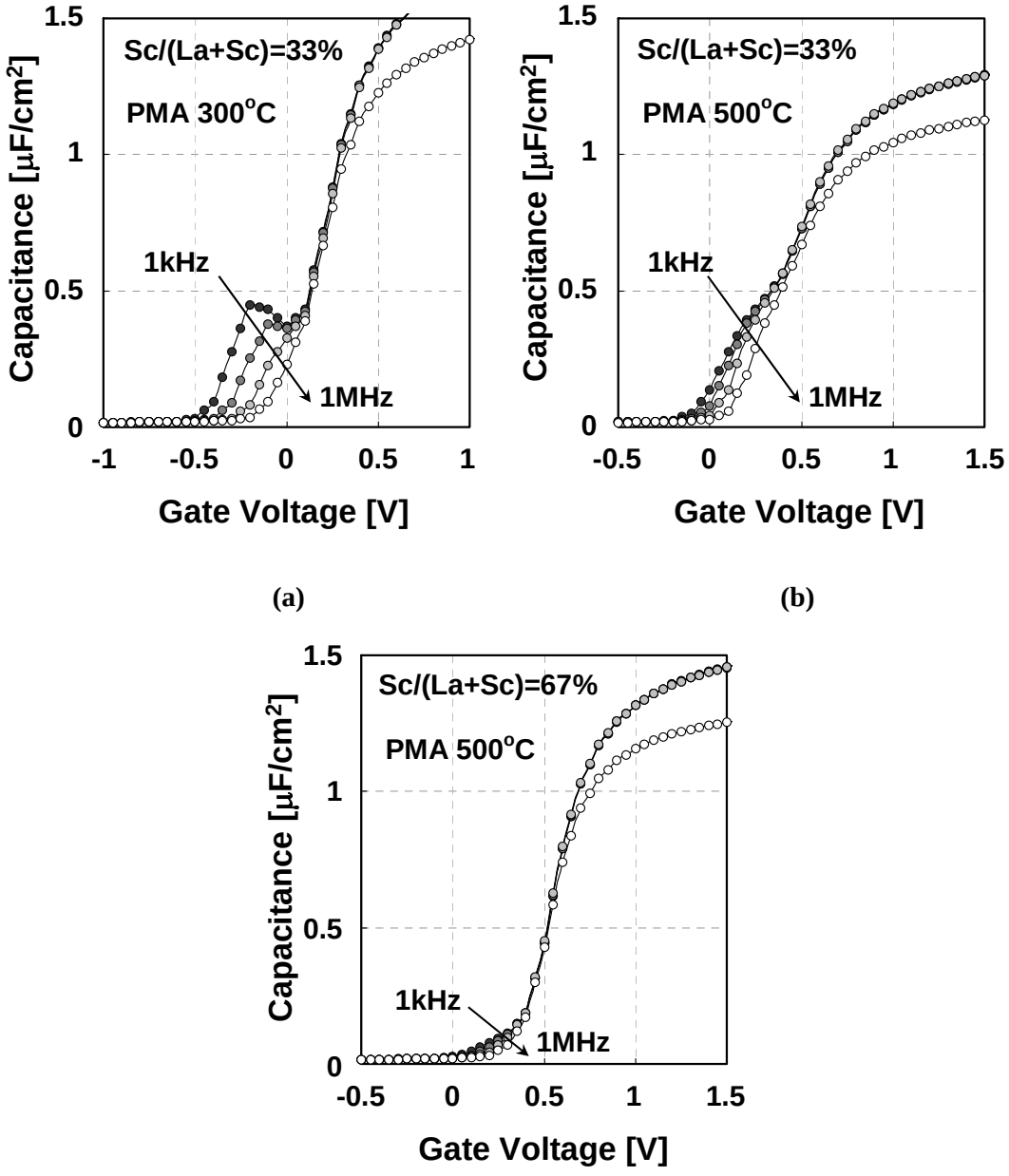

Fig. 4.7 *Frequency dispersion of C-V curves*

(a) *Sc/(La+Sc) = 33% at PMA300°C*

(b) *Sc/(La+Sc) = 33% at PMA500°C*

(c) *Sc/(La+Sc) = 67% at PMA500°C*

In other words, it is suggesting that Sc/(La+Sc) = 67% at PMA500^{o}C sample has good interface properties.

Subsequently, the interface state density, D_{it}, was estimated by conductance method. Figure 4.8 shows the equivalent circuit of MOS capacitor which is used to extract the interface state density. C_{ox} is the gate oxide capacitance, C_p is the interface-trap capacitance, G_p is the conductance. Figure 4.9 shows the interface state density distribution as a function of the energy. This result corresponds to the frequency dispersion of C-V curves as shown in Figure 4.7. Sc/(La+Sc) = 67% at PMA500^{o}C sample which was observed few frequency dispersion demonstrates the low interface state density compared to those of another two samples. Sc/(La+Sc) = 33% at PMA300^{o}C and Sc/(La+Sc) = 33% at PMA500^{o}C show the different behavior along the energy. This result represents the energy distribution of interface states is differing which corresponds to the frequency dispersion of C-V curves.

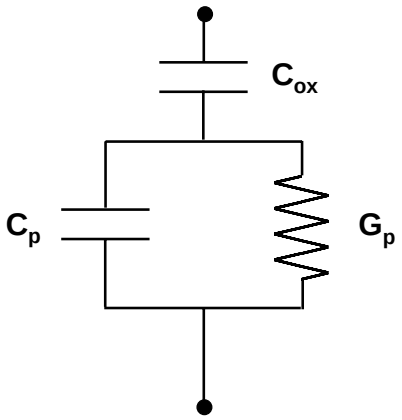

Fig. 4.8 *Equivalent circuit of a MOS capacitor*

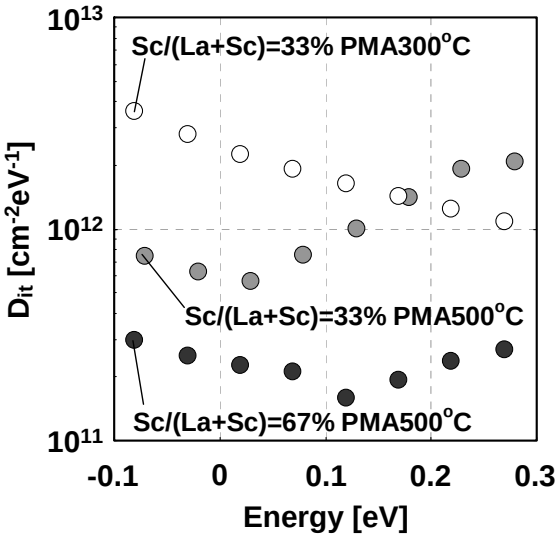

Fig. 4.9 *Interface state density distribution as a function of the energy*

4.6 Summary

In this section, the electrical characteristics of La-Sc oxides complex gate dielectrics with various film compositions were mainly described. Incorporation of Sc into La can suppress the EOT increase after performing high annealing temperature. Flatband voltage can tune by changing the composition ratio of La to Sc.

It assumes that flatband voltage shift is due to fixed charges at Si interface. The difference fixed charges becomes more than $10^{20}cm^{-2}$ orders, which seems to be too large in reality. Thus, the origin of this flatband voltage shift is mainly presented a dipole at Si interface.

From the frequency dispersion of C-V curves and interface state density estimated by conductance method, incorporation of Sc into La can suppress the interface state density, especially high Sc concentration. It is considered that Sc_2O_3 does not form the interfacial layer after PMA500^{o}C as mentioned in chapter 3.

Considering the idea flatband voltage and interface properties, Sc/(La+Sc) = 67% is the optimum value in this study.

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Chapter 5 Characterization of La-Sc Oxides Complex Gate nMOSFET

5.1 Introduction

In the chapter 3 and chapter 4, the basic properties of Sc_2O_3 single layer and the electrical characteristics of La-Sc oxide complex gate dielectric were described. In this section, electrical characteristics of La-Sc oxide complex gate nMOSFET are investigated. There are few reports of MOSFET characteristics with La-Sc oxide complex. The prepared samples are Sc/(La+Sc) = 33%, 50% and 67%. Sample fabrication method is same as MOS capacitors (5-6nm). Forming Gas Annealing was performed at 500^{o}C for 30min. Firstly, I_d-V_g characteristics and subthreshold characteristics are described. Subsequently, the interface state density is investigated using charge pumping method. Finally, the effective mobility with La-Sc oxide complex is examined and discusses the origin of the mobility degradation.

5.2 I_d-V_g and Subthreshold characteristics

Figure 5.1 shows the Id-Vg characteristics of La-Sc oxides complex gate nMOSFET with various film compositions. Figure 5.1 (a) is a linear scale and (b) is a logarithmic scale, respectively.

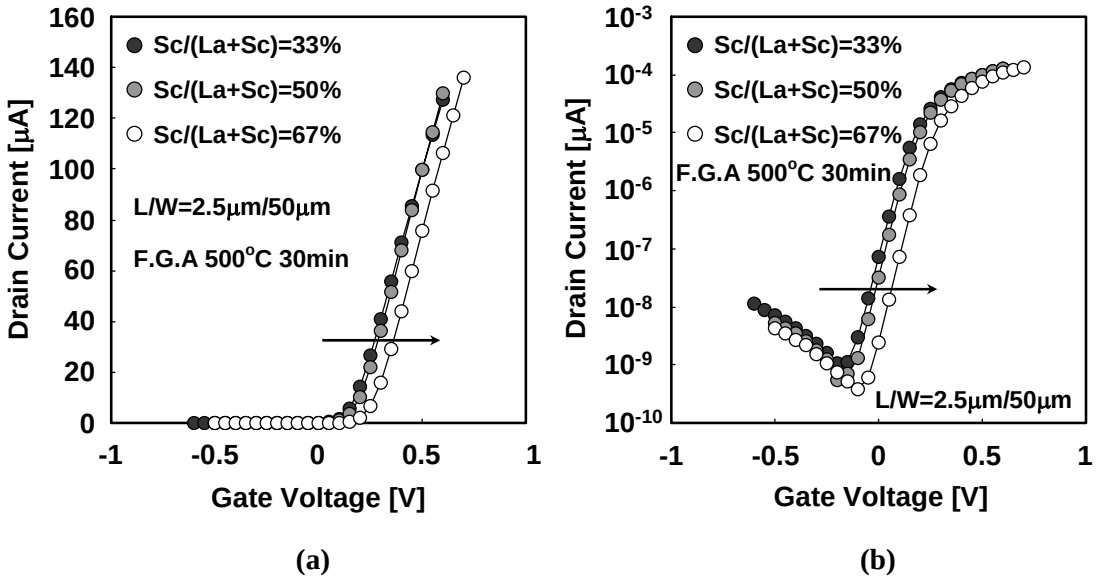

Fig. 5.1 *I_d-V_g characteristics of La-Sc oxides complex nMOSFET changing composition ratio* ***(a)*** *linear scale and* ***(b)*** *logarithmic scale*

As mentioned in chapter 4, changing the composition ratio can tune the flatband voltage at low annealing temperature, which means threschold voltage V_{th} can tune in the case of MOSFET. From Figure 5.1, the positive V_{th} shifts are observed with increasing Sc concentration. This result is completely identical in the case of MOS capacitors. An amount of V_{th} shift is small compared to Figure 4.3. This is due to high temperature

annealing. This result is also identical at the results of MOS capacitors. Figure 5.2 represents the amount of subthreshold slope which are estimated by the slope of Figure 5.1 (b) [5.1].

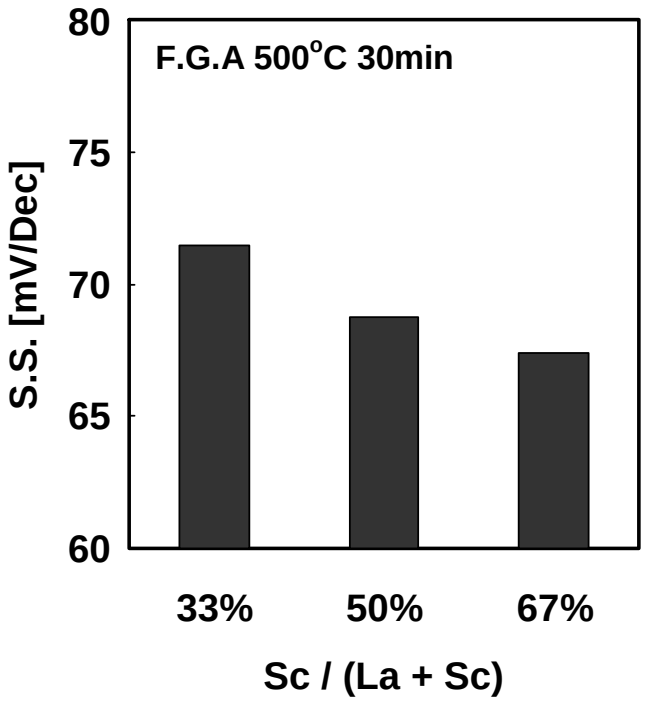

Fig. 5.2 *Subthreshold slope of La-Sc oxides complex nMOSFET changing composition ratio*

The subthreshold slope is typically 70-100mV/Dec [5.1]. The subthreshold slope may be more degraded if the interface state density is high. Figure 5.2 means good interface properties. The subthreshold slope is witten as Eq. (2.13) in the chapter 2. It is considered that the difference of subthreshold slope is due to difference of physical thickness after forming gas annealing at 500^{o}C.

5.3 Interface State Density

As described previously, good subthreshold slopes are obtained from all the samples. Subsequently, the interface state density is estimated using charge pumping method. Figure 5.3 shows the charge pumping current. The interface state density is calculated by Eq. (2.18). There are no appreciable differences of interface state density in three samples. However, these values are more higher compared to HfSiON gate MOSFET [5.2]. It is considered that inversion carriers may be scattered by interface state density and degrade effective mobility.

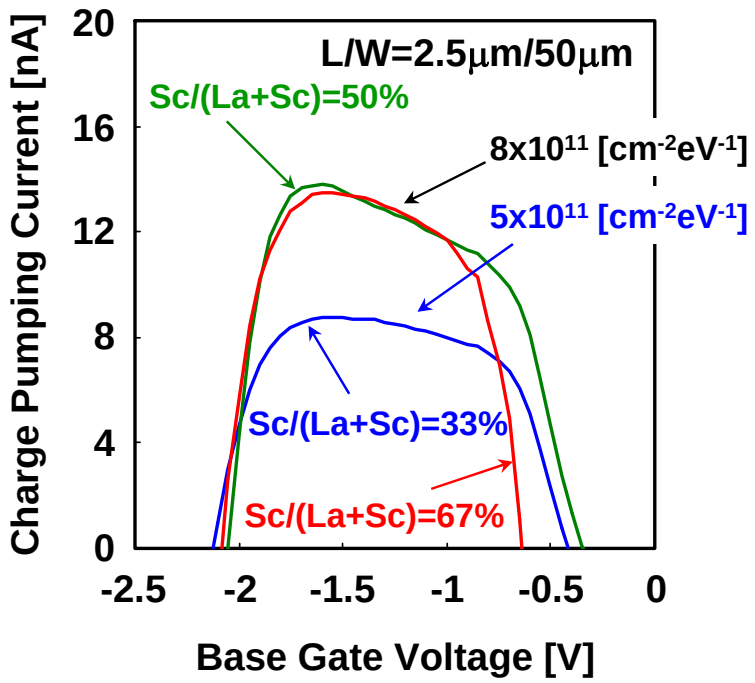

Fig. 5.3 *Charge pumping current and interface state density, frequency is 83kHz*

5.4 Effective Mobility

By charge pumping method, there are no appreciable differences of interface state density in three samples. In this section, the effective mobility of La-Sc oxides complex MOSFET with various film compositions are experimentally evaluated. Mobility is measured by Split C-V method at 1MHz. The parasitic capacitances are subtracted by measuring different gate length (L_g) samples [5.3].

Figure 5.4 shows the gate-channel capacitance (C_{gc}) measured by Split C-V technique. As using the tungsten (W) metal gate, decreasing gate capacitance due to depletion of poly-Si gate do not occur. Therefore, the EOT can be extracted using NCSU CVC program. The EOT values of Sc/(La+Sc) = 50% and 67% samples are almost identical, EOT = 1.4nm. On the other hand, capacitance value of Sc/(La+Sc) = 33% samples are drastically decreased compared to Sc/(La+Sc) = 50% and 67% samples. The difference of EOT is about 1nm. This result indicates decreasing dielectric constant. It has reported that dielectric constant of Hf-silicate is more low compared to HfO_2 [5.4]. Thus, decreasing capacitance value indicates changing La_2O_3 to La-silicate according to react with Si substrate. As Sc_2O_3 is seems not to be react with Si substrate described in chapter 3, the amount of decreasing dielectric constant is low.

Figure 5.5 represents the effective mobility of La-Sc oxides complex MOSFETs. Sc/(La+Sc) = 33% sample shows most high mobility in three samples. This results corresponds to the interface state density by charge pumping measurement.

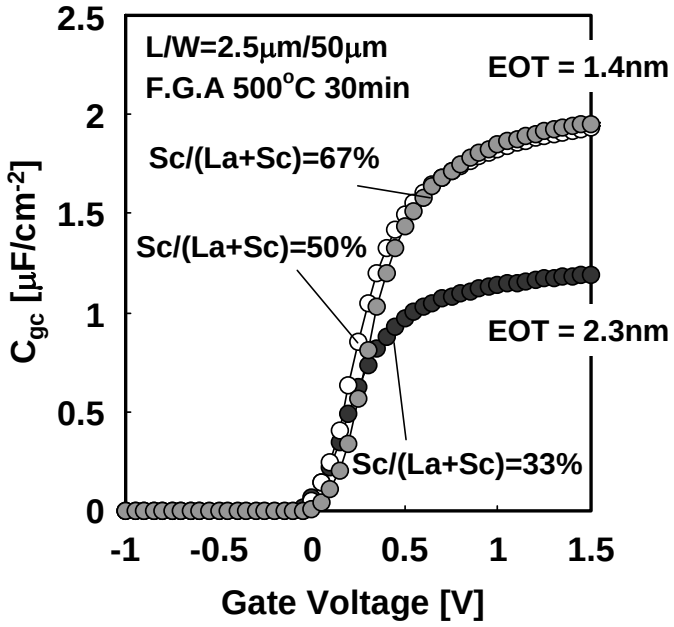

Fig. 5.4 *Gate-channel capacitances measured by Split C-V method*

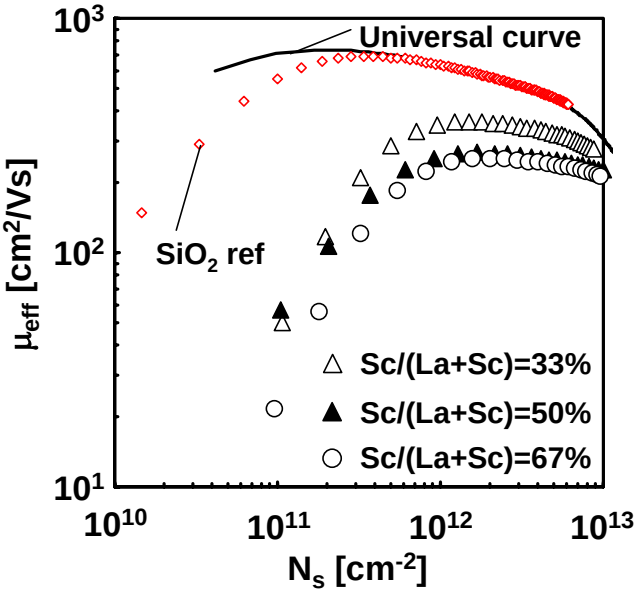

Fig. 5.5 *Effective mobility of La-Sc oxides complex gate MOSFETs*

5.5 Discussion

It has reported that drain current of HfSiON gate MOSFET is degraded with different Hf/Hf+Si ratio. The higher Hf concentration is more degraded than low Hf concentration [5.5]. In addition, a lot of charge trap sites are existence in the HfSiON with higher Hf concentration. It is considered that degradation of mobility for low La concentration is same as HfSiON gate MOSFET. According to changing La_2O_3 to La-silicate, a lot of trap sites may be suppressed and increasing mobility. On the other hand, charge trap sites remain in gate oxides for low La concentration samples and leading mobility reduction.

5.6 Summary

In this chapter, the electrical characteristics of La-Sc oxides complex gate MOSFET. Good subthreshold slope were demonstrated. However, it is necessary to reduce the interface state density. Higher La concentration MOSFET presents most high mobility in three samples. This is because trap sites in the gate oxide are reduced by changing La_2O_3 to La-silicate. It is needed for improving mobility not to decrease the dielectric constant.

5.7 References

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Chapter 6 Characterization of HfO_2/La_2O_3 Stacked Gate nMOSFET

6.1 Introduction

As mentioned in chapter 1, it has reported that combination of HfO_2 and La_2O_3 can increase crystallizing temperature or suppress the oxygen vacancies from first principle calculation. One of major problem of the Hf-based gate oxide is needed for the SiO_2-based interfacial layer. Hence, the scaling limit is determined by the interfacial layer thickness. In this chapter, the electrical characteristics of HfO_2 and La_2O_3 stacked MOSFET replacement with SiO_2-based interfacial layer are examined in order to continue the scaling. In addition, effective mobility is experimentally investigated in the HfO_2 and La_2O_3 stacked MOSFET.

Figure 6.1 shows the prepared stacked samples with various film thicknesses. Forming Gas Annealing was performed at 500^oC for 30min. All the samples are firstly deposited La_2O_3 followed by deposited HfO_2. As La_2O_3 films were deposited simultaneously, the physical thickness of La_2O_3 films is same and only differing HfO_2

thicknesses.

Firstly, I_d-V_g characteristics and subthreshold characteristics are described. Subsequently, the interface state density is investigated using charge pumping method. Finally, the effective mobility is examined.

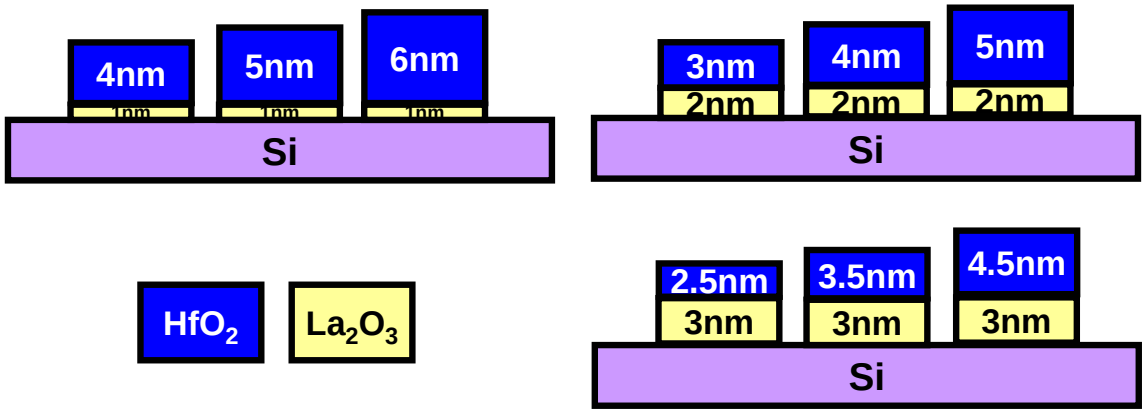
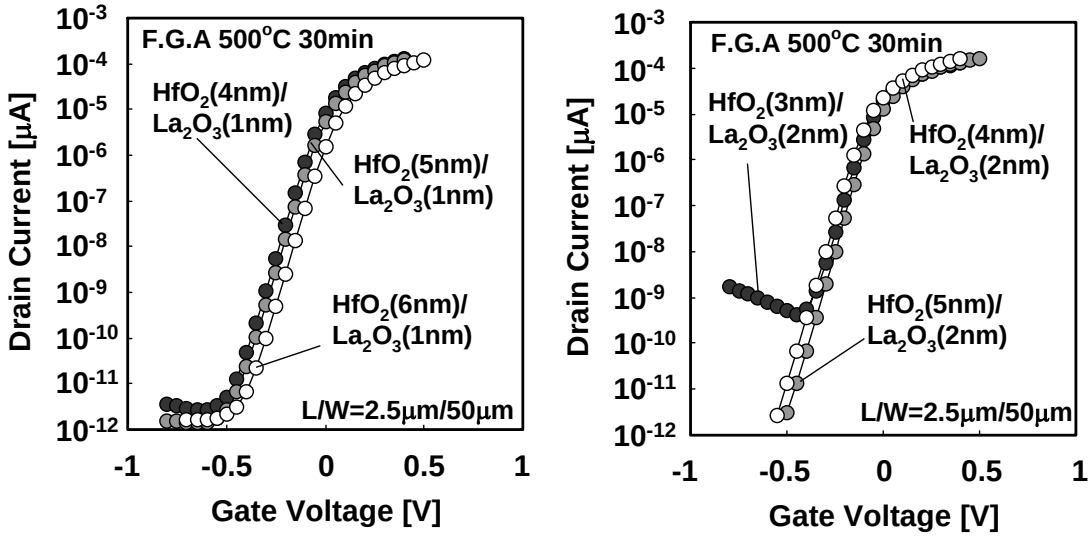


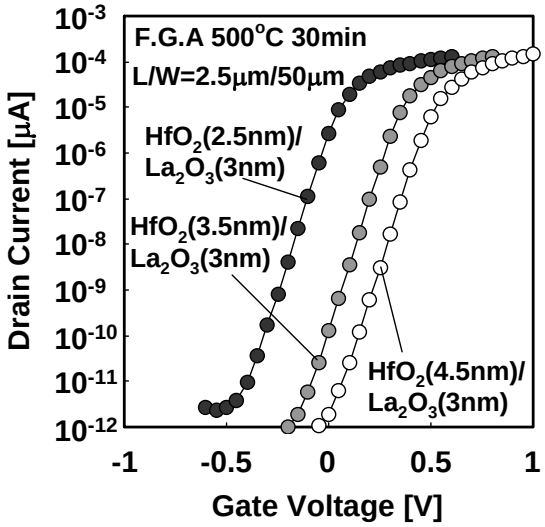
Fig. 6.1 *Prepared sample structures of HfO_2 and La_2O_3 stacked gate oxides*

6.2 I_d-V_g and Subthreshold characteristics

Figure 6.2 shows the I_d-V_g characteristics of HfO_2 and La_2O_3 stacked MOSFET. Figure 6.2 (a) is 1nm-La_2O_3 samples, (b) is 2nm-La_2O_3 samples, and (c) is 3nm-La_2O_3 samples, respectively. Negative threshold voltage was obtained from all the samples. It is because La_2O_3 was firstly deposited on the Si substrate. As described in chapter 4, flatband voltage shift (namely threshold voltage shift) is determined by amount of atoms at the Si interface. The subthreshold slope extracted by the slope of Figure 6.2 is about 70mV/dec at all samples. It can be easy to understand that all the samples were deposited La_2O_3 followed by HfO_2. Therefore, all the samples of interface properties are same and similar to La_2O_3 single layer. However, in the case of thin La_2O_3 samples, it is considered that mixture of HfO_2 and La_2O_3 at Si interface may be occurred.



(a) **(b)**



(c)

Fig. 6.2 *I_d-V_g characteristics of HfO_2 and La_2O_3 stacked gate oxides*

(a) *1nm-La_2O_3 samples*

(b) *2nm-La_2O_3 samples*

(c) *3nm-La_2O_3 samples*

6.3 Interface State Density

As described previously, the subthreshold slopes of all the samples are almost identical, about 70mV/Dec. However, it is necessary to investigate the interface state density because the interface state density is one of the physical origins responsible for mobility degradation. The interface state density was extracted by using the charge pumping method. Figure 6.3 represents the interface state density estimated by charge pumping current. The interface state density of all devices was about 2~5x10^{11} $cm^{-2}eV^{-1}$, while, increasing the interface state density with decreasing EOT.

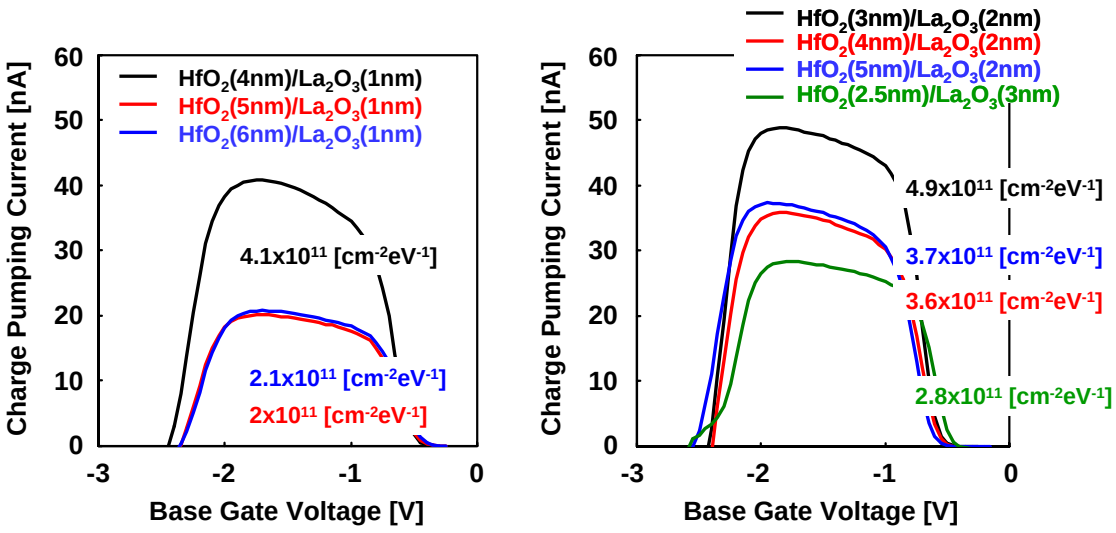


Fig. 6.3 *Charge pumping current and interface state density, frequency is 500kHz*

6.4 Effective Mobility

In this section, the effective mobility of HfO_2 and La_2O_3 stacked MOSFET are investigate. Figure 6.4 shows the effective mobility of HfO_2 and La_2O_3 stacked MOSFETs as a function of EOT. As physical thickness of HfO_2 and La_2O_3 films are differences, the EOT which extracted by gate-channel capacitances using Split C-V method is almost identical as same color plots except for green plots. The peak mobility decreases with decreasing EOT and shows only EOT dependence in spite of each physical thickness. The mobility lowering is observed from High-k/SiO_2 stacked with decreasing SiO_2 interfacial layer thickness. These results are completely distinct from mobility with High-k/SiO_2 stacked MOSFETs [6.1].

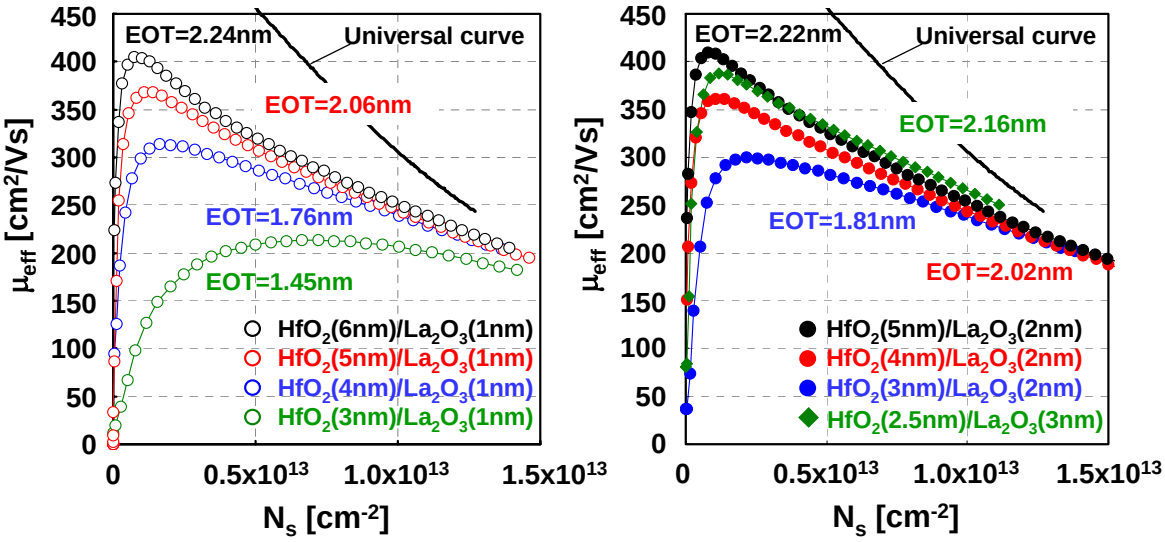


Fig. 6.4 *Effective mobility of staked MOSFETs as a function of EOT*

6.5 Discussion

In this section, the scattering component responsible for the mobility lowering is extracted by Matthiessen's rule. Firstly, Coulomb scattering associated with substrate impurity are subtracted using SiO_2 MOSFET which is same Si substrate as Figure 6.4. Figure 6.5 shows the measured effective mobility of SiO_2 MOSFET. The universal mobility is also plotted as a solid line [6.2].

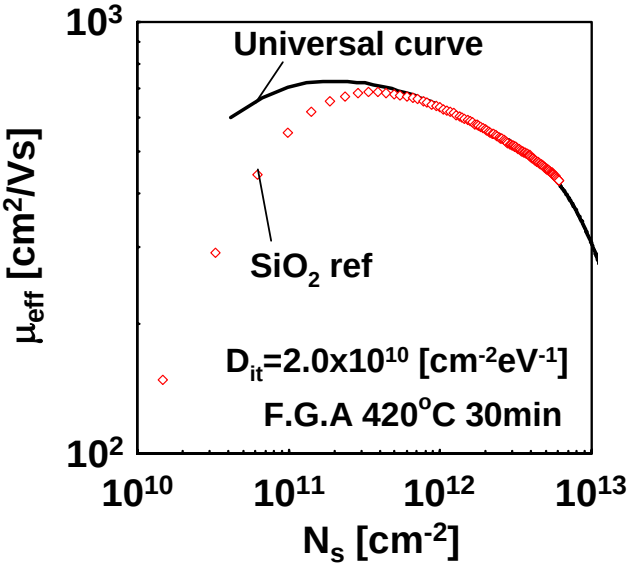


Fig. 6.5 *Effective mobility of SiO_2 MOSFET as a reference*

The mobility component due to substrate impurity scattering was subtracted from the experimental mobility. Figure 6.6 shows the estimated values of $\Delta\mu$ for HfO_2/La_2O_3 stacked MOSFETs as a function of surface carrier density (N_s). It is reported that mobility limited by interface state density shows the $N_s^{+0.5}$ dependence [6.3]. On the other hand, scattering centers located at the remote positions from the channel is depends on $N_s^{+0.6}$ [6.4]. Figure 6.6 represents the $N_s^{+0.6}$ dependence which indicates the

mobility may be reduced by additional scattering component except for interface state density. Moreover, Figure 6.6 means that the mobility component associated with thinner EOT becomes influential. This result indicates that the additional scattering component is existed in the dielectric.

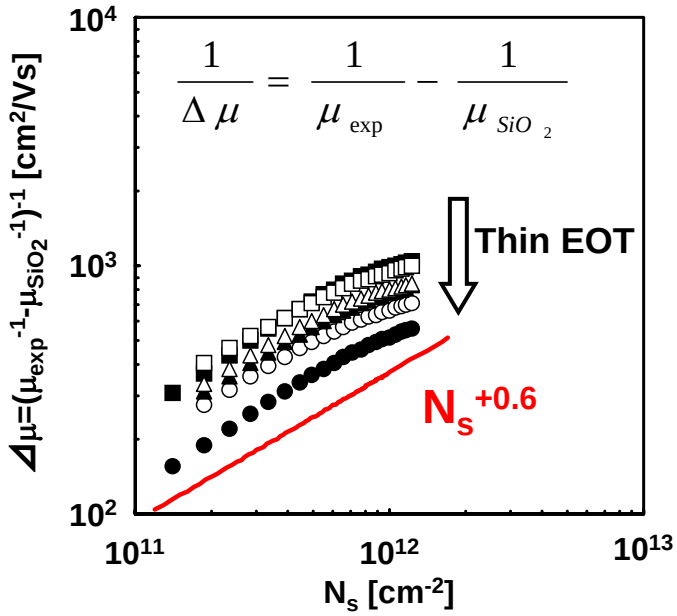


Fig. 6.6 *Mobility component determined by Matthiessen's rule as a function of* N_s

As shown in Figure 6.3 and 6.4, the peak mobility is degraded and the interface state density is increased as EOT becomes thinning. Thus, the impact of mobility lowering associated with interface state density is experimentally evaluated. The interface charges are intentionally generated by applying constant negative gate bias (V_g=-2V) for 10^3sec. Figure 6.7 shows the charge pumping current before and after electrical stress. After applying electrical stress, the charge pumping current increased to the same extent $4.1x10^{11}$ $cm^{-2}eV^{-1}$. Figure 6.8 shows the I_d-V_g characteristics of before and after electrical stress. Open circle means sweep direction is forward (- to +) and solid circle

means sweep direction is reverse (+ to -). The threshold voltage shift between forward and reverse sweep is negligible small. It indicates that the amount of bulk trap states is small.

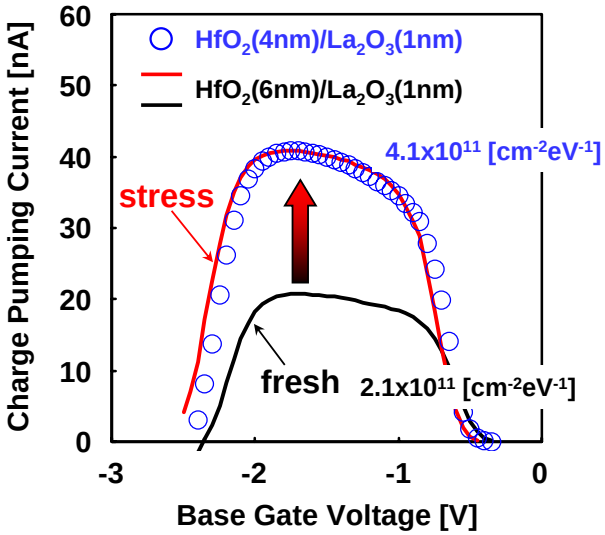


Fig. 6.7 *Increasing charge pumping current after electrical stress*

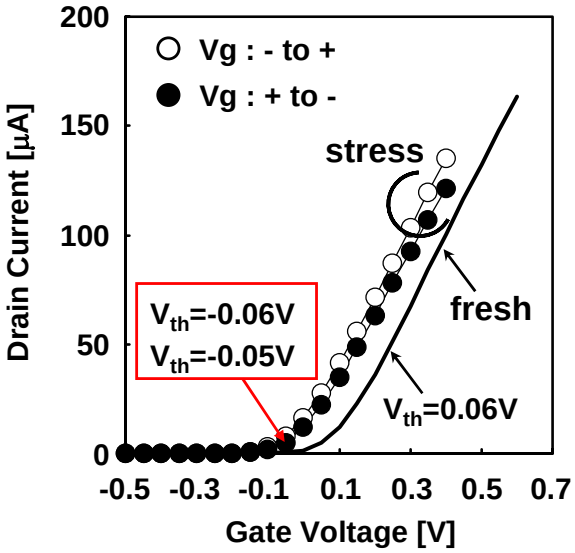


Fig. 6.8 *I_d-V_g characteristics before and after electrical stress*

The threshold voltage shift was observed before and after electrical stress, which indicates the interface charges are generated by electrical stress.

As the threshold voltage was shifted due to electrical stress, it can not be extracted electron mobility from Split C-V and I-V measurement. Because parasitic capacitances are subtracted using different L_g devices, it is difficult to extract accurate gate-channel capacitance. Thus, the amount of mobility lowering associated with interface charges is estimated from transconductance (g_m). Although the interface state density is increased by applying electrical stress, effective gate-channel capacitance is unchanged. Figure 6.9 shows the transconductance before and after electrical stress. Reduction of transconductance was confirmed after electrical stress. The estimated mobility value of $\Delta D_{it}=2x10^{11}$ $cm^{-2}eV^{-1}$ is about $3700cm^2/Vs$ at $N_s=8x10^{11}cm^2$ using Matthiessen's rule, $1/\mu_{stress}-1/\mu_{fresh}$. The difference value of mobility between HfO_2(6nm)/La_2O_3(1nm) and HfO_2(4nm)/La_2O_3(1nm) at $N_s=8x10^{11}cm^2$ shown in Figure 6.4 is about $1030cm^2/Vs$. The contribution of $\Delta\mu_{it}(\Delta D_{it})$ to the difference value between HfO_2(6nm)/La_2O_3(1nm) and HfO_2(4nm)/La_2O_3(1nm) at $N_s=8x10^{11}cm^2$ is approximately 28%. The mobility lowering at low N_s region is mainly caused by an additional scattering component associated with EOT.

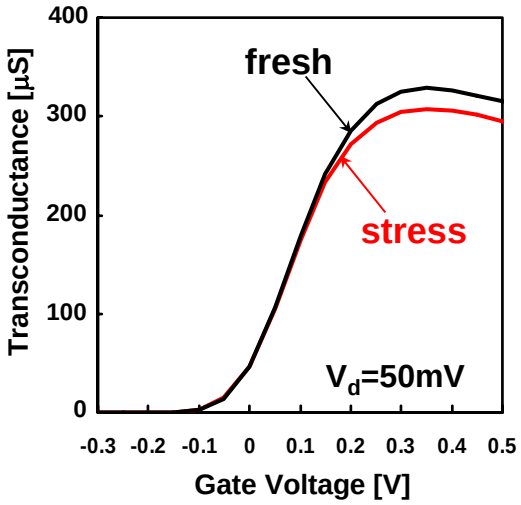


Fig. 6.9 *Degradation of transconductance after electrical stress*

Next, additional scattering component associated with EOT is experimentally extracted by Matthiessen's rule. To identify the origin of the mobility reduction, temperature dependence of electron mobility was measured at 293K and 413K. Figure 6.10 shows electron mobility of HfO_2(6nm)/La_2O_3(1nm) and HfO_2(5nm)/La_2O_3(1nm) devices at 293K and 413K. As shown in Figure 6.3, both HfO_2(6nm)/La_2O_3(1nm) and HfO_2(5nm)/La_2O_3(1nm) devices showed the same interface state density, whereas EOT was distinct. Using these two devices, mobility scattering component associated with EOT are extracted from Matthiessen's rule, $1/\mu_{EOT}=1/\mu_{thin}-1/\mu_{thick}$. Comparing the temperature dependence of μ_{EOT}, the source of the scattering component is determined.

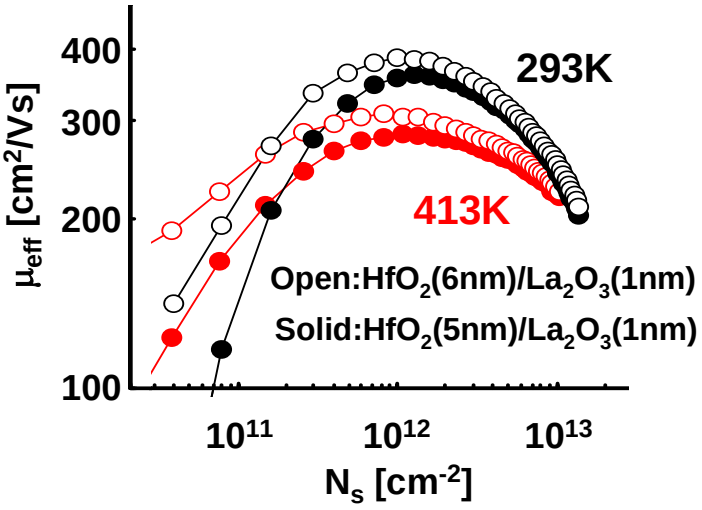


Fig. 6.10 *Temperature dependence of electron mobility*

Figure 6.10 shows Ns dependence of μ_{EOT} at 293K and 413K. μ_{EOT} increases with N_s and also increases with temperature. This is the specific trend for Coulomb scattering limited mobility. Coulomb scattering limited mobility is more effective the higher the inversion carrier density by screening effect and also shows an increasing trend with temperature due to increasing kinetic energy of inversion carrier. This result indicates the main origin of mobility lowering component is remote Coulomb scattering due to scattering centers located in the dielectric.

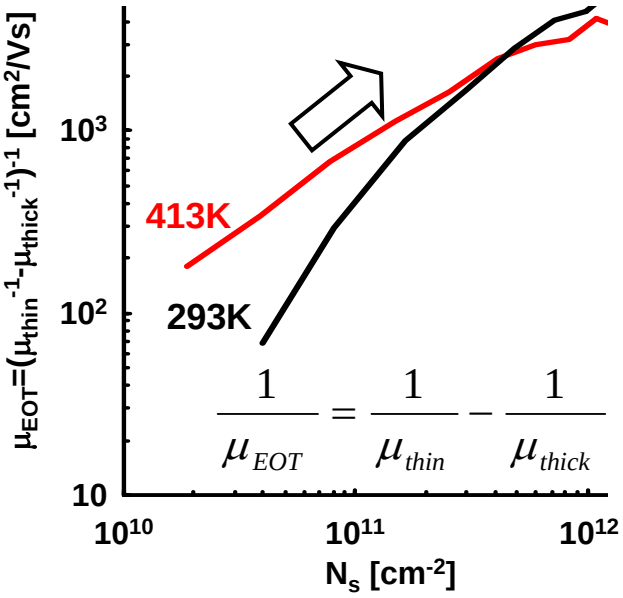


Fig. 6.11 *Temperature dependence of additional mobility component at low N_s region*

As mentioned above, the mobility lowering in low N_s region is mainly due to scattering centers in the dielectric. Although the stack structure of gate insulator is different from each device, the peak mobility is almost identical shown in Figure 6.4. It indicates that the position of scattering centers in the dielectrics is not modulated by stack structure of gate insulator. Whether the position of scattering centers is modulated due to differing stack structure or not, gate leakage characteristics are investigated to clarify the modulation of the scattering centers. Figure 6.12 shows the Arrehenius plots of gate leakage current for each device.

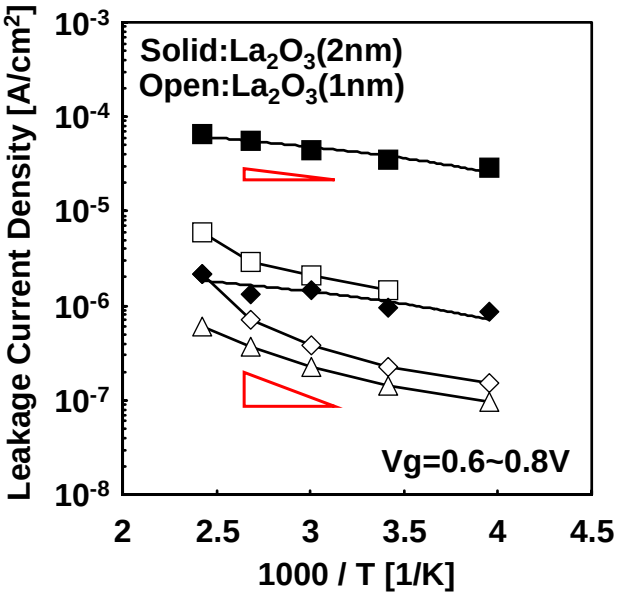


Fig. 6.12 *Arrehenius plots of gate leakage current*

This relatively weak temperature dependence of gate leakage current implies charge-center-mediated carrier transport mechanism. The slope of plots is different compared to La_2O_3 (1nm) and La_2O_3 (2nm). It means differing in trap level or trap

density, whereas the peak mobility is nearly equal. Thus, two cases are considered from this result. One is that the modulation of trap centers is unlikely to have a significant impact on the electron mobility. The other is that there is no relation between the scattering centers and trap centers which observed by Arrehenius plots.

As shown in the previous, the origin of mobility lowering is mainly Coulomb scattering centers in the dielectrics. A model of MOSFET with High-k/SiO_2 stack was previously proposed to explain the mobility reduction in terms of fixed charged or dipoles shown in Figure 6.13 [6.5, 6.6, 6.7].

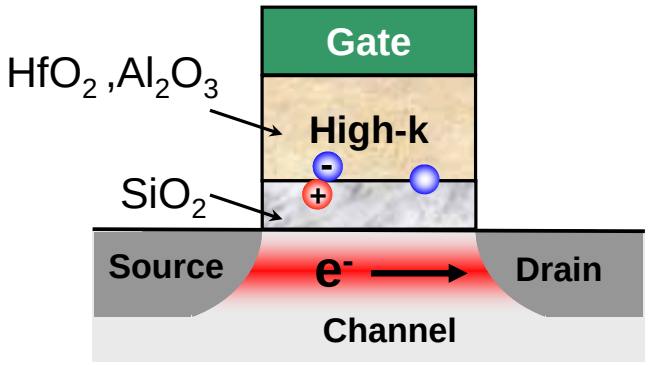


Fig. 6.13 *Model of MOSFET with High-k/SiO_2 stack*

We apply a model of MOSFET with High-k/SiO_2 stack to our experimental results. If we assume that fix charges or dipoles are located at the HfO_2/La_2O_3 interface, mobility lowering associated with a reduced La_2O_3 thickness can be easily accountable because the position of fix charges or dipoles located at the HfO_2/La_2O_3 interface is approaching toward inversion layer. This is in good agreement with experimental date as shown in Figure 6.4. On the other hand, mobility lowering associated with a reduced HfO_2 thickness can not be explained by this model. As EOT is relatively large, it is unlikely

that defects at the Metal/High-k interface reduced the electron mobility [6.4]. Hence, we propose a model of origin for mobility lowering associated with a reduced boss La_2O_3 and HfO_2 thickness. Figure 6.14 shows a feasible model of mobility lowering. Firstly, we regard a stack structure shown in (a) as a single layer with relative permittivity, ε_x shown in (b). The relative permittivity, ε_x is easy able to calculate from EOT (C-V characteristics) and total physical thickness of stack structure. Subsequently, we assume that the scattering centers associated with traps or defects are located in the dielectrics.

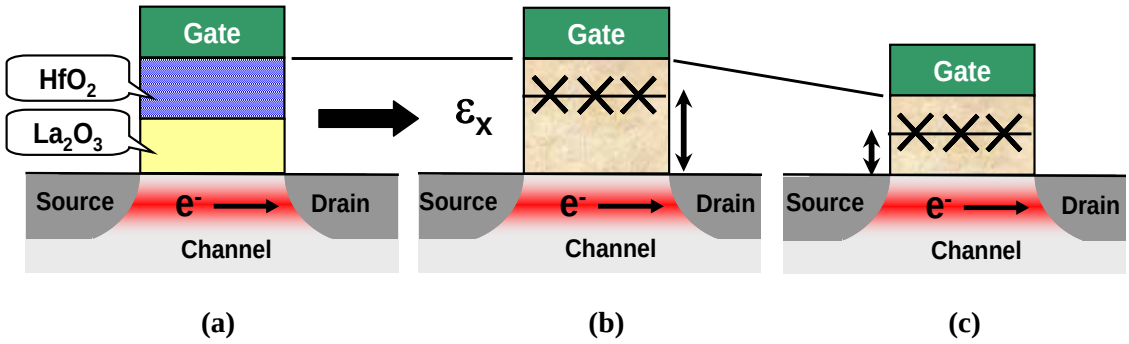


Fig. 6.14 *A feasible model of origins for mobility lowering*

Since we consider a stack structure as a single layer, the scattering centers become reliant on EOT which is varied with physical thickness of La_2O_3 and HfO_2. As a result, the electron mobility at low N_s region is not dependent on physical thickness of La_2O_3 and HfO_2 but EOT shown in (c).

6.6 Summary

In this section, electrical characteristics of HfO_2 and La_2O_3 stacked MOSFET are described. The main origin of mobility lowering at low N_s region is Coulomb scattering centers in the dielectric. Since electron mobility depends on EOT, this can no be explained by remote charge scattering from fix charges or dipoles at the HfO_2/La_2O_3 interface. We proposed a feasible model of origin for mobility lowering and Figure 6.15 shows mobility limiting component in HfO_2/La_2O_3 stack MOSFET.

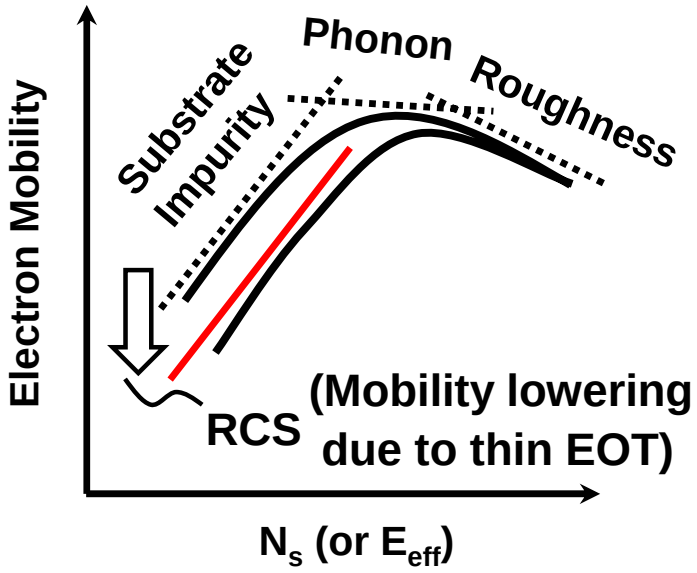


Fig. 6.14 *Schematic illustration of mobility limiting component in HfO_2/La_2O_3 stack MOSFET*

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7 Conclusion and Future works

In this study, to clarify the optimum structure (stack or complex) of high-k gate insulator and the combination of high-k materials for improving the effective mobility are investigated. Moreover, the influence of electron mobility due to various high-k gate stack engineering based on La_2O_3 is examined.

Firstly, Sc_2O_3 is selected as a candidate because which has great affinity with oxygen. In order to clarify the basic properties of Sc_2O_3 gate dielectrics, the electrical characteristics of MOS capacitor with Sc_2O_3 gate dielectrics were investigated. We confirmed that no interfacial layer was formed at PMA 500^{o}C sample.

The electrical characteristics of La-Sc oxides complex gate dielectrics with various film compositions were mainly investigated. We found that the flatband voltage can be shifted by changing the composition ratio. The origin of the flatband voltage shift is mainly presented a dipole at Si interface. Higher La concentration MOSFET in La-Sc oxides shows most high mobility. This is because trap sites in the gate oxide are reduced by changing La_2O_3 to La-silicate. On the other hand, relative permittivity of La-silicate is lower compared to La_2O_3.

The electrical characteristics of HfO_2 and La_2O_3 stacked MOSFET are described. The main origin of mobility lowering is Coulomb scattering centers at the remote position from the channel. As electron mobility shows EOT dependence, this can no be explained by remote charge scattering from fix charges or dipoles at the HfO_2/La_2O_3 interface. Thus, we proposed a model of origin for mobility lowering in the case of HfO_2 and La_2O_3 stacked MOSFET. Since we consider a stack structure as a single layer, the scattering centers become reliant on EOT.

Continuing the scaling, it is necessary that high-k gate oxides are directly deposited on Si substrate to realize ultrathin EOT. Moreover, high electron mobility is required for high drive current. More detailed verification is needed for whether the model of mobility lowering is correct or not. We need to establish methods of controlling scattering centers in the dielectric by gate stack engineering. In addition, we must analyze electron mobility of directly deposited high-k gate MOSFET in sub 1.0nm-EOT region.

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