Master thesis

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A Novel Flat Band Voltage Tuning for Metal/High-k Gate Stack Structure

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Chapter 1
Introduction

1.1 Background of This Study

CMOS technology has been widely used as a main controlling unit everywhere in our life. From cellular phone, digital camera, navigation system for automobile to large scale network servers, CMOS has become one of the essential tools for living. The required speed for signal processing is depended on its application complexity, but, power consumption, at the same time, goes up due to the increase numbers of transistor in CMOS chip.

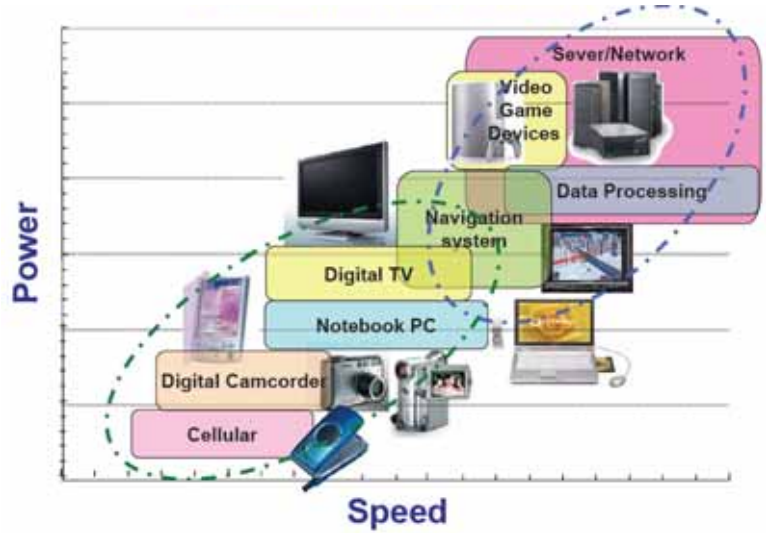


Fig 1.1 Electronic equipment benefiting from CMOS technology

Each specification of INTEL CPU's are shown in figure1.2. Thanks to the "downsizing" of CMOS technology, exponential increase of transistors are mounted in a chip, and the state-of-the-art CMOS chip contains millions or even billions of transistors. The numbers of transistors about 2000 in the old device has now reached to 800 millions. Moreover, clock frequency, which mean processing speed, was also increased 30 thousand times from 1971 to 2007.

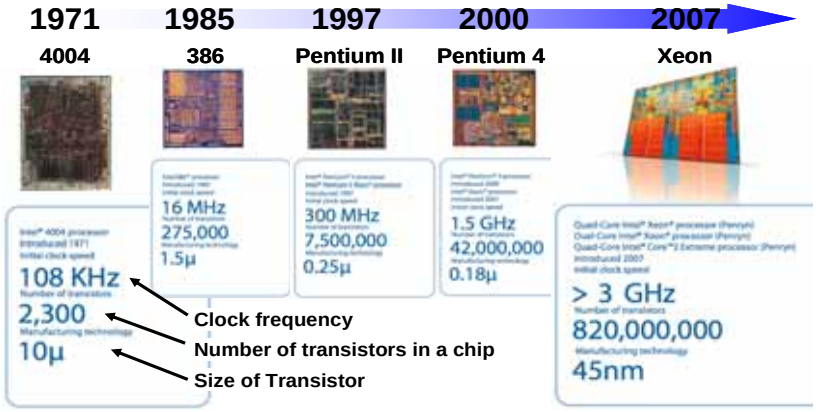


Fig 2.2 Specification of INTEL CPU's

The performance of silicon LSI depends on the capability of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) which is core part of LSI systems. In order to obtain high performance devises, it is necessary to miniaturize the MOSFET with the scaling method. The scaling method is based on reducing the device dimension in both lateral and vertical. The consensus scenario of how the device parameters are scaled for the next technology is provided in the International Technology Roadmap for Semiconductor (ITRS). A simple description of miniaturization with scaling factor of κ is shown in Figure 1.3 and Table 1.1. To gain k times of the device performance, the physical device dimensions are reduced by k times, while the electrical parameters are increased by k times.

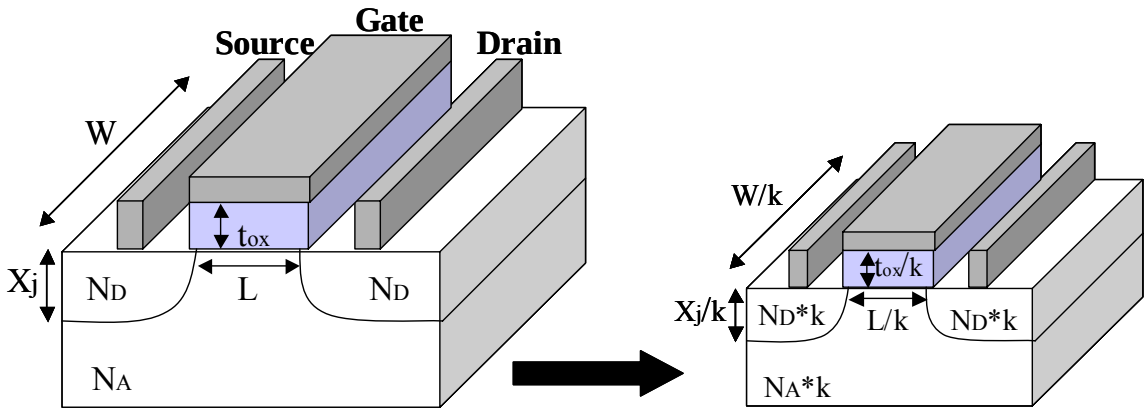


Figure 1.3 Scaling of MOSFET

Table 1.1 Scaling of MOSFET by a scaling factor of k

Quantity	**Before Scaling**	**After Scaling (k>1)**
Channel Length	L	L/k
Channel Width	W	W/k
Device Area	A	A/k^2
Gate Oxide Thickness	t_{ox}	t_{ox}/k
Gate Capacitance per Unit Area	C_{ox}	$C_{ox}*k$
Junction Depth	Xj	Xj/k
Power Supply Voltage	V_{DD}	V_{DD}/k
Threshold Voltage	Vth	Vth/k
Delay Time	t_d	t_d/k
Required Power	$V_{DD}I$	$V_{DD}I/k^2$
Doping Densities	N_A N_D	N_A*k N_D*k

1.2 Scaling Limit of SiO_2 Gate Dielectric

As is well known, Silicon dioxide film is the most common materials as the gate insulator film. However, a big hurdle is confronted to miniaturize the element size as in the past with keeping high performance and high integration.

From ITRS 2006 up date (Table 1.2), Equivalent Oxide Thickness (EOT) will rise to the below 1nm level in near future [2]. On the other hand, the direct-tunneling leakage current is too increasing to be neglected as shown in figure 1.4. Therefore, SiO_2 gate insulator film is to be replaced with an alternative material, which can be suppressed leakage current.

Table 1.2 ITRS 2006 up date

Year of Production	2005	2007	2010	2014	2018
Physical Gate Length (nm)	32	25	18	11	7
EOT (nm)	1.1	0.9	0.7	0.6	0.5
Gate Leakage Current Density (A/cm^2)	$5.20*10^2$	$5.20*10^2$	$5.20*10^3$	$5.20*10^3$	$5.20*10^4$

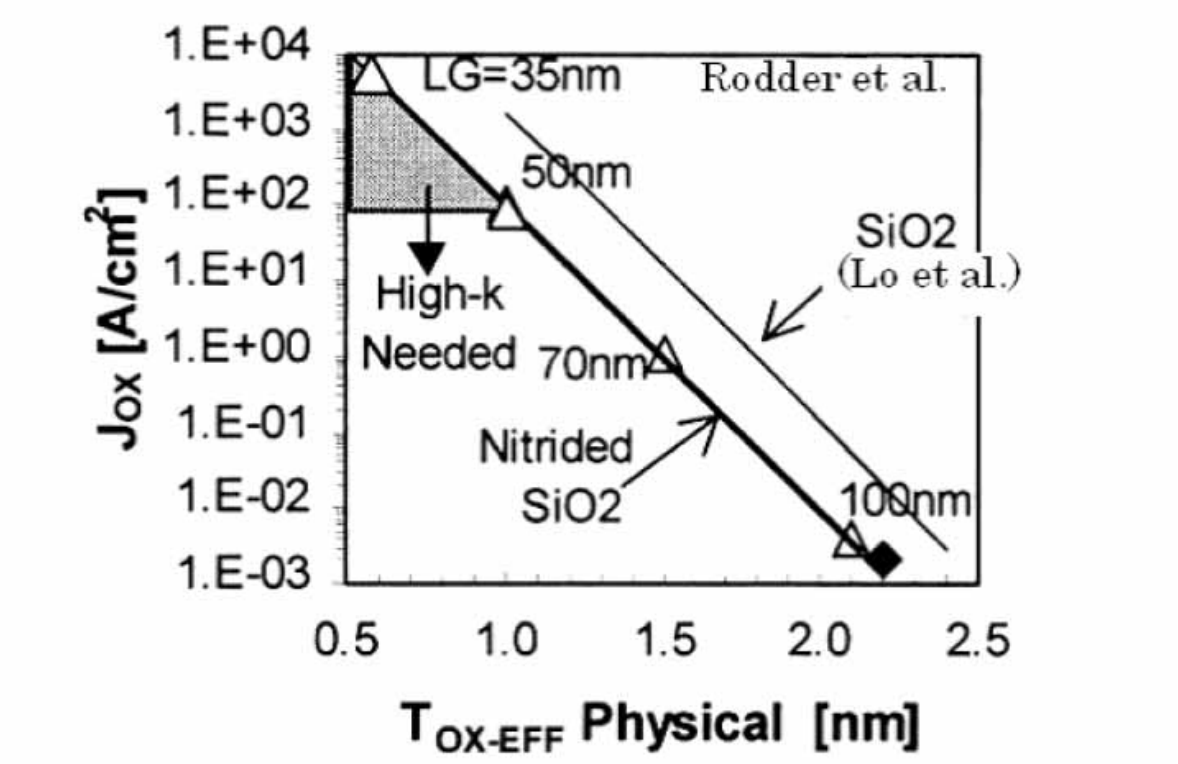


Fig 1.4 Relations between gate leakage current and physical thickness of SiO_2 film.

1.3 Requirement of High-k materials

The high dielectric constant (high-k) materials have been attracted to suppress the leakage current. The key guidelines for selecting an alternative gate dielectric material are high dielectric constant, large band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability. Among them, high dielectric constant and large band gap are the minimum required characteristics to suppress the gate leakage current. The direct-tunneling leakage current (J_{DT}) flow through a gate insulator film is determined by the tunneling probability of carrier. The tunneling probability of carrier (D_{DT}) is shown in below equation where physical thickness of insulator (d), electron effective mass in the gate insulator film (m^*) and barrier height of insulator (φ_b).

$$J_{DT} \propto D_{DT} \propto \exp\left\{-\frac{4\pi d(2m^*\phi_b)^{\frac{1}{2}}}{h}\right\}$$

Relationship between physical thickness of SiO_2 (d_{EOT}) and physical thickness of high-k gate insulator (d) obtained by the same gate capacitance value (C) is shown in below equation where dielectric constant of SiO_2 (ε_{ox}) and high-k gate insulator (ε_{high-k}).

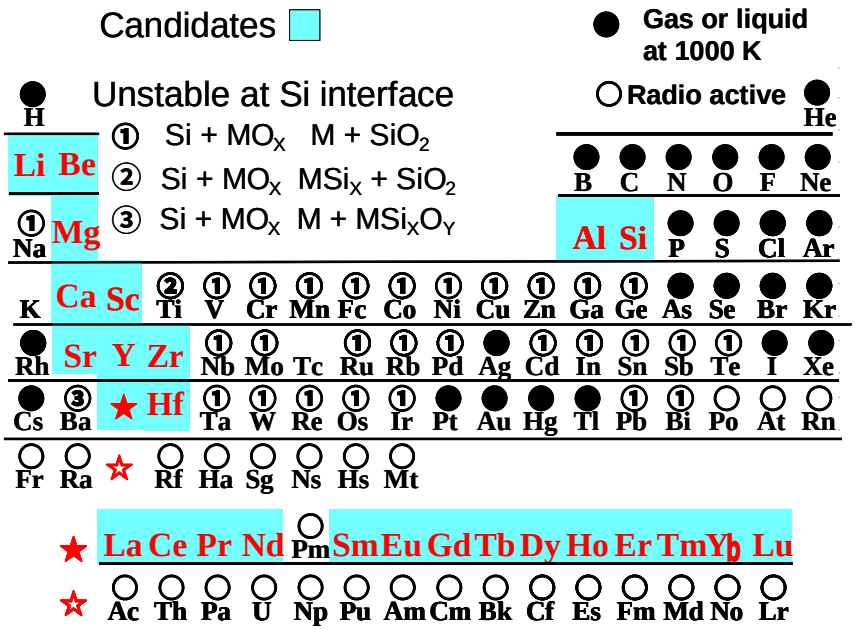
$$C = \frac{\varepsilon_{high-k}}{d} = \frac{\varepsilon_{ox}}{d_{EOT}}$$

$$d = \frac{\varepsilon_{ox}}{\varepsilon_{high-k}} d_{EOT}$$

Therefore, the gate leakage current can be suppressed by using high-k materials, which means that the physical thickness of high-k films can be thicken without changing EOT. In addition, the gate leakage current can also be suppressed by using large band gap materials. The possible candidate of several metal oxides system for the use of gate

dielectric material is shown in Table 1.3.

Table 1.3 Cadidate of metal oxide that has possibility to be used as high-k gate insulator



Among the candidate of high-k materials, Hf-based materials are the most promising candidate of them. As shown in Figure 1.5, many papers on high-k materials are submitted in the primary conferences up to 2002. However, from 2003 to now, the candidate of high-k materials have narrowed down to Hf-based materials. Therefore, Hf oxides (HfO_2) and Hf-based silicates or nitrides (HfSiON), with dielectric constants of 25 and 10 to 15 respectively, are among the promising materials for the 65 or 45-nm-technology nodes.

Usually, when the EOT becomes small, the effective carrier mobility tends to decrease due to scattering in the high-k layer or at the interface between the high-k layer and the substrate. It has reported that Hf-based films have reduced scattering when a SiO_2-based interfacial layer of 0.5 to 0.7 nm is inserted.

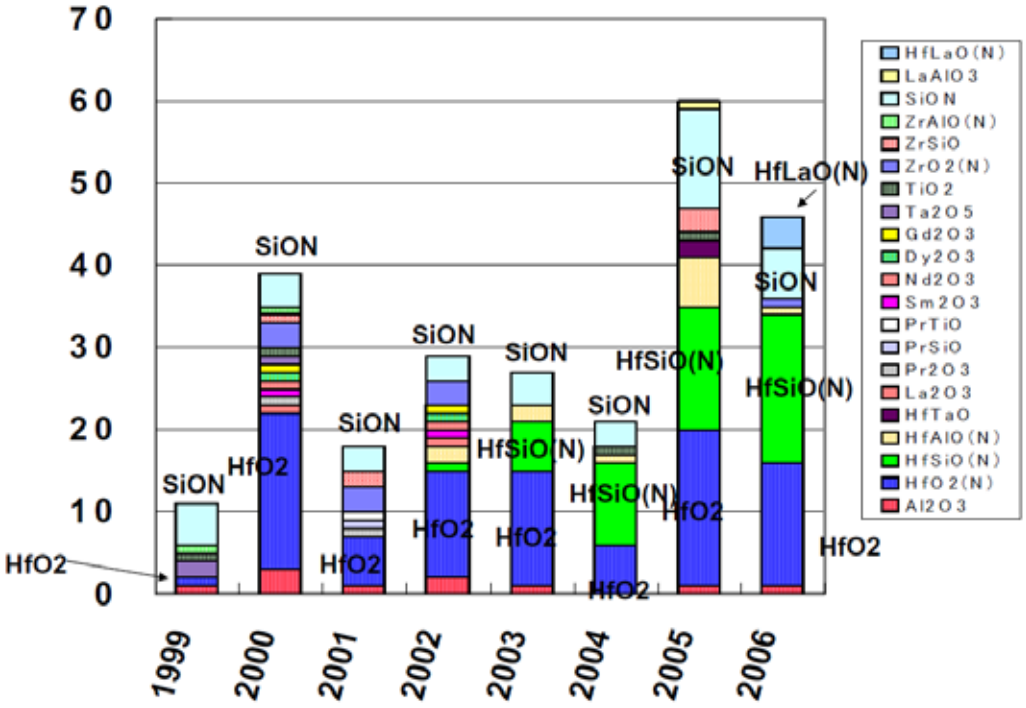


Fig 1.5 High-k materials reported in VLSI and IEDM

1.4 The requirement of Dual Metal/High-k Gate Stack Structure

Poly-Silicon has been used for CMOS devices as gate electrode. However, Poly-Si has some problems in proportion to advance the scaling.

1 Gate depletion

2 Boron penetration

3 V_{th} control by changing doping density

Metal gate technology is essential to overcome these problems. In addition to, poly-silicon gate have suffer from Fermi Level Pinning on high-k dielectrics as shown in figure 1.6.[3]

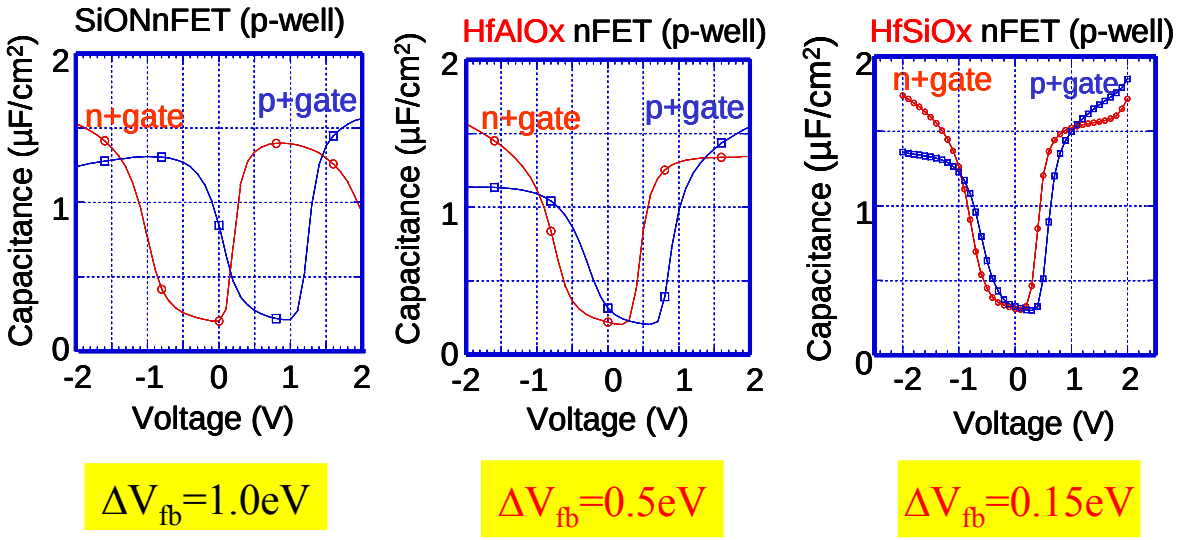


Fig 1.6 V_{fb} difference between n+ and p+ poly-Si HfO_2 based MOSCAPs

For bulk CMOS devices, metal gate must have proper work functions within 0.2 eV of the *Ec* and *Ev* of Si for n- and p-MOSFET, respectively as shown in table 1.3.[4]

Table 1.3 ITRS 2006 up date

Year of Production	2008	2009	2010	2011	2012
DRAM Half Pitch (nm)	57	50	45	40	36
EOT (nm) for Metal Gate	0.9	0.75	0.65	0.5	0.5
Metal Work Function $\lvert E_{v,c}-\phi_m \rvert$ (eV)	<0.2	<0.2	<0.2	<0.2	<0.2

1.5 Purpose of this study

Dual metal gate/High-k gate stack has been required to continue the downscaling CMOS devices. HfO_2 based oxide is considered to be promising candidate as high-k dielectric thanks to its high temperature endurance and relatively high permittivity. One of the issues of HfO_2 based oxides is the difficulty in reducing the threshold voltage (V_{th}) as relatively high V_{th} were obtained with HfO_2 based oxides whatever the electrode material is. On the other hand, it has been reported that La_2O_3 and Sc_2O_3 produce negative shift V_{FB} with respect to HfO_2 reference.[5]

In this work, in order to suppress and control the V_{th} of HfO_2, we propose a novel V_{th} tuning method using of different kind materials incorporating in HfO_2.

Chapter 2
Fabrication and Characterization Methods

2.1 Experiment procedure

2.1.1 Cleaning process

Prior to deposit of high-k gate thin films for LSI fabrication process, the ultra-pure surface of a Si-substrate should be chemically cleaned to remove particles contamination, such as metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. It is considered that this substrate cleaning process is very important to realize desirable device operation and its reproducibility. In full fabrication processes as well as substrate cleaning, DI (de-ionized) water is one of the most important because DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. Theoretical resistively of pure water at 25ºC is 18.3 MΩ·cm. The resistively value of ultra-pure water (UPW) used in this study achieve more than 18.2 MΩ·cm and have fewer than 1.2 colony of bacteria per milliliter and no particle larger than 0.25 um. In this study, the method of substrate cleaning process was used a typical processing using hydrofluoric acid, which is usually called RCA cleaning method, was proposed by W. Kern et al. But some steps were reduced. The steps were shown in Fig.2.1. Firstly, a cleaning steps in solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2 = 1:4, called by SPM) performed to remove any organic material and metallic impurities after UPW cleaning. Secondly, the step in a solution of dilated hydrofluoric acid (HF:H_2O=1:100) was performed to remove chemically and native oxides which might have been formed on Si surface. Final step was dipped in UPW because hydrogen-terminated surface.

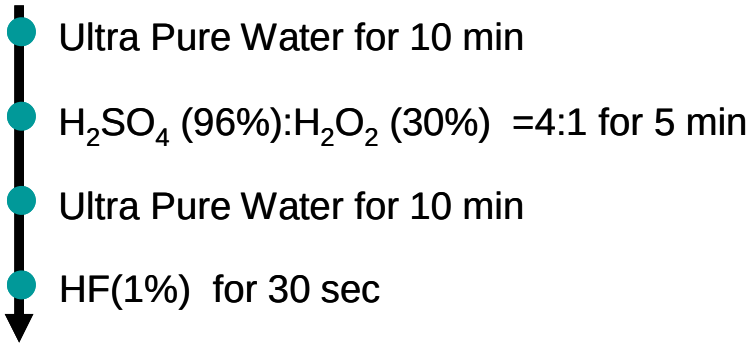


Fig 2.1 Si cleaning process flow

2.1.2 Fabrication procedure for MOS capacitors

Figure 2.2 shows device fabrication flow of Metal/High-k gate stack MOS capacitor. Si(100) substrates with 200 nm-thick field SiO_2 in which diode holes were opened (1-10 ohm-cm) were cleaned in a mixed solution of H_2SO_4 and H_2O_2, followed by dipping in diluted HF. The substrates were then thermally oxidized to grow 3.5-nm-thick SiO_2 film. High-k dielectrics were deposited on these substrates by e-beam evaporation with O_2 partial pressure of $1x10^{-4}$ Pa. Tungsten (W) gate electrode was *in-situ* deposited by RF sputtering. The W film was lithographically patterned and etched by reactive ion etching (RIE) using SF_6 chemistry to form gate electrodes for MOS capacitors. Annealing in forming gas (3 %-H_2+97 %-N_2) was performed at 420 ^oC for 30 min. Finally, aluminum (Al) was thermally evaporated on backside of the wafers for bottom electrode.

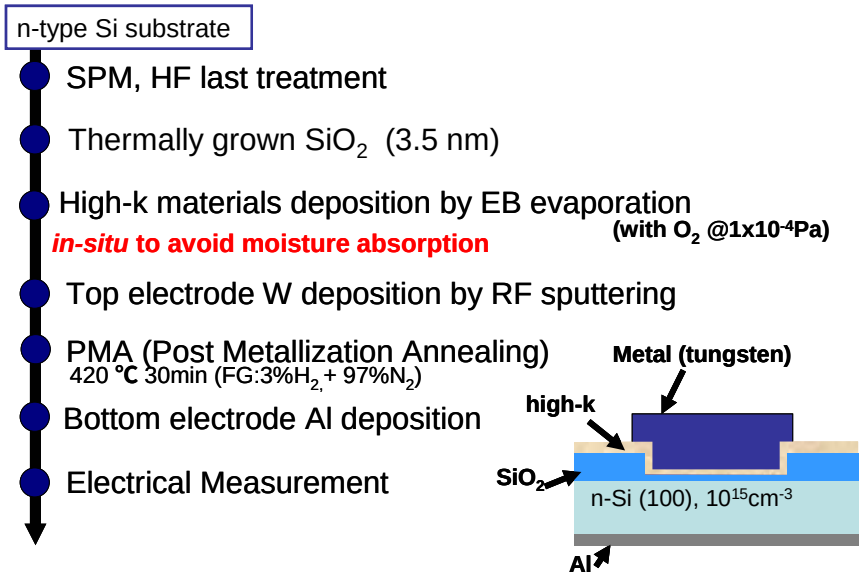


Fig 2.2 The fabrication procedure for MOSCAP

2.1.3 Fabrication procedure for MOSFETs

The fabrication procedure for nMOSFET is shown in Figure 2.3. nMOSFET fabrication was started from S/D implanted Si(100) substrate. High-k thin film was deposited by Electron-Beam Evaporation followed by substrate cleaning. After metal gate formation, the gate area was defined with photolithography followed by metal gate etching. Annealing in forming gas was performed at 500 ^{o}C for 30 min. The Al-Pad area was formed with lift-off process under acetone solution and Al back side electrode were formed afterwards.

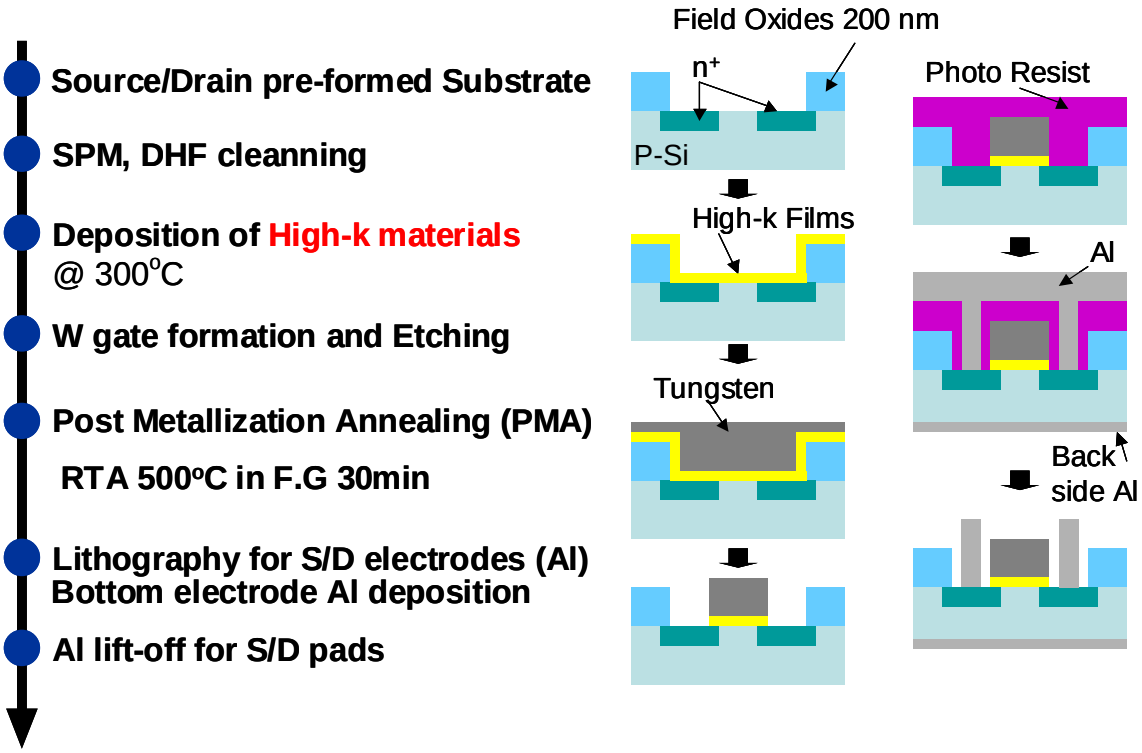


Fig 2.3 The fabrication procedure for nMOSFET

2.2 Measurement Methods

2.2.1 *C-V* (Capacitance-Voltage) Measurement

C-V characteristic measurements were performed with various frequencies (1kHz ~ 1MHz) by precision LCR Meter (HP 4284A, Agilent). The energy band diagram of an MOS capacitor on a p-type substrate is shown in figure 2.4 [6]. The intrinsic energy level E_i or potential φ in the neutral part of device is taken as the zero reference potential. The surface potential φ_s is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \qquad (2.1)$$

It is the change of charge due to a change of voltage and is most commonly given in units of farad/units area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS capacitor from the gate, $C = dQ_G / dV_G$, where Q_G and V_G are the gate charge and the gate voltage. Since the total charge in the device must be zero, assuming no oxide charge, $Q_G = -(Q_S + Q_{it})$, where Q_S is the semiconductor charge, Q_{it} the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \varphi_s$, where V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and φ_s the surface potential, allowing Eq. (2.1) to be rewritten as

$$C = \frac{dQ_s + dQ_{it}}{dV_{ox} + d\phi_s} \tag{2.2}$$

The semiconductor charge density Q_S, consists of hole charge density Q_p, space-charge region bulk charge density Q_b, and electron charge density Q_n. With $Q_S = Q_p + Q_b + Q_n$, Eq. (2.2) becomes

$$C = -\frac{1}{\frac{dV_{ox}}{dQ_s + dQ_{it}} + \frac{d\phi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \tag{2.3}$$

Utilizing the general capacitance definition of Eq. (2.1), Eq. (2.3) becomes

$$C = -\frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_p + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_{it}} \tag{2.4}$$

The positive accumulation Q_p dominates for negative gate voltages for *p*-substrate devices. For positive V_G, the semiconductor charges are negative. The minus sign in Eq. (2.3) cancels in either case.

Eq. (2.4) is represented by the equivalent circuit in figure 2.5 (a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_p is very high

approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in figure 2.5 (b) and the overall capacitance is C_{ox}. For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = -qN_AW$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} as shown in figure 2.5 (c). In weak inversion C_n begins to appear. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (figure 2.5 (d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in figure 2.5 (e) applies in inversion, with $C_b = K_s \varepsilon_o / W_{inv}$ with W_{inv} the inversion space-charge region width. The flatband voltage V_{FB} is determined by the metal-semiconductor work function difference φ_{MS} and the various oxide charges through the relation

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{tox} \rho_m(x)dx - \frac{1}{C_{ox}}\int_0^{tox} \frac{x}{t_{ox}}\rho_{ot}(x)dx \quad (2.5)$$

where $\rho(x)$ = oxide charge per unit volume. The fixed charge Q_f is located very near the Si-SiO_2 interface and is considered to be at that interface. Q_{it} is designated as $Q_{it}(\varphi_s)$, because the occupancy of the interface trapped charge depends on the surface potential.

Mobile and oxide trapped charges may be distributed throughout the oxide. The x-axis is defined in figure 2.4. The effect on flatband voltage is greatest, when the charge is located at the oxide-semiconductor substrate interface, because then it images all of its charge in the semiconductor. When the charge is located at the gate-insulator interface, it images all of its charge in the gate and has no effect on the flatband voltage. In the

study, principally, EOT values and flatband voltage were extracted from *C-V* characteristics by using the NCSU CVC modeling program [7]. EOT values were calculated with taking quantum effect into account.

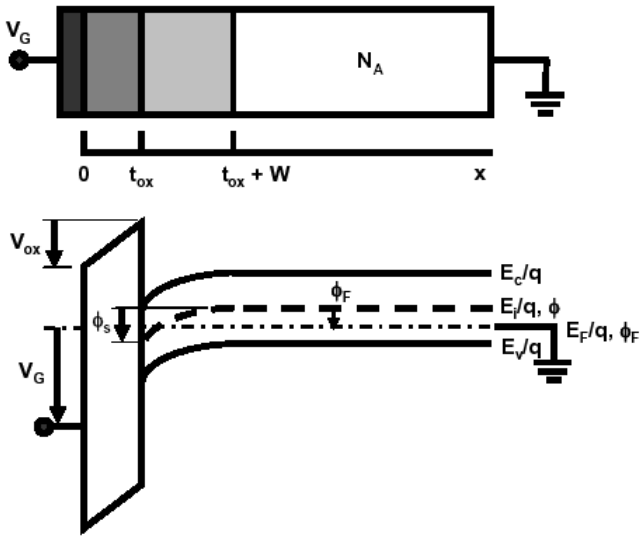


Fig 2.4 The energy band diagram of an MOS capacitor on a p-type substrate

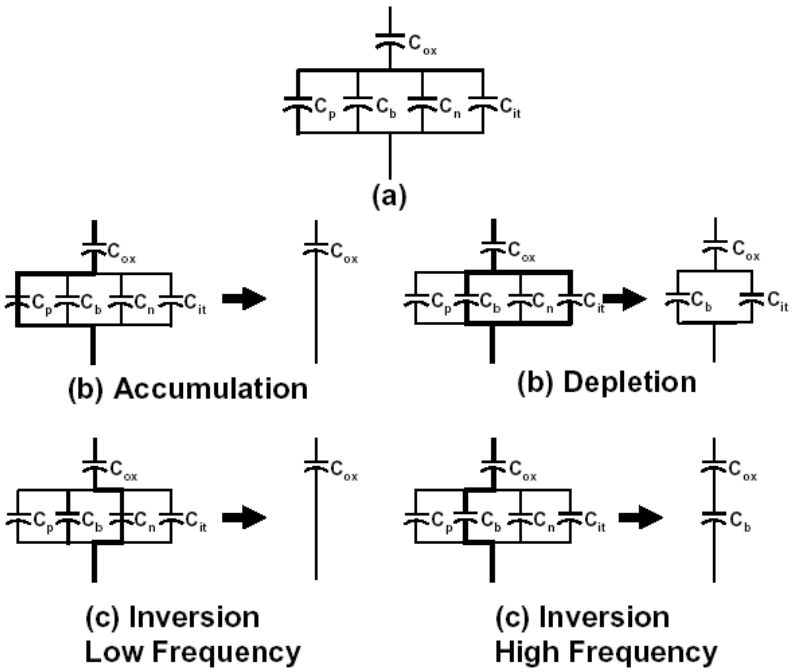


Fig 2.5 Capacitances of an MOS capacitor for various bias conditions.

2.2.2 Threshold Voltage (V_{th}) Measurement

A common threshold voltage measurement technique is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of typically 50-100mV to ensure operation in the linear MOSFET region.

The threshold voltage is determined from the extrapolated or intercepts gate voltage V_{GSi} by

$$V_T = V_{GSi} - \frac{V_{DS}}{2} \tag{2.6}$$

where

$$V_{GSi} = V_{GS,\max} - \frac{I_{D,\max}}{g_{m,\max}} \tag{2.7}$$

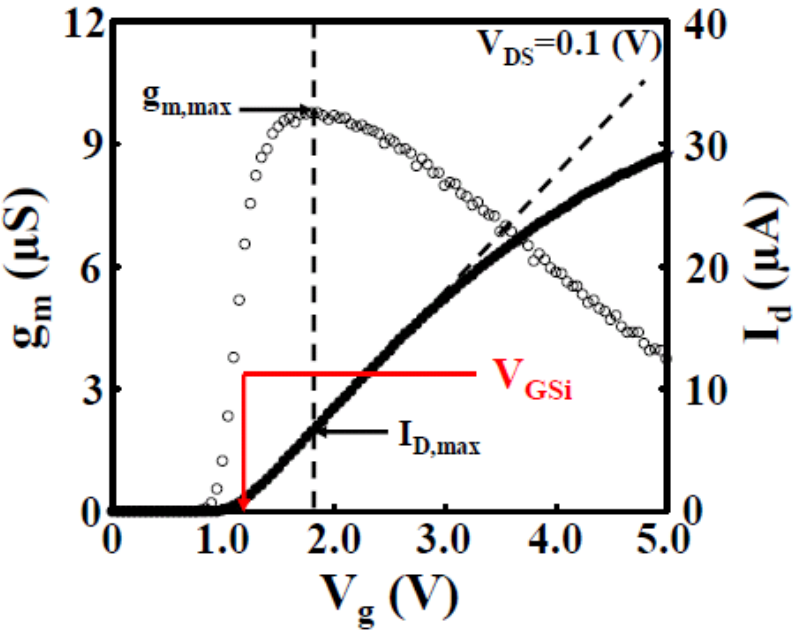


Fig 2.6 The linear extrapolation method

2.2.3 Subthreshold Slope *(S.S.)* Measurement

The subthreshold current is independent of the drain voltage once V_{ds} is larger than a few kT/q, as would be expected for diffusion-dominanted current transport. The dependence on gate voltage, on the other hand, is exponential with an inverse subthreshold slope,

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{mkT}{q} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \qquad (2.8)$$

of typically 70-100mV/decade. Here $m=1+(C_{dm}/C_{ox})$. If the Si-SiO_2 interface trap density is high, the subthreshold slope may be more graded than given by Eq(2.8), since the capacitance associated with the interface trap is in parallel with the depletion-layer capacitance C_{dm}.

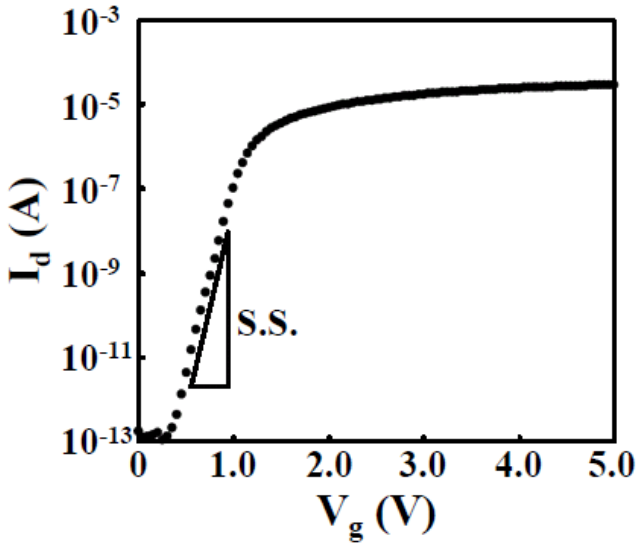


Fig 2.7 The subthreshold slope calculated from I_d-V_g characteristic

2.2.4 Split *C-V* Method

One of the most common measurements to obtain the effective mobility (μ_{eff}) is the split C-V method, which combines gate-to-channel capacitance (C_{gc}) and gate-to-bulk capacitance (C_{gb}).

μ_{eff} is obtained from below equation,

$$\mu_{eff} = \frac{g_d L}{W Q_n} \tag{2.9}$$

where the drain conductance g_d and the inversion density Q_n are define as

$$g_d = \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}=constant} \tag{2.10}$$

$$Q_n = \int_{V_{FB}}^{V_{GS}} C_{gc} dV_{GS} \tag{2.11}$$

E_{eff} is obtained from below equation,

$$E_{eff} = \frac{1}{\varepsilon_{Si}}(|Q_d| + |Q_n|) \tag{2.12}$$

where ε_{Si}=11.9 and the depletion charge density Q_d are defined as

$$Q_d = \int_{V_{FB}}^{V_{th}} C_{gb} dV_{GS} \tag{2.13}$$

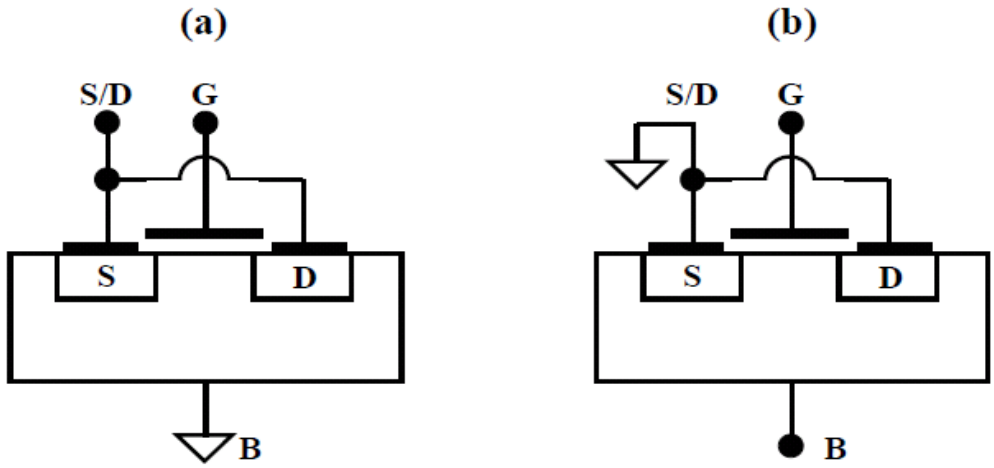


Fig 2.8 Configuration for (a) gate to channel, (b) gate to substrate capacitance measurements

2.2.5 Charge Pumping Methods

In the charge pumping method, originally proposed in 1969, a MOSFET is used as the test structure, making it suitable for interface trap measurements on small-geometry MOSFETs instead of large –diameter MOSCAP.

Let us begin by considering the MOSFET in inversion shown in Figure 2.9(a). The corresponding semiconductor band diagram from the Si surface into the substrate is shown in figure 2.9(c). The interface traps, continuously distributed through the band gap, are represented by the small horizontal lines at the semiconductor surface with the filled circles representing electrons occupying interface traps. When the gate voltage changes from positive to negative potential, the surface change from inversion to accumulation and ends up as in figure 2.9(b,f). However, the important processes take place during the transition from inversion to accumulation and from accumulation to inversion.

When the gate pulse falls from its high to its low value during its finite transition time, most electrons in the inversion layer drift to source and drain and electrons on those interface traps near the conduction band (figure 2.9 (d)) and also drift to source and drain. Those electrons on interface traps deeper within the band gap do not have sufficient time to be emitted and will remain on interface traps. Once the hole barrier is reduced(figure 2.9 (e)), holes flow to the surface where some are captured by those interface traps still occupied by electrons. Holes are indicated by the open circles on the band diagrams. Finally, most traps are filled with holes as shown in figure 2.9(f). Then, when the gate returns to its positive voltage, the inverse process begins and electrons flow into the interface to be captured. Hence, charge pumping current I_{cp} is proportional

to D_{it}.

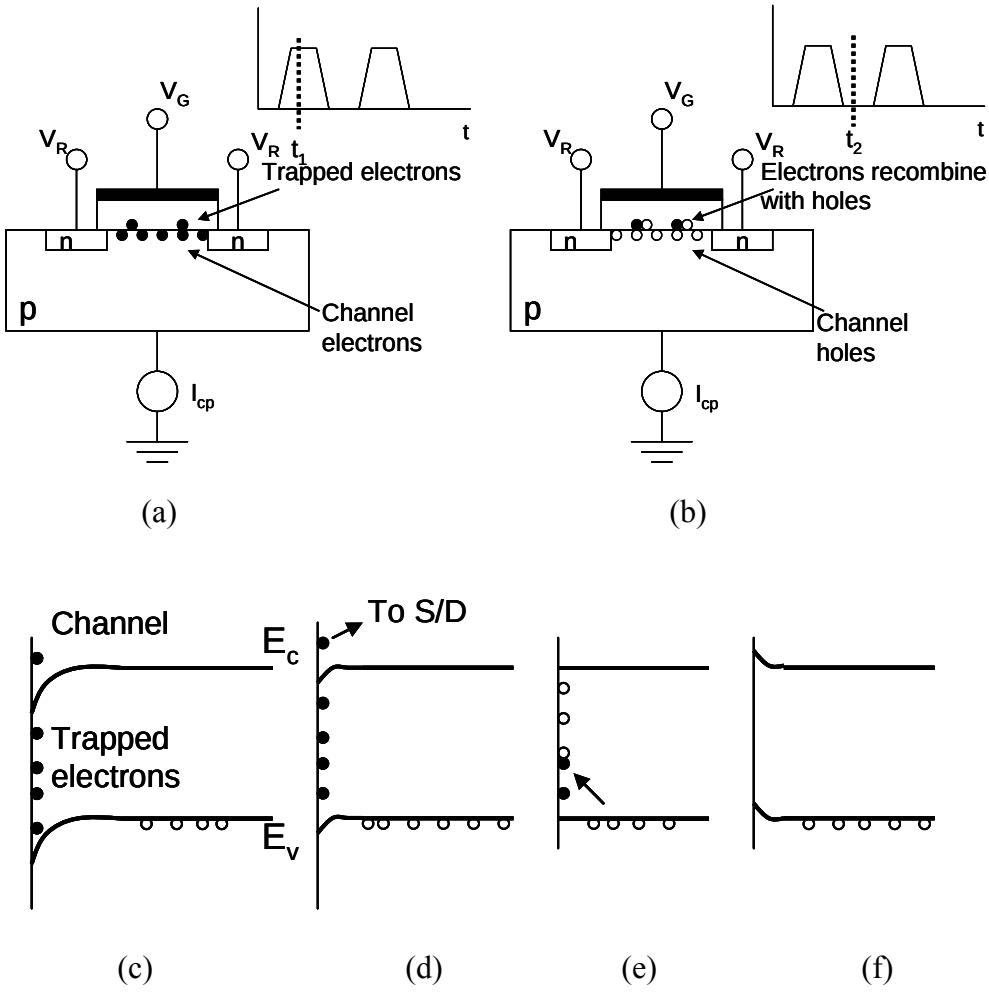


Fig 2.9 Device cross-section and energy band for charge pumping measurements.

Dit holes being supplied at rate of *f* Hz to a MOSFET with gate area A_G gives the charge pumping current,

$$I_{cp} = qA_G fD_{it} \qquad (2.14)$$

The gate voltage waveform can be of various shapes. Early work used square waves. Later trapezoidal and sinusoidal waveforms were used. The waveforms can be constant base voltage in accumulation and pulsing with varying the base voltage from inversion to accumulation keeping ΔV constant as shown in figure 2.10. The letters "a" to "e" on figure 2.10 correspond to the points on the current waveforms.

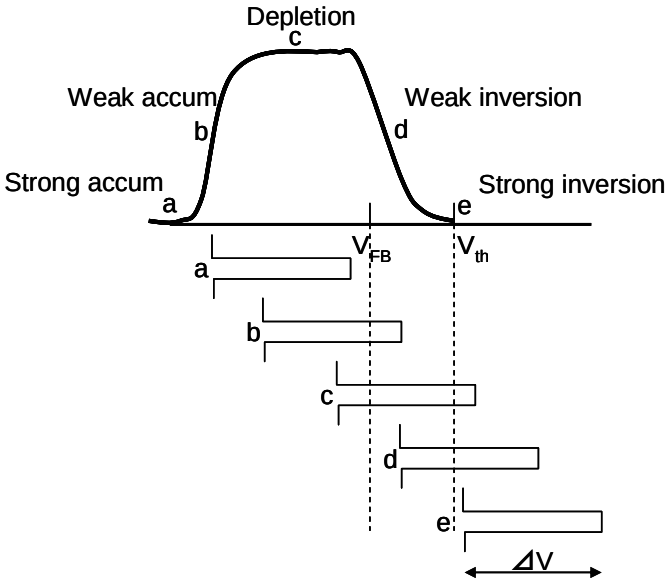


Fig 2.10 Bilevel charge pumping wave form

2.2.6 XPS Measurement

XPS, also known as the Electron Spectroscopy for Chemical Analysis (ESCA), is one of the useful methods to evaluate chemical bindings in the oxide or at the interface. Figure 2.3 explains the principle of XPS. Samples were irradiated with X-ray and the emitted photoelectrons with kinetic energy KE were detected. Measured KE was given by

$$KE = h\nu - BE - \phi_s \qquad (2.15)$$

where $h\nu$ is the photon energy, BE is the binding energy of the atomic orbital from which the electron generates and ϕ_s is the spectrometer work function. The binding energy is the minimum energy needs for breaking the chemical bond of molecule and is inherent in each bond of molecule. Thus, the binding states can be identified by the positions of the binding energy which the peak appears. In the case that the peak position was different from the expected position, the chemical bond states were discussed considering the amount of shift to higher or lower energy side.

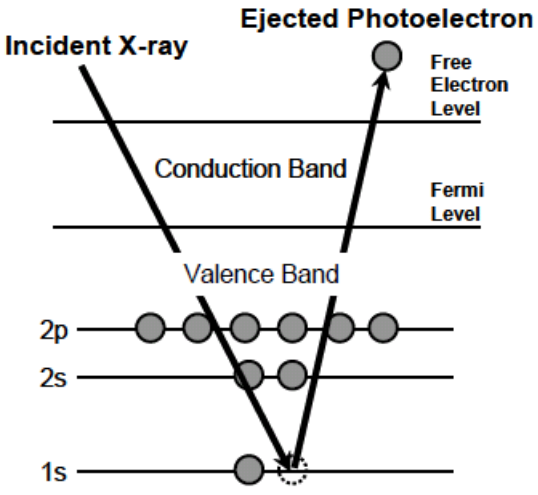


Fig 2.11 Principle of XPS measurement.

Conventional XPS techniques with low excitation energies are surface-sensitive due to short inelastic mean-free-paths (IMFPs), and it is difficult to obtain information on the bulk electronic structures which are closely correlated with the characteristics of the intrinsic materials. In this study, Hard X-ray Photoemission Spectroscopy (HX-PES) is performed at Super Photon ring- 8 GeV (SPring-8). SPring-8 is the one of the world's largest radiation facilities. The advantages of SPring-8 over average XPS equipments are the high-brightness of radiation which is about a hundred thousand times as high as normal X-ray and the high radiation energy of 30keV ~ 40keV.

Chapter 3
Flat-band Voltage (V_{FB}) Shift in Double Layer Dielectric Films

3.1 Introduction

HfO_2 based materials have been the promising candidates for next generation gate dielectric thanks to its high temperature endurance and relatively high permittivity. One of the issues of HfO_2 based oxides is the difficulty in reducing the threshold voltage (V_{th}) as relatively high V_{th} were obtained. On the other hand, it has been reported that La_2O_3 and Sc_2O_3 produce negative shift in V_{FB} with respect to HfO_2 reference. However, the detailed mechanism is not clarified yet. In this chapter, first we extract the effective work function (*EWF*) of W gate metal on high-k dielectrics, and then investigated the effect of La_2O_3 incorporation into a HfO_2 layer in a metal/HfO_2/SiO_2/Si MOS capacitor.

3.2 Effective Work Function *(EWF)* Extraction on High-k Materials

In order to investigate the *EWF* on dielectrics, high-k films were fabricated, as shown in Figure 3.1. Capacitors with single layer of SiO_2, HfO_2 , La_2O_3 and Sc_2O_3 are fabricated. The thickness of the interfacial layer (IL) was designed to have 3.5 nm. CV characteristics of the W/high-k/IL structures with 420^{o}C PMA in F.G ambient for 30min are shown in Figure3.2.

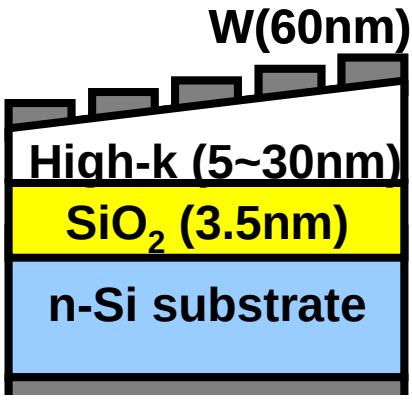


Figure 3.1 Schematic illustration of fabricated MOS capacitors with W/high-k/IL/Si structures.

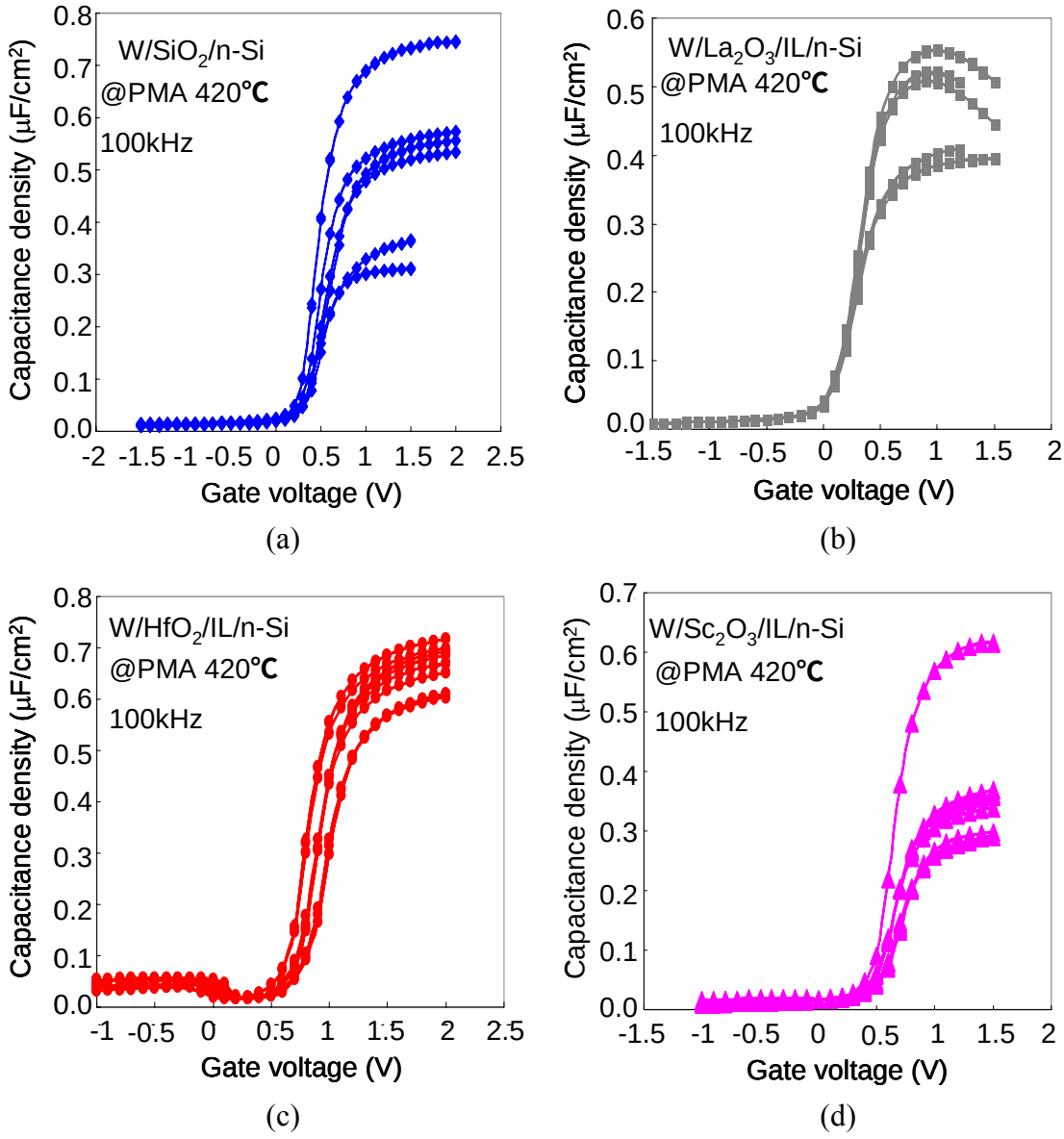


Fig 3.2 C-V curves for W/high-k/IL(3.5nm) structures.
(a) SiO_2 single layer, (b) La_2O_3/IL, (c) HfO_2/IL, (d) Sc_2O_3/IL,

Figure 3.3 shows the typical *C-V* curves of La_2O_3/IL, HfO_2/IL and Sc_2O_3/IL capacitors. The difference between $V_{FB}(HfO_2/IL)$ and $V_{FB}(La_2O_3/IL)$ is about 0.48 V, whereas difference between $V_{FB}(HfO_2/SiO_2)$ and $V_{FB}(Sc_2O_3/SiO_2)$ is 0.15 V. It is clear that V_{FB} of the *CV* characteristics with HfO_2/IL stacks reside at the positive direction compared to those of Sc_2O_3/IL and La_2O_3/IL stacks.

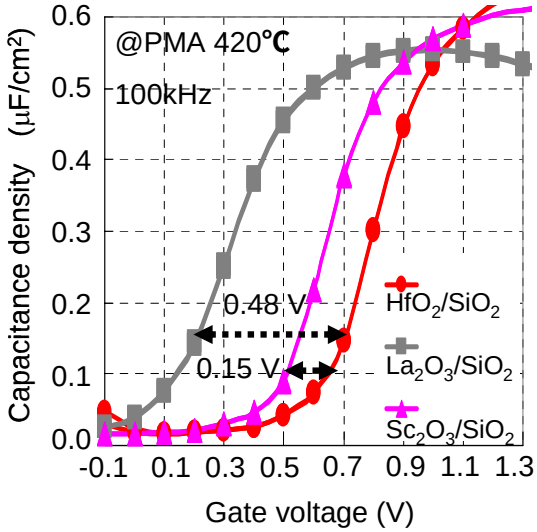


Fig.3.3 *C-V* characteristics of MOS capacitors with single layered high-k dielectric (HfO_2, La_2O_3, Sc_2O_3)

A schematic model of the charge locations in a metal/SiO_2/Si structure and metal/high-k/SiO_2/Si structure are illustrated in Fig 3.4. As the thickness of the dielectric layer is small, the bulk charges of each oxide can be neglected.[8] Indeed, the results shown in Fig. 3.5 revealed a linear relationship between V_{FB} and the EOT, thus, it is reasonable to assume low charge concentration inside the SiO_2 and the high-k layer. Under the assumption, the effective work function (*EWF)* of metal on a SiO_2 can be derived from the relation of V_{FB} and EOT using the following equation,

$$V_{FB} = -\left(\frac{Q_{SiO2/Si}}{\varepsilon_0 \varepsilon_{ox}} \right) \cdot EOT + \frac{\varphi_{ms}}{q} + q\Delta_{SiO2/Metal} + q\Delta_{SiO2/Si} \qquad (3.1)$$

where $Q_{SiO2/Si}$ is the fixed charge at the SiO_2/Si interface, ϕ_{ms} is the work function difference of gate metal and semiconductor, and $\Delta_{SiO2/Metal}$ and $\Delta_{SiO2/Sil}$ are the dipole at metal/oxide and oxide/Si interfaces. The *EWF* of gate metal, defined as $\frac{\varphi_{ms}}{q} + q\Delta_{SiO2/Metal} + q\Delta_{SiO2/Si}$, can be extracted by the y-intercept from the V_{FB}-EOT slope. When interfacial SiO_2 layer (IL) is inserted between high-k dielectric and Si substrate, the Eq.(3.1) can be modified using total EOT as shown in eq.(3.2),

$$V_{FB}^{\cdot} = -\left(\frac{Q_{high-k/IL} + Q_{SiO2/Si}}{\varepsilon_0 \varepsilon_{ox}} \right) \cdot EOT + \frac{Q_{high-k/IL}}{\varepsilon_0 \varepsilon_{ox}} \cdot EOT_{IL} + \frac{\varphi_{ms}}{q} + q\Delta_{Metal/high-k} + q\Delta_{high-k/SiO2} + q\Delta_{SiO2/Si}$$

(3.2)

Here, $Q_{high\text{-}k/IL}$, $\Delta_{high\text{-}k/Metal}$ and EOT_{IL} are the fixed charge at high-k/IL interface, the dipole at high-k/metal interface and the EOT of IL, respectively. Eventually, the *EWF* of metal on high-k/SiO_2 stack can be expressed as follows,

$$EWF_{(high-k)} = EWF_{(SiO2)} + (q\Delta_{high-k/Metal} + q\Delta_{high-k/SiO2} - q\Delta_{SiO2/Metal}) \qquad (3.3)$$

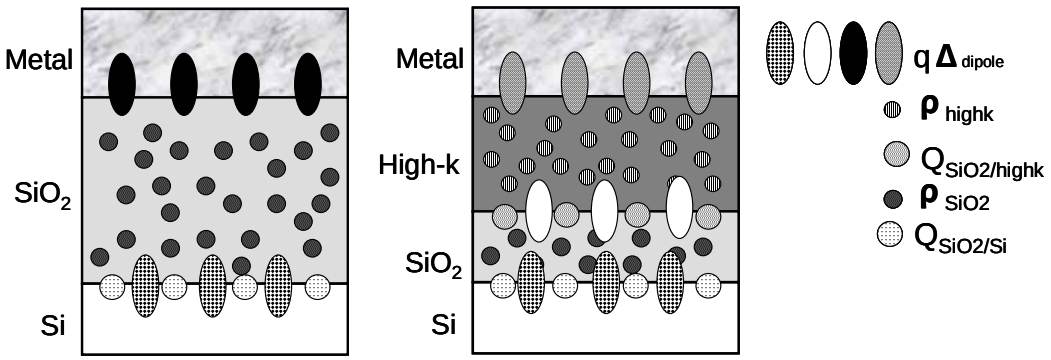


Fig 3.4 Schematic model of the charge locations used in the extraction of fixed charge and dipoles

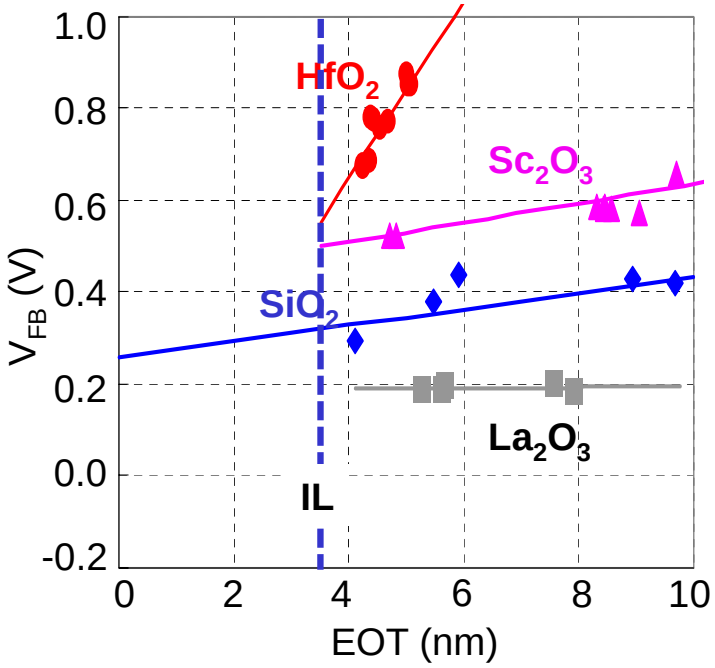


Fig 3.5 V_{FB}-EOT plot obtained from the analysis of *C-V* curves

Capacitors with SiO_2 with different thickness are also shown to derive $Q_{SiO2/Si}$. Using the equation (3.1), $Q_{SiO2/Si}$ of $-3.72x10^{11}cm^{-2}$ can be obtained by SiO_2 capacitors. Then $Q_{high-k/IL}$ for La_2O_3, HfO_2 and Sc_2O_3 using equation (3.2), can be estimated as shown in table 3.1. As shown in figure 3.6(a), the presence of La-Silicate layer was confirmed by transmission electron microscope (TEM) observation. In this calculation, the presence of La-silicate was neglected simplicity.

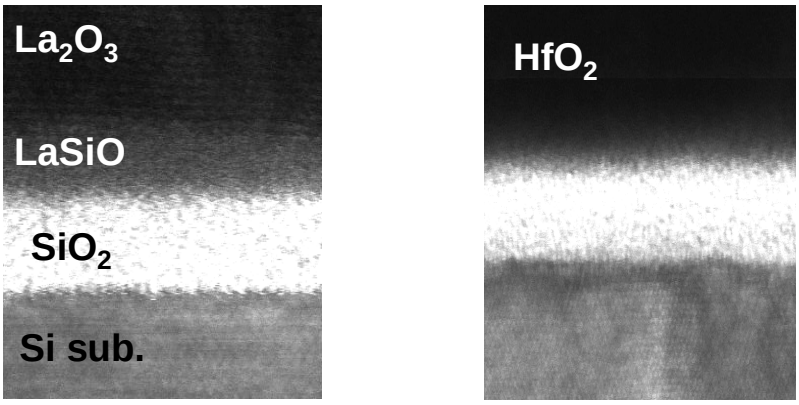


Fig 3.6 The cross-sectional TEM images of La_2O_3/La-silicate/IL (a) and HfO_2/IL (b). La-silicate was confirmed about 2.5nm.

Table 3.1 Fixed charges at high-k/SiO_2 interface as W electrode

$Q_{SiO2/Si}$	$-3.72\times10^{11}(cm^{-2})$
$Q_{HfO2/SiO2}$	$-4.27\times10^{10}(cm^{-2})$
$Q_{La2O3/SiO2}$	$3.89\times10^{11}(cm^{-2})$
$Q_{Sc2O3/SiO2}$	$-8.32\times10^{11}(cm^{-2})$

The difference of total dipole between the $q\Delta_{high-k}$ and $q\Delta_{SiO2}$ is shown in table 3.2.

The dipole differences at W/high-k interface cannot be separated at this point.

Table3.3. The difference of total dipole between the $q\Delta_{high\text{-}k}$ and $q\Delta_{SiO2}$

Dipole difference $q(\Delta_{high\text{-}k}-\Delta_{SiO2})$	(eV)
$q(\Delta_{La2O3}-\Delta_{SiO2})$	**- 0.14 eV**
$q(\Delta_{HfO2}-\Delta_{SiO2})$	**0.22 eV**
$q(\Delta_{Sc2O3}-\Delta_{SiO2})$	**0.16 eV**

EWF of W on SiO_2, HfO_2, La_2O_3 and Sc_2O_3 can be calculated and summarized in Table.3.1 and 3.2. The smallest *EWF* of 4.46 eV was obtained with La_2O_3, whereas relatively large value was obtained with HfO_2.

Table3.3. Effective work function of W gate electrode on various gate dielectric (SiO_2, La_2O_3, HfO_2, Sc_2O_3)

Gate Oxide	SiO_2	La_2O_3	HfO_2	Sc_2O_3
EWF (eV)	4.59	4.46	4.80	4.75

These results suggest high V_{th} in nMOSFET when HfO_2 is used as gate dielectrics. In the next subsection, the origin of V_{FB} is examined in detail.

3.3 Origin of Flat-band Voltage Shift in Double Layer Dielectric Films

3.3.1 C-V Characteristics of W/HfO_2/La_2O_3 or (La_2O_3/HfO_2)/n-Si Stack Structure

In order to investigate the V_{FB} shift on stacked dielectrics, double layer without IL stacked films were fabricated, as shown in Fig. 3.7.

Capacitors with single layer of HfO_2 or La_2O_3 are also fabricated as references. The total thickness of the high-k film was designed to have 5 nm, in which the thickness of each layer was modified from 1 to 4 nm.

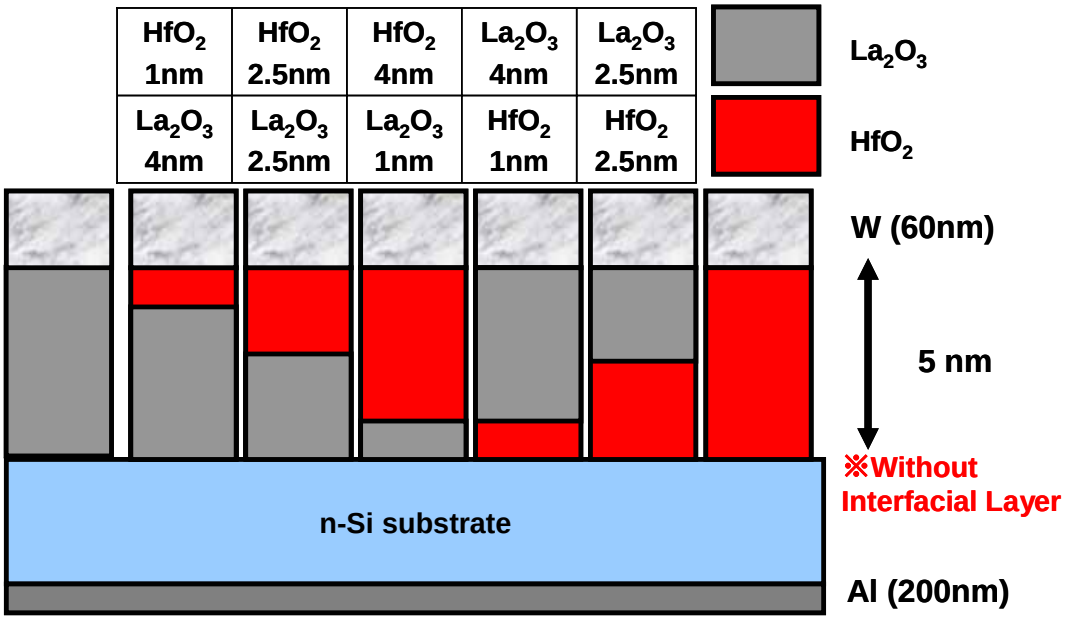


Fig 3.7 Schematic illustration of fabricated with out IL MOS capacitors with stack of HfO_2 and La_2O_3. Capacitors with single HfO_2 or La_2O_3 layer are fabricated as references.

Figure 3.8 and 3.9 shows the *C-V* characteristics of $W/HfO_2/La_2O_3$ or $W/La_2O_3/HfO_2$ stacked MOS capacitors with as deposition and 420°C PMA in F.G ambient for 30min. In case of as deposition as shown in figure 3.8, We cannot estimate the V_{FB} to be right by existence of large hysteresis and growth of hump with La_2O_3 insertion.[9]

On the other hand, the capacitance with La_2O_3 even with 1 nm insertion at HfO_2/Si interface showed negative V_{FB} shift with 420°C PMA. Almost no dependence on the insertion thickness was observed up to La_2O_3 single layer capacitor. On the contrary, the capacitors with HfO_2 at the Si interface showed positive V_{FB} shift, which are close to HfO_2 single layer capacitor. Therefore, it is clear from this result that the main cause for shifting the V_{FB} is determined by high-k, which is contact to Si substrate.

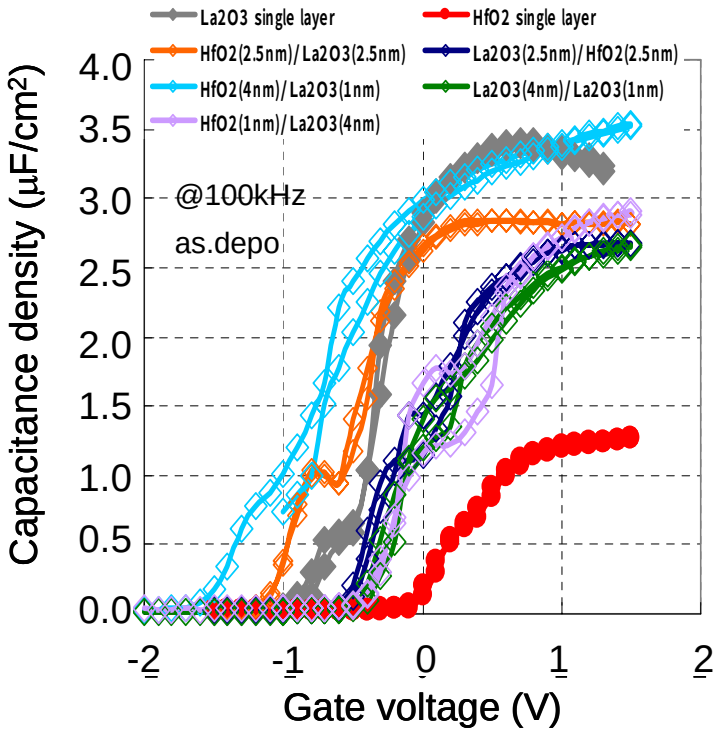


Fig 3.8 *C-V* characteristics of La_2O_3 and HfO_2 stacked MOS capacitors without thermal treatment.

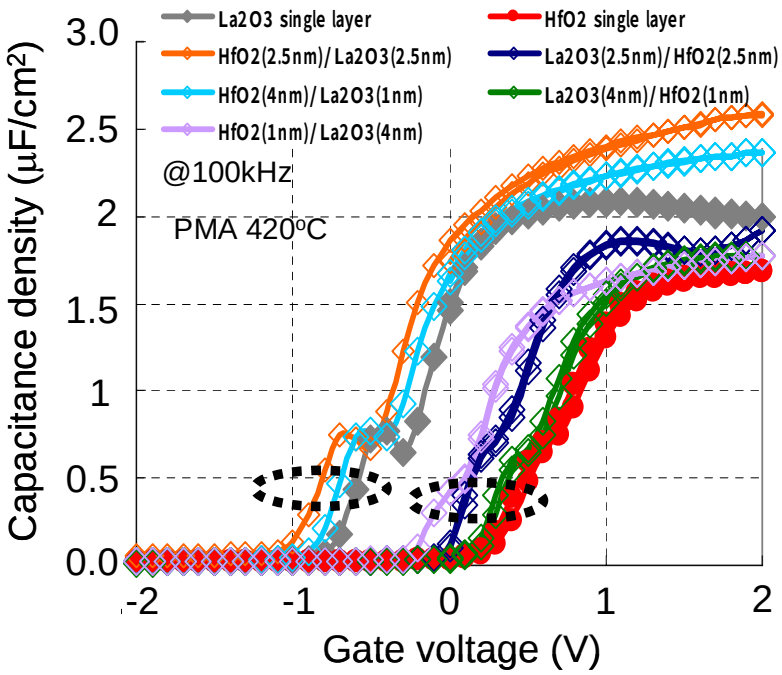


Fig 3.9 *C-V* characteristics of La_2O_3 and HfO_2 stacked MOS capacitors with PMA 420°C.

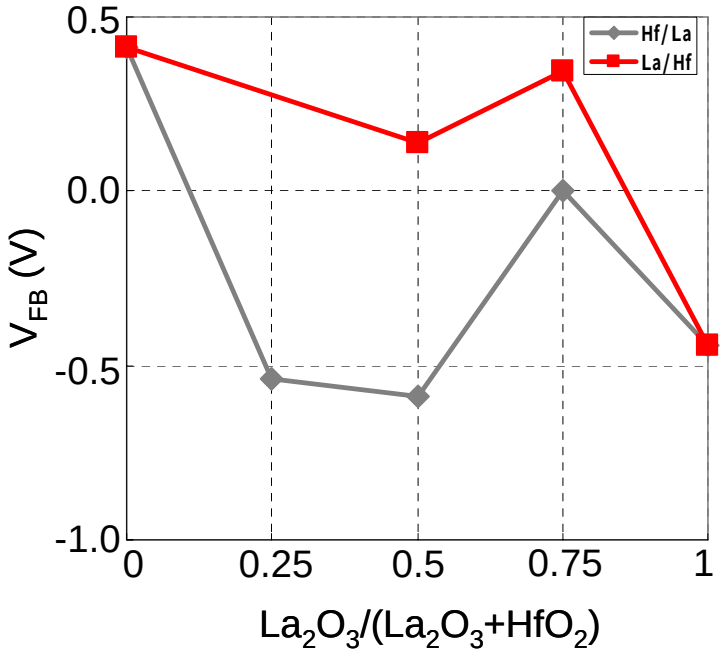


Fig 3.10 Flatband voltages of La_2O_3 and HfO_2 stacked capacitors on n-Si at PMA 420°C.

3.3.2 *C-V* Characteristics of W/HfO_2/La_2O_3 or (La_2O_3/HfO_2)/IL/n-Si Stack Structure

As is the case with HfO_2/La_2O_3 without IL structures, We fabricated and characterized capacitors with La_2O_3 and HfO_2 stack with IL for 420°C PMA in F.G ambient for 30min. Figure 3.11 shows the schematic illustration of the fabricated MOS capacitors with high-k stacks. The total thickness of the high-k films were all set to 5 nm, in which the thickness of each layer was modified from 1 to 4 nm.

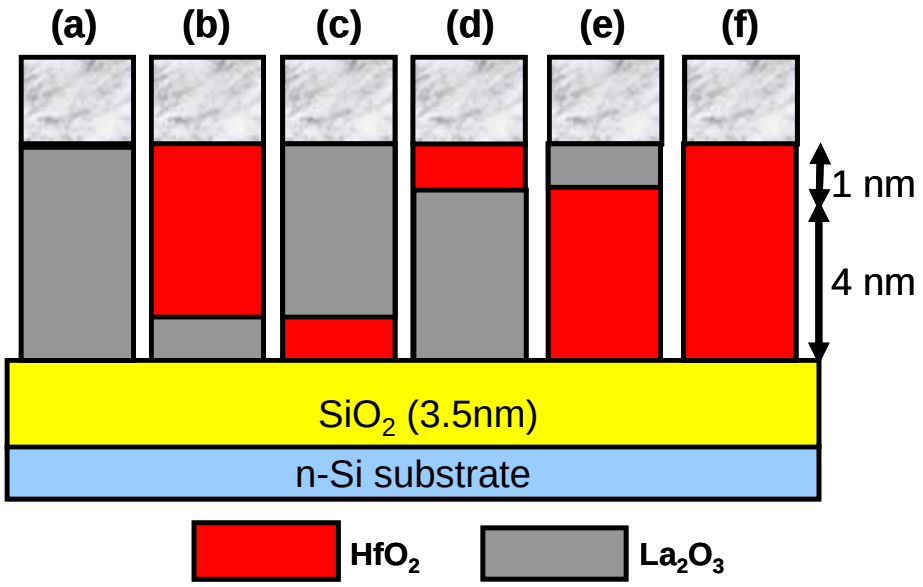


Fig 3.11 Schematic illustration of fabricated MOS capacitors with IL (3.5nm) of HfO_2 and La_2O_3. Capacitors with single HfO_2 or La_2O_3 layer are fabricated as references.

Figure 3.12 shows the *CV* characteristics of the stacked MOS capacitors. *CV* curves HfO_2/IL and La_2O_3/IL capacitors are also shown for comparison. Capacitors with La_2O_3 on IL regardless of the thickness showed negative V_{FB}, which corresponds to that of La_2O_3/IL capacitor. On the contrary, capacitors with HfO_2 on IL showed positive V_{FB}, which correspond to HfO_2/IL capacitor. Therefore, it is clear that the main reason of V_{FB} shift exists at the interface of high-k/IL and the dipole difference at W/high-k can be considered as equal. As the thickness of HfO_2 and La_2O_3 has little dependence on the shift of V_{FB}, fixed charges or dipoles between the high-ks, interface at La_2O_3 and HfO_2, can be ignored.

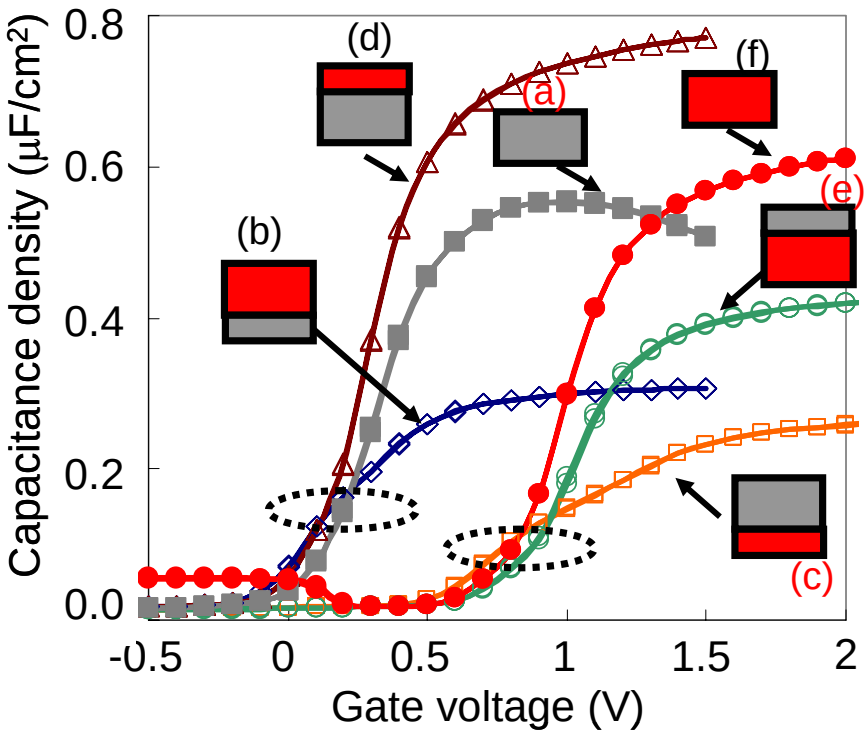


Fig 3.12 *C-V* characteristics of high-k stacked MOS capacitors with IL. The V_{FB} is determined by the high-k on IL.

3.4 Discussion

From the result of subsection 3.3.2, the *EWFs* of tungsten, which was calculated, are not valid, unless the effect of high-k/SiO_2 interface is known. But, it is clear that the V_{FB} shift is mainly determined by the high-k materials in contact to Si or SiO_2 IL.

There should be the presence of either fixed charges or dipoles, or both, which are not clarified yet (figure 3.13).

Next chapter, we would like to propose a possibility of controlling V_{FB} by changing the composition of high-k at SiO_2 interface.

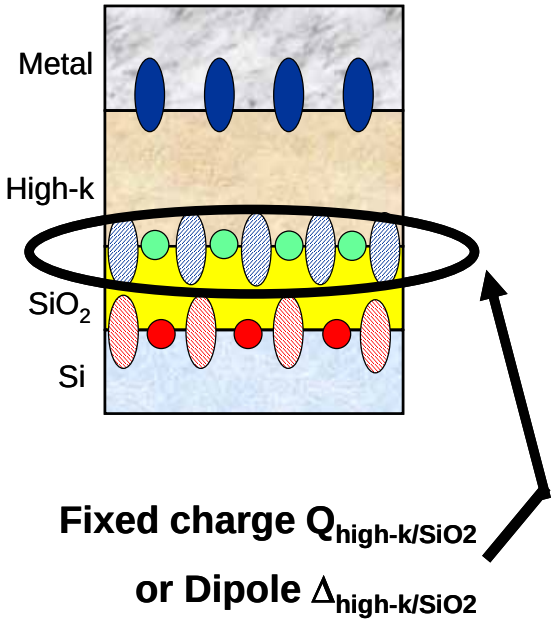


Fig 3.13 The presence of fixed charges or dipoles at the high-k/IL interfaces.

Chapter 4
V_{FB} Shift Dependence on Mixed High-k Incorporation at HfO_2/SiO_2 Interface

4.1 Introduction

In this chapter, the V_{FB} shift depending on the amount of La_2O_3 at the high-k/SiO_2 interface is investigated. From the result (Fig 3.12) that even 1 nm of La_2O_3 at high-k/SiO_2 interface can negatively shift the V_{FB}, the amount of the incorporated La_2O_3 to realize controllability of V_{FB} should be less than 1 nm.

To obtain precise controllability of amount of insertion high-k films at the HfO_2/IL interfaces, we employed co-evaporation of HfO_2 and La_2O_3 or Sc_2O_3 with different concentration as shown in figure 4.1.

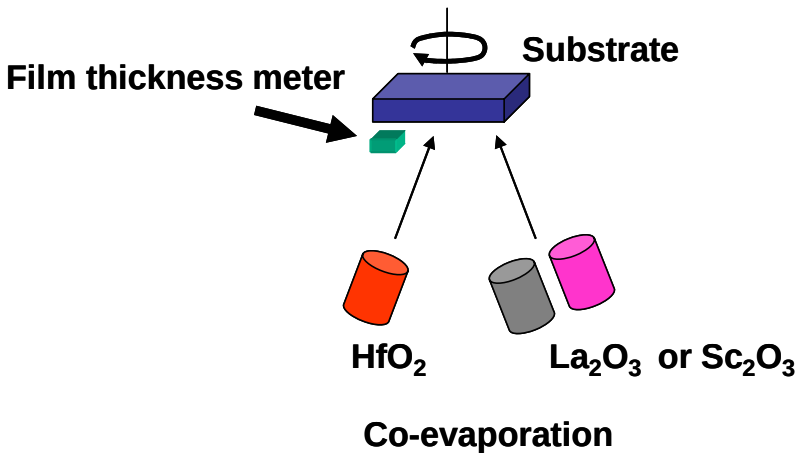


Fig 4.1 Schematic illustration of co-evaporate HfO_2 and La_2O_3 or Sc_2O_3

4.2 V_{FB} Shift Dependence on High-k Incorporation at HfO_2/SiO_2 Interface

4.2.1 V_{FB} Controlled by La_2O_3 Incorporation into HfO_2

We employed co-evaporation of HfO_2 and La_2O_3 with different concentration, those are 20, 50 and 80 %. The thickness of the mixed high-k layers was set to 1 nm. HfO_2 with 5 nm thickness was capped on the mixed high-k. The schematic illustrations of the fabricated capacitors are shown in figure 4.2.

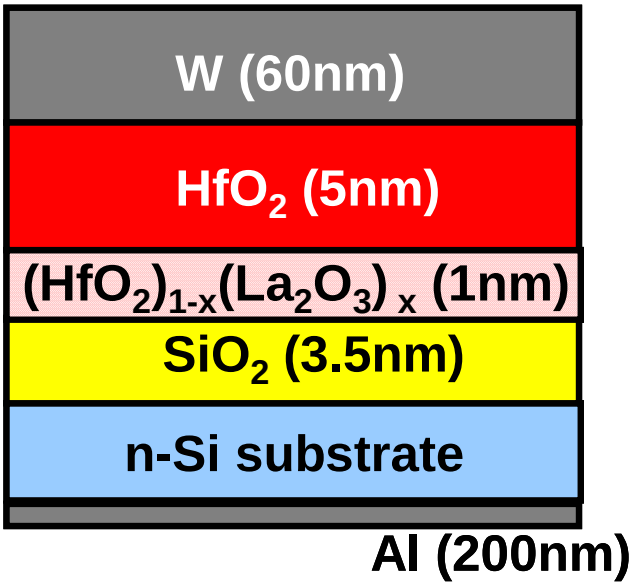


Fig 4.2 Schematic illustration of fabricated MOS capacitor with co-evaporation La_2O_3 and HfO_2 into HfO_2/SiO_2 interface

The *C-V* characteristics of the mixed high-k stack capacitors together with those of the references with La_2O_3 and HfO_2 capacitors are shown in figure 4.3. With the La_2O_3 concentration of 80%, the V_{FB} of *C-V* curves showed almost identical value for the La_2O_3 reference, where that of 20 % showed in between of those of HfO_2 and La_2O_3 references. With 50 % of La_2O_3 incorporation, the V_{FB} was slightly positive to the La_2O_3 reference. Also from these results, it is noted that the *EWF* of the gate metal is mainly dominated by the high-k/IL interface, not at the Metal/high-k interface. By plotting the V_{FB} on La_2O_3 concentration, as is shown in figure 4.4, we obtain a monotonic relation between concentration and V_{FB}. It can be concluded that V_{FB} can be effectively controlled by changing the concentration of the mixed high-k at the high-k/IL interface.

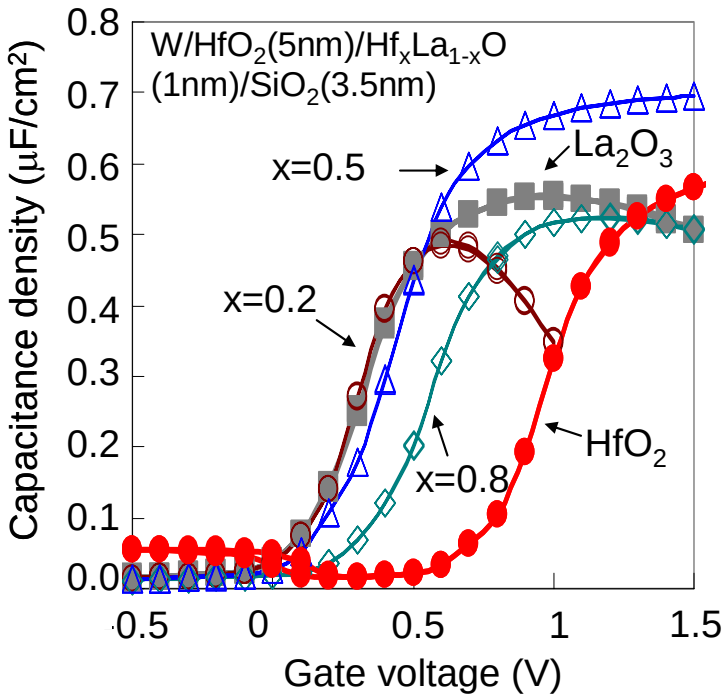


Fig 4.3 *C-V* curves of $W/HfO_2/(HfO_2)_{1-x}(La_2O_3)_x/SiO_2$ structure

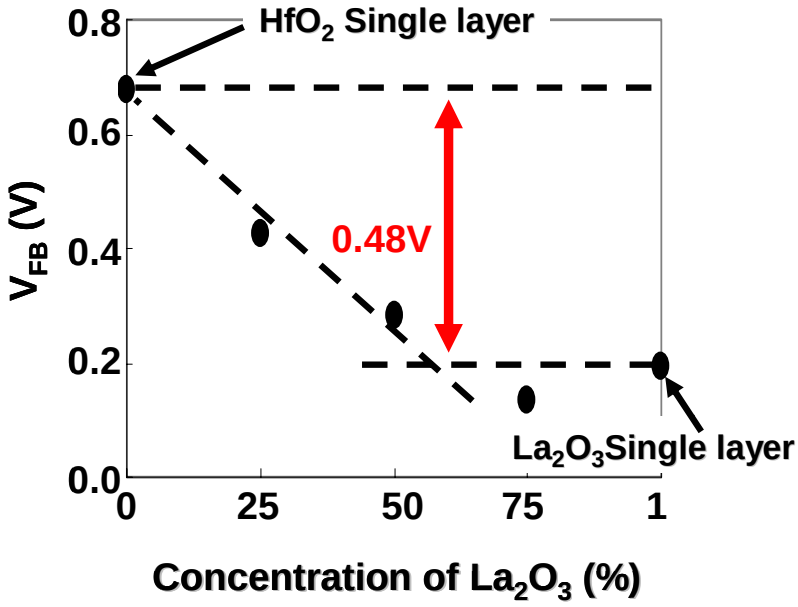


Fig 4.4 V_{FB} shift depending on incorporation of La_2O_3 at HfO_2/SiO_2 interface

4.2.2 V_{FB} Controlled by Sc_2O_3 Incorporation into HfO_2

The same experiments were carried out using Sc_2O_3 and HfO_2. In this case, the thickness of Sc_2O_3-HfO_2 mixed high-k and HfO_2 capping layer were set to 1 nm and 5 nm, respectively. The structure is depicted in figure 4.5. The concentrations of Sc_2O_3 were set to 33, 50 and 67%.

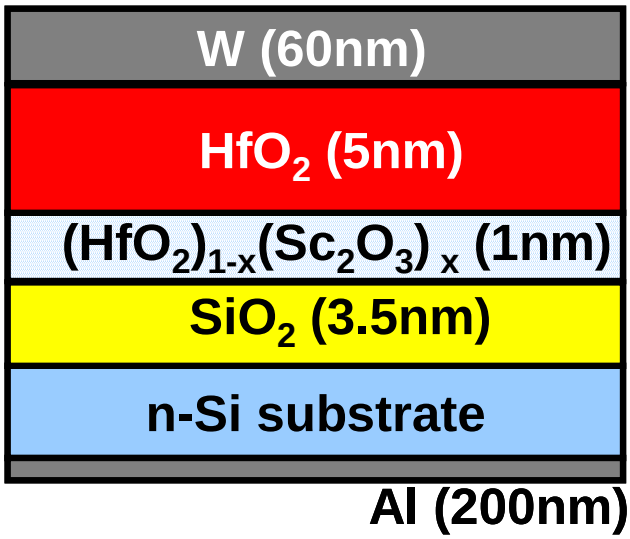


Fig 4.5 Schematic illustration of fabricated MOS capacitors incorporating Sc_2O_3 into HfO_2/SiO_2 interface

Figure 4.6 shows the *C-V* curves of the Sc_2O_3 incorporated HfO_2 capacitors. Also Sc_2O_3 and HfO_2 references are shown. Negative shifts of V_{FB} with increase in the concentration of Sc_2O_3 were obtained. The relation between the concentration and V_{FB} is shown in Figure 4.7. From this figure, the V_{FB} control range of 0.15 V was achieved using Sc_2O_3 incorporation into HfO_2. This value is smaller than that of La_2O_3, which can be expected from Sc_2O_3 single layer capacitor. Therefore, Sc_2O_3 and La_2O_3 incorporation technique is useful as fine and coarse tuning of V_{FB}, respectively.

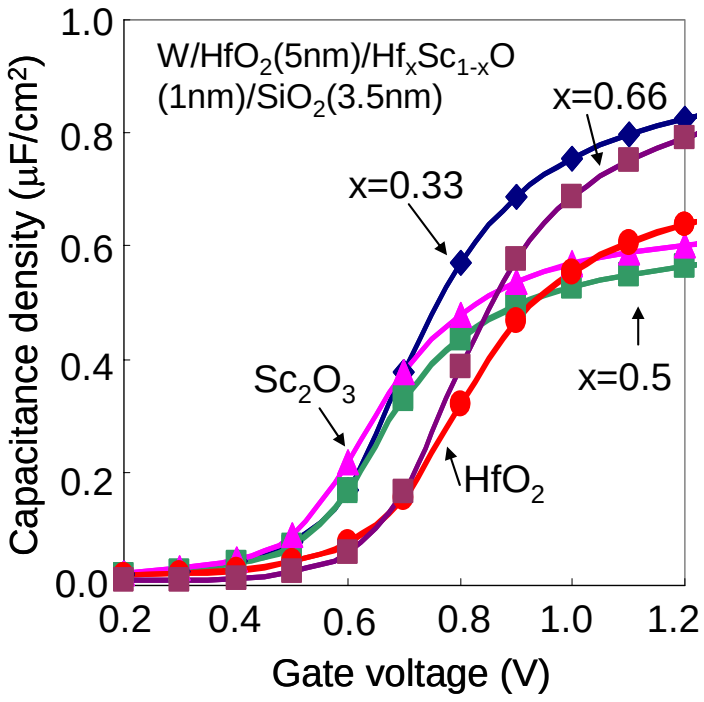


Fig 4.6 *C-V* curves of $W/HfO_2/(HfO_2)_{1-x}(Sc_2O_3)_x/SiO_2$ structure

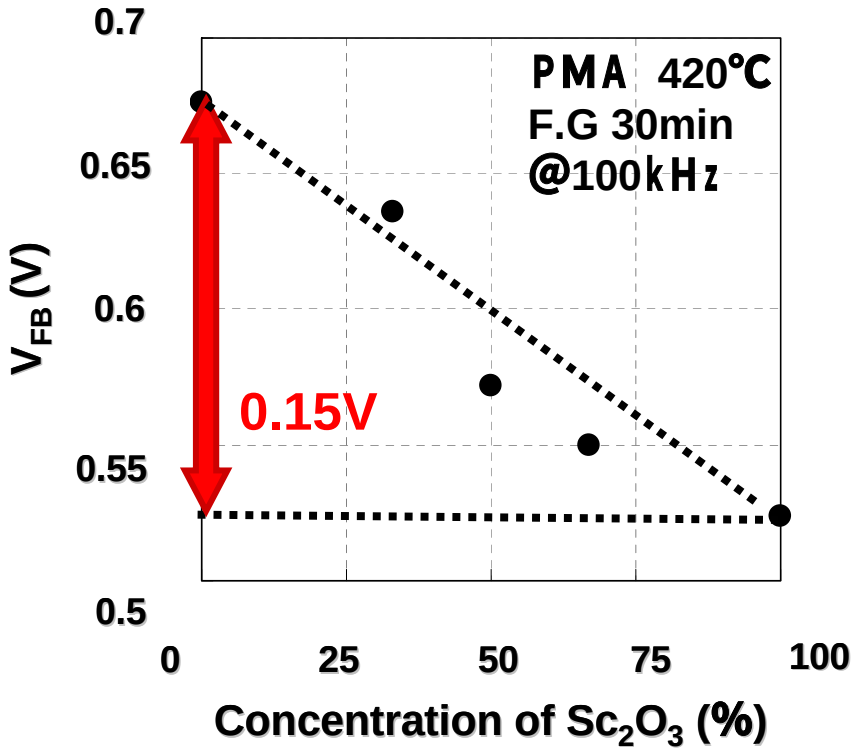


Fig 4.7 V_{FB} shift depending on incorporation of Sc_2O_3 at HfO_2/SiO_2 interface

4.3 Electrical Characteristics of Mixing La_2O_3 and HfO_2 MOSFETs

4.3.1 *I-V* Characteristics

In this subsection, we will report characteristics HfO_2/HfLaOx/Si stacked dielectrics transistor with 500°C PMA in F.G ambient for 30min. Figure 4.8 show I_d-V_d characteristics of HfO_2/HfLaOx/Si stacked structure ((a) La_2O_3 66% and (b) La_2O_3 33%)transistor, respectively. The gate length and the gate width of this transistor were 2.5 μm and 50μm, respectively. In I_d-V_d characteristics, the applied gate voltage were from 0V to 1.0V with 0.2 V step. As this figure, we found that operation of the transistor.

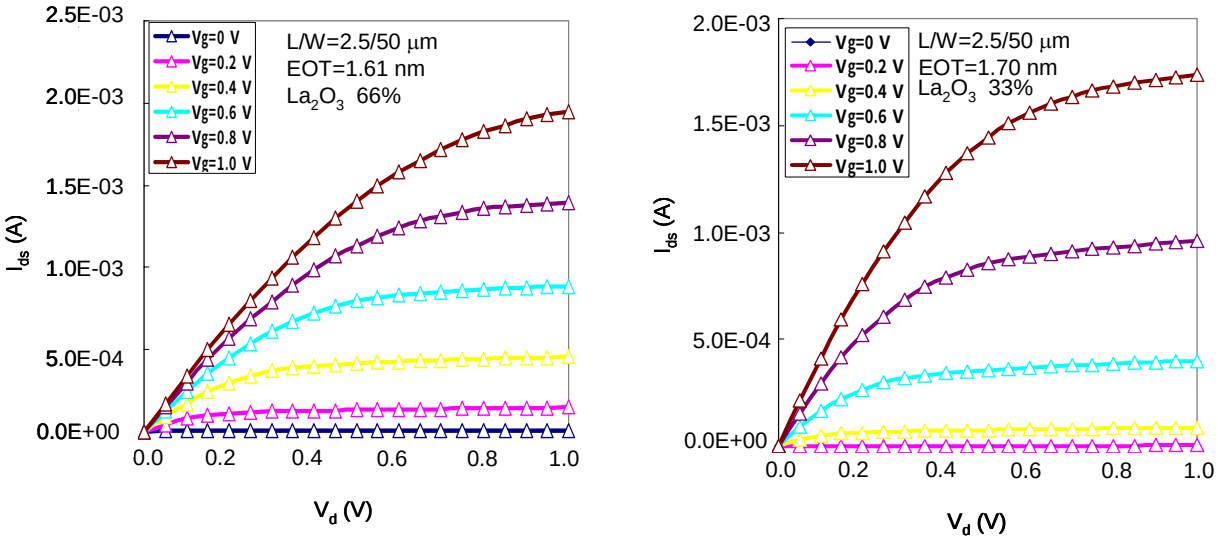


Fig 4.8 *Id-Vd* characteristics of incorporation of La_2O_3 at HfO_2/Si interface (a) La_2O_3 66% (b) La_2O_3 33%

Figure 4.9 shows I_d-V_g characteristics at V_d =50mV. S-factor and threshold voltage dependent on La_2O_3 insertion rates were shown in figure 4.10 and 4.11. Negative shifts of V_{th} with increase in the concentration of La_2O_3 were obtained.

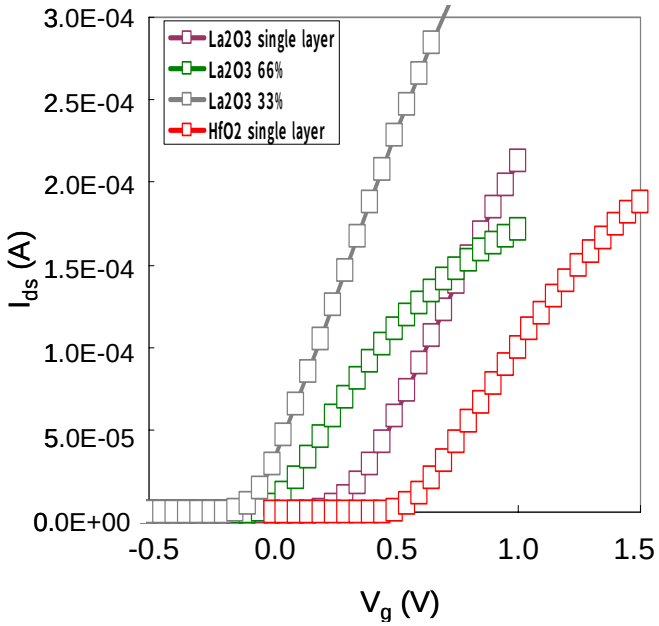


Fig 4.9 *Id-Vg* characteristics of incorporation of La_2O_3 at HfO_2/Si interface

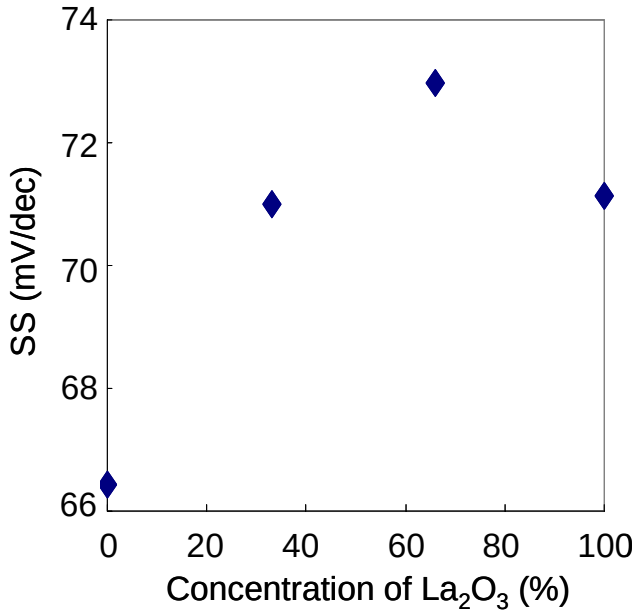


Fig 4.10 S-factor dependent on La_2O_3 insertion rate

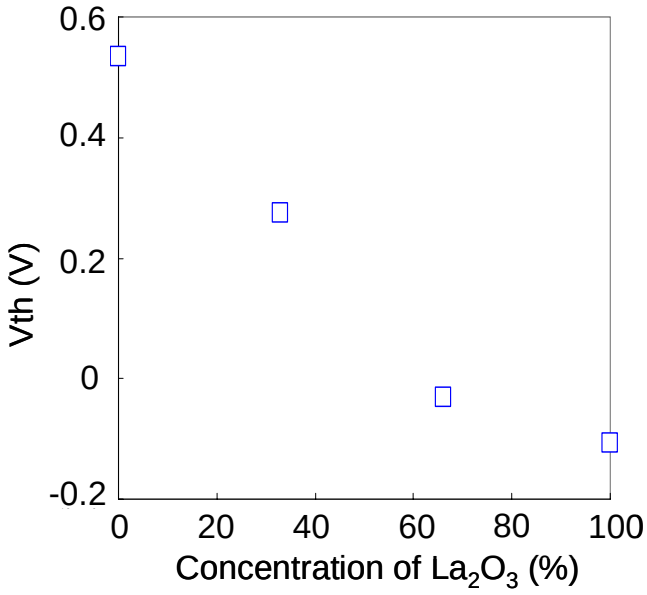


Fig 4.11 Threshold voltage dependent on La_2O_3 insertion rate

4.3.2 Characteristics of Interface States

The interface states density was characterized by charge pumping method. Figure 4.12 shows the charge pumping current (*Icp*) applying the square wave form pulse as a function of pulse base voltage. Figure 4.13 shows the insertion of La_2O_3 dependent on charge trapped density (D_{it}). Increasing the concentration of La_2O_3, D_{it} was increased. Soaring of S-factor, as shown in figure 4.10, could be caused of D_{it} soaring for insertion of La atomic density.

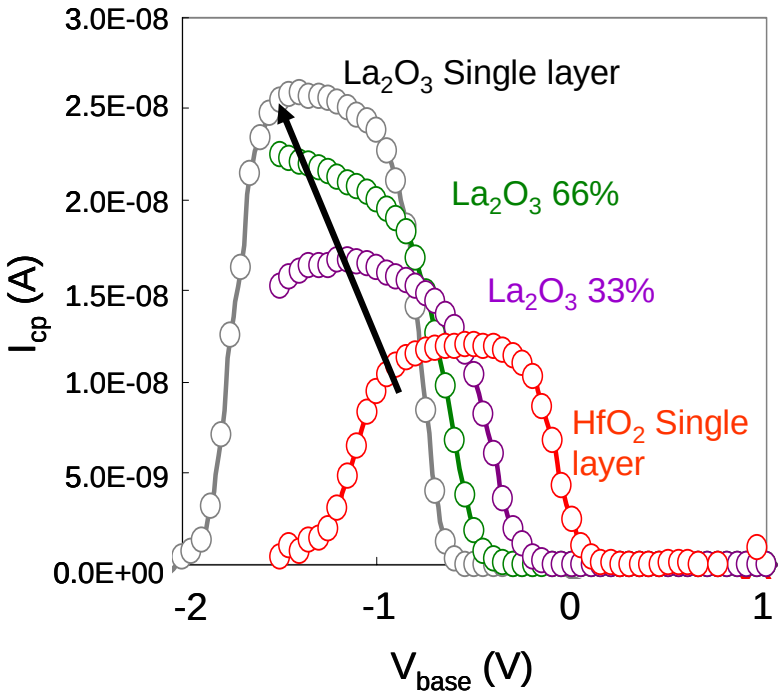


Fig 4.12 Charge pumping currents dependent on La_2O_3 insertion.

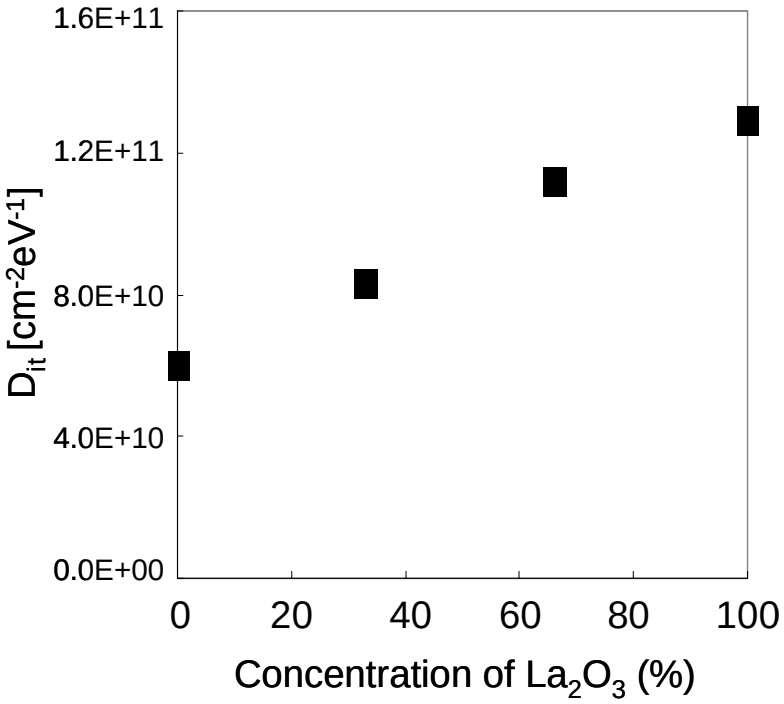


Fig 4.13 Charge pumping currents dependent on La_2O_3 insertion.

4.4 Discussion

Figure 4.14 shows a Model of V_{FB} shift of compound high-k $HfLaO_x/SiO_2$ interface. In the case of HfO_2 and La_2O_3 compound films, These results indicated that, diffusion of La_2O_3 to SiO_2 interface could be occured when the samples were annealed at high temperature 420 ^oC and finally La rich layers could be formed as a result of La pile-up at the bottom of $HfLaO_x$. On the contrary, in the case of HfO_2 and Sc_2O_3 compound films, The diffusion of Sc_2O_3 to SiO_2 interface could not be occurred when annealed at high temperature as shown in figure 4.15.

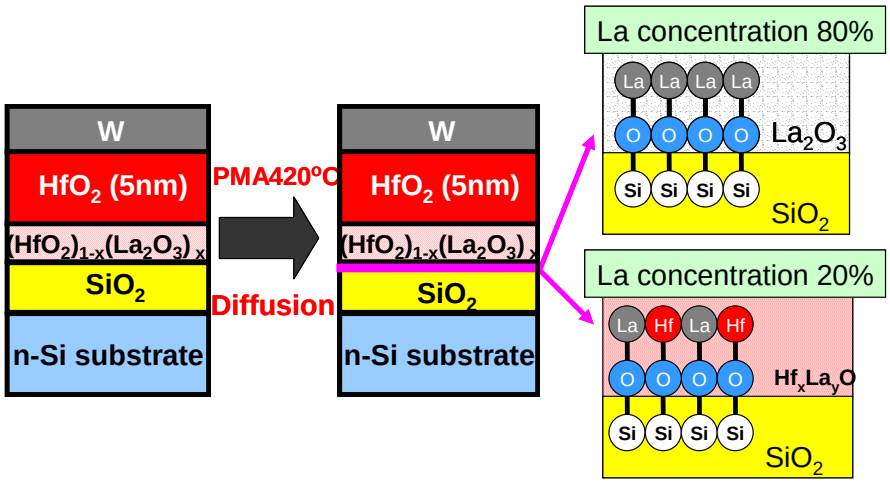


Fig 4.14 Model of La atoms which were separated from $HfLaO_x$ layer

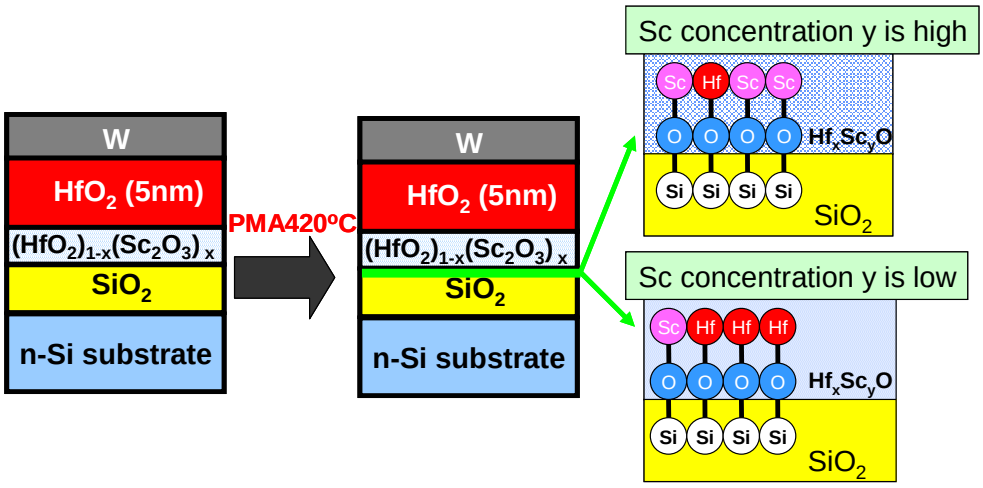


Fig 4.15 Model of La atoms which were separated from $HfScO_x$ layer

The V_{FB} is dependent on concentration of La_2O_3 or Sc_2O_3, and the large concentration results in large negative V_{FB} shift up to the V_{FB} obtained for the capacitors using La_2O_3/SiO_2 or Sc_2O_3/SiO_2. Coarse and fine tuning of V_{FB} for HfO_2 gate dielectrics were successfully observed by La_2O_3 and Sc_2O_3 incorporation, respectively as shown in figure 4.16.

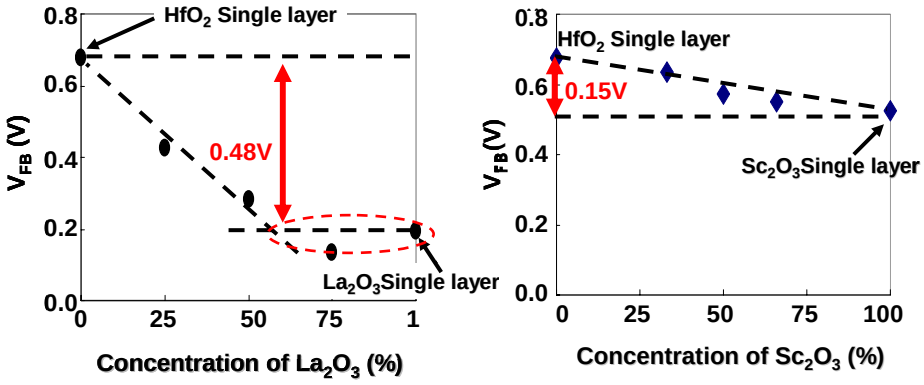


Fig 4.16 Coarse and fine tuning of V_{FB} for HfO_2 gate dielectrics.

Chapter 5

Origin of V_{FB} Shift in Ultra-Thin La_2O_3 for HfO_2 Gate Dielectrics

5.1 Introduction

As discussed above chapter 3 and 4, the high-k at IL interface is dominant for V_{FB}. Next, in order to investigate the mechanism of V_{FB} shift in detail, the V_{FB} shift of HfO_2/IL MOS capacitors with ultra thin La_2O_3 insertion, less than one mono layer (ML), at HfO_2/IL interface is examined as shown in figure 5.1. HfO_2 with thickness of 4 nm was deposited, then 8 nm tungsten gate electrodes were formed in order to avoid any contamination, on all capacitors at the same time.

For Hard X-ray Photoemission Spectroscopy (HXPES) measurement, spectra were obtained using high-energy x-ray radiation (hν=7940 eV) at Spring 8 with BL47XU [10] equipped with high-resolution GAMMADATA SCIENTA R4000 spectrometer. In order to eliminate any changing effect during the photoelectron counting, surface tungsten electrode were connected to the substrate ground level, thus the Fermi level of metal coincides to that of Si substrate as shown in figure5.2. Therefore, the band vending profile can be obtained by directly measuring the core spectra of the Si substrate surface [11]. The measured spectra in this work were Si_{1s},$La3d_{5/2}$,$Hf3d_{5/2}$.

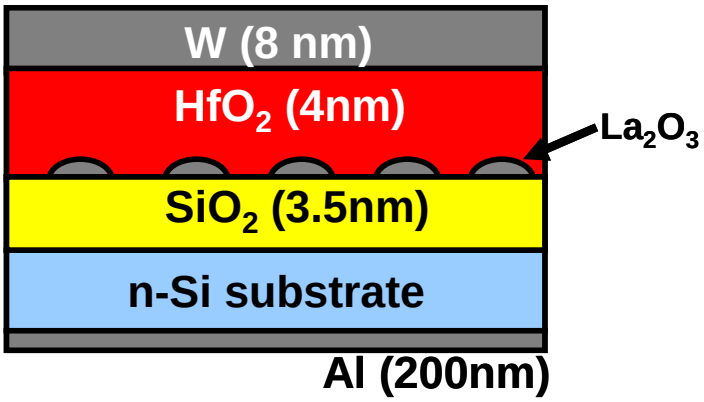


Fig 5.1 Schematic illustration of fabricated W/HfO_2/SiO_2/n-Si with ultra thin La_2O_3 insertion, less than one mono layer at HfO_2/IL interface.

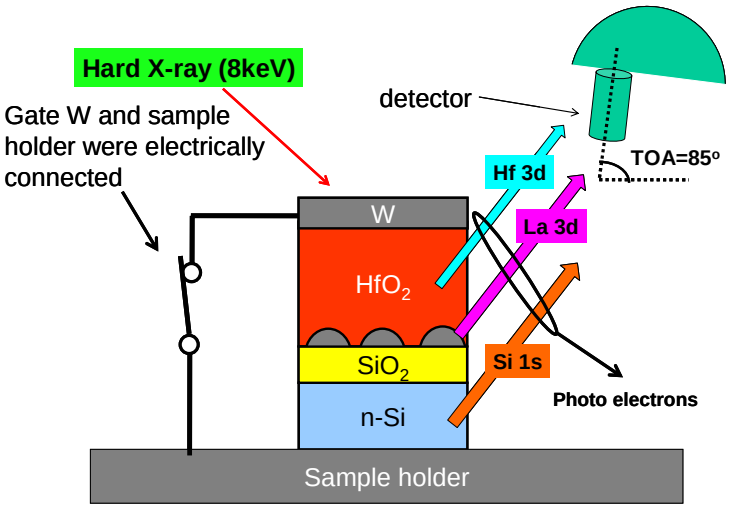


Fig 5.2 Schematic illustration of measurement through 8 nm thick gate electrode HX-PES

5.2 Characterization of W/HfO_2/SiO_2/Si with Ultra-Thin La_2O_3 Insertion Structure

Figure 5.2 shows the TEM of a sample, which has the largest amount of inserted La_2O_3. The thickness of the observed interlayer between HfO_2 and SiO_2 can be measured to be 1.3 nm.

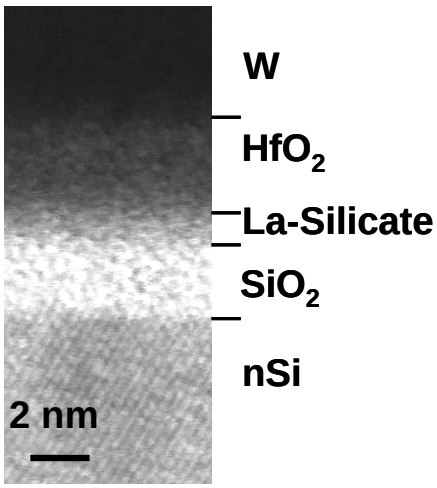


Fig 5.2 Cross sectional TEM image of W/HfO_2/La_2O_3/SiO_2/n-Si stack after annealing 420°C.

From Si_{1s} spectrum, shown in figure 5.3, this interlayer can be identified to be La-silicate, as the electronegativity of La (χ=1.1) is smaller than that of Si (χ=1.90), the peak appeared around 1843.23 eV smaller than that of SiO_2 (1844.92 eV) can be considered as Si-O-La bonding. If a volume expansion of 40% due to the reaction of La_2O_3 and SiO_2 is taken into account, the amount of inserted La_2O_3 can be calculated to be 1.0 nm.

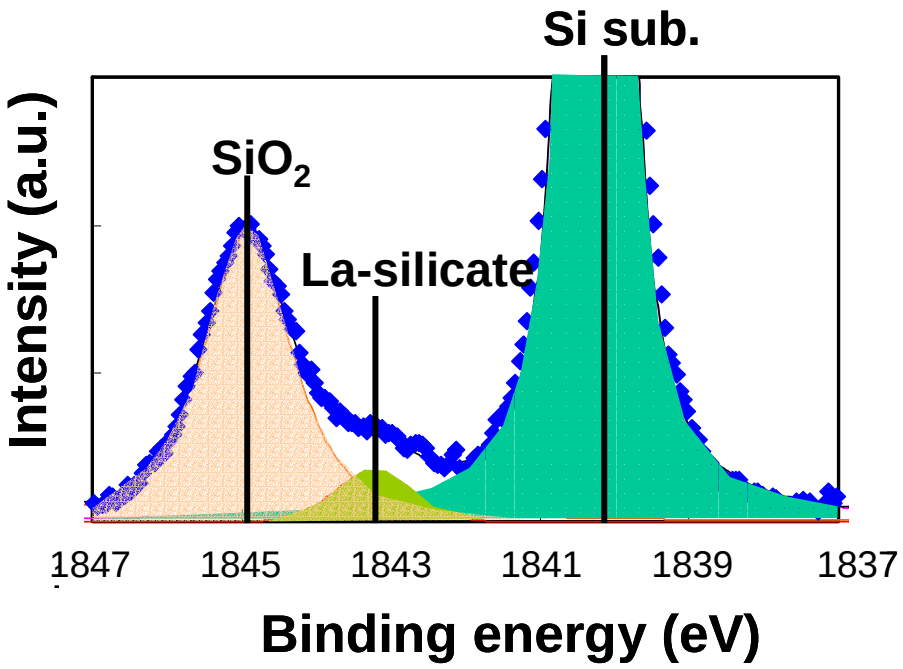


Fig 5.3 After annealing, the inserted La_2O_3 reacts to from La-silicate layer, which can be identified by Si1s core spectrum.

Figure 5.4 (a) shows the *CV* characteristics of W/HfO_2/SiO_2/n-Si with various amount of La_2O_3 insertion at HfO_2/SiO_2 interface . By increasing the amount of La_2O_3, from 0.11 to 0.27 nm, the V_{FB} showed negative shift toward to V_{FB} of La_2O_3/SiO_2 capacitors. The V_{FB} control range of 0.52 V was achieved using La_2O_3 incorporation into HfO_2 as shown in figure 5.4 (b). The thickness of 1.0nm La_2O_3 was measured by TEM image and the others are estimated by $La3d_{5/2}$ counts.

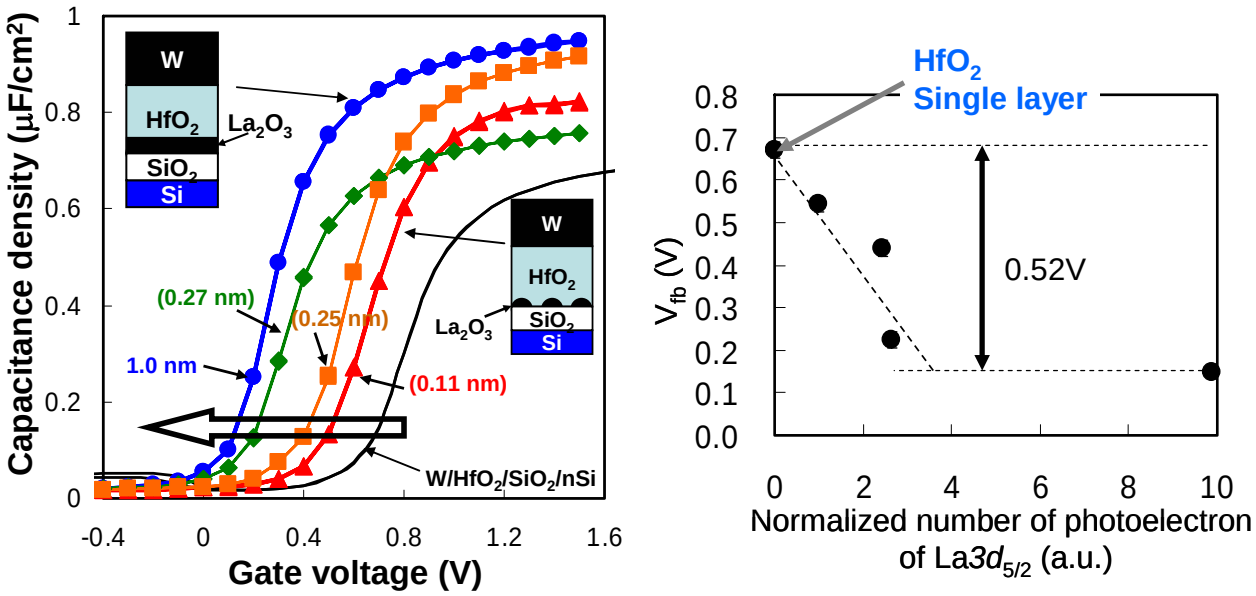


Fig 5.4 (a) *CV* curves of W/HfO_2/SiO_2/n-Si capacitors with La_2O_3 insertion at HfO_2/SiO_2 interface. (b) V_{FB}-normalized number of photo electron of $La3d_{5/2}$ plots.

5.3 Band Bending Measurement By XPS

As the surface W layer is electrically connected to the sample substrate, band vending of Si substrate can be estimated by directly comparing the Si core level binding energy among the samples [12]. Figure 5.5 shows the set of Si1s binding energy the samples with different La_2O_3 thickness. By increasing the amount of La_2O_3 insertion, the peak shift towards higher binding energy. The difference between the smallest and 1.0 nm insertion can be measured to be 0.27 V. Note that negligible peak shifts were observed $Hf3d_{5/2}$ and $La3d_{5/2}$ spectra.

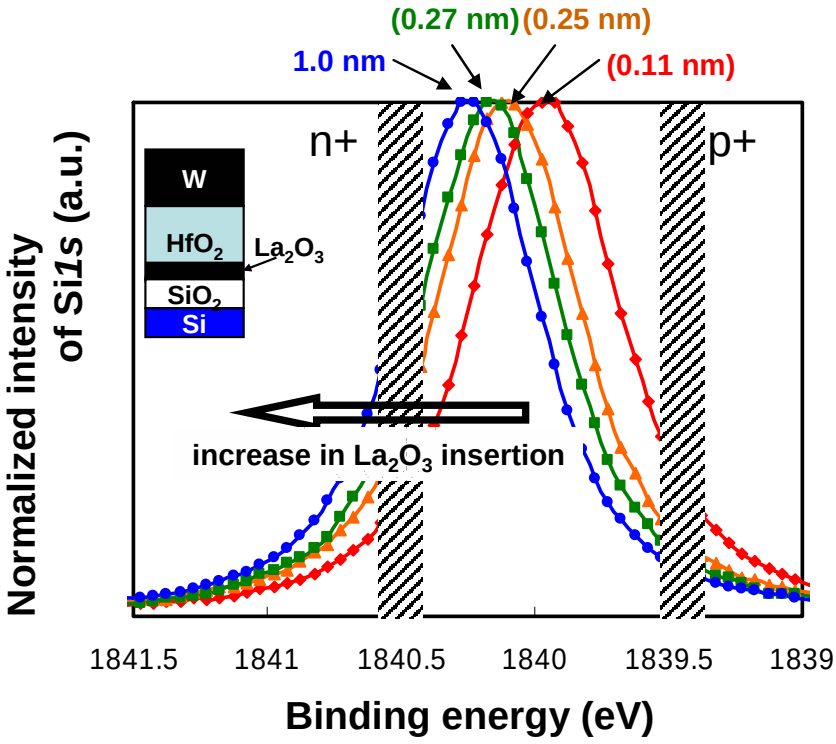


Fig 5.5 XPS measurement of Si*1s* binding energy for $W/HfO_2/SiO_2/n\text{-}Si$ stack with La_2O_3 insertion.

In figure 5.6, the peak shift of Si*1s* binding energy is plotted against the number of photoelectrons from La3d$_{5/2}$. From this figure, the thickness of the smallest La_2O_3 insertion can be estimated to be 0.1 nm, which would take the form of islands rather than a continuous layer. By extrapolation, the substrate Si1s peak position without any La_2O_3 insertion can be estimated to be located at 1839.84 eV. Therefore, the overall contribution by La_2O_3 insertion to the peak shift can be estimated to be 0.41 eV. This peak shift might be obtained when the insertion thickness is enough to form a La-silicate monolayer. From this result, at least 0.36 nm is required to form a La-silicate monolayer.

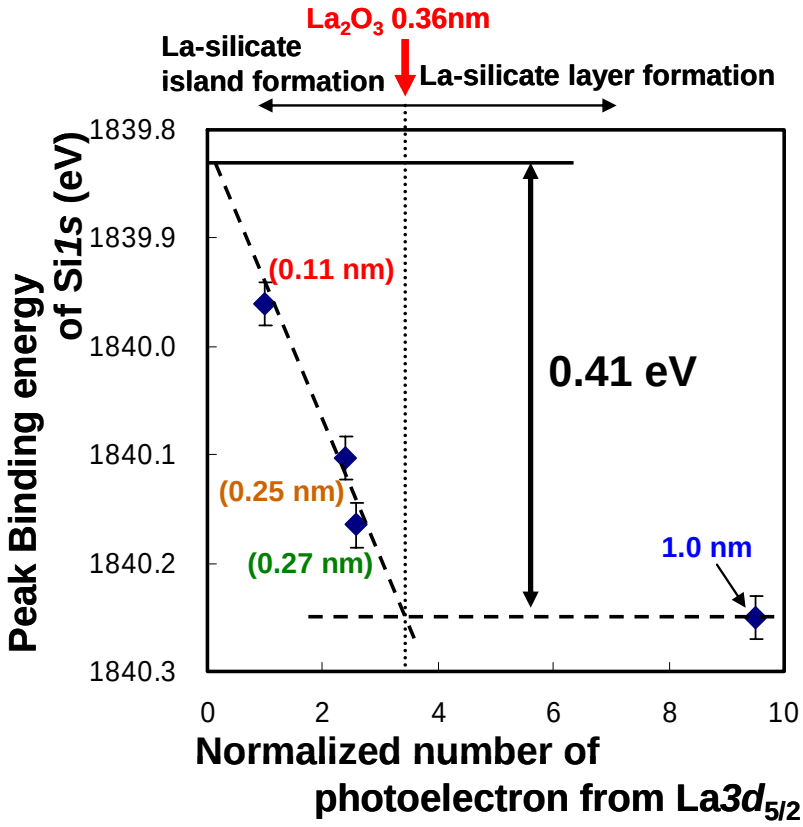
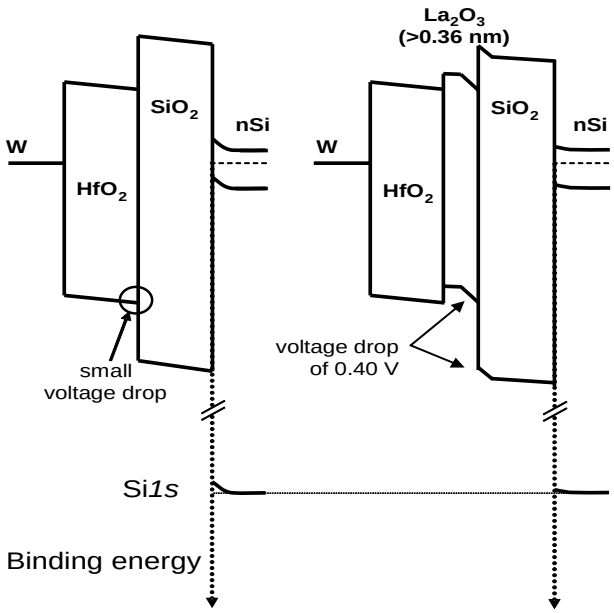


Fig 5.6 Peak energies of Si*1s* are plotted against the normalized number of photoelectron from La3d$_{5/2}$.

From the *CV* measurements and XPS measurement obtained above, band diagrams of $W/HfO_2/SiO_2/n\text{-}Si$ capacitor with and without La_2O_3 layer can be drown as shown in figure 5.7. As the peak binding energy of $Hf3d_{5/2}$ and $La3d_{5/2}$ were almost constant, a voltage shift must be located at La_2O_3/SiO_2 interface, which bends down the Si band. If the amount of La_2O_3 is not enough to form monolayer, these two diagrams would be effectively merged depending on the amount of La_2O_3. As the thickness of SiO_2 layer is 3.5 nm in this work, the voltage drop across this SiO_2 layer is as small as 0.01 V. Therefore, the relative voltage shift difference at HfO_2/SiO_2 and La_2O_3/SiO_2 can be estimated as 0.40 V.



(a) (b)

Fig 5.7 Energy band diagram of $W/HfO_2/SiO_2/n\text{-}Si$ capacitor (a) without La_2O_3 insertion (b) with La_2O_3 insertion.

5.4 Summary

In this chapter, we have confirmed the V_{FB} shift of W/HfO_2/SiO_2/n-Si with La_2O_3 insertion using hard X-ray photoelectron spectroscopy. By measuring Si1s core spectra, the surface potential of Si substrate increases along with the amount of inserted La_2O_3. A voltage drop difference of HfO_2 and La_2O_3 at SiO_2 interface can be estimated as 0.40 V.

Chapter 6
Proposition of Dipole Moment Model Using Electronegativity

6.1 Modeling of The Dipole Moment

6.1 Modeling of The Dipole Moment

The magnitude of interfacial dipole moment (μ) at high-k/IL or high-k/Si can be considered as a result of charge transfer across the chemical bondings, therefore, electronegativity difference (Δχ) between each atom and oxygen (χ =3.44) and its bonding length (*d*) can be used to model the VFB shift. The value of χ, Δχ, d and μ are tabulated in table 6.1 [13]. To consider the effect of SiO2, SiO molecule is assumed and its χ was calculated by arithmetic mean based on the work of R.T Sanderson [14].

Table 6.1 Electronegativity difference (Δχ) between each atom and oxygen. SiO molecule is estimated by arithmetic mean. The relative magnitude of interface dipole moment (μ) can be estimated by Δχ *d*.

	χ	Δχ	d (nm)	μ= Δχd
La	1.10	2.34	0.258	0.604
Hf	1.30	2.14	0.196	0.419
Si	1.90	1.54	0.160	0.246
(SiO)	(2.56)	0.88	(0.160)	0.141

The bonding configuration of each interface examined in this work is shown in figure 6.1. In case of (a) SiO_2/Si, the dipole moment of $\mu_{Si\text{-}O}$ approximately cancels out. In case of (b) La_2O_3/Si and (c) HfO_2/Si without IL, the valency difference should be taken into account. As the valencies of La and Hf are 3 and 4, respectively, the overall dipoles moment can be calculated as $2/3\mu_{La\text{-}O}\text{-}1/2\mu_{Si\text{-}O}$ and $1/2\mu_{Hf\text{-}O}\text{-}1/2\mu_{La\text{-}O}$, respectively. On the other hand, in the case of (d) La_2O_3 and (e) HfO_2 on SiO_2 substrate, the dipole moments inside SiO_2 can be neglected as the case of SiO_2/Si. However, when considering the Si-O bonding at high-k/IL interface, another dipole moment of Dm

should be incorporated due to the presence of O in SiO_2 layer, which acts as a second nearest neighbors. Therefore, $\Delta\mu$ need to be added to estimate the overall dipole moments. $\Delta\mu$ can be roughly estimated by the dipole moment difference between $\mu_{Si\text{-}O}$ and $\mu_{SiO\text{-}O}$, which yields a value of 0.105. As the dipole difference of (d) and (e) has been experimentally deduced to be 0.36 eV as shown in chapter 3 (table 3.3), V_{FB} of all structures can be calculated with an additional information of ϕ_{ms}. Table 6.2 shows the dipole moment of each structure and the calculated V_{FB}, in which ϕ_{ms}=0.4 eV is assumed. Note that fixed charges are not presented in the estimated V_{FB}. The estimated V_{FB} using proposed model matches well to the experimentally obtained V_{FB}.

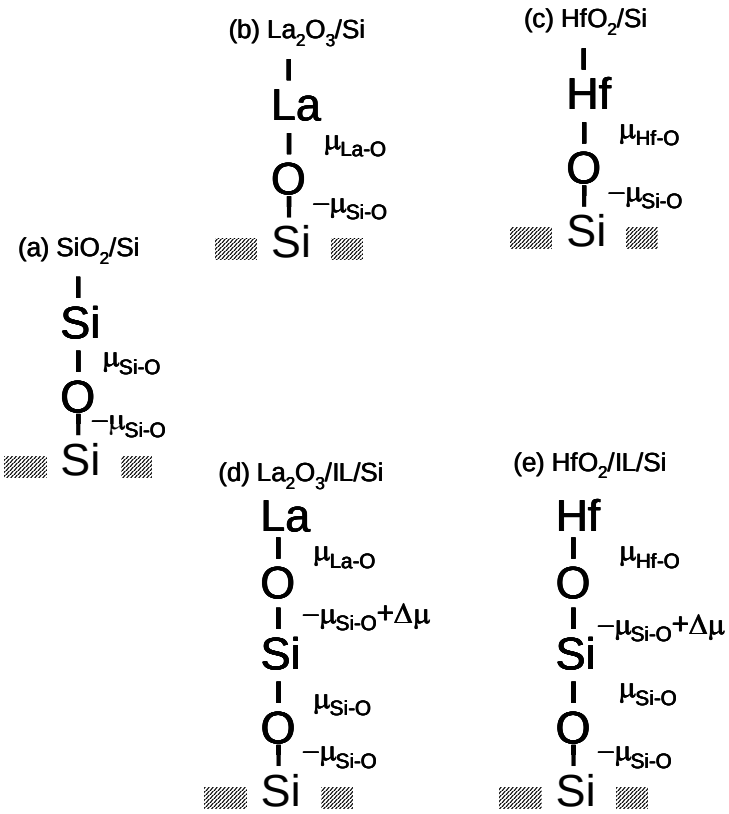


Figure 6.1 Schematic illustration of atoms at the interface with relative magnitude of dipoles at each bonding. (a) SiO_2/Si (b) La_2O_3/Si (c) HfO_2/Si (d) La_2O_3/IL/Si (e) HfO_2/IL/Si

Table 6.2 Overall dipole moment calculation. By using the dipole difference of 0.36 eV in structure (d) and (e) , V_{FB} of all structures due to dipole can be calculated.

	Calculation	μ_{all}	V_{FB} (V)
(a) SiO_2/Si	$1/2\mu_{Si-O}$-$1/2\mu_{Si-O}$	0	0.40
(b) La_2O_3/Si	$2/3\mu_{La-O}$-$1/2\mu_{Si-O}$	0.279	-0.12
(c) HfO_2/Si	$1/2\mu_{Hf-O}$-$1/2\mu_{Si-O}$	0.087	0.24
(d) La_2O_3/SiO_2	$2/3\mu_{La-O}$-$1/2\mu_{Si-O}$+$\Delta\mu$	0.169	0.08
(e) HfO_2/SiO_2	$1/2\mu_{Hf-O}$-$1/2\mu_{Si-O}$+$\Delta\mu$	-0.023	0.44

Chapter 7

Conclusion

7.1 Results of This Study
7.2 For Future Works

7.1 Results of This Study

In this thesis, we investigated the main factor of the V_{FB} shift in the W/high-k/Si or W/high-k/IL/Si structure. In this chapter, the studies referred to in this thesis are summarized.

V_{FB} Shift in Double Layer Dielectric Films (Chapter 3)

MOS capacitors with stacked high-k using La_2O_3/HfO_2/IL or HfO_2/La_2O_3/Si structure have revealed that V_{FB} shift is mainly determined by the high-k materials in contact to Si or SiO_2 IL.

V_{FB} Shift Dependence on Mixed High-k Incorporation at HfO_2/SiO_2 Interface (chapter4)

The V_{FB} is dependent on concentration of La_2O_3 or Sc_2O_3, and the large concentration results in large negative V_{FB} shift up to the V_{FB} obtained for the capacitors using La_2O_3/SiO_2 or Sc_2O_3/SiO_2. Coarse and fine tuning of V_{FB} for HfO_2 gate dielectrics were successfully observed by La_2O_3 and Sc_2O_3 incorporation.

Origin of V_{FB} Shift in Ultra-Thin La_2O_3 for HfO_2 Gate Dielectrics (chapter 5)

By measuring Si1s core spectra, the surface potential of Si substrate increases along with the amount of inserted La_2O_3. A voltage drop difference of HfO_2 and La_2O_3 at SiO_2 interface can be estimated as 0.40 V.

Proposition of Dipole Moment Model Using Electronegativity (chapter 6)

We evaluated the dipole moment using electronegativity difference. The estimated V_{FB} using proposed model matches well to the experimentally obtained V_{FB}.

7.2 Subject to the Future

Hf-based oxides have been the promising candidates for next generation gate dielectric. We proposed a new method to solve the V_{th} tuning by incorporating different kind materials at HfO_2/IL or HfO_2/Si interfaces. However, there are many problems to use HfO_2 for sub-1 nm MOSFET such as increasing EOT by growth of IL or V_{th} increasing by Fermi-level-pinning in case of high temperature (~1000^{o}C) annealing[15][16]. There should pay attention to it next investigation object.

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Yokohama Japan

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