Master Thesis

A Study on Process Optimization for High Performance La_2O_3-MOS devices

Presented by:
05M36358 Kiichi Tachi

Department of Electronics and Applied Physics
Interdisciplinary Graduate School of Science and Engineering
Tokyo Institute of Technology

Supervisor:
Professor Hiroshi Iwai

February 2007

To my father and mother

CONTENTS

1

INTRODUCTION

1.1 Background of This study
1.2 Limits of SiO_2
1.3 Requirements of high-k materials
1.4 Properties of La_2O_3
1.5 Purpose of This Study

1.1 BACKGROUND OF THIS STUDY

In recent years, our lives are becoming affluent with the global promotion of Information Technology (IT) as represented by computers, internets and cell-phones. As it is now, these are fundamental part of everyday life. These information equipments are realized by astonishing progress in silicon LSI (Large-Scale Integration) technology. The performance of silicon LSI depends on the capability of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) which is core part of LSI systems. In order to obtain high performance devises, it is necessary to miniaturize the MOSFET with the scaling method. The scaling method is based on reducing the device dimension in both lateral and vertical. The consensus scenario of how the device parameters are scaled for the next technology is provided in the International Technology Roadmap for Semiconductor (ITRS). A simple description of miniaturization with scaling factor of κ is shown in Figure 1.1 and Table 1.1. To gain κ times of the device performance, the physical device dimensions are reduced by κ times, while the electrical parameters are increased by κ times.

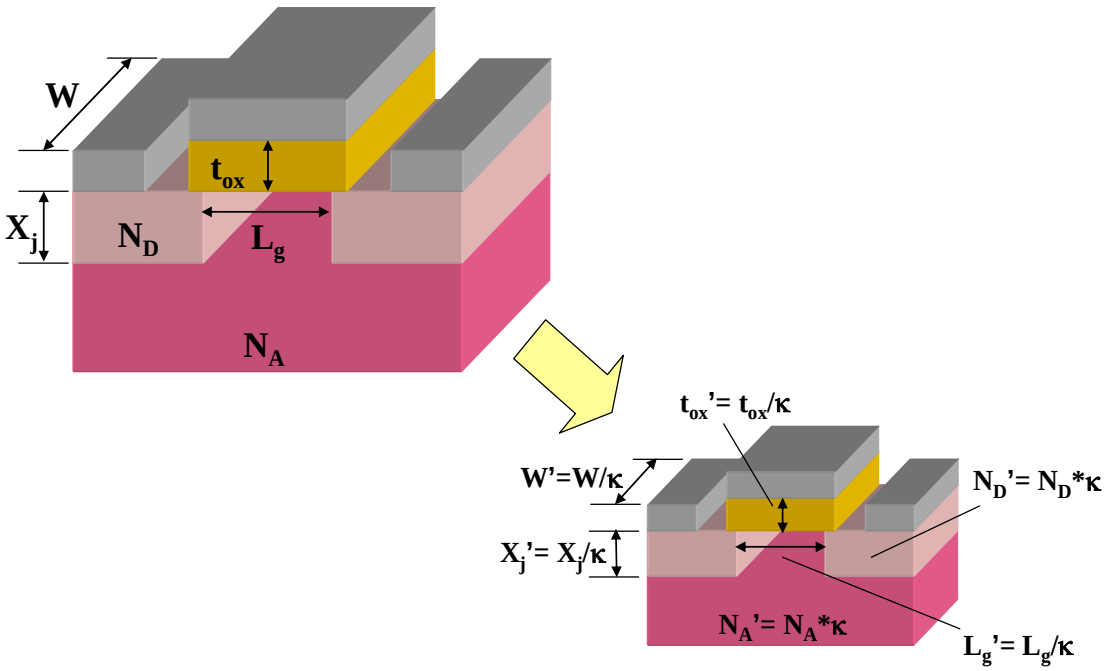


FIGURE 1.1 Scaling of MOSFET

TABLE 1.1 Scaling of MOSFET by the scaling factor κ [1].

Parameter	Inisial	Scaled
Channel Length	L	L/κ
Channel Width	W	W/κ
Total Device Area	A	A/κ^2
Gate Oxide Thickness	t_{ox}	t_{ox}/κ
Gate Capacitance	C_{ox}	C_{ox}*κ
Junction Depth	X_j	X_j/κ
Power Supply Voltage	V_{dd}	V_{dd}/κ
Threshold Voltage	V_{th}	V_{th}/κ
Doping Concentration	N_A	N_A*κ
	N_D	N_D*κ

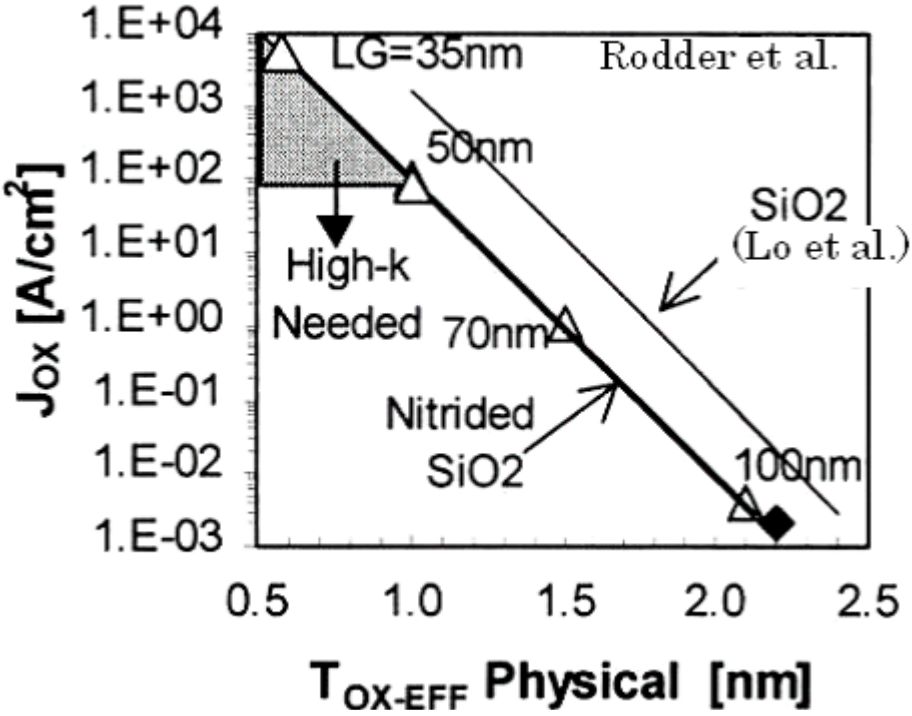
1.2 LIMITS OF SiO_2

As is well known, Silicon dioxide film (SiO_2) is the most common materials as gate insulator film. However, a big hurdle is confronted to miniaturize the element size as in the past with keeping high performance and high integration.

From ITRS 2006 up date (Table 1.2), Equivalent Oxide Thickness (EOT) will rise to the below 1nm level in near future [2]. On the other hand, the direct-tunneling leakage current is too increasing to be neglected as shown in Figure 1.2. Therefore, SiO_2 gate insulator film is to be replaced with an alternative material, which can be suppressed leakage current.

TABLE 1.2 ITRS 2006 up date

Year of Production	2005	2007	2010	2014	2018
Physical Gate Length (nm)	32	25	18	11	7
EOT (nm)	1.1	0.9	0.7	0.6	0.5
Gate Leakage Current Density (A/cm^2)	$5.20*10^2$	$9.30*10^2$	$1.90*10^3$	$9.09*10^3$	$2.40*10^4$
Power Supply Voltage (V)	1.1	1.1	1.0	0.9	0.7



FIFURE 1.2 Relations between gate leakage current and physical thickness of SiO_2 film.

1.3 REQUIREMENTS OF HIGH-*k* MATERIALS

To overcome this problem, high-k (high dielectric constant) materials have been attracted much attention. The key guidelines for selecting an alternative gate dielectric material are high dielectric constant, large band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability. Among them, high dielectric constant and large band gap are the minimum required characteristics to suppress the gate leakage current. The direct-tunneling leakage current (J_{DT}) flow through a gate insulator film is determined by the tunneling probability of carrier. The tunneling probability of carrier (D_{DT}) is shown in below equation where physical thickness of insulator (d), electron effective mass in the gate insulator film (m^*) and barrier height of insulator (ϕ_b).

$$J_{DT} \propto D_{DT} \propto \exp\left\{-\frac{4\pi d\left(2m^*\phi_b\right)^{\frac{1}{2}}}{h}\right\}$$

Relationship between physical thickness of SiO_2 (d_{EOT}) and physical thickness of high-k gate insulator (d) obtained by the same gate capacitance value (C) is shown in below equation where dielectric constant of SiO_2 (ε_{ox}) and high-k gate insulator ($\varepsilon_{high\text{-}k}$).

$$C = \frac{\varepsilon_{high-k}}{d} = \frac{\varepsilon_{ox}}{d_{EOT}}$$

$$d = \frac{\varepsilon_{ox}}{\varepsilon_{high-k}} d_{EOT}$$

Therefore, the gate leakage current can be suppressed by using high-k materials, which means that the physical thickness of high-k films can be thicken without changing EOT. In addition, the gate leakage current can also be suppressed by using large band gap materials.

The possible candidate of several metal oxides system for the use of gate dielectric

materials is shown in white spaces of Table 1.3.

TABLE 1.3 Candidate of metal oxides that has possibility to be used as high-k gate insulator.

●=Not a solid at 1000 K
○= Radioactive
①=Failed reaction 1: $Si + MO_x \rightarrow M + SiO_2$
②=Failed reaction 2: $Si + MO_x \rightarrow MSi_x + SiO_2$
⑥=Failed reaction 6: $Si + MO_x \rightarrow M + MSi_xO_y$

● H																	● He
Li	Be											B	C	N	O	F	Ne
① Na	Mg											Al	Si	● P	● S	● Cl	● Ar
K	Ca	Sc	② Ti	① V	① Cr	① Mn	① Fc	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr
● Rh	Sr	Y	Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe
● Cs	⑥ Ba	R	Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn
○ Fr	○ Ra	A	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt									

R	La	Ce	Pr	Nd	○ Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
A	○ Ac	○ Th	○ Pa	○ U	○ Np	○ Pu	○ Am	○ Cm	○ Bk	○ Cf	○ Es	○ Fm	○ Md	○ No	○ Lr

Among the candidate of high-k materials, Hf-based materials are the most promising candidate of them. As shown in Figure 1.3, many papers on high-k materials are submitted in the primary conferences up to 2002. However, from 2003 to now, the candidate of high-k materials have narrowed down to Hf-based materials. Therefore, Hf oxides (HfO_2) and Hf-based silicates or nitrides (HfSiON), with dielectric constants of 25 and 10 to 15 respectively, are among the promising materials for the 65 or 45-nm-technology nodes.

Usually, when the EOT becomes small, the effective carrier mobility tends to

decrease due to scattering in the high-k layer or at the interface between the high-k layer and the substrate. It has reported that Hf-based films have reduced scattering when a SiO_2-based interfacial layer of 0.5 to 0.7 nm is inserted, however, this attempt increases the EOT.

Consequently, in this work, Lanthanum Oxide (La_2O_3), one of the rare earth oxides, has been tried as a gate insulator, because it has a relatively high dielectric constant of 27, which is slightly higher than that of HfO_2 and a high band offset of 2.3 eV from the conduction band of silicon to La_2O_3 has the advantage of further reducing the leakage current.

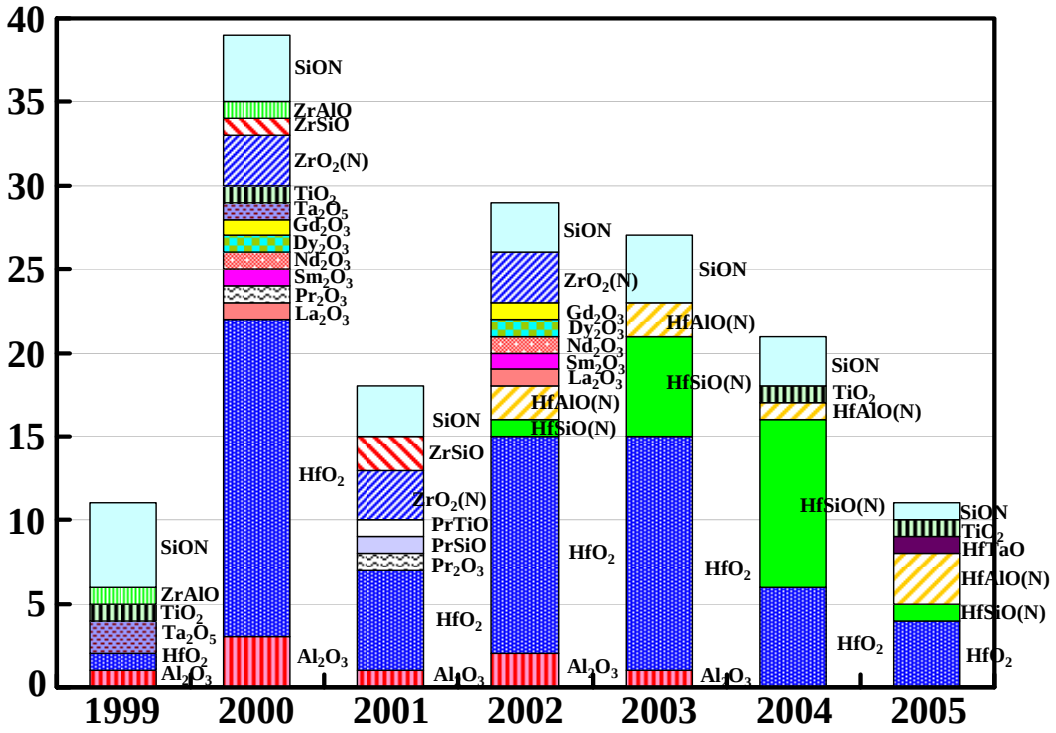


FIGURE 1.3 Reported High-k materials at IEDM and VLSI symposium.

1.4 PROPERTIES OF La_2O_3

To perform a low EOT, high-k gate dielectrics materials must have high enough dielectric constant. However, material with very high dielectric constant tends to have narrower band gap that allows higher Schottky conduction currents and tunneling currents. Figure 1.4 shows band gap energy of several metal oxide and silicate materials as a function of dielectric constants. La_2O_3 gives high dielectric constant of 27 and wide band gap of 5.6 eV that is suitable for the use of gate dielectrics.

To inhibit a low leakage current due to Schottky emission conduction mechanism, the high-κ gate dielectric materials must have wide band gap and high barrier of more than 1 eV for both electrons and holes. Figure 1.5 predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy. La_2O_3 has a good symmetrical band barrier of more than 2 eV for both electrons and holes that is compatible for CMOS devices.

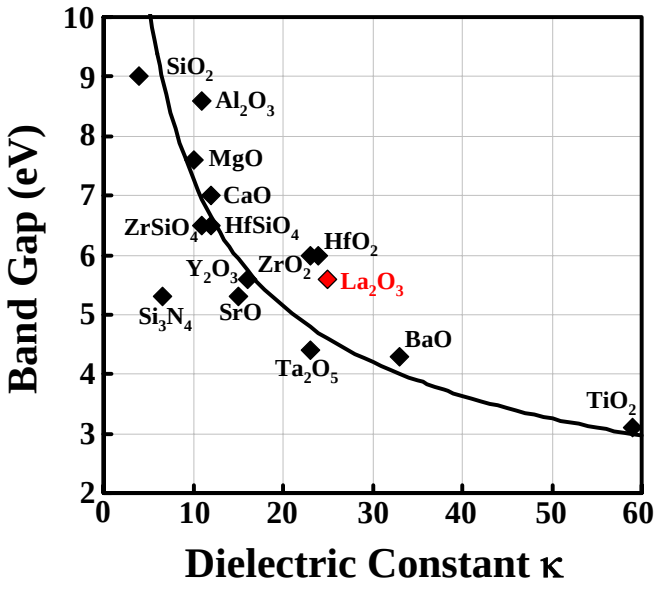


FIGURE 1.4 Band gap energy of several metal oxide and silicate materials as a function of dielectric constant [3].

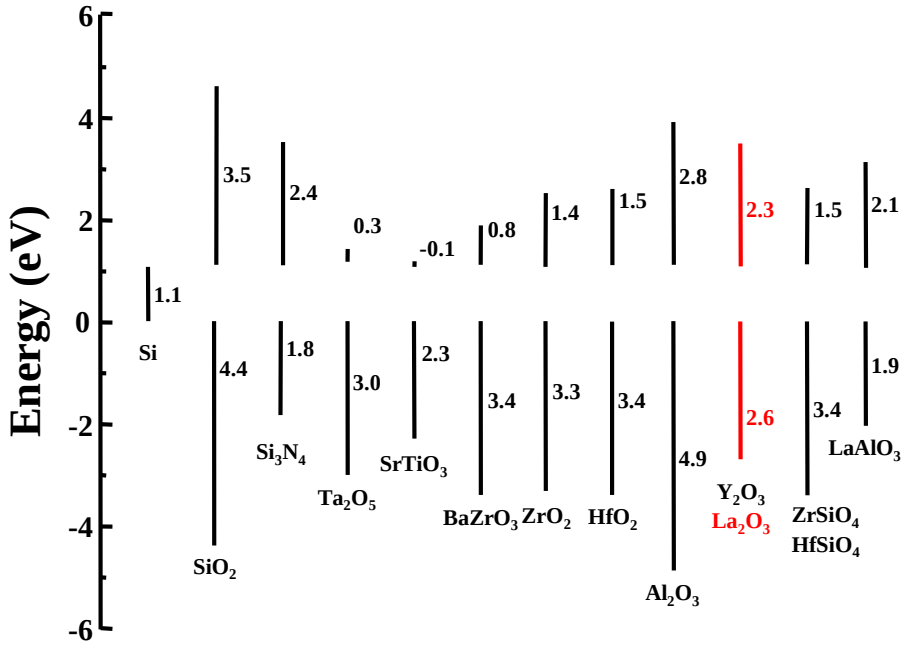


FIGURE 1.5 Predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy [3].

Previously, excellent results on several high-k gate dielectrics materials have been reported. Figure 1.6 shows reported leakage current density of various high-k gate materials as a function of EOT. From Figure 1.6, the superiority of La_2O_3 is obvious, low EOT with low leakage current can be achieved with La_2O_3.

Finally, La_2O_3 is considered to be the most promising gate dielectric material for the next generation gate dielectric technology. La_2O_3 material shows good physical properties, high dielectric constant of 27, wide band gap of 5.6 eV, symmetrical band offset for electrons and holes of more than 2 eV, and good thermal stability in contact with silicon. In this study, the electrical properties of MOSFET with La_2O_3 gate dielectrics will be evaluated.

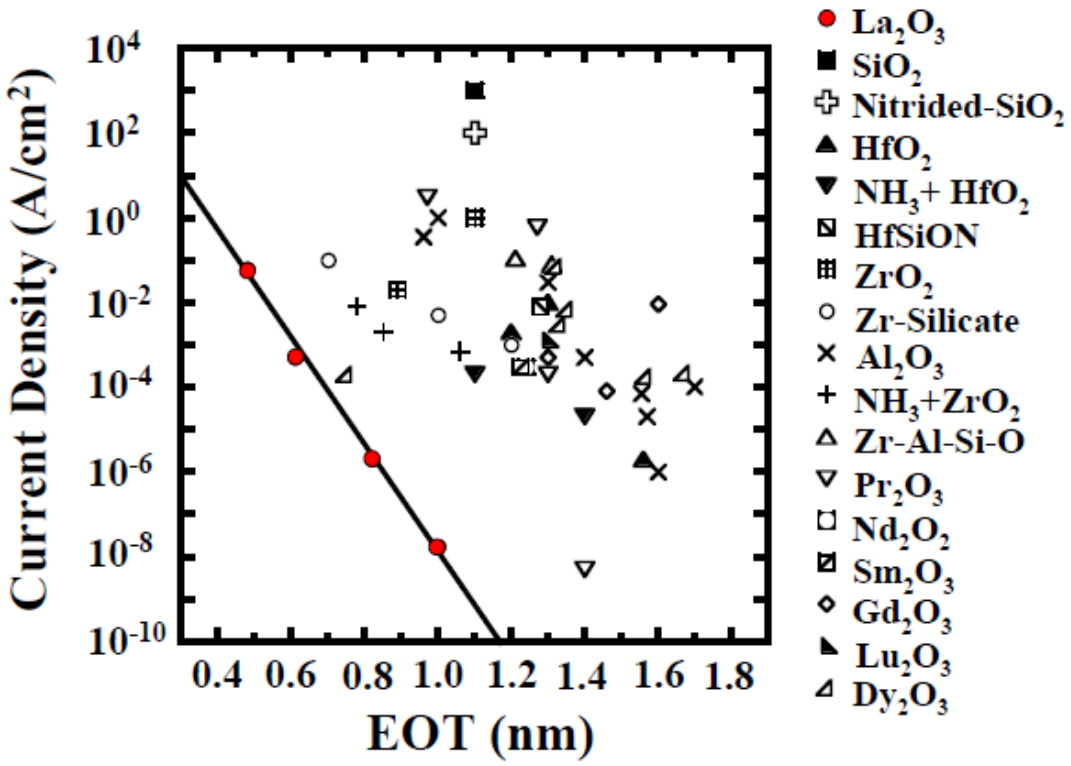


FIGURE 1.6 Reported leakage current density of various high-k gate materials as a function of EOT [4].

1.5 PURPOSE OF THIS STUDY

This study is performed for La_2O_3 CMOS application. The objective of this study is to maximize the dielectric constant of La_2O_3 and to improve the quality of the film. The points of view on optimization are followed by

- ✓ EOT (< 1 nm)
- ✓ Leakage current
- ✓ Thermal stability
- ✓ Oxide traps

By investigating these points, finally, the possibility of practical use on La_2O_3 MOSFET is deliberate.

2

FABRICATION AND CHARACTERIZATIO METHODS

2.1 EXPERIMENTAL PROCEDURE

2.1.1 Fabrication Procedure for MOS Capacitor

Figure 2.1 summarizes device fabrication flow of La_2O_3 MOS-capacitors. La_2O_3 MOS capacitors were fabricated on n-type (100)-oriented 2-5 Ω-cm Si substrate. To determine the capacitor area and to avoid unexpected peripheral effect, 300 nm-thick thermal oxide was formed and patterned photolithography. The wafers were then cleaned by a mixture of H_2SO_4/H_2O_2 at 85 ^oC for 5 min to remove all the resist-related organic contamination, followed by diluted HF cleaning. Thin film of La_2O_3 was deposited using e-beam evaporation from La_2O_3 pressed target in an ultra-high vacuum chamber of 10^{-7} Pa. The tungsten (W) gate electrode of 50 nm was coated by RF sputtering with power of 150 W. Electrode was finally lithographically patterned to form MOS capacitors. Post-deposition annealing (PDA) and post-metallization annealing (PMA) in N_2 were carried out. The detailed explanation of each process and experimental equipment will be described in next section.

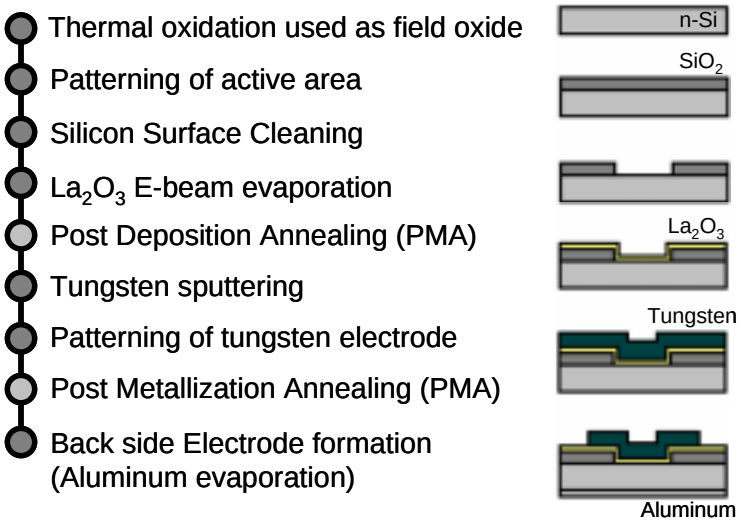


FIGURE 2.1 The fabrication procedure for MOS-Capacitor

2.1.2 Silicon surface Cleaning Process

Prior to deposit of high-*k* gate thin films for LSI fabrication process, the ultra-pure surface of a bare Si-substrate should be chemically cleaned to remove particles contamination, such as metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. It is considered that this substrate cleaning process is very important to realize desirable device operation and its reproducibility.

In full fabrication processes as well as substrate cleaning, DI (de-ionized) water is one of the most important factors because DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. Theoretical resistively of pure water at 25ºC is 18.3 MΩ·cm. The resistively value of ultra-pure water (UPW) used in this study achieve more than 18.2 MΩ·cm and have fewer than 1.2 colony of bacteria per milliliter and no particle larger than 0.25 um.

In this study, the method of surface cleaning process was used a typical processing using hydrofluoric acid, which is usually called RCA cleaning method, was proposed by W. Kern *et al*. But some steps were reduced. First, silicon substrates were dipped in SPM solution, mixed 4 parts H_2SO_4 (96%) with 1 part H_2O_2 (30%) at 85 degrees, generating heat helping organic materials oxidize. And then, dipped in hydrofluoric acid diluted at 1% to remove chemical or natural oxide layers and obtain hydrogen-terminated surface. Hydrogen-terminated surface is stable and a preventive oxidation.

2.1.3 Electron-Beam Evaporation Method

La_2O_3 dielectrics were deposited in ultra high vacuum by electron-beam evaporation method. Figure 2.2 shows the schematic drawings and a photo of the equipment. The background pressure in growth chamber reached as high as 10^{-8} Pa and was approximately 10^{-7} Pa during deposition. In the growth chamber, a sintered La_2O_3 target, which is evaporation source, is irradiated with electron beam accelerated by 5 kV. The target is heated up and LaO_x molecules are evaporated. Then ultra thin LaO_x film is deposited on the Si-substrate. Physical thickness of the film is monitored with a film thickness counter using crystal oscillator. The temperature of the substrate is controlled by a substrate heater and is measured by a thermocouple.

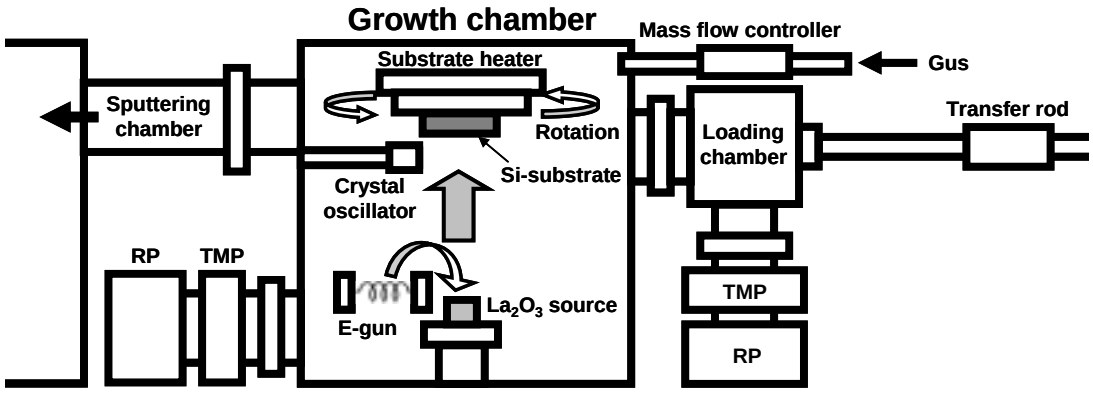


FIGURE 2.2 Schematic drawing of e-beam evaporation system.

2.2 MEASUREMENT METHODS

2.2.1 X-ray Photoelectron Spectroscopy (XPS)

XPS, also known as the Electron Spectroscopy for Chemical Analysis (ESCA), is one of the useful methods to evaluate chemical bindings in the oxide or at the interface. Figure 2.3 explains the principle of XPS. Samples were irradiated with X-ray and the emitted photoelectrons with kinetic energy KE were detected. Measured KE was given by

$$KE = hv - BE - \varphi_s \tag{2.1}$$

where hv is the photon energy, BE is the binding energy of the atomic orbital from which the electron generates and φ_s is the spectrometer work function. The binding energy is the minimum energy needs for breaking the chemical bond of molecule and is inherent in each bond of molecule. Thus, the binding states can be identified by the positions of the binding energy which the peak appears. In the case that the peak position was different from the expected position, the chemical bond states were discussed considering the amount of shift to higher or lower energy side.

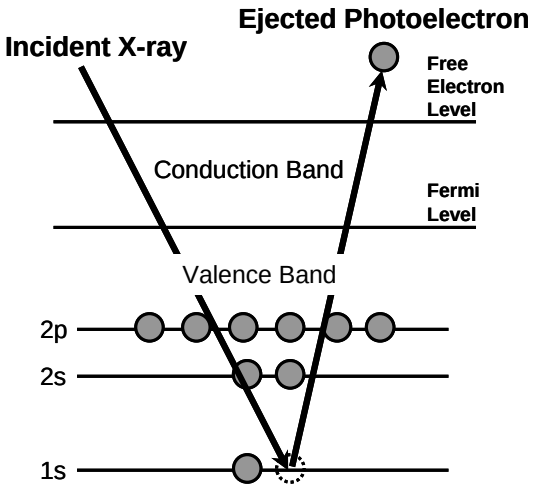


FIGURE 2.3 Principle of XPS measurement.

Conventional XPS techniques with low excitation energies are surface-sensitive due to short inelastic mean-free-paths (IMFPs), and it is difficult to obtain information on the bulk electronic structures which are closely correlated with the characteristics of the intrinsic materials. In this study, Hard X-ray Photoemission Spectroscopy (HX-PES) is performed at Super Photon ring- 8 GeV (SPring-8). SPring-8 is the one of the world's largest radiation facilities. The advantages of SPring-8 over average XPS equipments are the high-brightness of radiation which is about a hundred thousand times as high as normal X-ray and the high radiation energy of 30keV ~40keV.

The schematic view and picture of SPring-8 facilities is shown in figure 2.4(a) and (b), respectively. The electrons generated by E-gun are accelerated by linear-accelerator up to 1 GeV. Additionally, the ellipsoid-shaped synchrotron accelerates the electron and delivers them to the storage ring. The storage ring with diameter of 500 m can preserve the electrons keeping the energy at 8 GeV for more than 100 hours. The principle of radiation emission is shown in figure 2.5. As the electron with a speed close to light passes through the magnetic field, the track of electron is bent and radiate electromagnetic wave in the tangential direction of track. The radiation has the wide range spectrum from micro wave to x-ray, additionally, good directivity and polarization. For such qualities, the radiation has been utilized in many scientific technology fields as the best light source in the wavelength ranging from vacuum ultraviolet ray to x-ray.

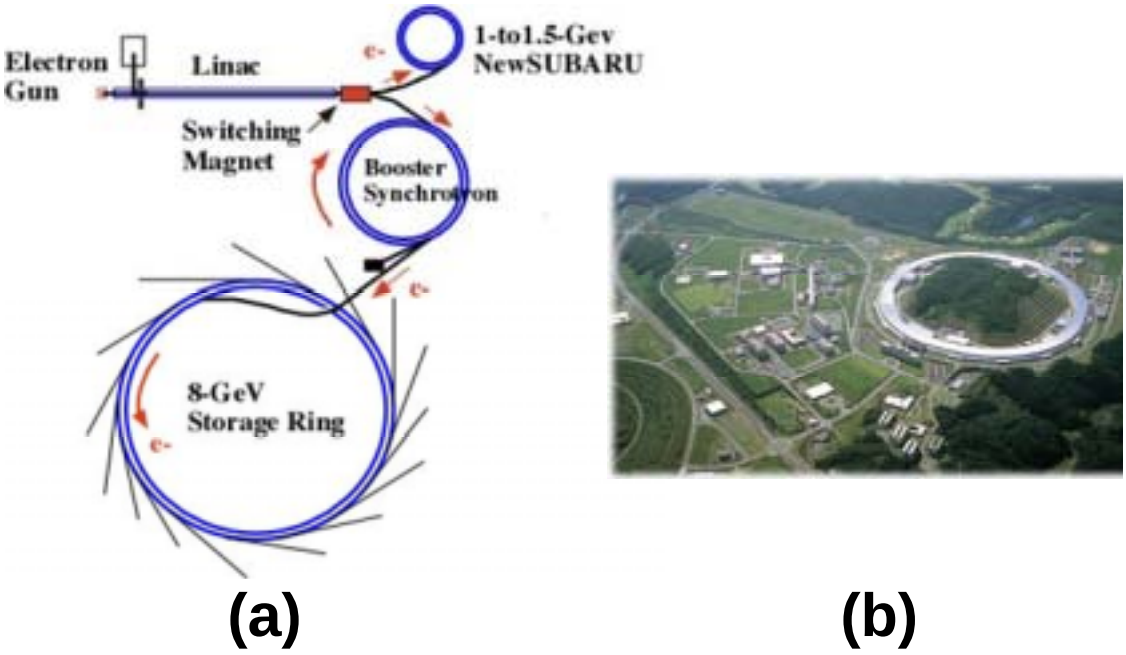


FIGURE 2.4 (a) Schematic view and (b) picture of SPring-8 facilities.

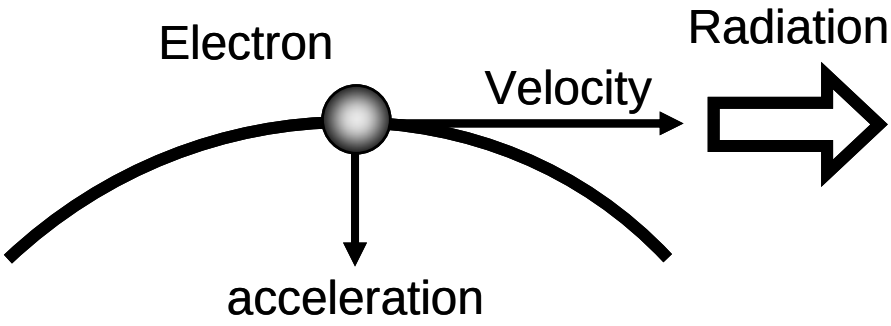


FIGURE 2.5 The principle of radiation emission

2.2.2 C-V (Capacitance-Voltage) Measurement

C-V characteristic measurements were performed with various frequencies (1kHz ~ 1MHz) by precision LCR Meter (HP 4284A, Agilent). The energy band diagram of an MOS capacitor on a p-type substrate is shown in figure 2.6 [5]. The intrinsic energy level E_i or potential ϕ in the neutral part of device is taken as the zero reference potential. The surface potential ϕ_s is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \tag{2.2}$$

It is the change of charge due to a change of voltage and is most commonly given in units of farad/units area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS capacitor from the gate, $C = dQ_G / dV_G$, where Q_G and V_G are the gate charge and the gate voltage. Since the total charge in the device must be zero, assuming no oxide charge, $Q_G = -(Q_S + Q_{it})$, where Q_S is the semiconductor charge, Q_{it} the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \phi_s$, where V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and ϕ_s the surface potential, allowing Eq. (2.2) to be rewritten as

$$C = \frac{dQ_S + dQ_{it}}{dV_{ox} + d\phi_s} \tag{2.3}$$

The semiconductor charge density Q_S, consists of hole charge density Q_p, space-charge region bulk charge density Q_b, and electron charge density Q_n. With $Q_S = Q_p + Q_b + Q_n$, Eq. (2.3) becomes

$$C = -\frac{1}{\dfrac{dV_{ox}}{dQ_S + dQ_{it}} + \dfrac{d\phi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \tag{2.4}$$

Utilizing the general capacitance definition of Eq. (2.2), Eq. (2.4) becomes

$$C = -\frac{1}{\dfrac{1}{C_{ox}} + \dfrac{1}{C_p + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \tag{2.5}$$

The positive accumulation Q_p dominates for negative gate voltages for *p*-substrate devices. For positive V_G, the semiconductor charges are negative. The minus sign in Eq. (2.4) cancels in either case.

Eq. (2.5) is represented by the equivalent circuit in figure 2.7 (a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_p is very high approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in figure 2.7 (b) and the overall capacitance is C_{ox}. For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = -qN_AW$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} as shown in figure 2.7 (c). In weak inversion C_n begins to appear. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (figure 2.7 (d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in figure 2.7 (e) applies in inversion, with $C_b = K_s\varepsilon_o / W_{inv}$ with W_{inv} the inversion space-charge region width.

The flatband voltage V_{FB} is determined by the metal-semiconductor work function difference ϕ_{MS} and the various oxide charges through the relation

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{t_{ox}} \rho_m(x)dx - \frac{1}{C_{ox}}\int_0^{t_{ox}} \frac{x}{t_{ox}}\rho_{ot}(x)dx \tag{2.6}$$

where $\rho(x)$ = oxide charge per unit volume. The fixed charge Q_f is located very near the Si-SiO_2 interface and is considered to be at that interface. Q_{it} is designated as Q_{it} (ϕ_s), because the occupancy of the interface trapped charge depends on the surface potential. Mobile and oxide trapped charges may be distributed throughout the oxide. The *x*-axis is defined in figure 2.6. The effect on flatband voltage is greatest, when the charge is located at the oxide-semiconductor substrate interface, because then it images all of its charge in the semiconductor. When the charge is located at the gate-insulator interface, it images all of its charge in the gate and has no effect on the flatband voltage.

In the study, principally, EOT values and flatband voltage were extracted from C-V characteristics by using the NCSU CVC modeling program [6]. EOT values were calculated with taking quantum effect into account.

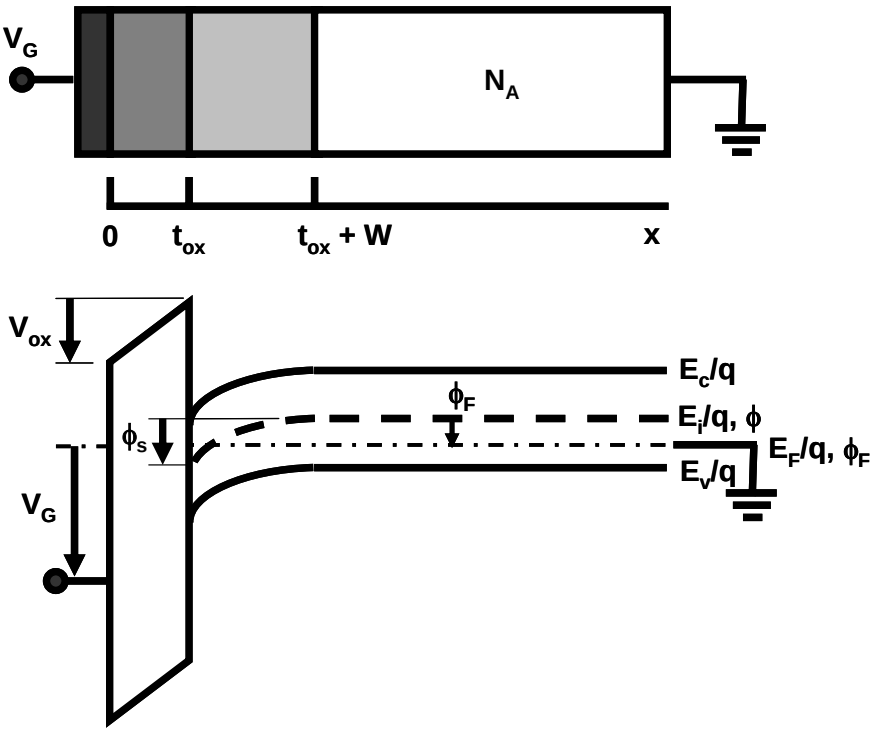


FIGURE 2.6 Cross-section and potential diagram of an MOS capacitor

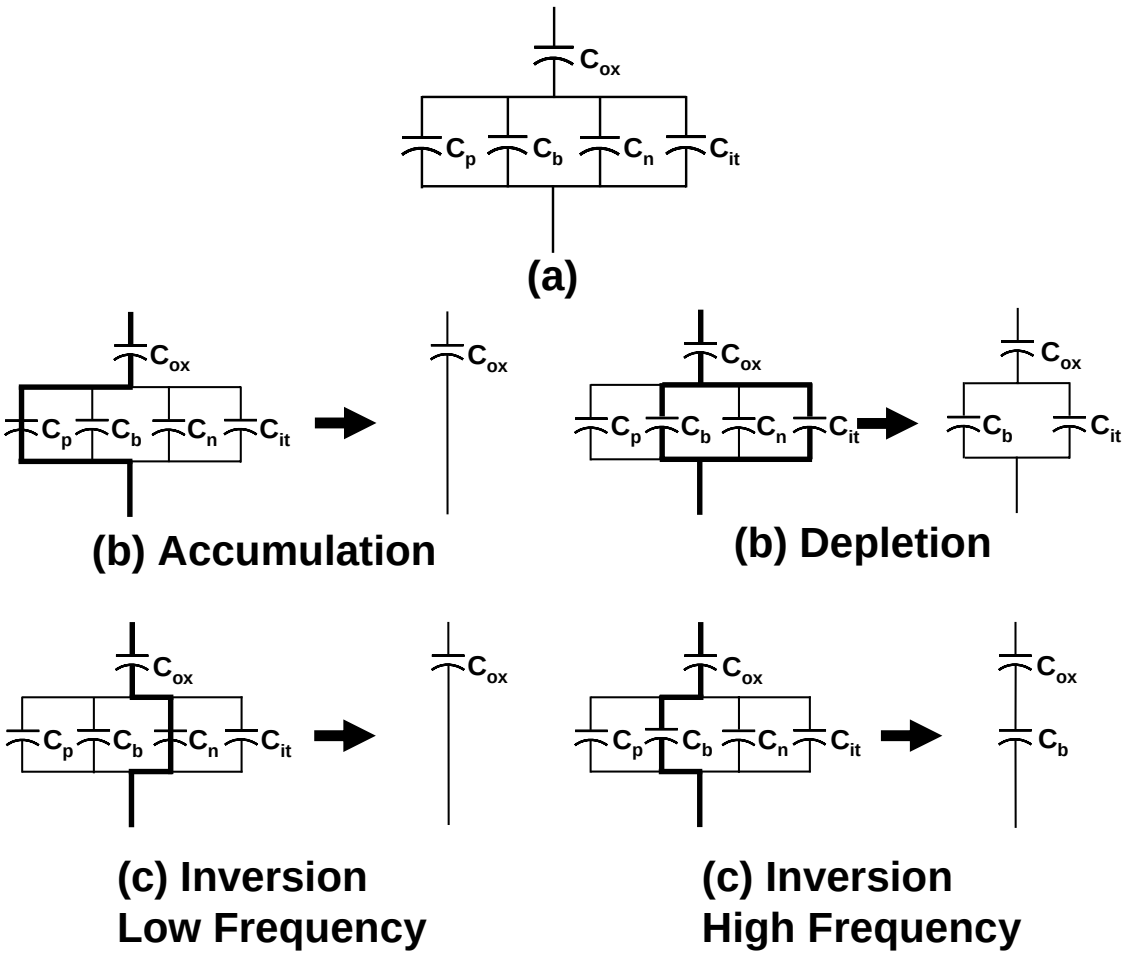


FIGURE 2.7 Capacitances of an MOS capacitor for various bias conditions.

2.2.3 Conductance Method for Interface Trap Density

The conductance method, proposed by Nicosia and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it} [5]. Interface trap densities of 10^9 cm^{-2}-eV^{-1} and lower can be measured. It is also the most complete method, because it yields D_{it} in the depletion and weak inversion portion of the band gap, the capture cross-sections for majority carriers, and information about surface potential fluctuation. The technique is based on measuring the equivalent parallel conductance G_p of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in figure 2.8(a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_s, and the interface trap capacitance C_{it}. The capture-emission of carriers by D_{it} is a lossy process, represented by the resistance R_{it}. It is convenient to replace the circuit of figure 2.8(a) by that in figure 2.8(b), where C_p and G_p are given by

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{2.7}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2.8}$$

Where $C_{it} = q^2 D_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it}C_{it}$, the interface trap time constant, given by $\tau_{it} = [\upsilon_{th}\sigma_p N_A \exp(-q\phi_s/kT)]^{-1}$. Dividing G_p by w makes Eq. (2.8) symmetrical in $\omega\tau_{it}$. Equations (2.7) and (2.8) are for interface traps with a single

energy level in the band gap. Interface traps at the SiO_2-Si interface, however, are continuously distributed in energy throughout the Si band gap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] \tag{2.9}$$

Equations (2.8) and (2.9) show that the conductance is easier to interpret than the capacitance, because Eq.(2.8) does not require C_s. The conductance is measured as a function of frequency and plotted as G_p/ω versus w. G_p/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_p/q\omega$. For Eq.(2.9) one can find $\omega \sim 2/\tau_{it}$ and $D_{it} = 2.5G_p/q\omega$ at the maximum. Hence one can determine D_{it} from the maximum G_p/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis. G_p/ω versus f plots, calculated according to Eqs. (2.8) and (2.9).

Experimental G_p/ω versus ω curves are generally broader than predicted by Eq. (6.49), attributed to interface trap time constant dispersion caused by surface potential fluctuations due to non-uniformities in oxide charge and interface traps as well as doping density. Surface potential fluctuations are more pronounced in p-Si than in n-Si. Surface potential fluctuations complicate the analysis of the experimental data. When such fluctuations are taken into account, Eq. (2.9) becomes

$$\frac{G_p}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] P(U_s)\,dU_s \tag{2.10}$$

where P(Us) is a probability distribution of the surface potential fluctuation given by

$$P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(- \frac{\left(U_s - \overline{U}_s\right)^2}{2\sigma^2} \right) \tag{2.11}$$

With $\overline{U}_s$ and σ the normalized mean surface potential and standard deviation, respectively.

An approximate expression giving the interface trap density in terms if the measured maximum conductance is

$$D_{it} \approx \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{\max}. \tag{2.12}$$

Capacitance meters generally assumed the device to consist of the parallel C_m-G_m combination in figure 2.8 (c). A circuit comparison of figure 2.8(b) to 2.8(c) gives G_p/ω in terms of the measured capacitance C_m, the oxide capacitance, and the measured conductance G_m as

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 \left(C_{ox} - C_m\right)^2} \tag{2.13}$$

assuming negligible series resistance. The conductance measurement must be carried out over wide frequency range. The portion of the band gap probed by conductance measurements is typically from flatband to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50mV or less to prevent harmonics of the signal frequency giving rise to spurious conductances. The conductance depends only on the device area for a given D_{it}. However, a capacitor with thin oxide has a high capacitance relative to the conductance, especially for low D_{it} and the resolution of the capacitance meter is dominated by the out-of-phase capacitive current component. Reducing C_{ox} by increasing the oxide

thickness helps this measurement problem.

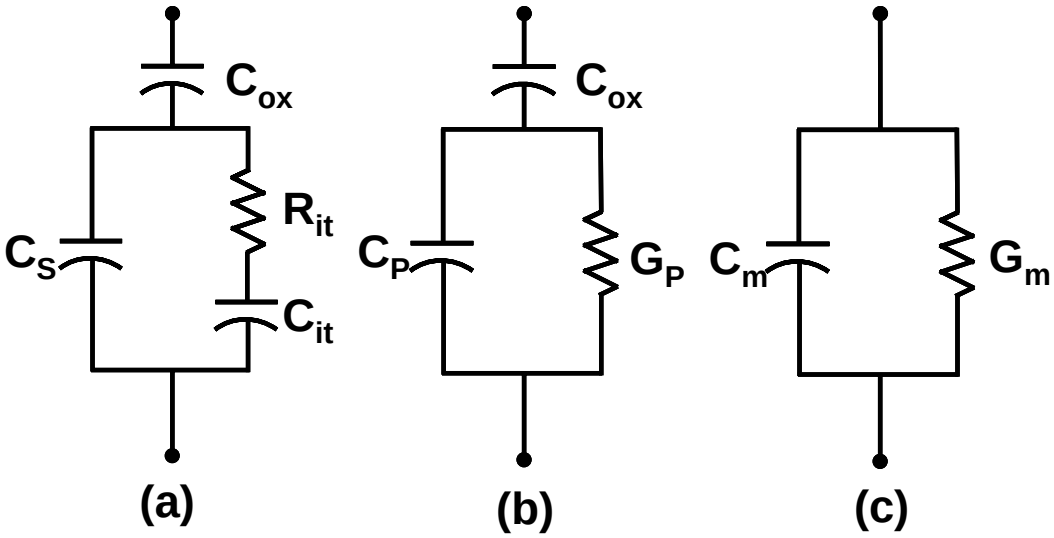


FIGURE 2.8 Equivalent circuits for conductance measurement; (a) MOS-capacitor with interface trap time constant $\tau_{it} = R_{it} C_{it}$, (b) simplified circuit of (a), (c) measured circuit.

2.2.4 J-V (Leakage Current - Voltage) Measurement

It is important to suppress the leakage current of the gate dielectric film as small as possible in order to lower the power consumption of LSI. To estimate the leakage current density, J-V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.).

2.2.4.1 Schottky (SK) Conduction

The Schottky effect is the image-force-induced barrier for charge carrier emission with an applied field [7]. Figure 2.9 shows potential barrier at the metal-vacuum interface. Maximum barrier height is reduced to image-force effect when an electric field is applied. This can help the emission of thermally activated carriers from the metal electrode, which is called Schottky emission. This type of carrier emission is completely analogous to thermionic emission expect that the applied field lowers the barrier height. Metal-vacuum system seen in Figure 2.9 is also equivalent to metal-insulator system as well as semiconductor-insulator system, expect for the dielectric constant of vacuum part.

The main feature of Schottky emission is Schottky barrier lowering (or image-force lowering) [7];

$$\Delta\phi_B = q\sqrt{\frac{qE}{4\pi\varepsilon}} \tag{2.14}$$

Permittivity ε should be replaced by an appropriate permittivity characterizing the medium. Since carrier emission occurs at much higher energy levels than Fermi level oh the injecting electrode, tunneling probability can be regard as 1. So Tunneling current is

$$J = \frac{4\pi m^* q}{h^3} k_B{}^2 T^2 \exp\left(-\frac{E_m - E_F}{k_B T}\right)\left[1 - \exp\left(-\frac{V}{k_B T}\right)\right] \tag{2.15}$$

$$E_m - E_F = \phi_0 - \left(\frac{qE}{4\pi\varepsilon_0\varepsilon_i} \right)^{1/2} \tag{2.16}$$

Here, h is Plank constant, k_B is Boltzmann constant, E_m is barrier height ($\phi_0=\phi_m-\chi$), V is applied voltage. On condition is $V>>k_BT$, Eq. 2.14 - 2.16 becomes

$$J = \frac{4\pi m^* q}{h^3} {k_B}^2 T^2 \exp\left(-\frac{\phi_0}{k_B T} \right) \exp\left(\frac{\beta_s}{k_B T} E^{1/2} \right) \tag{2.17}$$

$$\beta_s = \left(\frac{q}{4\pi\varepsilon_0\varepsilon_i} \right)^{1/2} \tag{2.18}$$

This J is also called Richardson-Schottky equation.

As expected, the Schottky current is thermally activated process and the activation energy is characterized by Eq.2.14 - 2.17. The activation energy is modulated by applied bias with Schottky barrier height lowering effect. One notice that the barrier deformation decrease as the dielectric constant increase, indicating that, in high-k oxide films, Schottky emission seems to be less probable than in conventional SiO_2 film.

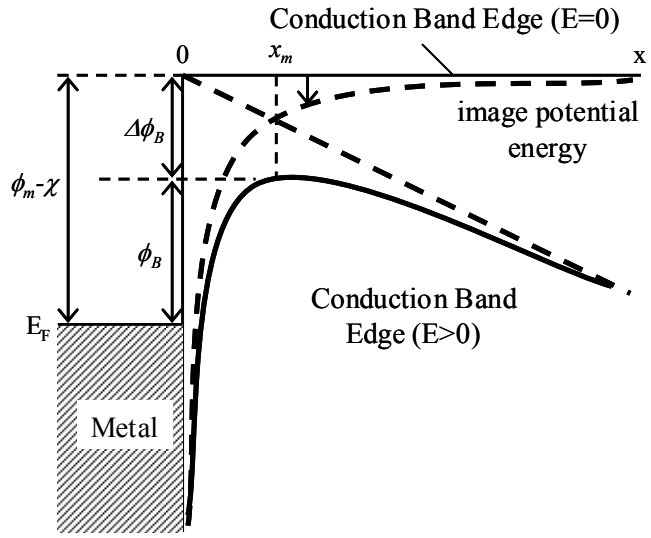


FIGURE 2.9 Band-Energy diagram between a metal surface and a vacuum.

2.2.4.2 Poole-Frenkel (P-F) Conduction

In MIS (Metal-Insulator-Semiconductor) structure, the P-F and Schottky emission results from the lowering of a Coulomb potential barrier by an applied field. The Schottky is associated with the insulator barrier near to the injecting electrode, whereas the P-F effect is associated with the barrier at the trap well in the bulk of insulator film. Thus, neutral donor traps that is neutral when filled and positive when empty don't experience the P-F effect owing to the absence of the Coulomb potential.

Figure 2.10 shows thermionic emission of trapped carrier in the bulk of the film, which occurs at the trap site. Internal thermionic emission is called P-F emission, while external one is Schottky emission. Another way for emission of electron is hopping process, which is a kind of tunneling process in a short range.

It should be notified here that P-F conduction by P-F emission is closely related to the oxide film thickness while Schottky conduction by Schottky emission isn't related to that, as far as the equal oxide field is concerned.

Figure 2.11 shows the restoring force in both Schottky and P-F effect, which comes from Coulomb interaction between escaping electron and a positive charge. The restoring force is due to electrostatic potential that make electron move back to its equilibrium position. Although the restoring force is same of the both, they differ in the positive image charge is fixed for the P-F barriers but mobile with Schottky emission. This results in a barrier lowering twice as great for the P-F effect.

$$\Delta\phi_{PF} = \left(\frac{q^3 E}{\pi\varepsilon_0\varepsilon_i}\right)^{1/2} = \beta_{PF} E^{1/2} \tag{2.19}$$

$$\Delta\phi_{SK} = \left(\frac{q^3 E}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2} = \beta_{SK} E^{1/2} \tag{2.20}$$

In that the electrons have enough energy to go over the energy barrier and travel in the conduction band with a mobility μ which is dependent on the scattering with the lattice, the general expression of the bulk current is expressed by

$$J = qn(x)\mu E \tag{2.21}$$

The concentration of free carrier in the insulator is following.

$$n = N_c \exp\left(-\frac{q(E_c - E_F)}{kT}\right) \tag{2.22}$$

Since E_c-E_F is equal to effective trap barrier height including barrier lowering effect described by Eq. 2.19, the effective barrier height and governed by the P-F emission is written by following.

$$E_c - E_F = \phi_{SK} - \Delta\phi_{PF} = \phi_{SK} - \beta_{PF} E^{1/2} \tag{2.23}$$

$$J = qN_c \exp\left(-\frac{\phi_{SK}}{kT}\right)\exp\left(\frac{q}{kT}\beta_{PF} E^{1/2}\right)\mu E \tag{2.24}$$

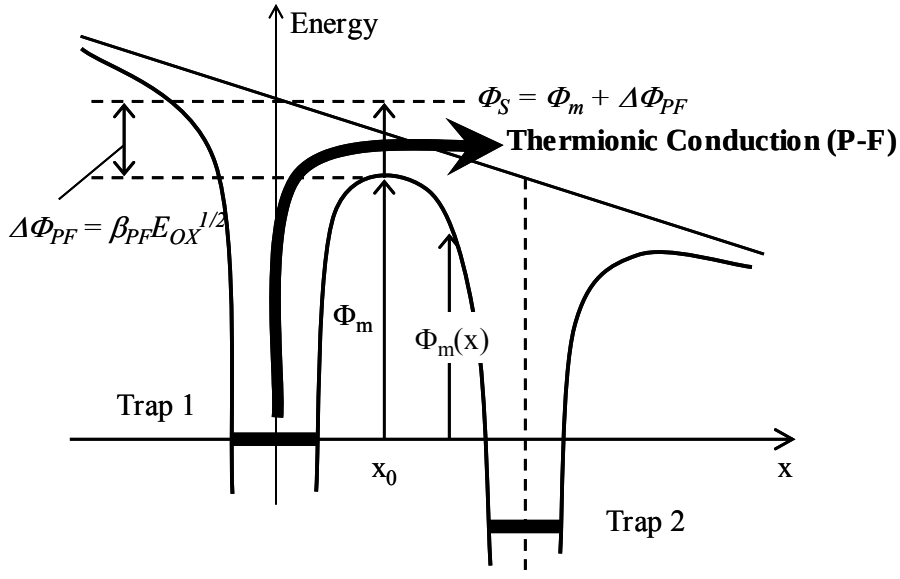


FIGURE 2.10 Thermionic condition (Poole-Frenkel Condition)

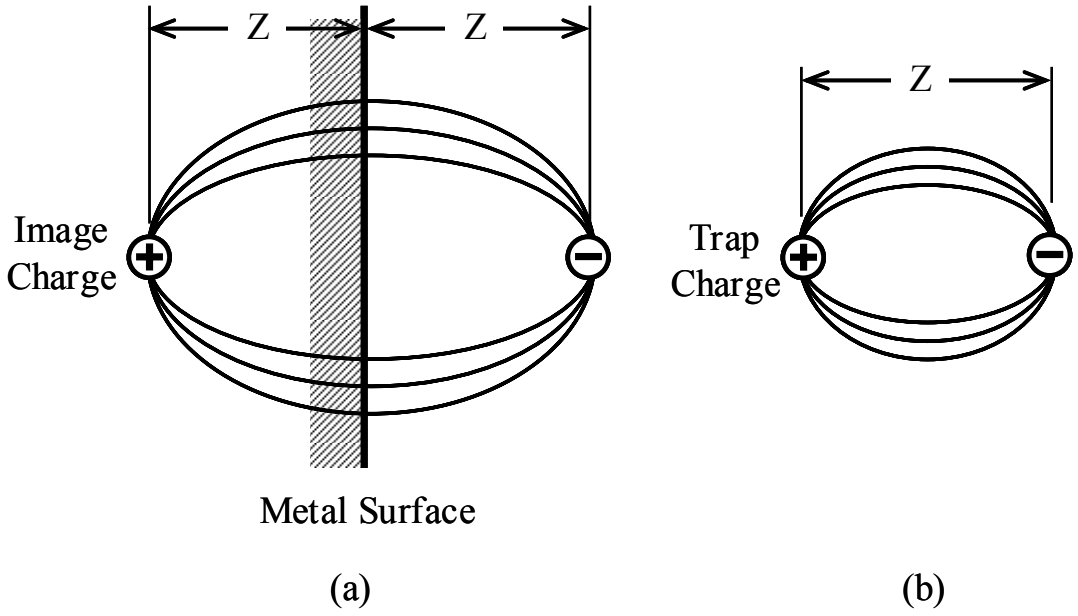


FIGURE 2.11 Restoring force on escaping electron [8]

2.2.4.3 Fowler-Nordheim (F-N) Conduction

F-N tunneling occurs when electrons tunnel into the conduction band of the oxide layer. Figure 2.12 (a) shows F-N tunneling of electrons from the silicon surface inversion layer. The complete theory of F-N tunneling is rather than completed. For the simple case where the effects of finite temperature and image-force barrier lowering are ignored the tunneling current density is given by [9]

$$J = \frac{q^3 E}{8\pi h \phi_{OX}} \exp\left(-\frac{4\sqrt{2m^*}\phi_{OX}^{3/2}}{3\hbar qE} \right) \tag{2.25}$$

Here, h is Plank constant, q is electric charge, E is electric field in the oxide, ϕ_{OX} is barrier height of the oxide.

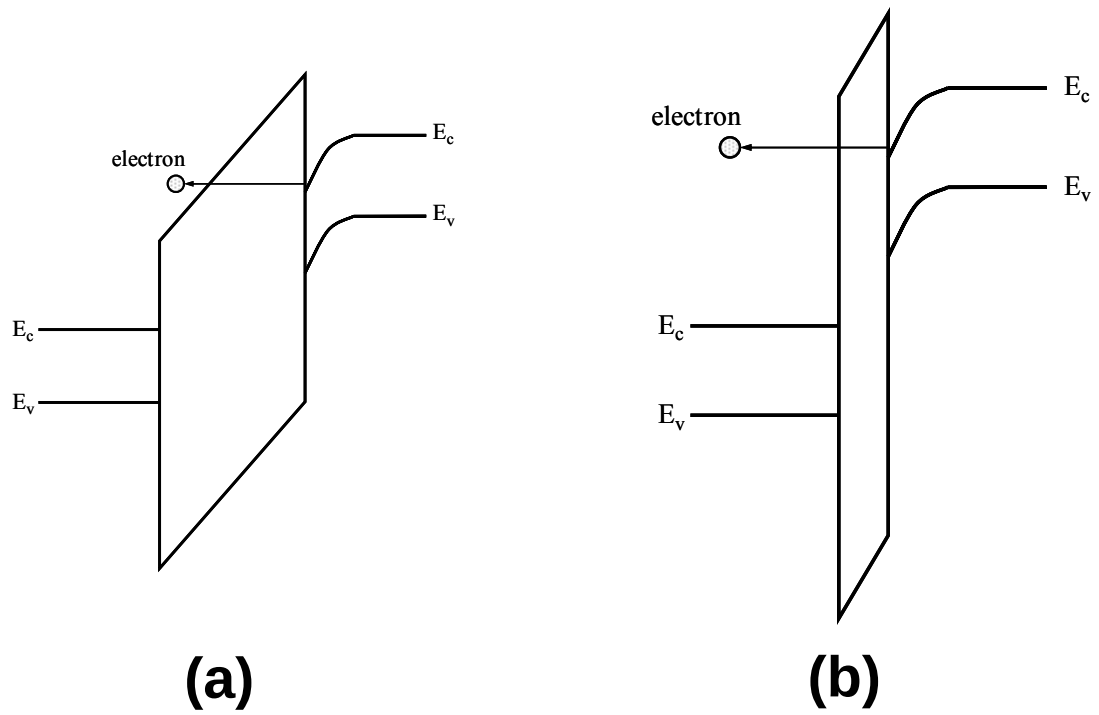


FIGURE 2.12 (a) F-N tunneling and (b) direct tunneling [1]

3

PROCESS OPTIMIZATION OF ABSORBED La_2O_3

3.1 INTRODUCTION

Post-deposition stability to ambient exposure is one of the key issues that need to be examined as reactions with ambient gases like H_2O, CO_2, and vapors of organic solvents present in the laboratory atmosphere may lead to significant degradation of the electrical properties of the film. It is well known that La_2O_3 is hygroscopic forming hydroxide. Bernal *et al.* exposed three different samples of La_2O_3 in air for several months to years and found that air exposure transformed them to partially carbonated lanthanum hydroxide [10]. The thermal decomposition of the air stabilized samples was studied using thermogravimetric analysis, temperature programmed desorption, Fourier transform infrared spectroscopy (FTIR) and x-ray diffraction (XRD) and a schematic reaction mechanism for the thermal decomposition of the lanthanum hydroxicarbonate was proposed. By reversing the steps of this mechanism, T. Gougousi *et al.* described the reaction of La_2O_3 films with H_2O and CO_2 through the scheme [11]:

$$La_2O_3 + CO_2 \xrightarrow{\text{first step}} La_2O_2CO_3$$

$$La_2O_2CO_3 + 2H_2O \xrightarrow{\text{second step}} La_2(OH)_{6-2x}(CO_3)_x$$

$$La_2O_3 + 2H_2O \xrightarrow{\text{first step}} LaOOH$$

$$La_2OOH \xrightarrow{\text{third step}} 2La(OH)_3$$

In addition, effects of the moisture absorption on the permittivity of La_2O_3 film and on the surface roughness of La_2O_3 film have been investigated by Yi Zhao *et al.* [12]. The moisture absorption degrades the permittivity of La_2O_3 film annealed in N_2 ambient after exposure to the air for several hours because of the formation of $La(OH)_3$ with a lower permittivity in figure 3.1. Furthermore, AFM results indicate that the moisture

absorption also increases the surface roughness of La_2O_3 films on silicon.

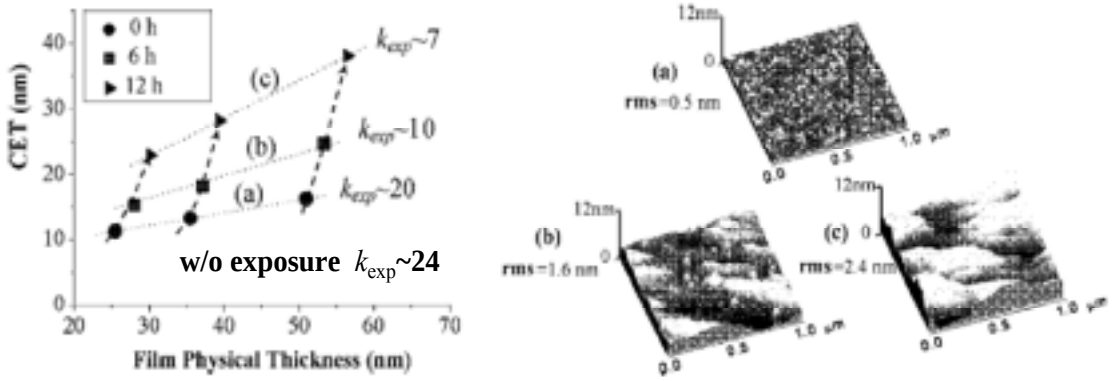


FIGURE 3.1 Time series analysis of the moisture absorption on the permittivity of La_2O_3 film and on the surface roughness of La_2O_3 film by Yi Zhao *et al*.

In this chapter, the process optimization of ultra-thin La_2O_3/Si by the thermal decomposition of $La(OH)_3$ is reported.

3.2 PROCESS OPTIMIZATION WITH ABSORBED La_2O_3 COMPOSITION

It is mentioned in section 3.1 that La_2O_3 form $La(OH)_3$ layer due to strong absorbent, then the layer is increased in time sequence. In this section, the transformation of the absorbed La_2O_3 composition by thermal treatment and the influence of the shading on the electrical characteristics are investigated and the best condition is extracted.

3.2.1 Analysis of Absorbed La_2O_3 Composition by XPS

By using HX-PES, ultra-thin La_2O_3 (4 nm)/Si structure is measured for the confirmation of hydroxide and investigation of composition transformation to annealing. These measured samples are coated with self-organizing monomolecular film (Hexamethyldisilazane, HMDS, $[(CH_3)_3Si]_2NH$) by way of avoiding the change in time sequence.

Figure 3.2(a) shows O1s spectra of HMDS/La_2O_3/Si in various post-deposition annealing (PDA) temperatures. In as deposition (1), the largest peak from La-O-H bonds and little or nothing La-O-La peak are observed. This result means that almost La_2O_3 change the hydroxide. In PDA300 ^oC sample (2), there is clearly La-O-La peak It is considered that some $La(OH)_3$ was resolved into La_2O_3 by annealing at 300 ^oC. In PDA500 ^oC (3) and PDA700^oC samples (3), there are large peak of La-O-Si bonds. This peak denotes that La_2O_3/Si interface reaction was accelerated by higher temperature annealing. Figure 3.2 (b) exhibits the PDA temperature dependence of the maximum values on each component. According to literature [13], $La(OH)_3$ bulk thermally decomposes into La_2O_3 at about 500 ^oC. In this case of ultra-thin La_2O_3/Si system, $La(OH)_3$ also decrease with increasing in PDA temperature. But $La(OH)_3$ even remain

at 700 ^{o}C. The cause of this residue may be short annealing time of 5 min. When compiling these results, $La(OH)_3$ is resolved into La_2O_3 by annealing more than 300 ^{o}C, then a part of La_2O_3 transform into La-silicate. At 700 oC annealing, almost nothing is La-O-La combinations, then La atoms composed La-silicate. La_2O_3/Si interface reaction can be more definitely confirmed from Figure 3.3. Figure3.3 (a) is Si 1s spectra of HMDS/La_2O_3/Si on various PDA temperatures. At 300 oC annealing, La_2O_3/Si interface scarcely transform. The interface reaction exponentially occurs at 500 ^{o}C, and then La-silicate and SiOx layer more largely grow at 700^{o}C. Figure3.3 (b) shows the dependence on take-off angle of electrons in O 1s spectra of PDA 700 ^{o}C sample. Each spectrum is normalized at La-O-Si peak. When take-off angle become big, Si-O-Si intensity increases. This phenomenon means there is SiO_x under La-silicate.

In summary, almost La_2O_3 change into $La(OH)_3$ due to strongly moisture-absorption property. The formed $La(OH)_3$ resolve into La_2O_3 by annealing more than 300 oC, but La_2O_3/Si interface reaction occur at more than 500 ^{o}C annealing, and then La-silicate and SiO_x layer is formed. In this measurement, the sample in PDA 300 ^{o}C has much quantity of La_2O_3.

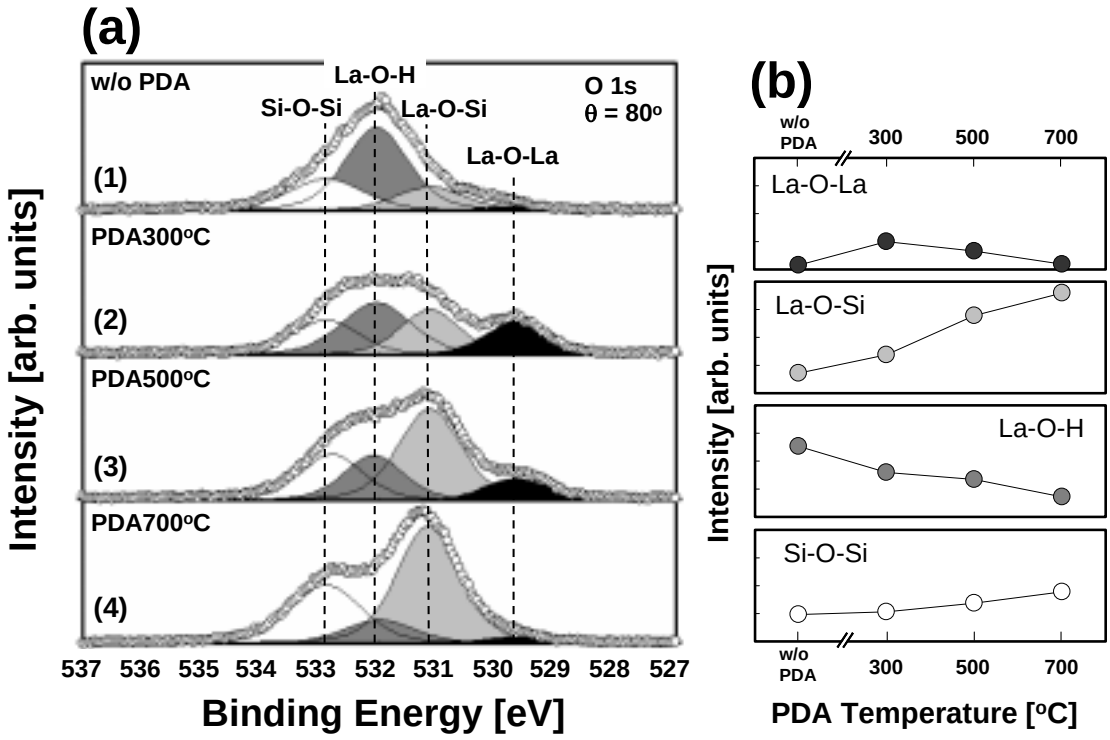


FIGURE 3.2 (a) O1s spectra of HMDS/La_2O_3/Si. Sample (1) is as deposited. Sample (2), (3), and (4) are annealed in nitrogen at 300°C, 500°C, and 700°C, respectively. HMDS was coated after annealing. (b) PDA temperature dependence of each component.

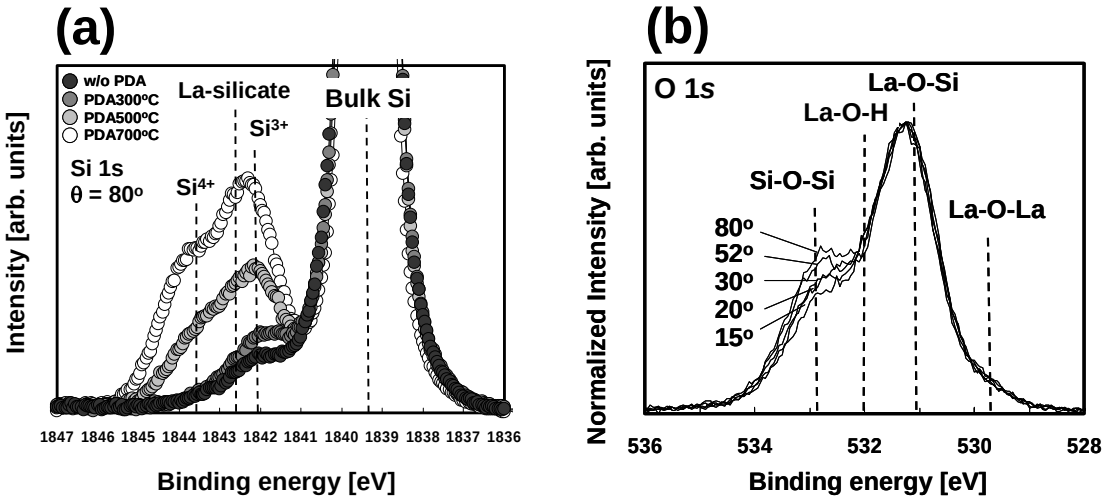


FIGURE 3.3 (a) Si1s spectra of HMDS/La_2O_3/Si on various PDA temperatures. (b) O1s spectra of various take-off angles on PDA700°C sample.

3.2.2 Electrical Characteristics of Absorbed La_2O_3

In this section, I discuss the influence that the composition change of La_2O_3 explained in section 3.2.1 gives various electric characteristics.

Figure 3.4 shows C-V curves at various PDA temperatures with W/La_2O_3/n-Si. After La_2O_3 of these samples is deposited at once, each sample is annealed at each temperature. PDA 300 ^oC sample results in largest accumulation capacitance of all samples. A shoulder-like feature nearby zero voltage grows big depending on annealing temperature. This ‘‘hump’’ can sometimes be observed in MOS structures using high-k and can be attributed to the interface defects and traps [14, 15]. The reason why a hump grew big with increase of PDA temperature may be that there is much Si-dangling bonds due to interfacial layer. Insets in Figure 3.4 show enlarged views at square dotted line of each *C-V* data. *C-V* hysteresis widens as PDA temperature, and then it narrow at PDA 700 ^oC. In general, *C-V* hysteresis is caused for “border traps” of slow response, described by various names such as “slow traps”, “near-interface oxide traps”, and “slow interface states”, and this traps decrease with annealing [16, 17]. This widening may be attributed to increasing in border traps by thermally resolving of $La(OH)_3$. Figure 3.5 shows flat band voltage (V_{FB}) as a function of PDA temperature. Nothing is large V_{FB} shift. Figure 3.6(a) shows physical thickness and EOT dependence on PDA temperature. These physical thicknesses are measured by spectroscopic ellipsometerl. The physical thickness of this film decreases by annealing at 300 ^oC. This may resulted from a densification of La_2O_3 film and/or thermal resolution of $La(OH)_3$. As a result of foregoing section, PDA 300 ^oC sample has most quantity of La_2O_3. The effective dielectric constant (k_{eff}), however, does not increase because of the formation of La-silicate (Figure 3.6 (b)). In the case of PDA 500 oC and 700 oC, their physical

thicknesses increase and EOT decrease. These alternation is because of the volume of Si reacted and the lower dielectric constant on La-silicate and SiO_x interfacial layer. As a result, as-deposited sample has k_{eff} = 18.9, on the other hand, PDA 700 oC sample has k_{eff} = 11.0. Figure 3.7 shows J_g at V_g = 1V versus EOT plots of these samples. The annealing at higher temperature increase in the leakage current. In particular, although the thicknesses significantly grow with annealing more than 500oC, the leakage current increase. This result gives three possible causes followed by

1. Crystallization of dielectric film by annealing higher temperature
2. Defects generation by thermally resolving $La(OH)_3$
3. Defects generation by intense reaction of La_2O_3/Si interface.

In next section, these possible causes are discussed in detail.

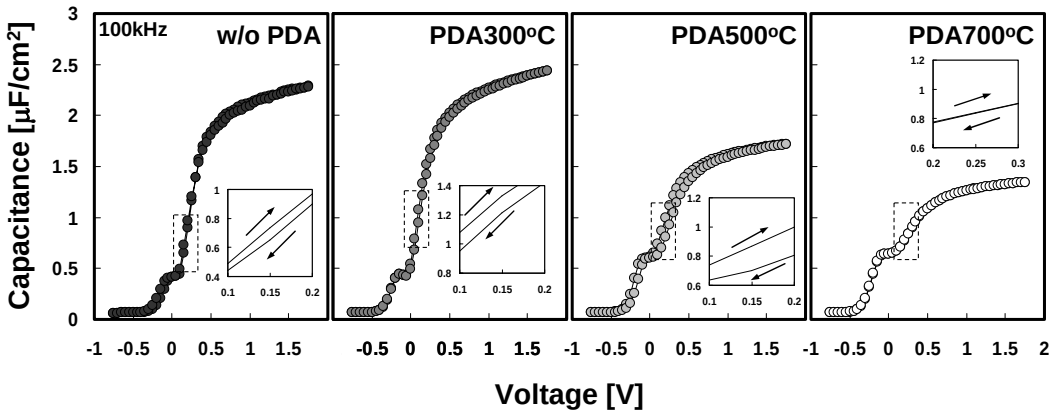


FIGURE 3.4 C-V curves showing the effect of PDA temperature at 300 ^{o}C, 500 ^{o}C, and 700 ^{o}C in N_2. Insert figures are the expansion of a square dotted line. Capacitors are measured at 100 kHz.

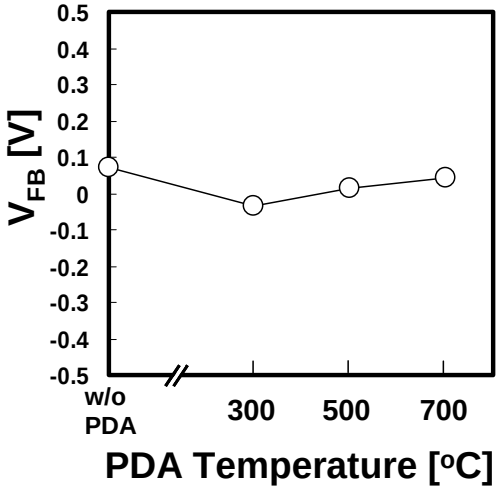


FIGURE 3.5 V_{FB} shift dependence on PDA temperature

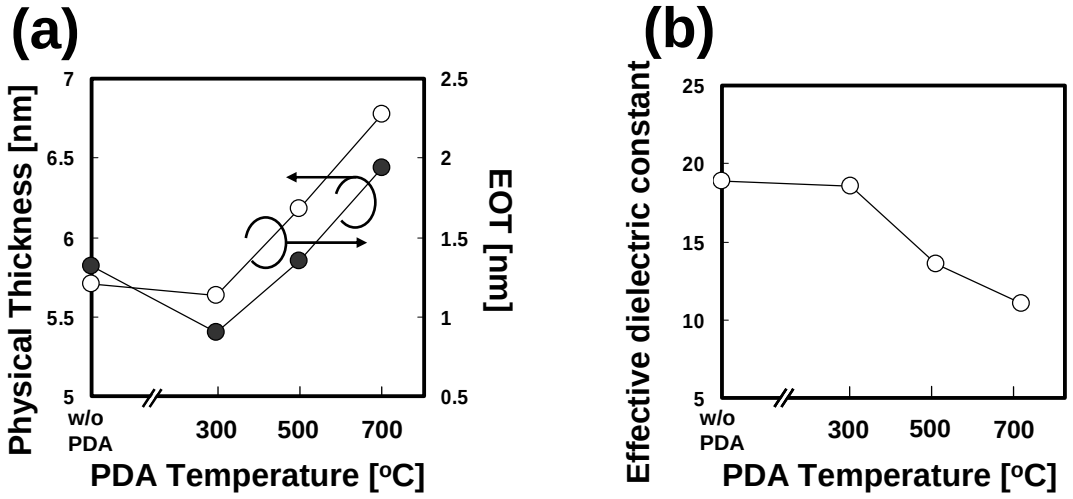


FIGURE 3.6 (a) Physical thickness and EOT dependence on PDA temperature. (b) Effective dielectric constant dependence on PDA temperature.

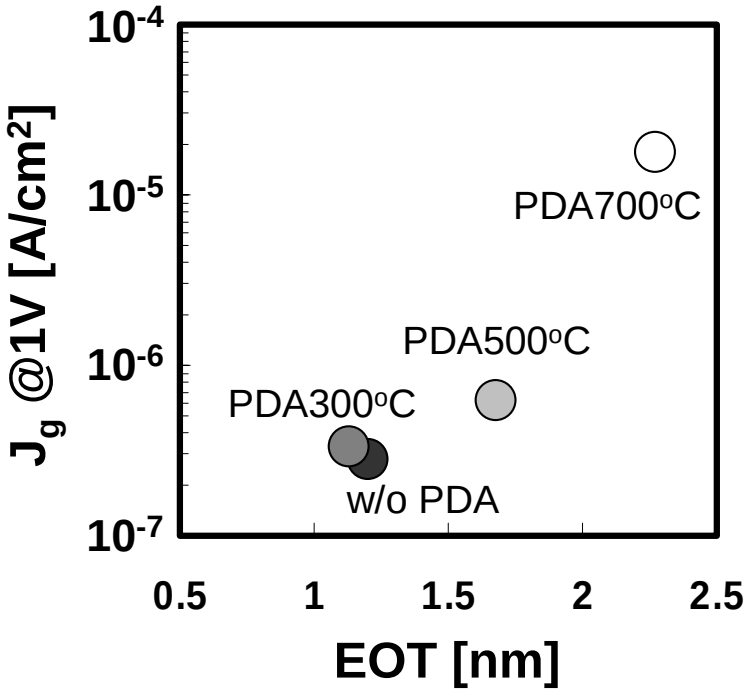


FIGURE 3.7 J_g at V_g = 1V versus EOT plots of W/La_2O_3/Si MOS capacitors with various PDA temperatures.

3.2.3 ANALYSIS OF THREMAL STABILITY

In section 3.2.2, it was mentioned that the leakage current increase though the thicknesses significantly grow with annealing more than 500oC. In addition, I suggest three possible causes;

1. Crystallization of dielectric film by annealing higher temperature
2. Defects generation by thermally resolving $La(OH)_3$
3. Defects generation by intense reaction of La_2O_3/Si interface.

In this section, it is thought to these causes.

3.2.3.1 Crystallization of La_2O_3 with PDA

A lot of crystallization by high temperature heat-treatment of high-*k* films is reported. In generally, the crystallization of the dielectric film causes the degradation of electrical characteristics, especially carrier mobility [18] and leakage current [19], on MOS device. Figure 3.8 shows two examples of crystallization with HfO_2 film. M.Y. Ho et al. report as-deposited ALD HfO_2 films grown on thermal SiO_2 are polycrystalline and the degree of crystallinity depends strongly on the annealing temperature but only weakly on annealing time (Figure 3.8 (a))[20]. Figure 3.8 (b) reported by H. Kim et al. shows that significant crystallization of the 30-Å-thick ALD HfO_2 films was observed after annealing for 30 min at ~500 °C, but a monotonic decrease in leakage current density with increasing annealing temperature is observed after 30 min anneals at temperatures of 700 °C and higher due to increasing in interfacial oxide thickness after annealing at these annealing temperatures [21]. In this section, the crystallization of dielectrics with La_2O_3/Si system is investigated. The evaluation of crystallization was performed by using X-ray diffraction method at

Spring-8.

The measured samples are Carbon (C)/La_2O_3 (4 nm)/n-Si structure. Carbon (~10 nm) on La_2O_3 was deposited by E-beam evaporation by way of avoiding the change in time sequence after PDA. Figure 3.9 shows XRD θ–2 θ scan profiles result for sample annealed at various PDA temperatures. The top of the panel shows the peak positions for crystalline of La-based oxide. All samples have a broad peak between 25 degree and 30 degree because La-based oxide peaks concentrate there. These peaks mean an existence of polycrystalline layer. The crystallization even occurs in the as-deposited film. In as-deposited sample, there is a sharp peak of $La_2Si_2O_7$ at 13 degree. With increase of annealing temperature, La_2O_3 peak of 46 degree becomes sharp. This result displays the growth of poly-crystallized La_2O_3 with increase of PDA temperature. This growth may cause increasing leakage current in section 3.2.2 because defective grain boundary regions may enhance electronic conduction.

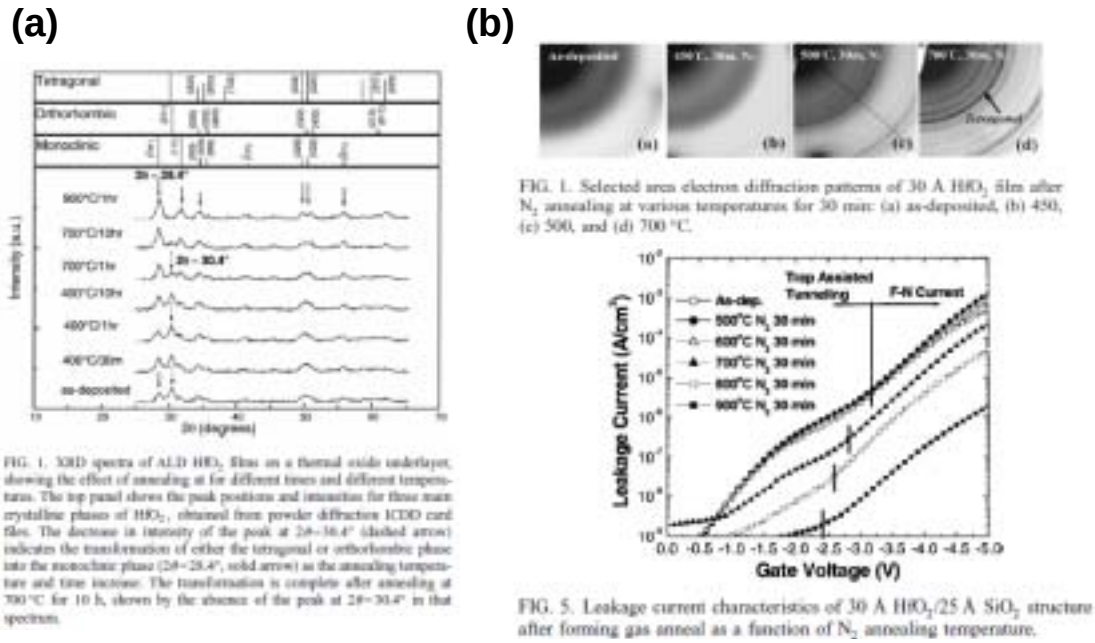


FIG. 1. XRD spectra of ALD HfO_2 films on a thermal oxide underlayer, showing the effect of annealing at for different times and different temperatures. The top panel shows the peak positions and intensities for three main crystalline phases of HfO_2, obtained from powder diffraction ICDD card files. The decrease in intensity of the peak at $2\theta \sim 30.4°$ (dashed arrow) indicates the transformation of either the tetragonal or orthorhombic phase into the monoclinic phase ($2\theta \sim 28.4°$, solid arrow) as the annealing temperature and time increase. The transformation is complete after annealing at 700 °C for 10 h, shown by the absence of the peak at $2\theta \sim 30.4°$ in that spectrum.

FIG. 1. Selected area electron diffraction patterns of 30 Å HfO_2 films after N_2 annealing at various temperatures for 30 min: (a) as-deposited, (b) 450, (c) 500, and (d) 700 °C.

FIG. 5. Leakage current characteristics of 30 Å HfO_2/25 Å SiO_2 structure after forming gas anneal as a function of N_2 annealing temperature.

FIGURE 3.8 Crystallization of HfO_2. (a) XRD spectra of ALD HfO_2 films on thermal oxide showing the effect of various annealing conditions [20]. (b) Electron diffraction and leakage current characteristics of HfO_2 after annealing at various temperatures [21].

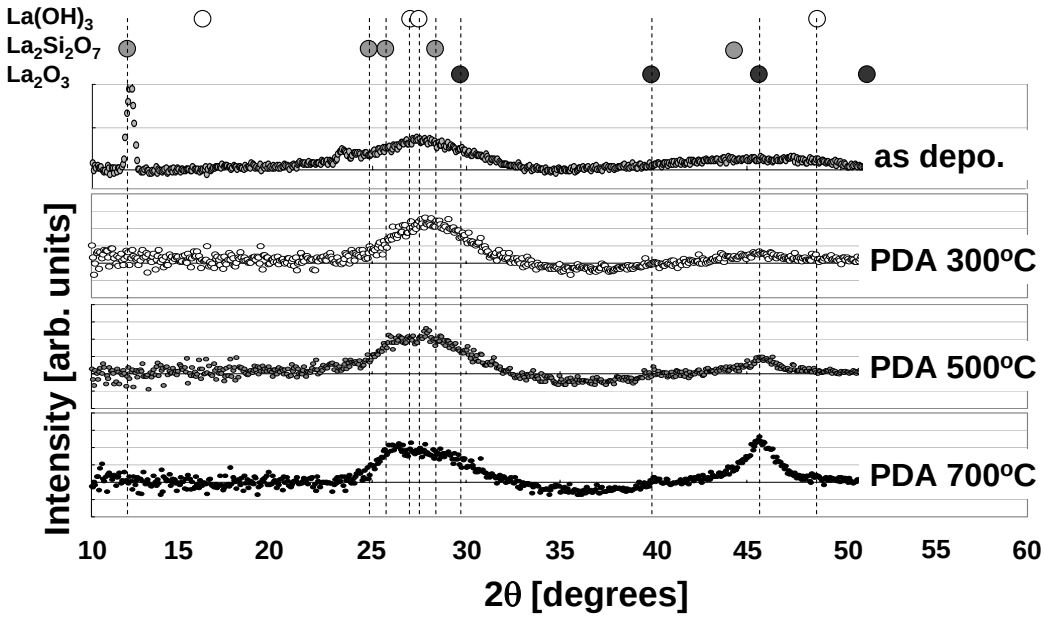


FIGURE 3.9 XRD θ–2 θ scan profiles of C/La_2O_3/Si showing the effect of various annealing temperatures. Carbon is coated by E-beam evaporation after PDA. The top of the panel shows the peak positions for crystalline of La-based oxide.

3.2.3.2 Generation of Defects by $La(OH)_3$ Resolution and Interface Reaction

According to A. Fukuyama, in Pt/La_2O_3/Pt MIM structure, the carrier conduction mechanism of PDA 300^{o}C condition is from Schottky to Poole-Frenkel (P-F) to F-N conduction (Figure 3.10) [22]. On the other hand, post-metallization annealing (PMA) 300oC do not have P-F conduction. P-F conduction mechanism is caused in a trap site of insulator and interface. In this section, I discuss the change of the leakage current depending on PDA temperature in section 3.2.2 to direct my attention to the generation of defects by $La(OH)_3$ resolution and interface reaction.

Figure3.11 shows *C-V* characteristics of W/La_2O_3/Si MOS-capacitors with carrying out PMA 300 ^{o}C and 500 ^{o}C. These La_2O_3 film is deposited at once with the former PDA samples. Nothing is the change of accumulation capacitance from as-deposited sample to PMA 300 ^{o}C. The capacitance of PMA 500 ^{o}C sample decrease, compared to as-deposited. Insets in Figure 3.11 show enlarged views at square dotted line of each *C-V* data. *C-V* hysteresis of PMA 300 ^{o}C and PMA 500 ^{o}C is much smaller than as-deposited sample. Figure 3.12 shows (a) V_{FB} and (b) EOT yielded from these *C-V* data as a function of annealing temperature. In the case of PMA, V_{FB} move from as-deposited V_{FB} to positive direction with PMA 300 ^{o}C and transfer from there to negative direction with PMA 500 ^{o}C. An EOT of PMA 300 ^{o}C is the same as as-deposited, and PMA 500 ^{o}C increase. I guess a mechanism of these phenomena. In PDA at 300 oC, as a result that H_2O fall out from the film due to thermal resolution of La(OH)3, EOT decrease by decreasing the physical thickness and reviving La_2O_3. In PMA at 300 oC, on the other hand, EOT do not decrease because H_2O remain in the film. In addition, the C-V hysteresis of PDA sample widen at 300 oC and 500 oC since

the border trap generation by H_2O falling out, while PMA samples has very little C-V hysteresis. The difference of V_{FB} between PDA 300 ^oC and PMA 300 ^oC may be related to the defect generation, which is oxygen vacancy, by H_2O falling out. Figure 3.13 shows Si 1s XPS spectra of (a) PDA samples of HMDS/La_2O_3/Si and (b) PMA samples of W/La_2O_3/Si. The interfacial layer growth of PMA is the almost same as PDA.

Figure 3.14 shows J_g at V_g = 1V versus EOT plots of W/La_2O_3/Si MOS capacitors with PDA and PMA. It is same EOT in PDA 500 ^oC and PMA 500 ^oC, but a large difference is seen in a leakage current. This result disagrees with a former argument that PMA film with a few defects is formed as compared with PDA. Perhaps, it may be caused by defect generation by reaction with W.

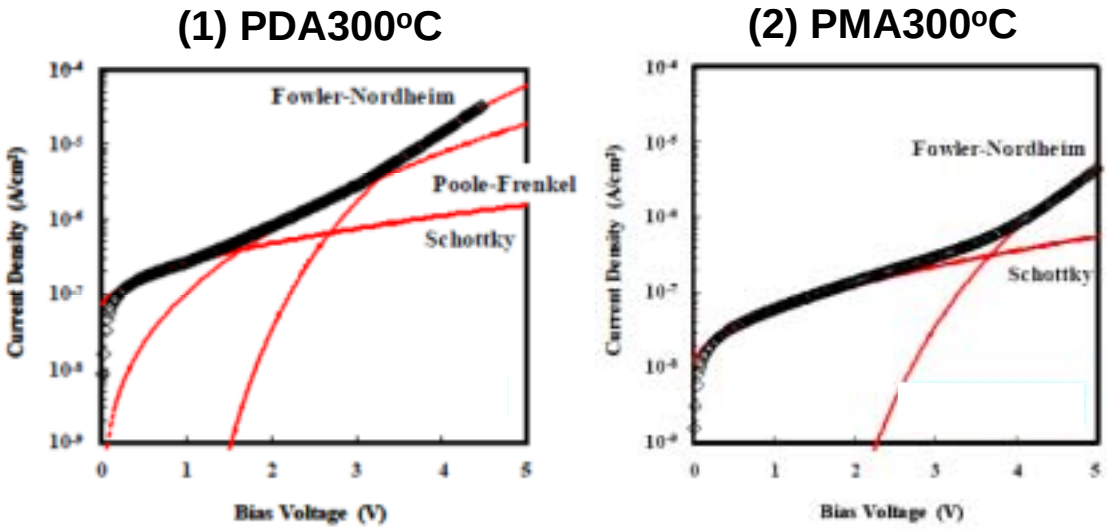


FIGURE 3.10 Leakage current mechanism of Pt/La2O3/Pt MIM-capacitors (a) PDA300^{o}C (b) PMA300^{o}C

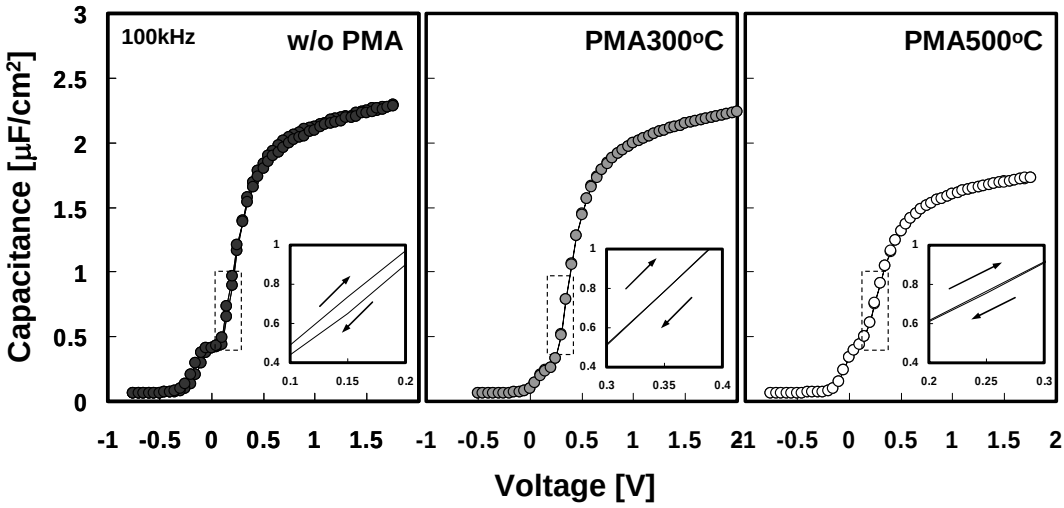


FIGURE 3.11 C-V curves showing the effect of PMA temperature at 300 ^{o}C and 500 ^{o}C in N_2. Insert figures are the expansion of a square dotted line. Capacitors are measured at 100 kHz.

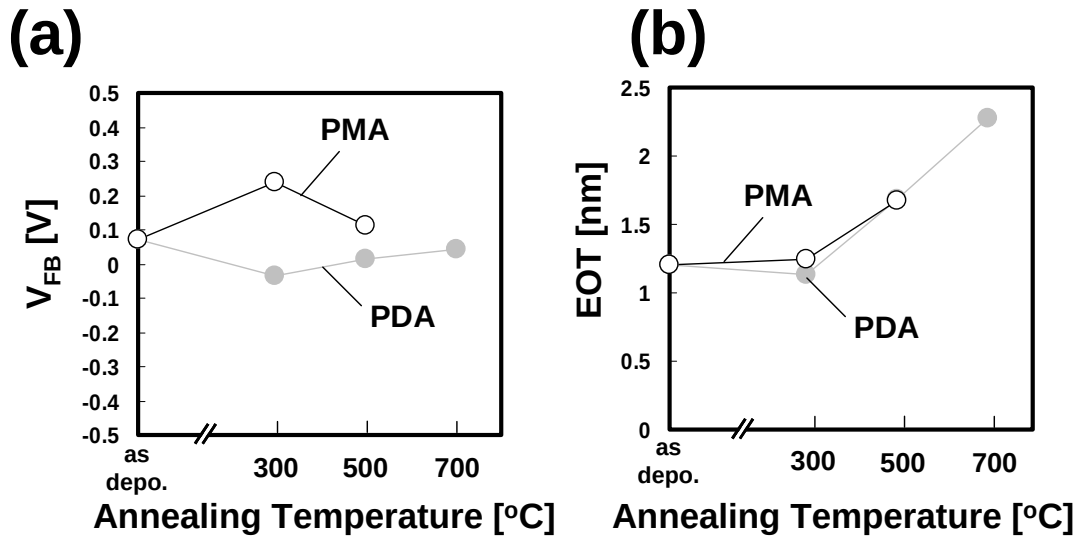


FIGURE 3.12 Annealing temperature dependence of (a) flatband voltage and (b) EOT.

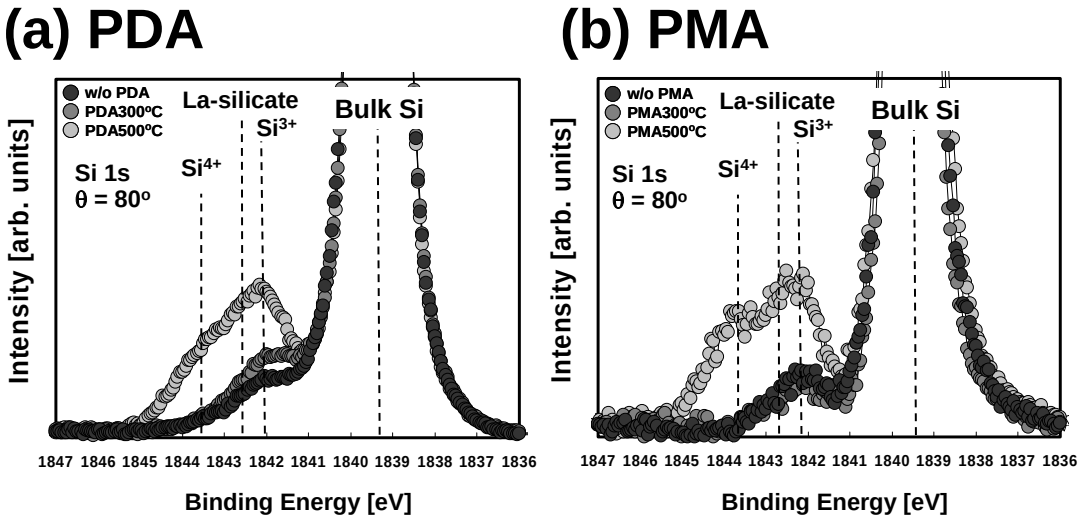


FIGURE 3.13 Si 1s XPS spectra of (a) PDA samples of HMDS/La_2O_3/Si and (b) PMA samples of W/La_2O_3/Si

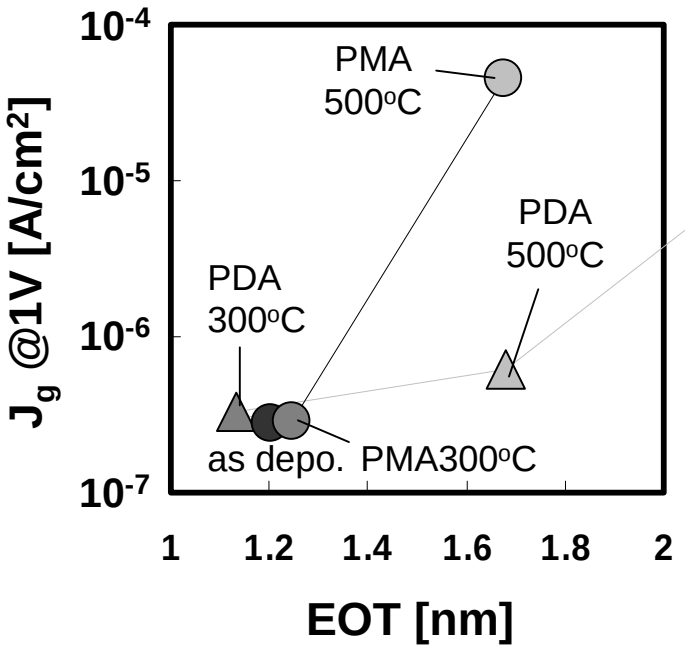


FIGURE 3.14 J_g at V_g = 1V versus EOT plots of W/La_2O_3/Si MOS capacitors with PDA and PMA.

3.3 SUMMARY

In this chapter, absorbed La_2O_3 was discussed. La_2O_3 transform into $La(OH)_3$ since La_2O_3 has strong absorption. This $La(OH)_3$ of the lower dielectric constant resolves into La_2O_3 by annealing at more than 300 ^oC. Meanwhile at La_2O_3/Si interface, the strong reaction is caused at 500 ^oC, and then La-silicate and SiO_x layer to lead to increase in EOT is formed. As far as the reduction of La_2O_3 and the growth of interfacial layer are concerned, PDA 300 ^oC is best condition.

In spite of the increase in EOT attended by PDA, the leakage current tends to be increased. This phenomena is discussed in terms of the crystallization by PDA and the defect generation by thermally resolving $La(OH)_3$ and the La_2O_3/Si interfacial reaction. As a result, the crystalline layer grows by increasing in PDA temperature. As compared with PMA which shut H_2O into La_2O_3 film, PDA 300 ^oC decrease in EOT, PMA, which shut H_2O into La_2O_3 film, do not decrease. Although PDA films have more defects than PMA from *C-V* characteristics, the leakage current of PDA is more. This may be related to the diffusion of W in La_2O_3. Seeing from a point of view to thermal stability, the difference was hardly seen in a change of EOT, but a PDA at 500 ^oC is better about a leakage current.

4

PROCESS OPTIMIZATION OF *IN-SITU* La_2O_3 PROCESS

4.1 INTRODUCTION

In chapter 3, the absorbed La_2O_3 was discussed. As a result, the most of effective dielectric constant is 18.9 contrary to theoretically ~27. This degradation attribute to the existence of $La(OH)_3$ and the interface reaction. Therefore, with the aim of avoiding the deterioration by absorbent, *in-situ* metallization proceeded without exposing La_2O_3 to air after La_2O_3 deposited. In this chapter, this *in-situ* sample is evaluated.

4.2 EFFECT OF *IN-SITU* La_2O_3 PROCESS

4.2.1 Properties of As-deposition

A structure of samples is W/La2O3/n-Si stack, and then *in-situ* metallization proceeded without exposing La_2O_3 to air after La_2O_3 deposited. Figure 4.1 shows C-V curve of W/La_2O_3/Si MOS-capacitors with *in-situ* and *ex-situ* metallization without annealing. The physical thickness of the *in-situ* La_2O_3 is 5.8 nm measured from cross-sectional Transmission Electron Microscope (TEM) image. An *ex-situ* samples with the same physical thickness as *in-situ* was used for comparison. The physical thickness of the *ex-situ* La_2O_3 was measured by spectroscopic ellipsometer. Although the same thickness, these accumulation capacitance differ largely. These *C-V* data yields an EOT = 0.99 nm and 1.20 nm with *in-situ* and *ex-situ*, respectively. The in-situ sample has large hysteresis. If this in-situ *C-V* is regarded as a characteristic of original La_2O_3, the absorption of H_2O decreases *C-V* hysteresis. It is thought that OH^- ions compensate for the oxygen vacancies of La_2O_3. For a same reason, the *in-situ* V_{FB} positively shift. Figure 4.2 shows these effective dielectric constants calculated from the EOT and physical thickness. The calculation method of dielectric constant is expressed in detail

in Section 5.21. The in-situ film has $\varepsilon_{in\text{-}situ} = 23.4$, compared to $\varepsilon_{ex\text{-}situ} = 18.9$ with ex-situ. Figure 4.3 shows the current density – voltage (J-V) data. The current of the in-situ sample is higher than the ex-situ in spite of the same physical thickness. It is probable that this higher current is caused by the harder electrical field due to larger ε_{eff} and the more defects.

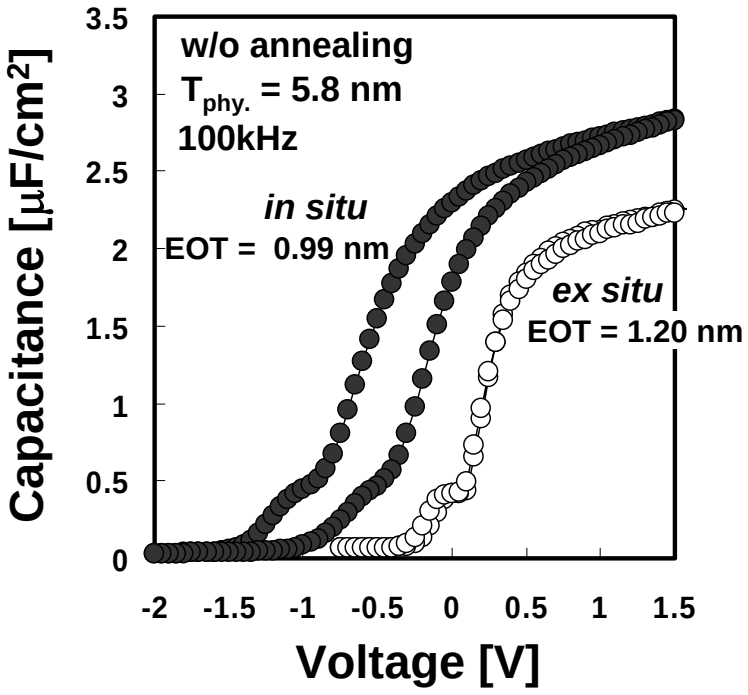


FIGURE 4.1 C-V curve of $W/La_2O_3/Si$ MOS-capacitors with *in-situ* and *ex-situ* metallization without annealing. Capacitance is measured at 100 kHz.

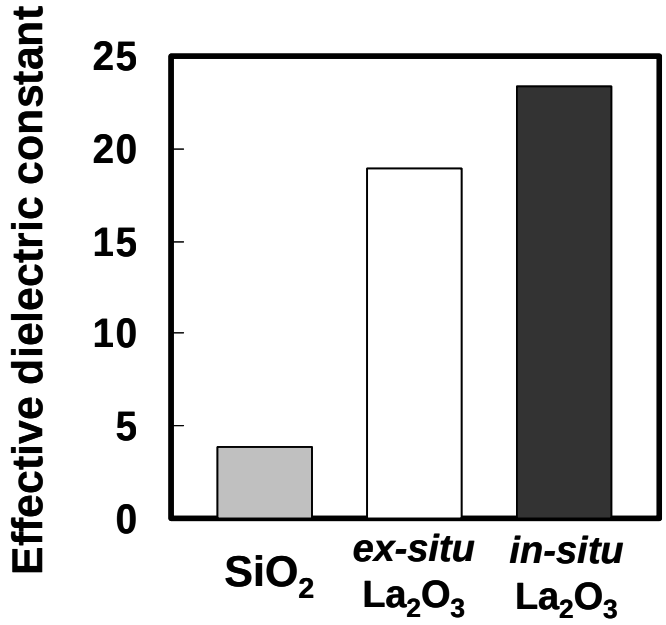


FIGURE 4.2 Difference of Effective dielectric constant of La_2O_3 on *in-situ* process from *ex-situ* process.

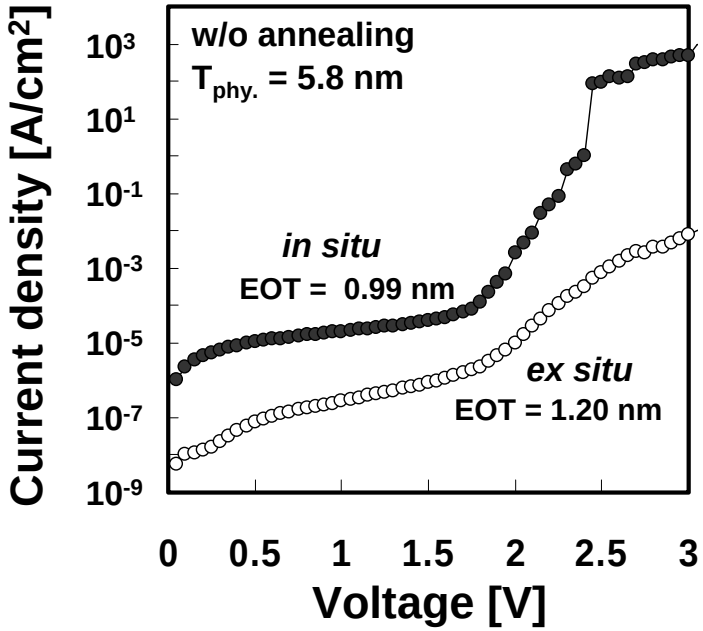


FIGURE 4.3 J-V characteristics of W/La_2O_3/Si MOS-capacitors with *in-situ* and *ex-situ* metallization without annealing.

4.2.2 Thermal Stability

In this section, a thermal stability of the in-situ sample is evaluated by PMA. Figure 4.4 shows the variation of *C-V* characteristics by annealing temperature of W/La_2O_3/Si MOS-capacitors with *in-situ* and *ex-situ* metallization. In *in-situ* samples, as PMA temperature increases, the accumulation capacitance and hysteresis decreases, and then the hump increases. It is though that all of these changes are caused by interface reaction. The capacitance diminution results from the growth of the lower dielectric constant layer. The hysteresis shrink is attributed to border traps decrease due to interface reaction. The hump growth probably means the reaction increase in the interface states. The EOT and V_{FB} calculated from these C-V data are shown as a function of PMA temperature in figure 4.5 (a) and (b), respectively. Compared to as-deposited and PMA 300 ^oC samples, the EOT difference between in-situ and ex-situ diminish at PMA 500 ^oC. It is thought that the reason is because the low dielectric constant layer formed by heat-treatment became dominant. The V_{FB} shifts by annealing for the *in-situ* capacitor is larger than the *ex-situ*. K. Shiraishi et al. reports that the oxygen vacancies near high-k/poly-Si interface cause Fermi-level pinning due to interface dipole formation [23]. In the *in-situ* capacitor without annealing, the large hysteresis represents the many existence of the oxygen vacancy near La_2O_3/Si. And it is possible that the interlayer growth by annealing decrease in the border traps, which decrease interface dipoles and make V_{FB} largely shift. In the *ex-situ* capacitor without annealing, on the other hand, almost nothing is the oxygen vacancies as a result of little hysteresis. Accordingly, V_{FB} shift by annealing is small. In addition, it can be seen that the *in-situ* PMA 500 ^oC has the V_{FB} that is about the same as *ex-situ*. Figure 4.6 shows J_g at V_g = 1V versus EOT plots of W/La_2O_3/Si MOS capacitors with various annealing

temperatures in *in-situ* and *ex-situ* process. In the case of the *in-situ* samples, the leakage current decrease by annealing with increasing in EOT. This result is contrary to the *ex-situ* samples. The effect that shut H_2O into the film may increase in the current.

Figure 4.7 shows difference between *in-situ* PMA and *ex-situ* PDA process in annealing temperature dependence of EOT. Both *in-situ* PMA and *ex-situ* PDA increase in EOT as annealing temperature increases. It is remarkable that EOT reverses in annealing of 700 ^{o}C. In figure 4.8, there is the cause of this reversal. Figure 4.8 is Si 1s spectra for (a) *in-situ* PMA, (b) *ex-situ* PMA, and (c) *ex-situ* PDA. With 500oC annealing, all process show the almost same in the interface reaction. However, a big difference appears in heat-treatment of 700 ^{o}C. The in-situ La_2O_3 exponentially reacts with Si substrate. This unusual growth of interfacial layer has EOT suddenly increasing. The leakage current also largely changes at PMA 700^{o}C for the in-situ sample in figure 4.9. The detailed current mechanism has not been investigated as yet, but it is clear that the current mechanism is different from other sample. Figure4.10 shows J_g at V_g = 1V versus EOT plots of various annealing temperatures in *in-situ* PMA and *ex-situ* PDA process. The current of the *in-situ* films is, on the whole, larger than the *ex-situ* films. In particular, the PMA 700 ^{o}C sample of the in-situ process has as large leakage current as the SiO_2 film. While OH^- ions have the dielectric constant declining, they may suppress the defects in the film.

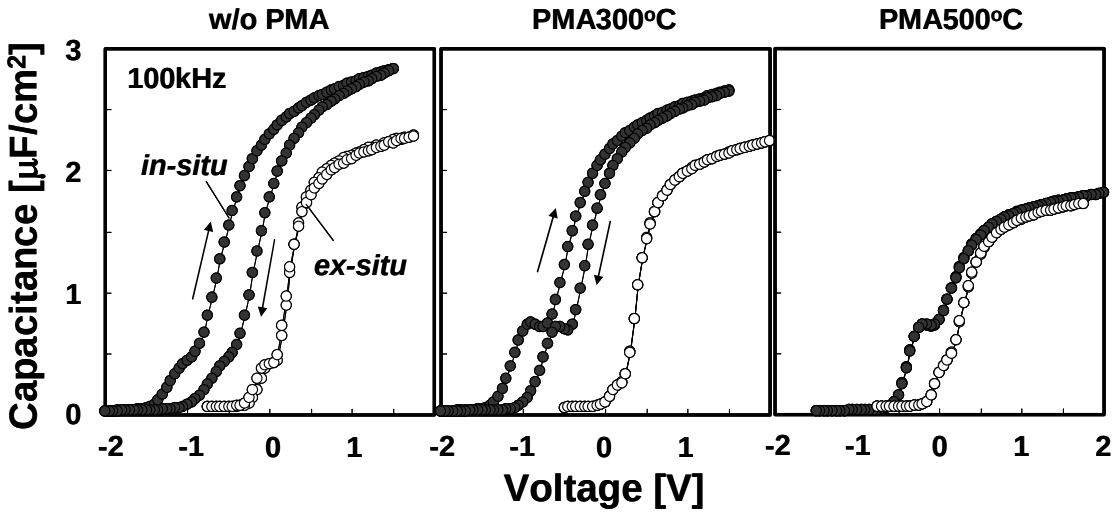


FIGURE 4.4 *C-V* curves dependence on annealing temperature of W/La_2O_3/Si MOS-capacitors with *in-situ* and *ex-situ* metallization.

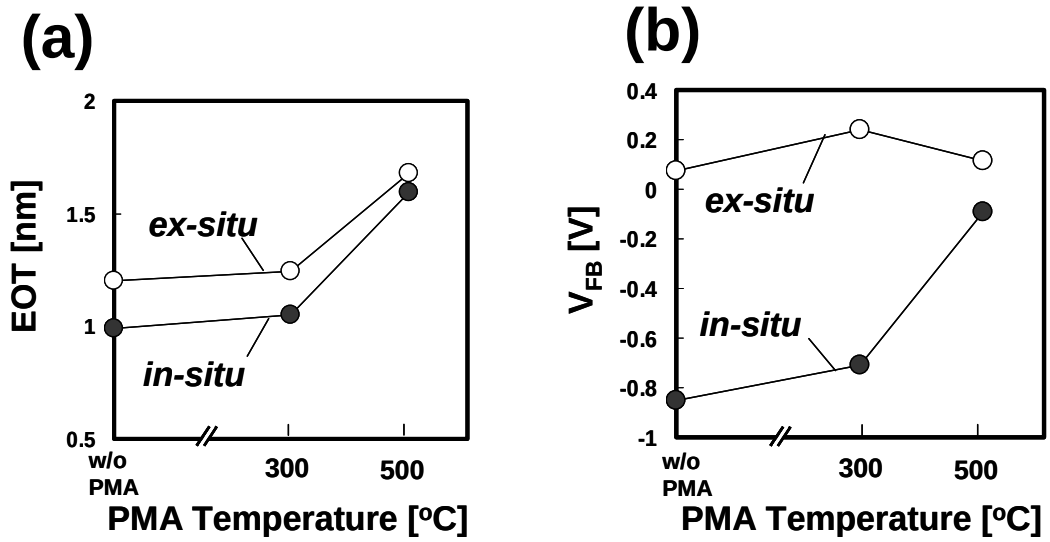


FIGURE 4.5 Annealing temperature dependence of (a) EOT and (b) flatband voltage.

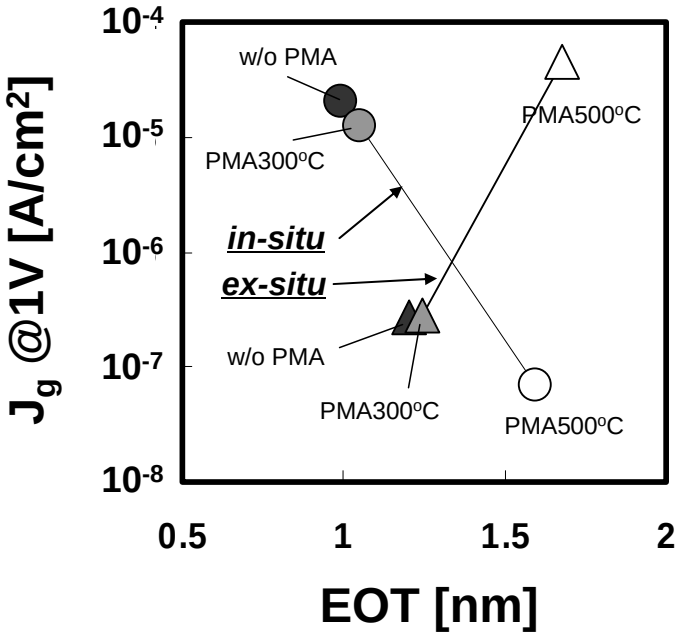


FIGURE 4.6 J_g at V_g = 1V versus EOT plots of W/La_2O_3/Si MOS capacitors with various annealing temperatures in *in-situ* and *ex-situ* process.

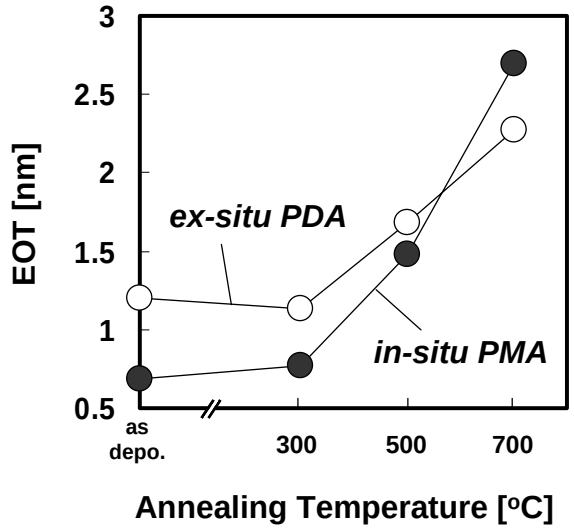


FIGURE 4.7 Difference between *in-situ* PMA and *ex-situ* PDA process in annealing temperature dependence of EOT

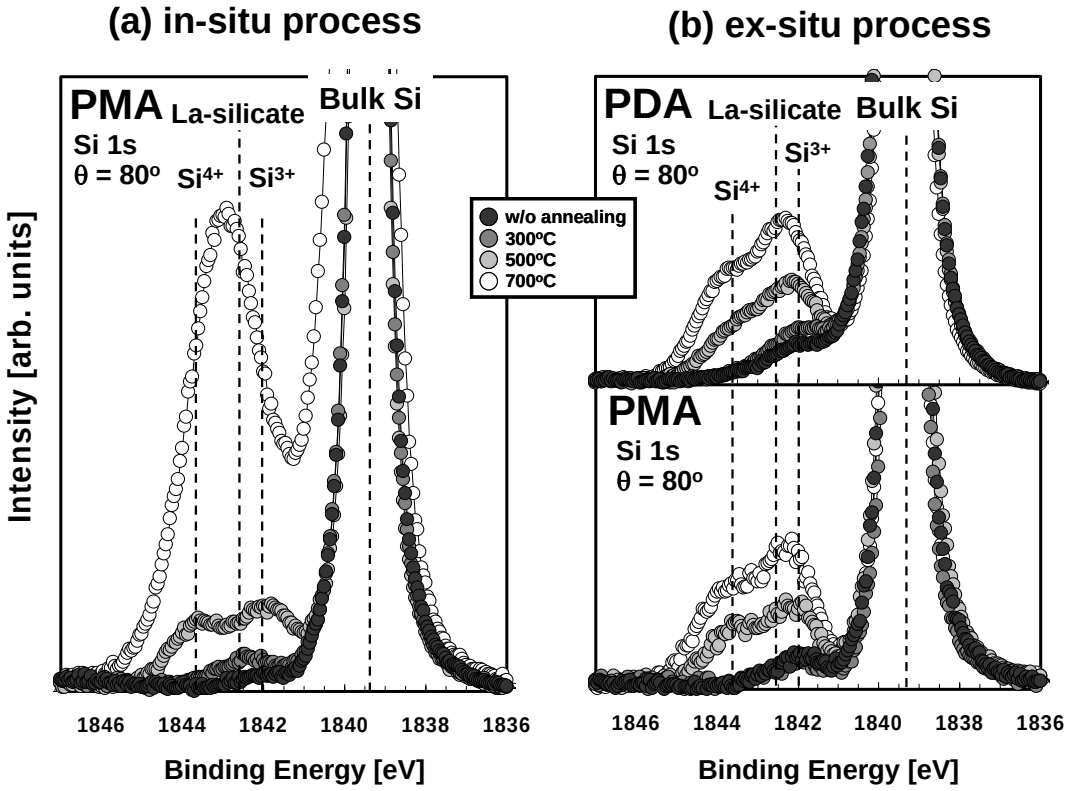


FIGURE 4.8 Difference of Si 1s XPS spectra between (a) *in-situ* PMA, (b) *ex-situ* PMA and *ex-situ* PDA process. The structures of *in-situ* PMA, *ex-situ* PMA, and *ex-situ* PDA sample are Pt/La_2O_3/Si, W/La_2O_3/Si, and HMDS/La_2O_3/Si, respectively.

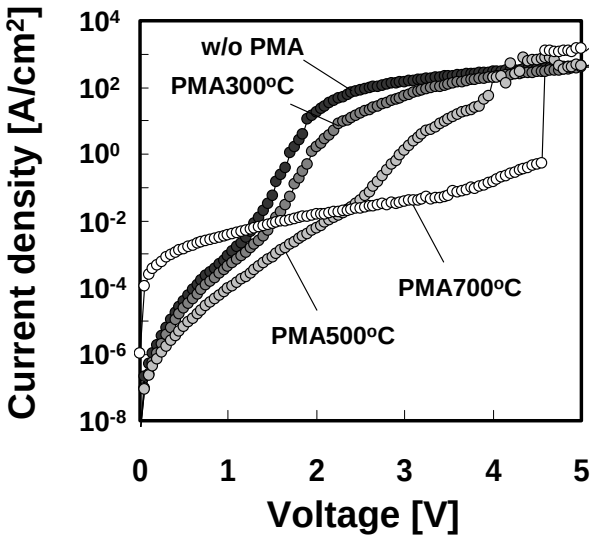


Figure 4.9 Difference of leakage current density in annealing temperatures with *in-situ* PMA.

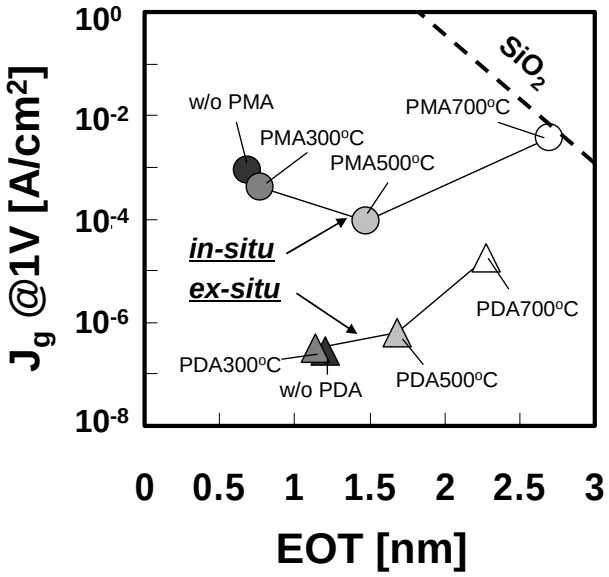


Figure 4.10 J_g at V_g = 1V versus EOT plots of various annealing temperatures in *in-situ* PMA and *ex-situ* PDA process.

4.3 SUMMARY

In this chapter, I evaluated the samples which *in-situ* metallization proceeded without exposing La_2O_3 to air after La_2O_3 deposited with the aim of avoiding the deterioration by absorbent. As a result, compared with ε_{eff} = 18.9 of the *ex-situ* La_2O_3, ε_{eff} = 23.4 of the *in-situ* is obtained. The defects in the film, however, increased. In a thermal stability, the exponential growth of the interfacial layer at 700 ^oC annealing was confirmed. This vastly increases EOT. This result means that OH^- ions may suppress the interface reaction. Finally, J_g at V_g = 1V versus EOT plots of various physical thicknesses with in-situ process is shown in figure 4.11. These plots suggest that the thermal treatment aggravate the device characteristics. In this study, the smallest EOT of this *in-situ* process is 0.47 nm, and then the leakage current at 1V is 6.4 x 10^{-3} A/cm^2.

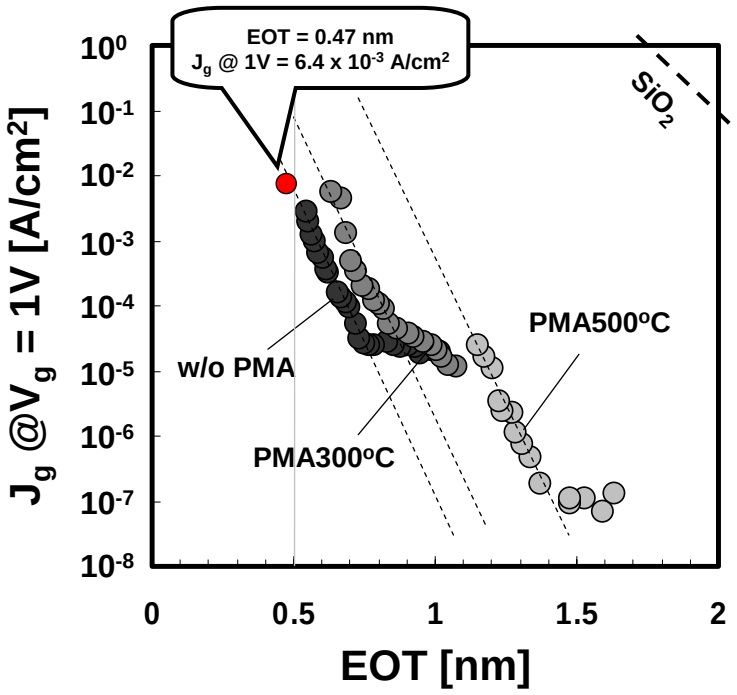


FIGURE 4.11 J_g at V_g = 1V versus EOT plots of various physical thicknesses with in-situ process.

5

EFFECT OF La_2O_3 DEPOSITION WITH FLOWING OXYGEN

5.1 INTRODUCTION

For high-*k* MOSFET, the poor drive current due to degraded field-effect carrier mobility is a major issue. To my knowledge, there has been no report on high-k dielectrics yielding field-effect mobilities matching those of the universal curves [24] generally observed for high-quality SiO_2. The degraded mobility generally observed for high-k dielectrics has been attributed to higher interface-state density D_{it}, higher fixed-charge density, or electron wave-function penetration due to a lower barrier height as compared with SiO_2. It is interesting to note that if interface charge trapping is taken into account, the field-effect mobility for a high-k dielectric can be very close to that of the universal mobility curve for SiO_2 [25]. Typical HfO_2 films exhibit hysteresis in *C-V* characteristics due to charge trapping by near-interface traps. Even in the best case, the hysteresis of 1.3 nm EOT HfO_2 amounts to >20 mV, corresponding to an area trap density >2 x 10^{11} cm^{-2}. [26] Hence, traps likely play a significant role in the degradation of carrier mobility [27].

According to John Robertson, SiO_2 has such a low defect concentration for two reasons. First, its large heat of formation (large Si–O bond strength) means that off-stoichiometry defects such as O vacancies are costly and so they are rare. The second is that SiO_2 has a low coordination. Its covalent bonding means that the main defects are dangling bonds, and the low coordination allows the SiO_2 network to relax to remove any dangling bonds by re-bonding the network. This occurs particularly for defects at the Si/SiO_2 interface.

The high-k oxides differ from SiO_2 in that their bonding is ionic and they have a higher coordination number [28]. The more ionic bonding and higher coordination numbers mean that the high-k oxides are poorer glass formers. The effect of poor

glass-forming ability and high coordination is that the oxides have larger non-equilibrium defect concentrations. The oxides still have high heats of formation, so the equilibrium defect concentrations should be low. However, the non-equilibrium defect concentration is high because the oxide network is less able to relax to re-bond and remove defects.

As a result of Chapter 4, the MOS-capacitor for the *in-situ* process possesses the larger dielectric constant than the ex-situ, while the in-situ La_2O_3 has more defects. The film of low quality causes the increase of C-V hysreresis and the degradation of thermal stability. The La_2O_3/Si interface reaction may have to do with oxygen vacancy. In this chapter, for the purpose of decreasing in oxygen vacancy in La_2O_3 deposition, I experimented with in La_2O_3 deposition in a trace of oxygen gas.

5.2 EFFECT OF La_2O_3 DEPOSITION WITH FLOWING OXYGEN

A trace of oxygen was introduced into the chamber during the La_2O_3 deposition, which set the oxygen partial pressure to 1 x 10^{-5} Pa, 7 x 10^{-4} Pa, and 3 x 10^{-3} Pa.

5.2.1 Evaluation of Interface Reaction

Figure 5.1 shows cross-sectional TEM images of as-deposited La_2O_3 MOS capacitors (a) without and (b) with oxygen flow. A sharp interface between La_2O_3 and Si was obtained with capacitor without oxygen supply, while interfacial layer (IL) formation was clearly observed when oxygen was introduced. The thickness of the formed IL was estimated to be 1.7 nm out of the total thickness of 5.2 nm. EOT obtained from measured C-V characteristics with fitting was 1.05 nm. By treating this binary layer structure as two capacitors in series, we have

$$EOT = \frac{\varepsilon_{ox}}{\varepsilon_{IL}} PT_{IL} + \frac{\varepsilon_{ox}}{\varepsilon_{La2O3}} PT_{La2O3}, \qquad (5.1)$$

where ε_{ox}, ε_{IL} and ε_{La2O3} are the dielectric constant of SiO_2, interfacial layer and La_2O_3, respectively, and PT_{IL} and PT_{La2O3} is the physical thickness (PT) of interfacial layer and La_2O_3, respectively. The relation between EOT and total physical thickness is given by

$$EOT = \frac{\varepsilon_{ox}}{\varepsilon_{La2O3}} PT + \left(1 - \frac{\varepsilon_{IL}}{\varepsilon_{La2O3}}\right) EOT_{IL} \quad [29]. \qquad (5.2)$$

Figure 5.2 shows that nothing is interfacial layer for the sample without flowing oxygen as well as cross-sectional TEM image. From equation (5.2) and the slope of Figure 5.2, we obtain ε_{La2O3} 23.4. By using this value, I can also estimate ε_{IL} 14.4 from equation (5.1). The interfacial layer EOT_{IL} is 0.43nm from the intercept of equation (5.2).

XPS measurement was performed on as-deposited La_2O_3 film with and without

flowing oxygen. Figure 5.3 shows Si 1s spectra. The formation of La-silicate is confirmed in sample with oxygen.

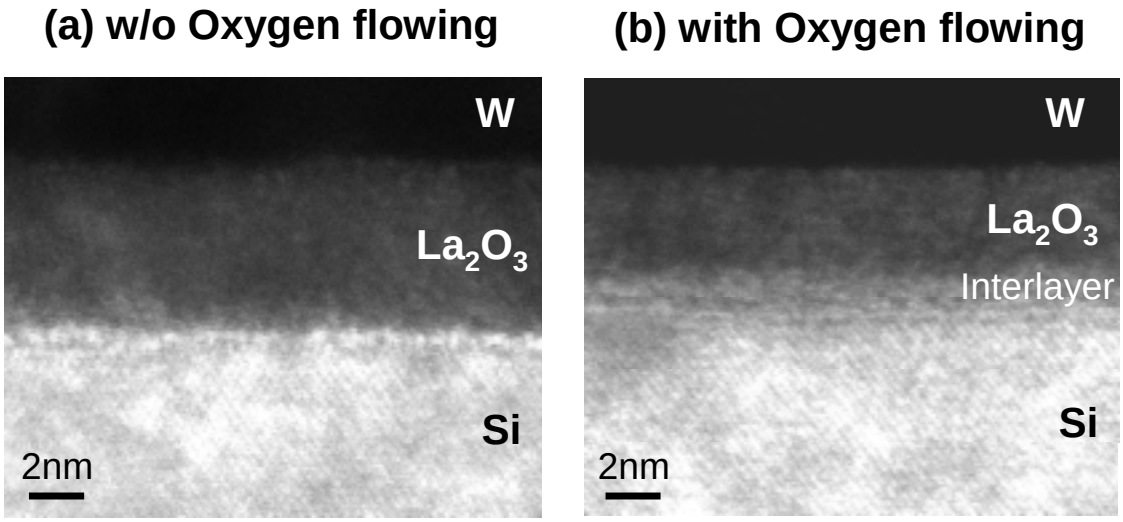


FIGURE 5.1 Cross-sectional TEM images of La_2O_3 as-deposited (a) without and (b) with flowing oxygen. The interfacial layer is observed with oxygen flow, and then the dielectric thickness is indicated in each image.

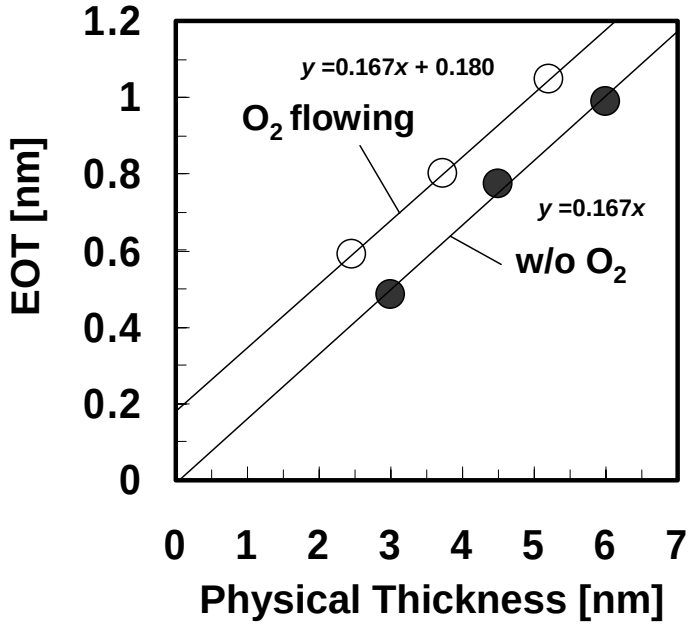


FIGURE 5.2 EOT versus physical thickness showing with and without oxygen flow. Both plots are linear relationship, but y-intercept is different.

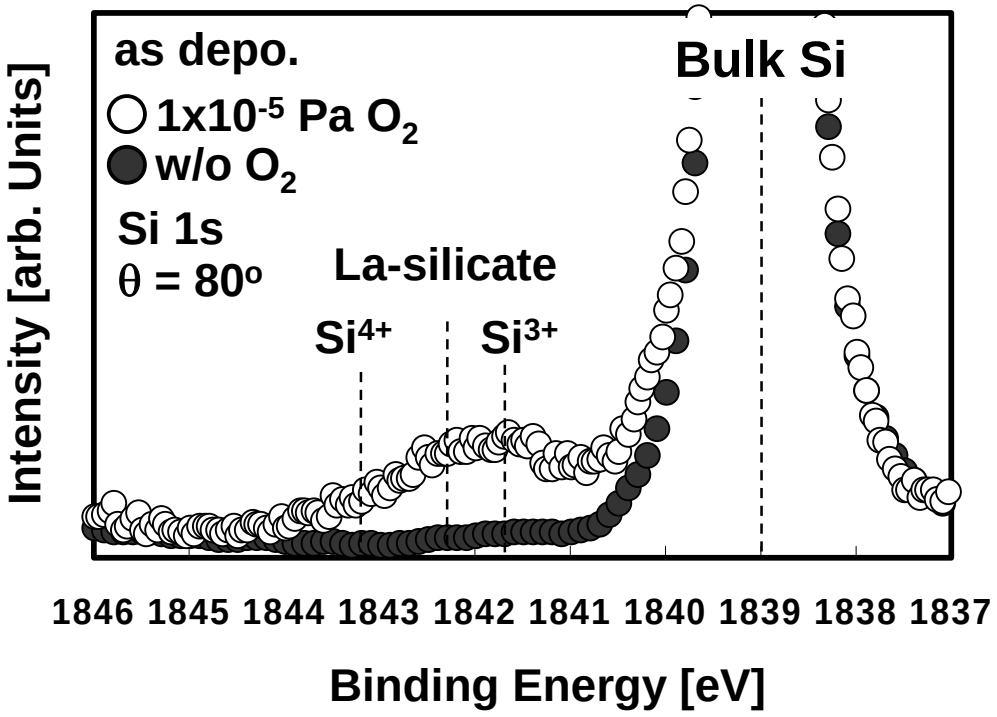


FIGURE 5.3 XPS Si 1s spectra of the W/La_2O_3/Si system prepared under La_2O_3 deposited with flowing oxygen and Pt/La_2O_3/Si without oxygen.

5.2.2 Evaluation of Defects from Leakage Current Conduction Mechanism

In this section, the defects in La_2O_3 are evaluated from the leakage current conduction mechanism. We have considered different conduction mechanisms: Schottly conduction, Poole-Frenkel (P-F) conduction, and Fowler-Nordheim (F-N) conduction, the current density is expressed as a function of the oxide electric field. Figure 5.4 show conduction mechanisms plots on W/La_2O_3/Si MOS-capacitors deposited with and without flowing oxygen. Their current density is measured at room temperature. Both samples conduction mechanism is Schottly conduction, P-F conduction, and F-N conduction mechanism. At low voltage from 0 V to 1.1 V, Schottky conduction mechanism was shown due to La_2O_3/Si interface has high barrier height. The P-F conduction is fitted well in two applied voltage ranges: no oxygen supplying sample is from 1.1 V to 1.9 V and oxygen supplying sample is from 1.1 V to 1.7 V. No oxygen supplying sample is dominated by P-F conduction at wider range than another one. The F-N conduction is also fitted well in two applied voltage ranges: no oxygen supplying sample is from 1.2 V to 2.0 V and oxygen supplying sample is from 1.5 V to 1.9 V. Since no oxygen supplying sample has smaller EOT than another sample, F-N conduction, which is tunneling conduction, is observed at lower voltage.

Leakage current of fabricated W/La_2O_3/Si MOS capacitors were measured at various temperature. Large leakage current dependence on temperature suggests Poole-Frenkel emission, which follows the relation:

$$In\left(\frac{J_{PF}}{E_i}\right) = \ln(A) + \frac{-q\Phi_{PF} + q\sqrt{qE_i/\pi\varepsilon_i}}{k}\frac{1}{T}, \qquad (5.3)$$

where A is proportional factor, T is measured temperature, E_i is electric field applied to insulator, ε_i is insulator permittivity, q is electronic charge, k is Boltzmann's constant, and $q\Phi_{PF}$ is barrier height of contributory defect to carrier conduction [7]. Figure 5.5 (a) and (b) shows J-V characteristics measured at various temperatures on the films with and without oxygen flowing during La_2O_3 deposited. As the measured temperature increasing, both leakage currents increase at their voltage ranges which P-F conductions are observed in Figure 5.4 (b). Figure 5.6 shows the Arrhenius plot on measured leakage current density at 1.0V above the flatband voltage of La_2O_3 film with and without oxygen. The strait relation reveals that the conduction mechanism is P-F emission. A barrier height of 0.13 eV can be estimated with oxygen supplied La_2O_3. On the other hand, two barrier heights of 0.44 and 0.66 eV were obtained with no oxygen supplied. This difference of trapping levels below the La_2O_3 conduction band edge may be explained as arising from the electron trapping or de-trapping between the intrinsic and charged oxygen vacancy states. John Robertson report oxygen vacancy states in La_2O_3 by calculating (Figure 5.7) [28]. V^{2+} occupies an energy level of about 1.1 eV below the La_2O_3 conduction edge. This vacancy can be filled with electrons injected from the substrate. After capturing an electron (V^+) it relaxes by about 0.3 eV to 1.4 eV. Further electron capture will relax by another 0.3 eV to 1.7 eV below the conduction band edge of the dielectric. Their calculated values are larger than these experimental values. But the interval of their values is close to the calculation value of 0.3 eV. I do not know the cause of their differences. Perhaps the interfacial layer on La_2O_3 with flowing oxygen may be related to this matter. In the least, the decrease of trap level by supplying oxygen may mean that the oxygen vacancies thinned as little dependence on temperature.

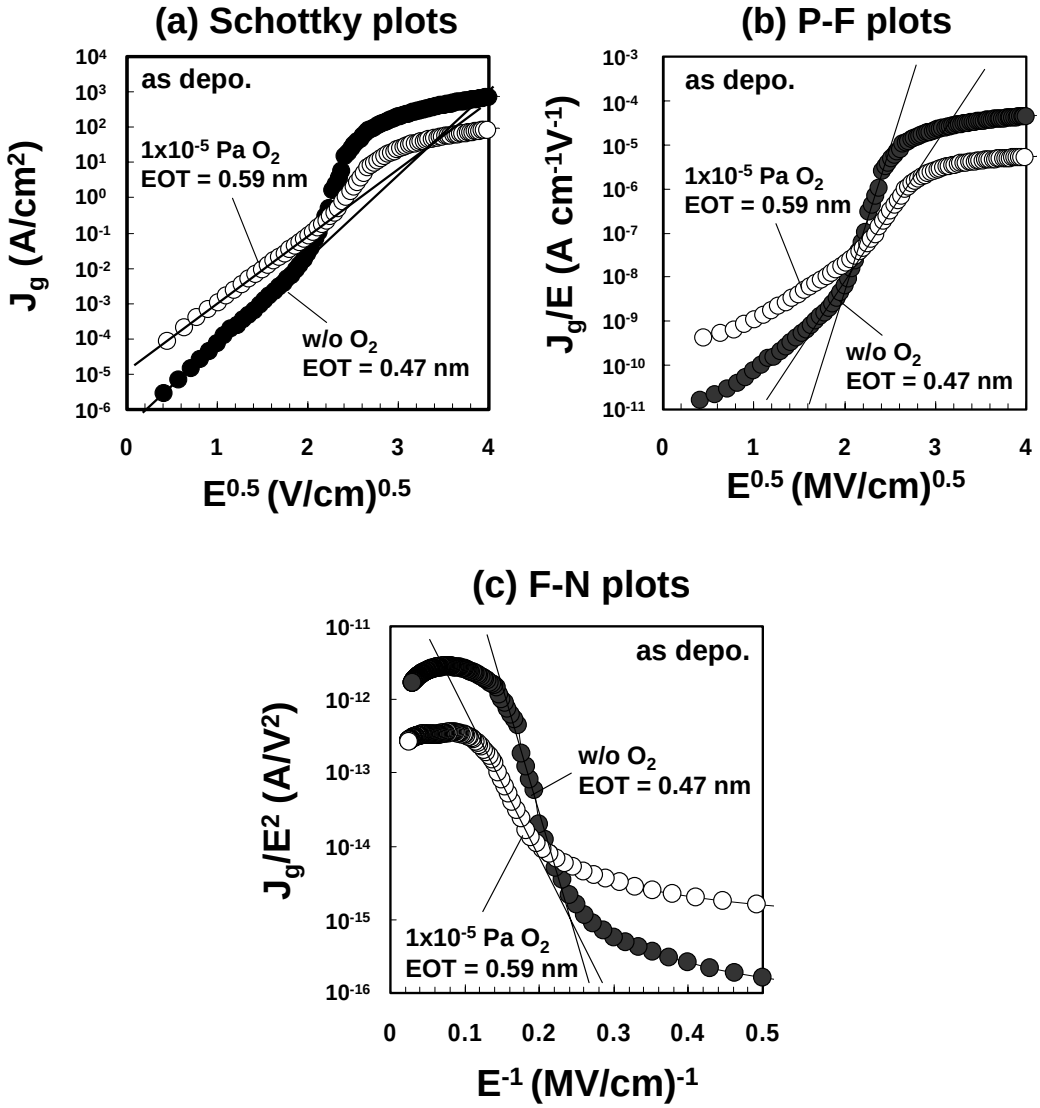


FIGURE 5.4 Carriers conduction mechanism of samples on La2O3 deposited with and without oxygen. (a) Schottky plots, (b) Poole-Frenkel plots, and (c) Fowler-Nordheim plots.

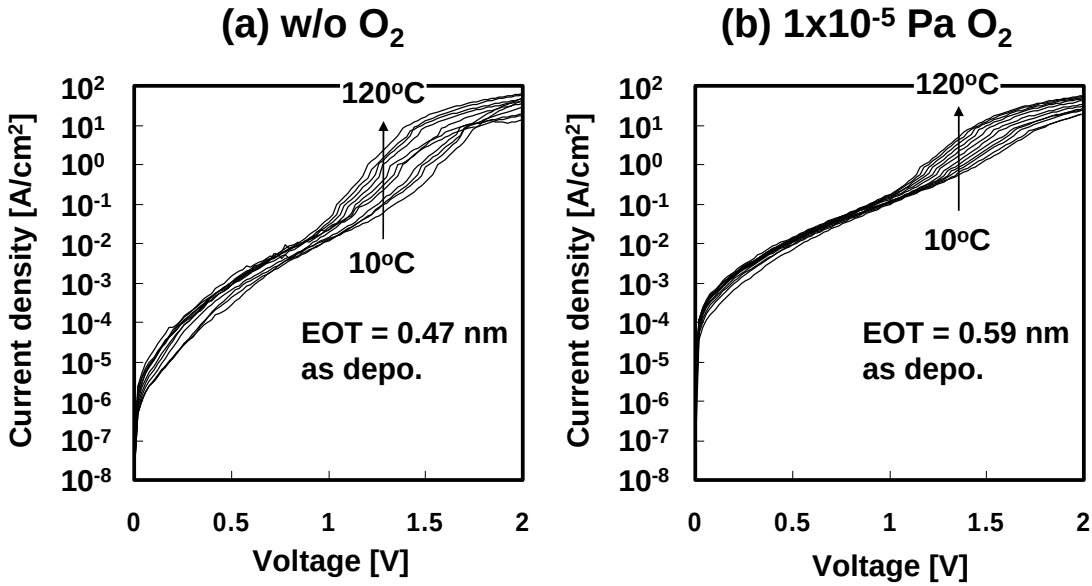


FIGURE 5.5 J-V characteristics measured at various temperatures on the films (a) without and (b) with oxygen flowing during La_2O_3 deposited.

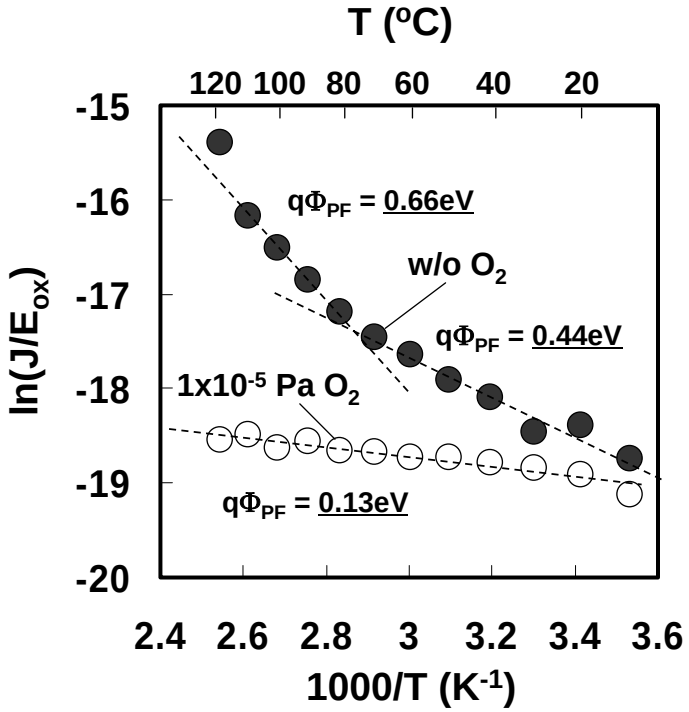


FIGURE 5.6 Arrhenius plot of current density at different deposition condition of La_2O_3. On each temperature, the current density at the gate voltage which the constant electric field was applied to insulator was plotted.

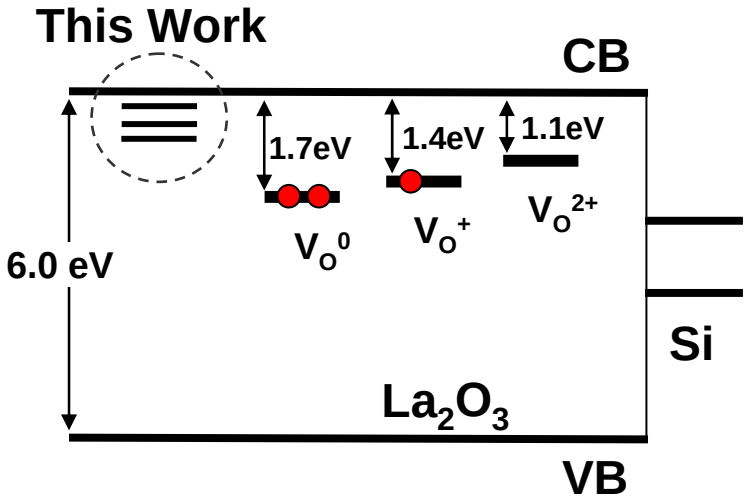


FIGURE 5.7 Molecular orbital diagram of relaxed oxygen vacancy in La_2O_3 in various charge states by John Robertson and these experimental results.

5.2.3 Dependence on Partial Oxygen Pressure

In this section, it is investigated that what kind of influence the oxygen quantity in deposition chamber gave. The prepared samples is W/La_2O_3/n-Si MOS capacitors, La2O3 was deposited with flowing oxygen at 1 x 10^{-5} Pa, 7 x 10^{-4} Pa, or 3 x 10^{-3}Pa. Figure 5.8 shows *C-V* characteristics of La_2O_3 deposited under various oxygen partial pressures. These samples are MOS-capacitors made by the *in-situ* process without annealing, and then they are the same quantity of La_2O_3 evaporated which was controlled by quartz oscillator in the deposition chamber. A change of C-V curve by increase of oxygen partial pressure is three points of the following.

① a decrease in accumulation capacitor

② a growth of "hump"

③ a reduction of hysteresis

Below is the consideration for these changes. First, a decrease in accumulation capacitance is deliberated. Figure 5.9 shows EOT as a function of oxygen partial pressure. The increase of EOT, that is to say the decrease of capacitance, is caused by the growth of the interfacial layer whish is dependent on oxygen pressure. Second, it is examined that "hump" grow by supplying oxygen. Figure 5.10 shows the interface trap density (D_{it}) as a function of the trap energy within the band gap of silicon, which was measured by conductance method. D_{it} increase with high oxygen pressure. This increase accords the growth of hump. It is probable that this result from the formation of Si dangling bonds by reacting at La_2O_3/Si interface. Even in the sample without oxygen, however, the D_{it} amount to >1 x 10^{-12} cm^{-2} eV^{-1}. The Si substrate surface before La_2O_3 deposition is terminated by hydrogen, while this hydrogen leaves Si of the surface by heating the substrate. In gradually, a post metallization or "final" anneal in hydrogen or

in a hydrogen-containing ambient, at temperatures around 400 oC is quite effective in minimizing the density interface traps [1]. Figure 5.11 shows C-V characteristics measured at various frequencies for La_2O_3 MOS-capacitor annealed at 420 ^oC for 30 min in 3%-H_2+N_2 (forming gas, FG). Against expectation, the hump remains large. Perhaps, since the hydrogen is taken in La_2O_3, Si dangling bond stay behind FG annealing. Third, the influence of the deposition conditions on *C-V* hysteresis was also investigated. For the no oxygen supplying sample, hysteresis due to the border traps is clearly seen, and the trap density is estimated [30] to be ~ 6.4 x 10^{12} cm^{-2}, whereas the remarkably reduced hysteresis is evident for La_2O_3 deposition sample with oxygen pressure of 3 x 10^{-3} Pa, and the trap density is estimated to be as small as ~ 9.5 x 10^9 cm^{-2} in figure 5.12. Figure 5.13 shows (a) normalized *C-V* curves and (b) V_{FB} shift as a function of oxygen partial pressure. Forward *C-V* curves is the almost same except these hump. In common, "stretching" of *C-V* curve is well known as the influence of interface traps [31]. These samples, however, have no change by stretching of *C-V* curve though D_{it} change with oxygen pressure. I can not understand this reason. In figure 5.13 (b), a small positive shift of V_{FB} with increase in oxygen pressure is because the positive fixed charge, which is probably oxygen vacancy, decrease. Finally, J_g at 1V versus EOT plots is shown in figure 5.14. Although EOT and physical thickness increase by a growth of interfacial layer, the leakage current does not change except the sample which is highest oxygen pressure. This result is contrary to the reduction of oxygen vacancies which can become trap sites. The leakage current may be concerned with interface traps.

As a result, the supplying oxygen grows in interfacial layer, increase in EOT, and make interface trap, on the other hand, decrease in oxygen vacancies.

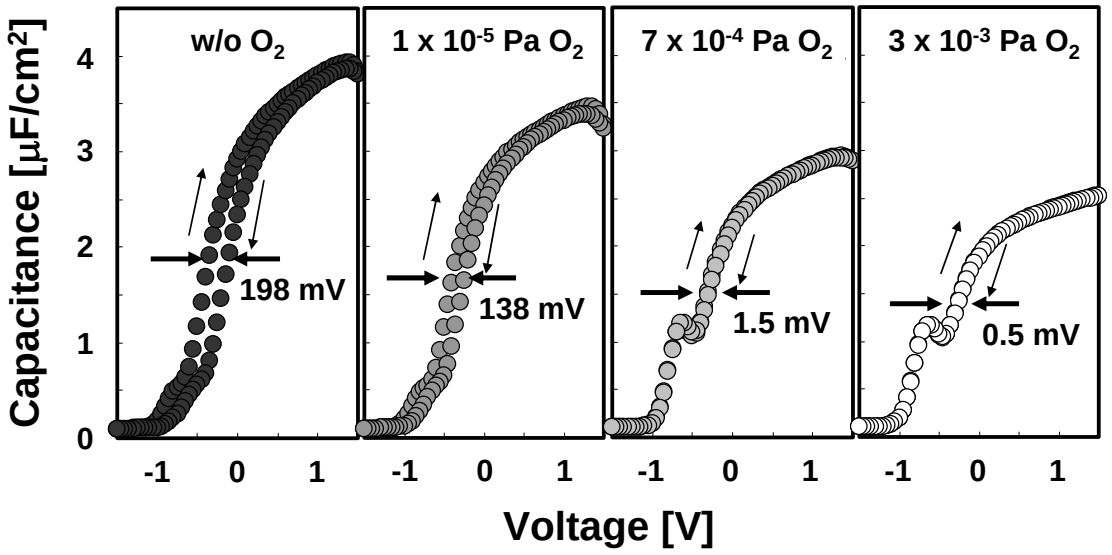


FIGURE 5.8 C-V characteristics of La_2O_3 deposited under various oxygen partial pressures. Capacitance is measured at 100 kHz.

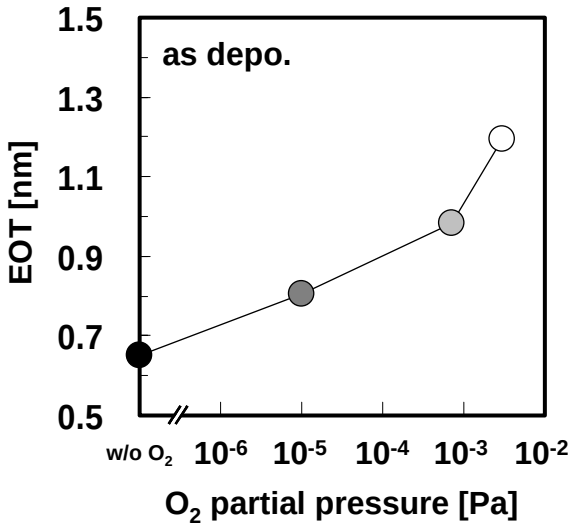


FIGURE 5.9 Variation of EOT with oxygen partial pressure. EOT is increased by supplying oxygen.

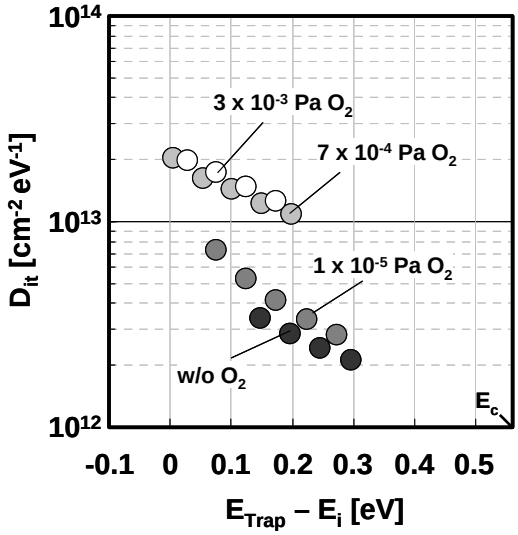


FIGURE 5.10 Distribution of the interface trap density D_{it} as a function of the trap energy within the band gap of silicon.

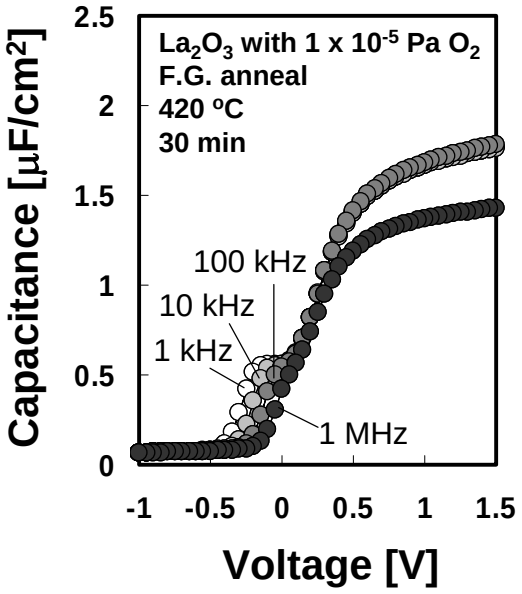


FIGURE 5.11 Effect of PMA in forming gas at 420 °C for 30 min. La_2O_3 is deposited with oxygen pressure of 1 x 10^{-5} Pa.

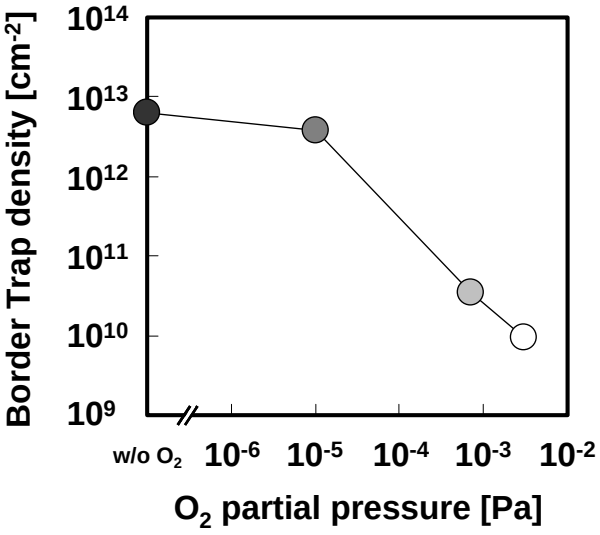


FIGURE 5.12 Effect of PMA in forming gas at 420 ^{o}C for 30 min. La_2O_3 is deposited with oxygen pressure of 1 x 10^{-5} Pa.

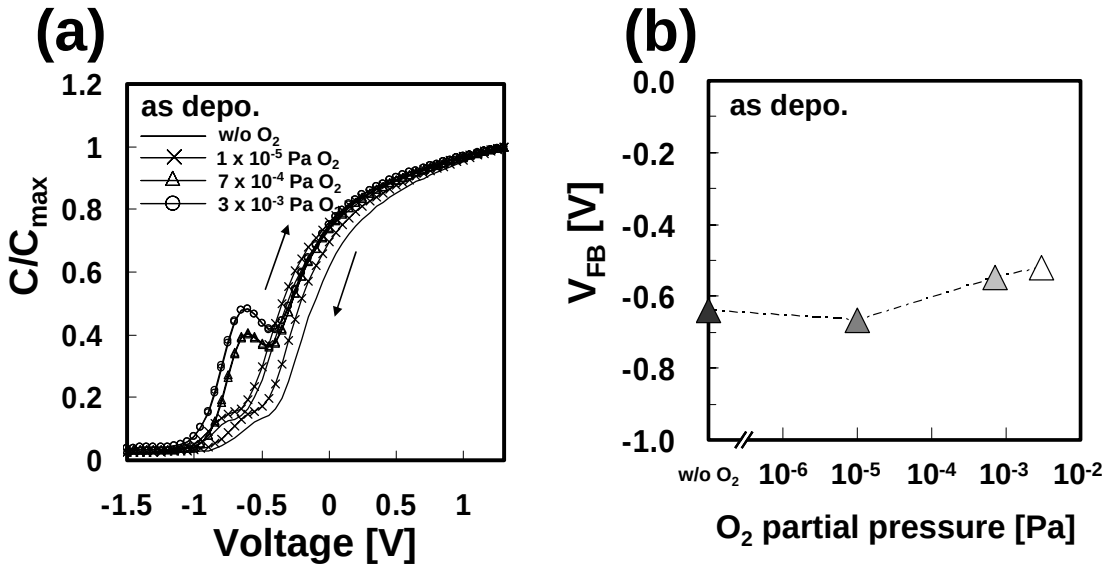


FIGURE 5.13 (a) Normalized C-V characteristics of La_2O_3 deposited under various oxygen partial pressures. (b) Flatband voltage as a function of oxygen partial pressure.

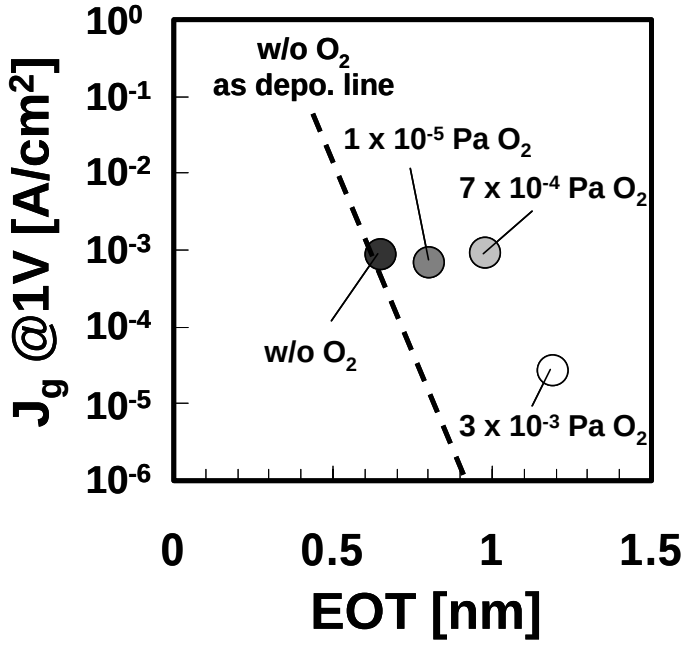


FIGURE 5.14 J_g at V_g = 1V versus EOT plots of W/La_2O_3/Si MOS capacitors with various oxygen partial pressure.

5.2.4 Evaluation of Thermal Stability

In this section, the thermal stability with the sample supplying oxygen is investigated. Figure 5.15 shows EOT of La_2O_3 deposited with various oxygen partial pressures as a function of PMA temperature. PMA was performed at 300 ^oC, 500 ^oC, and 700 ^oC for 5 min in nitrogen. With high oxygen pressure, the thermal stability is slightly improved at PMA700 ^oC. The interfacial layer by flowing oxygen may suppress the interfacial layer growth by annealing. But, as a whole, EOT largely increase at 500 ^oC and 700 ^oC.

Figure 5.16 shows the Dit as a function of annealing temperature. Dit is exacted by conductance method, estimated D_{it} extrapolated to midgap. The sample of without flowing oxygen and annealing have the lowest D_{it}. In addition to flowing oxygen, Dit increase by annealing at 300 ^oC. PMA 500 ^oC decrease in D_{it}. In 700 oC annealing, which exponentially react at interface, D_{it} is more than 2 x 10^{-13} cm^{-2} eV^{-1} in all sample. Too much D_{it} is one of the most serious problems for high performance MOSFET.

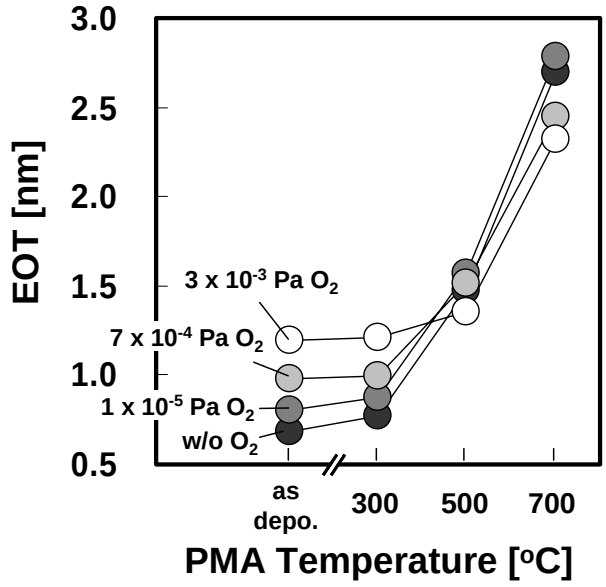


FIGURE 5.15 EOT of La_2O_3 deposited with various oxygen partial pressure as a function of PMA temperature.

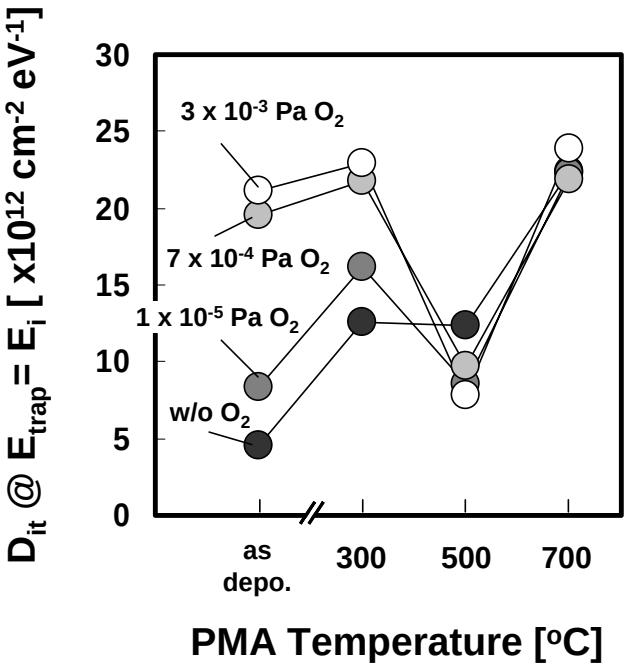


FIGURE 5.16 Interface trap density (D_{it}) of La_2O_3 deposited with various oxygen partial pressure as a function of PMA temperature. Estimated D_{it} extrapolated to midgap.

5.3 SUMMARY

The La_2O_3 film with in-situ process has many defects. In this chapter, for the purpose of decreasing in oxygen vacancy in La_2O_3 deposition, I experimented with in La_2O_3 deposition in a trace of oxygen gas. As a result, the supplying oxygen grows in interfacial layer, increase in EOT, and make interface trap, on the other hand, decrease in oxygen vacancies. In addition, the growth of the interfacial layer whish is dependent on oxygen pressure, and then EOT increase. The traps in La_2O_3 film have the two trapping levels of 0.44 eV and 0.66 eV below the La_2O_3 conduction band edge. In the case of supplying oxygen, this trap level decrease to 0.13 eV. With high oxygen pressure, the thermal stability is slightly improved at PMA700 ^{o}C, but D_{it} increase.

6

CONCLUSION

In this thesis, various problems had La_2O_3 film for the downscaling are investigated. In Chapter 6, the studies referred to in this thesis are summarized and their importance is described.

a) Process optimization of absorbed La_2O_3 (Chapter3)

La_2O_3 having strong absorption form $La(OH)_3$ in air. This $La(OH)_3$ of the lower dielectric constant resolves into La_2O_3 by annealing at more than 300 ^oC. Meanwhile at La_2O_3/Si interface, the strong reaction is caused at 500 ^oC, and then La-silicate and SiO_x layer to lead to increase in EOT is formed.

In spite of the increase in EOT attended by PDA, the leakage current tends to be increased. This phenomena is discussed in terms of the crystallization by PDA and the defect generation by thermally resolving $La(OH)_3$ and the La_2O_3/Si interfacial reaction.

b) Process optimization of in-situ La_2O_3 process (Chapter4)

Compared with ε_{eff} = 18.9 of the *ex-situ* La_2O_3, ε_{eff} = 23.4 of the *in-situ* is obtained. The defects in the film, however, increased. In a thermal stability, the exponential growth of the interfacial layer at 700 ^oC annealing was confirmed.

c) Effect of La_2O_3 deposition with flowing oxygen (Chapter5)

The supplying oxygen grows in interfacial layer, increase in EOT, and make interface trap, on the other hand, decrease in oxygen vacancies. With high oxygen pressure, the thermal stability is slightly improved at PMA700 ^oC, but D_{it} increase.

FOR FUTURE WORKS

La_2O_3 was the difficult material due to strong absorption. It is necessary that an in-situ gate metallization process is adopted for maintaining the high dielectric constant. However, in this study, the degradation of the film quality is hard, and some breakthrough will be needed for high performance La_2O_3 CMOS application.

The problem of La2O3 next to absorption is the poor thermal stability. I think throughout this study that it is impossible to prevent La2O3/Si interface reaction by heat-treatment. To my knowledge, there are two approaches for the solution. One is to innovate other material in La2O3 or between La2O3 and Si substrate. At present, various materials are investigated in the world. Y2O3 and Sc2O3 may designate better thermal stability because of larger Gibbs free energy than La2O3 [32]. But the mixing or insert will cause EOT increase. Another is the reduction of the grown interfacial layer by heat-treatment. This is virtually unexplored methods. This should pay attention to it as an investigation object.

In conclusion, the original studies referred to in this thesis were useful and timely in the successive technology generations of Si semiconductor, contributing to the realization of high-performance and highly reliable CMOS integrated circuits during the past 20 years. They are also expected to contribute to the future progress of LSIs.

REFERENCES

[1] Y. Taur and T. Ning, Fundamentals of Modern VLSI devices, Cambridge, 1998

[2] International Technology Roadmap for Semiconductors (ITRS), 2006 up date

[3] P.W. Peacock and J. Robertson, "*Band offsets and Schottky barrier heights of high dielectric constant oxides"*, *J. Appl. Phys.*, **92**, 4712 (2002).

[4] Y. Kuroki, "Novel Gate Stack and Process Optimization for La_2O_3-MOSFET" Tokyo Tech. master thesis (2006)

[5] Dieter K. Schroder, Semiconductor Material and Device Characterization 3rd Edition, John Wiley & Sons Inc., 2005

[6] "NCSU CVC Analysis, Version 5.0", (North Carolina State University, 2000).

[7] S. M. Sze, Physics of Semiconductor Devices 2nd Edition, John Wiley & Sons Inc., 1981

[8] J. R. Yeargan and H. L. Taylor, "The Poole-Frenkel Effect with Compensation Present", *J. Applied Physics*, 39(12), pp.5600-5604, 1968

[9] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO_2", *J. Applied Physics*, 40(1), pp.278-283, 1969

[10] S. Bernal, J. A. Diaz, R. Garcia, and J. M. Roddriguez-Izquierdo, "Study of some aspects of the reactivity of La_2O_3 with CO_2 and H_2O", *J. Mater. Sci.* 20, pp.537-541 (1985).

[11] Theodosia Gougousi and Gregory N. Parsons, "Postdeposition reactivity of sputter-deposited high-dielectric-constant films with ambient H_2O and carbon-containing species", *J. Appl. Phys.*, 95, pp.1391-1396 (2004)

[12] Yi Zhao, M. Toyama, K. Kita, K. Kyuno, and A. Toriumi, "Moisture-absorption-induced permittivity deterioration and surface roughness enhancement of lanthanum oxide films on silicon", *Appl. Phys. Lett.* 88, 072904 (2006)

[13] Gin-ya Adachi, "SCIENCE of rare earths" pp.304

[14] S. Mudani, F. Li, S. B. Samavedam, P. J. Tobin, C. S. Kang, R. Nieh, J. C. Lee, L. F. Register, and S. K. Banerjee, "Interfacial Defect States in HfO_2 and ZrO_2 nMOS Capacitors," *IEEE Elec. Dev. Lett.* 23, 728-730 (2002).

[15] Daniel J. Lichtenwalner, Jesse S. Jur, Angus I. Kingon, Melody P. Agustin, Yan Yang, Susanne Stemmer, Lyudmila V. Goncharova, Torgny Gustafsson, and Eric Garfunkel, "Lanthanum silicate gate dielectric stacks with subnanometer equivalent oxide thickness utilizing an interfacial silica consumption reaction", *J. Appl. Phys.* **98**, 024314 (2005)

[16] Daniel M. Fleetwood, ""Border Traps" in MOS Devices", *IEEE Trans. Nucl. Sri.*, 39, pp.269-271 (1992)

[17] Zhu W.J., Tamagawa T., Gibson M., Furukawa T., Ma T.P, **"**Effect of Al inclusion in HfO_2 on the physical and electrical properties of the dielectrics**",** *IEEE ELECTRON DEVICE LETT*. 23, pp.649-651 (2002)

[18] S. Saito, D. Hisamoto, S. Kimura, and M. Hiratani, "Unified mobility model for high-κ gate stacks," in *IEDM Tech. Dig.*, Washington, DC, 2003, pp.797–800.

[19] Hyoungsub Kim, Ann Marshall, Paul C. McIntyre and Krishna C. Saraswat "Crystallization kinetics and microstructure-dependent leakage current behavior of ultrathin HfO_2 dielectrics: *In situ* annealing studies", *Appl. Phys. Lett.* 84, pp.2064-2066 (2004)

[20] M.-Y. Ho, H. Gong, G. D. Wilk, B. W. Busch, M. L. Green, P. M. Voyles, D. A. Muller, M. Bude, W. H. Lin, A. See, M. E. Loomans, S. K. Lahiri and Petri I. Räisänen "Morphology and crystallization kinetics in HfO_2 thin films grown by atomic layer deposition", *J. Appl. Phys.* 93, pp1477-1481 (2003)

[21] Hyoungsub Kim, Paul C. McIntyre and Krishna C. Saraswat "Effects of crystallization on the electrical properties of ultrathin HfO_2 dielectrics grown by atomic layer deposition", *Appl. Phys. Lett.* 82, 106 (2003)

[22] A. Fukuyama, "Electrical Characteristics of La_2O_3 MIM Capacitor with Different Process Condition", Tokyo Tech. master thesis (2006)

[23] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Konno, T. Chikyow, H. Kitajima and T. Arikado, *Jpn. J. App. Phys.* 43, pp.L1413-L1415 (2004)

[24] S. Takagi, M. Iwase, and A. Toriumi, "On the universality of inversionlayer mobility in n- and p-channel MOSFETs," in *IEDM Tech. Dig.*, 1988, pp. 398–401.

[25] W. J. Zhu, J. P. Han, and T. P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-k dielectrics", *IEEE Trans. Electron Devices* 51, 98 (2004)

[26] K. Onishi, S. K. Chang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J. C. Lee, Symp. on *VLSI Tech*., Honolulu, 22 (2002)

[27]Hideki Takeuchi, Daewon Ha, and Tsu-Jae King, "Observation of bulk HfO_2 defects by spectroscopic ellipsometry", *J. Vac. Sci. Technol. A* 22, pp.1337 (2004)

[28] John Robertson, "High dielectric constant gate oxides for metal oxide Si transistors**",** *Rep. Prog. Phys.* **69** (2006) 327–396

[29] Zhihong Zhang, Min Li, and Stephen A. Campbell, "A study on charge reduction in HfO_2 gate stacks", *IEEE Trans. Electron Devices*, 52, 1839 (2005)

[30] N. Bhat and K. C. Saraswat, "Characterization of border trap generation in rapid thermally annealed oxides deposited using silane chemistry", *J. Appl. Phys.* 84, 2722 (1998)

[31] Hong, Y.D., Yeow, Y.T, "Modeling the Effects of Interface Traps on Scanning Capacitance Microscopy dC/dV Measurement"**,** *COMMAD*.2004. pp.149-152

[32] K. J. Hubbard and D. G. Schlom, ”Thermodynamic stability of binary oxides in contact with silicon”, *J. Mater. Res.* 11, 2757 (1996).

ACKNOWLEDGEMENTS

The author would like to thank his supervisor at Tokyo Institute of Technology, Professor Hiroshi Iwai for his excellent guidance and continuous encouragement.

The author is also grateful to Prof. Hiroshi Ishiwara, Prof. Noriaki Nakayama, Prof. Yoshihiro Arimoto, Prof. Shun-ichiro Ohmi of Tokyo Institute of Technology for reviewing the thesis and for valuable advice.

The author would like to thank Professor Takeo Hattori for his valuable advice on XPS.

The author would like to thank Professor Nobuyuki Sugii very much for his polite instruction, useful advice, and continuous support.

The author would like to thank Associate Professor Kazuo Tsutsui for his valuable discussions.

The author would like to thank Dr. Kuniyuki Kakushima and Dr. Parhat Ahmet for his useful discussions and appropriate advice for this study.

The author would like to thank Mr. Yusuke Kuroki for his kind instruction for the experiment.

The author would like to thank all members of Professor Iwai's Laboratory, Mr. Atsushi Kuriyama, Mr. Mollina Reyes Joel, Mr. Yuichiro Sasaki, Mr. Hendriansyah Sauddin, Mr. Issui Aiba, Mr. Ruifei Xiang, Mr. Kentaro Nakagawa, Mr. Akira Fukuyama, Mr. Satoshi Yoshizaki, Mr. Koji Nagahiro, Mr. Jaeyeol Song, Mr. Takashi shiozawa, Mr. Yasuhiro shiino, Mr. Masayuki Nakagawa, Mr. Woei Yuan Chong, Mr. Manabu Adachi, Mr. Yoshihisa Ohishi, Mr. Takamasa Kawanago, Mr. Soushi Satoh, Mr. Yasuhiro Morozumi and Mr. Ko-ichi Okamoto for their kind friendship and discussions.

The author would like to express sincere gratitude to laboratory secretaries, Ms. N. Iizuka, Ms. M. Karakawa, Ms. T. Fukuyama and Ms. A. Matsumoto.

This study was partially supported by Semiconductor Technology Academic Research Center (STARC).

Finally the author would like to thank his father Kimio, his mother Fumiko, his brothers Kumi and Yoshi, and his friends Maya Yamamoto, Daisuke Tamaru for their everlasting supports, encouragements and understanding. .

Kiichi TACHI

Yokohama, JAPAN

January 2007