Master Thesis

A Study on Process Optimization of Ge-MOS Devices with La_2O_3 Gate dielectric

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Chapter 1. Introduction

1.1 Limits of Planar Si MOS Devices Scaling

1.2 Ge-based MOS Devices

1.3 Search for Next Generation high-k Gate Dielectric

1.4 The Purpose of this Study

1.1 Limits of Planar Si MOS Devices Scaling

Since the invention of metal-oxide-silicon field effect transistor (MOSFET) [1, 2], the scaling down of the device is inevitable for the reason of high performance, device reliability, and cost-down of MOSFET. In 1965, G. Moore observed an exponential growth in the number of transistors per integrated circuit and predicted that this trend would continue [3]. The press called it “Moore’s law”. The law states that density is double every 18 months. In other words, density is quadrupled every 3 years. This relationship can be expressed by the equation:

$$\log_{10}\left(\frac{y}{y_o}\right) = \frac{(x - x_o)}{3}\log_{10}(4) \tag{1-1}$$

here, y and y_o correspond to the device density at a certain year x and the base year x_o.

Figure 1-1 shows the scaling down of bits in DRAM [4] and transistors in CPU [5]. The solid line called Moore line corresponds to Eq. (1-1). It can be seen that the Moore line fits well the number of bits or transistors at each year.

The most important parameter in scaling down of MOSFET is the gate length and other factors are scaled down by the principle of constant-field scaling [6]. However, if the gate length is scaled down too small, the short-channel effects which the output of drain region influence the input of source region will get severe and electric properties of MOSFET come to degrade. Thus planar Si MOS devices have faced its scaling limit under gate length of 20nm as shown in figure 1-2 [7] and breakthrough is needed for further improvement.

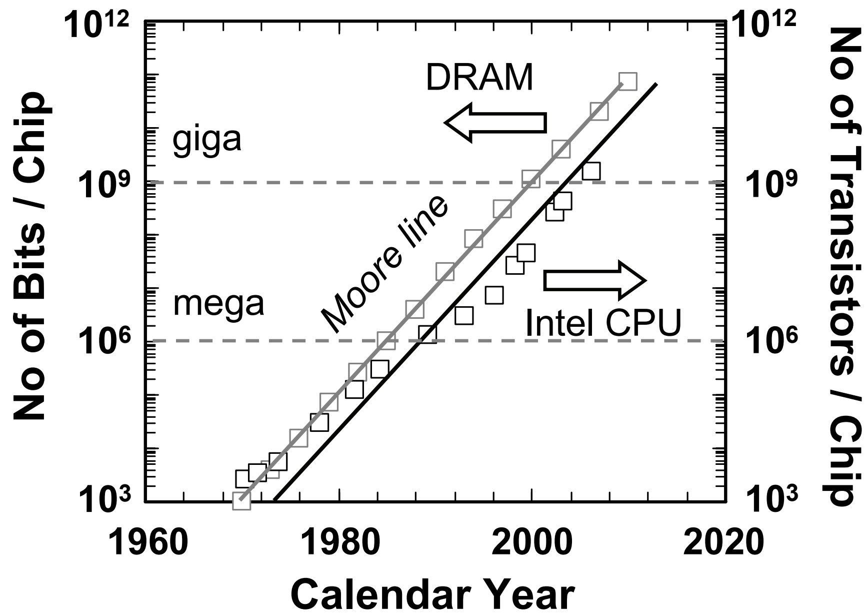


Figure 1-1. Scaling down of the number of bit in DRAM [4] and the number of transistors in CPU [5].

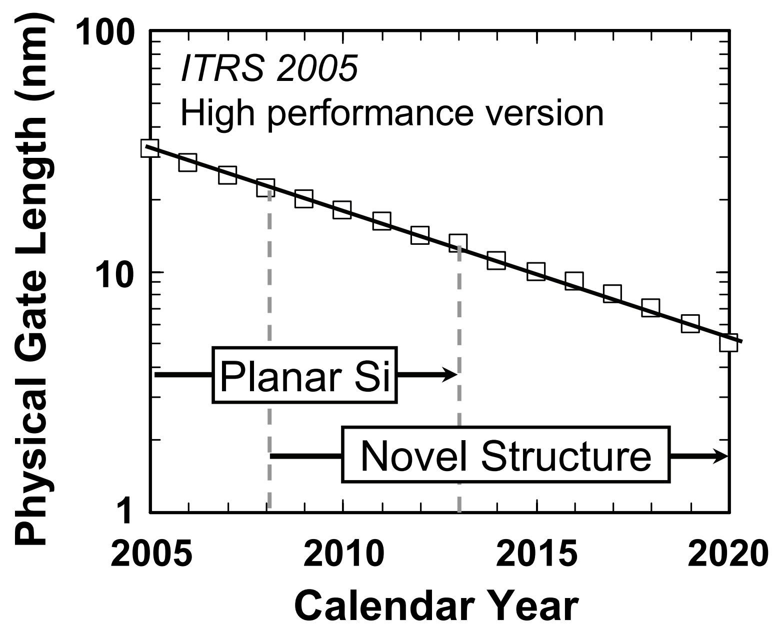


Figure 1-2. The scaling down of physical gate length on ITRS 2005

On the other hand, there is one more significant scaling limit in Si MOSFET. When the MOSFET is scaled down, the gate length and the gate oxide should be scaled down as same ratio to keep the equal electric field, as shown in Figure 1-3 [7]. It is well known that the invention and the continuous scaling-down of MOSFET are attributed at the superiority of the silicon dioxide (SiO_2) as a gate dielectric, compared to other dielectrics. However, state-of-the-art technology focuses on the alternative dielectric with high dielectric constant (high-*k*) compared to silicon dioxide. This is because the gate oxide approaches the direct tunneling regime. It has been reported that the direct tunneling occurs when the oxide is as thin as 3 nm [8]. If the direct tunneling current is appreciable to the channel current, transistor is unworkable.

The channel current, i.e., drain-to-source current I_{ds} can be expressed as a function of the inversion charge density Q_i with the gradual channel approximation (GCA) [9]:

$$I_{ds} = \mu_{eff} \frac{W}{L} \int_0^{V_{ds}} -Q_i(V)dV \tag{1-2}$$

here, μ_{eff} is the carrier mobility. W and L are width and length of the gate. V_{ds} is drain-to-source voltage. Q_i can be expressed by the following with the charge-sheet approximation:

$$Q_i = -C_{ox}\left(V_g - V_{fb} - 2\psi_B - V\right) - Q_d\ , \tag{1-3}$$

where C_{ox} is the gate oxide capacitance, V_g the gate voltage, V_{fb} flat band voltage, ψ_B the bulk potential, Q_d the bulk depletion charge density. Q_i is proportional to C_{ox} and so does I_{ds}. On the other hand, the direct tunneling current is principally determined by the gate oxide thickness T_{ox}. It can be seen by the approximated form of the direct tunneling current I_{DT}:

$$I_{DT} \sim \exp\left(-\frac{1}{|E_{ox}|} \right) \tag{1-4}$$

here, E_{ox} is the electric field across the oxide. Thus, by increasing the dielectric constant and by decreasing the film thickness of the gate oxide, it is possible to maintain the drain-to-source current of the MOSFET and direct tunneling current of gate oxide of the MOSFET.

The requirement for high-k dielectric as a gate oxide can be easily understood in the following manner. Substituting Eq. (1-3) into Eq. (1-2) and Taylor series expansion for large V_{ds}, one can get the saturation current expression in the linear region

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \left[(V_g - V_t) V_{ds} - \frac{m}{2} V_{ds}^2 \right] \tag{1-5}$$

where

$$m = 1 + \frac{C_{dm}}{C_{ox}} \tag{1-6}$$

here m typically lies between 1.1 and 1.4 and is related to body effect [9]. Since the tunneling current of gate oxide is important in the linear region, rather than in the saturation region, dividing I_{DT} by I_{ds}, one can obtain the simple current ratio describing gate tunneling current portion with respect to the drain current of the MOSFET:

$$\frac{I_{DT}}{I_{ds}} \sim \frac{\exp(-1/|E_{ox}|)}{|C_{ox}|} = \frac{1-1/|E_{ox}|}{\varepsilon_{ox} V_{ox}} \sim \frac{T_{ox}}{\varepsilon_{ox}} \tag{1-7}$$

This equation simply tells that higher dielectric constant of the gate oxide leads to the small portion of the tunneling current, at the same gate oxide thickness. This concept is also introduced elsewhere [10]. When the gate oxide is leaky, more precise derivation results in that $I_{ds}=I_{ds0}+I_g/2$ [11], where I_{ds0} is the drain current without gate

leakage current. However, the prediction from Eq. (1-7) does not change. This point is illustrated in Figure 1-4.

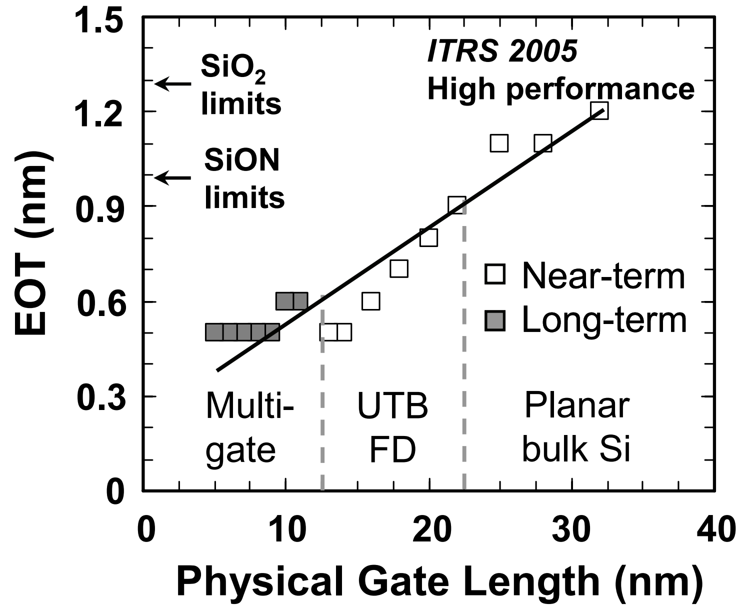


Figure 1-3. EOT versus physical gate length reported on ITRS 2005.

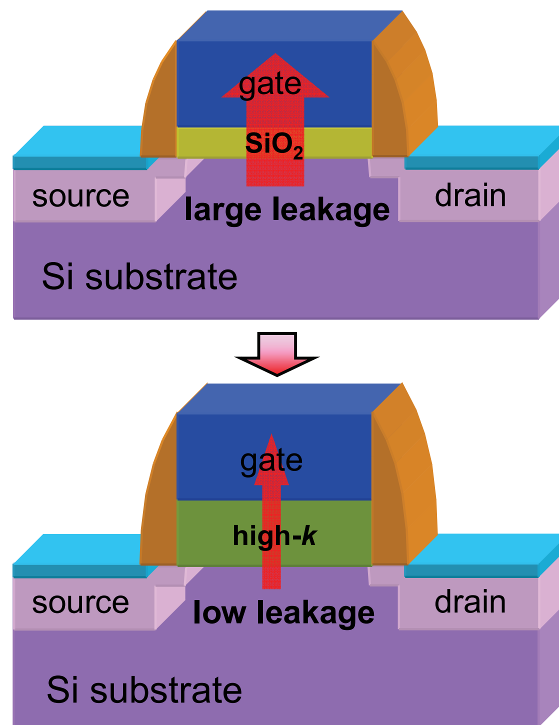


Figure 1-4. Illustration of high-k gate dielectric keeping the same charge density with lower leakage current.

Generally, high-k gate dielectrics are formed by deposition on substrate, while SiO_2 gate dielectric is obtained by thermal oxidation of Si substrate. Insofar as using high-k gate dielectric, there is no need to use Si as a channel material by all means. In order to resolve the scaling limit of planar Si MOS devices, alternative channel materials which have higher mobility compared to Si attract its attention. In many materials which have higher mobility than Si, Ge is focused with the highest hole mobility as shown in table 1-1. As complementary MOSFET (CMOSFET) use both n-MOS and p-MOS, low mobility of p-MOS degrade the total device performance. In this reason, higher performance in CMOS with Ge channel is expected.

Table 1-1. Electron and hole mobilities in various semiconductors at 300k

	μ_e[cm^2/Vs]	μ_h[cm^2/Vs]
Si	1400	450
Ge	3900	**1900**
GaAs	8500	400
InP	4600	650

1.2 Ge-based MOS Devices

Historically, Ge had been one of the most important semiconductors in the past as the first MOSFET and the integrated circuit were fabricated in Ge. However, some inferior properties of Ge as compared to Si make Ge extinguish in semiconductor industry. Inferior properties in Ge are classified into two parts; one is Ge itself to use as a substrate and another is its oxide as a gate dielectric and field isolator.

Table 1-2 shows the inferior factors of Ge itself as compared to Si. First is hardness, second is thermal conductivity and finally deposit. As the hardness of Ge is smaller than that of Si, Ge substrate is more fragile. When a chip operates with a billion of transistors, a large amount of heat is generated and it must be emitted. As thermal conductivity of Ge is smaller than that of Si, heat in a chip with Ge substrate is hardly emitted and the chip is easy to overheat. Fundamental problem is that Ge exists very little even less than gold [12], while Si is one of the largest materials on earth. It goes without saying that the production cost using Ge substrate is higher than that using Si substrate. In order to resolve these problems about Ge substrate, some researches on the epitaxial growth of Ge on the Si substrate and strained germanium-on-insulator (s-GOI) wafer have been proceeded recently, which suggest that Ge is used as only channel region on Si substrate as shown in figure 1-5 and 1-6 [13,14]. Especially, it was proved that p-MOS transistor with s-GOI wafer had 4 to 5 times mobility rather than universal hole mobility of Si [14].

Table 1-2. The inferior properties of Ge substrate compared to Si substrate.

	Ge	Si
Mohs Hardness	6.0	6.5
Thermal Conductivity at 300 K (W/cm-°C)	0.6	1.5
Deposit (1000ton)	>0.5	large

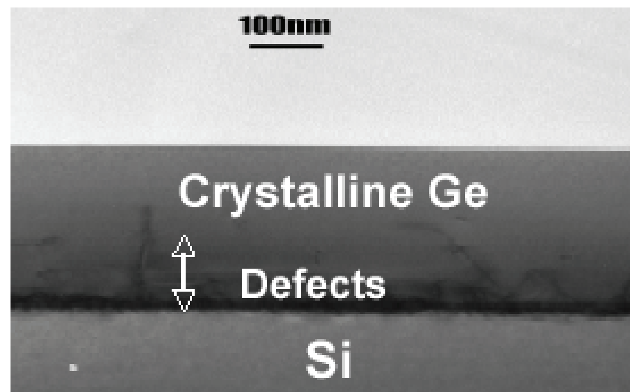


Figure 1-5. Epitaxial growth of Ge on Si substrate [13]

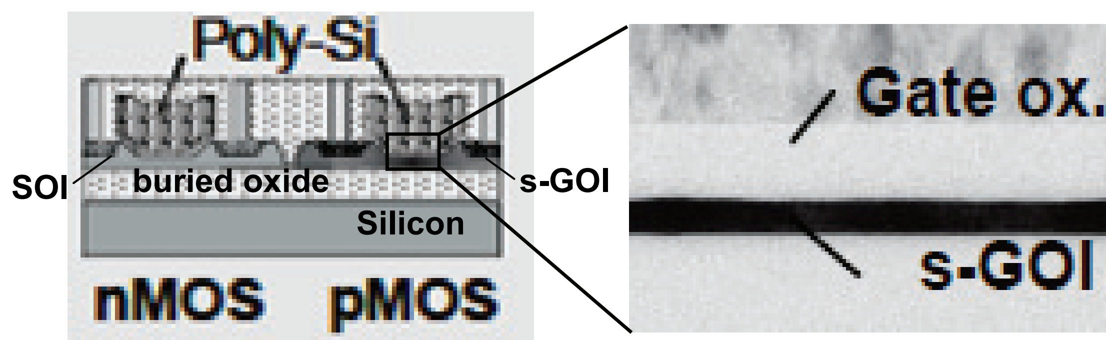


Figure 1-6. strained germanium-on-insulator (s-GOI) structure fabricated by Ge condensation method [14].

Although the problems of using Ge as a substrate have been resolved, another big issue on Ge oxide is still remained. Ge dioxide (GeO_2) can be formed lower temperature than SiO_2, however, GeO_2 component decay and Ge sub-oxides are formed with annealing temperature above 450°C [15]. Though the electric properties of GeO_2 are not poor, the sub-oxides enlarge the hysteresis of Ge MOS capacitors [16]. Moreover, it is well known that Ge oxide is dissolved by dipping in water, which means that Ge oxide is inappropriate in wet processes. Considering that the wet processes are inevitable for reduction in cost, water solubility of Ge oxide is fatal for adopting Ge in semiconductor industry. For these reasons SiO_2, GeO_xN_y, Ge_3N_4, high-*k* materials such as Al_2O_3, ZrO_2, HfO_2, HfO_xN_y and Y_2O_3 have been studied as gate dielectric for Ge-based devices [17-35]. Especially, studies on Ge-MOS devices using high-k dielectric have increased recently in order to achieve smaller EOT without increasing the leakage current.

1.3 Search for Nest Generation High-k Gate Dielectric

In making a choice among so many high-*k* materials, a sufficiently high dielectric constant, large band-gap and both conduction and valence band offset from substrate and thermodynamic stability are the key requirements for gate insulator application. Band gap of several candidate oxides for gate dielectric is shown in figure 1-7, as a function of the relative dielectric constant. Figures 1-7 (a) shows data summarized from various international journals and conference whereas figure 1-7 (b) is measurement results obtained from X-ray photoelectron spectroscopic (XPS) [36]. One can find the most promising dielectric in terms of the figure of merit given by the product of the band gap and the relative dielectric constant. They are Al_2O_3, ZrO_2,

HfO_2, La_2O_3, TiO_2, and etc.

Compared to other high-k materials, Lanthanum oxide (La_2O_3) is electrically hopeful for the gate insulator of the future MOSFET. La_2O_3 possesses high dielectric constant (~27) and large band-gap, especially higher band offset to silicon conduction band as shown in figure 1-7. In addition, it has achieved smaller EOT with low leakage current, which seems better than Hf-based materials as shown in figure 1-8. In fact, La_2O_3 has been mentioned and reported in various versions of ITRS as the potential gate insulator for post-Hf generation, which is shown in figure 1-9.

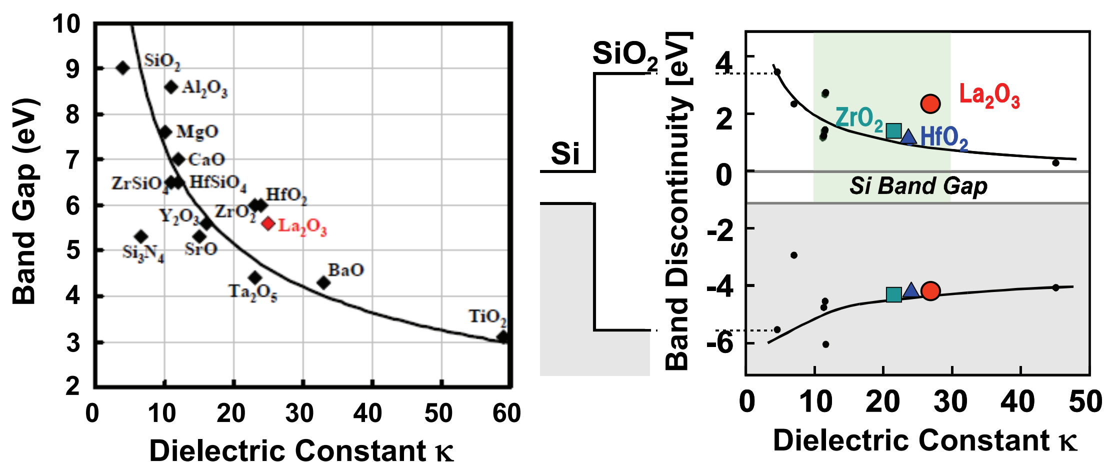


Figure 1-7. Band gap versus dielectric constant plots from (a) published data from journals and conference and (b) experimental results from XPS [36].

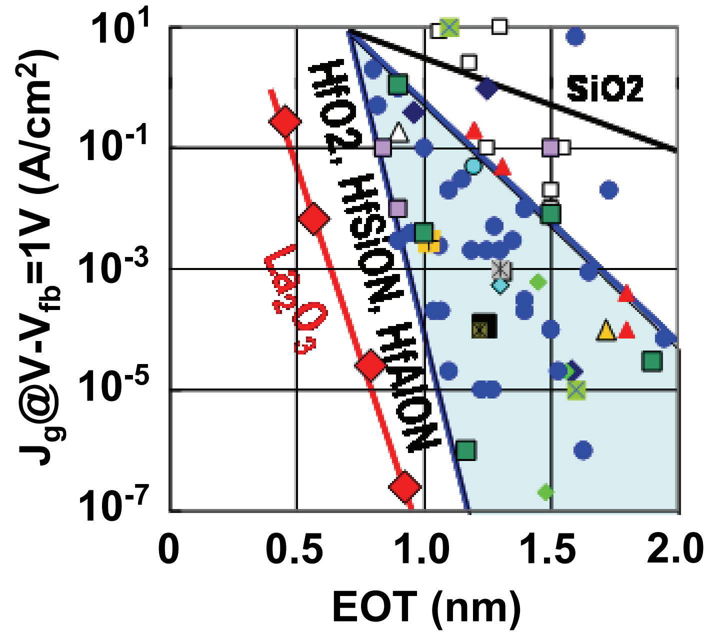


Figure 1-8. Leakage current density versus EOT plot for La_2O_3 and Hf-based high-k gate dielectric.

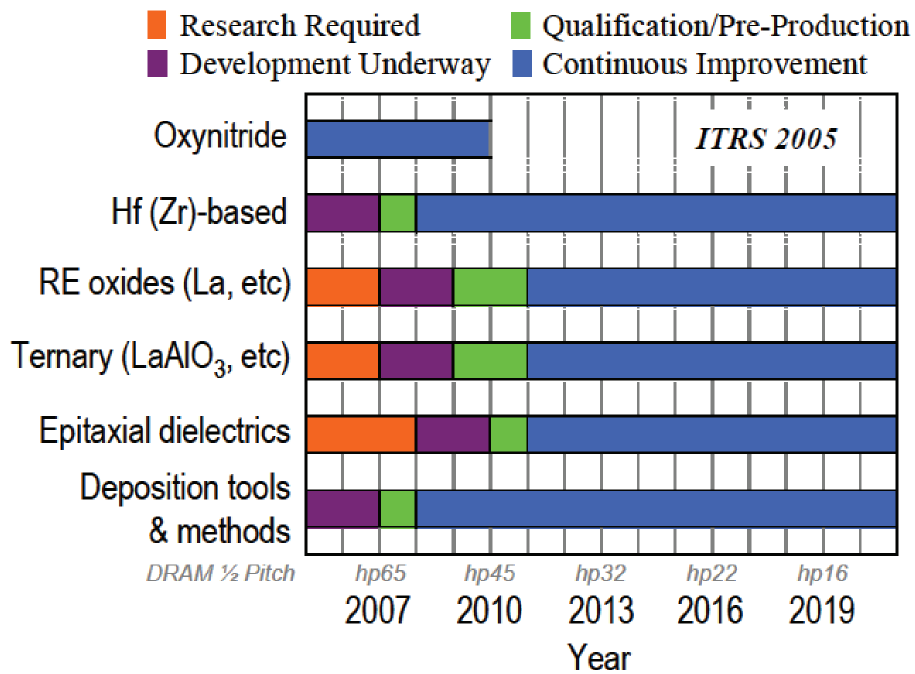


Figure 1-9. Roadmap of gate dielectric according to ITRS 2005.

1.4 The Purpose of this Study

So far, motivation for alternative channel materials and gate dielectrics, and general properties of high-k materials have been discussed. It seems that germanium with highest hole mobility is appropriate as a alternative channel materials and La_2O_3 is good as its gate dielectric due to the high dielectric constant and large band-gap.
In introducing the high-k materials as gate dielectric, interfacial properties such as interface trap density and interfacial layer growth between high-k and substrate are very important factor. Interface trap density degrades the effective mobility [37] and interfacial layer which has lower dielectric constant increases the EOT. Moreover, thermal stability of MOS structure with high-k gate dielectric is necessary during annealing for activation the source and drain region and recrystallization after interconnection.

For these reasons, the objective of this study is to investigate the interfacial properties between La_2O_3 and Ge substrate and to improve thermal stability of metal/La_2O_3/Ge MOS structure under various annealing conditions.

Chapter 2. Fabrication and Characterization Method

2.1 Fabrication Method

2.2 Characterization Method

2.1 Fabrication Method

2.1.1 Ge Substrate Cleaning

For deposition of high quality thin film, ultra clean surface is required, without metallic, organic and ionic contaminations, particles, native oxide. It has been reported that surface region of Si wafers is contaminated with various matters when it is as-received. It being similar in case of Si substrate, C, O and Sn related XPS signals was detected on the surface of as-received Ge(100) wafers [38].

The Si substrate is cleaned by the RCA cleaning process, which was proposed by W. kern et al. In case of Si, The surface oxide was removed completely with HF treatment, and HF-last surface does not oxidize soon in air. However, chemical cleaning method of the surface of Ge has not been established yet. XPS results show that Ge suboxide still remained with HF treatment as shown in figure 2-1. This suboxide might be rests not removed by HF treatment and/or re-oxidation of Ge surface during transfer to XPS chamber. In order to achieve the ultra-clean surface, alternative method forming GeO_2 as a passivation layer and performing annealing in ultra-high vacuum (UHV) chamber has been proposed [39, 40]. Figure 2-2 shows the XPS results in sample with annealing in UHV chamber at 600°C for 5min, which the suboxide was removed completely. Moreover, H. Okumura et al. proposed more useful $NH_4OH/H_2O_2/H_2O$ (1/2/20) treatment to form the protective Ge oxide layer. It is effective for particle removal with NH_4OH, moreover, organic and/or metallic contaminations was not detected by Auger electron spectroscopy measurement [38].

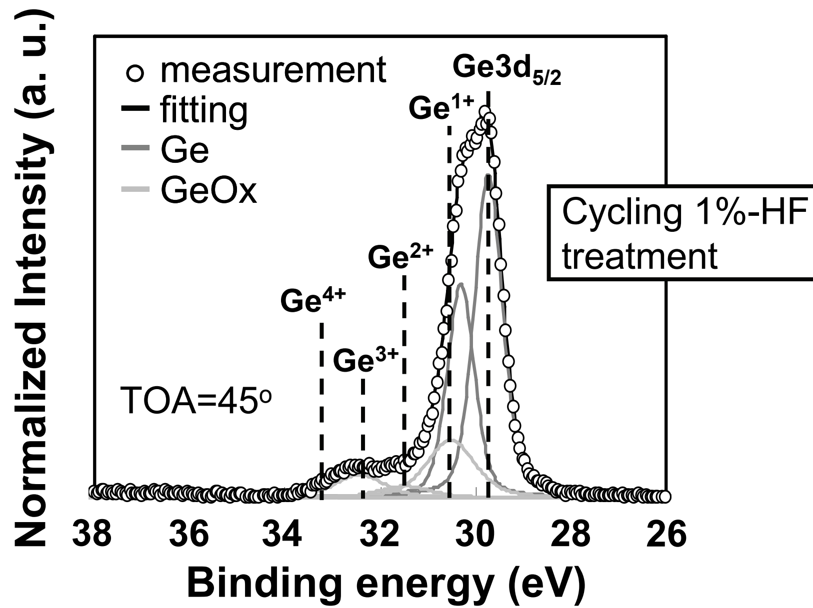


Figure 2-1. Deconvoluted XPS spectra of Ge3d from Ge substrate with cyclical treatment of dipping in 1%-HF solution and de-ionized (DI) water.

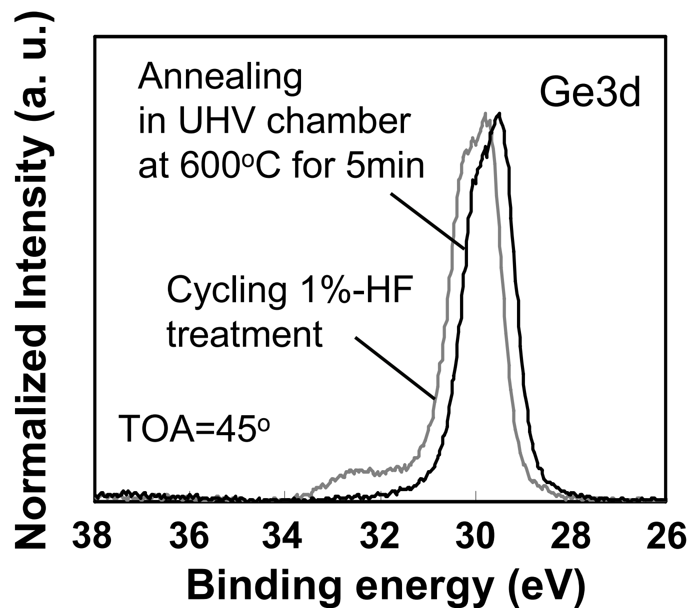


Figure 2-2. XPS spectra of Ge3d from Ge substrate with cyclical treatment of dipping in 1%-HF solution and DI water and with annealing in UHV chamber at 600°C.

2.1.2 Electron-beam Evaporation

As discussed by Lucovsky [41], the high-k gate dielectric film must be deposited. Lanthana film is deposited by the e-beam evaporation method in the UHV chamber, as shown in figure 2-3. There are four types of oxide sources in the bottom side of the chamber. One of the sources is La_2O_3 and heated by the electron-beam (E-beam) near the source. Then, since the chamber is maintained at the ultra high vacuum state, the Lanthana molecule begins to evaporate when the temperature of the source is greater than the evaporation temperature. Evaporation temperature is reported as 3620°C [42]. Figure 2-4 shows the equilibrium vapor pressure of La and La_2O_3 with some materials as a function of temperature.

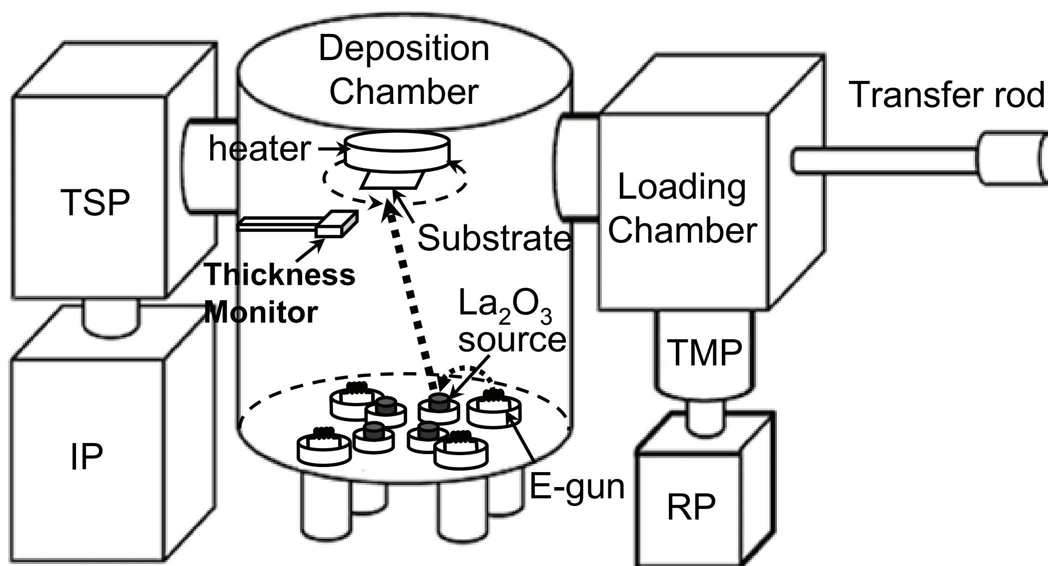


Figure 2-3. Schematic of the chamber for La_2O_3 film deposition.

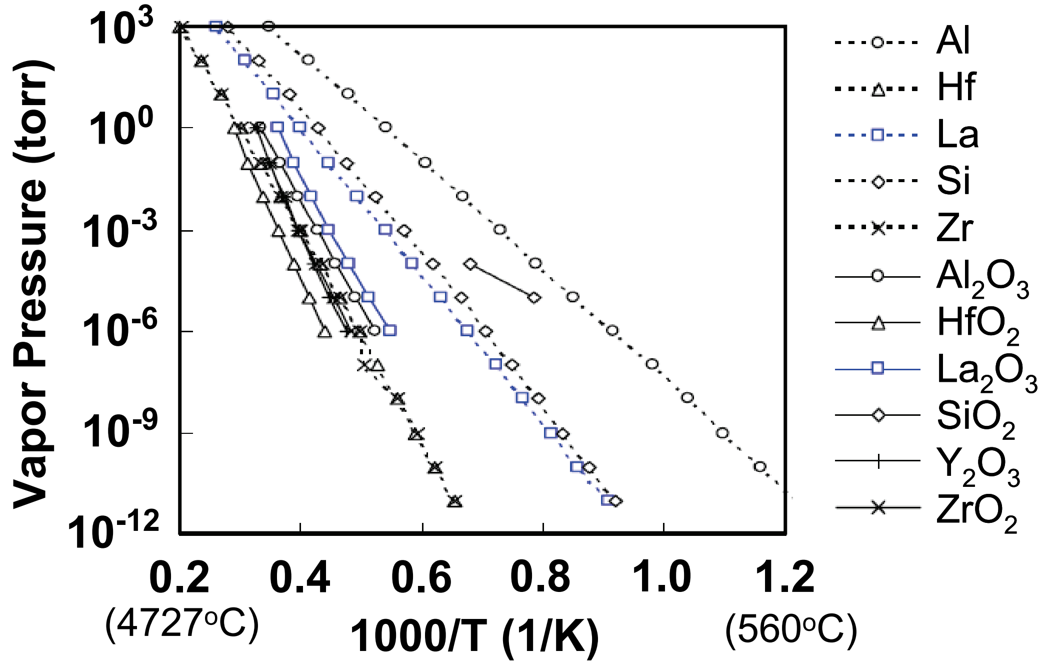


Figure 2-4 Equilibrium vapor pressure of La and La2O3 compared to some materials, as a function of temperature [43].

2.2 Characterization Method

2.2.1 Capacitance-Voltage (C-V) Characteristics

C-V characteristic measurements were performed with various frequencies (1kHz~ 1MHz) by precision LCR Meter (HP 4284A, Agilent). The energy band diagram of an MOS capacitor on a p-type substrate is shown in figure 2-5. The intrinsic energy level E_i or potential ϕ in the neutral part of device is taken as the zero reference potential. The surface potential ϕ_s is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \tag{2-1}$$

where Q_G and V_G are the gate charge and the gate voltage, respectively. It is the change of charge due to a change of voltage and is most commonly given in units of

farad/units area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS capacitor from the gate, $C = dQ_G / dV_G$, where Q_G and V_G are the gate charge and the gate voltage. Since the total charge in the device must be zero, assuming no oxide charge, $Q_G = -(Q_S + Q_{it})$, where Q_S is the semiconductor charge, Q_{it} the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{ox} + \phi_s$, where V_{FB} is the flatband voltage, V_{ox} the oxide voltage, and ϕ_s the surface potential, allowing Eq. (2-1) to be rewritten as

$$C = \frac{dQ_S + dQ_{it}}{dV_{ox} + d\phi_s} \tag{2-2}$$

The semiconductor charge density Q_S, consists of hole charge density Q_p, space-charge region bulk charge density Q_b, and electron charge density Q_n. With $Q_S = Q_p + Q_b + Q_n$, Eq. (2-2) becomes

$$C = -\frac{1}{\dfrac{dV_{ox}}{dQ_S + dQ_{it}} + \dfrac{d\phi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \tag{2-3}$$

Utilizing the general capacitance definition of Eq. (2-1), Eq. (2-3) becomes

$$C = -\frac{1}{\dfrac{1}{C_{ox}} + \dfrac{1}{C_p + C_b + C_n + C_{it}}} = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \tag{2-4}$$

The positive accumulation Q_p dominates for negative gate voltages for *p*-substrate devices. For positive V_G, the semiconductor charges are negative. The minus sign in Eq. (2-3) cancels in either case.

Equation (2-4) is represented by the equivalent circuit in figure 2-6(a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_p is

very high approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in figure 2-6 (b) and the overall capacitance is C_{ox}. For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = -qN_AW$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} as shown in figure 2-6(c). In weak inversion C_n begins to appear. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (figure 2-6(d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in figure 2-6(e) applies in inversion, with $C_b = K_s\varepsilon_o / W_{inv}$ with W_{inv} the inversion space-charge region width.

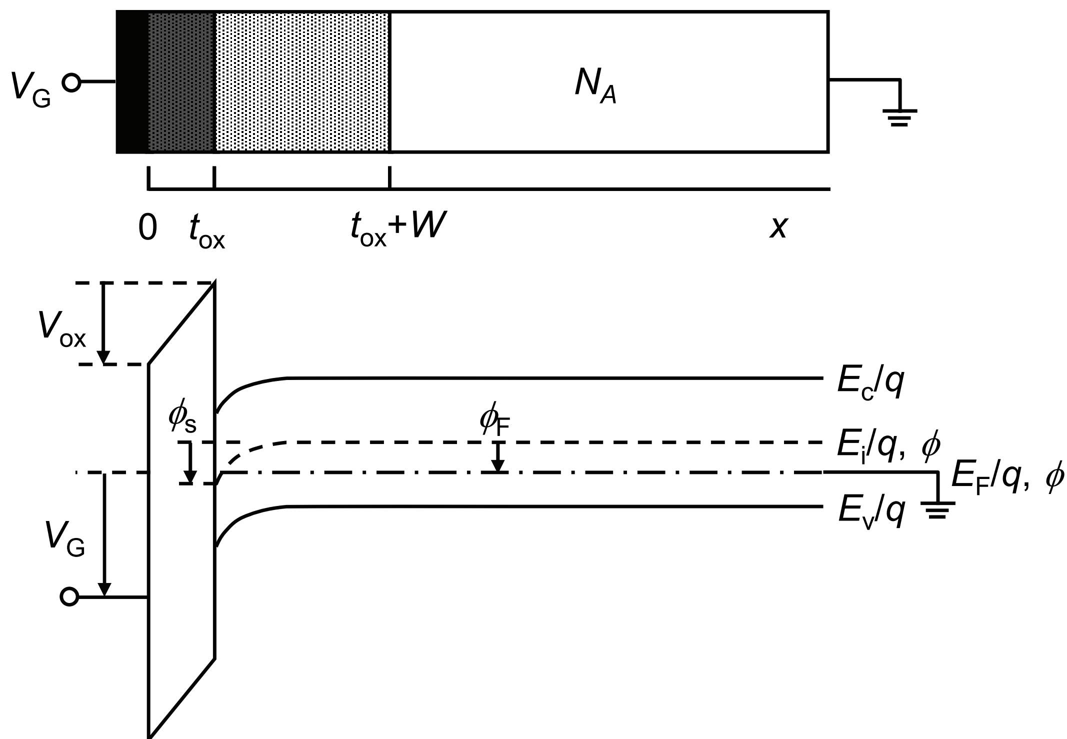


Figure 2-5. Cross section and potential band diagram of an MOS capacitor.

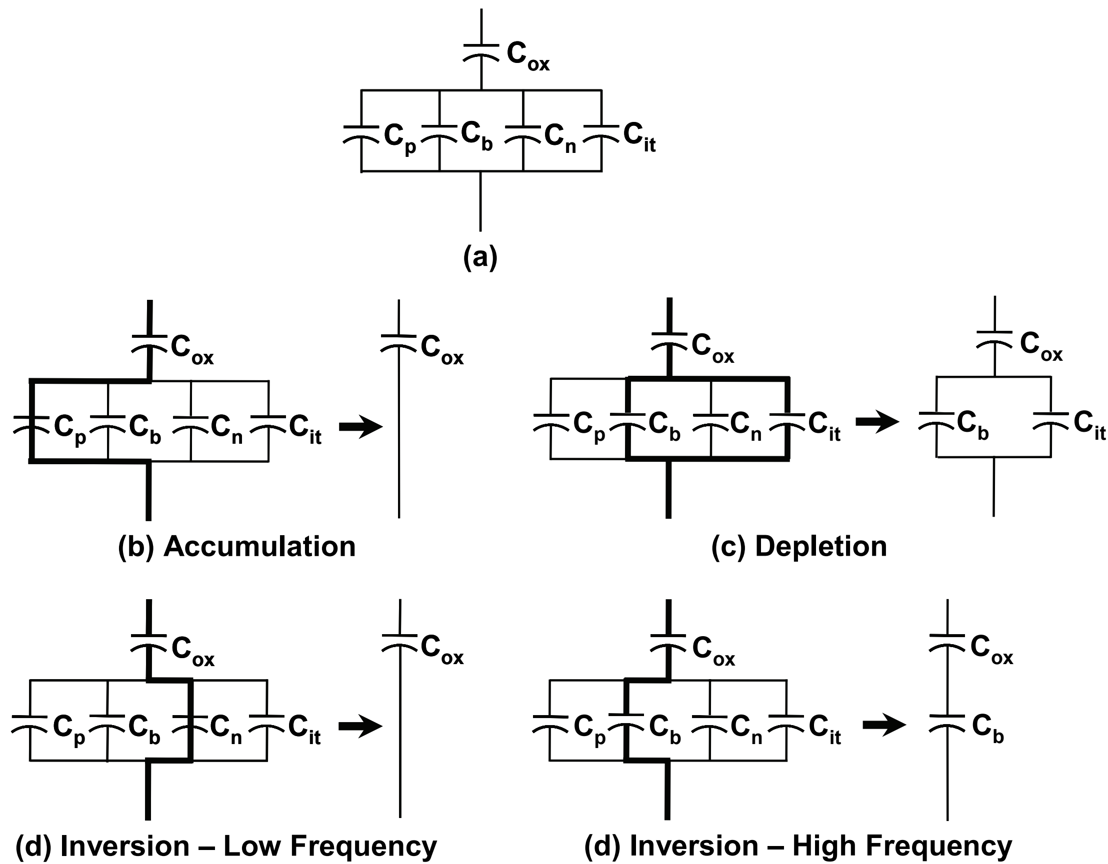


Figure 2-6. Capacitances of MOS capacitors for various bias conditions.

2.2.2 Leakage Current Density-Voltage (J-V) Characteristics

It is important to suppress the leakage current of the gate dielectric film as small as possible in order to lower the power consumption of LSI. To estimate the leakage current density, J-V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.).

2.2.3 Interface Trap Density by Conductance Method

The conductance method, proposed by Nicoliian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it}. Interface trap densities of 10^9 cm^{-2}-eV^{-1} and lower can be measured. It is also the most complete method, because it yields D_{it} in the depletion and weak inversion portion of the band gap, the capture

cross-sections for majority carriers, and information about surface potential fluctuation. The technique is based on measuring the equivalent parallel conductance G_p of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in figure 2-7(a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_s, and the interface trap capacitance C_{it}. The capture-emission of carriers by D_{it} is a lossy process, represented by the resistance R_{it}. It is convenient to replace the circuit of figure 2-7(a) by that in figure 2-7(b), where C_p and G_p are given by

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{2-5}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2-6}$$

where $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it}C_{it}$, the interface trap time constant, given by $\tau_{it} = [\upsilon_{th}\sigma_p N_A \exp(-q\phi_s/kT)]^{-1}$. Dividing G_p by w makes Eq. (2-6) symmetrical in $\omega\tau_{it}$. Equations (2-5) and (2-6) are for interface traps with a single energy level in the band gap. Interface traps at the SiO_2-Si interface, however, are continuously distributed in energy throughout the Si band gap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln\left[1+(\omega\tau_{it})^2\right]. \tag{2-7}$$

Equations (2-6) and (2-7) show that the conductance is easier to interpret than

the capacitance, because Eq.(2-6) does not require C_s. The conductance is measured as a function of frequency and plotted as G_p/ω versus w. G_p/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_p/q\omega$. For Eq.(2-7) one can find $\omega \sim 2/\tau_{it}$ and $D_{it} = 2.5G_p/q\omega$ at the maximum. Hence one can determine D_{it} from the maximum G_p/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis. G_p/ω versus f plots, calculated according to Eqs. (2-6) and (2-7).

Experimental G_p/ω versus ω curves are generally broader than predicted by Eq. (2-7), attributed to interface trap time constant dispersion caused by surface potential fluctuations due to non-uniformities in oxide charge and interface traps as well as doping density. Surface potential fluctuations are more pronounced in p-Si than in n-Si. Surface potential fluctuations complicate the analysis of the experimental data. When such fluctuations are taken into account, Eq. (2-7) becomes

$$\frac{G_p}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] P(U_s)\,dU_s \tag{2-8}$$

where P(Us) is a probability distribution of the surface potential fluctuation given by

$$P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{\left(U_s - \overline{U}_s\right)^2}{2\sigma^2}\right) \tag{2-9}$$

with $\overline{U}_s$ and σ the normalized mean surface potential and standard deviation, respectively.

An approximate expression giving the interface trap density in terms if the measured maximum conductance is

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max}. \tag{2-10}$$

Capacitance meters generally assumed the device to consist of the parallel C_m-G_m combination in figure 2-7(c). A circuit comparison of figure 2-7(b) to 2-7(c) gives

G_p/ω in terms of the measured capacitance C_m, the oxide capacitance, and the measured conductance G_m as

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2-11}$$

assuming negligible series resistance. The conductance measurement must be carried out over wide frequency range. The portion of the band gap probed by conductance measurements is typically from flatband to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50mV or less to prevent harmonics of the signal frequency giving rise to spurious conductances. The conductance depends only on the device area for a given D_{it}. However, a capacitor with thin oxide has a high capacitance relative to the conductance, especially for low D_{it} and the resolution of the capacitance meter is dominated by the out-of-phase capacitive current component. Reducing C_{ox} by increasing the oxide thickness helps this measurement problem.

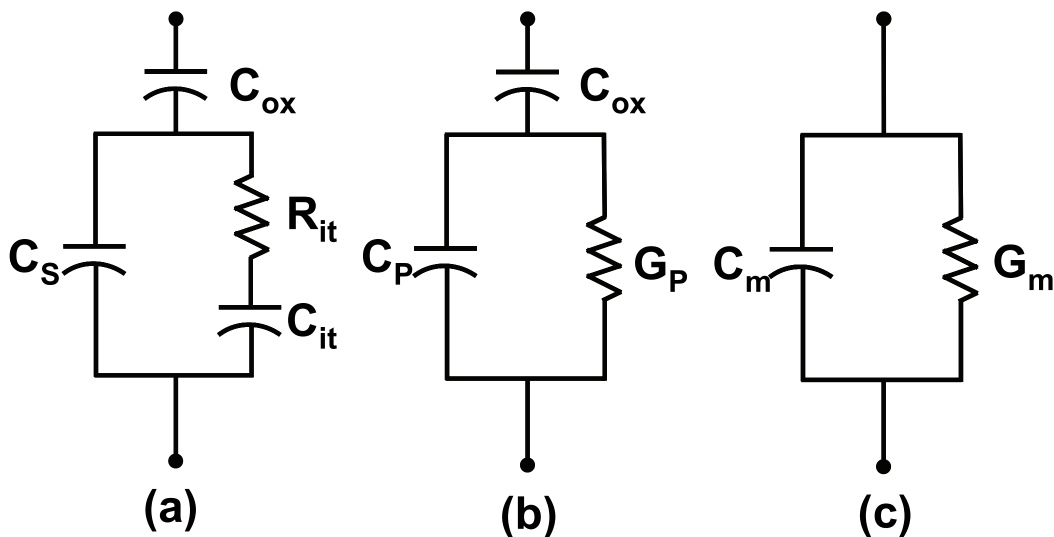


Figure 2-7. Equivalent circuit for conductance measurement; (a) MOS-C with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit.

2.2.4 X-ray Photoelectron Spectroscopy (XPS)

XPS, also known as the Electron Spectroscopy for Chemical Analysis (ESCA), is one of the useful methods to evaluate chemical bindings in the oxide or at the interface. Figure 2-8 explains the principle of XPS. Samples were irradiated with X-ray and the emitted photoelectrons with kinetic energy *KE* were detected. Measured *KE* was given by

$$KE = hv - BE - \phi_s \tag{2-12}$$

where *hv* is the photon energy, *BE* is the binding energy of the atomic orbital from which the electron generates and φ_s is the spectrometer work function.

Figure 2-9 explains the principle of XSP. The binding energy is the minimum energy needs for breaking the chemical bond of molecule and is inherent in each bond of molecule. Thus, the binding states can be identified by the positions of the binding energy which the peak appears. In the case that the peak position was different from the expected position, the chemical bond states were discussed considering the amount of shift to higher or lower energy side.

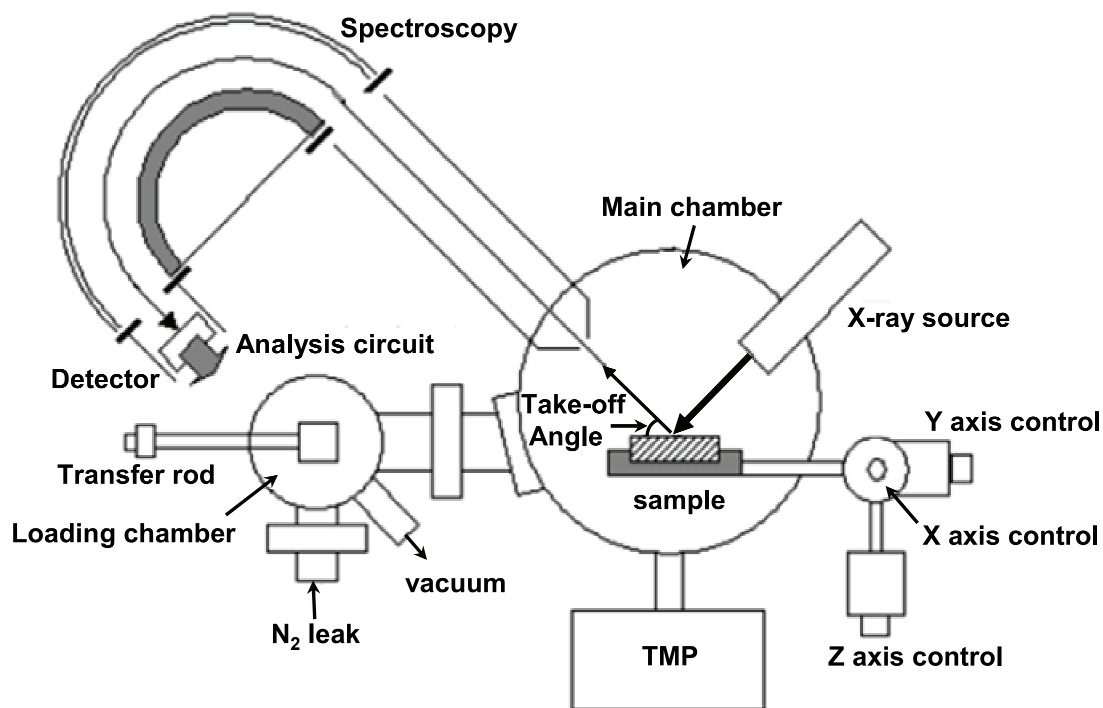


Figure 2-8. Schematic of XPS equipment

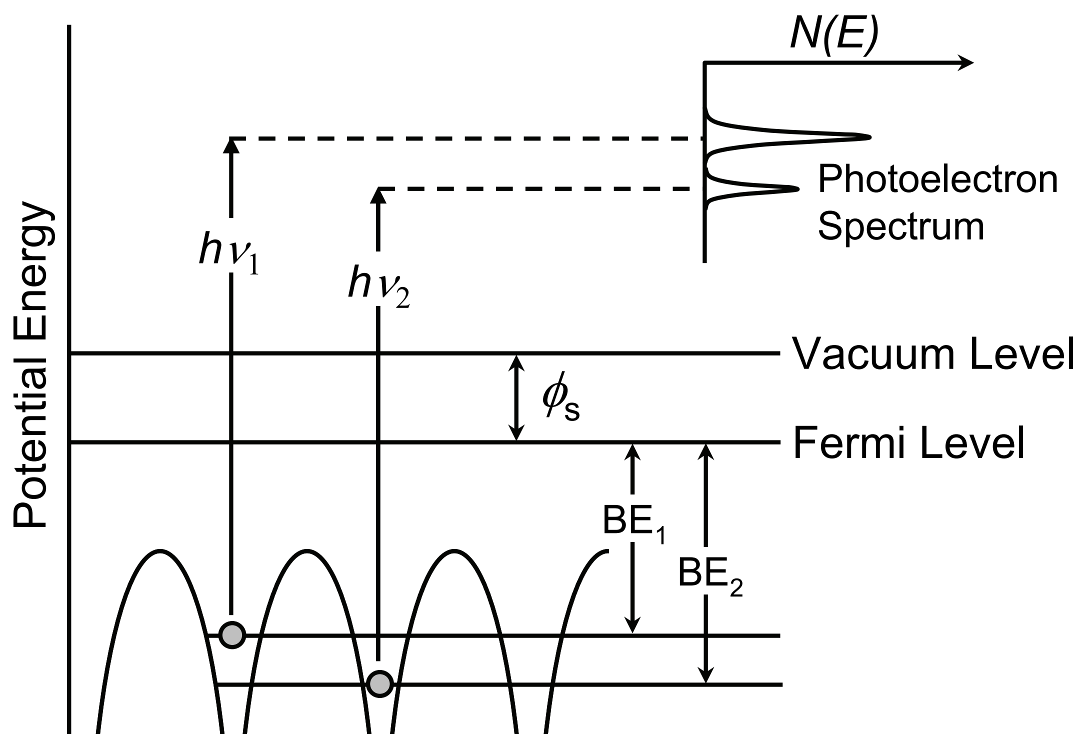


Figure 2-9. Principle of XPS measurement.

Chapter 3. Interfacial Properties of La_2O_3/Ge on Annealing Condition

3.1 Introduction

3.2 Experimental Procedure

3.3 Characterization of La_2O_3/Ge on PDA in N_2; comparison with that of La_2O_3/Si

3.4 The Effect of PMA on Pt/La_2O_3/Ge MOS Structure

3.5 Improvement of Interfacial Properties by Interfacial Ge-oxide Layer

3.6 Conclusion

3.1 Introduction

Interfacial properties such as interface trap density and interfacial layer growth are very important factor in introducing the high-k materials as gate dielectric. Interface trap density reduces the effective mobility [37] and interfacial layer which has lower dielectric constant increases the EOT.

In this chapter, interfacial properties between La_2O_3 and Ge substrate were studied under various annealing conditions.

3.2 Experimental Procedure

Figure 3-1 shows the fabrication process of Ge MOS capacitors. Ge MOS capacitors were fabricated on n-type Ge (100) wafers with resistivity of 1.9~2.4 Ωcm. Ge wafers were cleaned by dipping in an HCl/H_2O (1/4) solution followed by rinsing in de-ionized water. After that a protective Ge Oxide layer was formed by $NH_4OH/H_2O_2/H_2O$ (1/2/20) treatment at room temperature. The wafers were transferred into ultra-high vacuum (UHV) chamber (~10^{-8} Pa) and annealed at 600^oC to remove the protective Ge oxide. La_2O_3 films were deposited by electron-beam evaporation using La_2O_3 tablet as a source under pressure of ~1×10^{-6} Pa at substrate temperature of 250^oC. After the deposition, to improve the La_2O_3 films properties post-deposition annealing (PDA) was conducted under various gas conditions of N_2, O_2 and 5%-O_2+N_2 ambient at various temperatures. Gate electrode was formed by electron-beam evaporation or DC sputtering of Pt. Some samples were subjected to the post-metallization annealing (PMA) in N_2 ambient at 300℃-600℃ for 5 minutes after the metallization.

Capacitance-voltage (C-V) characteristics, leakage current density (J-V),

spectroscopic ellipsometry, High resolution transmission electron microscopy (HR-TEM), x-ray diffraction (XRD) and x-ray photoelectron spectroscopy (XPS) measurements were performed to characterize the interfacial properties of the samples.

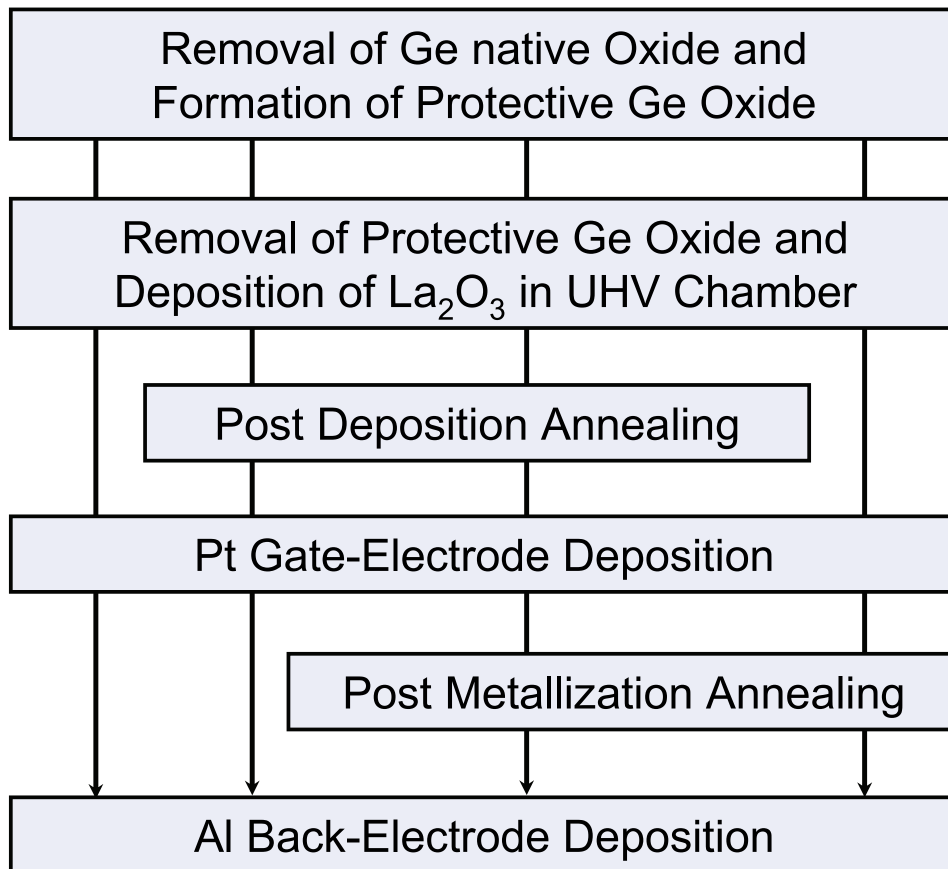
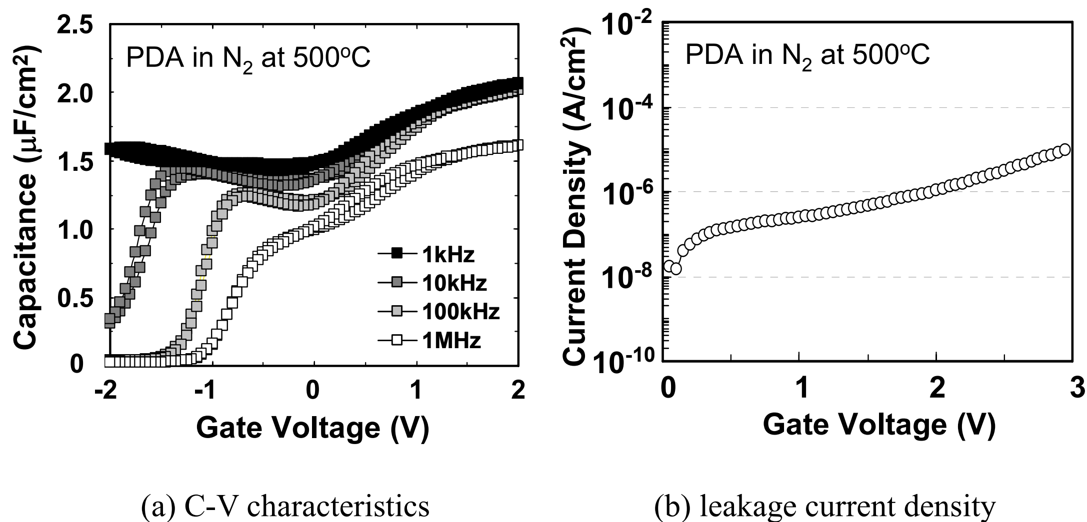


Figure 3-1. Fabrication process of Ge MOS capacitors.

3.3 Characterization of La_2O_3/Ge on PDA in N_2; comparison with that of La_2O_3/Si

Figure 3-2 shows the 1kHz~1MHz C-V characteristics and leakage current density of sample with PDA at 500°C. The capacitance equivalent thickness (CET) of 1.76 nm with leakage current density of 3×10^{-7} A/cm^2 at 1V was achieved from Pt/La_2O_3/Ge structure with PDA at 500°C, which is sufficiently high for activation the source and drain region for Ge MOSFET [16]. However, a large amount of frequency dependence and kink was observed and this result was also observed at other PDA temperatures. Capacitance decrease of 1MHz C-V curve in accumulation is attributed to series resistance effects [44]. Low-frequency behavior shown in 1kHz C-V characteristic is explained by high intrinsic carrier concentration of Ge [45]. Differential of capacitance depend on frequency nearby flat band voltage (Vfb) and kink shown in C-V curves measured above 10kHz is due to large amount of interface trap density of 1.3×10^{13} cm^{-2}eV^{-1} calculated by conductance method [46].



(a) C-V characteristics (b) leakage current density

Figure 3-2. C-V characteristics and leakage current density with PDA at 500°C.

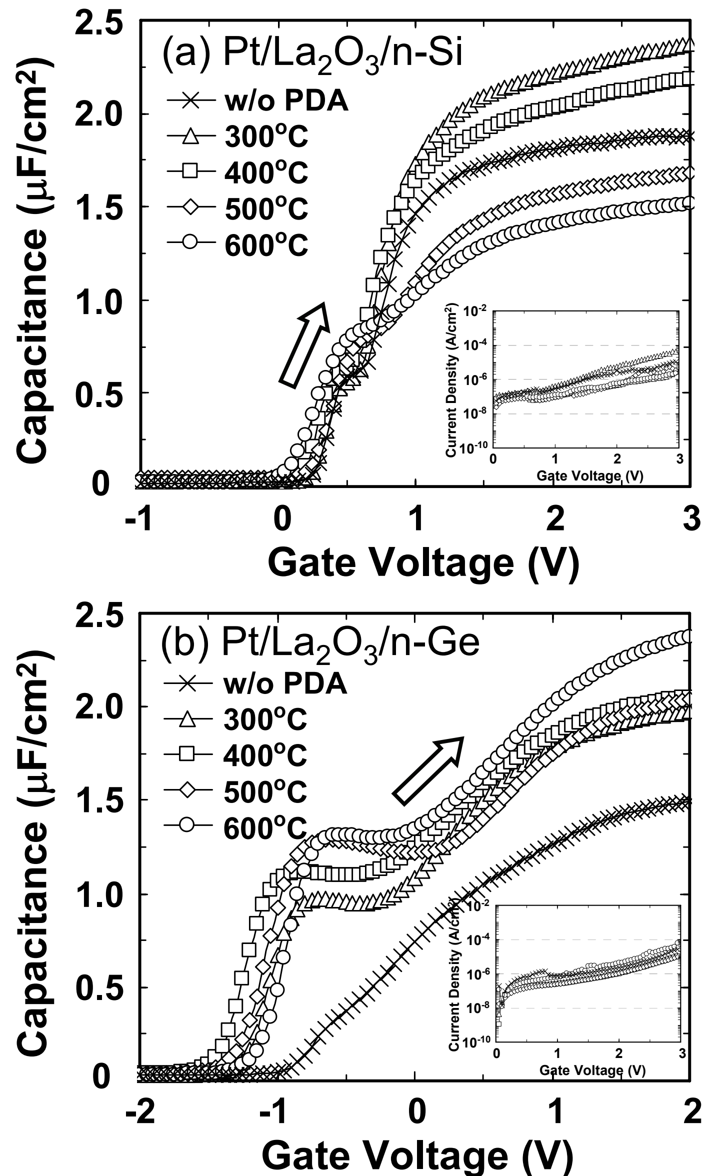


Figure 3-3. C-V characteristics of (a) Pt/La_2O_3/n-Si and (b) Pt/La_2O_3/n-Ge MOS structures with PDA at various temperatures. The inset shows leakage current of the MOS structures.

Figure 3-3 shows the C-V characteristics of (a) Pt/La_2O_3/n-Si and (b) Pt/La_2O_3/n-Ge MOS structures with PDA at various temperatures. The insets show the leakage current density of samples. As shown in figure 3-3 (a), capacitance of Si MOS structures once increased by PDA at 300°C, but decreased with increasing the PDA temperature. On the contrary, in case of Ge MOS structures, capacitance increased

along PDA temperature and showed largest value at 600°C as shown in figure 3-3 (b). Effective dielectric constant of La_2O_3 on Ge was about 14, whereas that of on Si was about 9 with high temperature PDA. Low dielectric constant on Si substrate can be explained by the reaction at the interface as shown below.

Figure 3-4 shows hysteresis of the C-V curves. A large amount of hysteresis was observed in samples with PDA up to 400°C and as-deposited one in Pt/La_2O_3/Ge structures compared with those of Pt/La_2O_3/Si structures. The small hysteresis shown in case of Si substrate might be due to silicate reaction of Si and La_2O_3 even in as-deposited samples [47], which silicon combined with dangling bonds caused by oxygen vacancy in La_2O_3. In case of Ge substrate, the hysteresis dramatically reduced at 500°C PDA, which suggests that dangling bonds were removed by reaction of Ge substrate and La_2O_3.

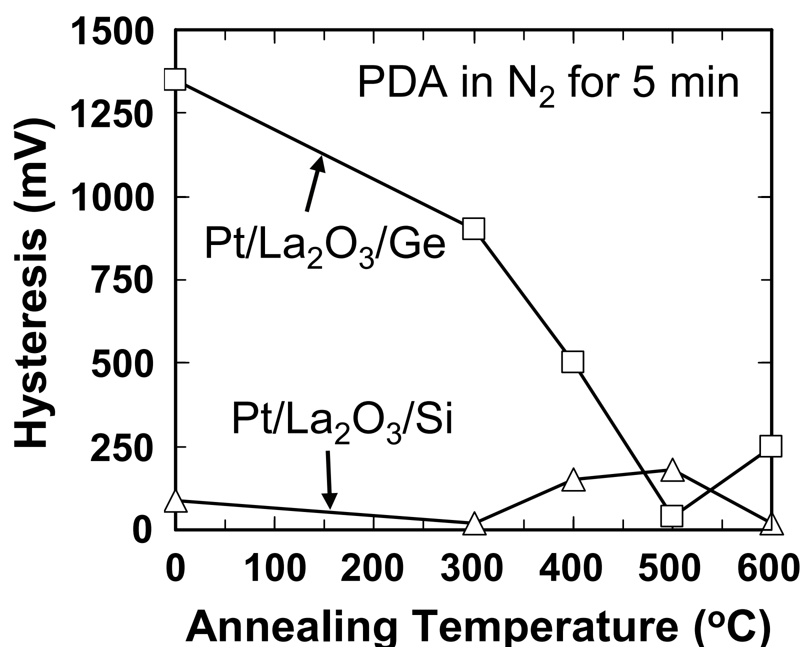


Figure 3-4. Hysteresis of Pt/La_2O_3/n-Si and Pt/La_2O_3/n-Ge MOS structures with PDA at various temperatures.

Figure 3-5 shows the physical thickness change of La_2O_3 films normalized by the value of the as-deposited films, which were measured by spectroscopic ellipsometry. At the temperature of 300^oC, the film thickness decreased in both Si and Ge substrate due to the densification of the La_2O_3 films [48]. However, PDA at 400^oC and above, the thickness of films formed on Si substrate increased, suggesting the growth of interfacial La-silicate and/or SiO_2 layer between the La_2O_3 film and the Si substrate [47, 48]. This growth of interfacial layer (IL) caused to decrease the capacitance with increasing the PDA temperature. On the contrary, film thickness on Ge substrate showed little change after the PDA at up to 500^oC, which suggests that either La-Germanate or GeO_2 layer is less formed by PDA in N_2. Moreover the film thickness of La_2O_3 on Ge substrate decreased with PDA at 600^oC, which eventually increased the capacitance. This decrease of thickness with PDA at 600^oC might be due to desorption of the hydroxyl group, which was absorbed into La_2O_3 to form $La(OH)_3$ from water component in air [49]. The dehydration was confirmed by XRD with thick La_2O_3 films (22 nm) on Ge (Figure 3-6). $La(OH)_3$ peaks were observed from samples with PDA up to 500^oC, and disappeared over 600^oC, where La_2O_3 start to appear.

The cross sectional images of the films with PDA at 600^oC were observed by HR-TEM (Figure 3-7). It should be noted that the thickness of the interfacial layer is less than 0.3 nm on a Ge substrate, while more than 1.7 nm SiO_2 layer was grown on a Si substrate. Such an absence of interfacial layer formation in high-*k*/Ge system has been reported in other high-*k* materials [29, 30, 35].

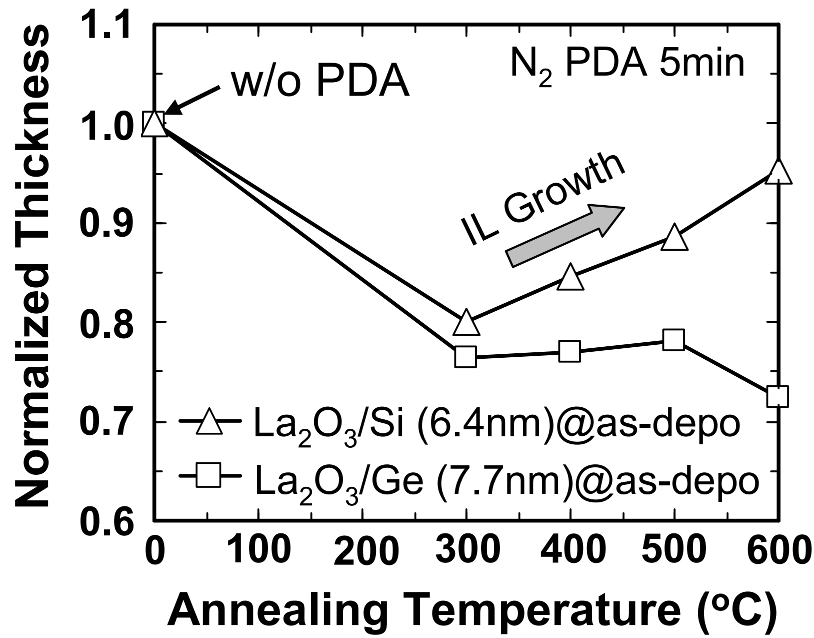


Figure 3-5. Physical thickness change of La_2O_3 films normalized by as-deposited thickness, which were measured by spectroscopy ellipsometry.

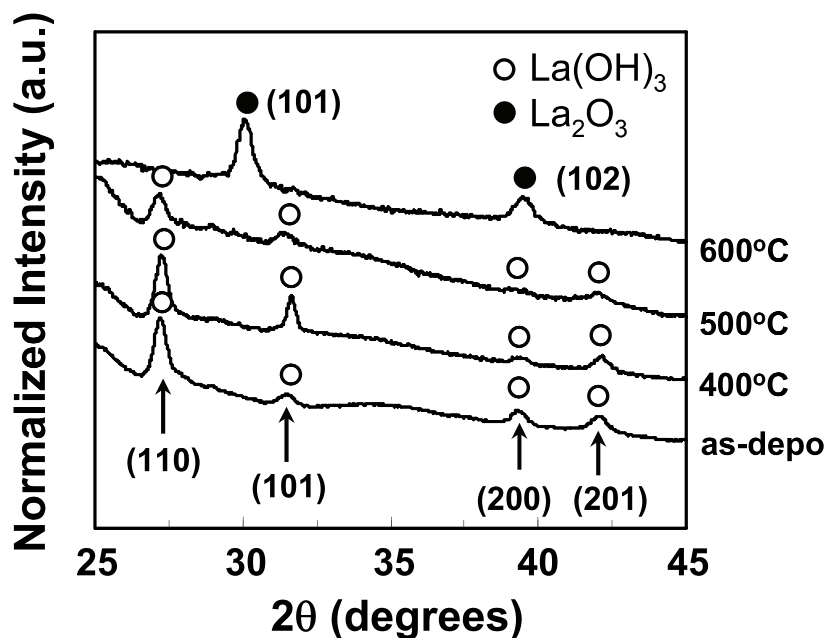


Figure3-6. XRD spectra for La_2O_3 (22nm) films with PDA at various temperature. $La(OH)_3$ peaks were observed with PDA up to 500°C, and disappeared over 600°C, where La_2O_3 peals start to appear.

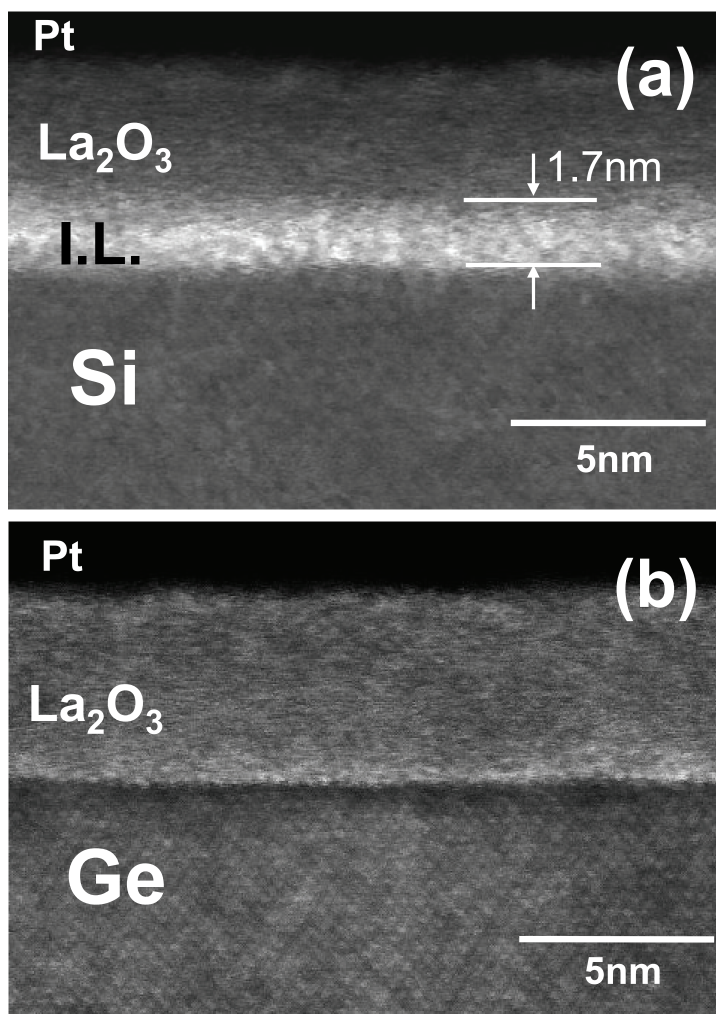


Figure 3-7. HR-TEM images of La_2O_3/Si and La_2O_3/Ge structures, which PDA was conducted at 600°C.

In order to examine the composition of the La_2O_3/Ge interface, chemical bonding configuration analyzed using was XPS, which is shown in Figure 3-8. The source x-ray was monochromatized Al $K\alpha$ radiation (1486.7 eV) and take-off angle was 80°. Thicknesses of La_2O_3 films were chosen to be 1.8~2.0 nm in order to acquire the signals from the interface of La_2O_3 and Ge substrate. Ge-oxide (GeO_x) spectra, chemically shifted from Ge3d peak, were deconvoluted using four GeO_x peaks (Ge^{1+}, Ge^{2+}, Ge^{3+}, Ge^{4+}) with energy shifts of 0.8, 1.8, 2.6, and 3.4 eV relative to the binding energy of elemental Ge3$d_{5/2}$ [50]. As shown in figure 3-8, no GeO_2 (Ge^{4+}) peak was

observed for all samples. This is in contrast to the case using a Si substrate; SiO_2 was detected even for the as-deposited film at the La_2O_3/Si interface [47]. Considering the Gibbs Free Energy of formation of GeO_2 (-387 kJ/mol at 1000K) and SiO_2 (-730kJ/mol at 1000K), GeO_2 is thermodynamically unstable compared to SiO_2 so that a GeO_2 layer unlikely forms at the La_2O_3/Ge interface. The sub-oxides (Ge^{1+}, Ge^{2+}) detected from the La_2O_3/Ge structure might be formed because of the interfacial bonding configured at the interface between La_2O_3 and Ge, considering that similar sub-oxides were also observed at the interface with other high-*k* materials on Ge [51, 52]. Taking into account of electronegativity of Si (χ_{Si}=1.9) and Ge (χ_{Ge}=2.0), La-Germanate peak is expected to appear around Ge^{3+} component. The peak for Ge^{3+} might thus include La-Germanate component.

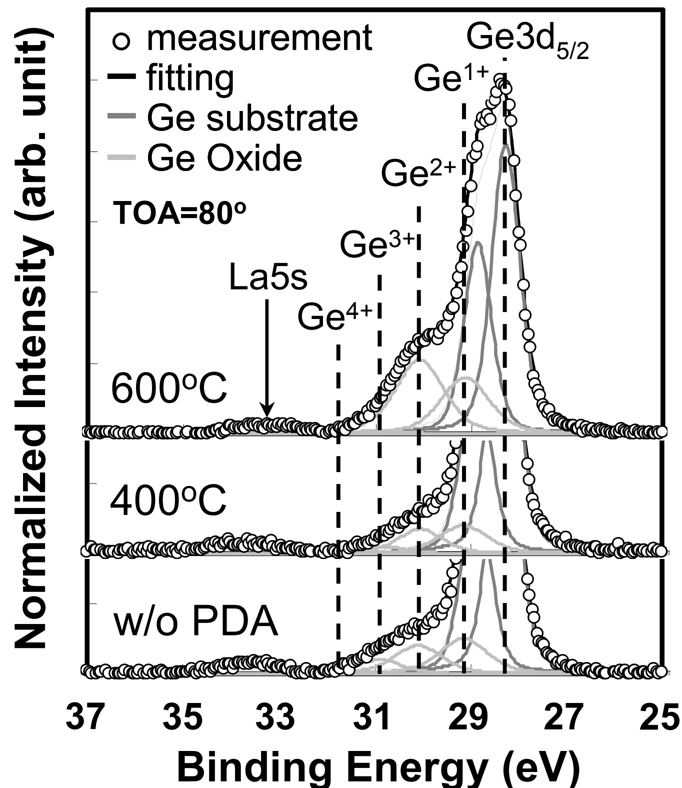


Figure 3-8. Deconvoluted XPS spectra of Ge3d from La_2O_3(2nm)/Ge structure with different annealing temperature.

3.4 The Effect of PMA on Pt/La_2O_3/Ge MOS Structure

Figure 3-9 shows 1kHz~1MHz C-V characteristics of Pt/La_2O_3/Ge MOS structure with PMA at 500°C. The film thickness of La_2O_3 is 9.2nm at as-deposited condition. Frequency dispersion decreased dramatically compared to sample with PDA at 500°C which was shown in figure 3-2 though hysteresis increased. Figure 3-10 shows 100kHz C-V characteristics of samples with PDA, PMA and PDA+PMA at 300°C. A large amount of kink shown in sample with PDA was significantly reduced by PMA and little kink was observed in sample conducted only PMA. This decrease of frequency dependence and kink was due to the reduction of interface trap density as shown in figure 3-11. The samples with PMA which showed little kink in C-V curves also had less interface trap density. The capacitance was largest in samples with PDA and decreased with PMA. This suggests that an interfacial layer is formed by PMA and interfacial layer improved the interfacial properties.

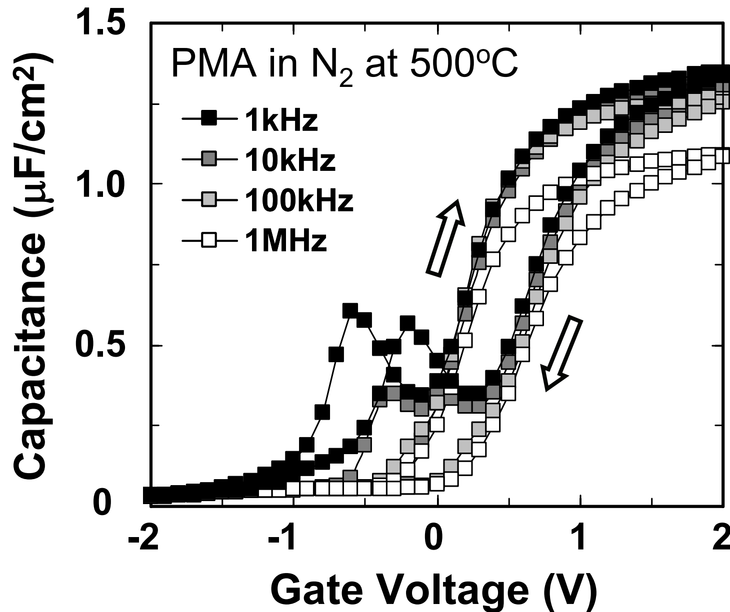


Figure 3-9. C-V characteristics of Pt/La_2O_3/n-Ge MOS structures with PMA at 500°C.

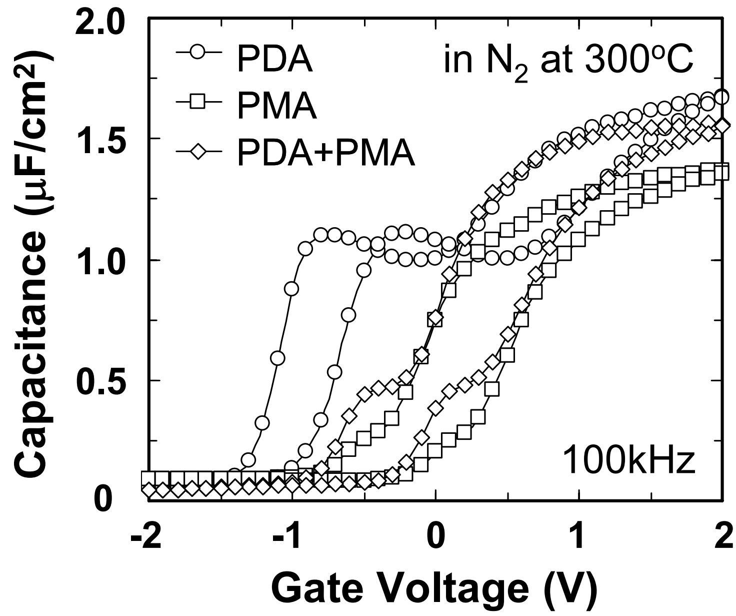


Figure 3-10. 1kHz C-V characteristics of samples with PDA, PMA and PDA+PMA at 300°C.

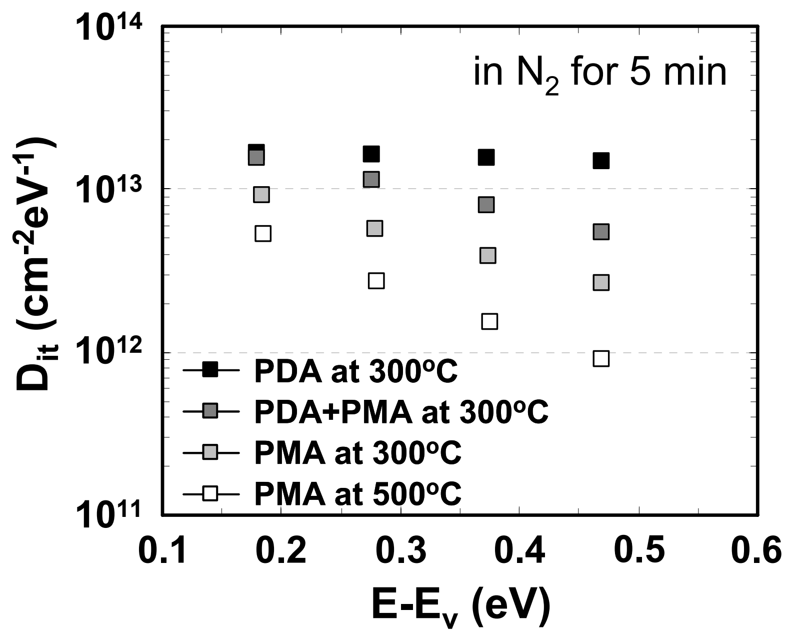


Figure 3-11. Interface trap density of samples with PDA, PMA and PDA+PMA at 300°C and sample with PMA at 500 °C.

In order to examine the formation of interfacial layer, XPS analysis was conducted using samples performed PDA or PMA at 400°C, which is shown in Figure 3-12 and 3-13. Thicknesses of La_2O_3 films and Pt electrode were 2.0 nm and 1.5nm respectively. The Ge Oxide exists in interface of La_2O_3 and Ge substrate considering the angle-resolved XPS analysis results as shown in figure 3-12. The ratio of GeO_x intensity to La5s intensity reduced as take-off angle was getting smaller. This means that GeO_x is located under the La_2O_3 films. Moreover, the ratio of GeO_x intensity to Ge3d intensity increased as take-off angle was getting smaller, which means that GeOx is located above the Ge substrate. Figure 3-13 shows the peak deconvolution of GeO_x spectra, which conducted as same way of chapter 3.4. As shown in figure 3-13, GeO_2 (Ge^{4+}) peak and large amount of Ge_2O_3 (Ge^{3+}) was observed in spectra of samples with PMA, which did not appear in spectra of sample with PDA. These Ge^{3+} and Ge^{4+} components might improve the interfacial properties and decrease the capacitance. The source of oxygen components to oxidize the Ge substrate might be hydroxyl and/or oxygen attached to La_2O_3 at surface of La_2O_3 considering the high hygroscopic property of La_2O_3. We guessed that surface hydroxyl and oxygen detached by annealing in case of PDA, however, Pt electrode prevented hydroxyl and oxygen from escaping in case of PMA. Due to this hydroxyl and oxygen which did not escape, there were enough oxygen components to oxidize Ge substrate.

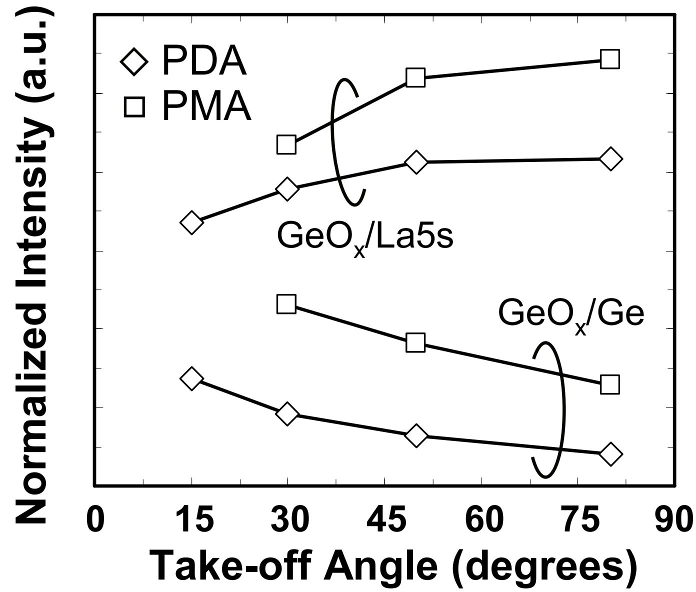


Figure 3-12. The intensity ratio of GeO_x/La5s and GeO_x/Ge against take-off angle calculated by angle-resolved XPS analysis

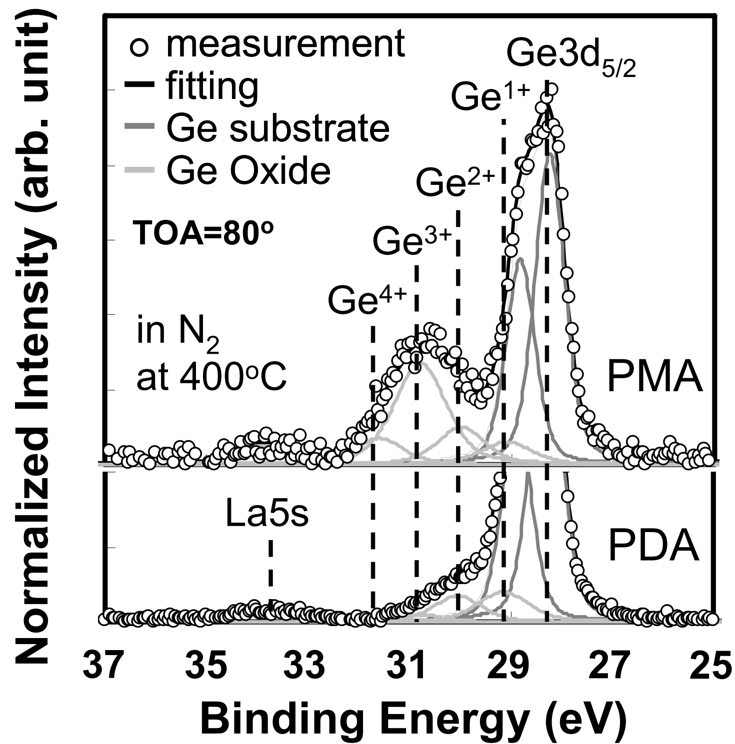


Figure 3-13. Deconvoluted XPS spectra of Ge3d from Pt(1.5nm)/La_2O_3(2nm)/Ge structure with PMA at 400°C and La_2O_3(2nm)/Ge structure with PDA at 400°C.

In order to confirm the effect of surface hydroxyl and oxygen, in-situ vacuum annealing was performed before Pt electrode deposition. After removing the surface hydroxyl and oxygen by 300°C vacuum annealing, Pt electrode was deposited at room temperature using DC sputtering system in UHV chamber as in-situ. The film thickness of La_2O_3 is 14.5nm at as-deposited condition.

Figure 3-14 shows 1kHz and 100kHz C-V characteristic of Pt/La_2O_3/Ge MOS structure with or without in-situ vacuum annealing before Pt electrode deposition, which was conducted PMA at 500°C. Capacitance was larger in sample with in-situ annealing than those of without in-situ annealing. Small frequency dispersion and kink was observed in the samples performed only PMA without in-situ vacuum annealing, however, a large amount of frequency dispersion at accumulation and kink appeared in those with in-situ vacuum annealing. Moreover, interface trap density was less in the samples without in-situ annealing than those with in-situ annealing as shown in figure 3-15. These results suggest that little interfacial GeO_x layer growth in sample with in-situ annealing as surface hydroxyl and oxygen was removed by in-situ vacuum annealing. Thus surface hydroxyl and/or oxygen might help formation of the interfacial Ge-oxide and improve the interfacial properties.

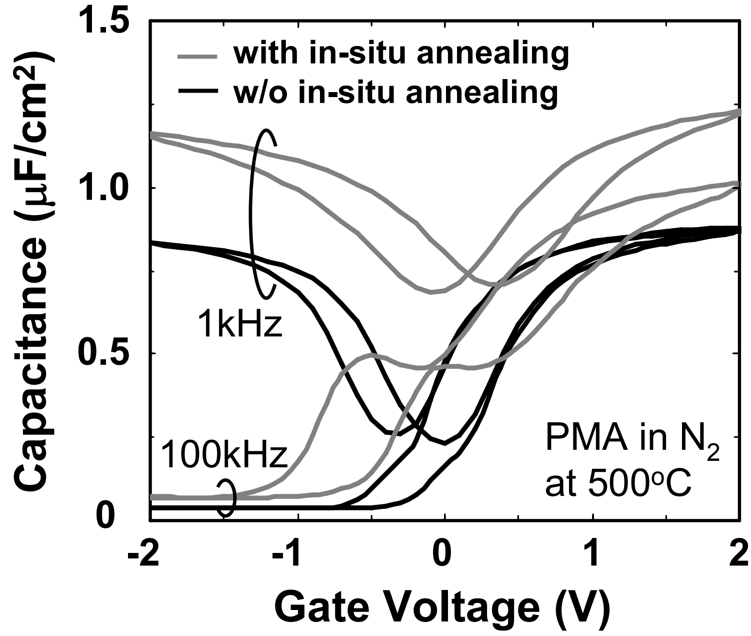


Figure 3-14. 1kHz and 100kHz C-V characteristic of Pt/La_2O_3/Ge MOS structures with or without in-situ vacuum annealing before Pt electrode deposition, which were conducted PMA at 500°C.

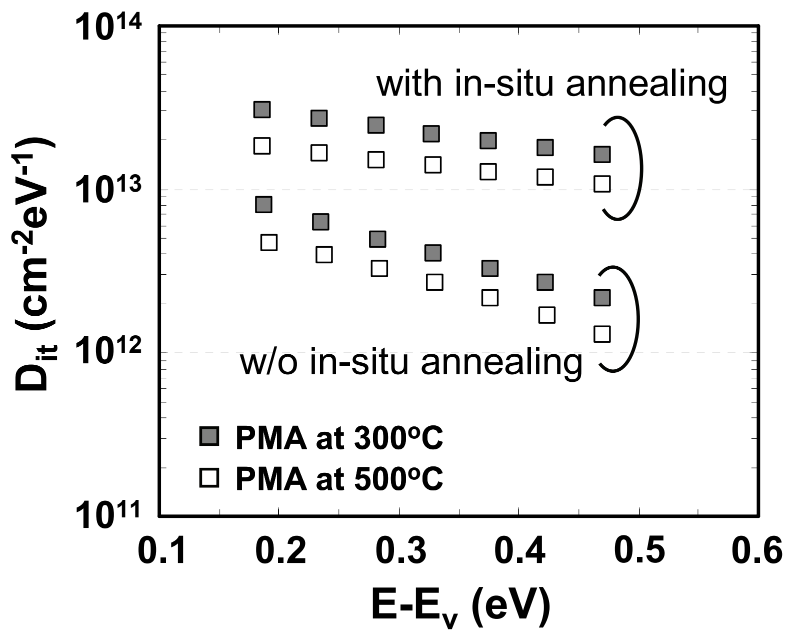


Figure 3-15. Interface trap density of Pt/La_2O_3/Ge MOS structures with or without in-situ vacuum annealing before Pt electrode deposition, which were conducted PMA at 300°C and 500°C

Interfacial layer formation was reconfirmed using XPS analysis shown in figure 3-16. Thicknesses of La_2O_3 films and Pt electrode were 4.5 nm and 1.5nm respectively. Spectra were normalized by La5s peak considering intensity of La_2O_3 should be same as it was deposited simultaneously. As shown in figure 3-16, stronger GeO_x intensity was observed in sample without in-situ vacuum annealing both case of PMA at 300°C and 500°C, which confirmed surface hydroxyl and/or oxygen helped formation of the interfacial Ge-oxide.

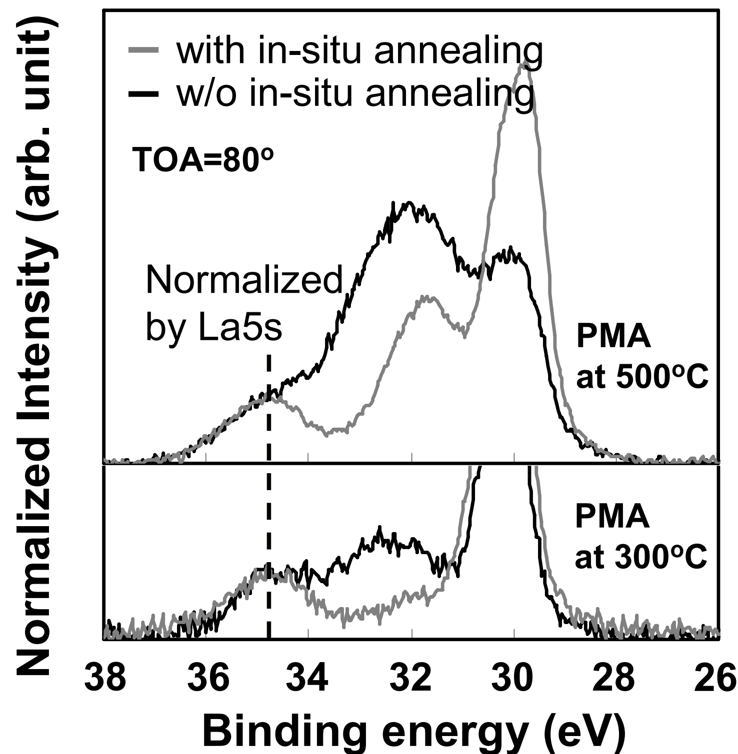
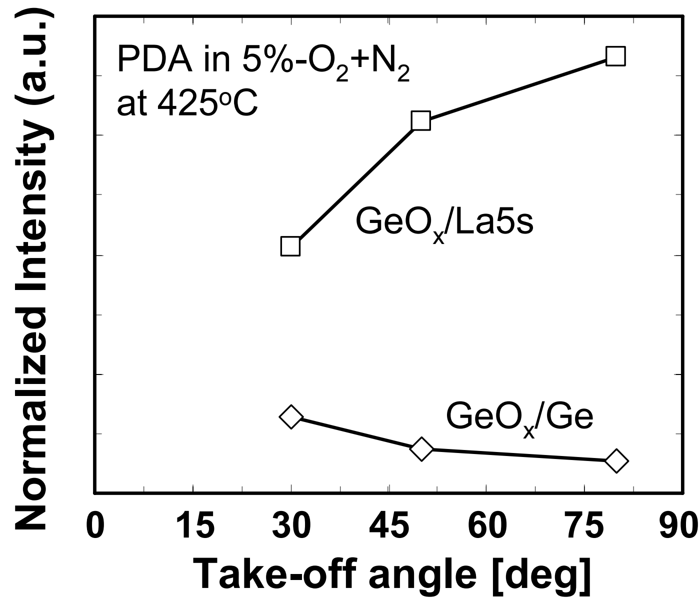


Figure 3-16. XPS spectra of Ge3d from Pt(1.5nm)/La_2O_3(4.5nm)/Ge structures with or without in-situ vacuum annealing before Pt electrode deposition. Spectra were normalized by La5s peak.

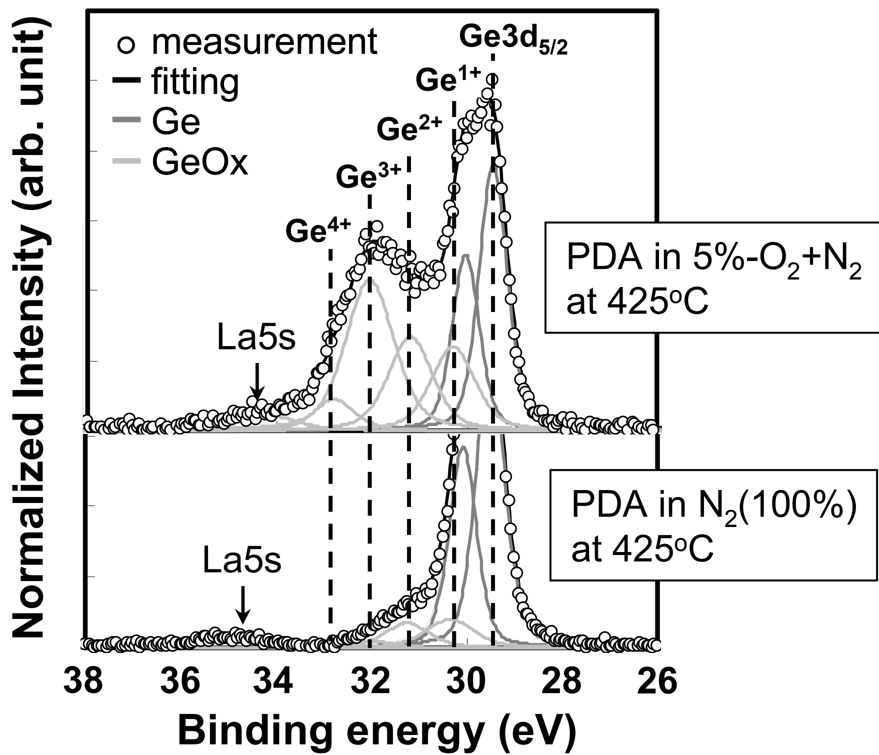
3.5 Improvement of Interfacial Properties by Interfacial Ge-oxide Layer

To confirm the improvement of interfacial properties by interfacial Ge-oxide layer and to investigate the properties of interfacial Ge-oxide, interfacial Ge-oxide layer was formed intentionally by performing PDA in 5%-O_2+N_2 ambient at various temperatures. Figure 3-17 shows XPS results of sample with PDA in 5%-O_2+N_2 ambient at 425°C for 5 minutes, which shows the interfacial Ge-oxide growth. The grown Ge-oxide layer were located in between La_2O_3 and Ge substrate as shown in figure 3-17(a) and Ge^{3+} increased significantly as shown in figure 3-17(b).

Figure 3-18 shows (a) 100kHz C-V characteristic and (b) interface trap density of Pt/La_2O_3/Ge MOS structure with PDA in N_2, 3%-H_2+N_2 (FG) and 5%-O_2+N_2 ambient at 425°C for 30 minutes. A huge kink was observed in N_2 and FG PDA, which has large amount of interface trap density as shown in figure 3-18.(b) In contrast, little kink appeared in 5%-O_2+N_2 PDA and interface trap density was smaller one order near the Fermi level rather than that in N_2 or FG. It is notable that interface trap density decreased with oxygen annealing in La_2O_3/Ge structure, while oxidation induced damages in HfO_2/Ge structure [53]. Moreover, the damages was recovered by FG annealing (FGA) in HfO_2/Ge structure, however, interfacial properties did not improved by FGA in La_2O_3/Ge structure.

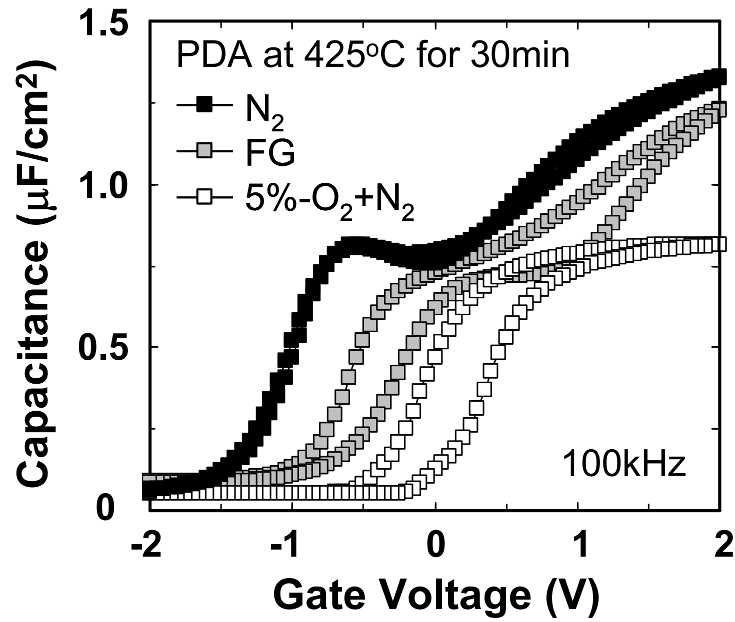


(a) The intensity ratio of GeO_x/La5s and GeO_x/Ge against take-off angle

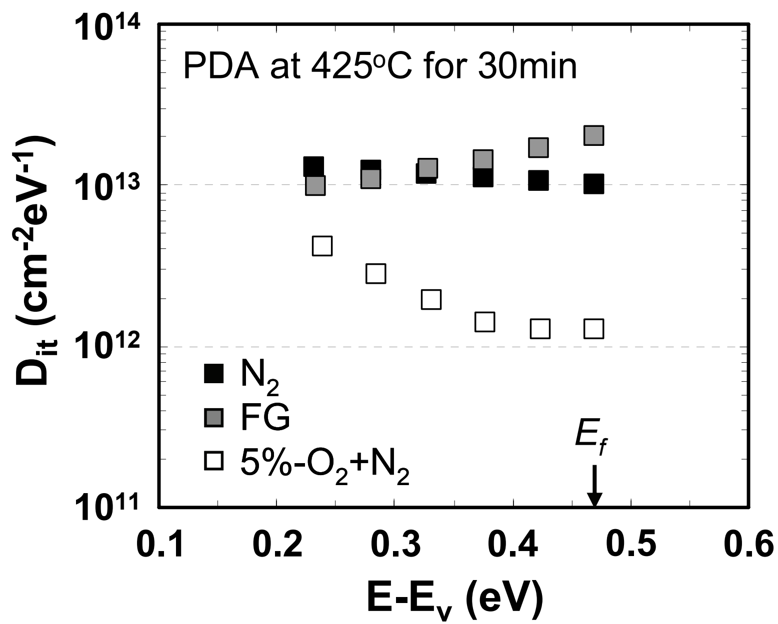


(b) Deconvoluted XPS spectra of Ge3d

Figure 3-17. XPS results of samples with PDA in 5%-O_2+N_2 ambient at 425°C and with PDA in N_2 at 400°C. Interfacial Ge-oxide layer increased with PDA in 5%-O_2+N_2 ambient at 425°C.



(a) 100kHz C-V characteristics



(b) Interface trap density

Figure 3-18. (a) 100kHz C-V characteristics and (b) interface trap density of samples with PDA in N_2, 3%-H_2+N_2 (FG) and 5%-O_2+N_2 ambient at 425°C for 30 minutes.

Figure 3-19 shows 1kHz~1MHz C-V characteristics of Pt/La_2O_3/Ge MOS structure with PDA in 5%-O_2+N_2 ambient at 425°C for 5 minutes. Less frequency dispersion and kink were observed in sample with PDA in 5%-O_2+N_2 compared to that with PDA in N_2 shown in figure 3-2, which suggests the decrease of interface trap density. Figure 3-20 shows 100kHz C-V characteristics of samples with PDA in 5%-O_2+N_2 at 400-500°C. Capacitance decreased with increasing annealing temperature, which suggests the increase of interfacial Ge oxide. Moreover, the kink of C-V curves decreased with increasing annealing temperature, there being no kink at 500°C PDA. The decrease of kink of C-V curves in proportion to reduction of interface trap density as shown in figure 3-21. The amount of hysteresis was almost same at all annealing temperature in 5%-O_2+N_2 ambient, however, the hysteresis in sample with PDA in 5%-O_2+N_2 at 500°C was larger than that of sample with PDA in N_2 at 500°C. This increase of hysteresis by PDA in 5%-O_2+N_2 at 500°C might be due to the large amount of Ge sub-oxide [16].

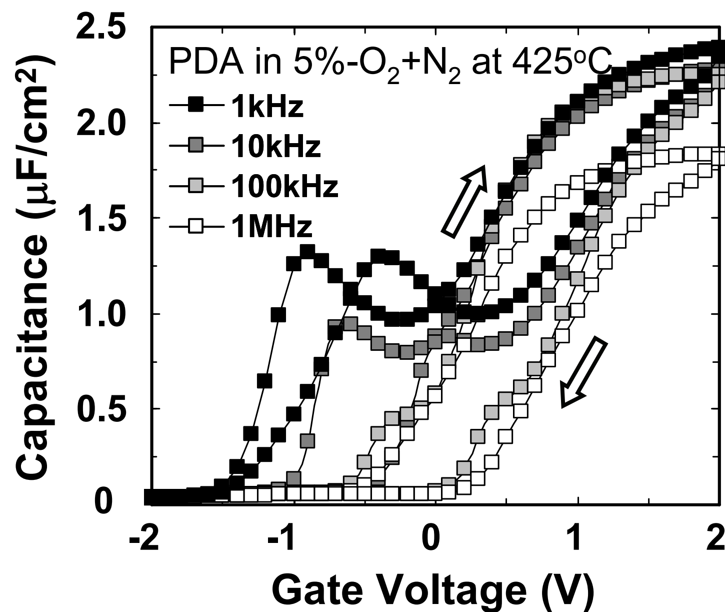


Figure 3-19. 1kHz~1MHz C-V characteristics of Pt/La_2O_3/Ge MOS structure with PDA in 5%-O_2+N_2 ambient at 425°C for 5 minutes.

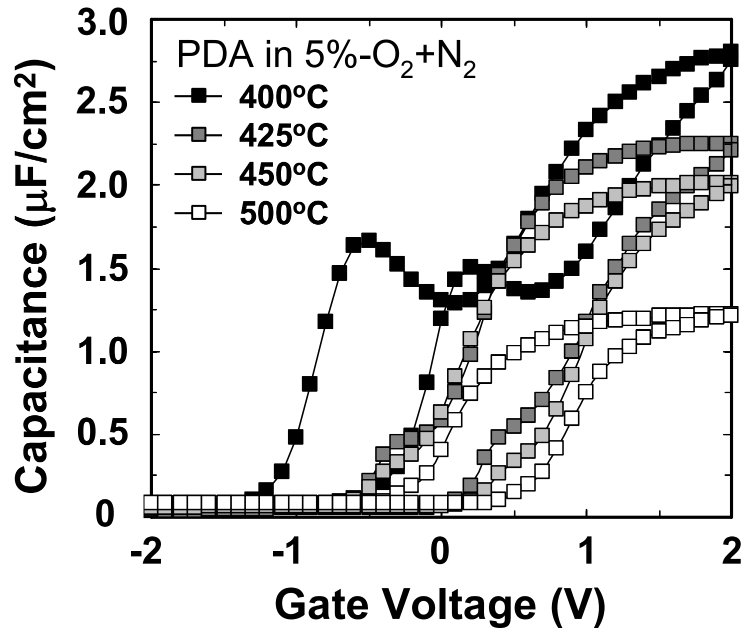


Figure 3-20. 100kHz C-V characteristics of samples with PDA in 5%-O_2+N_2 at 400-500°C for 5 minutes.

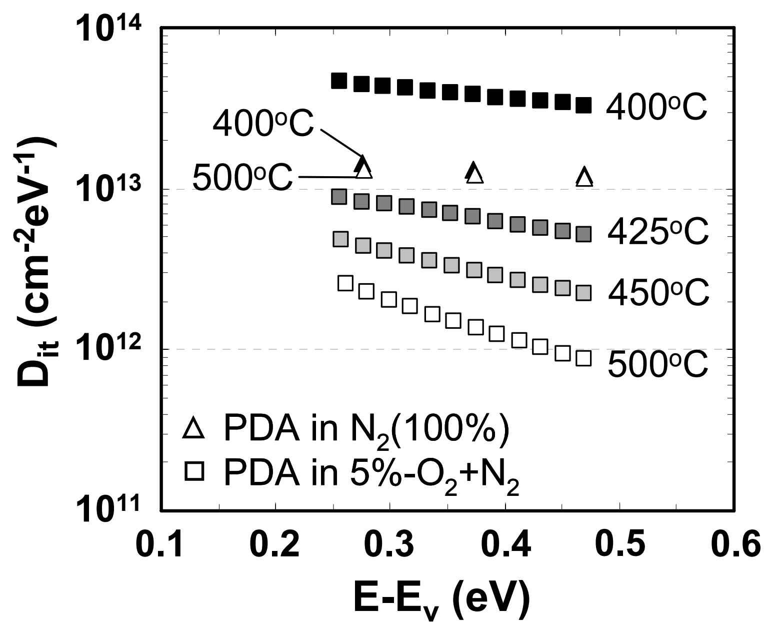


Figure 3-21. Interface trap density of samples with PDA in 5%-O_2+N_2 ambient at 400-500°C for 5 minutes.

Figure 3-22 shows the physical thickness change of La_2O_3 films in samples conducted PDA in N_2 or 5%-O_2+N_2, which was measured by spectroscopic ellipsometry. At the temperature of 400°C, the film thickness decreased in both PDA conducted in N_2 and 5%-O_2+N_2 ambient due to the densification of the La_2O_3 films. However, the film thickness increased significantly with increasing annealing temperature above 425°C in case of PDA in 5%-O_2+N_2 ambient, suggesting the growth of interfacial Ge-oxide layer, while film thickness with PDA in N_2 was almost same up to temperature of 600°C.

Similar results to those with PDA at various temperatures could be acquired in samples with PDA for various annealing time in 5%-O_2+N_2 ambient. Figure 3-23 shows 100kHz C-V characteristics of samples with PDA in 5%-O_2+N_2 for various annealing time at 425°C. With increasing annealing time, Capacitance and kink of C-V curves decreased, suggesting that growth of interfacial Ge-oxide layer increases. The thickness of films and CET increased in proportion to logarithmic order of annealing time as shown in figure 3-24.

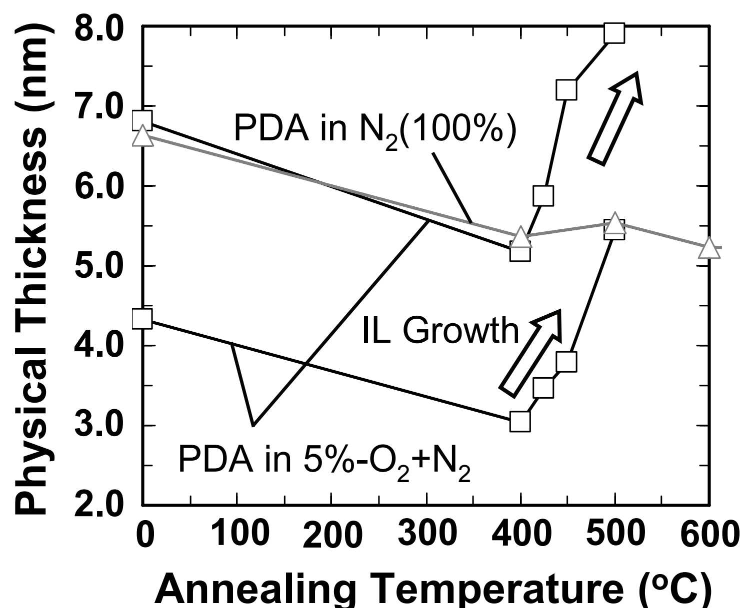


Figure 3-22. Physical thickness change of La_2O_3 films in samples conducted PDA in N_2 or 5%-O_2+N_2, which was measured by spectroscopic ellipsometry.

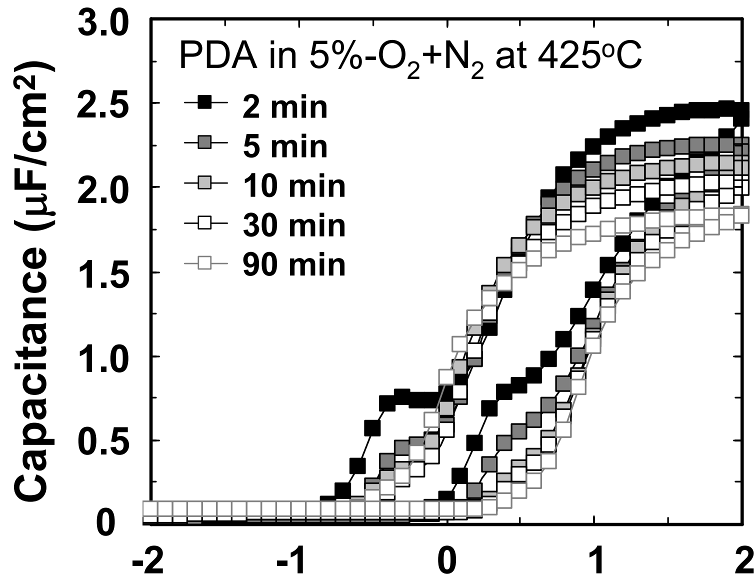


Figure 3-23. 100kHz C-V characteristics of samples with PDA in 5%-O_2+N_2 at 425°C for various annealing time

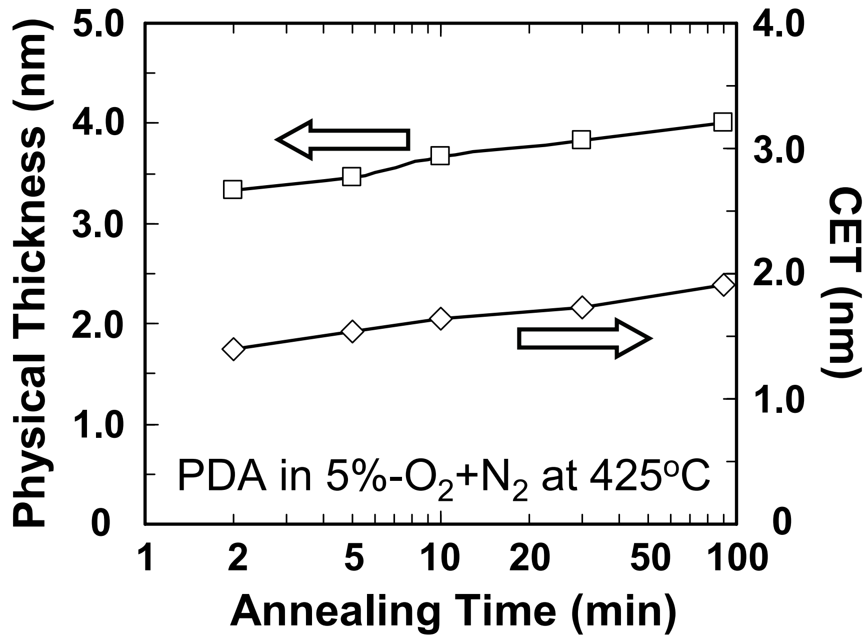


Figure 3-24. Physical thickness and CET change against annealing time. Physical thickness and CET increased in proportion to logarithmic order of annealing time.

Figure 3-25 shows CET changes in samples with PDA in 5%-O_2+N_2 ambient as a function of physical thickness. CET changes depend on annealing temperature or time. Considering that the increase of physical thickness and CET was due to the growth of interfacial Ge-oxide layer, dielectric constant of interfacial Ge-oxide layer was obtained from the slope in the figure 3-25 and the equation as shown below.

$$\Delta CET = \frac{\varepsilon_{SiO_2}}{\varepsilon_{GeO_x}} \Delta T_{phy} . \tag{3-1}$$

Here, ε_{SiO2} and ε_{GeOx} are dielectric constant of SiO_2 and interfacial GeO_x layer respectively. The calculated dielectric constant of interfacial Ge-oxide layer is 5.8~6.0, which is smaller than that in reference [54]. Considering that the dielectric constant of Ge and La_2O_3 are 16 and 27 respectively, as the dielectric constant of La-germanate would become much larger than the value of 6.0, the grown interfacial layer is not La-germanate but Ge-oxide clearly.

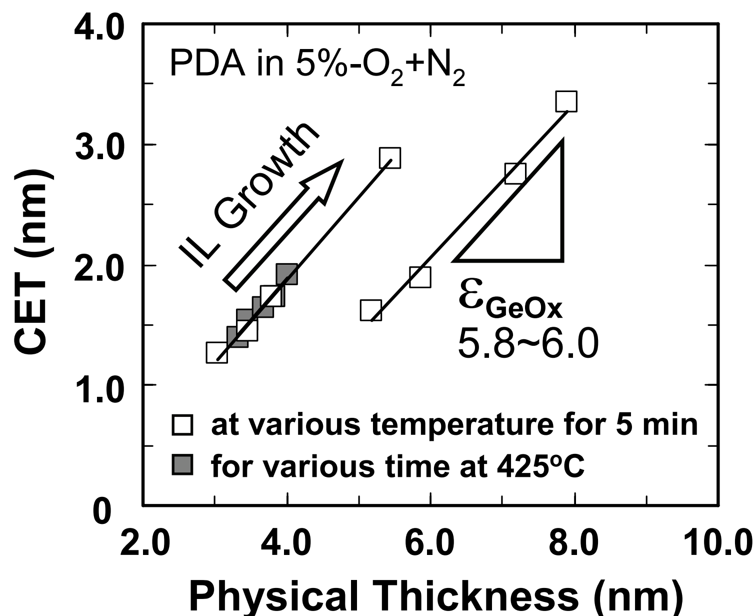


Figure 3-25. CET changes as a function of physical thickness, which depend on annealing temperature or time.

The physical thickness (PT) measured by spectroscopic ellipsometry actually consist of the physical thickness of La_2O_3 (PT_{La2O3}) and interfacial Ge-oxide layer (PT_{GeOx}), i.e.

$$PT = PT_{La_2O_3} + PT_{GeO_x} . \quad (3\text{-}2)$$

By treating the bilayer structure as two capacitors in series, we have

$$CET = CET_{La_2O_3} + CET_{GeO_x} . \quad (3\text{-}3)$$

On the other hand

$$PT_{La_2O_3} = \frac{\varepsilon_{La_2O_3}}{\varepsilon_{SiO_2}} CET_{La_2O_3} = \frac{\varepsilon_{La_2O_3}}{\varepsilon_{SiO_2}} (CET - CET_{GeO_x}) \quad (3\text{-}4)$$

and

$$PT_{GeO_x} = \frac{\varepsilon_{GeO_x}}{\varepsilon_{SiO_2}} CET_{GeO_x} . \quad (3\text{-}5)$$

Inserting Eq. 3-4 and 3-5 into Eq. 3-2 and rearranging, one can obtain

$$CET = \frac{\varepsilon_{SiO_2}}{\varepsilon_{La_2O_3}} PT + (1 - \frac{\varepsilon_{GeO_x}}{\varepsilon_{La_2O_3}}) CET_{GeO_x} . \quad (3\text{-}6)$$

From Eq. 3-6, CET_{GeOx} can be obtain easily by plotting CET against the physical thickness with different La_2O_3 film thickness and physical thickness of interfacial Ge-oxide layer can be calculated from Eq. 3-5.

Figure 3-26 shows CET versus physical thickness plot in samples with different La_2O_3 film thicknesses, which PDA was performed in 5%-O_2+N_2 ambient at 425-500°C. Dielectric constant of La_2O_3 films calculated from the slop is 18~19, which does not change by annealing temperature. This value is smaller than ideal one and other work, which was due to the water absorption of La_2O_3 films in air before deposition of gate electrode [55, 56]. Intercept of fitted lines to vertical axis at zero film thickness, which relates to interfacial layer thickness, is found to increase with

rise of annealing temperature as shown in figure 3-26. The calculated physical thickness of interfacial Ge-oxide layer from Eq. 3-5, 3-6 and figure 3-26 is 1.45, 1.97 and 3.70 nm with PDA at 425, 450 and 500°C respectively. The value of 1.45 nm with PDA at 425°C is lager than that of 1.1 nm from HR-TEM image in sample with La_2O_3 film of 3.5 nm thickness as shown in figure 3-27. This difference might be due to the values of CET not applied quantum mechanical correction. As the value of CET is commonly larger than that of EOT regarding quantum mechanical correction, the thicknesses of interfacial layer calculated from CET versus physical thickness plot were lager than that obtained from TEM and spectroscopic ellipsometry measurement as shown in figure 3-28.

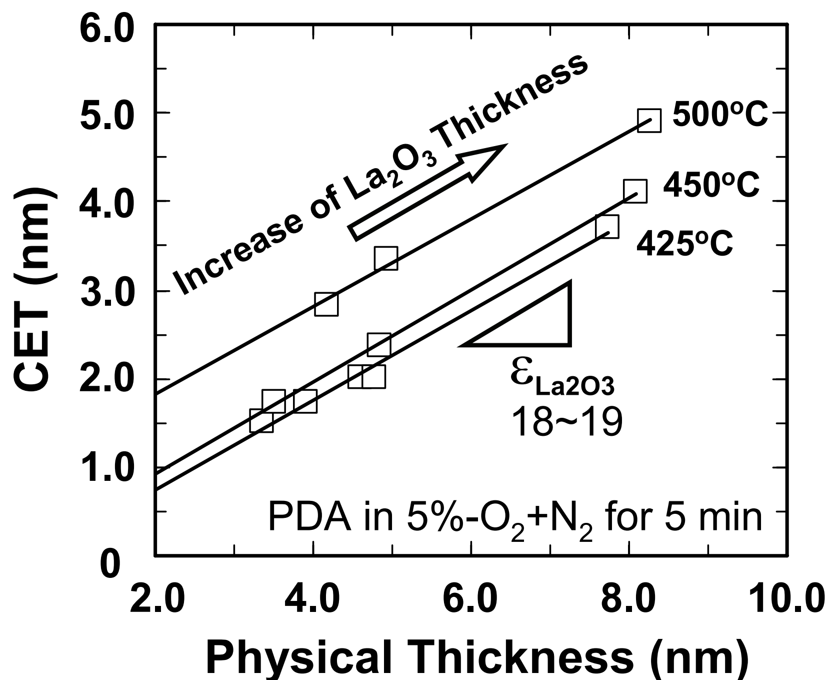


Figure 3-26. CET versus physical thickness plot in samples with different La_2O_3 film thicknesses, which PDA was performed in 5%-O_2+N_2 ambient at 425-500°C.

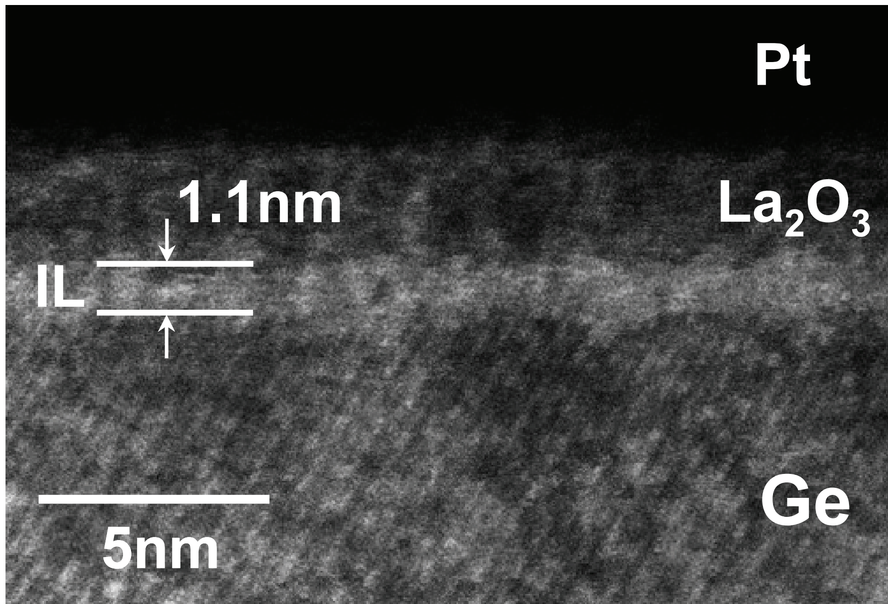


Figure 3-27. HR-TEM image of La_2O_3/Ge structure with PDA in 5%-O_2+N_2 at 425^oC for 5 minutes. The total film thickness is 3.5 nm and the thickness of the interfacial layer is 1.1 nm.

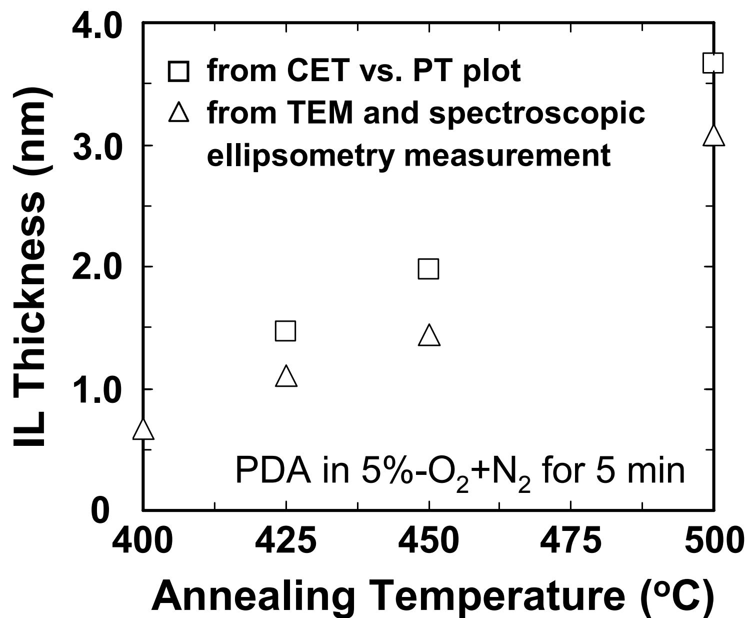


Figure 3-28. The thicknesses of interfacial layer calculated from CET versus physical thickness (PT) plot and obtained from HR-TEM image and spectroscopic ellipsometry measurement.

Figure 3-29 shows CET and interface trap density change against the thickness change of interfacial Ge-oxide layer, which interfacial layer thicknesses were estimated from HR-TEM images and spectroscopic ellipsometry measurement. The interface trap density was reduced significantly with increasing the interfacial layer thickness up to 1.5 nm, however, the decrease of interface trap density weakened over 1.5 nm. On the other hand, CET swelled with increasing the interfacial layer thickness relatively. Considering the both small CET and little interface trap density, appropriate thickness of the interfacial layer is regarded as the 1.0~1.5 nm.

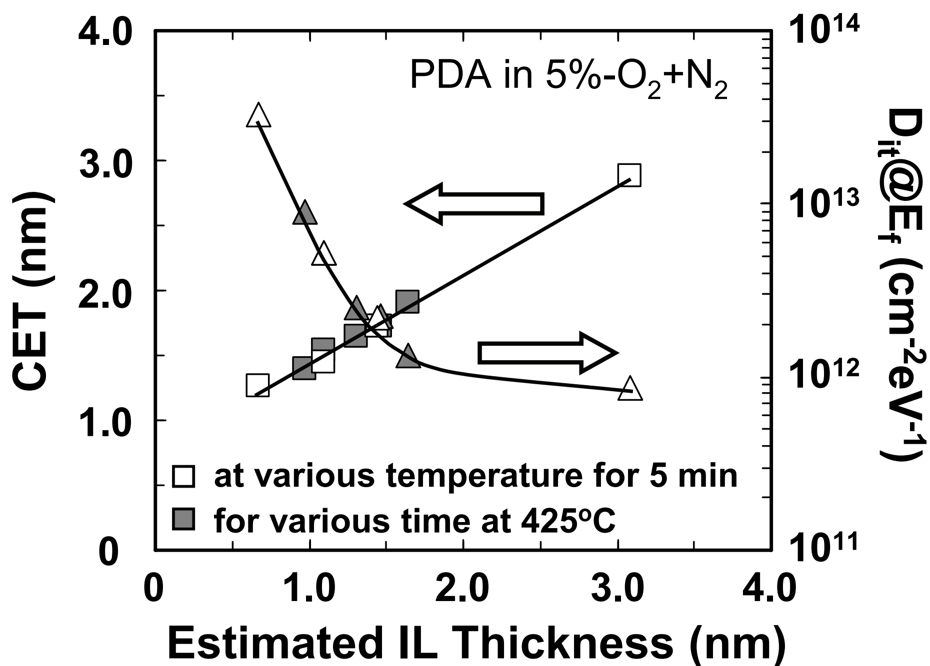


Figure 3-29. CET and interface trap density change against the thickness change of interfacial Ge-oxide layer, which interfacial layer thicknesses were estimated from HR-TEM images and spectroscopic ellipsometry measurement.

3.6 Conclusion

Interfacial properties between La_2O_3 and Ge substrate were studied under various annealing conditions. Interface trap density decreased with increasing interfacial Ge-oxide layer. However, interfacial Ge-oxide layer has low dielectric constant, which decreases capacitance of MOS capacitor. Considering the both small EOT and little interface trap density, appropriate thickness of the interfacial layer is regarded as 1.0~1.5 nm.

Chapter 4.

Study on PMA Process for Ge-based MOS Devices

4.1 Introduction

4.2 Experiments

4.3 Increase of Leakage Current in Pt/La_2O_3/Ge Structure with PMA

4.4 Characterization of Ge MOS Structure with Various Metal Gate Electrodes

4.5 Study on ***in situ*** Gate Electrode Formation Process using Tungsten

4.6 Conclusion

4.1 Introduction

For activation the source and drain region in self-align process and recrystallization after interconnection, post-metallization annealing (PMA) is crucial. To study on MOS structure using high-k materials, thermodynamic stability such as suppression of reaction between high-k materials and substrate or gate electrode during the PMA is very important fact. The interfacial properties between La_2O_3 and Ge substrate in Pt/La_2O_3/Ge structure with PMA were investigated in chapter 3. In this chapter, feasibility study in metal/La_2O_3/Ge structure performed PMA using various metal gate electrodes for Ge-based MOS devices. Moreover, in situ gate electrode formation process using tungsten was tried to prevent water absorption of La_2O_3.

4.2 Experiments

The fabrication process of Ge MOS capacitors is almost same as mentioned in chapter 3. Ge MOS capacitors were fabricated on n-type Ge (100) wafers with resistivity of 1.9~2.4 Ωcm. Ge wafers were cleaned by dipping in an HCl/H_2O (1/4) solution followed by rinsing in de-ionized water. After that a protective Ge Oxide layer was formed by NH_4OH/H_2O_2/H_2O (1/2/20) treatment at room temperature. The wafers were transferred into ultra-high vacuum (UHV) chamber (~10^{-8} Pa) and annealed at 600°C to remove the protective Ge oxide. La_2O_3 films were deposited by electron-beam evaporation using La_2O_3 tablet as a source under pressure of ~1×10^{-6} Pa at substrate temperature of 250°C. Gate electrode was formed by electron-beam evaporation with stencil shadow mask. Some samples were subjected to the metallization in situ after the deposition of La_2O_3, and gate electrodes were finally

lithographically patterned to form MOS capacitors in this case. After the metallization, PMA was carried out in N_2 ambient at 300^oC~700^oC for 5 or 30 minutes.

C-V characteristics, leakage current density, optical microscopy, HR-TEM and XPS measurements were performed to characterize electrical and physical properties of MOS structures.

4.3 Increase of Leakage Current in Pt/La_2O_3/Ge Structure with PMA

Being well known hardly to form an oxygen compound, Pt was often selected as a gate electrode in study of MOS devices using high-k materials, for Pt does not take the oxygen from high-k materials. In this reason, Pt electrode was also used in chapter 3 to concentrate the reaction of interface between La_2O_3 and Ge substrate. However, leakage current increased in PMA compared to PDA as shown in figure 4-1. This leakage current increase was getting lager with decreasing the L_2O_3 film thickness as shown in figure 4-2 and increasing the PMA time as shown in figure 4-3. As shown in figure 4-2, leakage current came to increase and disperse with film thickness around 7nm, and MOS capacitors almost broke at 6.3 nm thickness and below. Moreover, some extraordinary change was observed in surface of Pt electrode in sample with PMA at 600^oC as shown in figure 4-4. The leakage current increase and abnormal change in PMA might be due to the Ge diffusion and Pt-Germanide reaction considering the XPS analysis as shown below.

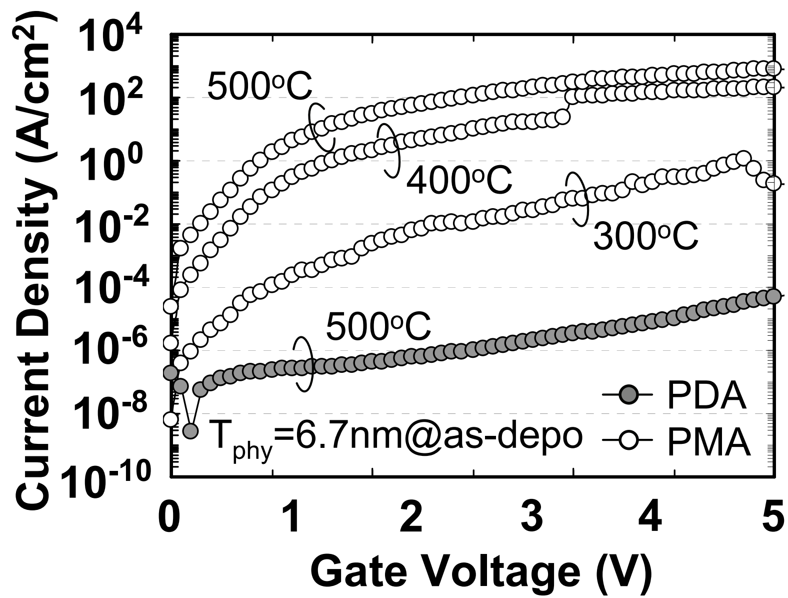


Figure 4-1. Leakage current density in samples with PMA or PDA at various temperatures. The film thickness of La_2O_3 is 6.7 nm at as-deposited condition.

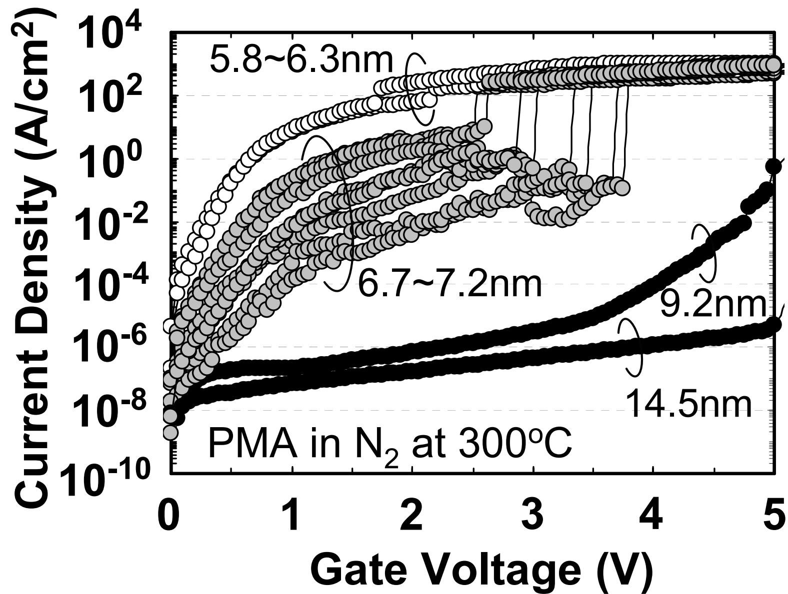


Figure 4-2. Film thickness dependence of leakage current density in samples with PMA at 300°C. Leakage current came to increase and disperse with film thickness around 7nm and below.

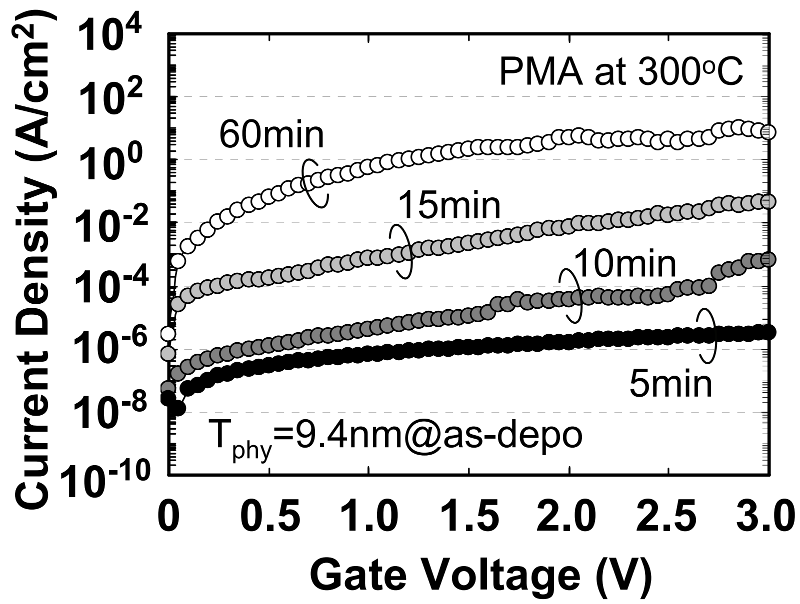


Figure 4-3. Annealing time dependence of leakage current density in samples with PMA at 300°C. Leakage current increased with increasing annealing time.

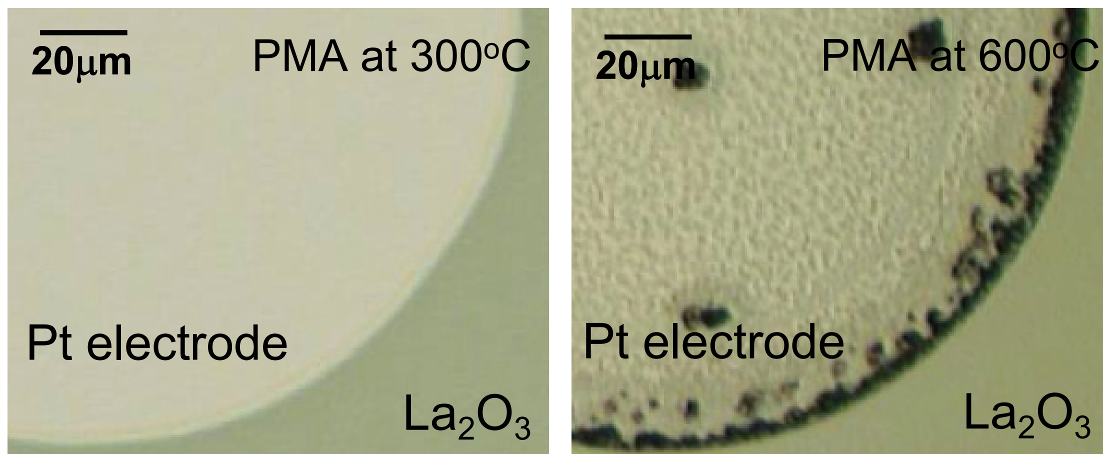


Figure 4-4. Optical microscopy images of Pt electrode in samples with PMA at 300°C and 600°C. Large amounts of stains were observed on Pt surface of sample with PMA at 600°C.

Figure 4-5 shows the XPS results of La_2O_3 film with thickness of 22 nm on Ge substrate, which was performed PDA at 600°C. As the source x-ray was monochromatized Al $K\alpha$ radiation (1486.7 eV), although the excited photoelectron could be escaped from depth of 7~8 nm maximally, the spectra of Ge-oxide was observed as show in figure 4-5. Moreover, the ratio of GeO_x intensity to La5s intensity increased with decreasing take-off angle as shown in figure 4-5 and 4-6, which means that Ge-oxide is located above La_2O_3. These suggest that Ge diffused to surface of La_2O_3 through the La_2O_3 of 22 nm thickness during PDA at 600°C, and abnormal change of Pt electrode as shown in figure 4-4 could be explained by the diffusion of Ge and Pt-germanide reaction at the electrode.

The leakage current increase observed in samples with PMA under 600°C might be also explained by Pt-germanide reaction in the La_2O_3 film. As Pt intermixes with Ge even at room temperature [57], diffused Ge and Pt - Pt diffusion might not be neglected, even if it was very small amount - could made Pt-germanide easily during annealing. Pt-germanide which existed in La_2O_3 film would be a leakage spot and whole leakage current increased by PMA, which schematic diagram is shown in figure 4-7.

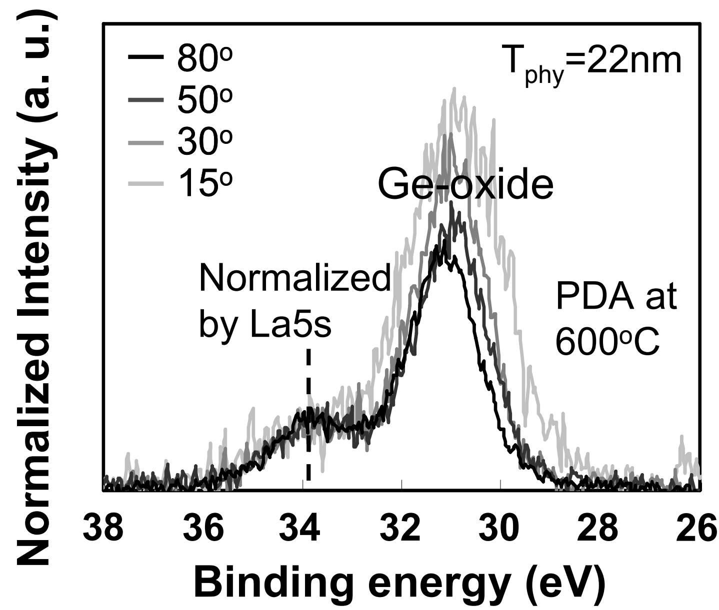


Figure 4-5. Angle-resolved XPS results of La_2O_3 film with thickness of 22 nm on Ge substrate, which was performed PDA at 600°C.

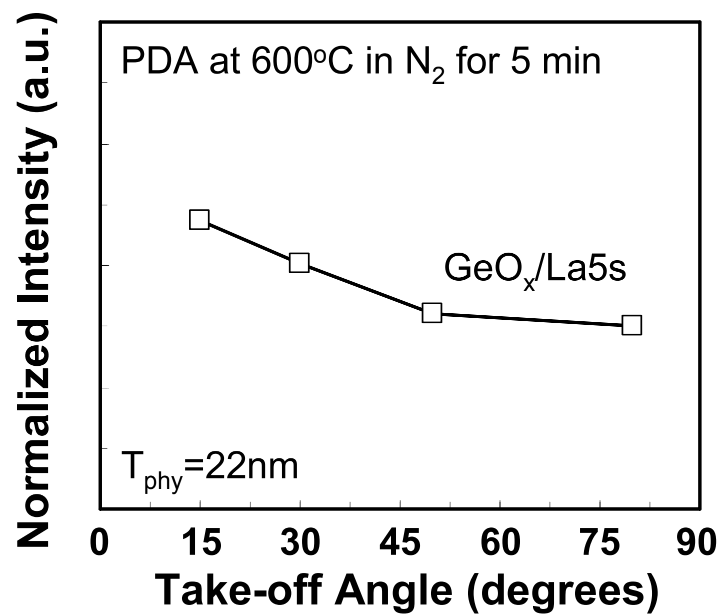


Figure 4-6. The ratio of GeO_x/La5s intensity calculated by angle-resolved XPS alaysis. The intensity of GeO_x to that of La5s increased with decreasing take-off angle

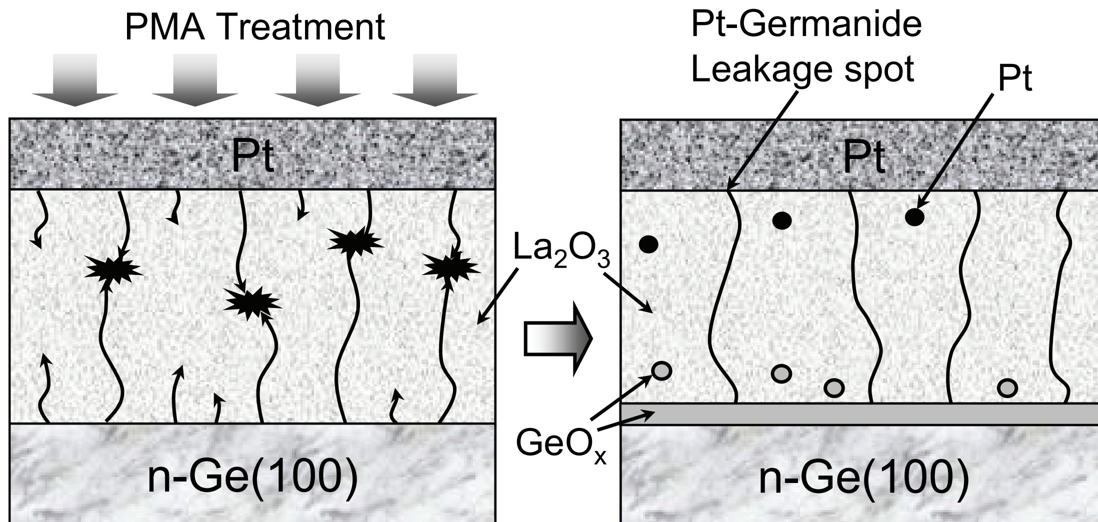
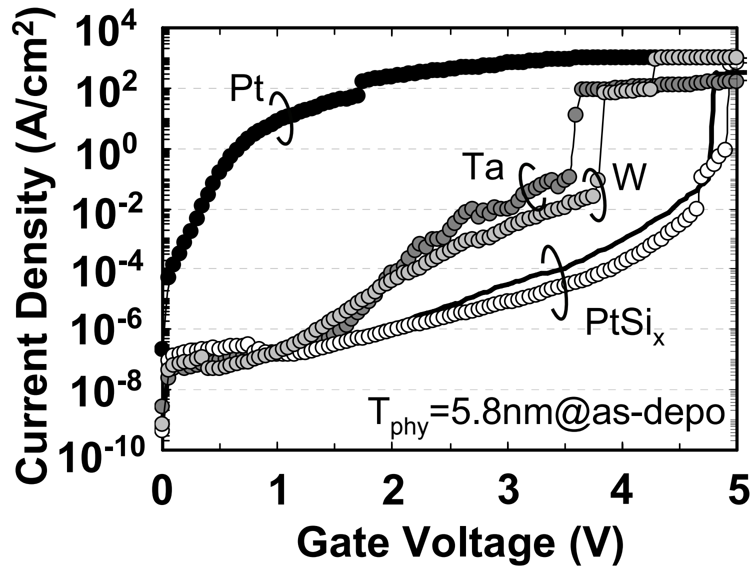


Figure 4-7. The schematic diagram of formation of Pt-germanide in La_2O_3 film during PMA, which become a leakage spot.

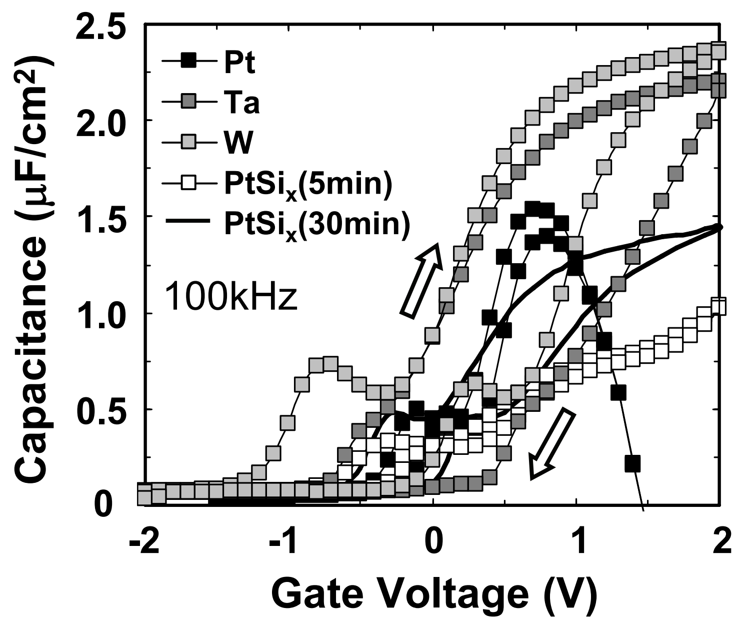
4.4 Characterization of Ge MOS Structure with Various Metal Gate Electrodes

The increase of leakage current by PMA was observed in Pt/La_2O_3/Ge structure, and the reason of the increase of leakage current might be due to the Pt-germanide reaction as shown above. In order to suppress the increase of leakage current with PMA, restraint of Ge and gate metal diffusion or control the metal-germanide reaction might be effective considering the results in chapter 4.3. Ge diffusion could be suppressed partially by Ge nitride or oxynitride layers; however this interfacial layer reduced the capacitance. Thus, metal/La_2O_3/Ge structures with PMA were characterized using various metals which are considered to react with Ge at high temperature. The basis of metal selection is reaction temperature of metal-silicide.

Figure 4-8 shows the leakage current density and 100kHz C-V characteristics in metal/La_2O_3/Ge structure with PMA at 300^oC using Pt, Ta, W and Pt-silicide ($PtSi_x$) as a gate electrode. All metals were deposited by electron-beam deposition and $PtSi_x$ were formed by reaction of deposited Si and Pt during PMA. PMA was conducted for 5 minutes except a sample using $PtSi_x$ electrode that was performed PMA for 30 minutes to use all Si to reaction with Pt, which is shown as solid line in figure 4-8. The leakage current in samples using alternative metals was reduced dramatically compared to that in sample using Pt electrode as shown in figure 4-8 (a). The leakage current except that in sample using Pt electrode was almost same up to 1.5V gate voltage, and the leakage current was less in sample using $PtSi_x$ electrode above 1.5V. On the other hand, leakage current with 30 minutes PMA increased a little compared to that with 5 minutes PMA in sample using $PtSi_x$ electrode. A large amount of difference was also observed in C-V characteristics with various metal electrodes as shown in figure 4-8 (b). The largest capacitance was obtained with W electrode and C-V characteristic was not measured completely with Pt electrode due to the large amount of leakage current. A large amount of hysteresis observed in samples with W and Ta electrode might be generated due to the dangling bond as metal electrode took oxygen from La_2O_3 considering lower Gibbs free energy of W-O and Ta-O formation compared to La-O formation [58, 59, 60]. The lower capacitance of sample with $PtSi_x$ electrode could be explained reaction of La-silicate during the annealing and Si might have remained with 5 minutes PMA.



(a) Leakage current density



(b) 100kHz C-V characteristics

Figure 4-8. Leakage current density and C-V characteristics in metal/La_2O_3/Ge structures with PMA at 300^oC using Pt, Ta, W and Pt-silicide ($PtSi_x$) as a gate electrode.

Figure 4-9 shows leakage current density at 1V against CET in samples with various metal electrodes, which PMA was performed at 300°C and 500°C. The data of sample using Pt electrode is not included because exact CET can not be calculated due to the large amount of leakage current. As shown in figure 4-9, though leakage current increased with PMA at 500°C in all samples, sample using W electrode shows the smallest CET with the less leakage current.

Figure 4-10 shows the leakage current of samples using W electrode with PMA at 300-700°C. As shown in figure 4-10, the leakage current increased with 500°C PMA, moreover the mechanism of leakage current also seemed to change. This result suggests that W-germanide was formed in La_2O_3 film at 500°C.

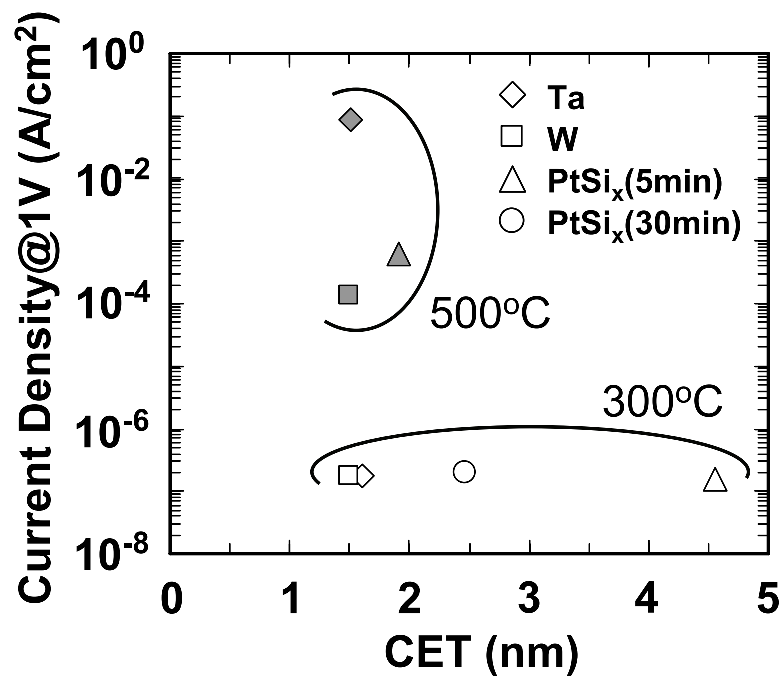


Figure 4-9. The plot of leakage current density at 1V against CET in samples using various metal electrodes, which PMA was performed at 300°C and 500°C

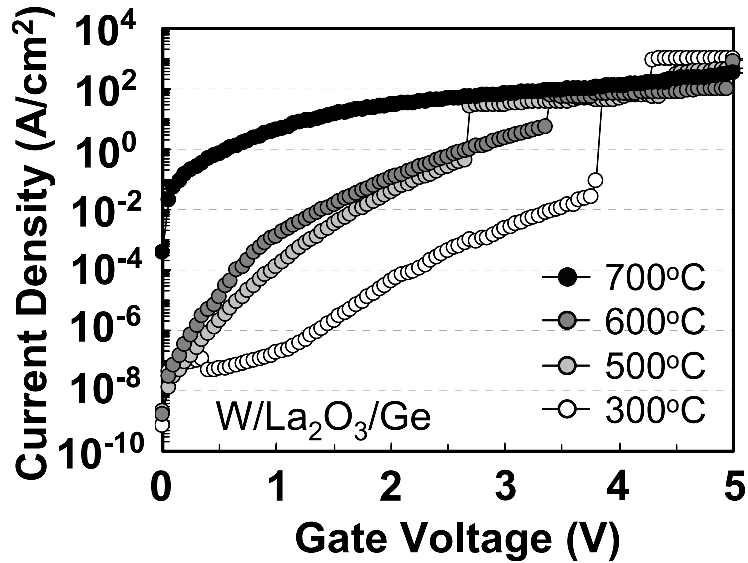
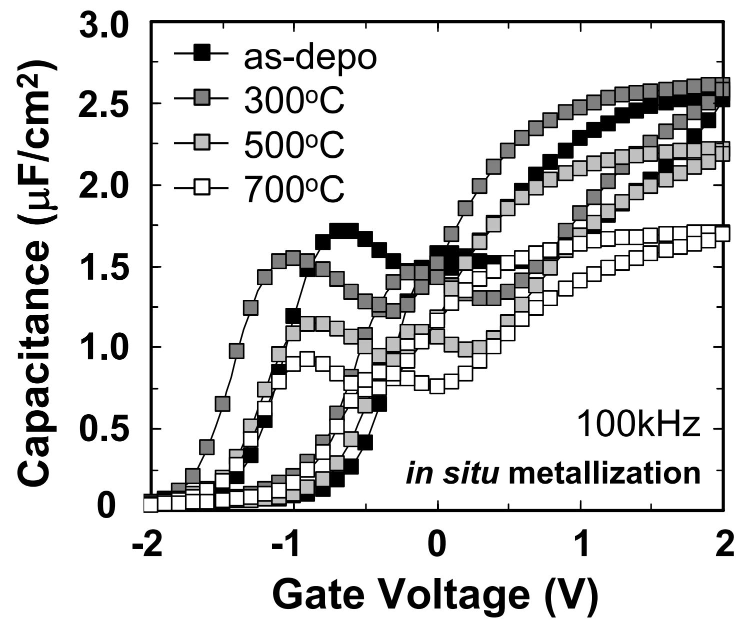


Figure 4-10. Leakage current density of samples using W electrode with PMA at 300-700°C.

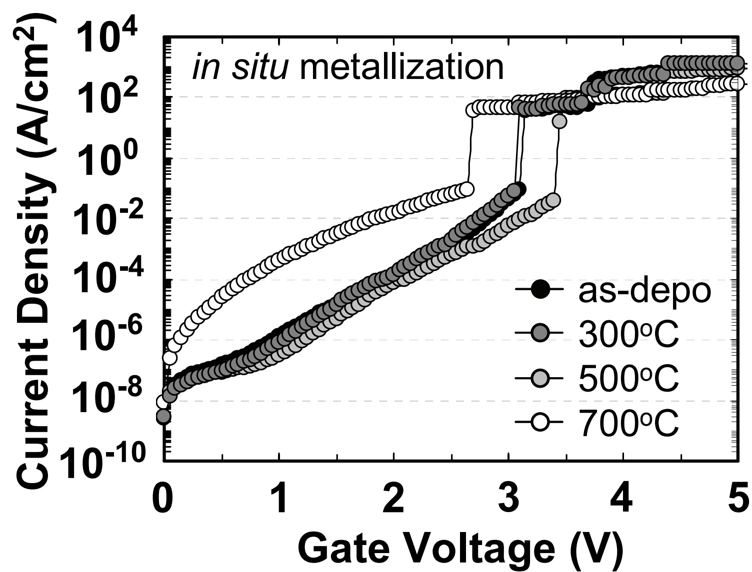
4.5 Study on ***in situ*** Gate Electrode Formation Process using Tungsten

For prevention of water absorption of La_2O_3 which reduced the dielectric constant [55], tungsten gate electrode was deposited in situ using electron-beam evaporation method after the deposition of La_2O_3. Figure 4-11 shows (a) 100kHz C-V characteristics and (b) leakage current density of samples formed gate electrode in situ, which was conducted PMA at 300°C~700°C. As shown in figure 4-11, capacitance once increased a little with PMA at 300°C; however it decreased with PMA above 500°C. Moreover, the kink of C-V curves diminished with increasing PMA temperature, which related the reduction of interface trap density as shown in figure 4-13. Decrease of capacitance and reduction of interface trap density suggest the growth of interfacial layer as shown in chapter 3. As shown in figure 4-12, the leakage

current is almost same up to 500°C and increase of leakage current and change of leakage current mechanism appeared at 700°C.



(a) 100kHz C-V characteristics



(b) leakage current density

Figure 4-12. (a) C-V characteristics and (b) leakage current density of samples formed gate electrode *in situ*, which was conducted PMA at 300°C~700°C.

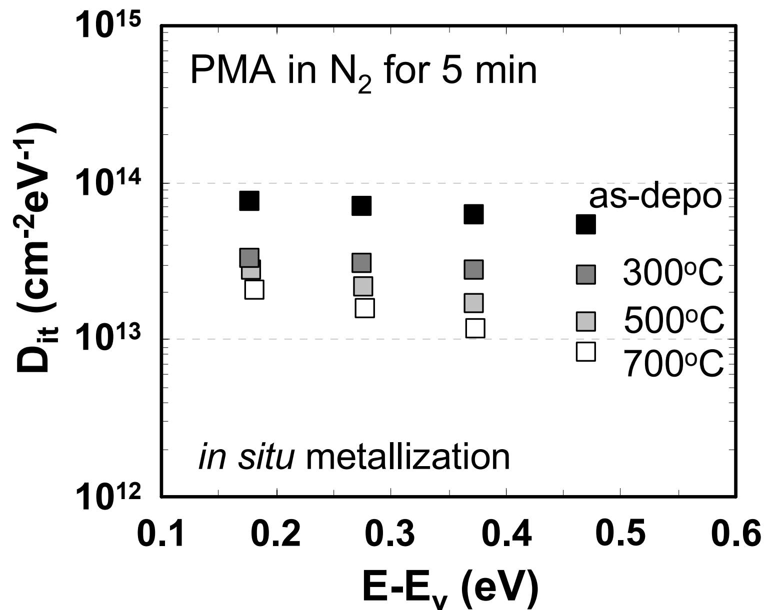


Figure 4-13. Interface trap density of samples formed gate electrode *in situ*, which was conducted PMA at 300°C~700°C.

Figure 4-14 shows the CET and leakage current change against the PMA temperature in sample with W electrode deposited *ex situ* or *in situ*. Almost same characteristics was showed in both *in situ* and *ex situ* metallization at 300°C PMA, however notable point is leakage current suppression with in situ metallization at 500°C PMA which is sufficiently high for activation the source and drain region for Ge MOSFET.

Figure 4-15 shows the leakage current density at 1V against CET in Ge-MOS devices using various high-k materials as gate dielectric. The data of La_2O_3 was from the samples with *in situ* W metallization, which PMA was conducted at 300-700°C. Very small CET with low leakage current achieved with La_2O_3 gate dielectric at 500°C, which is sufficiently high for activation the source and drain region for self-align process of Ge MOSFET.

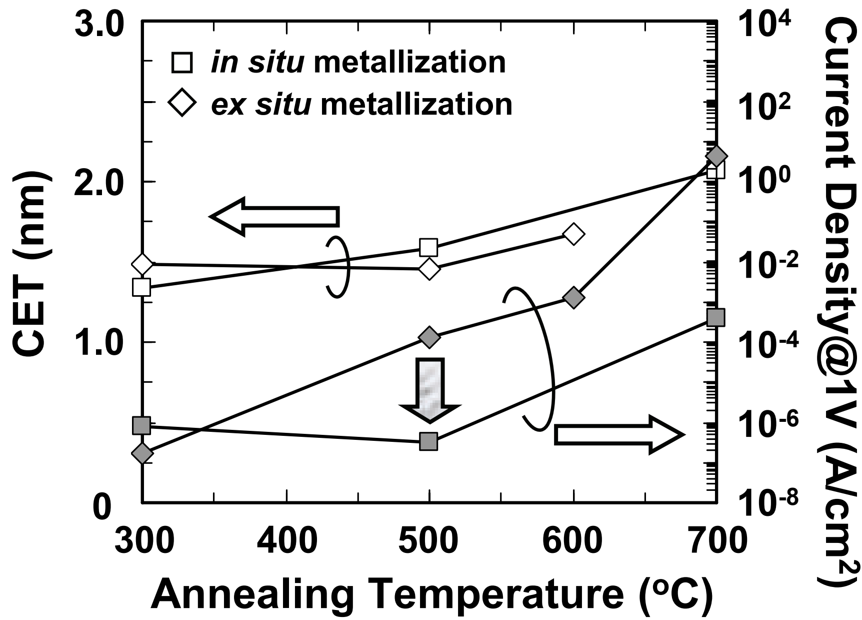


Figure 4-14. CET and leakage current change against the PMA temperature in sample with W electrode deposited *ex situ* or *in situ*.

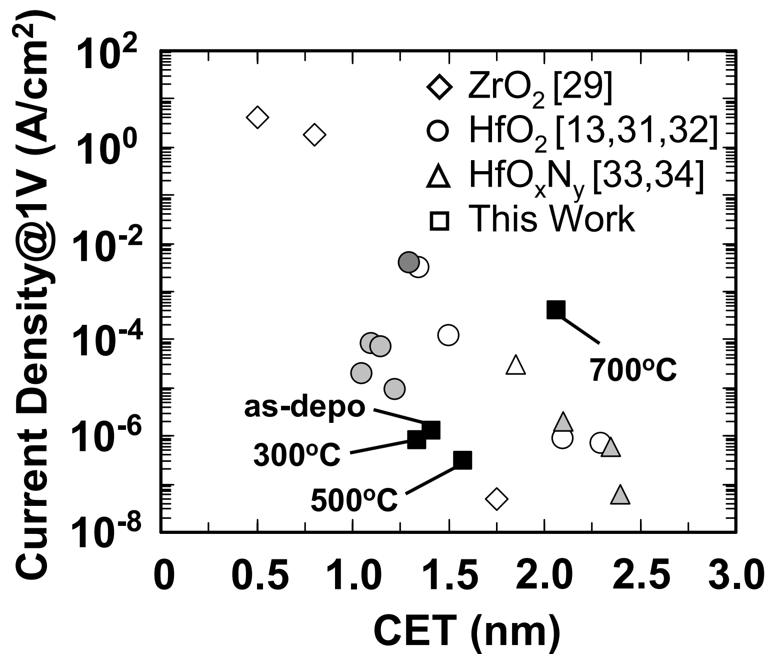


Figure 4-15. Leakage current density at 1V against CET in Ge-MOS devices using various high-k materials as gate dielectric. Very small CET with low leakage current achieved with La_2O_3 gate dielectric.

4.6 Conclusion

In this chapter, post-metallization annealing (PMA) was studied on metla/La_2O_3/Ge structure for self-align process of Ge-MOSFET. In case of Pt electrode, leakage current increased with PMA, which might be due to the Pt-germanide reaction of diffused Ge and Pt during PMA considering optical microscopy and XPS results. This leakage current increase with PMA was resolved by using W, Ta and $PtSi_x$ as a gate electrode. Among that gate electrode, smallest CET with less leakage current was achieved with W electrode. Moreover, very small CET with low leakage current achieved at 500°C with *in situ* W metallization, which is sufficiently high temperature for activation the source and drain region for self-align process of Ge MOSFET.

Chapter 5.
Conclusions

5.1 Results of this Study

5.2 Discussion to the Further Work for L_2O_3/Ge Structure

5.1 Results of this Study

Due to the scaling limit of Si-MOS devices with SiO_2, new channel material and alternate gate dielectric were necessary for further device improvement. In this study, Ge-MOS structures with La_2O_3 gate dielectric were investigated under various annealing conditions.

5.1.1 Interfacial Properties of La_2O_3/Ge

As the interfacial properties between high-k and substrate are very influential to device performance, interfacial properties between La_2O_3 and Ge substrate were studied under various annealing conditions. Interface trap density decreased with increasing interfacial Ge-oxide layer. However, interfacial Ge-oxide layer has low dielectric constant, which would decrease capacitance. Considering the both small EOT and little interface trap density, appropriate thickness of the interfacial layer is regarded as 1.0~1.5 nm.

5.1.2 Improvement of Thermal Stability on PMA

Post-metallization annealing (PMA) in metla/La_2O_3/Ge structure was studied for self-align process of Ge-MOSFET. In case of Ge-MOSFET, necessary temperature for activation the source and drain region is about 500°C, which is not so high temperature. With Pt electrode, leakage current increased by PMA at even 300°C compared to PDA, which might be due to the Pt-germanide reaction of diffused Ge and Pt during PMA. This leakage current increase with PMA was resolved by using W, Ta and $PtSi_x$ gate electrode which was considered to react to Ge at high tempaerature. Among that gate electrode, smallest CET with less leakage current was achieved with W electrode. Moreover, very small CET with low leakage current achieved at 500°C

PMA with *in situ* W metallization, which is sufficiently high temperature for activation the source and drain region for self-align process of Ge MOSFET.

5.2 Discussion to the Further Work for L_2O_3/Ge Structure

The interface trap density in La_2O_3/Ge MOS structure decreases with Ge-oxide layer between La_2O_3 and Ge substrate. In this study, interfacial Ge-oxide layer was grown by annealing in oxygen ambient, however suboxide increased also in this way. As this suboxide has a responsible for large amounts of hysteresis, generation of suboxide should be suppressed. To achieve the decrease in both interfacial layer and hysteresis, passivation of Ge substrate by GeO_2 layer without suboxide before the La_2O_3 deposition would be effective. Chemical oxidation by H_2O_2 or thermal oxidation under 450^oC could be formed GeO_2 with little suboxide.

On the other hands, as the GeO_2 layer that has lower dielectric constant increases the CET, it is necessary to control the interfacial GeO_2 layer. Thus, suppressing the formation of Ge suboxide, introduction of alternate interfacial layers that have larger dielectric constant rather than Ge-oxide is also practical to raise the performance of Ge-MOS devices with La_2O_3. It seems that Y_2O_3 and Sc_2O_3 are proper to the alternate interfacial layer. Being same rare earth oxide, Y_2O_3 and Sc_2O_3 have stronger affinity for oxygen rather than La_2O_3 and larger dielectric constant rather than GeO_2. Moreover, Ge_3N_4 might be also effective for interfacial layer of La_2O_3/Ge structure, as it has been reported that no hysteresis was observed in Ge_3N_4/Ge structure [25].

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