Master Thesis

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Novel Rare Earth Oxides Gate Stack for Advanced La_2O_3-MOSFET

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Chapter 1

Introduction

1.1 Background of This study

Today, the modern human society are becoming affluent for high technology electric products such as personal computer, mobile phones, video game machines, digital cameras, and human-like robot. These products are used various ultra-large-scale integration (ULSI). The Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) are the basic building block of the current ULSI integrated circuits (ICs). The performance of silicon ULSI depends on the capability of the MOSFET, especially the processing speed and electrical power dissipation which are hanged on the geometrical size of MOSFET.

Gordon Moore who is one of the founder of Intel Corporation, predicted that exponential growth in the number of transistors per integrated circuit and predicted this trend would continue, in a popular article written in 1965[1]. Figure1.1 shows Moore's original prediction. His prediction is popularly known as "Moore's Law". Moore's Law states that the number of transistors on integrated circuits doubles approximately every 24 months, resulting in higher performance at lower cost. This simple statement is the foundation of semiconductor and computing industries. It is the basis for the exponential growth of computing power, component integration that has stimulated the emergence of generation after generation of PCs and intelligent devices. As a practical matter, figure1.2 shows that the number of transistors on the intel's Central Processing Unit (CPU), with the first microprocessor, 4004, to the recent Pentium® 4 microprocessor. The total number of transistors on microprocessor was increased double every 18-24 months. It was applied well to the Moore's Law. [2]

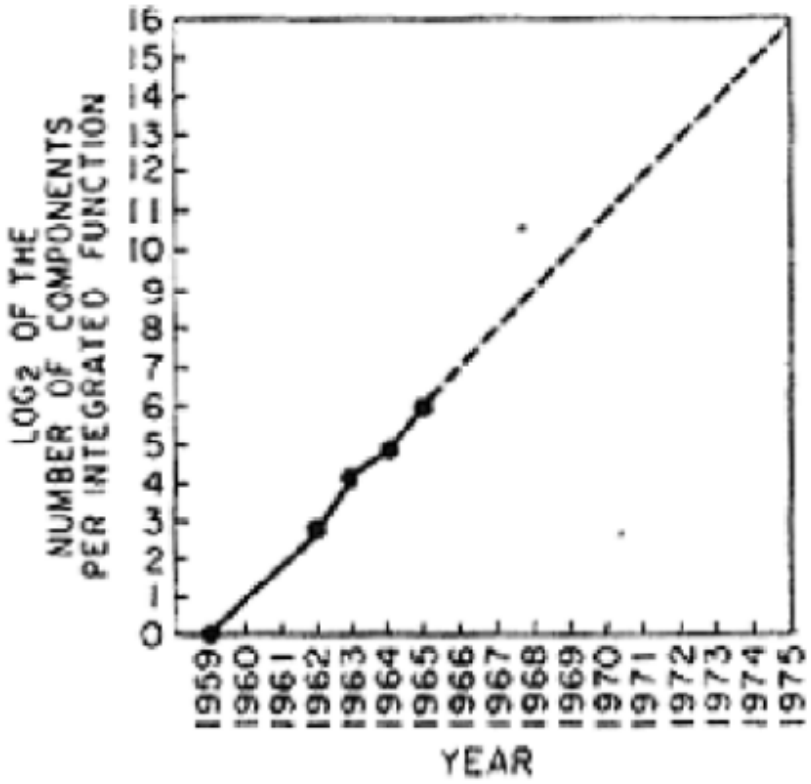


Figure1.1: Moore's original transistor prediction in 1965[1]

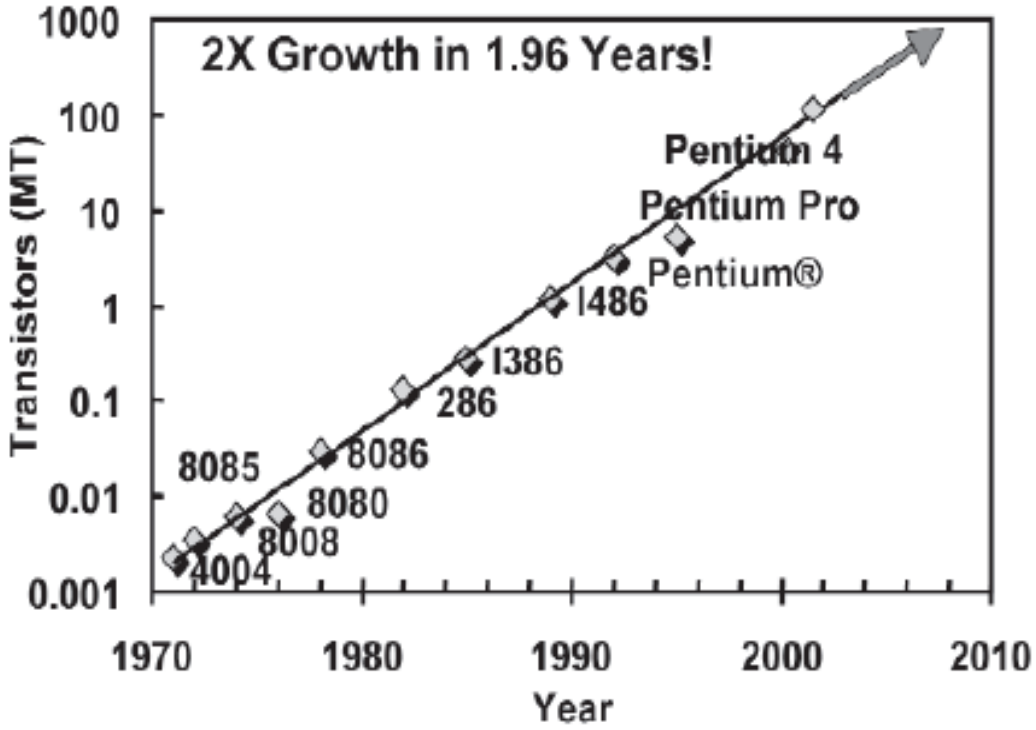
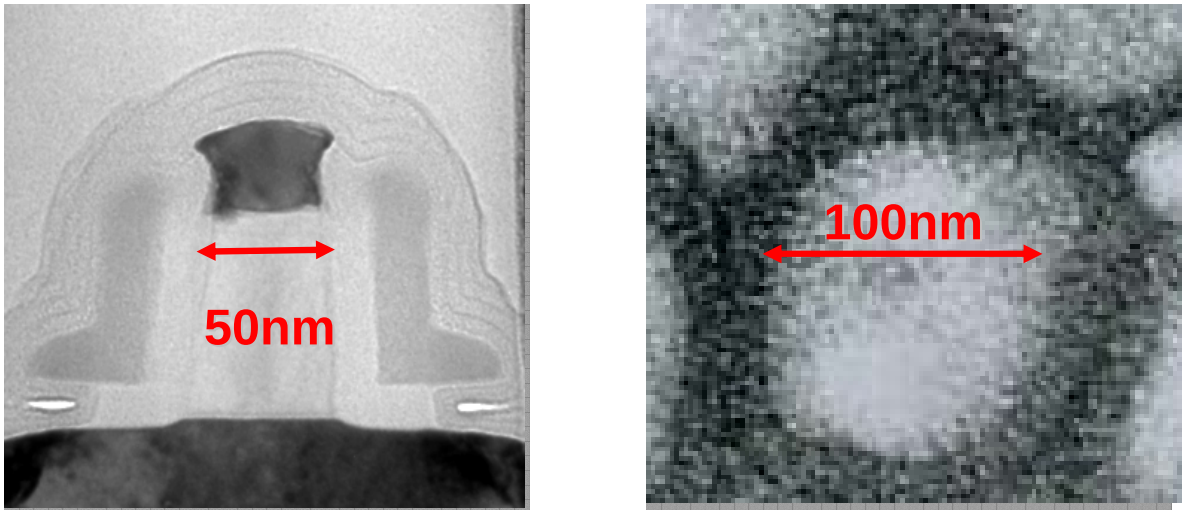


Figure1.2: The number of transistors on microprocessor from 1971 to 2001[2]

As the miniaturization of MOSFETs follow the Moore's Law, the gate length of 90nm-node transistor will be about 50nm which size is less than the influenza virus.[2] It occurs that the traditional silicon dioxide (SiO_2) gate dielectric becomes just a few atomic layers thick, which induce the tunneling current leakage and the resulting in the increasing power dissipation and heat become critical issues. At ISSCC2001[3], Patrick P. Gelsinger who is senior vice president of Intel Corporation, predicted that the power consumption of the microprocessor would reach 10 kW with 25 nm gate length CMOS under 30 GHz clock operation, if the current trend continues to 2008. If nothing changes these chips will produce as much heat, the heat generation at the surface of the silicon chip would become tremendously high at the same level of a nuclear reactor, a rocket nozzle, and the sun surface, in the future. Lately a lot of researches for miniaturization of MOSFET are struggle to find out the possibilities of technological advancement of MOSFETs for high performance LSI system.



(a)Transistor for 90nm-node **(b) Influenza virus**

Figure1.3: Comparison of the size (a)Transistor (b)Influenza virus

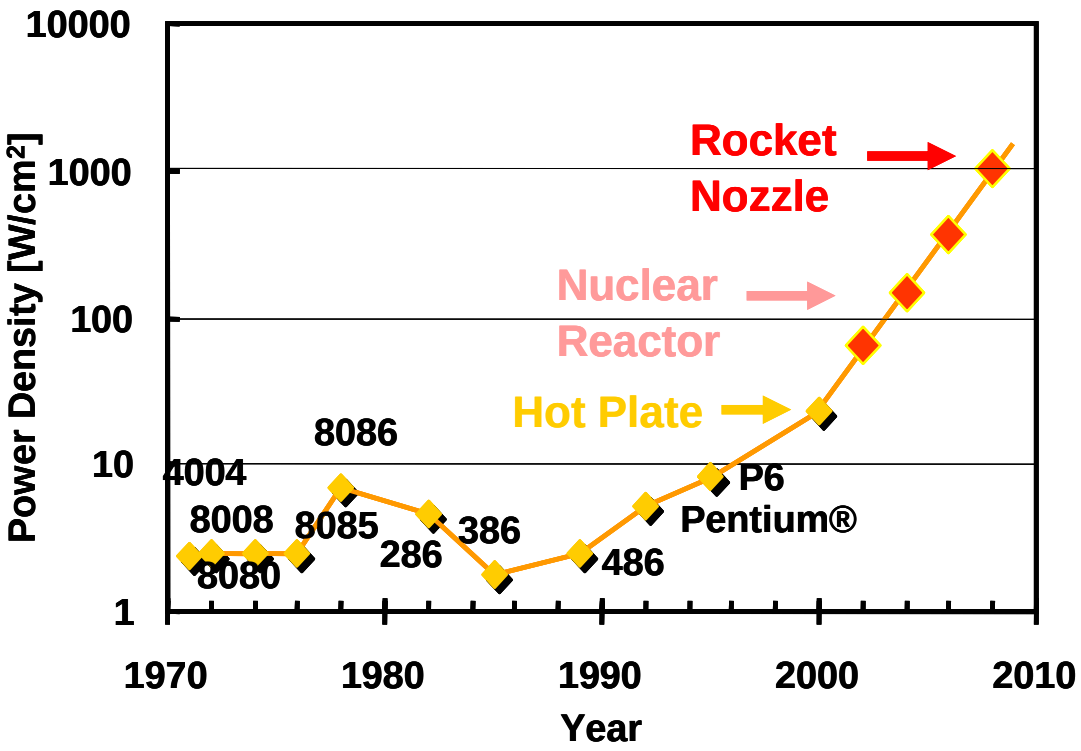


Figure1.4: Power density on microprocessor

1.2 Scaling Limits of SiO_2 Gate Dielectric

It is well known that Silicon dioxide film (SiO_2) is the most common materials as gate insulator film for MOSFET. The miniaturization of MOSFET follows the scaling law. Figure 1.5 and table 1.1 explain the scaling law of MOSFET. Each parts of the MOSFET are downsized with the same coefficient S. As a result of downsizing, LSI system as a whole will obtain the S times better performance, in theory.

The International Technology Roadmap for Semiconductors (ITRS) [4] is the result of an industry-wide cooperative effort to project the progression of IC technology over the next 15 years. The goal is to aid the IC industry in continuing to follow the Moore's Law so that the industry can continue to enjoy the resulting rapid rate of performance, density, power, and cost improvement during that period.

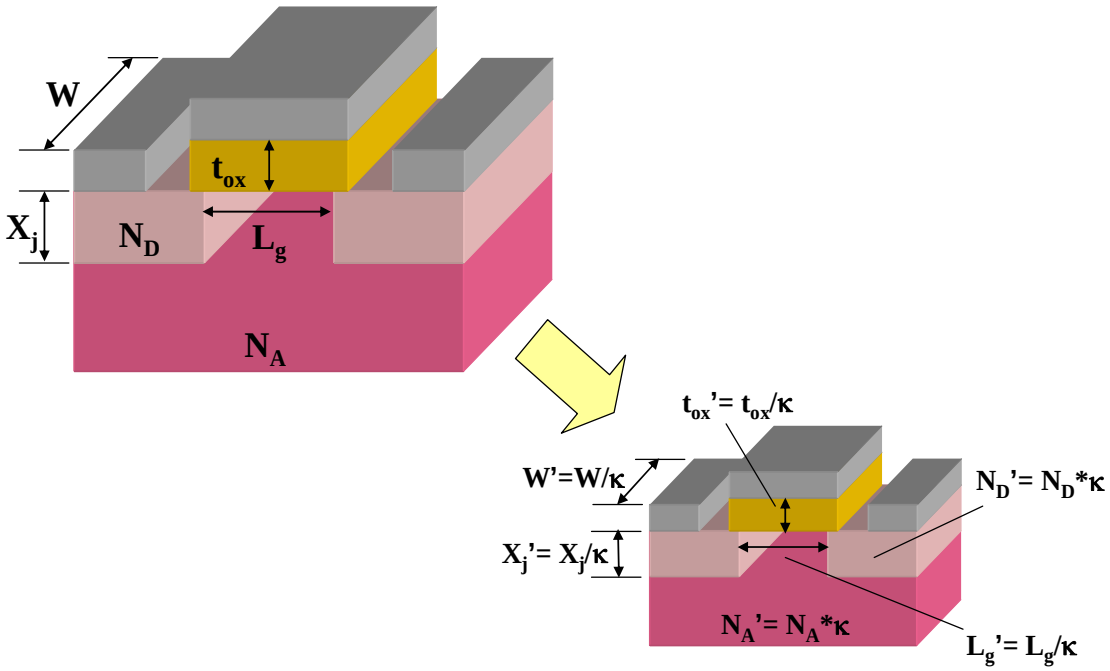


Figure 1.5 : Scaling Method.

Table 1.1 : Scaling of MOSFET by the scaling factor κ.

Parameter	Inisial	Scaled
Channel Length	L	L/κ
Channel Width	W	W/κ
Total Device Area	A	A/κ^2
Gate Oxide Thickness	t_{ox}	t_{ox}/κ
Gate Capacitance	C_{ox}	$C_{ox}*\kappa$
Junction Depth	X_j	X_j/κ
Power Supply Voltage	V_{dd}	V_{dd}/κ
Threshold Voltage	V_{th}	V_{th}/κ
Doping Concentration	N_A	$N_A*\kappa$
	N_D	$N_D*\kappa$

Table 1.2 shows the 2006 update of the ITRS, which suggests Equivalent Oxide Thickness (EOT) will be required under 1nm level in near future. On the other hand, the direct-tunneling leakage current is too increasing to be neglected as shown in Figure 1.6. Therefore, SiO_2 gate oxide film reaches its limit so that an alternative material gate insulator, such as high-k material is required to continue the scaling down of MOS transistors.

Table 1.2 : ITRS 2006 update[4]

Year of roduction	2005	2006	2007	2008	2009
Physical Gate Length	32	28	25	23	20
EOT	1.2	1.1	1.1	1.0	0.9
Gate Leakage Current Density [A/cm^2]	1.8*10^2	5.4*10^2	8.0*10^2	1.2*10^3	1.1*10^3
Power Supply Voltage [V]	1.1	1.1	1.1	1.1	1.0

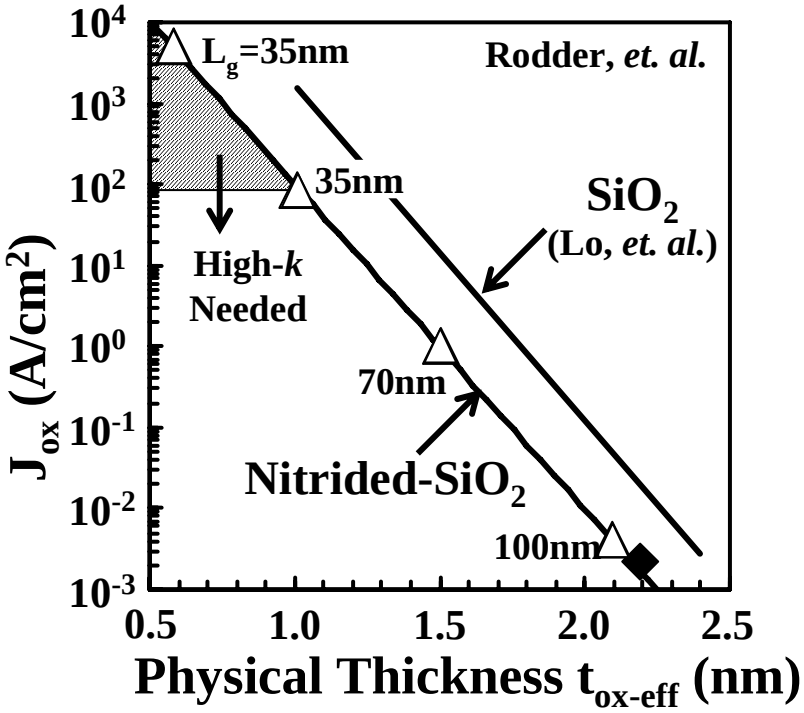


Figure 1.6 Relations between gate leakage current and physical thickness of SiO_2 and SiON film

1.3 Requirements of high-k materials

The high dielectric constant (high-k) materials have been attracted to suppress the leakage current. The key guidelines for selecting an alternative gate dielectric material are high dielectric constant, large band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability. Among them, high dielectric constant and large band gap are the minimum required characteristics to suppress the gate leakage current. The direct-tunneling leakage current (J_{DT}) flow through a gate insulator film is determined by the tunneling probability of carrier. The tunneling probability of carrier (D_{DT}) is shown in below equation where physical thickness of insulator (d), electron effective mass in the gate insulator film (m^*) and barrier height of insulator (ϕ_b).

$$J_{DT} \propto D_{DT} \propto \exp\left\{-\frac{4\pi d\left(2m^*\phi_b\right)^{\frac{1}{2}}}{h}\right\}$$

Relationship between physical thickness of SiO_2 (d_{EOT}) and physical thickness of high-k gate insulator (d) obtained by the same gate capacitance value (C) is shown in below equation where dielectric constant of SiO_2 (ε_{ox}) and high-k gate insulator ($\varepsilon_{high\text{-}k}$).

$$C = \frac{\varepsilon_{high-k}}{d} = \frac{\varepsilon_{ox}}{d_{EOT}}$$

$$d = \frac{\varepsilon_{ox}}{\varepsilon_{high-k}} d_{EOT}$$

Therefore, the gate leakage current can be suppressed by using high-k materials, which means that the physical thickness of high-k films can be thicken without changing EOT. In addition, the gate leakage current can also be suppressed by using large band gap materials.

The possible candidate of several metal oxides system for the use of gate dielectric

materials is shown in white spaces of Figure1.7.

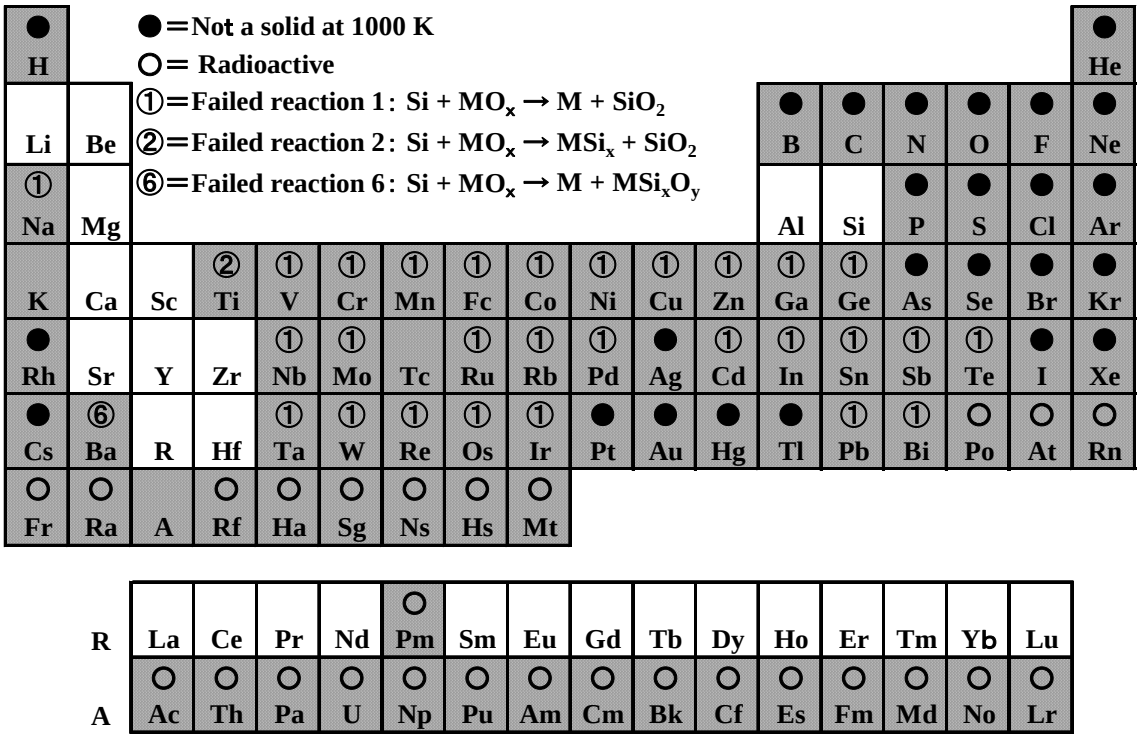


Figure.1.7 Candidate of metal oxides that has possibility to be used as high-k gate insulator

As shown in Figure 1.8, many papers on high-k materials are submitted in the primary conferences up to 2002. However, from 2003 to now, the candidate of high-k materials have narrowed down to Hf-based materials. Therefore, Hf oxides (HfO_2) and Hf-based silicates or nitrides (HfSiON), with dielectric constants of 25 and 10 to 15 respectively, are among the promising materials for the 45-nm-technology node.

Usually, when the EOT becomes small, the effective carrier mobility tends to decrease due to scattering in the high-k layer or at the interface between the high-k layer and the substrate. It has reported that Hf-based films have reduced scattering when a SiO_2-based interfacial layer of 0.5 to 0.7 nm is inserted, however, this attempt increases the EOT.

Consequently, in this work, Lanthanum Oxide (La_2O_3), one of the rare earth oxides, has been tried as a gate insulator, because it has a relatively high dielectric constant of 27, which is slightly higher than that of HfO_2 and a high band offset of 2.3 eV from the conduction band of silicon to La_2O_3 has the advantage of further reducing the leakage current. La2O3 is expected to be the third generation gate dielectrics, which is Hf-based oxides below 45 nm nodes.

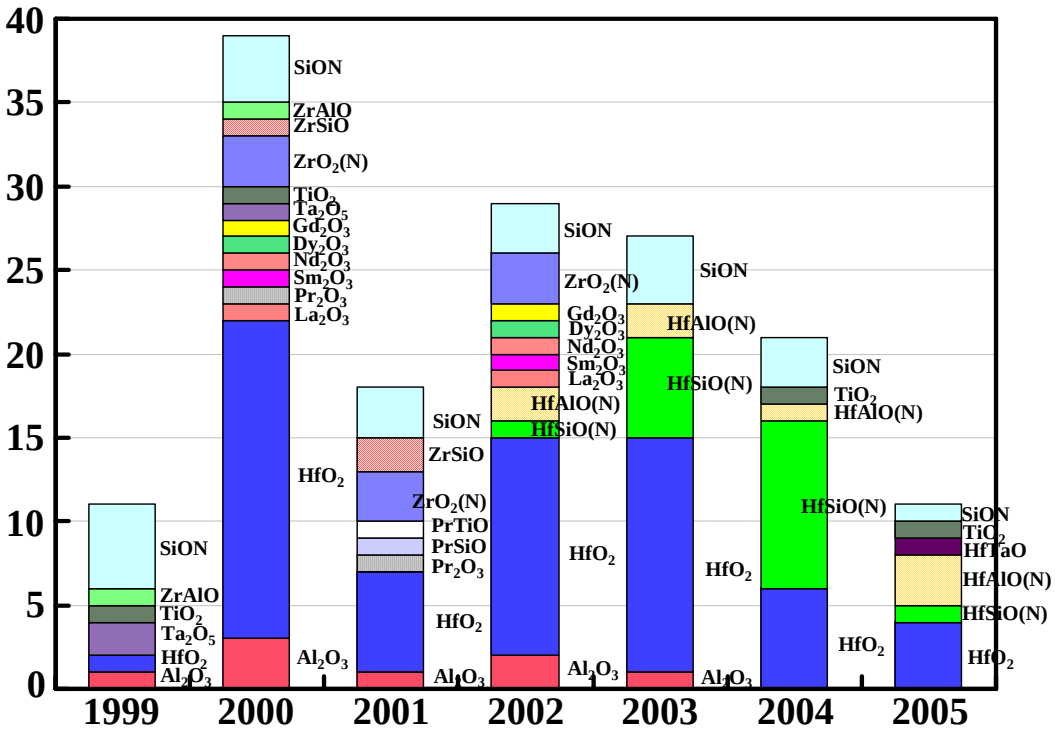


Figure 1.8 Reported High-k materials.

1.4 Properties of La_2O_3

For achieving a low EOT, high-k gate dielectrics materials must have high enough dielectric constant. However, material with very high dielectric constant tends to have narrower band gap that allows higher Schottky conduction currents and tunneling currents. Figure 1.9 shows band gap energy of several metal oxide and silicate materials as a function of dielectric constants. La_2O_3 gives high dielectric constant of 27 and wide band gap of 5.6 eV that is suitable for the use of gate dielectrics.

To inhibit a low leakage current due to Schottky emission conduction mechanism, the high-κ gate dielectric materials must have wide band gap and high barrier of more than 1 eV for both electrons and holes. Figure 1.10 predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy. La_2O_3 has a good symmetrical band barrier of more than 2 eV for both electrons and holes that is compatible for CMOS devices.

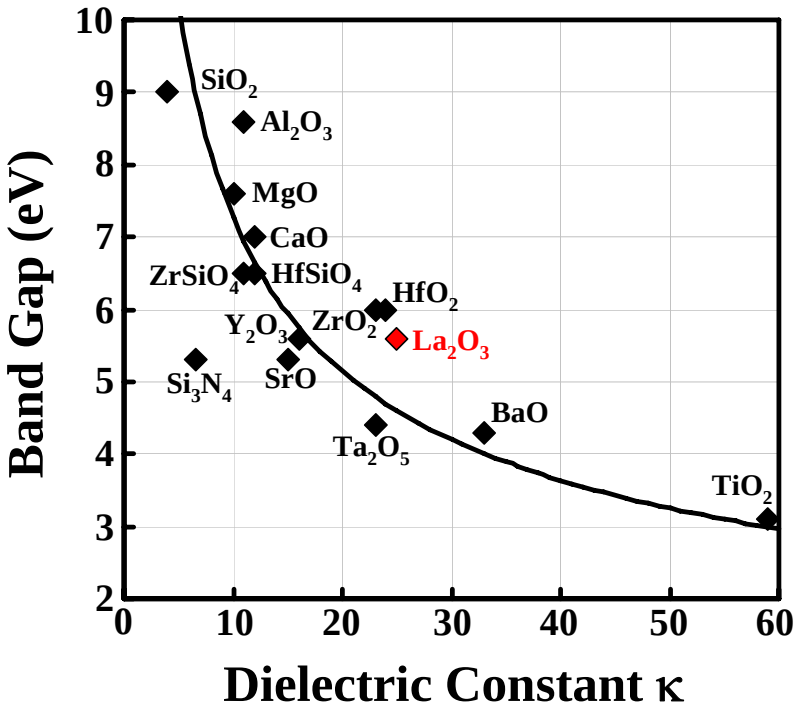


Figure 1.9 Band gap energy of several metal oxide and silicate materials as a function of dielectric constant.

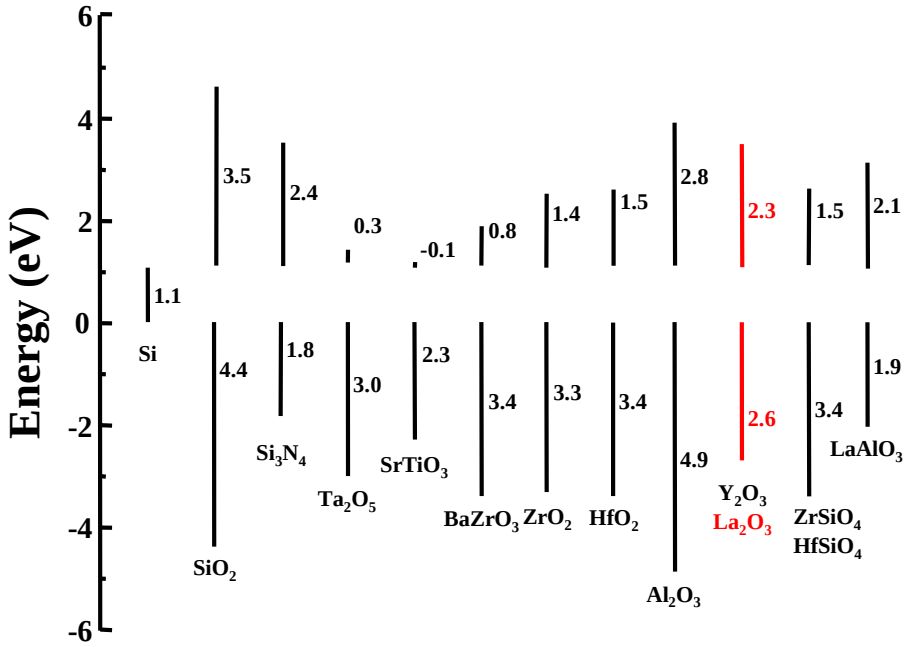


Figure 1.10 Predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy.

Previously, excellent results on several high-k gate dielectrics materials have been reported. Figure 1.11 shows reported leakage current density of various high-k gate materials as a function of EOT. From Figure 1.11, the superiority of La_2O_3 is obvious, low EOT with low leakage current can be achieved with La_2O_3.

Finally, La_2O_3 is considered to be the most promising gate dielectric material for the next generation gate dielectric technology. La_2O_3 material shows good physical properties, high dielectric constant of 27, wide band gap of 5.6 eV, symmetrical band offset for electrons and holes of more than 2 eV, and good thermal stability in contact with silicon. In this study, the electrical properties of MOSFET with La_2O_3 gate dielectrics will be evaluated.

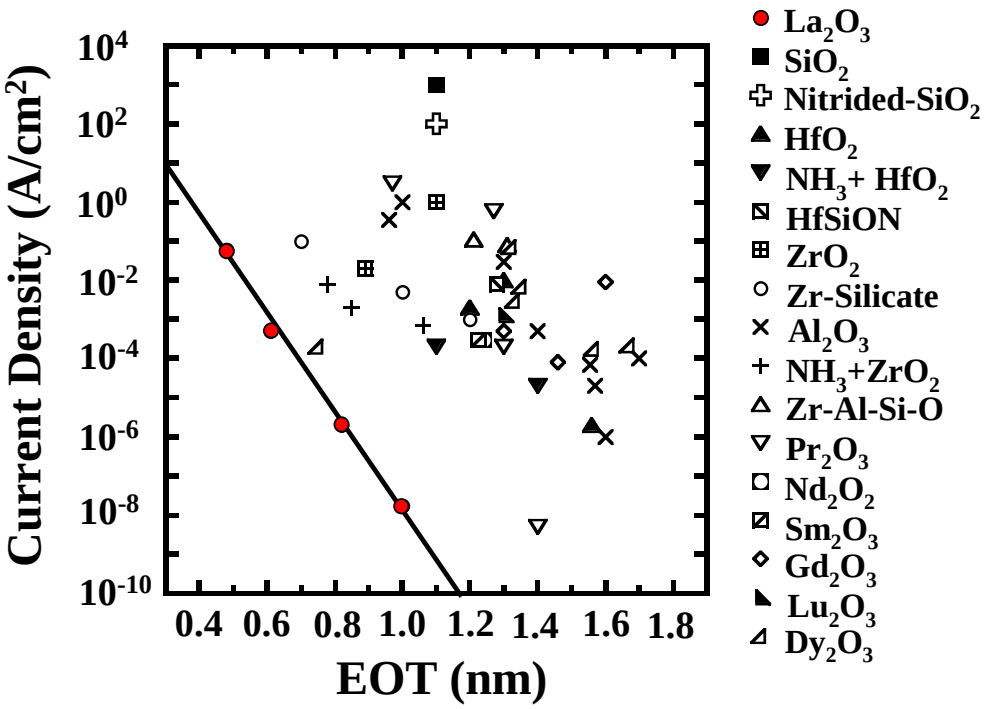


Figure 1.11 Reported leakage current density of various high-k gate materials as a function of EOT.

1.5 The Requirement of Sc_2O_3

La_2O_3 dielectric would be very hopeful, which is said before section. However, La_2O_3 dielectric has several problems. One is the formation of interfacial layer which is mixture of silicon oxides (SiO_x) and Lanthanum-silicate by heat treatment. Figure 1.12 shows the Si 1s spectra of La_2O_3 single-layer dielectric. It suggests that growth of interfacial layer, such as SiO_x and Silicate after annealing. The dielectric constant turned lower than La_2O_3 itself due to form the interfacial layer. And what is worse is that silicon atoms diffuse into La_2O_3 film and bind to La atoms via oxygen.

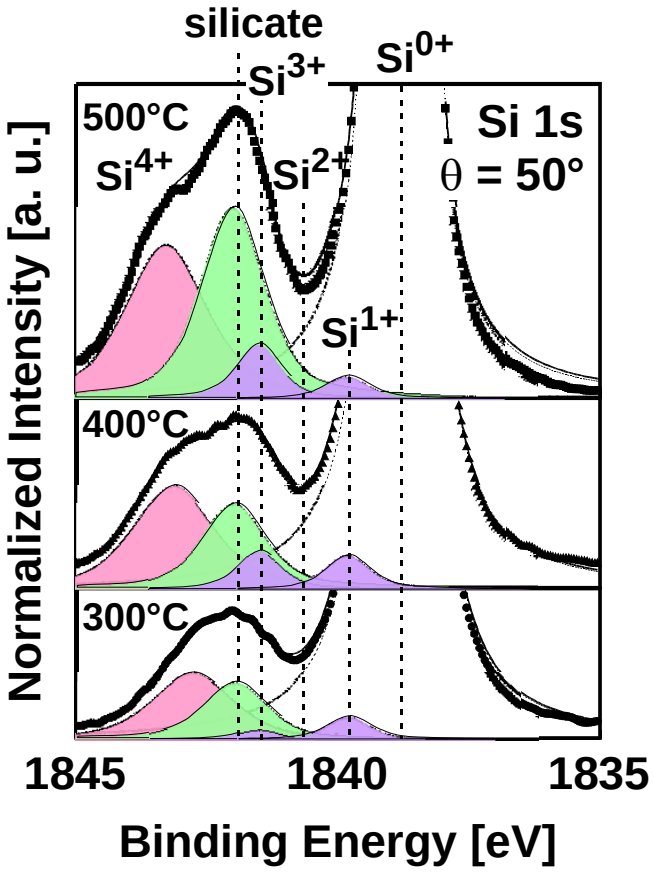


Figure1.12 Si 1s spectra of La_2O_3/Si

In the view point of the cost, the industry use is required 1050 ^oC 2 seconds thermal stability of gate dielectric for etched gate process. (Figure 1.13)[10] La_2O_3 has not such as thermal stability from figure 1.12.

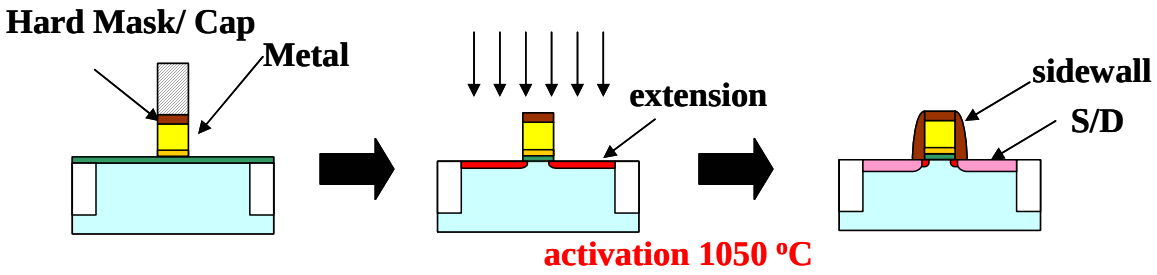


Figure 1.13 Etched gate process

Thermal stability on silicon is momentous affair as considering the alternative gate dielectrics in industry use. One of the best way to understand a thermal stability is to have the understandings of the Gibbs free energy[17]. Suppose, for example, there is a following reaction formula, a difference in Gibbs free energy (ΔG) between before and after rection is important.

$$A + B\ (G_1) \rightarrow C + D\ (G_2) \quad (1.3)$$

$$\Delta G = G_2 - G_1 \quad (1.4)$$

The magnitude and the sign of ΔG decide on whether the reaction is thermodynamically stable or not. In the Ref.[17], several key reactions were indentified by considering the phase diagram of a M-Si-O system, where M is (metal) binary oxides, to narrow down the list of binary oxides that could be stable in contact with silicon at 1000K. Among these reactions, most binary oxides were concluded whether to be stable or not in contact with silicon by following reaction path.

$$Si + MO_x \rightarrow M + SiO_2 \quad (1.5)$$

$$Si + MO_x \rightarrow MSi_z + SiO_2 \quad (1.6)$$

For each reaction, appropriately balanced for the particular binary oxide, MO_x, with coefficients ν $\Delta G^o_{f,1000}$ for the complete reaction was determined by subtracting the sum of the free energies of formation of the reactants from the sum of the free energies of formation of the products.

$$\Delta G^o_{1000} = \sum_{\text{Pr}oducts} \nu G^o_{f,1000} - \sum_{\text{Re}ac\,\text{tan}tss} \nu\, G^o_{f,1000} \quad (1.7)$$

The magnitude of $\Delta G^o_{f,1000}$ indicates the direction of the reaction. $\Delta G^o_{f,1000}$ for the reaction [Eqs. 1.5 and 1.6] for each of the well-known binary oxides are given in table 1.4. A negative value for $\Delta G^o_{f,1000}$ indicates that it is thermodynamically favorable for the reaction to proceed to its products. Thus, when it was determined that $\Delta G^o_{f,1000}$ for one of the above reactions was negative, indicating that silicon and MOx are not thermodynamically stable in contact with each other. Conversely, if a sign of $\Delta G^o_{f,1000}$ is a positive, MO_x is compatible with silicon. In addition, a larger magnitude of $\Delta G^o_{f,1000}$ value, the more unfavorable for the reaction to proceed to its products. In other words, the formation of silicon oxides and metal silicides are expected to be reduced. The table 1.3 shows the gibbs free energy change of binary oxide. Sc_2O_3 have the largest value of gibbs free energy, which is +123 kcal/mol Gibbs free energy at 1000 K, therefore gibbs free energy of Sc_2O_3 is larger than one of La_2O_3. In this reason, Sc_2O_3 is thermally stable property on silicon.

Table 1.3 The Gibbs free energy change at 1000 K

Binary Oxide (MO_x)	ΔG^*_{1000} per MO_x for $Si + Mo_x \rightarrow M + SiO_2$
Sc_2O_3	+123.105
Y_2O_3	+116.823
La_2O_3	+98.470
HfO_2	+47.648
ZrO_2	+42.326

Second problem is La_2O_3 has water absorption property. The water absorption problem is very severe because wet processes are essential for fabrication of MOSFETs. In general, the rare earth oxides become hydroxide in H_2O ambient [12]. Figure 1.14 shows reaction about the generation of La_2O_3 hydroxide. It is said that entire rare earth oxides become gradually hydroxide moisture in the air which induced the increasing the EOT and flatband voltage shift and degradation of carrier mobility. On the other hand, Sc_2O_3 has water resistance property.

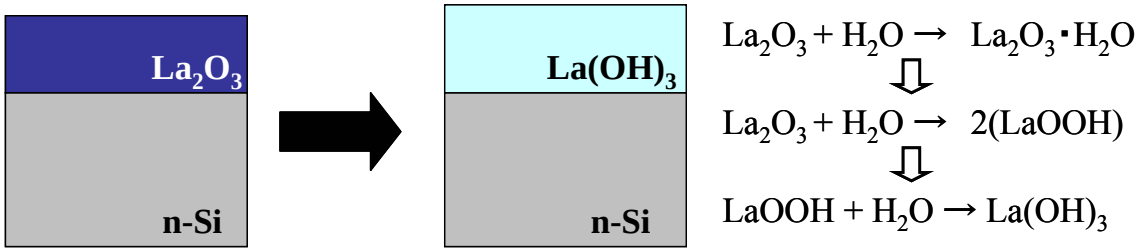


Figure1.14 Schematic of the hydroxide's generation

1.6 Objective of This Study

Although La_2O_3 has excellent properties, there are some of the problems induce the performance decrement of MOSFET. One of the problems in La_2O_3 is that high temperature annealing increases the leakage current density and forms SiO_x like I.L.. Therefore suppression of the reaction of La_2O_3/interface is crucial. Sc_2O_3 which has dielectric constant of 14, is known to have stable material on Si at 1000 K, has +123 kcal/mol Gibbs free energy at 1000 K, and has stronger affinity to oxygen than La. [6.] In this work, in order to suppress the leakage current and interfacial layer, one can expect the use of Sc_2O_3 layer as a buffer layer for La_2O_3 film.

Chapter 2

Fabrication and Characterization Methods

2.1 Experimental Procedure

2.1.1 Fabrication Procedure for MOS Capacitor

The fabrication procedure for MOS Capacitor is shown in Figure 2.1. La_2O_3 thin films and Sc_2O_3 thin film were deposited on n-type silicon (100) substrate by Electron-Beam Evaporation. at substrate temperature 300 ^oC followed by H_2SO_4/H_2O_2 mixture (SPM) cleaning and HF-dip processes. Then, upper electrode and back side electrode were formed by Vacuum Evaporation Method or RF Magnetron Sputtering Method. In this experiment, we performed two type of the annealing method using Rapid Thermal Annealing (RTA) method. One is the Post Deposition Annealing (PDA) and the other is the Post Metallization Annealing (PMA). After metal formation, t hermally evaporated Al was coated on backside of the wafer to characterize the electrical properties.

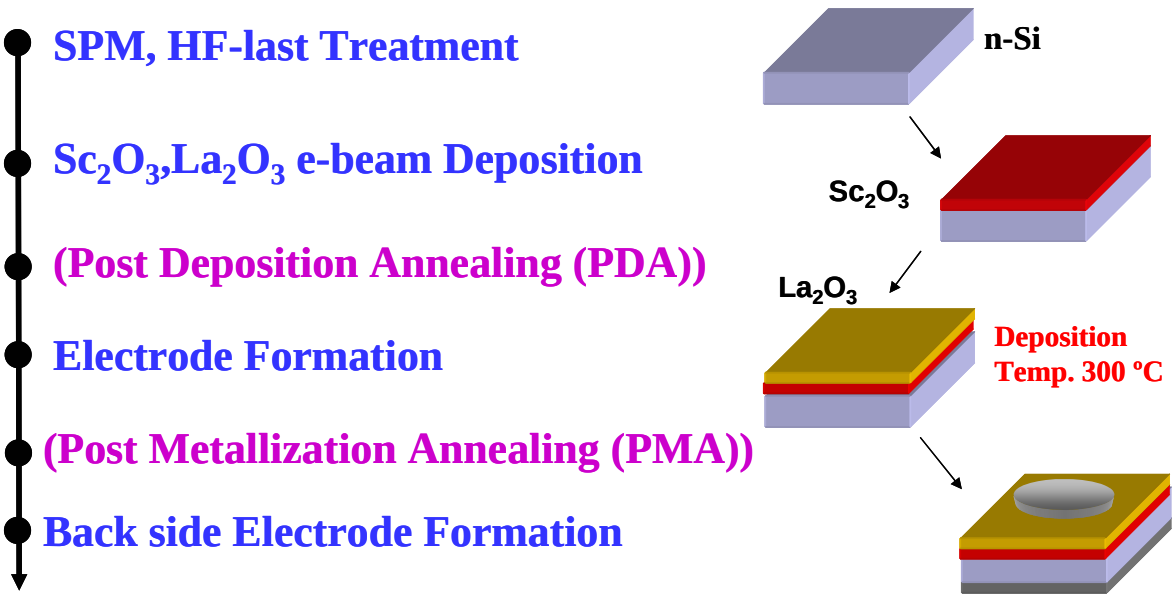


Figure 2.1. The fabrication procedure for MOSCAP.

2.1.2 Fabrication Procedure for n-MOSFET

The fabrication procedure for nMOSFET is shown in Figure 2.2 and the cross-sectional description in La_2O_3 nMOSFET fabrication is shown in Figure 2.3. nMOSFET fabrication was started from S/D implanted Si(100) substrate. La_2O_3 thin film was deposited by Electron-Beam Evaporation followed by substrate cleaning. After metal gate formation, the gate area was defined with photolithography followed by metal gate etching. The Al-Pad area was formed with lift-off process under acetone solution and Al back side electrode were formed afterwards.

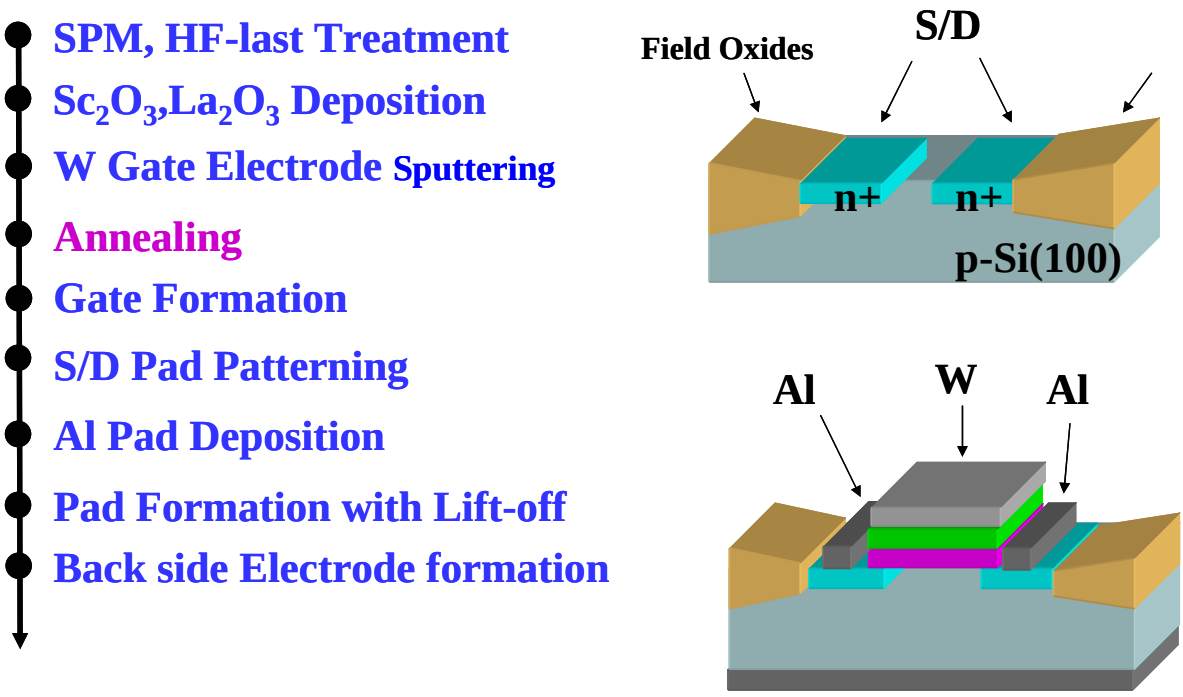


Figure 2.2. The fabrication procedure for n-MOSFET

2.2 Fabrication Methods

2.2.1 Wet Cleaning Method of Silicon Substrate

Prior to deposit of high-k gate thin films for LSI fabrication process, the ultra-pure surface of a bare Si-substrate should be chemically cleaned to remove particles contamination, such as metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. It is considered that this substrate cleaning process is very important to realize desirable device operation and its reproducibility.

In full fabrication processes as well as substrate cleaning, DI (de-ionized) water is one of the most important because DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. Theoretical resistively of pure water at 25ºC is 18.3 MΩ·cm. The resistively value of ultra-pure water (UPW) used in this study achieve more than 18.2 MΩ·cm and have fewer than 1.2 colony of bacteria per milliliter and no particle larger than 0.25 um.

In this study, the method of substrate cleaning process was used a typical processing using hydrofluoric acid, which is usually called RCA cleaning method, was proposed by W. Kern et al. But some steps were reduced. The steps were shown in Fig.2.4. Firstly, a cleaning steps in solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2 = 1:4, called by SPM) performed to remove any organic material and metallic impurities after UPW cleaning. Secondly, the step in a solution of dilated hydrofluoric acid (HF:H_2O=1:100) was performed to remove chemically and native oxides which might have been formed on Si surface. Final step was dipped in UPW because hydrogen-terminated surface.

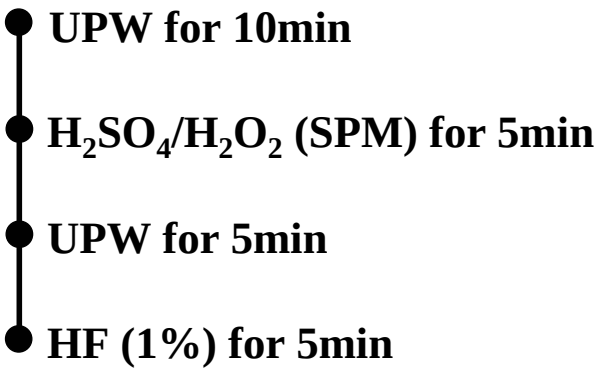


Figure 2.3. Si Surface cleaning process.

2.2.2 Electron-Beam Evaporation Method

Electron-Beam Evaporation method using MBD equipment is employed for depositing La_2O_3 in this study. Figure 2.4 shows the schematic drawings of the equipment and inside of its growth chamber. Air in the loading chamber is removed to degree of a vacuum of 10^{-8} Torr by a turbo molecular pump connected to a rotary pump. Vacuum in the growth chamber reaches as high as 10^{-10} Torr by the removal of air with an ion pump and the introduction of liquid N_2 trap.

In the growth chamber, sintered La_2O_3 target, which is evaporation source, is irradiated with electron beam accelerated by -5 kV. The target is heated up and La_2O_3 molecules are evaporated. Then ultra thin La_2O_3 film is deposited on the Si-substrate. The degree of a vacuum is from 10^{-7} to 10^{-8} Torr while deposition. The substrate rotates 10 times per 1 minute horizontally to uniform the film thickness. Physical thickness of the film is monitored with a film thickness counter using crystal oscillator. The temperature of the substrate is controlled by a substrate heater and is measured by a thermocouple.

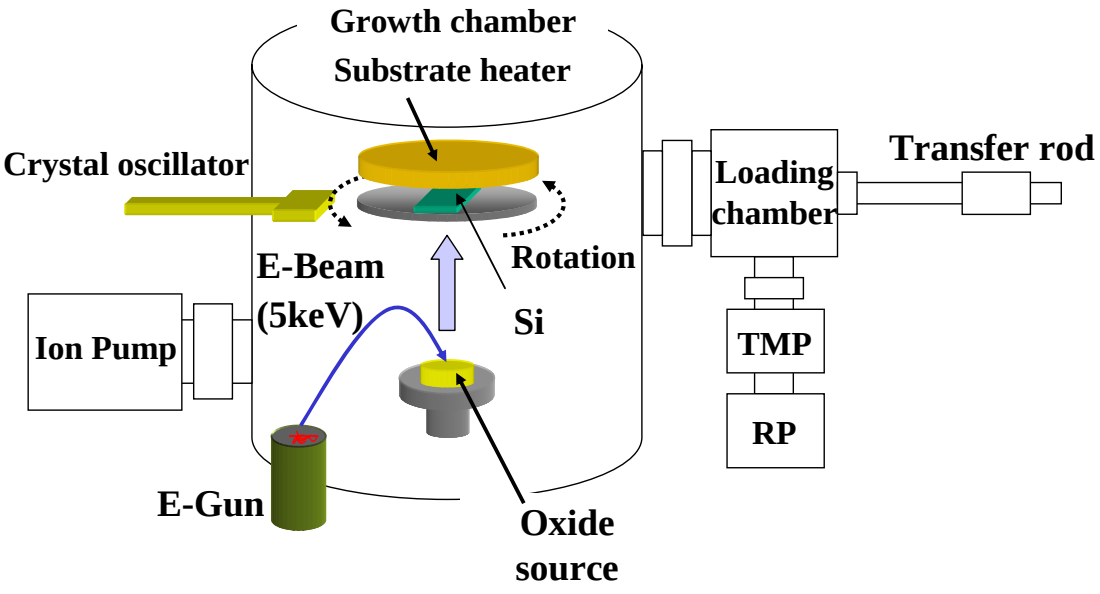


Figure 2.4. Schematic drawing of e-beam evaporation system.

2.2.3 Rapid Thermal Annealing (RTA) Method

Thermal annealing processes are often used in modern semiconductor fabrication for defects recovery or molecular introduction to dielectric thin films, for lattice recovery or impurity electrical activation of doped or ion implanted wafers. In this experiment, Rapid Thermal Processing MILA-3000 from ULVAC is used for annealing deposited La_2O_3 thin films. Figure 2.5 illustrated the schematic drawing for MILA-3000. High purity gas ambience can be obtained by pumping out and purging with the in use ambient gas. This RTP system is heated-up by infrared lamp heating furnace and cooled-down by flowing water radiator. The furnace temperature is of the range from room temperature to around 1200^{o}C with ramp-up of less than 50^{o}C/sec and much slower on cooling-down. The available of ambient gases are N_2 and O_2 at atmospheric pressure by keeping the flowing gas at the rate of 1 lt./min.

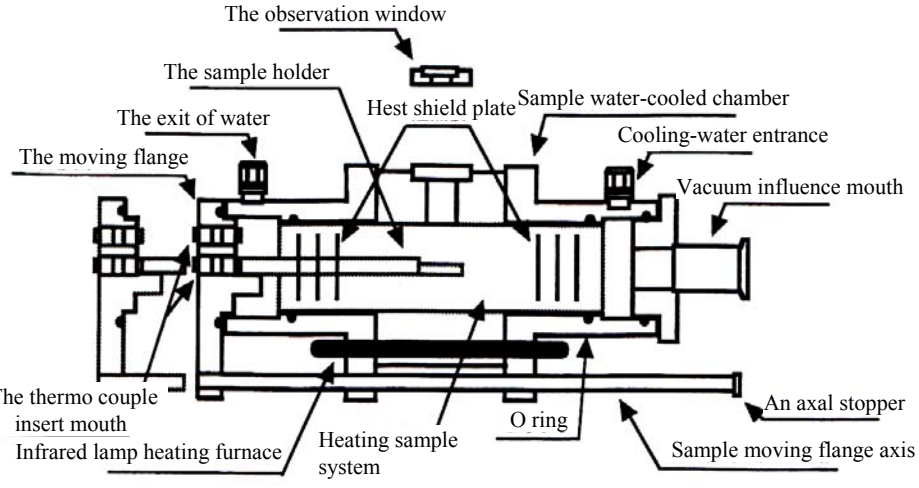


Figure 2.5. Schematic drawing for Rapid Thermal Annealing (RTA) MILA-3000

2.2.4 Vacuum Evaporation Method

All of Al metals in this work were obtained from deposition with bell jar vacuum thermal evaporation. Figure 2.6 illustrates a schematic drawing for vacuum thermal evaporation system. The system is utilized with Turbo Molecular Pump (TMP) to pump down to several 10^{-5} Torr. In case of MOS capacitor fabrication, metal shadow mask with circle opening of 200 μm diameters was used. Filament is made of tungsten, was used for heating the Al source up to its vapor temperature. Both filaments and Al sources are made of Nilaco, inc. with material purity of 99.999%.

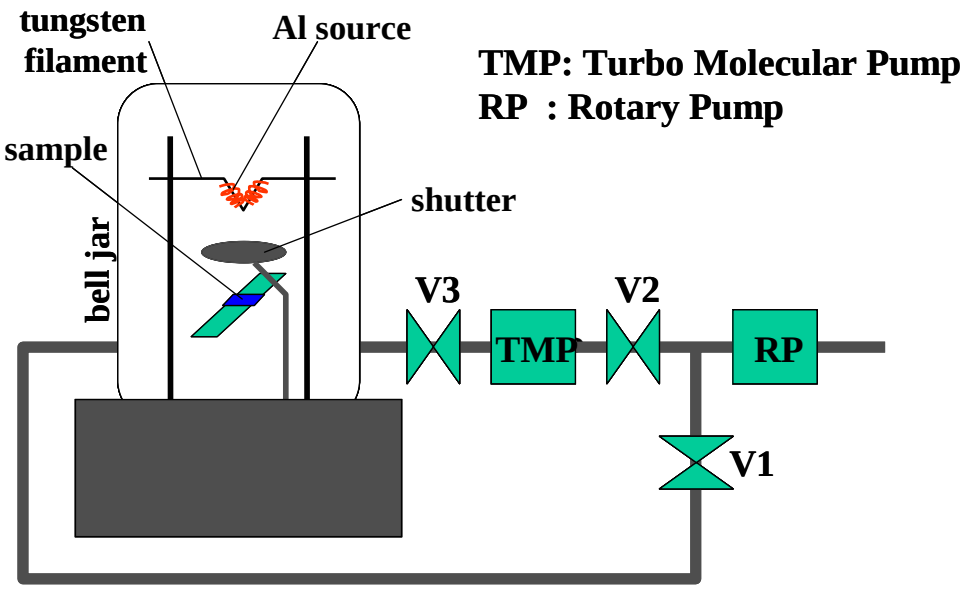


Figure 2.6. Schematic drawing for vacuum thermal evaporation system.

2.2.5 RF Magnetron Sputtering Method

Some of a gate electrode material was deposited by RF magnetron sputtering method. Figure 2.7 illustrates a schematic drawing for RF magnetron sputtering system. This equipment deposits metal film by means of physical sputtering that occurs in a magnetically-confined RF plasma discharge of an inert Ar gas. Before the introduction of gases (Ar, Kr, N_2 or O_2), the process chamber was evacuated to degree of 10^{-5} Pa by a turbo molecular pump connected to a rotary pump and a liquid N_2 trap. The flow rate of gases is (7sccm) controlled by mass flow. The RF power supply system has auto impedance matching equipment and its capability of power supply is ~ 500W.

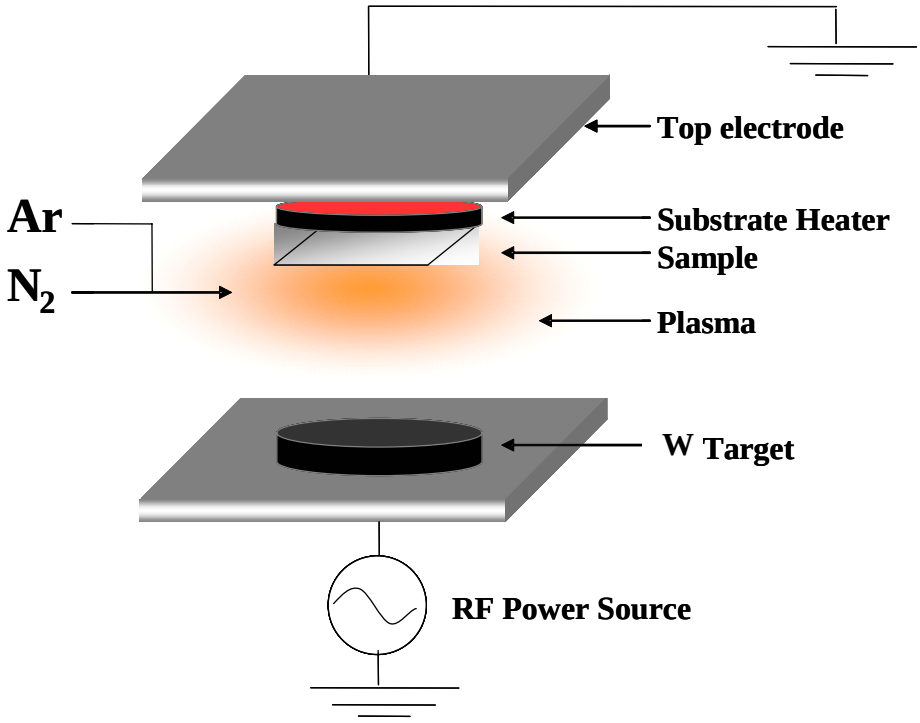


Figure 2.7. Schematic drawing for RF magnetron sputtering system.

2.2.6 Mask Aligner

The spin-coated photoresist was exposed through the mask with high-intensity ultraviolet light (405 nm). In this study, the exposure process was performed by contact-type mask aligner, MJB3 (Karl Suss Co. Ltd.). The exposure time was set to 12 sec. The photo-resist was developed using the specified developer (NMD-3, Tokyo Ohka Co. Ltd.).

2.2.7 Reactive Ion Etching (RIE)

RIE system was employed for etching TaN gate electrode. RIE combined the plasma and sputter etching process. Plasma systems are used to ionize reactive gases, and the ions are accelerated to bombard the surface. Etching process occurs though a combination of chemical reaction and momentum transfer from the etching species.

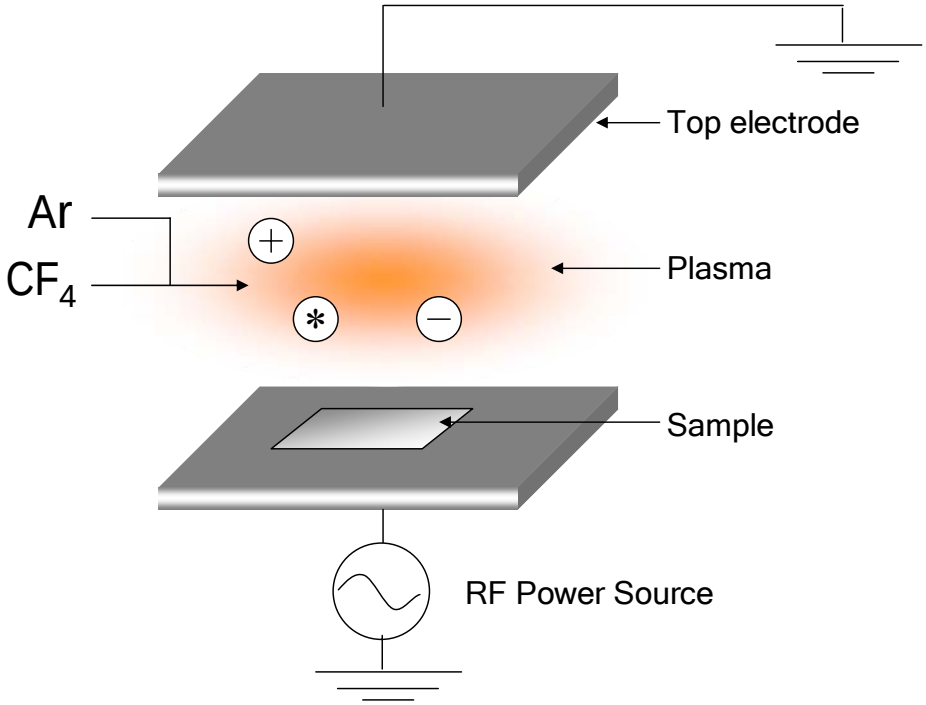


Figure 2.8 RF magnetron sputtering system

2.3 Measurement Methods

2.3.1 Spectroscopic Ellipsometry

The phisical thickness was optically extracted by FE-5000 ellipsometer using a Caucy model and a single layer approximation. Ellipsometry is the method to estimate the optical property of material or surface film thickness the change of polarization condition caused by the reflection of light. Generally, when light is illuminated to a material, the polarization condition of incident light and reflected light are different. This method evaluates the surface condition from this difference. P component of polarized light is horizontal to the plane formed by incident and reflected light and vertical component is S. Ordinary non-polarized light becomes linear polarized light in which the phase and intensity are the same between P and S polarization component when it was passed through 45^o declined polarizer. When the linear polarized light is illuminated to the material, phase different Δ arises between P and S component of polarized light because the reflectance of P and S component is different at the material surface.

P and S component in electric field vector of the reflected light are given by

$$\begin{aligned} E_P &= a_P \cos(\omega t - \delta_P) \\ E_S &= a_S \cos(\omega t - \delta_S) \end{aligned} \qquad (1)$$

Here, a_P, a_S are amplitudes of P and S direction respectively. δ_P and δ_S express the phase deviations in the each component. Introducing the relation $\delta_P + \delta_S = \Delta$, the following equation is obtained.

$$\frac{E_P^2}{a_P^2} + \frac{E_S^2}{a_S^2} - 2\frac{E_P E_S}{a_P a_S}\cos\Delta = \sin^2\Delta \qquad (2)$$

This equation expresses ellipsometry in general. The condition of elliptically polarized light is determined by the relative phase difference Δ and reflection amplitude ratio.

Taking the tangent, reflection amplitude ration is expressed as reflection amplitude angle ψ ellipsometer measures and determines Δ and ψ or $\cos\Delta$ and $\tan\psi$.

Following system is assumed for the typical measurement. The system consists of ambient, thin film, and substrate.

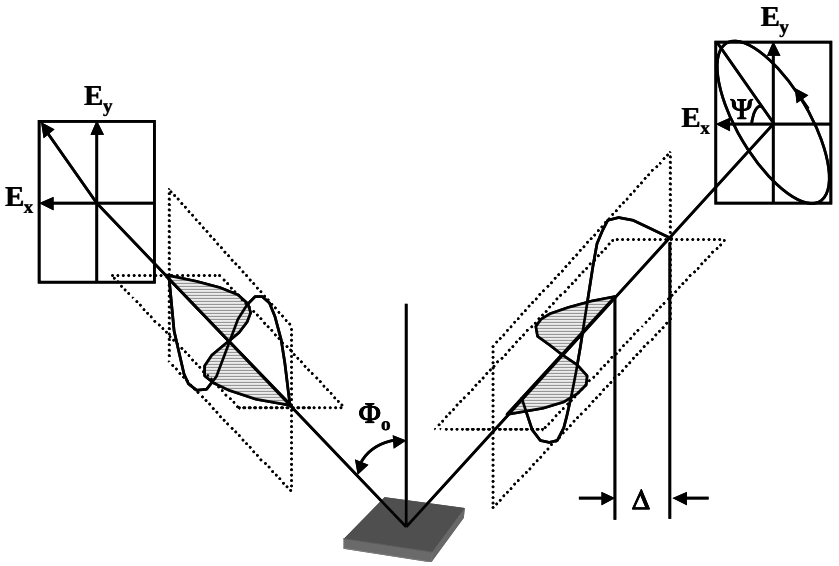


Figure 2.9. Conception for measuring optical thickness of thin film with spectroscopic ellipsometry

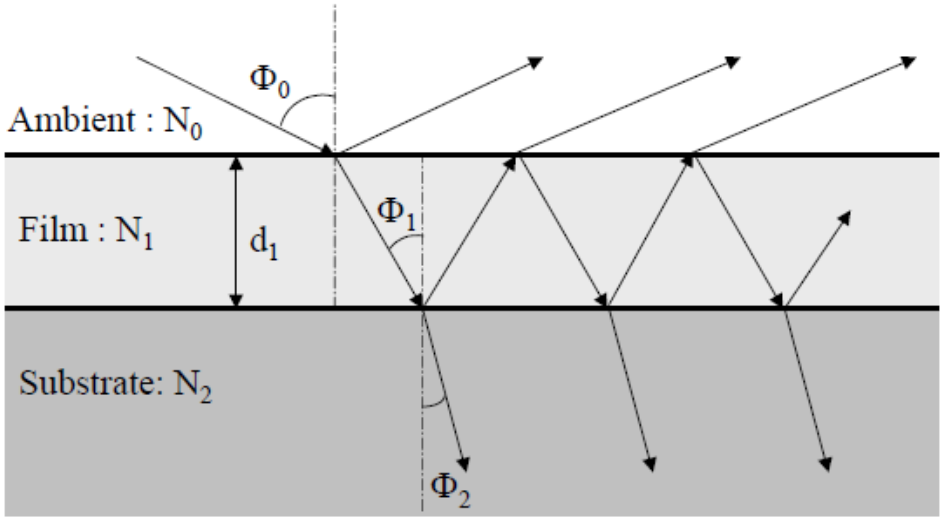


Figure 2.10. Model of Typical Thin Film Measurement

The relation between reflectance ratio in P, S component of polarized light and ellipsometry parameter is expressed as

$$\tan\psi e^{j\Delta} = \frac{R_P}{R_S} \qquad (2.3)$$

Here, R_P and R_S are complex reflection constant(Fresnel constant). Giving complex refraction $N_i = n_i - jk_i$, Fresnel constant at each interface is given by

$$\begin{aligned} r_{i,j+1} &= \frac{N_i \cos\Phi_{i-1} - N_{i-1}\cos\Phi_i}{N_i \cos\Phi_{i-1} + N_{i-1}\cos\Phi_i} \\ r_{i,j+1} &= \frac{N_{i+1} \cos\Phi_{i-1} - N_i \cos\Phi_i}{N_{i-1} \cos\Phi_{i-1} + N_i \cos\Phi_i} \end{aligned} \qquad (4)$$

The phase angle β_i in the i layer film is

$$\beta_i = 2\pi\left(\frac{d_i}{\lambda}\right)N_i \cos\Phi_i \qquad (5)$$

Here d_i is film thickness, λ is wavelength of incident light and φ_i is incident angle in the i layer. Using these parameter,

$$\begin{aligned} R_P &= \frac{r_{o1P} + r_{12P}e^{-j2\beta_1}}{1 + r_{o1P}r_{12P}e^{-j2\beta_1}} \\ R_S &= \frac{r_{o1S} + r_{12S}e^{-j2\beta_1}}{1 + r_{o1S}r_{12S}e^{-j2\beta_{1i}}} \end{aligned} \qquad (6)$$

Therefore, if complex reflection in each layer, incident angle and wavelength of light at measurement are known, film thickness can be calculated by measuring ellipsometry parameters.

2.3.2 Atomic Force Microscopy (AFM)

AFM enables to measure surface morphology by utilizing force between atoms and approached tip. The roughness of sample surface is observed precisely by measurement of x-y plane and z. Fig. 2.11 shows the principle of AFM. Tip is vibrated during measurement, and displacement of z direction is detected. This method is called tapping mode AFM (TM-AFM). Resolution limit for normal AFM is 5~10nm depending on distance between surface and tip. On the other hand, resolution limit for TM-AFM is depended on size of tip edge. Thus, resolution limit for TM-AFM is about 1nm.

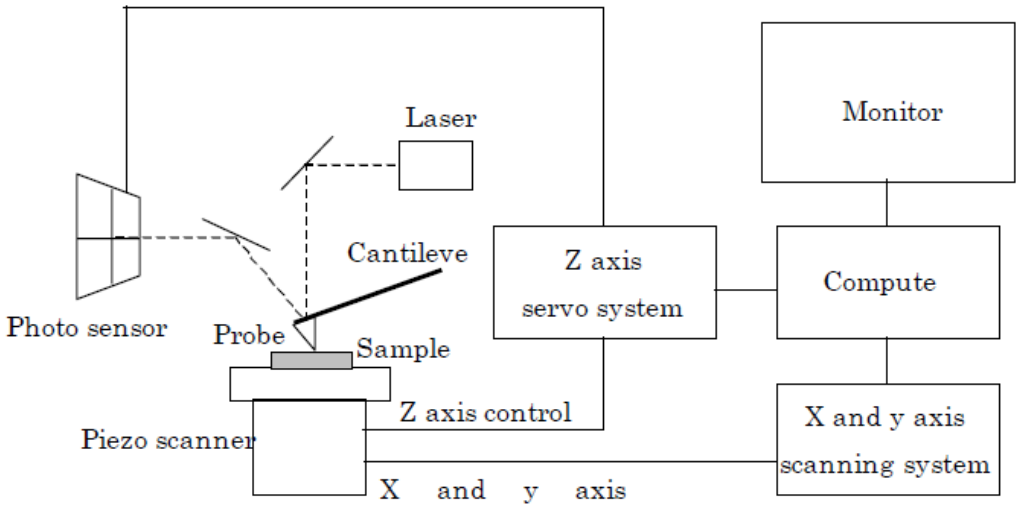


Figure 2.11. Schematic of AFM Principle

2.3.3 X-ray Photoelectron Spectroscopy (XPS)

XPS, which known as Electron spectroscopy for chemical analysis(ESCA) is one of the conventional methods that estimates thin film and Si interface.

Fig.2.12 shows photograph and scheme of XPS equipment used in this work. During analysis, the pressures of main chamber were about 10^{-9}(torr) vacuum with turbo pomp. Surface analysis by XPS is accomplished by irradiating a sample with soft X-ray and analyzing the energy of the detected electron. Non-monochromatic MgKα (1253.6 eV) X-ray is used in this study. The method is illustrated with the energy band diagram in Fig.2.13 This photoelectron has limited penetrating power in a solid on the order of 1-10μm. They interact with atoms in the surface region, causing electrons to be emitted by the photoelectric effect. The emitted electrons have measured kinetic energies given by

$$KE = h\nu - BE - \Phi_S$$

where $h\nu$ is the energy of the photoelectron, BE is the binding energy of the atomic orbital from which the electron originates and Φ_S is the spectrometer work function (4.8eV).

The binding energy may be regatded as the energy difference between the initial and final states of the ion from each atom, there is a corresponding variety of kinetic energies of the emitted electron. Because each element has a unique set of binding energies, XPS can be used to identify and determine the concentration of the elements in the surface. Variation in the elemental binding energies(chemical shift) arises from difference in the chemical potential and polarization of compounds. These chemical shifts can be used to identify the chemical states of the materials being analyzed.

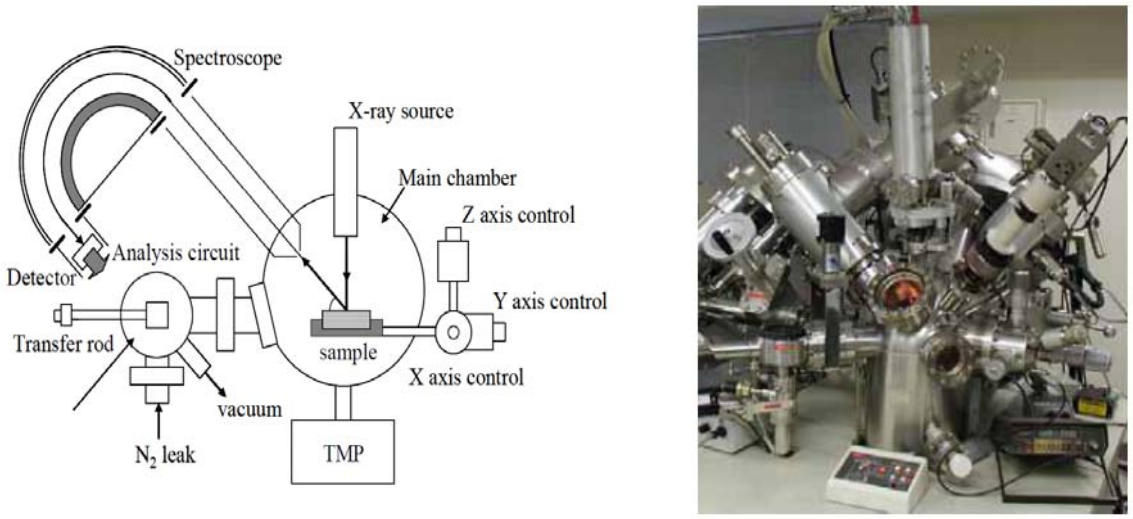


Figure 2.12. Photograph and Schematic of XPS Equipment

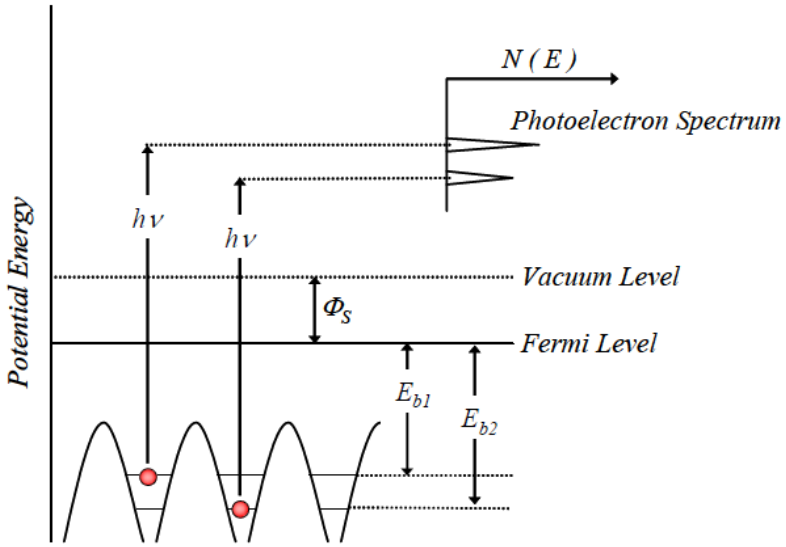


Figure 2.13. Illustration of measurement method with the energy

2.3.4 Transmission Electron Microscopy (TEM)

Cross section of the sample is observed by Transmission Electron Microscope (TEM). TEM is microscopic equipment for observing internal structure of a thin sample by radiating electron beam to it. Figure 2.14 shows schematic cross section of a TEM. The principle of TEM is similar to that of optical microscope. In case of TEM, observation is made in a high vacuum, and an electron gun and electromagnetic lenses are used in place of a light source and optical lenses, respectively. Because wavelength of electron beam is less than that of visible ray, resolution of TEM is higher than that of optical microscope. The thickness of sample must be not greater than 0.1 μm so as to transmit electron beam. In some case, Focused Ion Beam (FIB) equipment is used for the lamination of the sample.

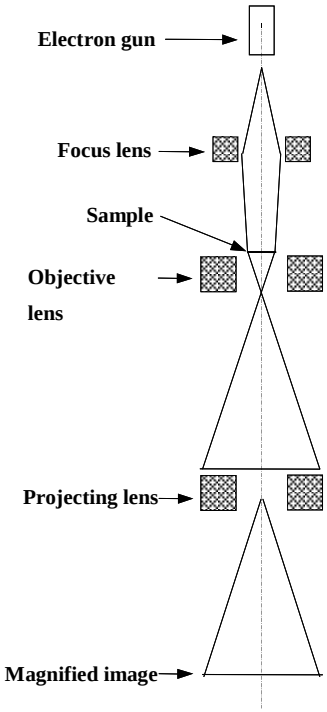


Figure 2.14. Schematic cross section of TEM

2.4 Characterization Method

2.4.1 Characterization of MOS Capacitor

2.4.1.1 C-V (Capacitance-Voltage) Measurement

Figure 2.14 shows the ideal of C-V characteristic of p-type MOS diode. Here, "ideal" MOS diode means that there is no interface-trapped charge (Q_{it}), fixed charge (Q_f), oxide trap charge (Q_{ot}) and mobile ion charge (Q_m). The total capacitance (C) of MOS diode equals the oxide capacitance (C_0) which is accumulated and the silicon capacitance (C_{Si}) connected in series as follows,

$$C = \frac{C_0 C_{Si}}{C_0 + C_{Si}} \text{ F/cm}^2.$$

And we obtain

$$\frac{C}{C_0} = \frac{1}{\sqrt{1 + \frac{2\varepsilon_{ox}{}^2 V}{qNA\varepsilon_{si}d^2}}},$$

where we have written out C_{Si} explicitly. This equation indicates that the capacitance decreases with increase of the gate voltage.

If applied voltage is negative, depletion layer is not generated but hole is accumulated in surface of silicon. As a result, the total capacitance equals approximately the oxide capacitance (ε_{ox}/d). Beyond strong inversion, even if the voltage increases more than that, the thickness of depletion layer doesn't increase any longer. The gate voltage is called threshold voltage (V_T) in this condition as follows.

$$V_T = \frac{\sqrt{2\varepsilon_{Si} q N_A (2\psi_B)}}{C_0} + 2\psi_B$$

Moreover, capacitance is as follows

$$C_{\min} = \frac{\varepsilon_{ox}}{d + (\varepsilon_{ox} / \varepsilon_{Si}) W_m}.$$

In conventional MOS diode, however, the difference of work function between metal and oxide (ϕ_{ms}) is not zero and there are varies space charges, such as Q_{it}, Q_f, Q_{ot} and Q_m, in oxide and interface of oxide-semiconductor, therefore those affect characteristics of ideal MOS diode. As a result, flat band voltage (V_{FB}) is shifted from ideal that as follows,

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_0}.$$

And C-V carve is parallel shifted as shown in Figure 2.14 (b) because ϕ_s, Q_m, Q_{ot} is not zero. And in addition to that, when there are much Q_{it}, that is changed by surface potential. Therefore, curve (c) as shown in Figure 2.14 is shifted and bended by Q_{it} value.

CET (Capacitance-equivalent-thickness) in other words, T_{ox} electrical equivalent means the thickness of equivalent SiO_2, can be calculated from accumulated capacitance of C-V characteristic as follows,

$$CET = \varepsilon_0 \varepsilon_{Si} \frac{S}{C_0}$$

where ε_0, ε_{Si} and S are permittivity of vacuum, dielectric constant of SiO_2 and area of a capacitor.

In this study, HP4284A (Hewlett-Packard Co. Ltd.) is used for measurement C-V characteristics. The range of measurement frequency is from 10k to 1MHz.

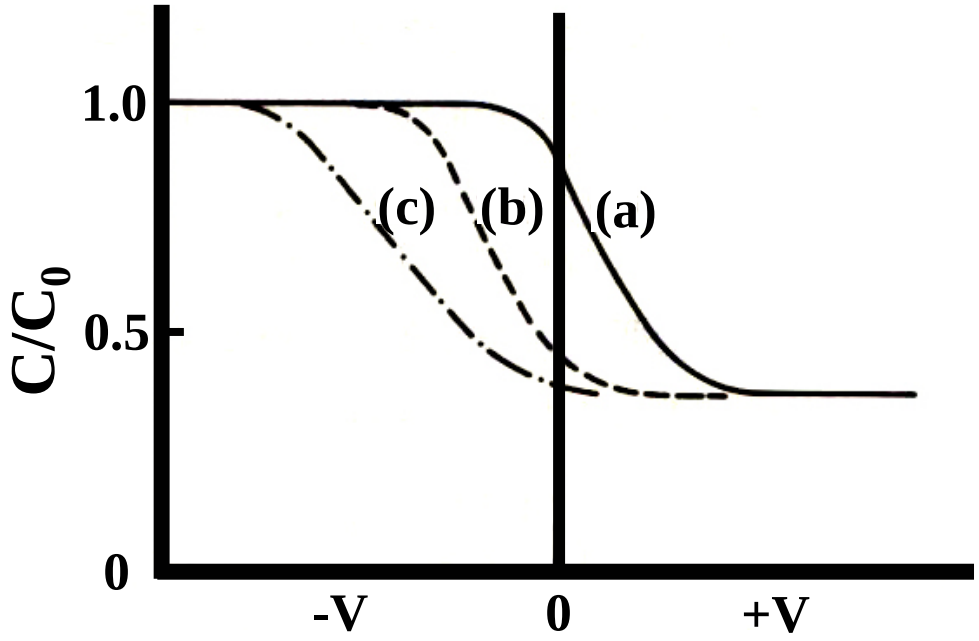


Figure 2.15 : The ideal of C-V characteristics of p-type MOS diode.

2.4.1.2 J-V (Leakage Current Density-Voltage) Measurement

It is important to suppress the leakage current of the gate dielectric film as small as possible in order to lower the power consumption of LSI. To estimate the leakage current density, J-V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.).

2.4.1.3 Interface State Density Measurement

Interface state density is very important to know the state of dielectric/Si. The interface state density was calculated by conductance method.

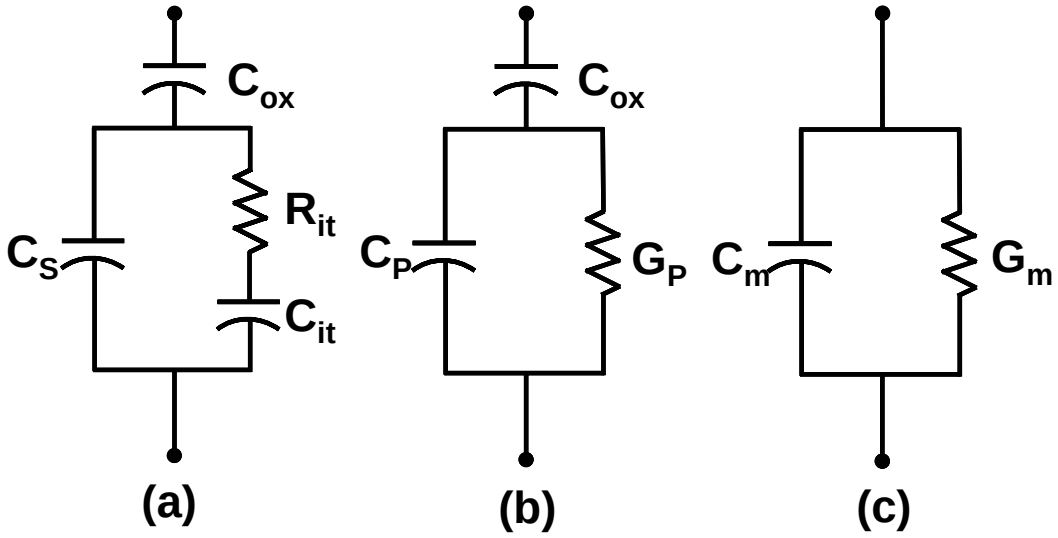


Figure 2.16. Equivalent circuits for conductance measurements

(a) MOS capacitor (b) simplified circuit of MOS capacitor (c) measured circuit

The conductance method, proposed by Nicoliian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it} [Dieter]. Interface trap densities of 10^9 cm^{-2}-eV^{-1} and lower can be measured. It is also the most complete method, because it yields D_{it} in the depletion and weak inversion portion of the band gap, the capture cross-sections for majority carriers, and information about surface potential fluctuation. The technique is based on measuring the equivalent parallel conductance G_p of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of

the interface trap density.

The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in figure 2.16(a). It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_s, and the interface trap capacitance C_{it}. The capture-emission of carriers by D_{it} is a lossy process, represented by the resistance R_{it}. It is convenient to replace the circuit of figure 2.15(a) by that in figure 2.15(b), where C_p and G_p are given by

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \qquad (2.41)$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \qquad (6.42)$$

Where $C_{it} = q^2 D_{it}$, $\omega = 2\pi f$ (f = measurement frequency) and $\tau_{it} = R_{it}C_{it}$, the interface trap time constant, given by $\tau_{it} = [\upsilon_{th}\sigma_p N_A \exp(-q\phi_s/kT)]^{-1}$. Dividing G_p by w makes Eq. (2.42) symmetrical in $\omega\tau_{it}$. Equations (2.41) and (2.42) are for interface traps with a single energy level in the band gap. Interface traps at the SiO_2-Si interface, however, are continuously distributed in energy throughout the Si band gap. Capture and emission occurs primarily by traps located within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1+(\omega\tau_{it})^2\right] \qquad (2.43)$$

Equations (2.42) and (2.43) show that the conductance is easier to interpret than the capacitance, because Eq.(2.42) does not require C_s. The conductance is measured as a function of frequency and plotted as G_p/ω versus w. G_p/ω has a maximum at $\omega = 1/\tau_{it}$ and at that maximum $D_{it} = 2G_p/q\omega$. For Eq.(2.43) one can find $\omega \sim 2/\tau_{it}$ and D_{it} =

$2.5G_p/q\omega$ at the maximum. Hence one can determine D_{it} from the maximum G_p/ω and determine τ_{it} from ω at the peak conductance location on the ω-axis. G_p/ω versus f plots, calculated according to Eqs. (2.42) and (2.43).

Experimental G_p/ω versus ω curves are generally broader than predicted by Eq. (2.43), attributed to interface trap time constant dispersion caused by surface potential fluctuations due to non-uniformities in oxide charge and interface traps as well as doping density. Surface potential fluctuations are more pronounced in *p*-Si than in *n*-Si. Surface potential fluctuations complicate the analysis of the experimental data. When such fluctuations are taken into account, Eq. (2.43) becomes

$$\frac{G_p}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_{it}} \ln\left[1+(\omega\tau_{it})^2\right] P(U_s)\,dU_s \qquad (2.44)$$

where P(Us) is a probability distribution of the surface potential fluctuation given by

$$P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{\left(U_s-\overline{U}_s\right)^2}{2\sigma^2}\right) \qquad (2.45)$$

With $\overline{U}_s$ and σ the normalized mean surface potential and standard deviation, respectively.

An approximate expression giving the interface trap density in terms if the measured maximum conductance is

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{\max}. \qquad (2.46)$$

Capacitance meters generally assumed the device to consist of the parallel C_m-G_m combination in figure 2.15 (c). A circuit comparison of figure 2.15(b) to 2.15 (c) gives

G_p/ω in terms of the measured capacitance C_m, the oxide capacitance, and the measured conductance G_m as

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 \left(C_{ox} - C_m\right)^2} \qquad (2.47)$$

assuming negligible series resistance. The conductance measurement must be carried out over wide frequency range. The portion of the band gap probed by conductance measurements is typically from flatband to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50mV or less to prevent harmonics of the signal frequency giving rise to spurious conductances. The conductance depends only on the device area for a given D_{it}. However, a capacitor with thin oxide has a high capacitance relative to the conductance, especially for low D_{it} and the resolution of the capacitance meter is dominated by the out-of-phase capacitive current component. Reducing C_{ox} by increasing the oxide thickness helps this measurement problem.

2.4.2 Characterization of nMOSFET

2.4.2.1 Threshold Voltage (Vth) Measurement

One of the common threshold voltage **(V_{th})** measurements is the linear extrapolation method with the drain voltage of typically 50-100 (mV) to ensure operation in the linear MOSFET region.

The threshold voltage is determined from the extrapolated or intercepts gate voltage V_{GSi} by

$$V_T = V_{GSi} - \frac{V_{DS}}{2},$$

where

$$V_{GSi} = V_{GS,\max} - \frac{I_{D,\max}}{g_{m,\max}}.$$

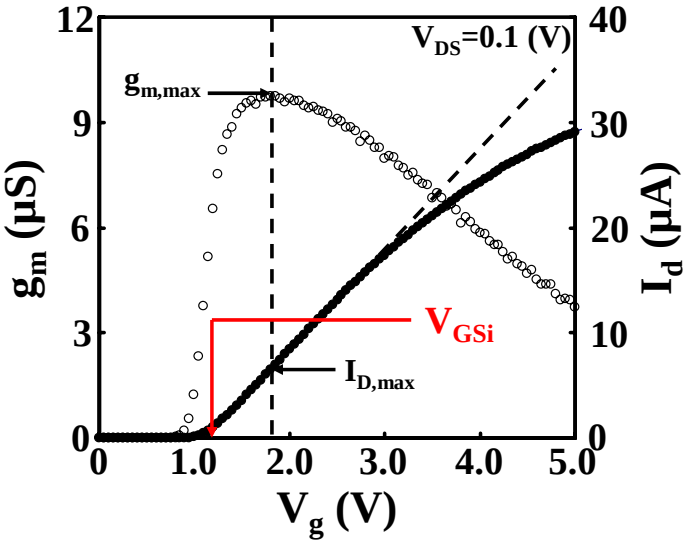


Figure 2.17 : The linear extrapolation method.

2.4.2.2 Subthreshold Slope (*S.S.*) Measurement

The subthreshold slope (*S.S.*) is calculated from below equation.

$$S.S. = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1}$$

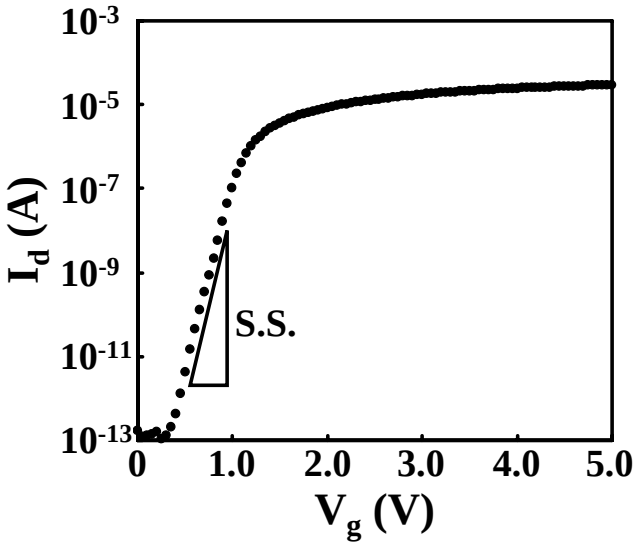


Figure 2.18 : The subthreshold slope calculated from I_d-V_g characteristic.

2.4.2.3 Split C-V Method

One of the most common measurements to obtain the effective mobility (μ_{eff}) is the split C-V method, which combines gate-to-channel capacitance (C_{gc}) and gate-to-bulk capacitance (C_{gb}).

μ_{eff} is obtained from below equation,

$$\mu_{eff} = \frac{g_d L}{W Q_n}$$

where the drain conductance g_d and the inversion charge density Q_n are defined as

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=const\,\tan t}$$

$$Q_n = \int_{V_{FB}}^{V_{GS}} C_{gc} dV_{GS}\,.$$

E_{eff} is obtained from below equation,

$$E_{eff} = \frac{1}{\varepsilon_{Si}}\left(|Q_d| + |Q_n|\right)$$

where ε_{Si}=11.9 and the depletion charge density Q_d are defined as

$$Q_d = \int_{V_{FB}}^{V_{th}} C_{gb} dV_{GS}$$

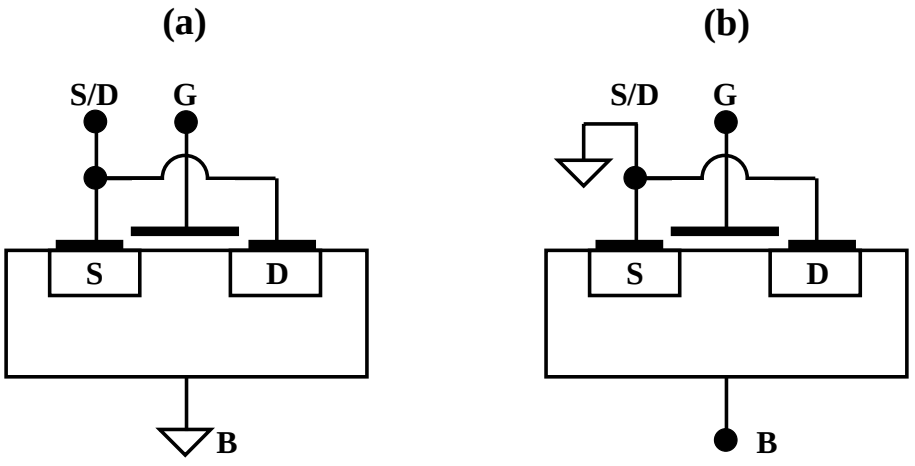


Figure 2.19. Configuration for (a) gate-to-channel, (b) gate-to-substrate capacitance measurements.

Chapter 3

Electrical Characteristics Of n-MOS Capacitors

3.1 Introduction

Figure3.1 shows the process flow for MOS capacitors. Two different processing methods were used to evaluate the effect of in-situ metallization on EOT and leakage current. One is ex-situ PDA process, which is process until deposition in chamber. It could be induce the La_2O_3 moisture absorption and any possible contamination. The other is in-situ PMA process, which is process until upper electrode formation in chamber. The Al-gated has some problems, which induced the Al_2O_3-based interfacial layer. Therefore, Platinum and Tungsten were used top electrodes for MOS capacitors.

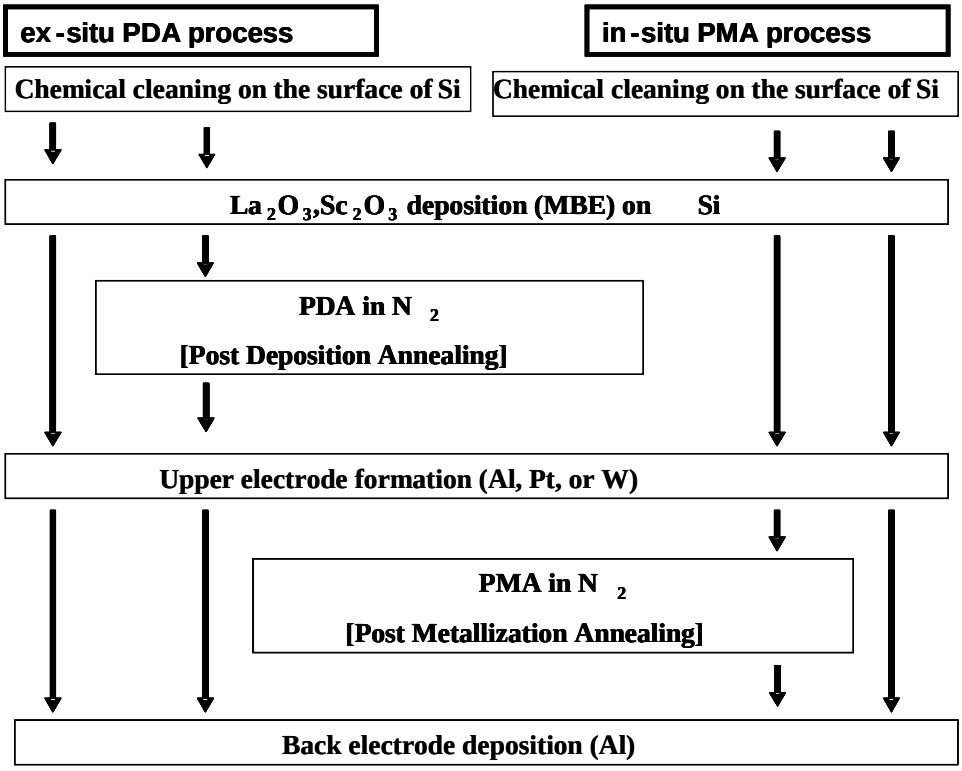


Figure3.1. Process flow for MOS Capacitors

3.1.1 Pt gated n-MOS Capacitors with ex-situ Process

In this session, the Pt gated n-MOS capacitors with La_2O_3/Sc_2O_3 stacked dielectric were fabricated, besides La_2O_3 and Sc_2O_3 single layer samples for reference. The detail fabrication process was mentioned in section 2.1. The thickness of gate dielectric was confirmed by ellipsometer, and we controlled the thickness near 4nm with as-deposited sample. Figure 3.2 shows the physical thickness of La_2O_3, Sc_2O_3, La_2O_3/Sc_2O_3 stacked layer depend on annealing temperature. The thickness of all as-deposited samples was decreased after 300 ^oC annealing, which suggests that the densification of gate dielectric was occurred the thermal treatment. However, for over 500 ^oC annealing, the thickness of the gate dielectric was increased proportionally to temperature annealing. This indicates that the gwoth of the interfacial layer proceeded from the 500 ^oC annealing.

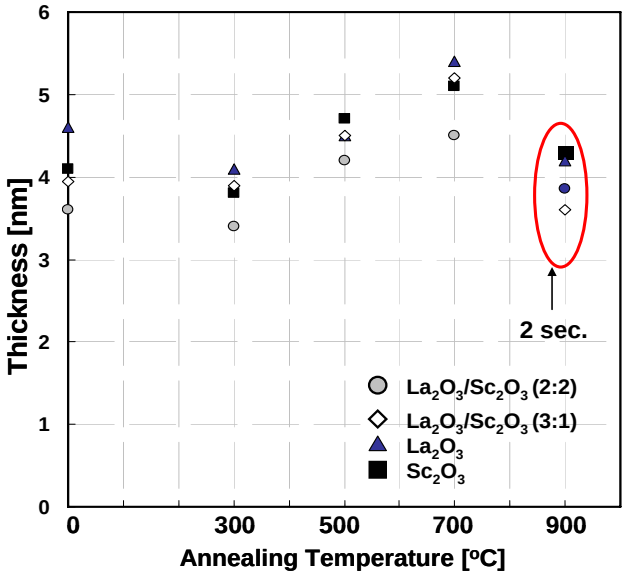


Figure 3.2 Physical Thickness of Gate Dielectric

Figure 3.3 shows the C-V characteristics for the samples of (a)La_2O_3 single layer, (b)Sc_2O_3 single layer, (c),(d)La_2O_3/ Sc_2O_3 stacked sample with PMAs in N_2 ambient at 300 ^oC, 500 ^oC , and 700 ^oC for 5 minutes, 900 ^oC for 2seconds. The La_2O_3/ Sc_2O_3 with structural proportion 2:2 stacked sample keep high capacitance fter 700 ^oC annealing .

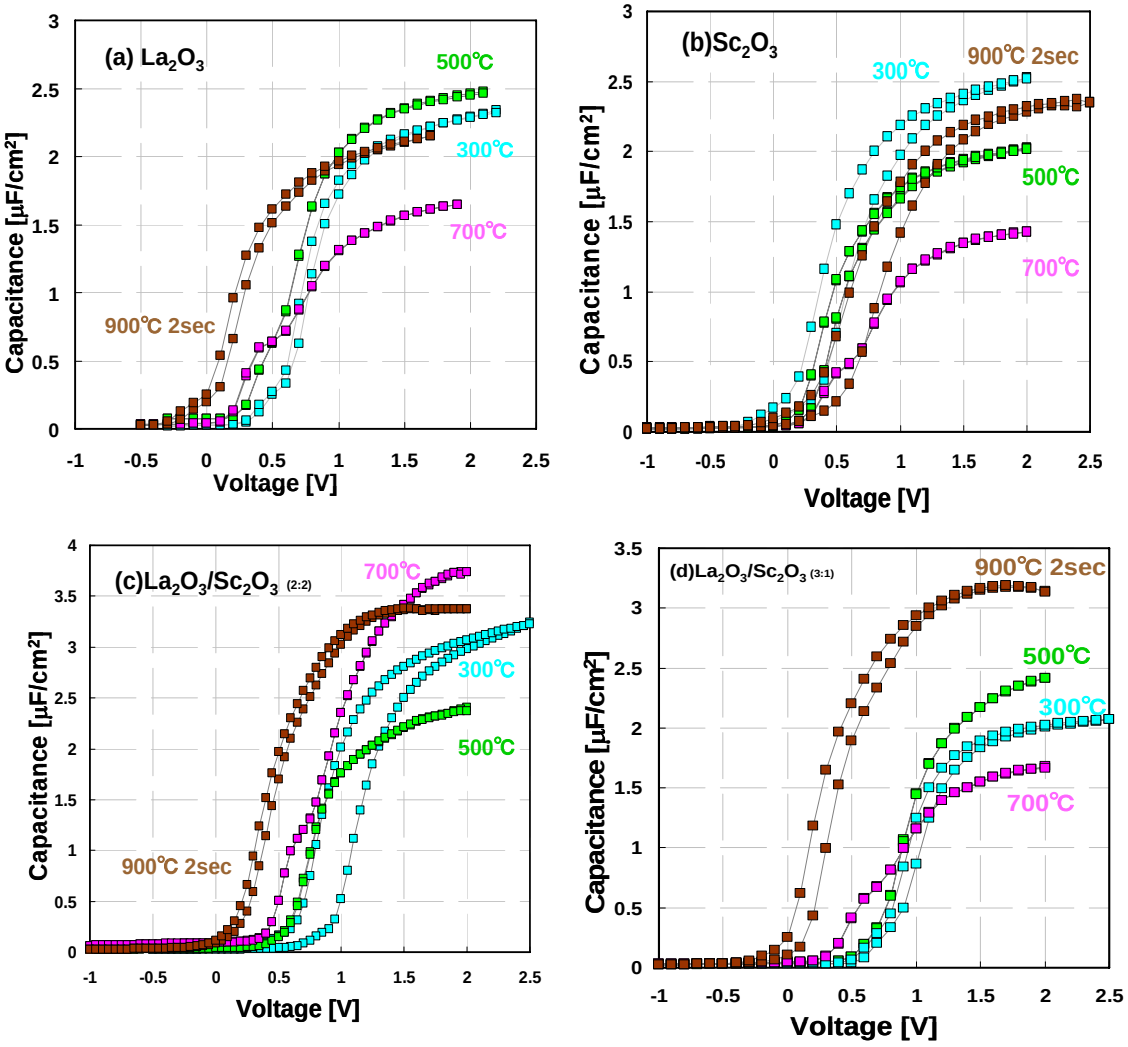


Figure 3.3 The C-V Characteristics of

(a) La_2O_3, (b) Sc_2O_3 (c) La_2O_3/Sc_2O_3 (d) La_2O_3/Sc_2O_3

Figure 3.4 shows the EOT and flatband voltage of (a)La_2O_3 single layer, (b)Sc_2O_3 single layer, (c),(d)La_2O_3/Sc_2O_3 stacked layer depend on the annealing condition. In the case of Sc_2O_3 single layer, the flatband voltage was shifted to positive voltage which suggest the formation of negative charge in the dielectric film.

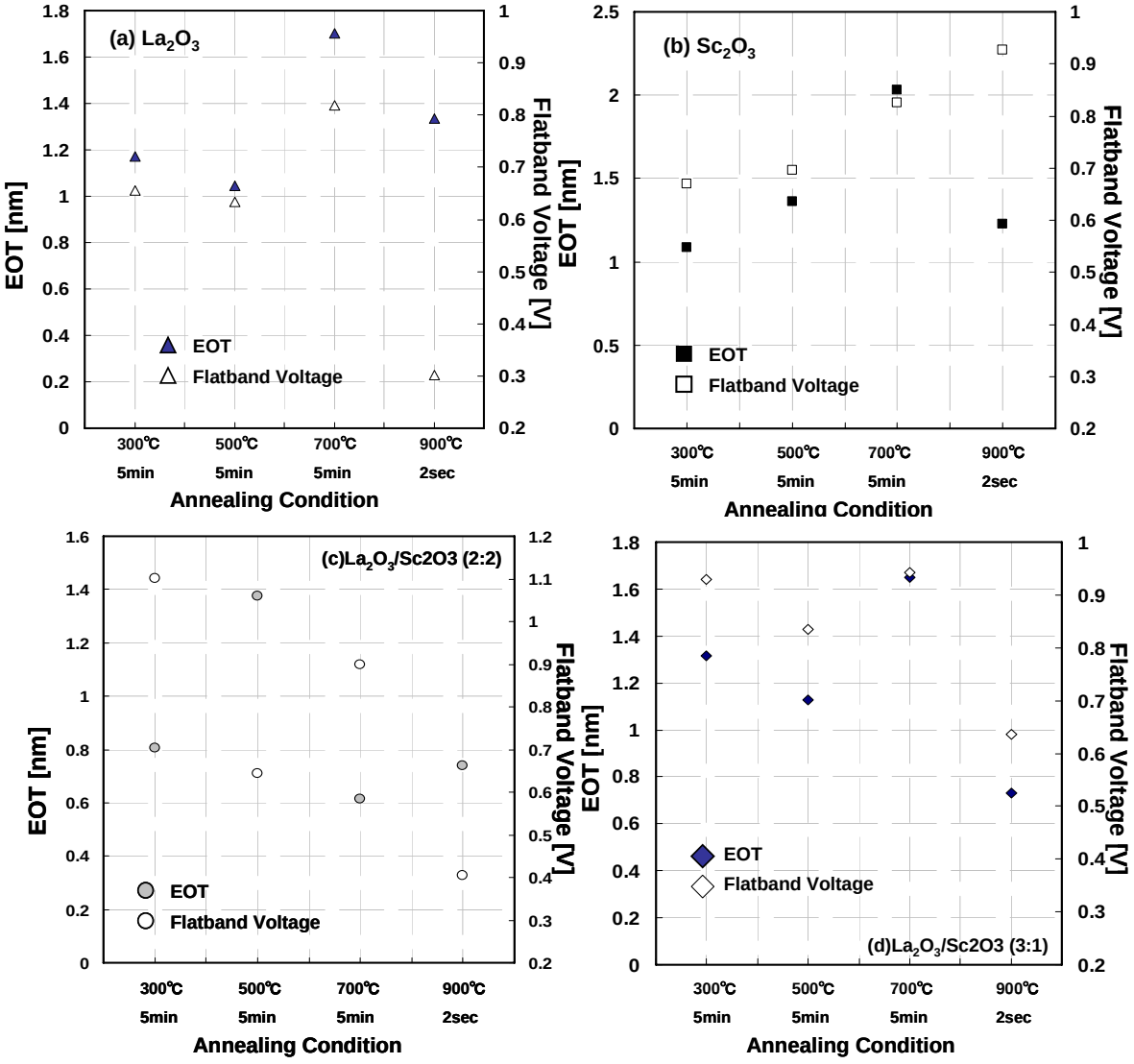


Figure 3.4 The EOT and Flatband Voltage vs. Annealing Condition plots of (a) La_2O_3, (b) Sc_2O_3 (c) La_2O_3/Sc_2O_3 (d) La_2O_3/Sc_2O_3

Figure 3.5 shows the gate leakage current versus EOT plots of each dielectric of (a) 300 ^oC, 5 minutes, (b) 500 ^oC 5 minutes, (c) 700 ^oC 5min, (d) 900 ^oC 2 secconds annealing. In the case of 900 ^oC 2 seconds annealing, the leakage current density of La_2O_3/Sc_2O_3 with structural proportion 3:1 stacked sample was drastically increased. It suggests the structure has same characteristics of La_2O_3 single layer sample due to high possession of La_2O_3 layer. La_2O_3/Sc_2O_3 with structural proportion 2:2 stacked sample was suppressed the increasing the EOT and leakage current with all temperature annealing.

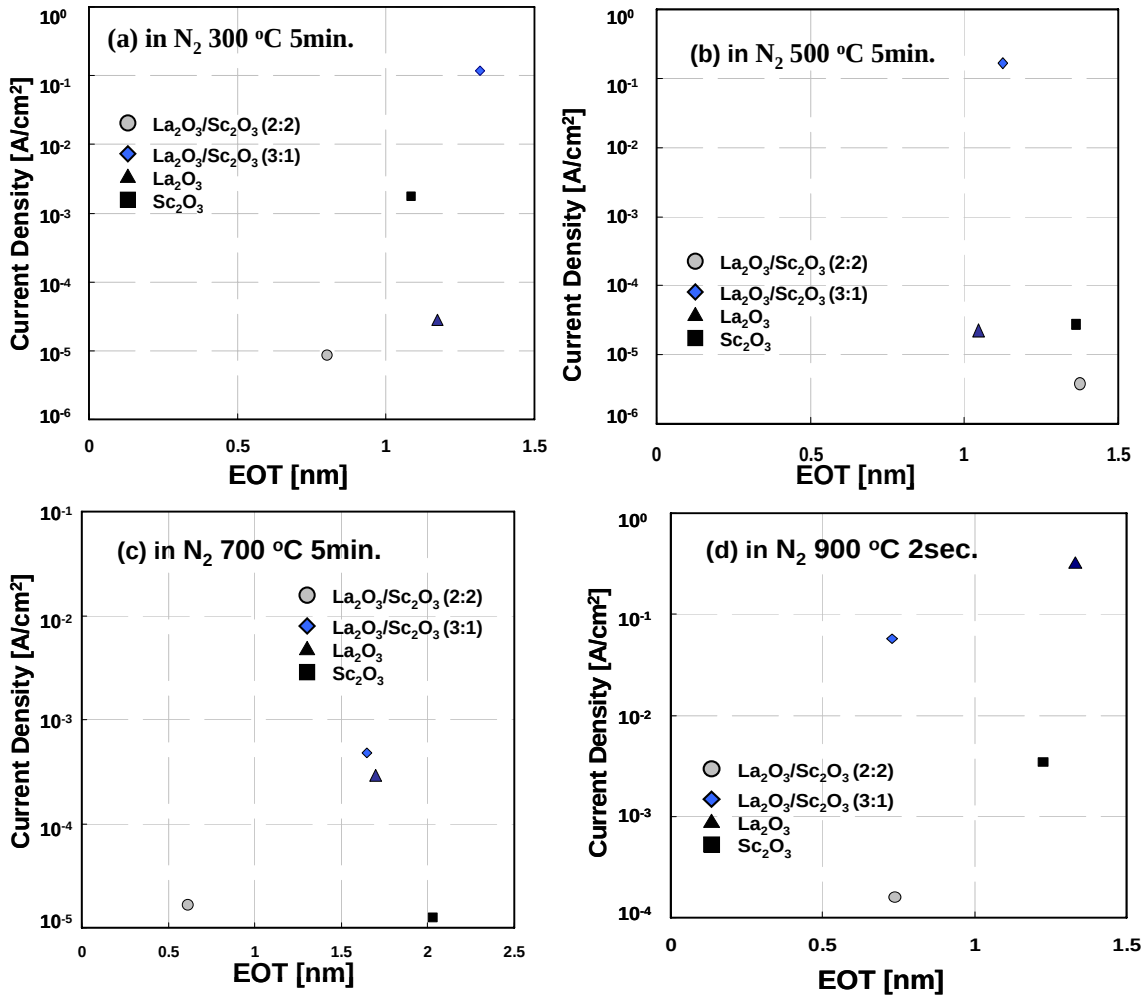


Figure 3.5 Leakage Current Density vs. EOT plots of (a) 300^{o}C5min, (b) 500^{o}C5min, (c) 700^{o}C5min, (d) 900^{o}C2sec.

3.1.2 W gated n-MOS Capacitors with ex-situ Process

In this session, the W gated n-MOS capacitors with La_2O_3/Sc_2O_3 stacked dielectric were fabricated. Figure 3.6 and 3.7 show the C-V, J-V characteristics of W gated MOS capacitors. Flatband shift was occurred over 900 ^oC annealing samples. The capacitance in accumulation decreases proportionally to the superimposed voltage with 900 ^oC and 1000 ^oC annealing samples, because of high leakage current density.

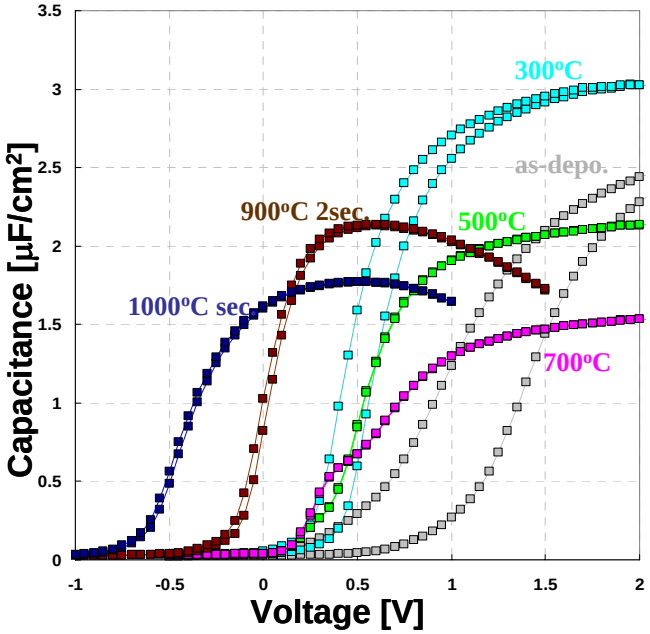


Figure3.6 C-V characteristics of capacitors

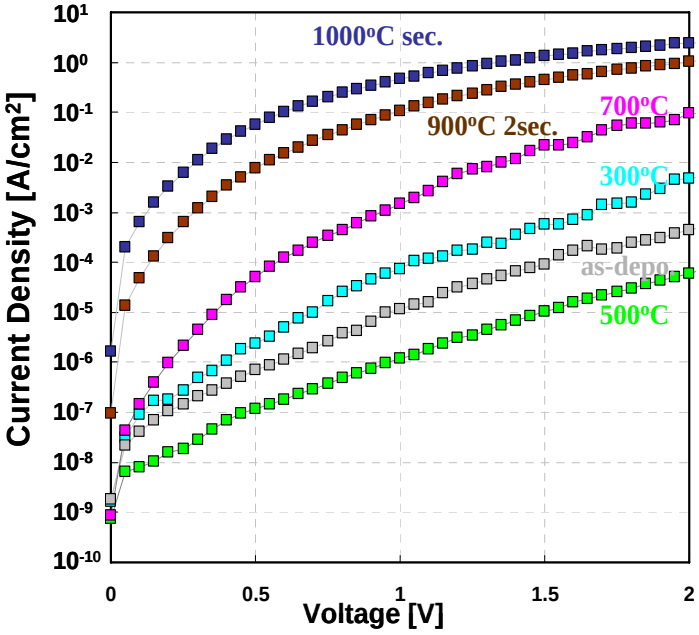


Figure3.7 J-V characteristics of capacitor

Figure 3.8 shows the annealing temperature dependence of EOT for W gated La_2O_3/Sc_2O_3 stacked MOS capacitors. In the view point of the EOT, it was suppressed the increasing the EOT with high temperature annealing sample. However it induced the high leakage current, it is difficult to fabricate less than 1nm EOT MOS capacitors with over 900 ^oC annealing. Therefore, it is required the something process technique to suppress the EOT and leakage current. The in-situ PMA process was tried the next session.

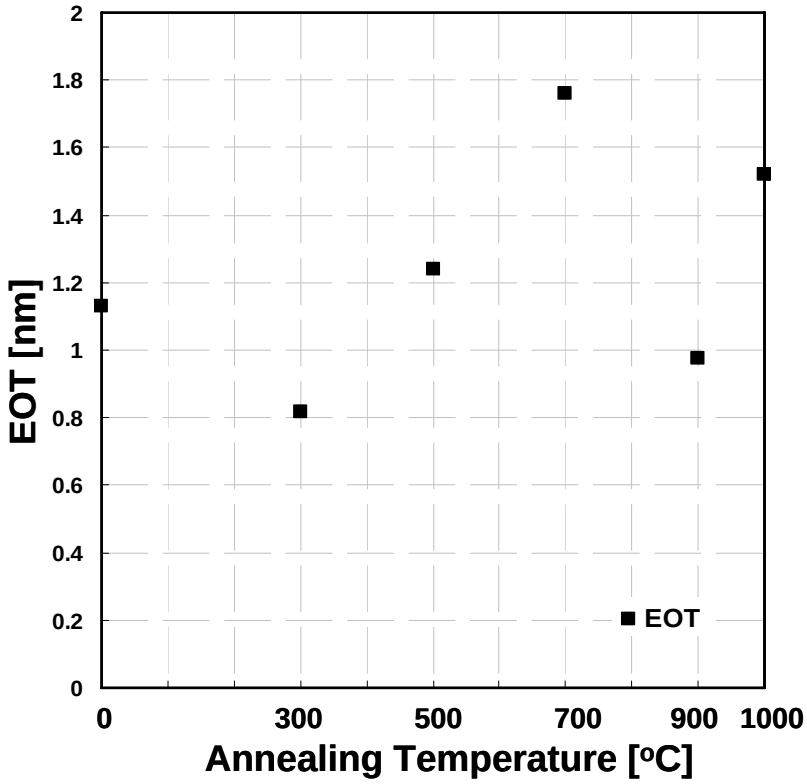


Figure 3.8. Annealing Temperature Dependence of EOT for W capacitors

3.2 W gated n-MOS Capacitors with in-situ PMA

3.2.1 Introduction

As La_2O_3 is known to absorb moisture easily from air, which decreases the dielectric constant, process without exposure to air is preferable. For this purpose, in-situ metal deposition right after the oxide evaporation was performed.

In this session, sputterd W metal gate was selected, because of Figure 3.9 whether hysteresis was appeared or not, good C-V curve and high value of capacitance.

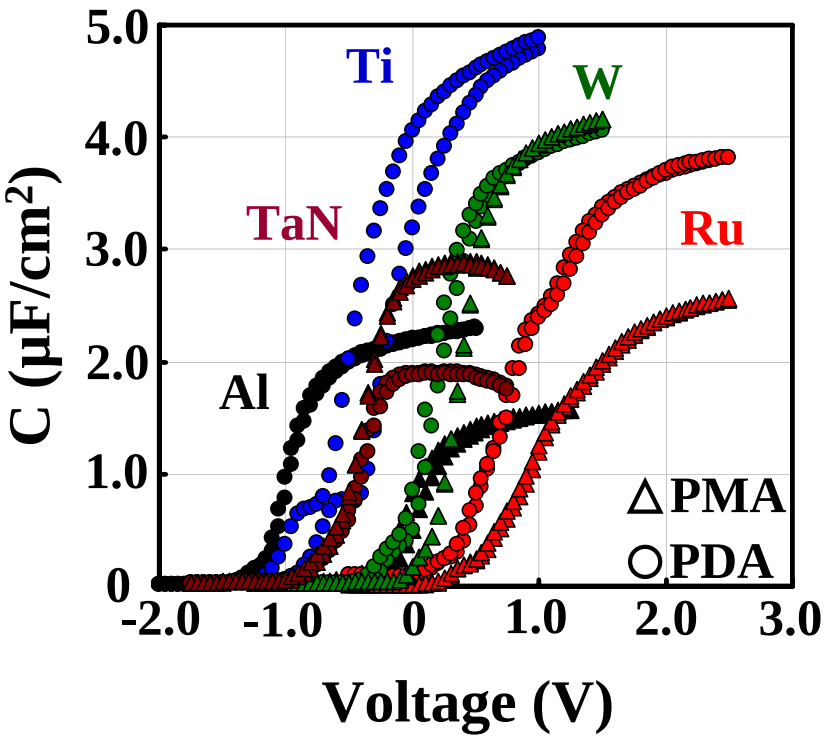


Figure 3.9 the C-V characteristics of each electrode

For La_2O_3 single layer, the EOT of ex-situ process capacitor is larger than that of in-situ process, which is shown in figure 3.10. It suggests in-situ process can prevent from water absorption of La_2O_3 gate dielectric. However, the leakage current of in-situ process is larger than the one of ex-situ process. On the other hand, there is no different between the EOT of ex-situ process and the one of in-situ process in the case of Sc_2O_3 single-layer (Figure 3.11). Therefore, it is evidence that Sc_2O_3 single-layer has property of water resistance. Though, the leakage current with ex-situ process is larger than one of in-situ process in the high electric field area. It is expected that ex-situ process method silicate. In this session, it is mentioned about seeking the optimal deposition of W gate La_2O_3/ Sc_2O_3 capacitors with in-situ process for solution of water absorption problem and large leakage current issue.

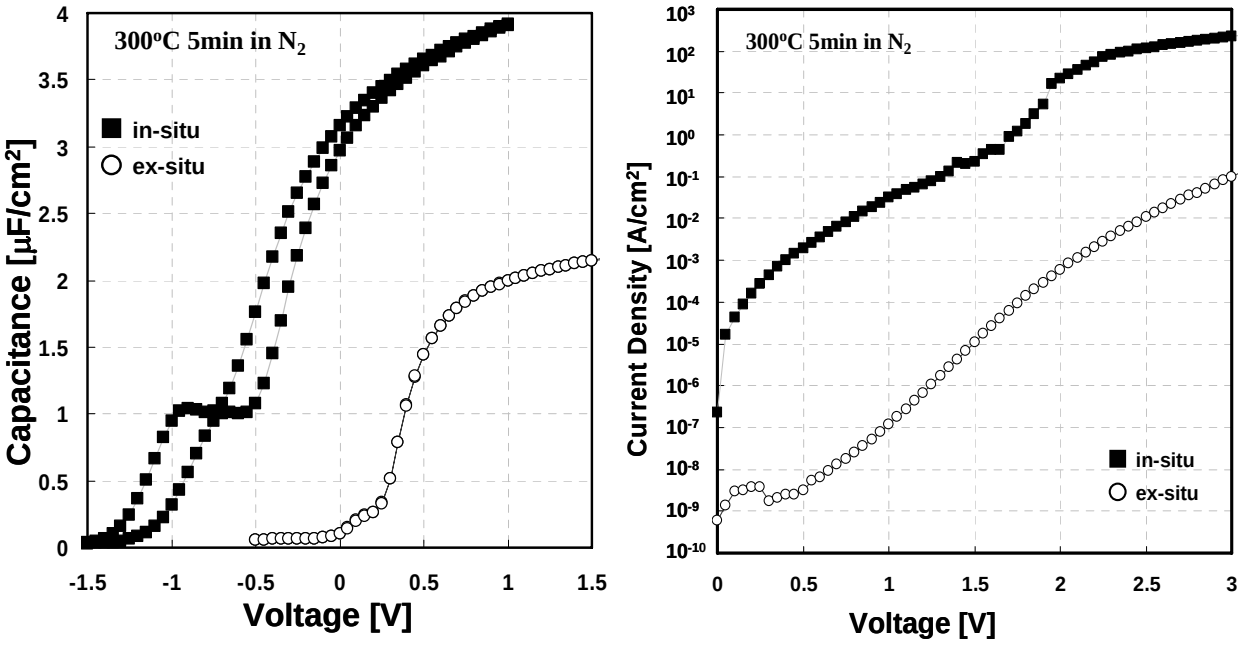


Figure3.10 The C-V and J-V Characteristics of La_2O_3 single layer

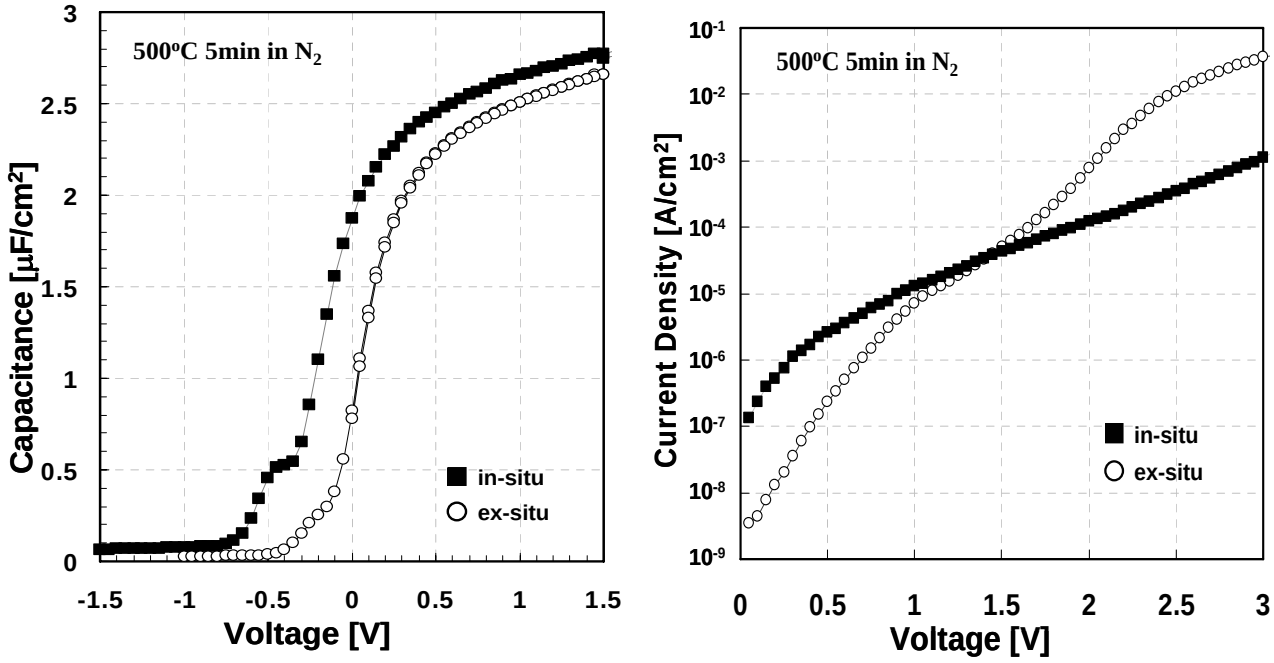


Figure3.11 The C-V and J-V Characteristics of Sc_2O_3 single layer

3.2.2 Depend on Deposition Temperature

The characteristic of gate dielectric is sensitive by deposition condition. For seeking the optimal deposition condition, dielectric deposition was carried out at room temperature and kept a constant temperature of 300 ^{o}C and 500 ^{o}C of substrate temperature. After the deposition, Tungsten top electrodes were formed on some of the samples by in-situ sputtering in sequence. After the electrodes formation, RTAs were performed in N_2 ambient at various temperatures. It is defined the in-situ PMA process. Since the dielectric film was covered by metal with in-situ PMA process, it could not confirm the thickness of dielectric layer by spectroscopic ellipsometry. Therefore, the constant thickness of each dielectric layers were evaporation by using the vibration signal of a crystal oscillator, and each dielectric thickness confirmed with TEM observation.

3.2.2.1 La_2O_3 Single-layer

Figure 3.12 shows the C-V characteristics of La_2O_3 single-layer samples (measurement frequency was 100kHz) of (a) 300 ^oC deposition, (b) 500 ^oC deposition with PMAs in N_2 ambient at 300 ^oC, 500 ^oC , and 700 ^oC for 5 minutes, 900 ^oC and 1000 ^oC for 2seconds. For the samples with N_2 in-situ PMA, the accumulation capacitance decreased with increase of annealing temperature, indicating the growth of the interfacial layer, such as SiOx and La-silicate. In the case of 300 ^oC deposition, there were hysterisis with as-deposited and 300 ^oC annealing sample. The hysterisis was disappeared over 500 ^oC anneling. On the other hand, there were no hysterisis with all samples of La_2O_3 single-layer in the case of 500 ^oC deposition. For the 500 ^oC deposition, the bump around the weak inversion region was larger than the bump of 300 ^oC deposition. It considered that W metal diffuse into La_2O_3 single-layer which induce high interface states.

Figure 3.13 shows the annealing temperature dependence of EOT for La_2O_3 deposited at 300 ^oC and 500 ^oC with PMAs in N_2 ambient at 300 ^oC, 500 ^oC, 700 ^oC, 900 ^oC, and 1000 ^oC for 5 minutes, 900 ^oC, and 1000 ^oC for 2 seconds. The EOT was drastically increased over 500 ^oC annealing in the 300 ^oC and 500 ^oC deposition. In the view point of EOT change, the 500 ^oC deposition samples have more thermal stability property than 300 ^oC deposition samples.

Figure 3.14 shows the annealing temperature dependence of flatband voltage for La_2O_3 deposited at 300 ^oC and 500 ^oC with PMAs in N_2 ambient at 300 ^oC, 500 ^oC , 700 ^oC, 900 ^oC, and 1000 ^oC for 5 minutes. For the 300 ^oC and 500 ^oC deposition, the flat band voltage of La_2O_3 single-layer shifted to positive direction proportionally to temperature annealing, which suggests the formation of negative charge.

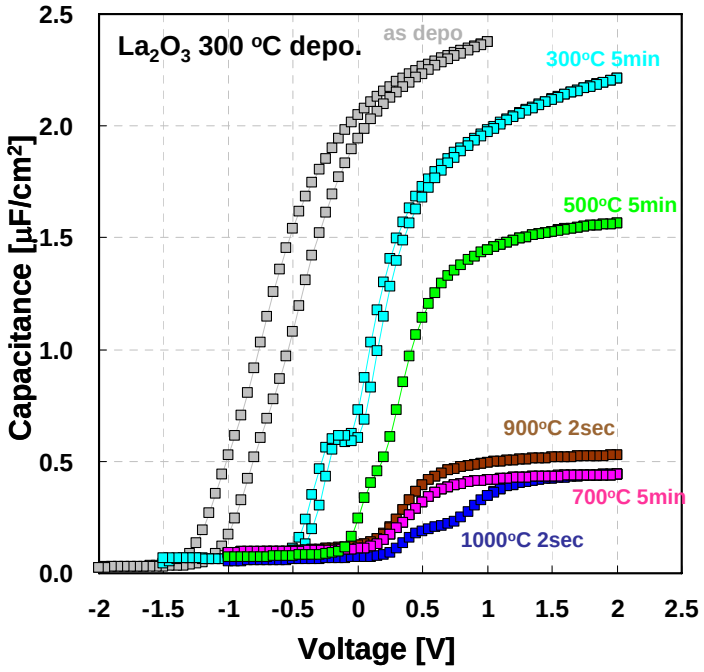


Figure 3.12 (a)C-V Characteristics of La_2O_3 300 ^oC Deposition

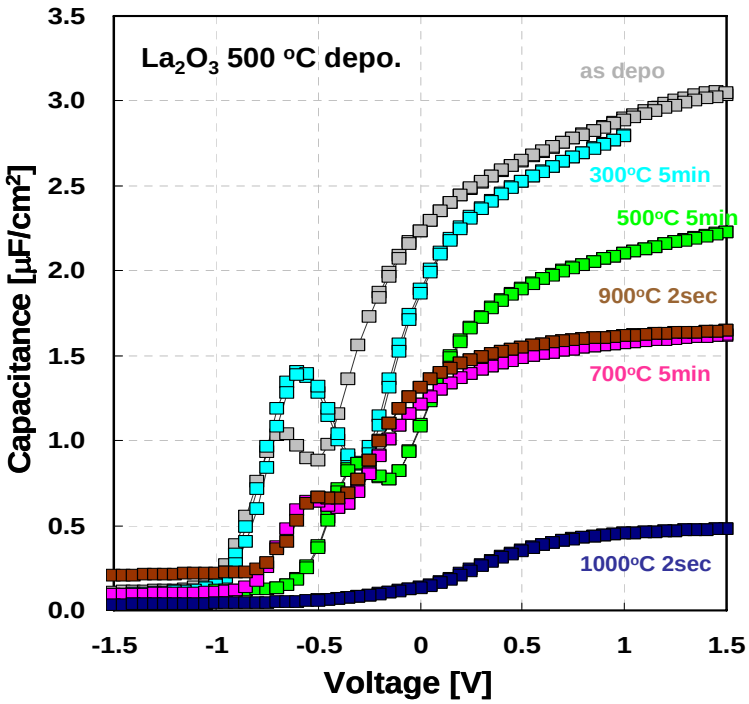


Figure 3.12 (b) C-V Characteristics of La_2O_3 500 ^oC Deposition

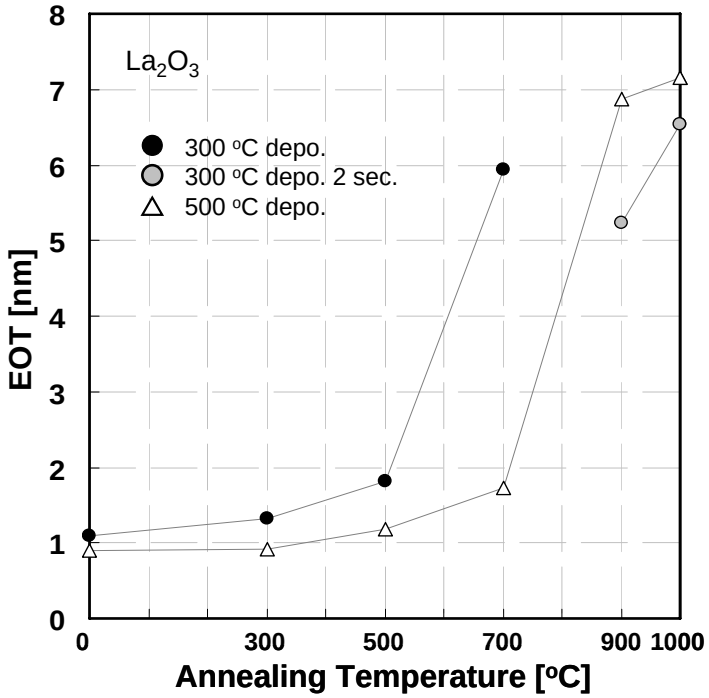


Figure 3.13 Annealing Temperature Dependence of EOT for La_2O_3

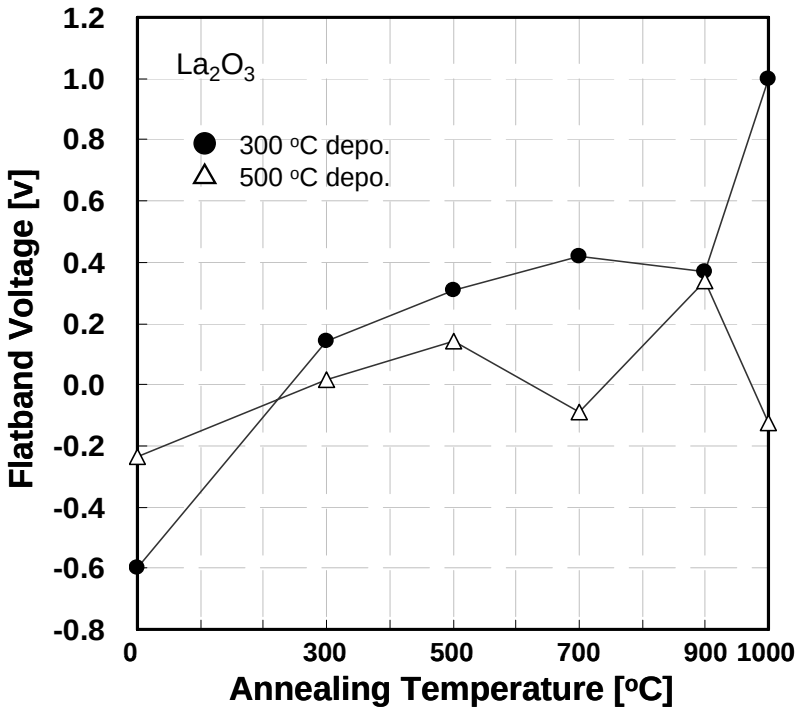


Figure 3.14 Annealing Temperature Dependence of Flatband Voltage for La_2O_3

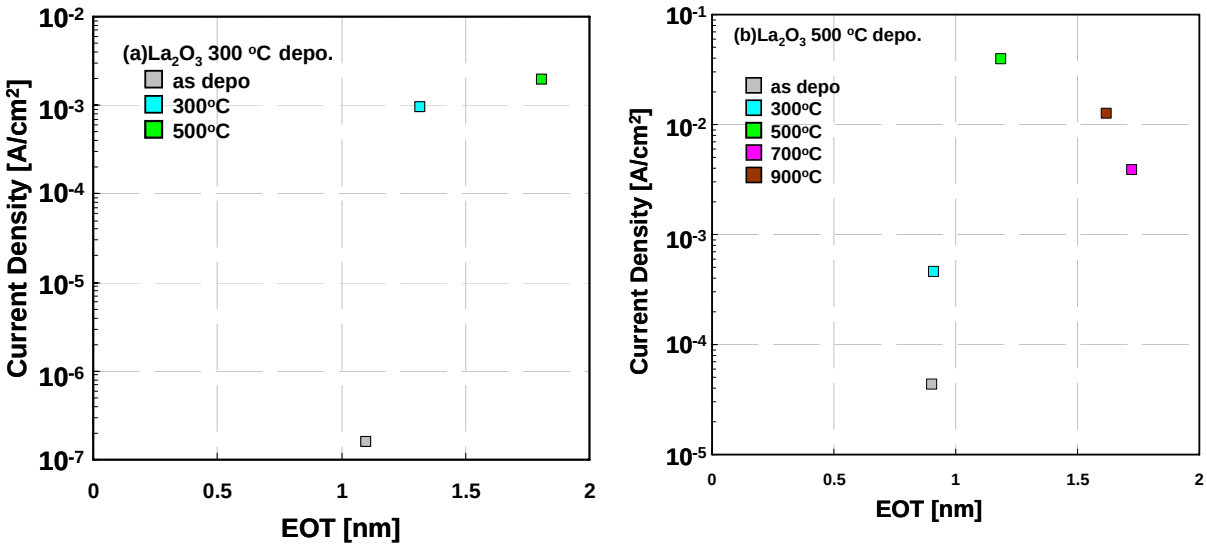


Figure 3.15 leakage current density of La_2O_3 (a)300 °C depo. (b) 500 °C depo.

Figure 3.15 shows the leakage current density of La_2O_3 single-layer (a)300 °C deposition samples (b) 500 °C deposition samples. Both of samples with as deposited were lowest leakage current. Figure 3.16 shows the interface state density of La_2O_3 single-layer with 300 °C and 500 °C deposited sample for various temperatures annealing. La_2O_3 singel-layer sample with 300 °C and 500 °C deposited sample was showed high interface state density after 700 °C 5 minutes annealing.

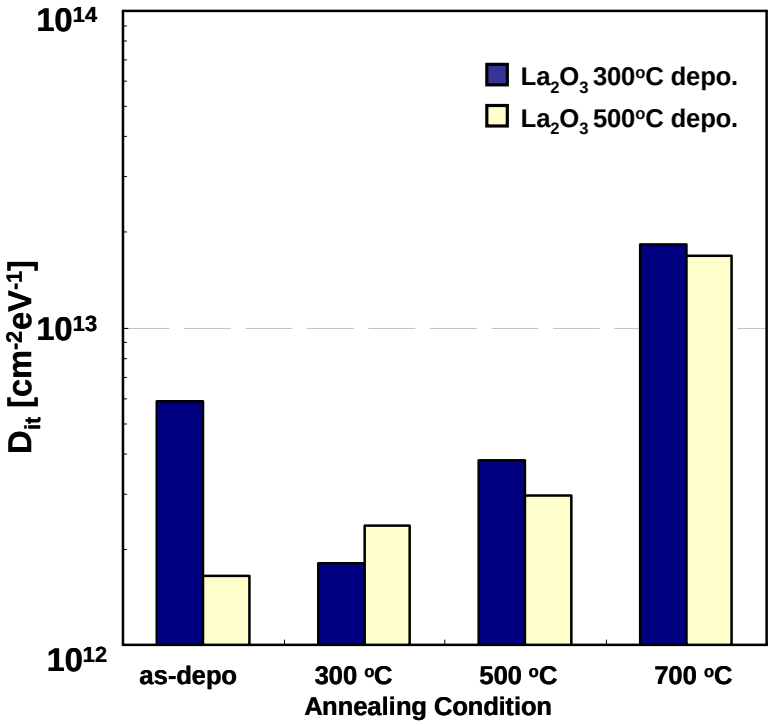


Figure 3.16 Interface State Density of La_2O_3 with 300 °C and 500 °C depo.

3.2.2.2 Sc_2O_3 Single-layer

Figure 3.17 shows the C-V characteristics (measurement frequency was 100kHz) for the samples of Sc_2O_3 single-layer (a) room temperature deposition, (b) 300 ^oC deposition, (c) 500 ^oC deposition with PMAs in N_2 ambient at 300 ^oC, 500 ^oC , and 700 ^oC for 5 minutes, 900 ^oC and 1000 ^oC for 2seconds. For the samples with N_2 in-situ PMA, the accumulation capacitance decreased with increase of annealing temperature, indicating the growth of the interfacial layer. The bump around the weak inversion region was observed. For the room temperature deposition, there were no hysterisis with 300 ^oC and 500 ^oC annealing sample. Although, the hysterisis was appeared with 700 ^oC and 900 ^oC annealing sample again. It was considered that the interfacial layer induced the memory effect. For the room 300 ^oC deposition, there were hysterisis with as-deposited and 300 ^oC annealing sample. The hysterisis was disappeared over 500 ^oC anneling. Taking note of more increase of capacitance for the sample annealed at 300 ◦C rather than as-deposited sample, this might be caused by densification of gate dielectric.

Judging from result of La_2O_3 single-layer at the 500 ^oC deposition, it was considered that 500 ^oC deposition has the effect of 500 ^oC annealing, so it was predicted no hysterisis with all samples of 500 ^oC deposition. Although, there were hysterisis with as-deposited and 300 ^oC annealing sample. The CV curves of as-deposited and 300 ^oC annealing sample were very similar. N_2 ambient annealing for Sc_2O_3 single layer has good effect which reduces the hysterisis.

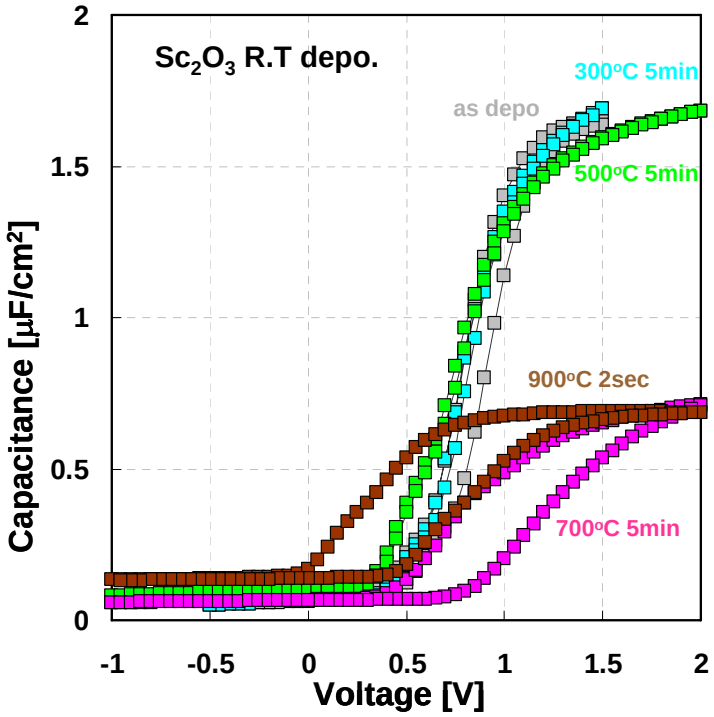


Figure 3.17 (a) C-V Characteristics of Sc_2O_3 Room Temperature Deposition

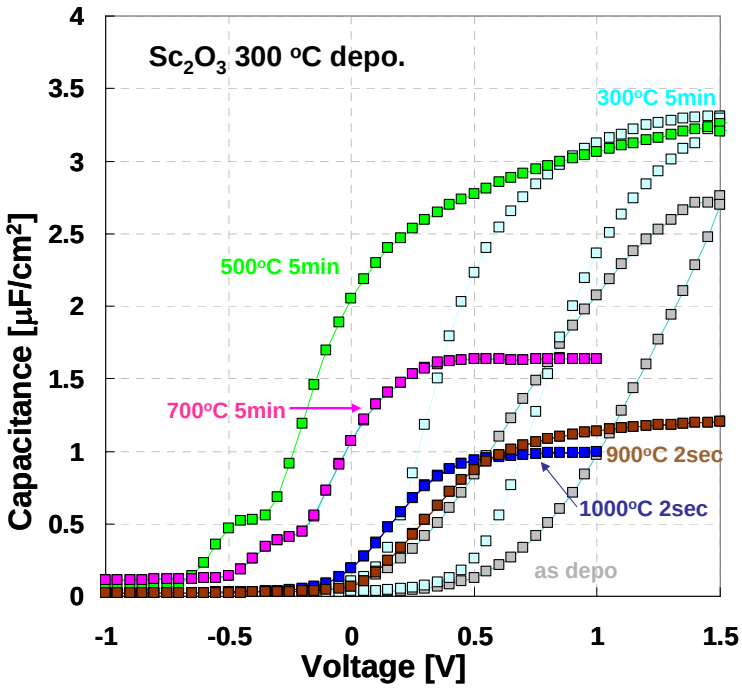


Figure 3.17 (b) C-V Characteristics of Sc_2O_3 300 ^oC Deposition

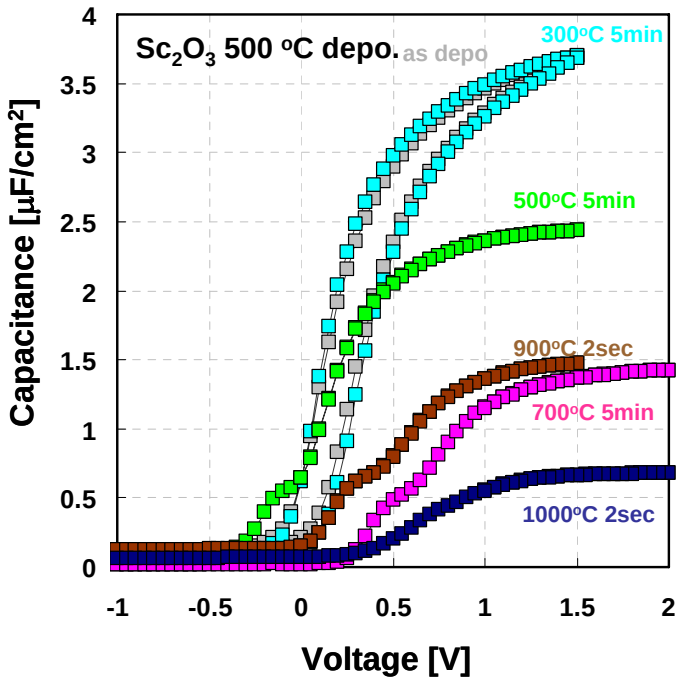


Figure 3.17 (c) C-V Characteristics of Sc_2O_3 500 ^oC Deposition

Figure 3.18 shows the annealing temperature dependence of EOT for Sc_2O_3 deposited at room temperature, 300 ^oC, 500 ^oC with PMAs in N_2 ambient at 300 ^oC, 500 ^oC, 700 ^oC, 900 ^oC, and 1000 ^oC for 5 minutes. The EOT comparisons of as-deposited sample between room temperature, 300 ^oC, and 500 ^oC deposition, the tendency is contribute to the densification of gate dielectric after deposition. In the case of the room temperature deposition sample, the EOT was drastically increased over 500 ^oC annealing, which suggests the formation of silicate and SiO_2 interfacial layers. In the both cases of the 300 ^oC and 500 ^oC deposition sample, the EOT was showed to suppress the EOT up to 700^oC annealing. In the view point of EOT change, the 300 ^oC and 500 ^oC deposition samples have more thermal stability property than as-deposited samples.

Figure 3.19 shows the annealing temperature dependence of flatband voltage for Sc_2O_3 deposited at room temperature, 300 ^oC, 500 ^oC with PMAs in N_2 ambient at 300 ^oC, 500

^{o}C , 700 ^{o}C, 900 ^{o}C, and 1000 ^{o}C for 5 minutes. For the room temperature deposition, the flat band voltage of Sc_2O_3 single-layer was stable at around 0.7 V up to 700 ^{o}C annealilng. For the 300 ^{o}C deposition, the flat band voltage of Sc_2O_3 single-layer shifted to negative direction proportionally to temperature annealing, which suggests the formation of positive charge. For the 500 ^{o}C deposition, the flat band voltage of Sc_2O_3 single-layer shifted to positive direction proportionally to temperature annealing, which is opposite direction as compared to that of Sc_2O_3 with 300 ^{o}C deposition.

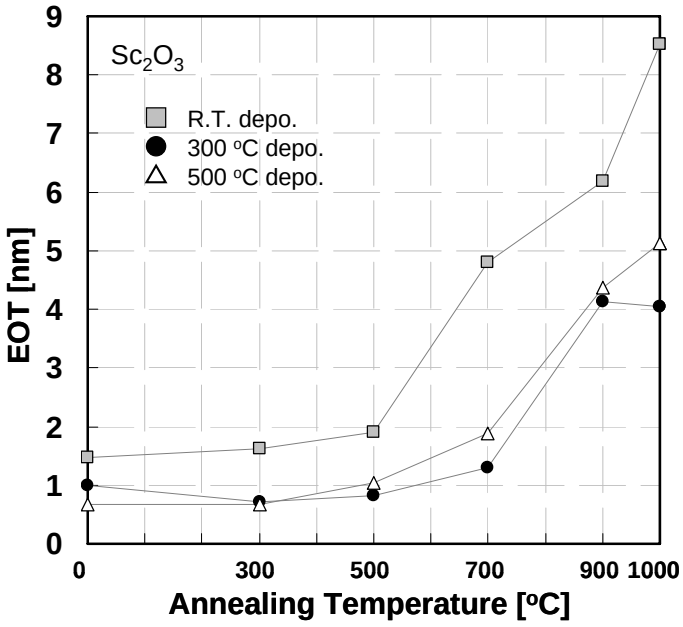


Figure 3.18 Annealing Temperature Dependence of EOT for Sc_2O_3

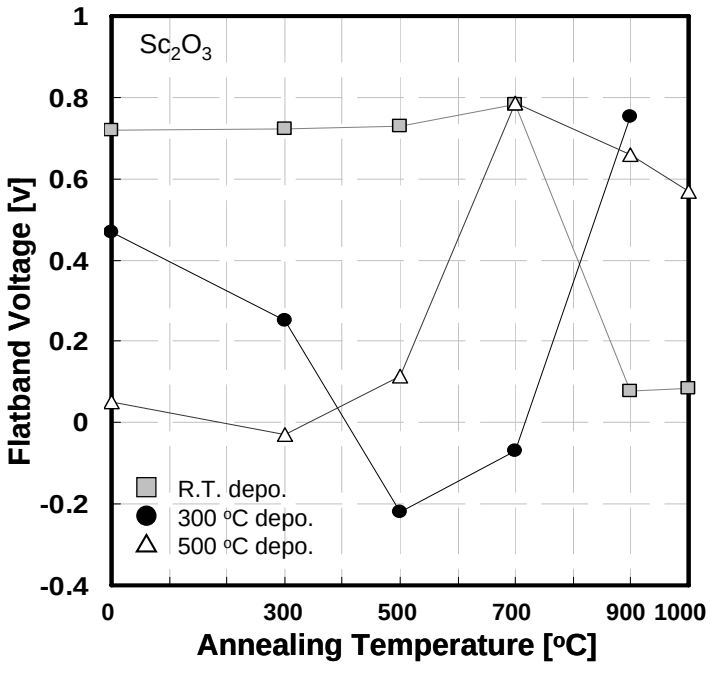


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Figure 3.19 Annealing Temperature Dependence of Flatband Voltage for Sc_2O_3

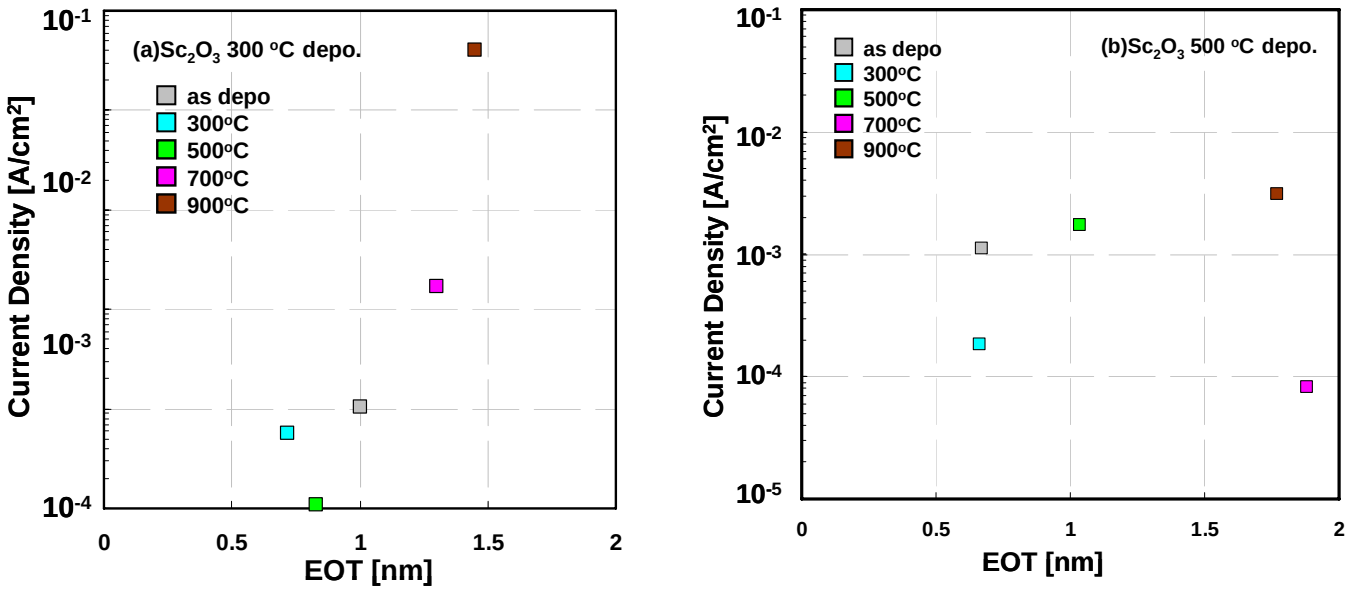


Figure 3.20 Leakage Current Density of Sc_2O_3 (a) 300°C depo. (b) 500°C depo.

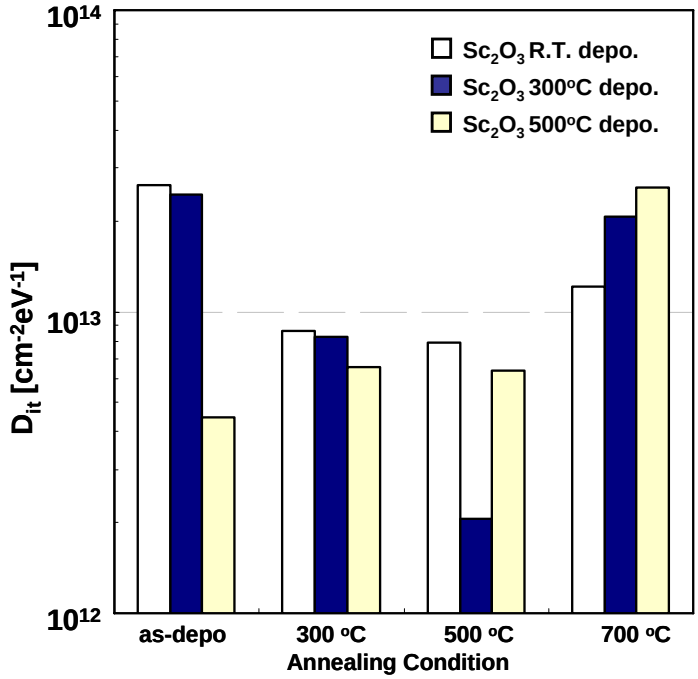


Figure 3.21 Interface state density of Sc_2O_3 single-layer with room temperature, 300 °C, and 500 °C deposited sample

Figure 3.20 shows the leakage current density of Sc_2O_3 single-layer (a) 300°C deposition samples (b) 500°C deposition samples. In the case of La_2O_3 single-layer, as deposited sample was the lowest leakage current density. However, in the case of Sc_2O_3 single-layer, it is considered as deposited sample has a lot of defect. It induced the high leakage current. Figure 3.21 shows the interface state density of Sc_2O_3 single-layer with room temperature, 300 °C, and 500 °C deposited samples for various temperatures annealing. All Sc_2O_3 singel-layer samples, which were room temperature, 300 °C, and 500 °C deposited samples, were showed high interface state density after 700 °C 5 minutes annealing.

3.2.2.3 La_2O_3/Sc_2O_3 stacked layer

Figure 3.22 shows the CV characteristics (measurement frequency was 100kHz) that are for the samples of La_2O_3/Sc_2O_3 stacked layer (a) room temperature deposition, (b) 300 ^oC deposition, (c) 500 ^oC deposition with PMAs in N_2 ambient at 300 ^oC, 500 ^oC , and 700 ^oC for 5 minutes, 900 ^oC and 1000 ^oC for 2seconds. For the samples with N_2 PMA, the accumulation capacitance decreased with increase of annealing temperature, indicating the growth of the interfacial layer. The bump around the weak inversion region was observed. There were no hysterisis with all samples of room temperature deposition. For the room 300 ^oC deposition, the point different from room temperature and 500 ^oC deposition is that as-deposited sample had the highest accumulation capacitance. For the room 300 ^oC and 500 ^oC deposition, there were hysterisis with as-deposited and 300 ^oC annealing sample. The hysterisis was disappeared over 500 ^oC anneling.

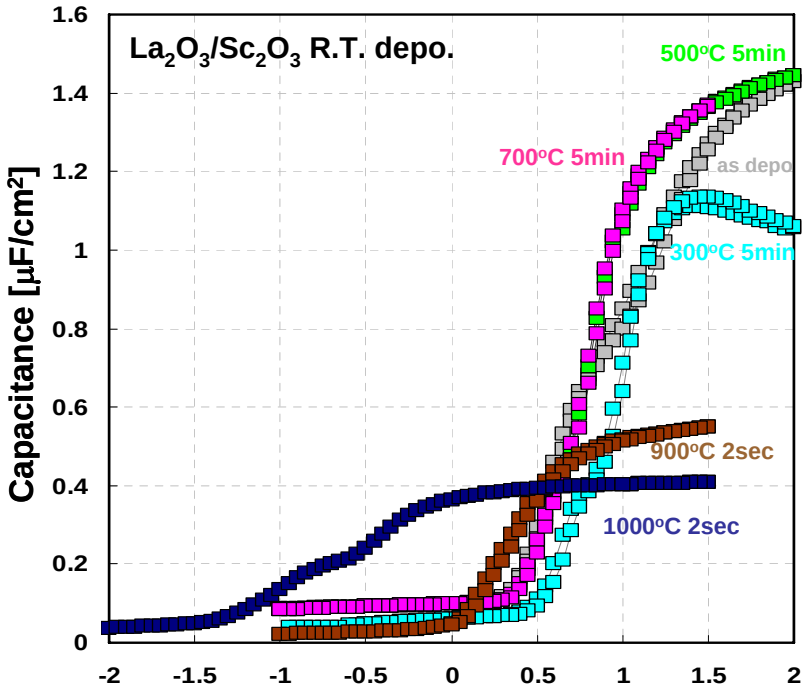


Figure 3.22(a) C-V Characteristics of La_2O_3/Sc_2O_3 Room Temperature Deposition

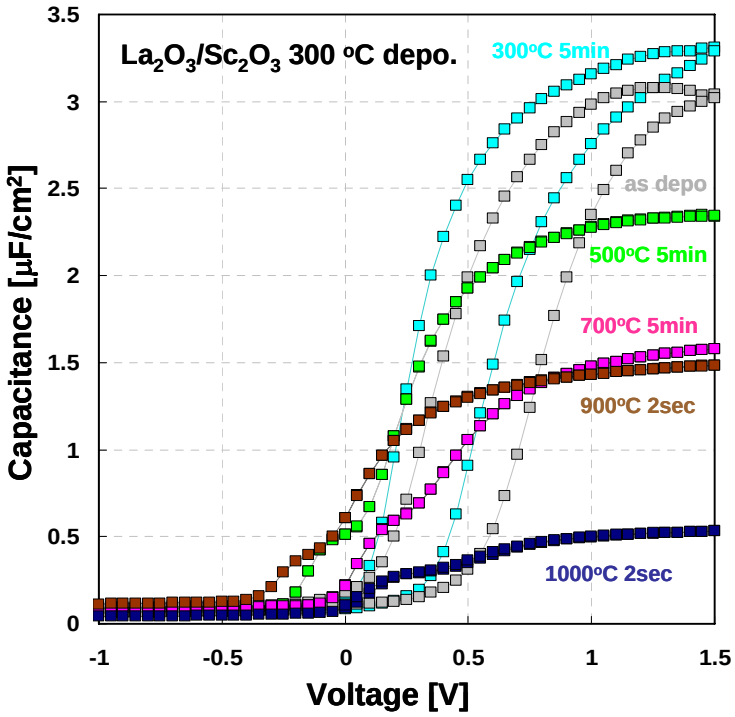


Figure 3.22(b) C-V Characteristics of La_2O_3/Sc_2O_3 300 °C Deposition

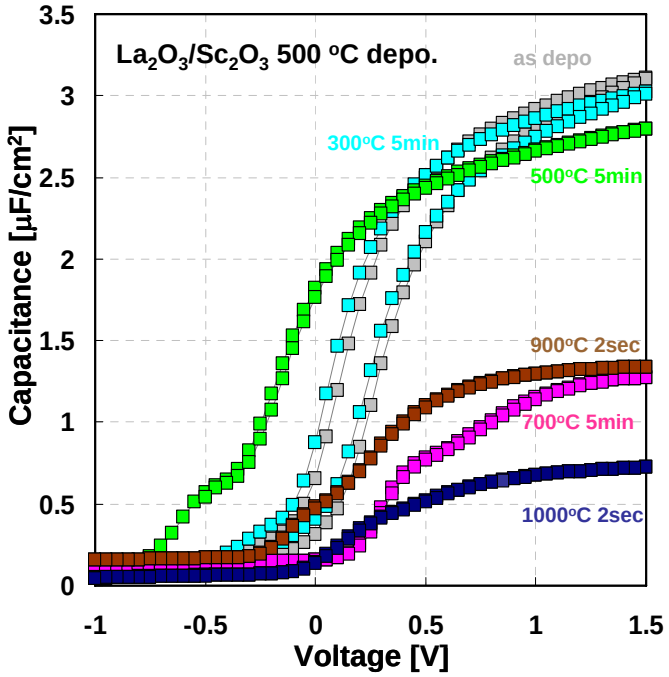


Figure 3.22(c) C-V Characteristics of La_2O_3/Sc_2O_3 500 °C Deposition

Figure 3.23 shows the annealing temperature dependence of EOT for La_2O_3/Sc_2O_3 deposited at room temperature, 300 ^oC, 500 ^oC with PMAs in N_2 ambient at 300 ^oC, 500 ^oC, 700 ^oC, 900 ^oC, and 1000 ^oC for 5 minutes. In the case of the room temperature deposition sample, the EOT of as-deposited sample is larger than the EOT of 300 ^oC and 500 ^oC deposition sample. It considered that La_2O_3/Sc_2O_3 is difficult to achieve under the 1nm of EOT by room temperature deposition method. In the both cases of the 300 ^oC and 500 ^oC deposition sample, the EOT was showed to suppress the EOT up to 700^oC annealing. In the view point of EOT change, the room temperature and 300 ^oC deposition samples have more thermal stability property than 500 ^oC deposition samples.

Figure 3.24 shows the annealing temperature dependence of flatband voltage for La_2O_3/Sc_2O_3 deposited at room temperature, 300 ^oC, 500 ^oC with PMAs in N_2 ambient at 300 ^oC, 500 ^oC , 700 ^oC, 900 ^oC, and 1000 ^oC for 5 minutes. In the both case of the room temperature deposition sample, the flat band voltage of La_2O_3/Sc_2O_3 stacked layer shifted to negative direction proportionally to temperature annealing, which suggests the formation of positive charge. In the both cases of the 300 ^oC and 500 ^oC deposition sample, the flat band voltage of La_2O_3/Sc_2O_3 stacked layer shifted to positive direction proportionally to temperature annealing, which is opposite direction as compared to that of La_2O_3/Sc_2O_3 with room temperature deposition.

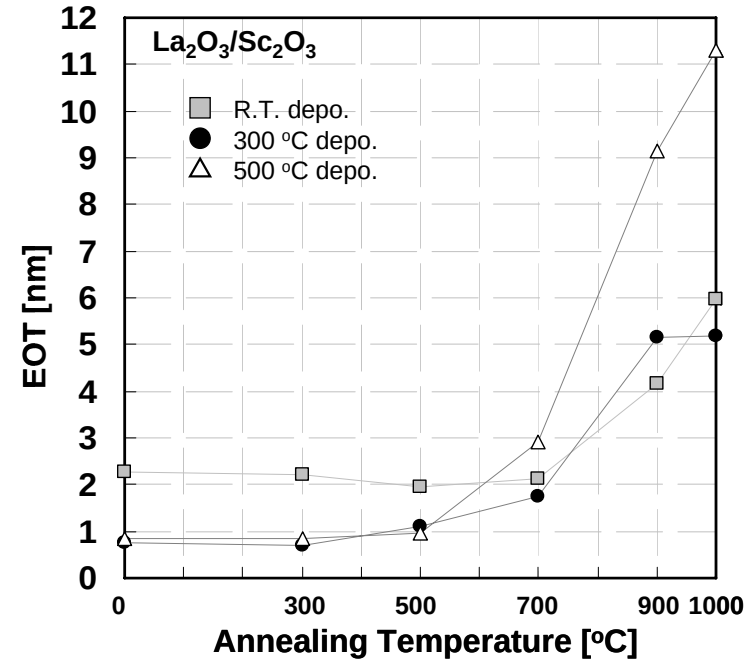


Figure 3.23 Annealing Temperature Dependence of EOT for La_2O_3/Sc_2O_3

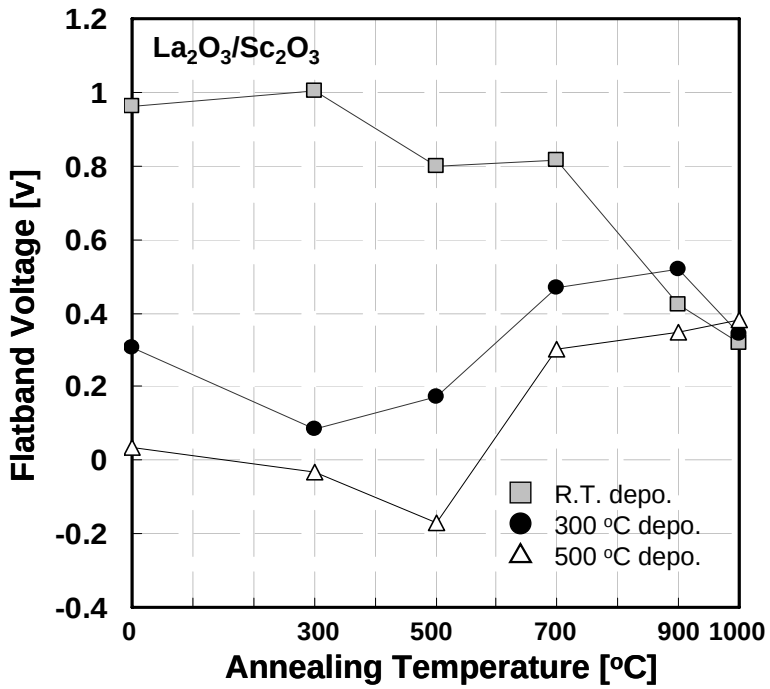


Figure 3.24 Annealing Temperature Dependence of Flatband Voltage for La_2O_3/Sc_2O_3

Figure 3.25 shows the leakage current density of La_2O_3/ Sc_2O_3 stacked sample with 300 ^oC and 500 ^oC deposited sample for various temperatures annealing. In the case of 300 ^oC, the leakage current and EOT suppressed until 500 ^oC annealing samples. Figure 3.26 shows the interface state density of La_2O_3/ Sc_2O_3 stacked sample with room temperature, 300 ^oC, and 500 ^oC deposited sample for various temperatures annealing. La_2O_3/ Sc_2O_3 stacked samples with room temperature and 500 ^oC deposited sample were showed high interface state density after 700 ^oC 5 minutes annealing. In the view point of interface state density, 300 ^oC deposition was considered best method for formation of La_2O_3/ Sc_2O_3 stacked insulator.

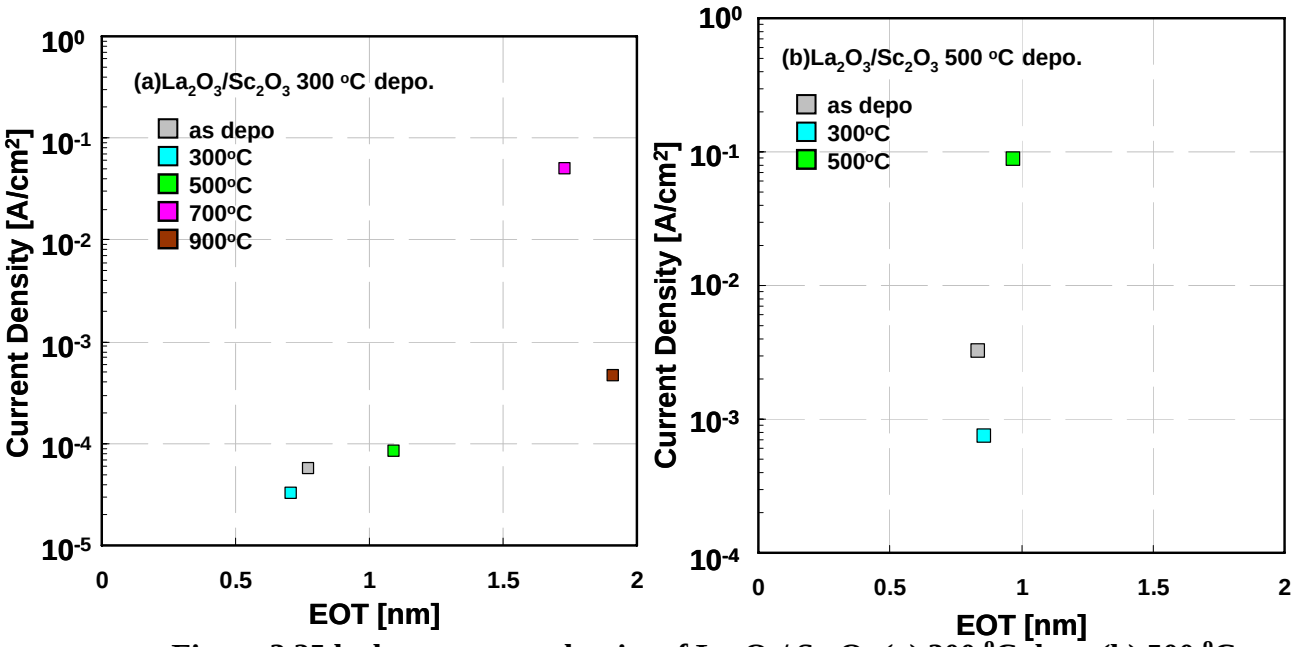


Figure 3.25 leakage current density of La_2O_3/ Sc_2O_3 (a) 300 ^oC depo.(b) 500 ^oC depo. samples for various temperatures annealing.

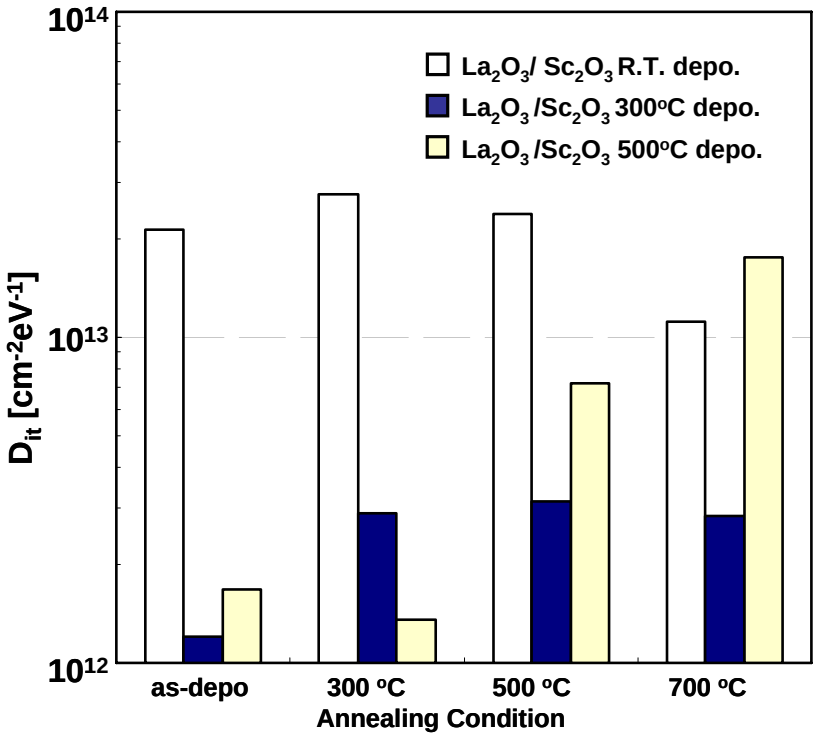


Figure 3.26 Interface state density of La_2O_3/ Sc_2O_3 with Room Temperature, 300 °C, and 500 °C deposited samples.

3.5.2 Depend on Deposition Structure

3.3.3.1 Introduction

Figure3.27 shows the 5 types samples which explain in this section. For seeking the optimal deposition structure, dielectric deposition was carried out 3 different thickness for La_2O_3/Sc_2O_3 stacked structures, and as a reference, we prepared La_2O_3 and Sc_2O_3 single-layer samples. The thickness of insulators were measured by cross Sectional TEM. All samples kept a constant temperature 300 ^oC of substrate temperature in dielectric deposition. For this experiment, Sputtered tungsten was used as a metal electrode.

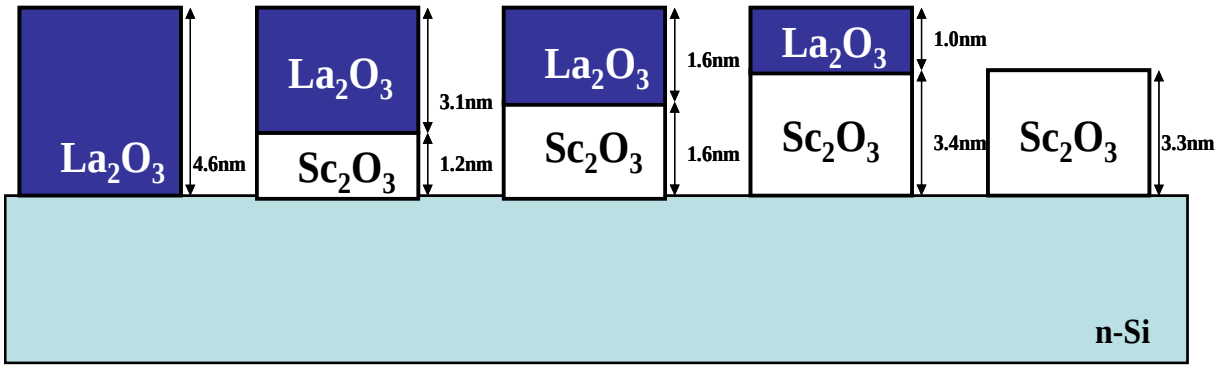


Figure3.27: 5types dielectric structure

3.3.3.2 La_2O_3 Single-layer

Figure 3.27 shows the CV characteristics of La_2O_3 single-layer sample (measurement frequency was 100kHz) with PMAs in N_2 ambient at 300 ^oC, 500 ^oC, and 700 ^oC for 5 minutes. The accumulation capacitance decreased with increase of annealing temperature, indicating the growth of the interfacial layer, such as SiO_x and La-silicate and SiO_x. The accumulation capacitance with 700 ^oC annealing sample was drastically decreased. The bump around the weak inversion region was observed with 300 ^oC annealing sample. The flat band voltage of La_2O_3 single-layer shifted to positive direction proportionally to temperature annealing, which suggests the formation of negative charge.

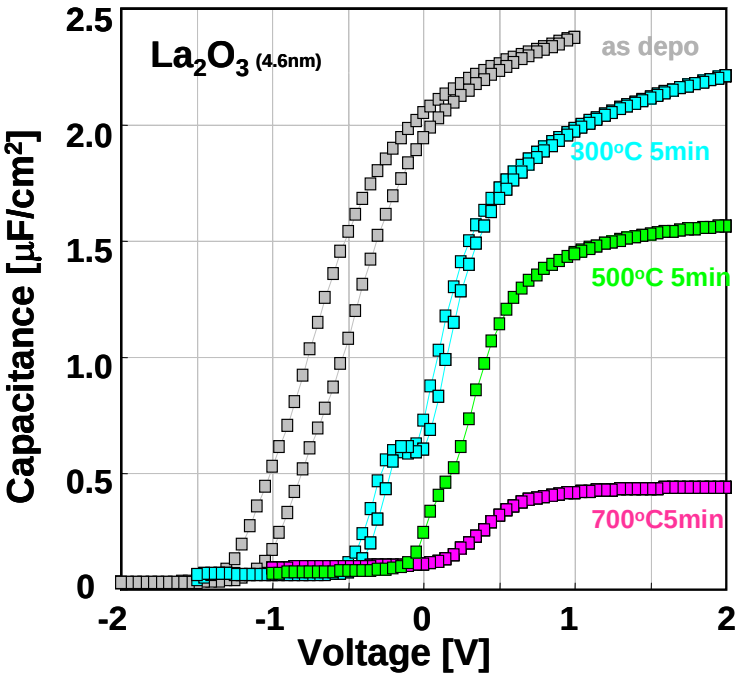


Figure3.27: C-V characteristics of La_2O_3 single-layer

3.3.3.3 Sc_2O_3 Single-layer

Figure 3.28 shows the CV characteristics of Sc_2O_3 single-layer sample (measurement frequency was 100kHz) with PMAs in N_2 ambient at 300 ^oC, 500 ^oC, and 700 ^oC for 5 minutes. The accumulation capacitance decreased with increase of annealing temperature from 300 ^oC to 700 ^oC, indicating the growth of the interfacial layer, such as SiO_x and Sc-silicate. The different point from La_2O_3 single-layer is that 300 ^oC annealing sample had the highest accumulation capacitance. The bump around the weak inversion region was observed with 300 ^oC and 500 ^oC annealing samples. The flat band voltage of Sc_2O_3 single-layer shifted to negative direction proportionally to temperature annealing, which suggests the formation of positive charge.

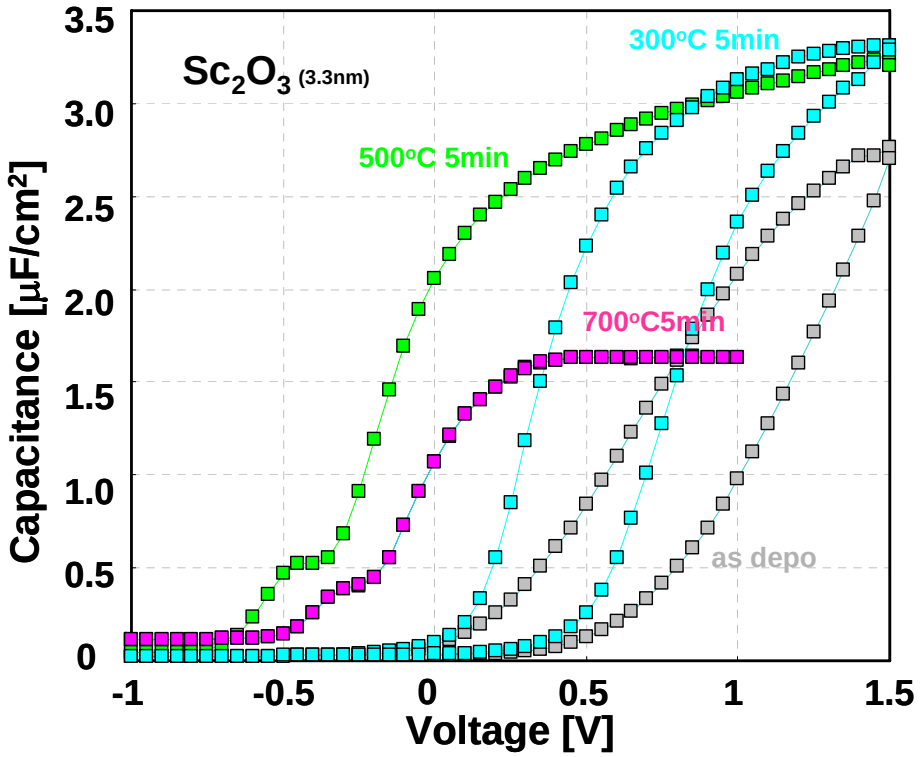


Figure3.28: C-V characteristics of Sc_2O_3 single-layer

3.3.3.4 La_2O_3/Sc_2O_3 stacked layer

Figure 3.29 shows the CV characteristics of La_2O_3/Sc_2O_3 stacked layer sample (measurement frequency was 100kHz) with PMAs in N_2 ambient at 300 ^oC, 500 ^oC, and 700 ^oC for 5 minutes, 900 ^oC and 1000 ^oC for 2 seconds. The accumulation capacitance decreased with increase of annealing temperature. However, the decreasing pace of capacitance from 500 ^oC to 900 ^oC was very slight. It was considered that the interfacial layer growth pace up to 900 ^oC annealing sample might become more slowly than La_2O_3 single-layer or Sc_2O_3 single-layer. The bump around the weak inversion region was observed with 500 ^oC, 700 ^oC, and 900 ^oC annealing samples. The flat band voltage of La_2O_3/Sc_2O_3 stacked layer was stable for 500 ^oC, up to 900 ^oC annealed sample. It considered that erase the negative charge which was occurred in La_2O_3 single-layer, and positive charge which was occurred in Sc_2O_3 single-layer.

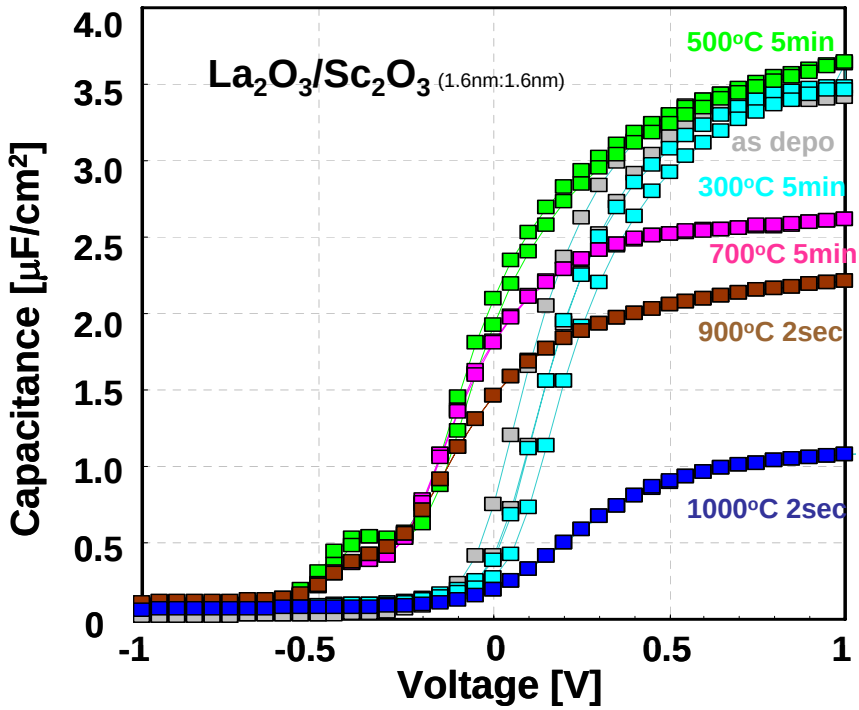
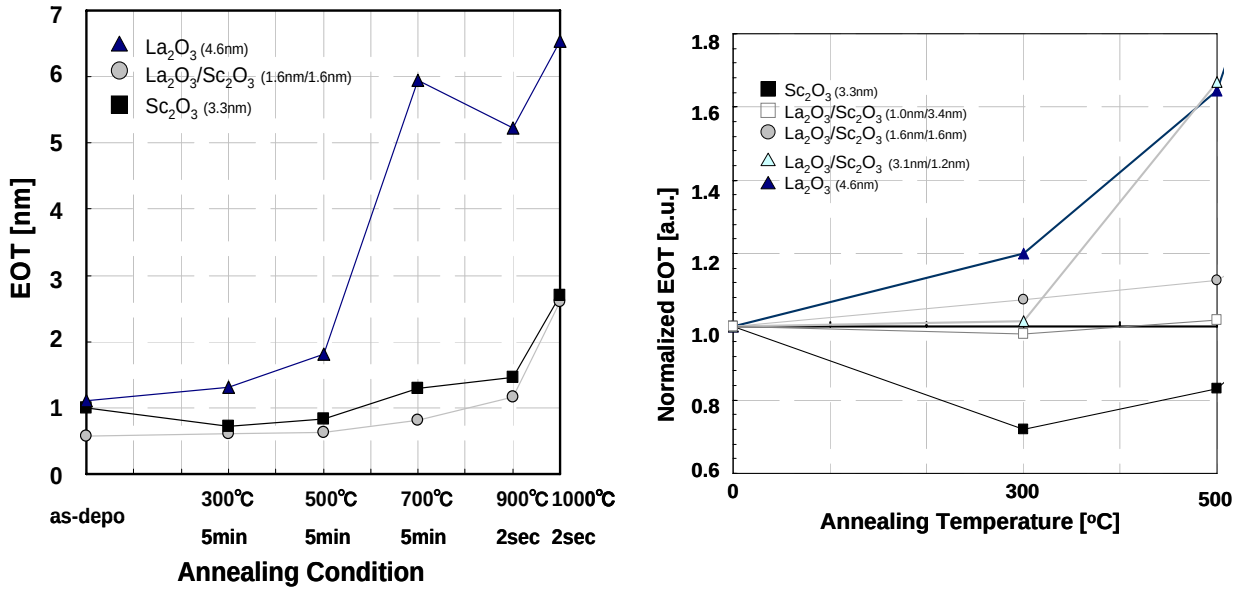


Figure3.29: C-V characteristics of La_2O_3/Sc_2O_3 stacked layer

3.5.3.5 The Comparison Between 5 Types Dielectric

Figure 3.30 shows the EOT change of La_2O_3/Sc_2O_3 stacked layer, La_2O_3 single-layer, and Sc_2O_3 single-layer capacitors after PMA at various temperatures. EOT with La_2O_3 single-layer capacitor drastically increase over 500 ^oC annealing was observed, which suggests the formation of low dielectric constant interfacial layer, such as silicate and SiO_2. On the other hand, Sc_2O_3 capacitor showed stable EOT up to 500 ^oC annealing and kept lower EOT growth compared to one of La_2O_3 capacitor. La_2O_3(1.6 nm) and Sc_2O_3(1.6 nm) stack film also showed stable EOT up to 500 ^oC and even at 700 ^oC the EOT was less than 1 nm. Sc_2O_3 single-layer and La_2O_3/Sc_2O_3 stacked layer have the effect which suppress the EOT up to 900 ^oC annealing.

For seeing the effect of Sc_2O_3 buffer layer clearly, it was evaluated normalized the EOT change with respect to the as deposited sample by changing the Sc_2O_3 thickness. Figure 3.30(b) shows the normalized the EOT change of La_2O_3/Sc_2O_3 stacked layer which are 3 types Sc_2O_3 thickness, La_2O_3 single-layer, and Sc_2O_3 single-layer capacitors with up to 500 ^oC annealing. As the thickness of Sc_2O_3 layer decreases, the EOT growth tends to follow the characteristics of La_2O_3 single layer. From this experiment, at least 1.6 nm of Sc_2O_3 is essential to prevent the EOT growth up to 500 ^oC. In the case of La_2O_3/Sc_2O_3 stacked layer which has more than 1.6nm Sc_2O_3 layer, the tendency of EOT is stable up to 500 ^oC annealing. Sc_2O_3 single-layer suppressed the increasing the EOT well.



(a) **(b)**

Figure3.30: the EOT change of La_2O_3/Sc_2O_3, La_2O_3, and Sc_2O_3 capacitors (a) 3types insulators (b) 5 types insulators

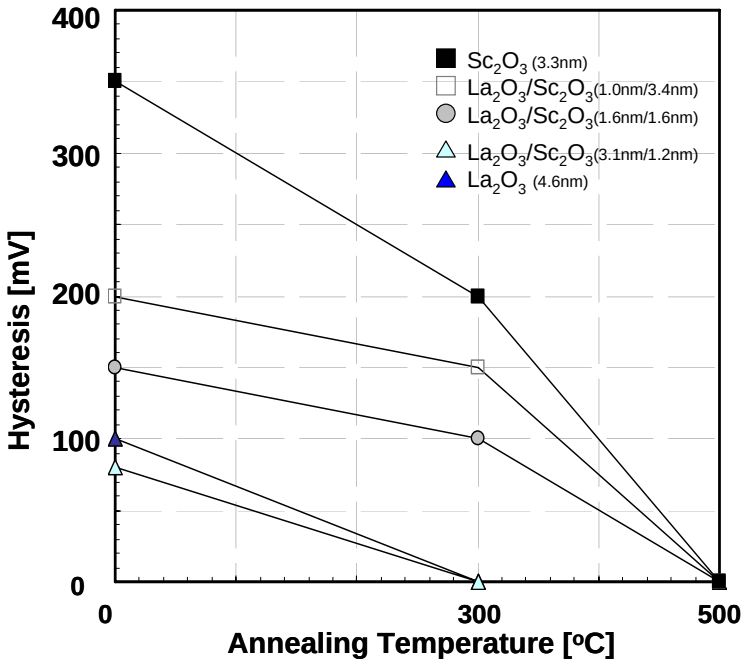


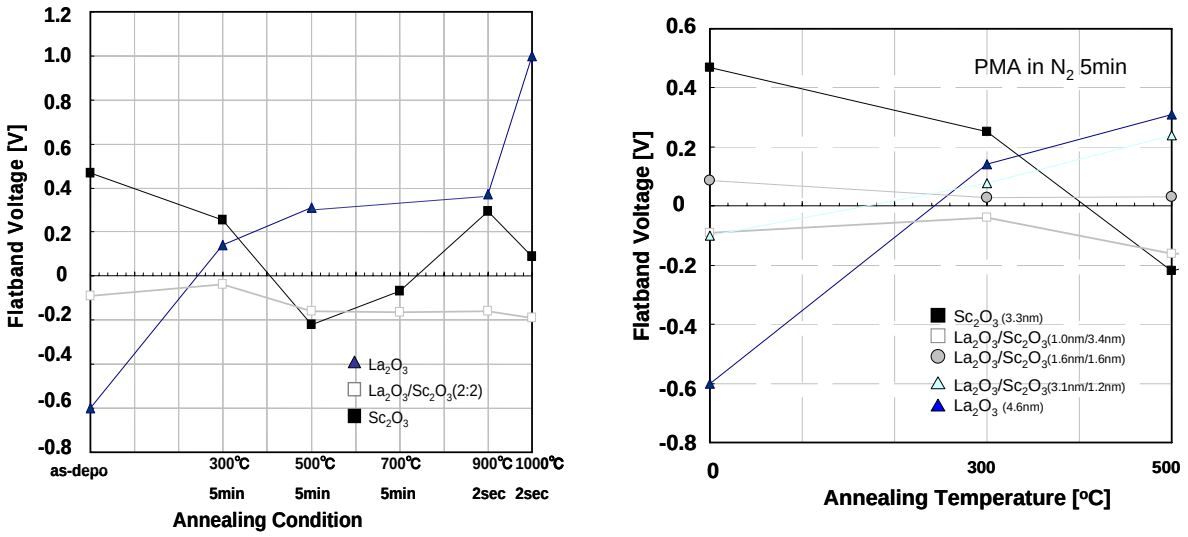
Figure3.31: **Hysteresis voltage change of La_2O_3/Sc_2O_3, La_2O_3, and Sc_2O_3**

Figure 3.31 shows the hysteresis voltage change of La_2O_3/Sc_2O_3 stacked layer, La_2O_3single-layer, and Sc_2O_3 single-layer capacitors on annealing temperature.

As scandium has strong affinity to oxygen, Sc_2O_3 at Si interface tend to have large hysteresis. This hysteresis can be reduced when Sc_2O_3 thickness is decreased. And high temperature annealing decreased the hysteresis, which suggests the reducing the defect of dielectric insulator. On the other hand, La_2O_3 showed small hysteresis, which disappeared at 300 ^oC PMA.

Figure 3.32 shows flatband voltage of La_2O_3/Sc_2O_3 stacked layer, La_2O_3 single-layer, and Sc_2O_3 single-layer capacitors on annealing temperature. The flatband voltage was obtained from the measured C-V characteristics, which is shown in Figure 3.11-3.11.

The flatband voltage of annealing temperature dependency was shown in Figure3.7. The flatband of La_2O_3 single-layer capacitor was shifted positive along with the annealing temperature, whereas Sc_2O_3 single-layer capacitor showed negative shift along with the annealing temperature. By inserting Sc_2O_3 at the interface, the flatband voltage was fixed as a result of charge compensation. From this experiment, at least 1.6 nm of Sc_2O_3 is required to prevent the flatband shift after annealing. In the case of La_2O_3/Sc_2O_3 stacked layer which has more than 1.6nm Sc_2O_3 layer, the tendency of flatband shift is also stable up to 500 ^oC annealing.



(a) (b)

Figure3.32: the hysteresis voltage change of La_2O_3/Sc_2O_3,La_2O_3, and Sc_2O_3 capacitors (a) up to 1000 °C (b) up to 500 °C

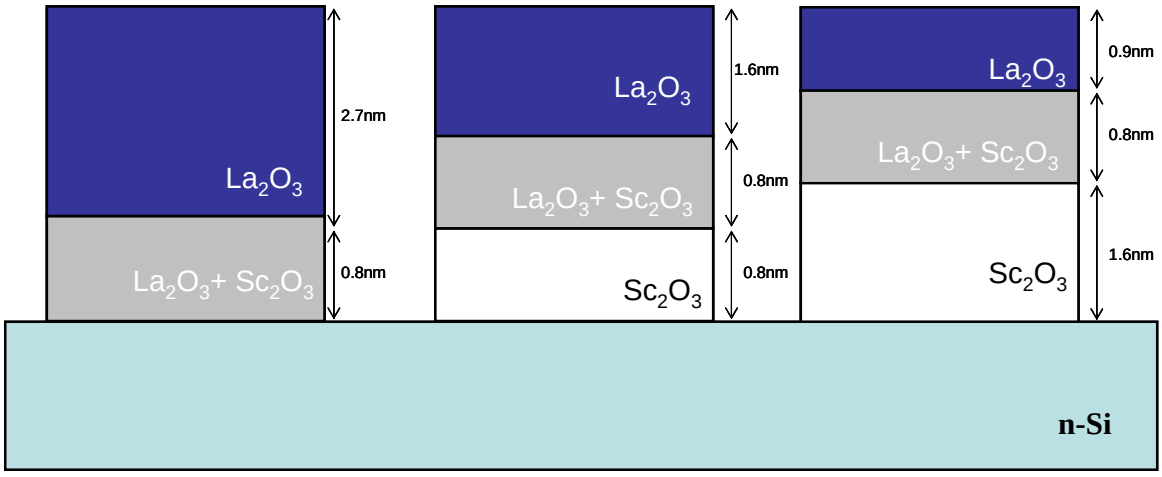


Figure3.33: Schematic of estimated insulator structure

Figure 3.33 shows the schematic of estimated La_2O_3/Sc_2O_3 stacked insulator structure. From rough estimation of each thickness with EOT and TEM observation, there exist a mixture layer of La_2O_3 and Sc_2O_3, even at as-deposited state, which is illustrated in figure 3.33. The dielectric constant of mixed layer was estimated as large as 16.

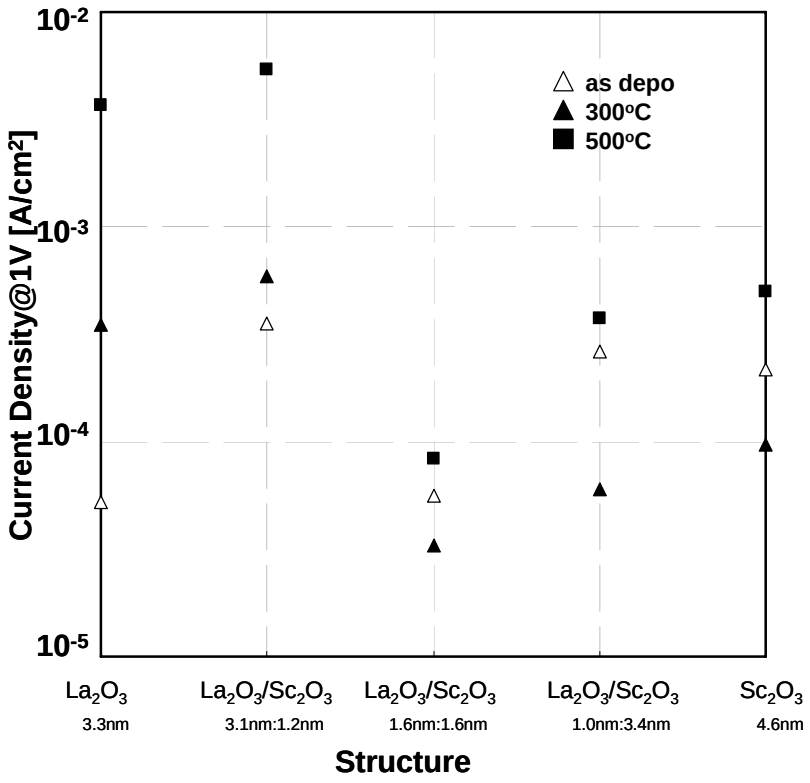


Figure3.34: Leakage Current Density of La_2O_3/Sc_2O_3, La_2O_3, and Sc_2O_3 capacitors

Figure 3.34 shows the leakage current change of La_2O_3/Sc_2O_3 stacked layer, La_2O_3 single-layer, and Sc_2O_3 single-layer on annealing temperature were monitored at gate voltage of 1 V. The lowest leakage current was obtained at as-deposited film with La_2O_3. When inserting 1.2 nm-thick-Sc_2O_3 followed the same tendency of La_2O_3 flim, while Sc_2O_3 more than 1.6 nm-thick insertion showed the lowest leakage current with 300 ^oC

PMA, which is the same characteristics of Sc_2O_3 capacitor. Here, in terms of thermal stability on capacitance, leakage current, hysteresis and flatband voltage shift, Sc_2O_3 insertion of 1.6 nm seems to be the optimum condition.

Figure 3.35 shows the interface state density of La_2O_3/Sc_2O_3 stacked, Sc_2O_3 single layer, and La_2O_3 single layer. La_2O_3/Sc_2O_3 stacked sample was kept the low interface state density even though 700 ^oC annealing. Sc_2O_3 single-layer of interface state density was higher than La_2O_3/Sc_2O_3 stacked sample, which is one of reason for not using Sc_2O_3 single-layer.

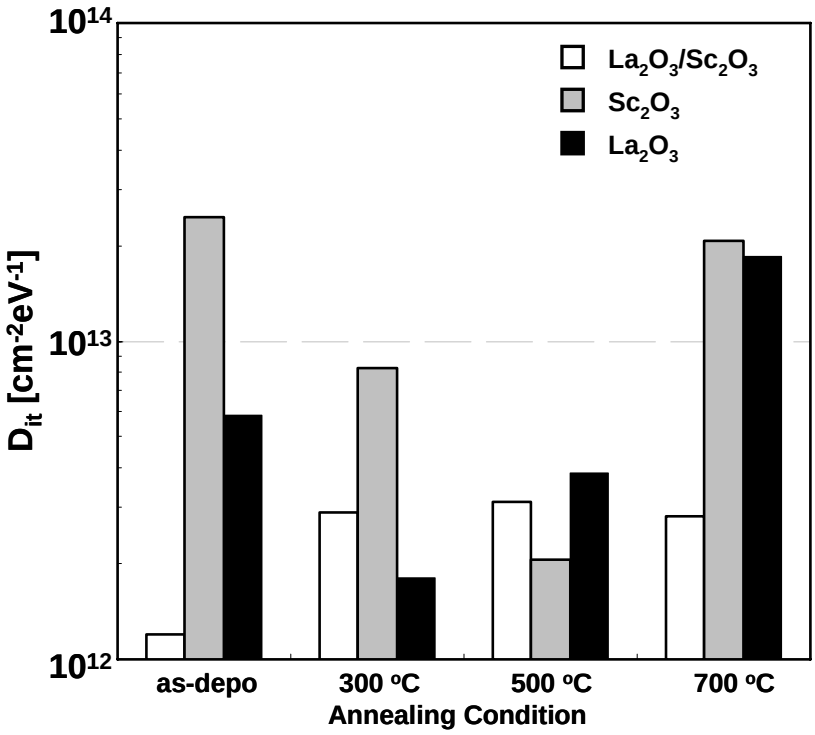


Figure3.35 Interface State Density of La_2O_3/Sc_2O_3, Sc_2O_3, and La_2O_3

3.3 Summary

The in-situ PMA process could suppress the EOT and leakage current for high temperature annealing. However, the slight bump around inversion region in CV curves which is not shown in PDA process. It caused that metal diffusion into gate insulator by W sputtering in in-situ process. And it induced high interfacial states density.[14]

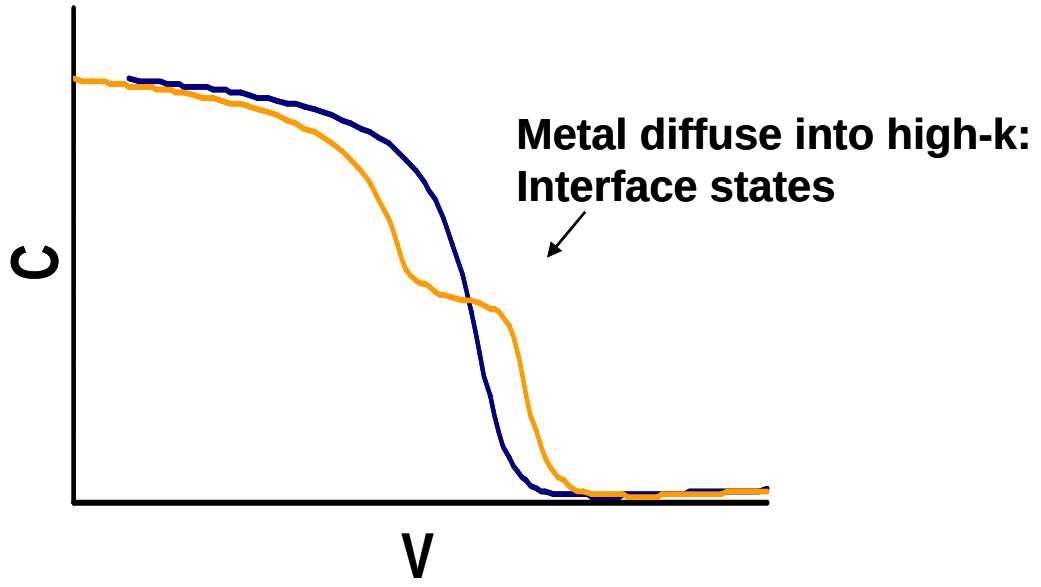


Figure3.36 Schematic of C-V curve with bump

Alternative W gate formation method such as evaporation or alternative material is required for erasing the slight bump around inversion region in CV curves reason from metal diffusion into gate insulator.

Chapter 4

Structural Analyses

4.1 Morphological Analyses

4.1.1 Introduction

The use of AFM method seems to be very perspective for investigation of surface changes after annealing of gate dielectric film – due to high sensitivity to relief change. The surface roughness contribute to the gate leakage currents or the mobility degradation. It is important to examine the surface morphology by AFM method. La_2O_3, Sc_2O_3 and La_2O_3/Sc_2O_3 stack films were deposited on silicon at 300 ^oC substrate temperature and annealed in N_2 at 300 ^oC-700 ^oC for 5minutes and 900 ^oC for 2seconds. AFM images and RMS (root-mean-square surface roughness) of after deposited and annealed samples were obtained.

4.1.2 Results and Discussion

Figure 4.1 shows the AFM images of La_2O_3 single film. The scanned area of the surface was 500×500 nm and the z direction was 5 nm/div. The RMS value in as-deposited sample was drastically improved after 300 ^oC annealing. The roughness which was observed in as-deposited sample is expected to be caused by the moisture absorption. High-temperature annealing samples tends to induce the increasing of RMS values.It considered that crystallization of La_2O_3 induced the increasing of the RMS values over 500 ^oC annealed samples.

Figure 4.2 shows the AFM images of Sc_2O_3 single film. The scanned area of the surface was 500×500 nm and the z direction was 5 nm/div.

For the Sc_2O_3 single film, the most high RMS value was observed in as-deposited sample. It is expected that there are strong relationship for Sc_2O_3 in as-deposited sample

having large hysteresis. It considered that crystallization of Sc_2O_3 induced the increasing of the RMS values at 700 ^oC annealed samples

Figure 4.3 shows the AFM images of La_2O_3/Sc_2O_3 film. The scanned area of the surface was 500×500 nm and the z direction was 5 nm/div . It seems to be totally flat for all the samples except for as-deposited film. Since the La_2O_3 surface absorbs moisture in the air, the roughness increased in as-deposited case. There are difference of lattice constant between La (a:3.937, c:6.130) and Sc (a:9.845). Since it considered that La_2O_3 layer and Sc_2O_3 layer mixing well after annealing, the RMS values of La_2O_3/ Sc_2O_3 stacked layer suppress up to 900^{o}C annealing.

Figure 4.4 shows the RMS values depend on the annealing temperature condition between La_2O_3 single layer, Sc_2O_3 single layer and La_2O_3/Sc_2O_3 stacked layer. The RMS values tendencies are similar. The RMS values of 300^{o}C annealing sample are smaller than the RMS values of as-deposited sample. It considered that densification of gate dielectric after annealing effect the roughness well. The RMS values of La_2O_3 single layer, Sc_2O_3 single layer and La_2O_3/ Sc_2O_3 stacked layer increased from 500 ^{o}C to 900 ^{o}C annealed samples. These tendencies are similar to the tendencies of dielectric thickness for La_2O_3 single layer, Sc_2O_3 single layer and La_2O_3/Sc_2O_3 stacked layer.

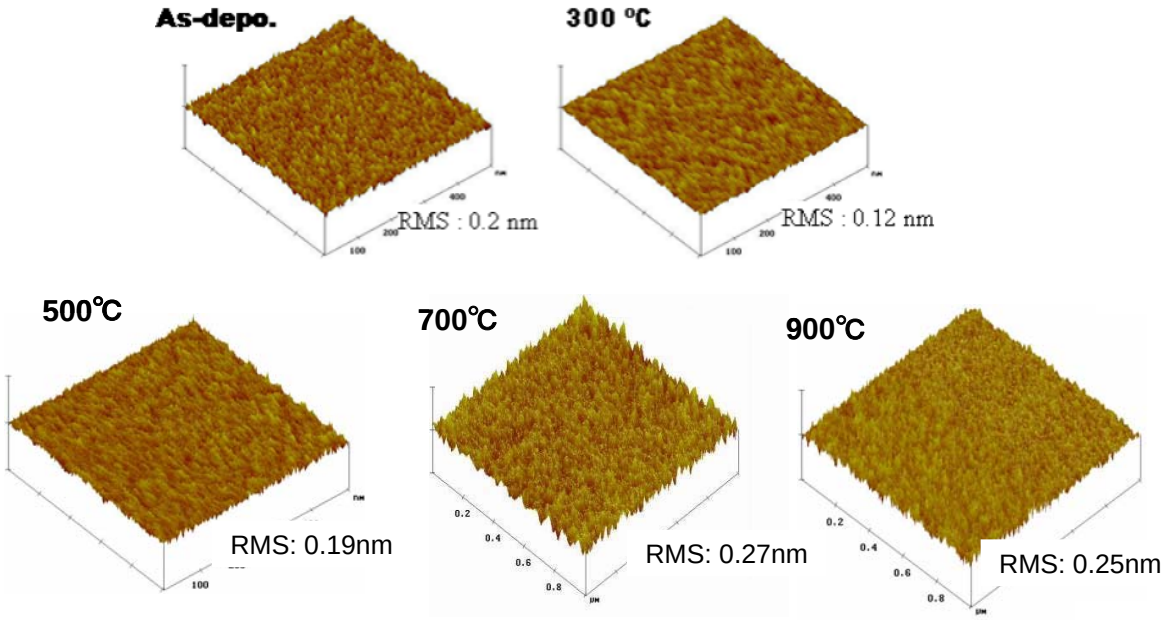


Figure 4.1. AFM images of La_2O_3 single film

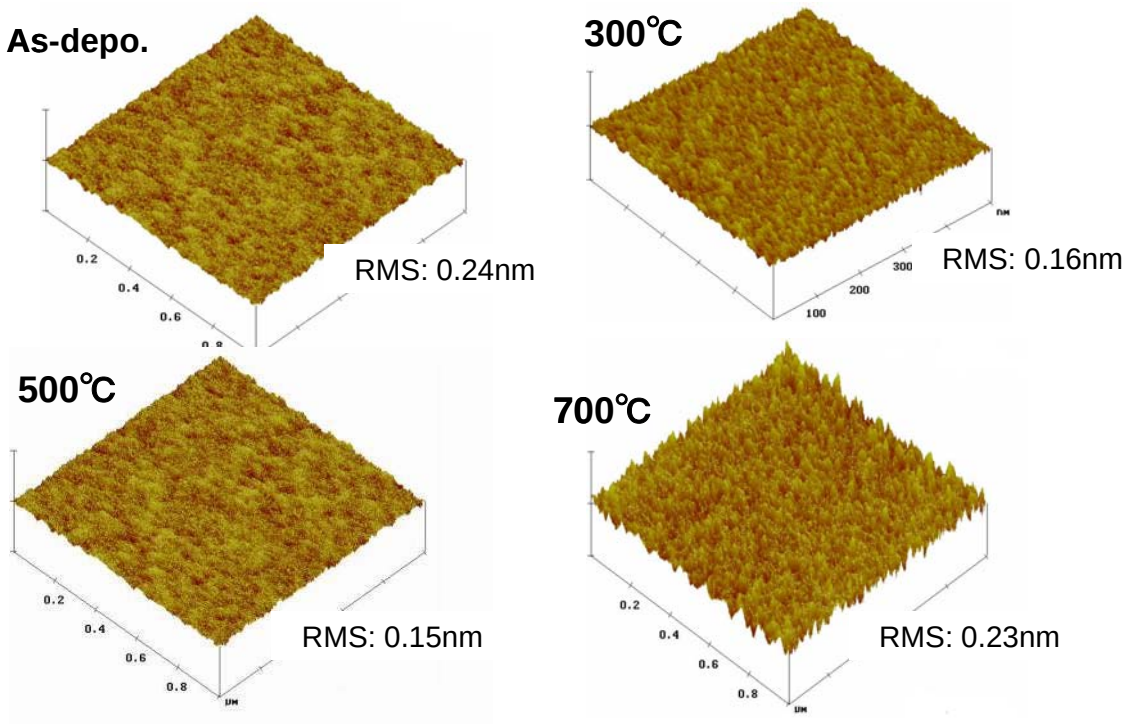


Figure 4.2. AFM images of Sc_2O_3 single film

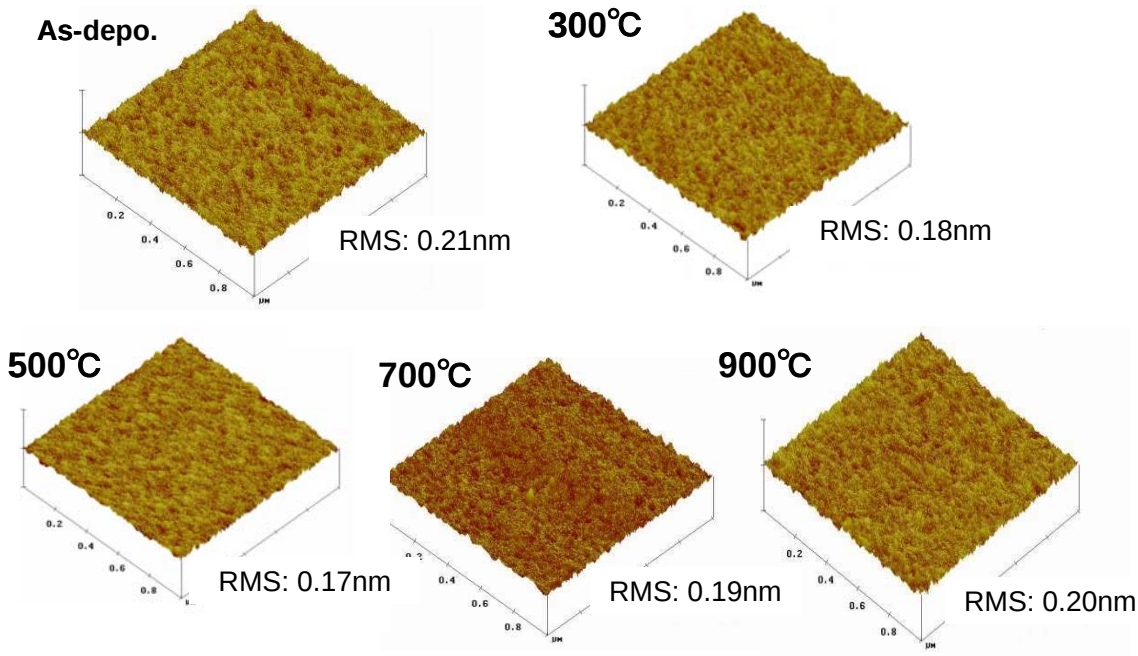


Figure 4.3. AFM images of La_2O_3/Sc_2O_3 single film

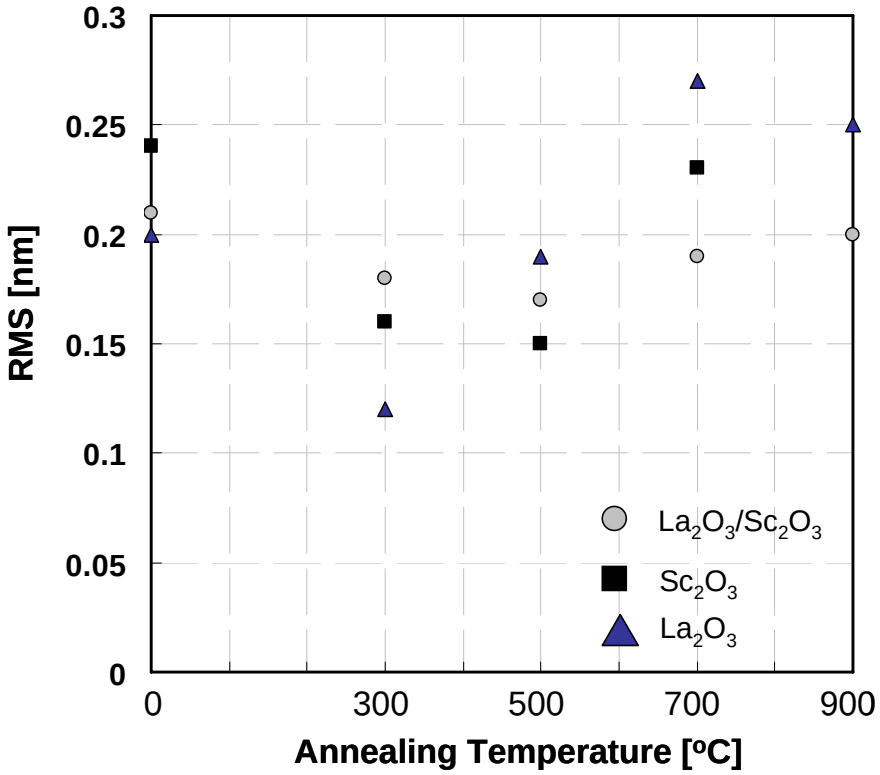


Figure 4.4. RMS values depend on annealing temperature

4.2 XPS analyses

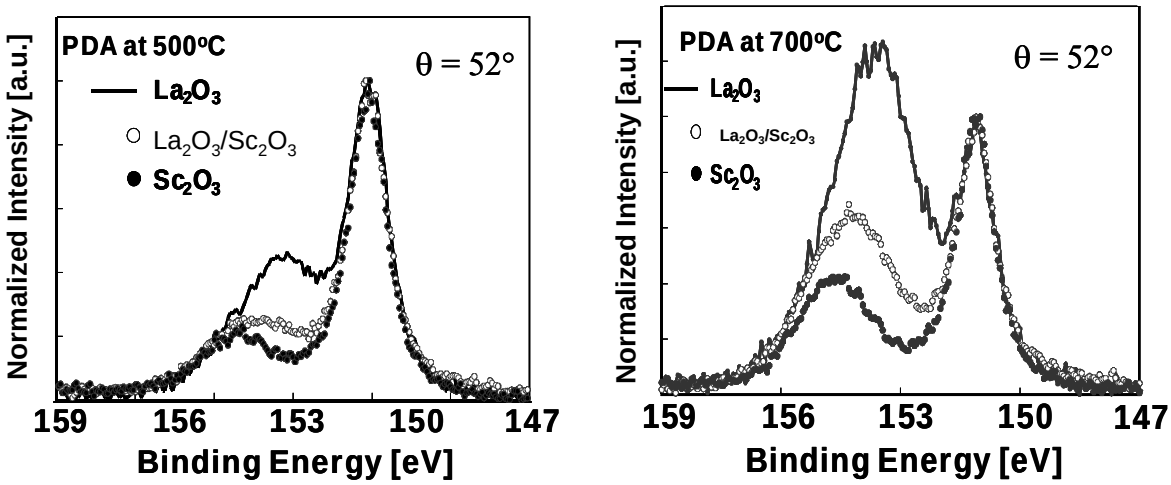
4.2.1 Introduction

XPS measurement is an electron spectroscopic technique for determining the elemental and chemical composition of materials' surface. The improvement of dielectric constant by Sc_2O_3 buffer layer was revealed from the viewpoint of the electrical characteristics in the previous section. One would expect the reason for improving the dielectric constant was the reduction of SiO_2 rich interfacial layer growth and limitation of La-Silicate by Sc_2O_3 buffer layer. In this section, consideration of the evidence of improving permittivity from the viewpoint of structural analyses by X-ray will be made. Analyses were made by Angle-Resolved X-ray Photoelectron Spectroscopy (AR-XPS). ESCA was used as a XPS equipment.

4.2.2 Results and Discussions

Figure 4.5 shows the Si2s spectra compared with La_2O_3 single layer sample, Sc_2O_3 single layer and La_2O_3/Sc_2O_3 stacked layer sample of (a) 500 ^oC and (b) 700 ^oC PDA for 5 minutes in N_2 ambient. Two peaks at approximately 151 eV and 154 eV were mainly observed for each dielectrics. The peak at 151 eV is corresponding to Si-Si peak and the peak at 154 eV is products of a reaction with silicon such as silicate and silicon oxides (SiO_x). All the peak intensities were normalized by Si-Si peak intensity. The silicate layer and silicon oxides (SiO_x) layer were decreased in this order of La_2O_3/Sc_2O_3 stacked layer, Sc_2O_3 single layer, La_2O_3 single layer. Especially, Si2s spectra for Sc_2O_3 and La_2O_3/Sc_2O_3 stacked film at 500 ^oC annealing were similar suggested these dielectrics have the same state with interface of Sc_2O_3/Si. There are

effect the suppressing the growth of significant amount of interfacial layer by using the Sc_2O_3 layer as buffer layer.



(a) PDA 500°C (b) PDA 700°C

Figure4.5. Comparison of Si2s spectra for La_2O_3, La_2O_3/Sc_2O_3 and Sc_2O_3

The composition of SiO_2 and the silicate in the interfacial layer should be separated to investigate the interfacial state in more detail. The component part of the interfacial layer in Si2s spectra was separated into SiO_2 and silicate using following equation.

$$Y = H\left(PG \cdot \exp\left(-(Ln2) \cdot \left(\frac{2(x-pp)}{FWHM} \right)^2 \right) \right) + \frac{1-PG}{1+\left(\frac{2(x-pp)}{FWHM} \right)^2}$$

where,

Y : Intensity of the spectrum H: peak height PG: Percent of Gaussian

x : binding energy value pp: peak position FWHM: Full Width Half Maximum

Figure4.6 shows Si2s spectra with separated components of SiO_2 and Silicate for (a) La_2O_3 single layer sample, (b) Sc_2O_3 single layer, (c) La_2O_3/Sc_2O_3 stacked layer sample and SiO_2 layer sample of 500 ^oC PDA for 5 minutes in N_2 ambient. The take off angle of photoelectrons was 60 ^{o} and intensities of spectra were normalized by bulk-Si peak. For La_2O_3 single layer sample, the significant increases of SiO_2 and the silicate were observed. For Sc_2O_3 single layer sample, there were no SiO_2 components. For La_2O_3/Sc_2O_3 stacked layer sample, the components of SiO_2 were very few, so it was considered to keep the dielectric constant.

Figure4.7 shows Si2s spectra with separated components of SiO_2 and Silicate for (a) La_2O_3 single layer sample, (b) Sc_2O_3 single layer, (c) La_2O_3/Sc_2O_3 stacked layer sample and SiO_2 layer sample of 700 ^oC PDA for 5 minutes in N_2 ambient. For La_2O_3 single-layer, both of SiO_2 and silicate peak are large after 700 ^oC annealing.

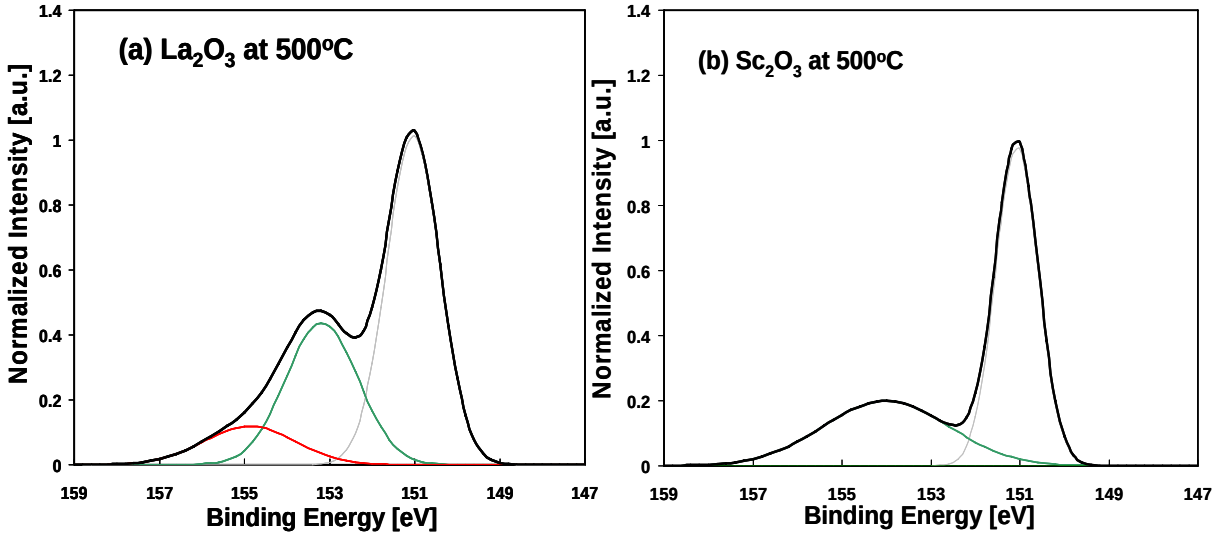


Figure4.6. Si2s spectra with separated components of SiO_2 and Silicate for (a)La_2O_3 500 °C, (b)Sc_2O_3 500 °C

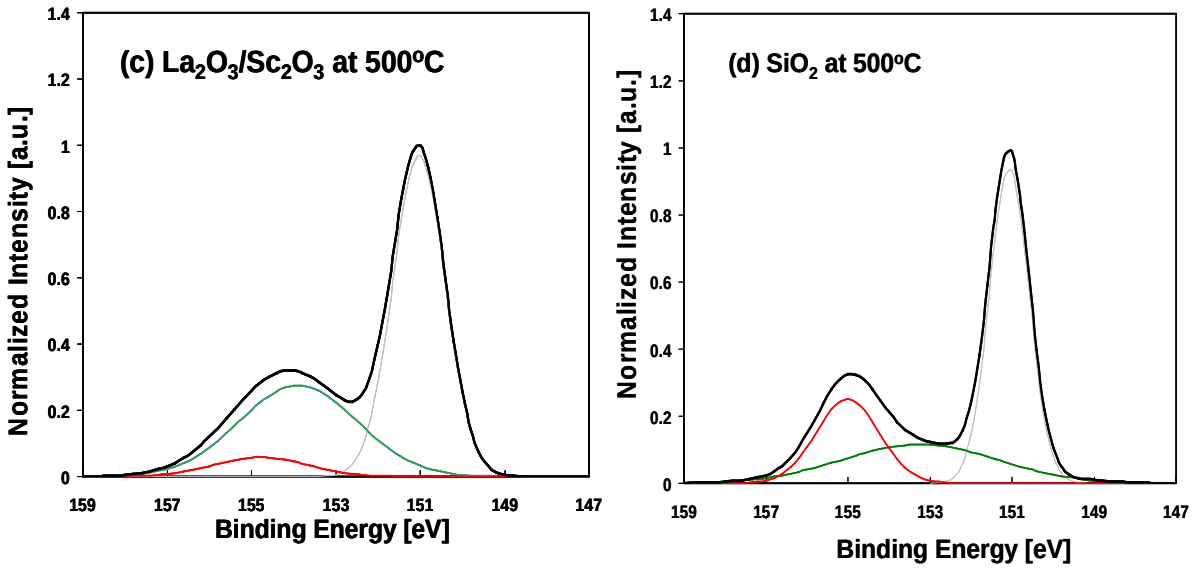


Figure4.6. Si2s spectra with separated components of SiO_2 and Silicate for (c)La_2O_3/ Sc_2O_3 500 °C, (d)SiO_2 500 °C

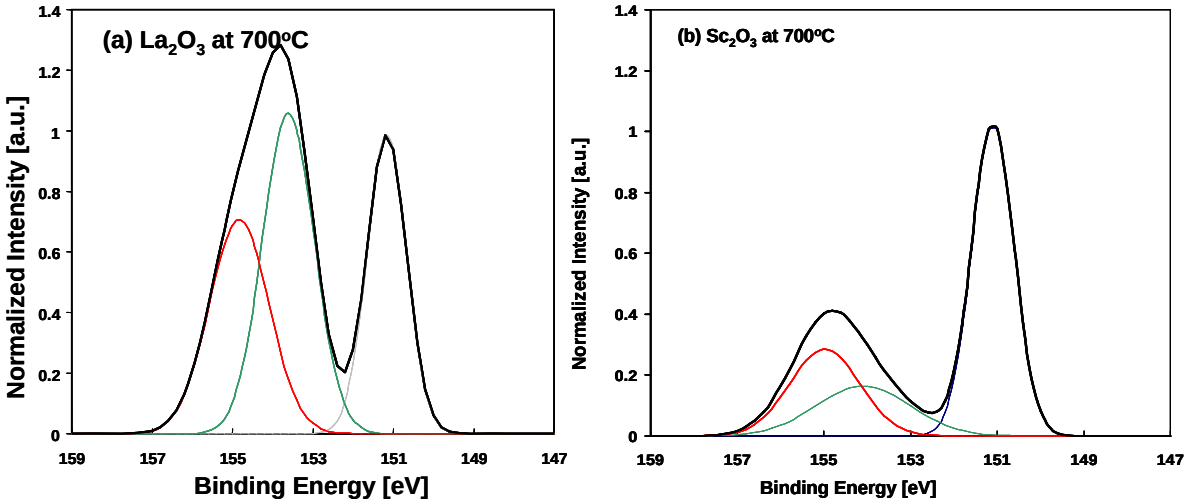


Figure4.7. Si2s spectra with separated components of SiO_2 and Silicate for (a)La_2O_3 700 °C, (b)Sc_2O_3 700 °C

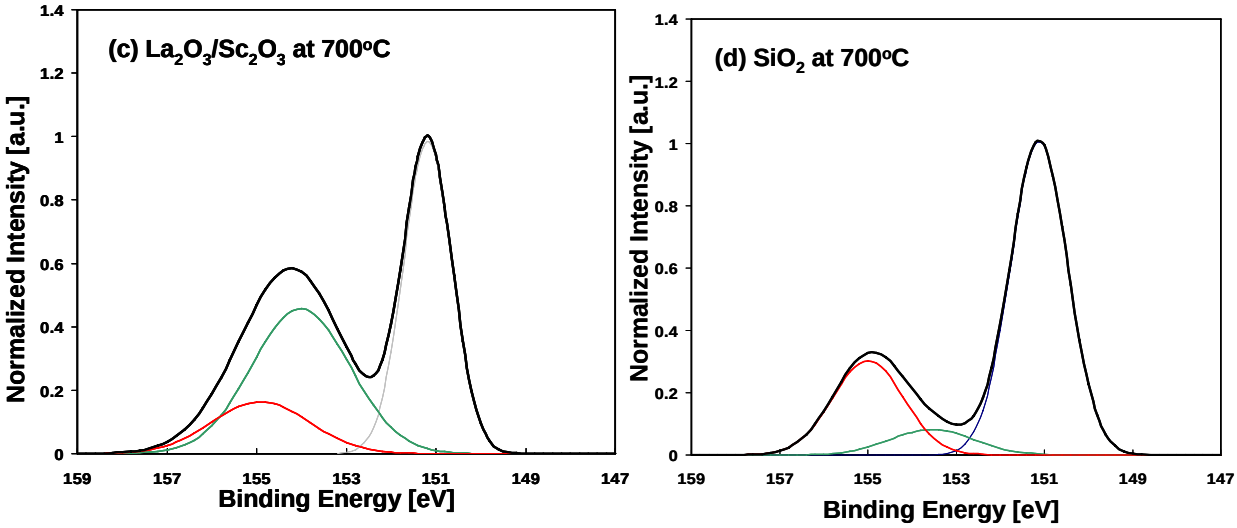


Figure4.7. Si2s spectra with separated components of SiO_2 and Silicate for (c)La_2O_3/ Sc_2O_3 500 °C, (d)SiO_2 500 °C

From Figure 4.6 and Figure 4.7 with components of SiO_2 and Silicate, the Silicate/bulk-Si and SiO_2/bulk-Si ratio were obtained for accurate comparisons of interfacial state.

Figure4.8 shows the SiO_2/bulk-Si ratio for each dielectric layers. For La_2O_3 single layer, the SiO_2 components were drastically increased after 700 °C annealing. Since La

has weaker affinity to oxygen than Sc, it was considered to induce the SiO_2 layer.

Figure4.9 shows the Silicate/bulk-Si count ratio for each dielectric layers. For La_2O_3 single layer, there were large amount of the Silicate component after 500 ^oC and 700 ^oC annealing. It was considered that La_2O_3 layer start to crystallization start 500 ^oC annealing. For Sc_2O_3 single layer with 700^oC annealing, the components of SiO_2 were not increased from 500 ^oC annealed sample. The La_2O_3 film was more likely to form a silicate than Sc_2O_3.

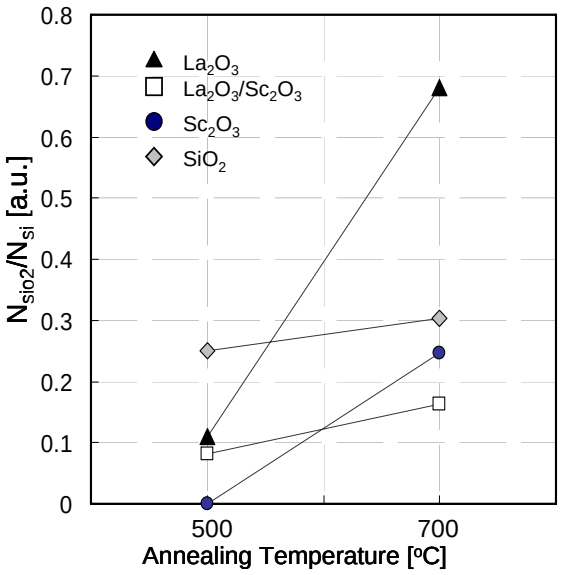


Figure4.8. the SiO_2/bulk-Si count ratio

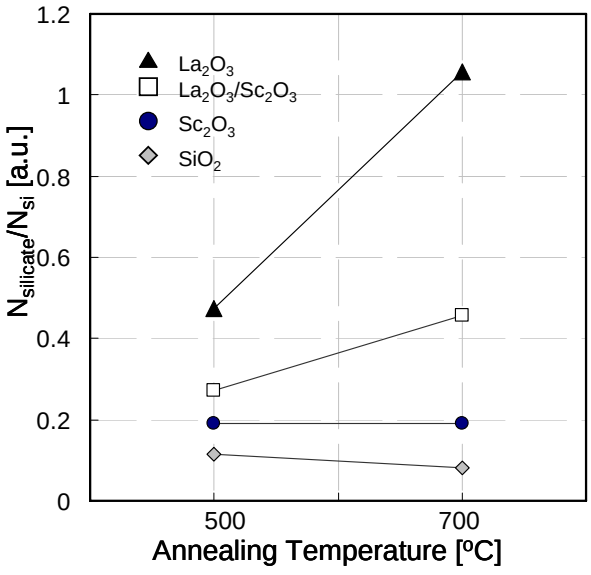


Figure4.9. the Silicate/bulk-Si count ratio

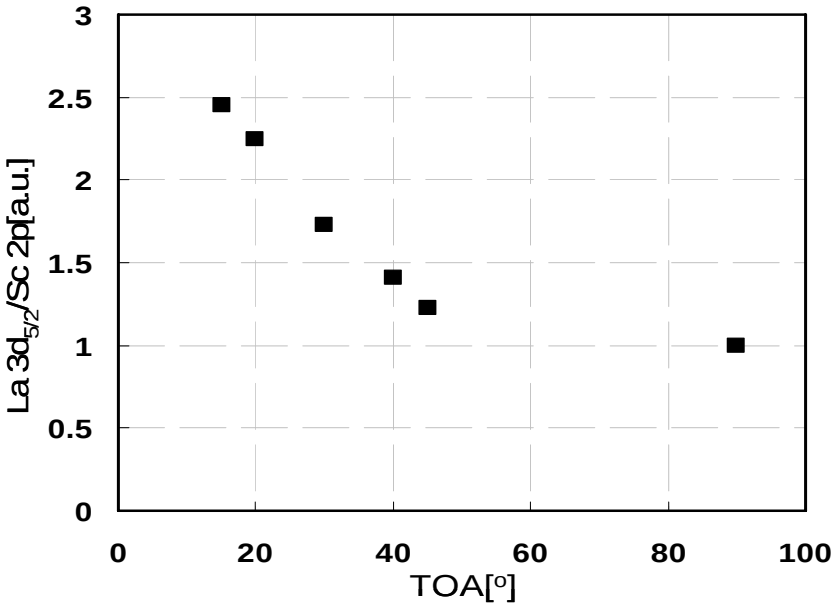


Figure4.10. comparison of signal intensity between La $3d_{5/2}$ /Sc 2p for La_2O_3/Sc_2O_3 stacked sample

Figure4.10 shows comparison of signal intensity between La $3d_{5/2}$ and Sc 2p for La_2O_3/Sc_2O_3 stacked sample with various take off angles of photoelectrons. Although La_2O_3/Sc_2O_3 stacked dielectric layer was deposited La_2O_3 and Sc_2O_3 separately, it shows La_2O_3 layer and Sc_2O_3 layer were mixed very well.

4.3 Conclusion

Morphological analyses on La_2O_3, Sc_2O_3 and La_2O_3/Sc_2O_3 stacked films in N_2 annealing were examined. The surface roughness of La_2O_3 single film were increased after 700 ^oC annealing. La_2O_3/Sc_2O_3 stacked films were found to suppress the increasing surface roughness after high temperature annealing.

Chemical compositions in La_2O_3, Sc_2O_3 and La_2O_3/Sc_2O_3 stacked films and the interfacial layer between silicon and dielectrics were analyzed using X-ray. The La_2O_3/Si interface was found to react with silicon substrate during high temperature treatment and grow SiO_2 and La-silicate layer. The La_2O_3/Sc_2O_3 stacked film suppressed the formation of interfacial layer such as, SiO_2 and La-silicate layer by effect of Sc_2O_3 buffer layer.

Chapter 5

Electrical Characteristics Of n-MOSFETs

5.1 W gated La_2O_3/Sc_2O_3 n-MOSFETs

In this section, we will report characteristics of La_2O_3/Sc_2O_3 stacked dielectrics transistor. Figure 5.1 (a) and (b) show I_d-V_d and I_d-V_g characteristics of La_2O_3/Sc_2O_3 stacked structure transistor, respectively. The gate length and the gate width of this transistor were 20um and 20um, respectively. In I_d-V_d characteristics, the applied gate voltage were from 0.60V to 1.0V with 0.1 V step. As this figure, we found that operation of stack structure transistor. Figure 4.1 (b) shows I_d-V_g characteristics at V_d =0.1V. S-factor and threshold voltage of this device were 90 mV/dec and 0.67 V.

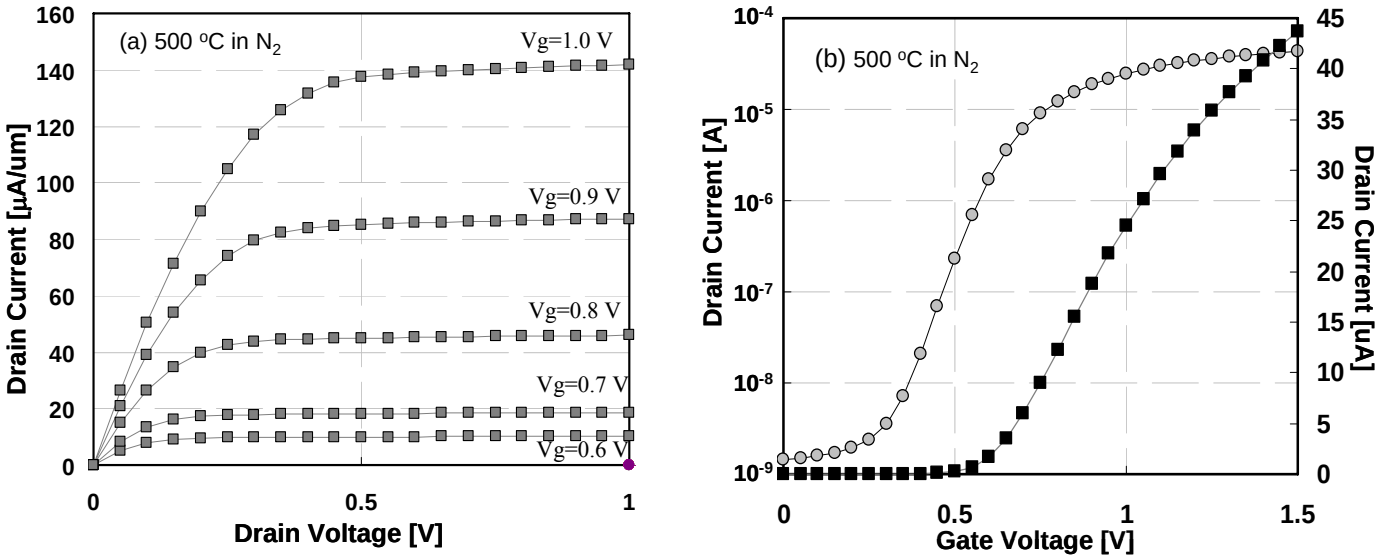


Figure 5.1 La_2O_3/Sc_2O_3 n-MOSFET of (a)I_d-V_d characteristics (b) I_d-V_g characteristics

Fig. 5.2 and 5.3 show the La_2O_3/Sc_2O_3 n-MOSFETs of of I_d-V_d I_d-V_g characteristics with 300 ^oC and 700 ^oC annealing, respectively.

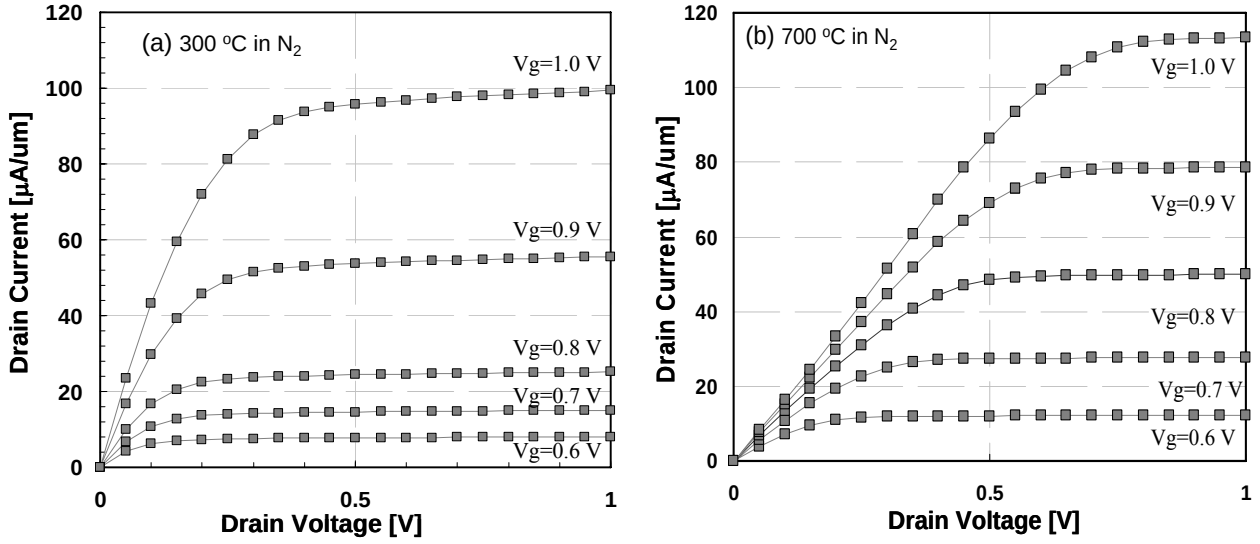


Figure 5.2 La_2O_3/Sc_2O_3 **n-MOSFET of** I_d-V_d **characteristics (a) 300^{o}C (b) 700^{o}C**

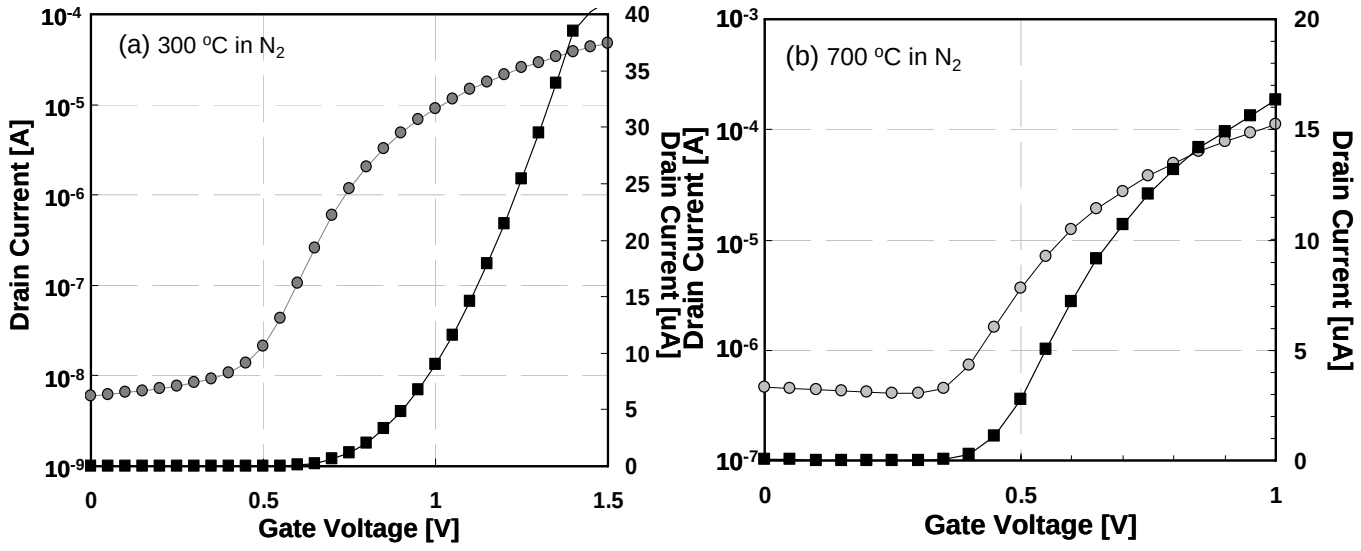


Figure 5.3 La_2O_3/Sc_2O_3 n-MOSFET of I_d-V_g characteristics (a) 300^{o}C (b) 700^{o}C

The effective mobility (μ_{eff}) was calculated by split CV method and μ_{eff} was plotted as a function of effective electric field (E_{eff}). Figure 5.4 shows that μ_{eff} vs. E_{eff} characteristics for La_2O_3/Sc_2O_3 MOSFETs with 500 ^oC and 700 ^oC annealing. The effective mobility was decreased after high temperature annealing. The peak mobility value of 121 cm^2/Vs with 500 ^oC 5 minuets annealing sample is not satisfactory high value. It was considered that there are a few possible reasons for the mobility degradation in this case. One is the influence of the damage induced by gate electrode W sputtering. Second is interface property between Sc_2O_3 and Si substrate. Third is influence at the La_2O_3/W gate electrode interface on the mobility, because of very thin EOT less than 1nm.

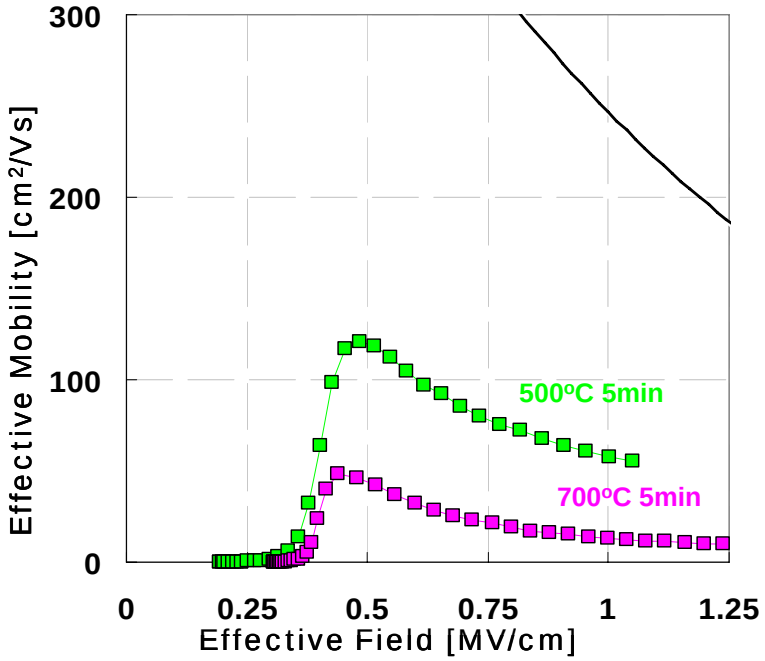


Figure 5.4 Effective Mobility of La_2O_3/Sc_2O_3 n-MOSFET

Chapter 6

Conclusions

6.1 Results of This Study

La_2O_3/Sc_2O_3 stacked dielectric was deposited by electron-beam evaporation method and the electrical characteristics of n-MOS capacitors and n-MOSFETs were evaluated with emphasis on the difference between La_2O_3 single-layer devices. And chemical compositions in the dielectric films were analyzed by X-ray photoelectron spectroscopy.

From the electrical properties of MOS capacitors, La_2O_3/Sc_2O_3 stacked dielectric was suppress the increasing the EOT at high temperature annealing by using Sc_2O_3 buffer layer.

From the XPS analyses, the La_2O_3/Si interface was found to react with silicon substrate during high temperature treatment and grow SiO_2 and La-silicate layer. The La_2O_3/Sc_2O_3 stacked film suppressed the formation of interfacial layer such as, SiO_2 and La-silicate layer by effect of Sc_2O_3 buffer layer.

La_2O_3/Sc_2O_3 stacked n-MOSFETs with EOT 0.80 nm was fabricated and evaluated successfully. It was found that degradation of the mobility after high temperature annealing.

6.2 For Future Works

La_2O_3 has been focused as the next generation of HfO_2 gate insulator application thanks to its high dielectric constant. Many attempts to reduce the EOT have been made for La_2O_3 film. However, the over 500 ^oC annealing for La_2O_3 film induced the more significant the gate leakage.

In this study, we obtained excellent results which are suppression of leakage current for gate dielectric thin films at high temperature annealing. Although, La_2O_3/Sc_2O_3 stacked structure of thermal endurance is still up to 900 ^oC for 2seconds. The etched gate process is required the thermal endurance of 1050 ^oC for 2 seconds for the semiconductor industry use. Since we considered $LaScO_3$ has thermal stability in our results, seeking the optimal condition to form the ternary structure of $LaScO_3$ dielectric layer by using $LaScO_3$ source, depositing La_2O_3 and Sc_2O_3 at once, or depositing La_2O_3 and Sc_2O_3 one after the other is required. Alternative W gate formation method such as evaporation or alternative material is required for erasing the slight bump around inversion region in CV curves reason from metal diffusion into gate insulator. And, for the application to the gate insulator of transistor, MISFETs which have larger EOT should be more investigate for high mobility transistors.

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