Study on RF Characteristics and Modeling of Scaled MOSFET

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Chapter 1

Introduction

1.1 RF CMOS Technology

With recent fast growth in the RF(Radio-Frequency) wireless communications market, the demand for high performance but low cost RF solutions is rising. And with the rapid growth of CMOS (Complementary Metal Oxide Semiconductor) technology due to its scaling, it comes to be considered as the mainstream of RF technology due to its low cost, low power and high integration. This advanced performance of CMOS is attractive for RF circuit design in view of a system-on-chip realization, where digital, mixed-signal baseband, and RF transceiver blocks would be integrated on a single chip. RF CMOS application is discussed in section 1.1.1.

However, with extreme scaling down of CMOS, several serious issues, e.g. short-channel and narrow width effects, impact ionization and gate leakage current, etc. have come out. Especially, gate leakage current is the most serious issue, because it makes difficult to realize Low Stand-by Power (LSTP) of CMOS devices. To improve this issue, high dielectric constant materials, so-called High-k, for gate oxide as replacement for conventional SiO_2 have attracted attention. High-k technology is discussed in section 1.1.2.

1.1.1 RF CMOS Applications

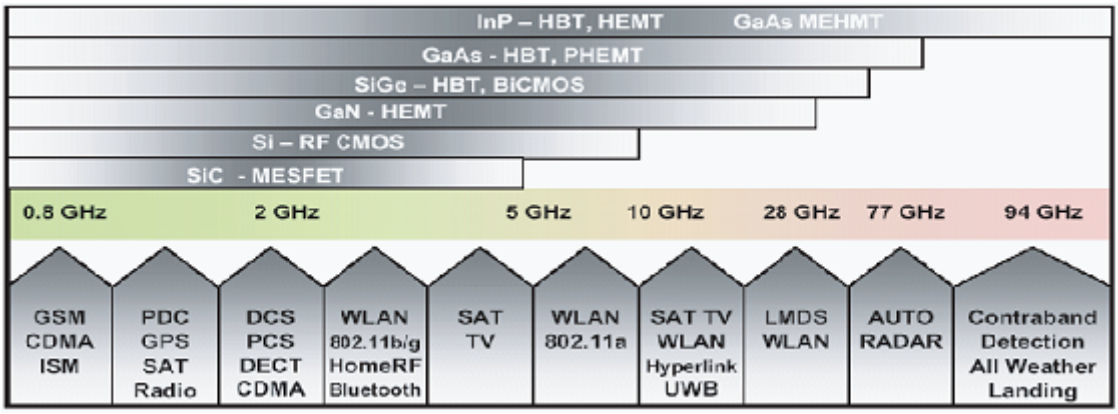


Figure 1.1 Application spectrum, ITRS2005

Recently, with the development of a highly-information-oriented society, the RF (Radio-Frequency) wireless communications market dramatically grows up. In the future, the demands of RF wireless technology will continue to increase all the more in various areas, e.g. our daily life, industrials and medicals. These demands are realized by the development of semiconductor products. Beforetime, the compound semiconductors composed of elements from group □ and □ in the periodic table such as SiGe, GaAs and InP had been mainly dominant for high-speed communications and RF applications as shown in Figure 1 [1]. However, RF CMOS application has been researched and developed by Universities in Europe and the United States cheifly [2][3], and then RF CMOS technology gets to be considered as the mainstream due to its low cost, low power, high integration and easy access to the technology, even though the compound semiconductors still dominate out of 5GHz as shown in Figure 1 [4]. Since RF characteristics, such as the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}), of Si ULSI come to advance up to several dozen GHz (see

Tabel 1), available bandwidth increases and the signal frequency transmitted to interconnection of LSI comes to over GHz. Thus, CMOS technology comes to be important for both the RF technology of wireless applications and digital LSI applications. The feature that CMOS circuit configuration and multi-layer interconnections are available for RF applications are also attractive. However, there are some challenges for RF CMOS applications in the following:

1. The necessity of optimization at semi-restricted process conditions.
2. The difficulty of adopting high resistive substrate.

The solution of these challenges is necessary for RF CMOS applications.

Table 1.1 The roadmap of RF CMOS characteristics [5]

Year	**1995**	**1997**	**1999**	**2001**	**2003**	**2005**	**2007**	**2009**
Gate length [nm]	**250**	**180**	**140**	**120**	**100**	**70**	**50**	**35**
Gate width [um]	**200**	**150**	**110**	**100**	**80**	**80**	**50**	**35**
f_T[GHz]	**39**	**50**	**65**	**80**	**105**	**145**	**205**	**420**
f_{max}[GHz]	**39**	**42**	**46**	**50**	**60**	**62**	**68**	**85**
NF_{min}@2GHz	**0.3**	**0.26**	**0.22**	**0.17**	**0.14**	**0.13**	**0.1**	**0.08**

1.2 The Indicators of RF Device

In evaluating device RF performance, some indicators are employed as the cut-off frequency f_T, the maximum oscillation frequency f_{max}, the minimum Noise Figure NF_{min} (and sometimes 1/f noise). In this section this three indicators are discussed especially.

1.2.1 The Cut-off Frequency f_T

f_T is defined as the transition frequency which small-signal current gain drops to unity. It is a measure of the maximum useful frequency of a transistor when it is used as an amplifier. f_T can be easily obtained by converting measured S21 parameter to H21 parameter.

$$f_T = \frac{g_m}{2\pi C_{gs}} \qquad (1.1)$$

1.2.2 The Maximum Oscillation Frequency f_{max}

f_T is surely a good indicator of the low-current forward transit time. However, as a performance indicator, it does not include the effects of gate resistance Rg, which are very important in determining the transient response of a transistor. So a indicator including Rg effects have been proposed, f_{max}. f_{max} is the frequency at which the unilateral power gain becoms unity.

$$UnilateralGain = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{K\left|\frac{S_{21}}{S_{12}} - \mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)\right|} \quad ; \text{K=Kfactor} \qquad (1.2)$$

$$f_{\max} = \frac{f_T}{2\sqrt{g_{ds}(Rg + Rs) + 2\pi f_T RgCgd}} \qquad (1.3)$$

1.2.3 The Noise Figure NF_{min}

The RF noise Figure is an important parameter. Due to the low effective gate resistance R_{gate} and the high f_T the minimum noise Figure is extremely small at frequencies of few GHz, and the measurements have to be accurately de-embedded and extended to get a proper picture.

Noise can be defined as any interference unrelated to the signal of interest. The most commonly accepted definition for NF is given by Eq. (1.4), where SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and output, respectively.

$$NF = \left.\frac{SNR_{in}}{SNR_{out}}\right|_{T=300K} \qquad (1.4)$$

NF is a measure of the degradation of the SNR as the signal passes through a system. For a noiseless circuit $SNR_{in} = SNR_{out}$. Therefore, regardless of the gain, NF equals to the unity. However in real systems the inner noise degrades the SNR, yielding NF>1. NF for circuits working in voltage-mode becomes

$$NF = \frac{V_{n,out}^2}{A_v^2 N_{RS}} \qquad (1.5)$$

For current-mode circuits NF becomes:

$$NF = \frac{I_{n,out}^2}{A_i^2 N_{RS}} \qquad (1.6)$$

Where $V_{n,out}^2$ =voltage of the total output-noise, $I_{n,out}^2$ = current of the total output-noise, Av= voltage gain, Ai= current gain, and NRS=noise of the resistance of a source.

Since noise performance is an important design factor regardless of the technology used, improving the noise Figure of a device is desirable.

1.3 Requirements of RF Characteristics

As a reference for the performance of the RF CMOS for circuit application, there are specific requirements. For many RF applications, such as PA drivers or wireless LAN PA's require power level over 20 dBm. Table 1.2 shows the requirements for wireless communication system.

Table 1.2 Requirement for wireless communication system

	PAN/LAN			Cellular Phone	
	Bluetooth	802.11b	802.11a/g	PDC	W-CDMA
Frequency(GHz)	2.4	2.4	5.2/2.4	0.8	2.1
Power Output(dBm)	0/20	20	20	29	24

1.4 High-k Gate Materials

As mentioned above, with its extreme scaling-down of CMOS devices, CMOS technology come to play an important role in digital and/or analog applications. However, MOS structure device has a rule, so-called *the scaling rules*, which make physical effects on device complex and difficult. Table 1.3 shows the scaling rules for various device parameters. In this table, scaling factor is $k>1$.

Table 1.3 Miniaturization with scaling factor of k[6]

Parameter	**Initital**	**Scaled**
channel length	L	L/k
channel width	W	W/k
total device area	A	A/k^2
gate oxide thickness	T_{ox}	T_{ox}/k
gate capacitance	C_{ox}	$C_{ox}\times k$
junction depth	X_j	X_j/k
power supply voltage	V_{dd}	V_{dd}/k
threshold voltage	V_{th}	V_{th}/k
substrate doping concentration	N_{SUB}	$N_{SUB}\times k$
S/D doping concentration	$N_{S/D}$	$N_{S/D}\times k$

As to gate oxide thickness T_{ox} which plays an important role in MOS structure device, with scaling aggressively, T_{ox} become too thin and the gate leakage current density will become increase as shown in Figure 1.2. This is the most serious issue in Si MOS device.

To control the gate leakage current, many materials as replacaement for SiO_2 which have a high dielectric constant, have been researched. Other keywords for High-k are its band gap, band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility and reliability. In this thesis, sub-100 nm RF CMOS with HfSiON high-k gate dielectrics will be evaluated.

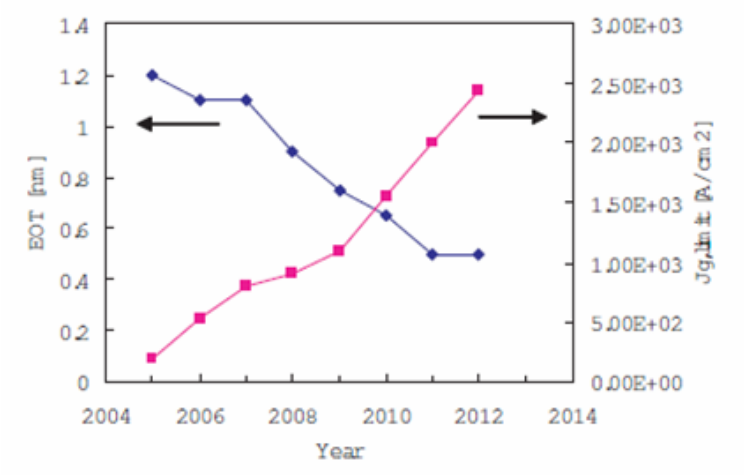


Figure 1.2 Prediction of equivalent oxide thickness and the maximum gate leakage current density variation[4]

1.4.1 Dielectric Dissipation

As important concern of high-k at RF region, dielectric dispersion is included. High-k may not keep the high dielectric constant at RF region, that is to say, high-k is not "high-k" at the region. Then, following mentions dielectric dispersion quoting from [7]. Frequency dependency of dielectric function is called dielectric dispersion generally. As for the dispersion where electronic polarization and ion polarization relate resonance type, or, oscillator dispersion is shown, but as for the dispersion where orientation polarization relates diapersion of relaxation type is shown as relaxation function of Debye type shows. Then, the dispersion of the microwave range which orientation polarization relates is especially called dielectric relaxation. The real part and imaginary part of dielectric function which respective polarization relates are shown in Figure 1.3 [8].

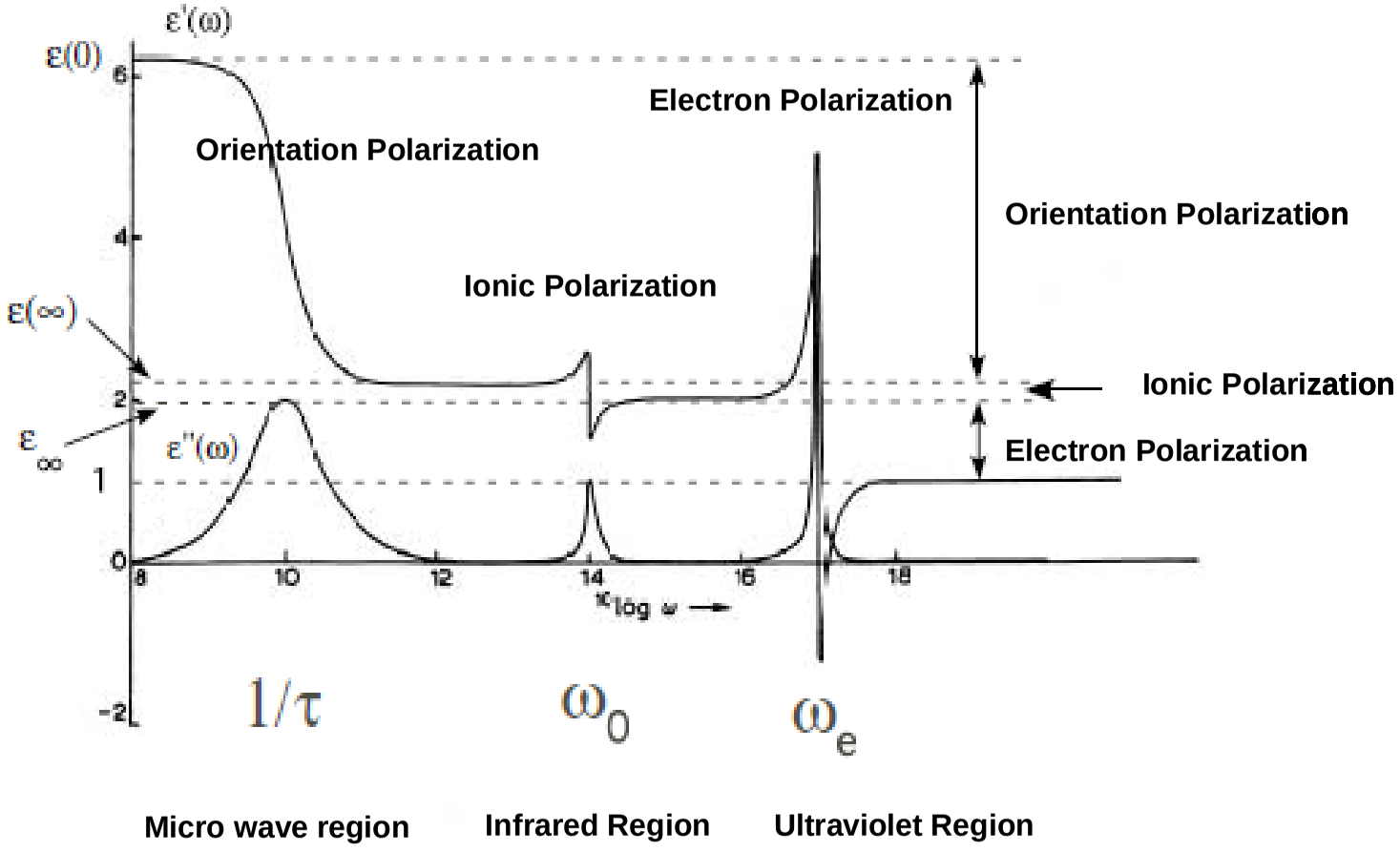


Figure 1.3 Dielectric dissipation [7],[8]

1.5 Purpose of This Study

In this thesis, device structure of next generation MOSFET including gate insulator and gate finger layout for maximizing the performance in RF circuit application is explored. Measuring S-parameter up to 40 GHz and Noise Fiugre of scaled MOSFET, we analyzed cut-off frequency f_T, maximum oscillation frequency f_{max} and minimum Noise Figure NF_{min} as indicators of RF performance based on extracted parameters by DC modeling and equivalent circuit.

In terms of solutions on the material of gate insulator, high-k material HfSiON is studied. High-k is now well researched and developed. However, report on RF application of high-k device is little until now. Although discussion about applying high-k to RF MOSFET is one of the purposes in this study, high-k MOSFET in RF region has some concerns. Those concerns are discussed about in Chapter 3.

Then, in terms of solutions on the structure which means the structure of gate finger on multi finger device for RF circuit, devices which have various finger length is studied. From the standpoints described above which are material of gate insulator and structure of gate finger, we explore the device solutions for RF circuit.

Chapter 2

Methodology of RF Measurement

2.1 S-parameter Measurement

Recently, with the rapid growth of RF (Radio-Frequency) wireless communications market, the requirements for RF applications increase. Therefore, at that stage of development, accurate RF measurement must be performed. It is well-known that accurate RF measurement on wafer is difficult due to parasitic components of system and device. Moreover, the effect of the surrounding parasitic components come to be bigger for device characteristics with continuous downscaling of the device dimensions. So two-step correction procedure has to be done as below:

1. Calibration
   - The measurement system has to be calibrated, defining a reference plane for the S-parameter measurements at the probe tips using a standard calibration technique (SOLT, LRM etc.).
2. De-embedding
   - The surrounding parasitic components on wafer have to be characterized, so that intrinsic S-parameters of transistor can be obtained from the measurement.

If calibration is performed exactly, S-parameters of inner reference plane can be obtained. Secondly, device parasitic components must be de-embedded which

methodology is discussed in the next section.

2.1.1 De-embedding

Resistance, capacitance or inductance included in the interconnect lines or bonding pads, which could neglect approximately in DC measurements (not completely neglect as for the interconnect lines resistance), largely influence to device RF performance. These parasitic components must be removed to evaluate intrinsic device characteristics at high frequency. De-embedding is the method of removing parasitic components.

For sub-micron transistors, the extraction is very sensitive to the input/output pads de-embedding. If the de-embedding is not complete, the correct values of the equivalent circuit components from direct extraction can not be obtained. Different de-embedding techniques have been developed based on different calibration test structures [9]-[12]. De-embedding procedure in this study is described as bellow. At first, Figure 2.1 shows OPEN and SHORT TEG (Test Element Group) for removing parasitic components of pad and interconnect lines.

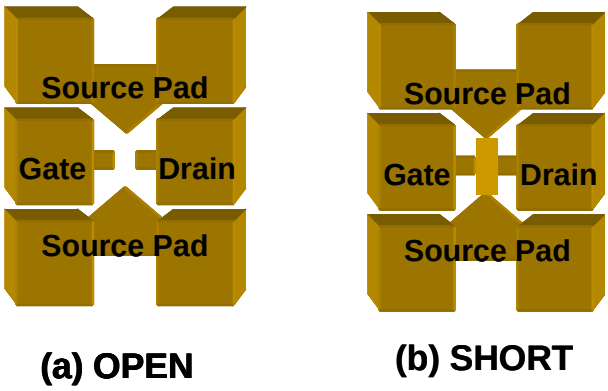


Figure 2.1 OPEN and SHORT TEG

As mentioned above, parasitic components are included in crude measured data. Then, parasitic capacitance of pads can be de-embedded by subtracting measured S-parameter of OPEN from crude measured S-parameter of DUT. Moreover, contact resistance can be de-embedded from measured S-parameter of SHORT. Finally, S-parameter of only device not including parasitic components can be gotten.

2.2 Noise Figure Measurement

Noise Figure measurement set up is shown in Figure 2.2.

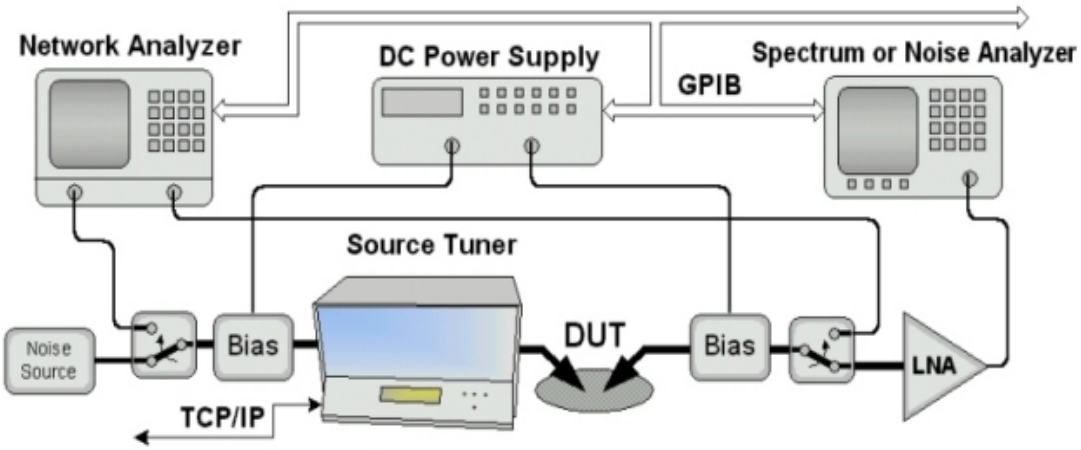


Figure 2.2 Noise Figure measurement set up

Noise measurements allow the determination of the four Noise Parameter of a device (transistor). For this concept four areas should be explained:

- Noise Parameters
- Noise Measurements
- Effect of second stage on noise behavior
- Noise Temperature

Noise Parameters:

These four numbers fully describe the noise behavior of an active or passive device (two port) at a given frequency. For practical reasons, following quantities are used as Noise Parameters:

- Minimum Noise Figure (NFmin): This is the small Noise Figure that the device can reach at a given frequency and bias, if it is optimally matched at the source.
- Equivalent Noise Resistance (Rn): This is a number in Ωdimension that indicates how fast the Noise Figure increases when the input (source) is mismatched.
- Optimum Noise Reflection Factor (Γopt): This is often used also as Optimum Admittance Yopt: Is the source admittance required for the DUT to perform NFmin (Yopt = Gopt+jBopt), 2 parameters.

The Noise Figure does not depend on the Load impedance presented to the device. It only depends on the source impedance.

There exists a simple relation between the four Noise Parameters:

Noise Figure $$NF(Y_S) = NF_{\min} + \frac{R_n}{G_S} \cdot \left| Y_S - Y_{opt} \right|^2 \qquad (2.1)$$

where Ys=Gs+jBs. This is the equation of a set of Circles on the Smith Chart (Noise

Circles) for which the value of the Noise Figure is the Level on each Circle.

This Circle Representation is only possible because the transistors Noise behavior is a Small Signal Phenomenon.

Measurement of the Noise Parameter:

The four Noise Parameters can be determined if the Noise Figure of a device are measured at a minimum of four different source impedances.

Because of errors associated with the extremely low-level noise measurements (the typical noise power of a transistor is about -110 dBm in 1 MHz bandwidth = the Noise Power is directly proportional to the Bandwidth).More than 4 impedances are in general measured and the measured data are averaged. 7 to10 impedances are typically sufficient for the determination of the noise parameters at each frequency.

The setup required to measure the Noise Parameter includes: - A Noise Analyzer or a Spectrum Analyzer- A Noise Source – A Programmable Tuner – A mixer and Local Oscillator (for f> 1.8 GHz) – Isolations, bias tees, etc.

Contrary to Load Pull measurements, it is not absolutely required that the Tuner used in Noise Measurements to be pre-calibrated. It can be set to a number of positions and readings that can be taken, both of the Noise Figures and the Tuner positions. If the tuner is then characterized at those positions using a Network Analyzer, the 4 Noise Parameters can be calculated. This is possible only because of Eq. (2.1). Of course, if the tuner is pre-calibrated, this facilitates a lot the operation and the result can be computed immediately. Again, a non pre-calibrate tuner well not permit to tune to the minimum Noise Figure; it will only permit to compute it.

2.3 Modeling of DC Model

Since BSIM3v3 (Berkley Short-channel IGFET Model 3 version 3) develped by UCB (University of California, Berkley) had been chosen for a standard compact model in 1995, this model have been widely used for digital and analog circuit design. A philosophy embedded in the BSIM3 model is to find a physically accurate functional form to describes a physical phenomenon and then use fitting parameters and even empirical terms to achieve quantitative match with the device characteristics. In this chapter, several models for DC parameter extraction such as thresholod voltage model and I-V models etc. in BSIM3v3 are described. In addition to this, extrinsic parameters extraction methodologies for a sub-circuit model are also described. With recent fast growth in the radio-frequency (RF) wireless communications market, the requirements for an accurate RF compact model rapidly increase.

2.3.1 Threshold Voltage Model

Accurate modeling of the threshold voltage (V_{th}) is one of the most important requirements for the precise description of a device electrical characteristics. By using the threshold voltage, the device operation can be divided into three operational regions. If the gate voltage is much larger than V_{th}, the MOSFETs is operating in the strong inversion region and the drift current is dominant. If the gate voltage is much less than V_{th}, the MOSFET operates in the weak inversion or subthreshold region and diffusion current is dominant. If the gate voltage is very close to V_{th}, the MOSFET operates in the transition region called moderate inversion where both diffusion and drift currents are important.

The complete V_{th} expression in BSIM3v3 is as following [17]:

$$V_{th} = VTH0 + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs}$$

$$+K1(\sqrt{1+\frac{NLX}{L_{eff}}} - 1)\sqrt{\phi_s} + (K3 + K3B \cdot V_{bs})\frac{TOX}{W'_{eff} + W0}\phi_s$$

$$-DVT0(\exp(-DVT1\frac{L_{eff}}{2l_t}) + 2\exp(-DVT1\frac{L_{eff}}{l_t}))(V_{bi} - \phi_s)$$

$$-(\exp(-DSUB\frac{L_{eff}}{2l_{t0}}) + 2\exp(-DSUB\frac{L_{eff}}{l_{t0}}))(ETA0 + ETABV_{bs})V_{ds}$$

$$-DVT0W(\exp(-DVT1W\frac{W'_{eff}L_{eff}}{2l_{tw}}) + 2\exp(-DVT1W\frac{W'_{eff}L_{eff}}{l_{tw}}))(V_{bi} - \phi_s) \quad (2.2)$$

In this equation, the second and third terms are used to model the verical non-uniform doping effect, the fourth term is for the lateral non-uniform doping effect, the fifth term is for the narrow width effect, the sixth and seventh terms are related to the short channel effect due to DIBL, and the last term is to descibe the small size effect in devices with both small channel length and small width. A simpler model for V_{th} would be preferred if it could offer the same adequate accuracy. In this work, since the fifth, sixth and last terms are not considered for DC parameter extraction, only considering terms will be introduced.

2.3.2 Essential Equation for I-V Characteristics

A DC MOSFET model is derived based on

$$J_n = q\mu_n nE + qD_n\nabla n \quad (2.3)$$

$$J_p = q\mu_p pE + qD_p\nabla n \quad (2.4)$$

J_n and J_p are the current dinsities for electrons and holes respectively, q is the electron charge, μ_n, μ_p are the mobility of electrons and holes respectively, n and p are the electorn and hole concentrations, E is the electric field and D_n and D_p are the diffusion coefficients of electrons and holes, respectively. D_n and D_p are linked to μ_n and μ_p with the following Einstein's relationship:

$$D_n = v_t \mu_n \qquad (2.5)$$

$$D_p = v_t \mu_p \qquad (2.6)$$

where v_t is the thermal voltage.

The terms of E in Eqs.(2.5),(2.6) represent the drift current components due to the electric field E. The second terms of Eqs.(2.5),(2.6) describe the diffusion current components due to the carrier cancentration gradient. In the strong inversion region, the current is dominated by the drift current. In the subthreshold region, the diffusion current component dominates. However, in the transition region (moderate inversion region) from subt-hreshold to s-trong inversion, both drift and diffusiion currents are important. As shown in Eqs.(2.5),(2.6), carrier density and the velocity-field relationship are two fundamental factors determining the I-V characteristics. We need to model the channel charge and mobility as well as the velocity-field relationship carefully to describe the current characteristics accurately and physically. We discuss the modeling of channel charge and mobility next before we introduce the modeling the I-V behavior

2.3.3 Channel Charge Density Model

For the weak inversion and the strong inversion regions, separate expressions for channel charge density have been given respectively:

$$Q_{inv} \approx \sqrt{\frac{q\epsilon_{si}N_a}{4\phi_B}} v_t \exp(\frac{V_{gs} - V_{th} - V_{OFF}}{nv_t}) \; in\ weak\ inversion \quad (2.7)$$

$$Q_{inv} = C_{ox}(V_{gs} - V_{th}) \quad in\ strong\ inversion \quad (2.8)$$

We can combine these expressions in the following form:

$$Q_{chs0} = C_{ox} V_{gsteff} \quad (2.9)$$

$$V_{gsteff} = \frac{2nv_t \ln[1 + \exp(\frac{V_{gs}-V_{th}}{2nv_t})]}{1 + 2nC_{ox}\sqrt{\frac{2\phi_s}{q\epsilon_{si}N_{CH}}} \exp(-\frac{V_{gs}-V_{th}-2V_{OFF}}{2nv_t})} \quad (2.10)$$

As shown in Figure 2.3 and 2.4, V_{gsteff} becomes V_{gs}-V_{th} in the strong inversion region, and follows $\sqrt{\frac{q\varepsilon_{Si}N_{CH}}{4\phi_B}} \frac{v_t}{C_{ox}} \exp(\frac{V_{gs} - V_{th} - V_{OFF}}{nv_t})$ in the subthreshold region.

The form of Eq.(2.10) was chosen to obtain a continuous equation for the channel charge and to match the measured Q_{chs}-V_{gs} characteristics in the moderate inversion (transition) region. The channel charge expression, Q_{chs0}, will be used in subsequent sections of this chapter to model the drain current. Furthermore, the model accurately predicts the charge in the transition (moderate inversion) region. The continuous and accurate nature of the model makes it very attractive and promising in circuit simulation since the moderate inversion region is becoming more important for low voltage/power circuit application.

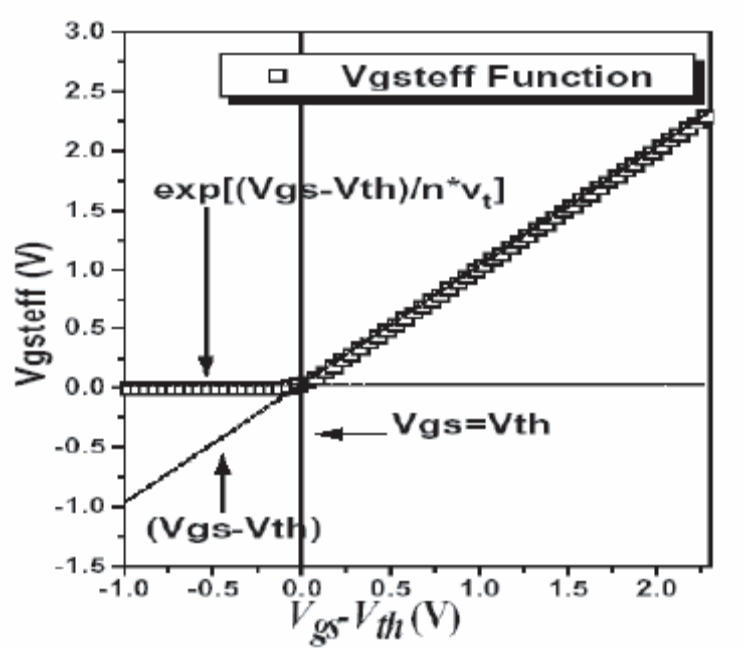


Figure 2.3 V_{gsteff} vs. V_{gs}-V_{th} in a linear plt [18].

2.3.4 Mobility Model

A good model for the carrier surface mobility is critical to the accuracy of a MOSFET model. The scattering mechanisims responsible for the surface mobility include phonons, coulombic scattering, and surface roughness scattering. For good quality interfaces, phonon scattering is the dominant scattering mechanism at room temperature. In general, mobility depends on many process parameters and bias conditions. For example, mobility depends on the gate oxide thickness, doping concentration, threshold voltage, gate voltage and substate voltage, etc.

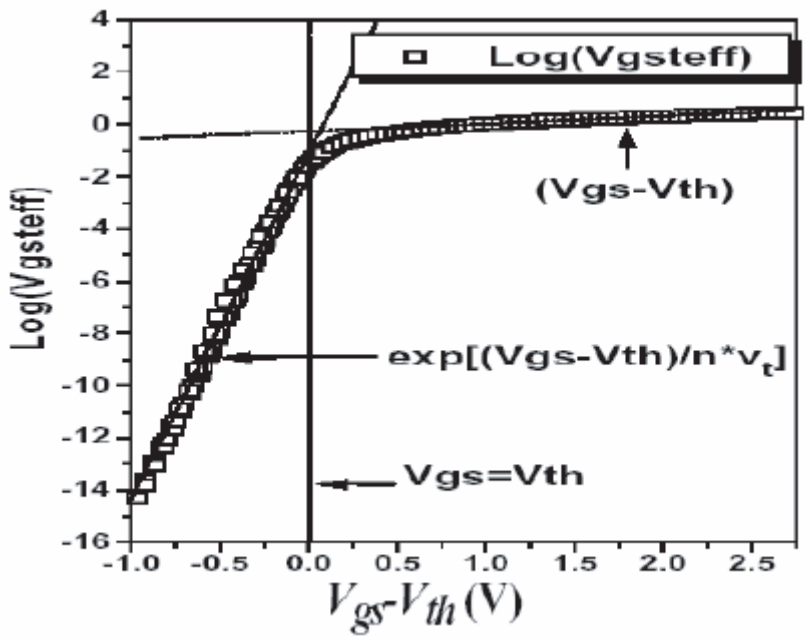


Figure 2.4 V_{gsteff} vs. V_{gs}-V_{th} in a semi-logarithmic plot [18]**.**

The continuity of mobility model is also required to ensure the continuity of the I-V model. To achieve continuity in the mobility model, BSIM3v3 uses a unified mobility expression based on the V_{gsteff} expression of Eq.(2.10),

$$\mu_{eff} = \frac{\mu_0}{1 + (U_A + U_C V_{bseff})(\frac{V_{gsteff}+2V_{th}}{T_{OX}}) + U_B(\frac{V_{gsteff}+2V_{th}}{T_{ox}})^2} \quad (2.11)$$

where

$$V_{bseff} = V_{bc} + 0.5\left[V_{bs} - V_{bc} - \delta_1 + \sqrt{(V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 V_{bc}}\right] \quad (2.12)$$

It can be seen that Eq.(2.11) follows Eq.(2.12) in strong inversion, and becomes a constant in the subthreshold region. Several mobility model options are provided for users to choose in BSIM3v3. a selector parameter called *mobMod* is introduced for this purpose. The mobility expression in Eq.(2.11) has been designated as *mobMod*=1. The following empirical mobility model option (*mobMod*=2) is better suited for depletion mode devices:

$$\mu_{eff} = \frac{\mu_0}{1 + (U_A + U_C V_{bseff})(\frac{V_{gsteff}}{T_{OX}}) + U_B(\frac{V_{gsteff}}{T_{ox}})^2} \quad (2.13)$$

BSIM3v3 also introduced a third mobility model option (*mobMod*=3):

$$\mu_{eff} = \frac{\mu_0}{1 + [U_A(\frac{V_{gsteff+2V_{th}}}{T_{ox}}) + U_B(\frac{V_{gsteff}}{T_{ox}})^2](1 + U_C V_{bseff})} \quad (2.14)$$

It is clear that all of the mobility models given above approach constant values that are independent of V_g when $V_{gs_i}V_{th}$. It should be pointed out that all of the mobility models given above account for only the influence of the vertical electrical field. The influence of the lateral electrical field on the mobility will be considered when discussing the velocity saturation effect in the next section.

2.3.5 I-V Model in the Strong Inversion Region

2.3.5.1 I-V Model in the linear (triode) Region

1. Intrinsic case (Rds=0)

In the strong inversion region, the current equation at any point y along the channel is

$$I_{ds} = W_{eff} C_{ox} (V_{gst} - A_{bulk} V_{(y)}) v(y) \quad (2.15)$$

where $V_{gs'}=(V_{gs}-V_{th})$, W_{eff} is effective device channel width. C_{ox} is the gate capacitance per unit area. V(y) is the potential difference between the channel and the source. A_{bulk} is the codfficient accounting for the bulk charge effect and v(y) is the velocity of carriers. BSIM3 I-V formulaition starts with a simple piece-wise saturation velocity model,

$$v(y) = \mu E_y \qquad E_y < E_{sat} \quad (2.16)$$

$$v(y) = v_{sat} \qquad E_y > E_{sat} \quad (2.17)$$

where E_y is the magnitude of the lateral electric field and E_{sat} is the critical electric field at which the carrier velocity becomes satureted. μis the mobility including the influence of the lateral electric field E_y and is given by

$$\mu = \frac{\mu_{eff}}{1 + (E_y / E_{sat})} \quad (2.18)$$

In order to have a continuous velocity model at $E_y=E_{sat}$, E_{sat} satisfies

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}} \qquad (2.19)$$

Thus, before the electric field reaches E_{sat} the drain current can be expressed

$$I_{ds} = W_{eff}C_{ox}(V_{gs} - V_{th} - A_{bulk}V_{(y)})\frac{\mu_{eff}E_y}{1 + E_y/E_{sat}} \qquad (2.20)$$

Eq.(2.20) canbe written as

$$E_y = \frac{I_{ds}}{\mu_{eff}W_{eff}C_{ox}(V_{gst} - A_{bulk}V_{(y)}) - I_{ds}/E_{sat}} = \frac{dV_{(y)}}{dy} \qquad (2.21)$$

By integratin Eq.(2.21) from y=0 to y=L_{eff}, the effective channel length, and V(y)=0 to V(y)=V_{ds}, we arrive at

$$I_{ds} = \mu_{eff}C_{ox}\frac{W_{eff}}{L_{eff}}\frac{1}{1 + V_{ds}/E_{sat}L_{eff}}(V_{gs} - V_{th} - A_{bulk}V_{ds}/2)V_{ds} \qquad (2.22)$$

The drain current model in Eq. (2.22) is valid before the carrier velocity saturates, that is, in the linear of the triode region.

2. Extrinsic case (Rds>0)

The parasitic source/drain resistance is an important device parameter which can affect MOSFET performance significantly in short channel devices. The most straightforward and accurate way of modeling the parasitic resistance effect is to use a circuit with

resistors in series with the intrinsic MOSFET. This leads to a complicated drain current expression. In order to make the model efficient, the drain current in the linear region can be modeled by extending Eq.(2.22).

$$I_{ds} = \frac{I_{ds0}}{1 + R_{ds} I_{ds0} / V_{ds}} \qquad (2.23)$$

where I_{ds0} is the intrinsic current expression given by Eq.(2.22). R_{ds} is a variable to account for the influence of the parasitic resistances at the source and drain.

2.3.5.2 Drain Voltage at Current Saturation, Vsat

1. Intrinsic case (Rds=0)

If the drain voltage (and hence the lateral electric field) is sufficiently high, the carrier velocity near the drain saturates. The channel may be divided into two portions: one adjacent to the source where the carrier velocity is field-dependent and the others adjacent to the drain where the velocity has satureted. At the boudary between the two portions, the channel voltage is the saturation voltage (V_{dsat}) and the lateral delctric field is equal to E_{sat}. We can substitute $v=v_{sat}$ and $V_{ds}=V_{dsat}$ into Eq.(2.15) to obtain the saturation current:

$$I_{dsat} = W_{eff} C_{ox} (V_{gst} - A_{bulk} V_{dsat}) v_{sat} \qquad (2.24)$$

By equating Eq.(2.15) and (2.24) at $V_{ds}=V_{dsat}$, we can solve for the saturation voltage

V_{dsat}:

$$V_{dsat} = \frac{E_{sat}L_{eff}(V_{gs} - V_{th})}{A_{bulk}E_{sat}L_{eff} + (V_{gs} - V_{th})} \qquad (2.25)$$

2. Extrinsic case (Rds>0)

Due to the parasitic resistance, the saturation voltage V_{dsat} will be larger than what is predicted

by Eq.(2.25). Equating Eq.(2.23) with Eq.(2.24), V_{dsat} with parasitic resistance R_{ds} will be

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \qquad (2.26)$$

$$a = A_{bulk}^2 R_{ds} C_{ox} W_{eff} v_{sat} + (\frac{1}{\lambda} - 1)A_{bulk} \qquad (2.27)$$

$$b = -[V_{gst}(\frac{2}{\lambda} - 1) + A_{bulk}E_{sat}L_{eff} + 3A_{bulk}R_{ds}C_{ox}W_{eff}v_{sat}V_{gst}] \qquad (2.28)$$

$$c = E_{sat}L_{eff}V_{gst} + 2R_{ds}C_{ox}W_{eff}v_{sat}V_{gst}^2 \qquad (2.29)$$

$\lambda=A_1+V_{gst}+A_2$ is introduced to account for non-saturating effect of the device I-V which will be discussed in 2.2.6.

2.3.6 Subthreshold I-V Model

In the subthreshold region, the potential in the channel exhibits a peak between the source and the drain. At or near the peak of the potential, the lateral electric field can be considered zero because the potential gradient is zero. Thus, the drift current can be ignored in the subthreshold region. According to the current density equation given in Eqs.(2.3) and (2.4), we have:

$$J_n = qD_n\nabla_n \quad (2.30)$$

We would like to use the charge sheet dinsity expression Q_{inv} in modeling the I-V characteristics. If we integrate Eq.(2.30) from the Si-SiO_2 interface to the edge of the depletion layer (X_{dep}) in the bulk, the current in the subthreshold region can be given as

$$I_{ds} = W_{eff}\mu_n v_t \frac{dQ_{inv}}{dy} \quad (2.31)$$

The current expression can be obtained by integrating Eq.(2.31) along the channel from source to drain,

$$I_{ds} = \frac{W_{eff}}{L_{eff}}\mu_n v_t (Q_{dinv} - Q_{sinv}) \quad (2.32)$$

where Q_{dinv} and Q_{sinv} are the channel inversion charge at the drain and source.

The channel charges at the source and drain can be written as,

$$W_{sinv} = \sqrt{\frac{q\epsilon_s iN_{CH}}{4\phi_B}} v_t \exp(\frac{V_{gs} - V_{th} - VOFF}{nv_t}) \quad (2.33)$$

$$W_{dinv} = \sqrt{\frac{q\epsilon_s iN_{CH}}{4\phi_B}} v_t \exp(\frac{V_{gs} - V_{th} - VOFF - V_{ds}}{nv_t}) \quad (2.34)$$

Therefore, the current expression becomes

$$I_{ds} = I_{s0}(1 - \exp(-\frac{V_{ds}}{nv_t}))\exp(\frac{V_{gs} - V_{th} - VOFF}{nv_t}) \quad (2.35)$$

$$I_{s0} = \mu_n \frac{W_{eff}}{L_{eff}} \sqrt{\frac{q\epsilon_s iN_{CH}}{4\phi_B}} v_t^2 \quad (2.36)$$

v_t is the thermal voltage (K_BT/q) and VOFF is the offset.

2.3.7 Other Important Parameters

1. The VOFF Parameter

The theoretical threshold voltage $V_{th,sub}$ needed to fit the subthreshold current is different form V_{th} that is used to fit strong inversion I-V. One explanation is that the surface potential corresponding to the V_{th} in strong inversion is actually higher than $2\varphi_B$. The difference between the threshold voltages discussed above is several v_t. To account for this fact, a parameter called VOFF is introduced so that

$$V_{th,sub} = V_{th} + VOFF \qquad (2.37)$$

V_{OFF} is determined experimentally from the measured I-V characteristics and is expected to be negative. Due to the physical meaning of VOFF, overly large absolute values of VOFF are not recommended in the model. The recommended range for VOFF is between -0.06 and -0.12V.

2. Drain and Source Parasitic Resistance, Rds

In BSIM3v3, the parasitic resistance of drain and source is modeld with th e following expression:

$$R_{ds} = \frac{RDSW\left[1 + PRWG \cdot V_{gsteff} + PRWB(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})\right]}{(10^6 W_{eff})^{WR}} \qquad (2.38)$$

where WR is a fitting parameter and RDSW has the units of Ω-μm^{WR}. PRWB is the body effect coefficient, and PRWG is the gate-bias effect coefficient.

3. The n Parameter for Subthreshold Swing

The n parameter can be called the subthreshold swing factor or the subthreshold slope factor because the traditional gate voltage swing of subthreshold slope can be defined as

$$S = \frac{dV_{ds}}{d\log I_{ds}} \approx 2.3nv_t \quad (2.39)$$

The subthreshold swing is the change in the gate voltage V_{gs} required to reduce the subthreshold current I_{gs} by one decade. Accordeing to Eq.(2.39), the n paramter is the key paramter in determining the subthreshold swing of the device. For long channel devices, n can be modeled as

$$n = 1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}} \quad (2.40)$$

where C_{dep} and C_{it} are the deplition layer capacitance and interface charge capacitance. However, Eq.(2.40) does not consider the influence of short cahnnel effects. In short channel devices, the potential at the surface of the channel will be determinde by both the gate bias and the drain bias through the coupling of C_{ox} and C_{dsc}, respectively, instead of the gate bias only. The coupling capacitance C_{dsc}(L) is an exponential function of the channel length. To reflect this phenomenon in BSIM3v3, the n parameter for the subthreshold swing is described in the following form:

$$n = 1 + NFACTOR\frac{C_{dep}}{C_{ox}} + \frac{C_{IT}}{C_{ox}} + \frac{(CDSC + CDSCD \cdot V_{ds} + CDSCB \cdot V_{bseff})(\exp(-DVT1\frac{L_{eff}}{2l_t}) + 2\exp(-DVT1\frac{L_{eff}}{l_t}))}{C_{ox}} \quad (2.41)$$

2.3.8 Source / Drain Series Resistance

The extrinsic parasitic resistances are important parameters which influence MOSFET performance largely. In deep sub-micron device, it becomes much more important

because the parasitic resistances are independence even if scaled down.

Ideally, in the discussion of MOSFET current, we consider the source and drain regions as conductor. However, in reality, as the current flows from the channel to the terminal contact, there is a small voltage drop in the source and drain regions due to the finite silicon resistivity and metal contact resistance. In a long-channel device, the source and drain parasitic resistances are negligible compared with the channel resistance. In a short-channel device, however, the source and drain series resistances can be an appreciable fraction of the channel resistance and can therefore cause significant current degradation. To model these parasitic resistances accurately, there are two approaches to model the parasitic source and drain resistances in BSIM3: (a) *lumped-resistance approach* and (b) *absorbedresistance approach*. It shows in Figure .

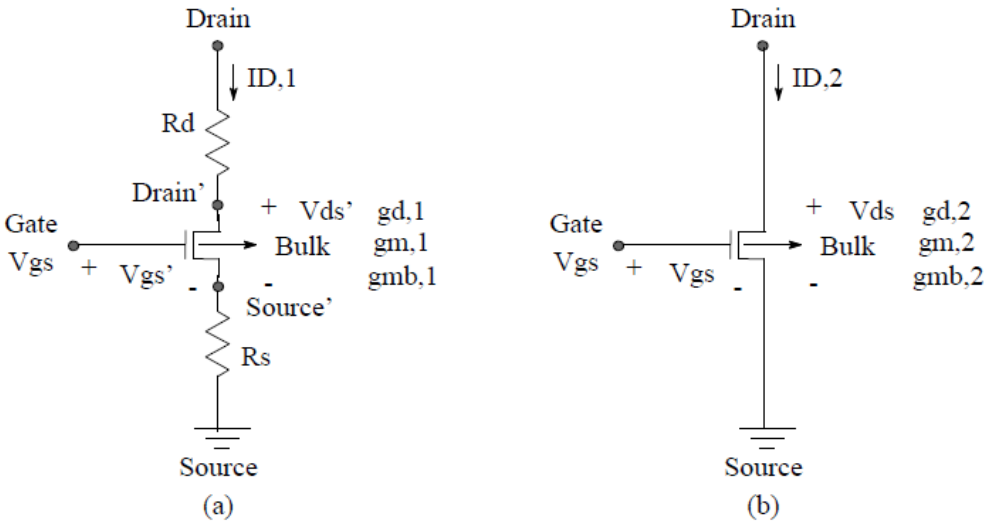


Figure 2.5 The parasitic source and drain resistances: (a) *lumped-resistance approach* and (b) *absorbed-resistance approach*.

The lumped-resistance approach, while being conceptually simple and, in fact, more accurate than the to-be-discussed second approach, has some drawbacks. First, there are

two more nodal voltages which need to be solved for each transistor; namely, the Source' and the Drain' nodes. This translates to lengthened computation time in a SPICE simulation. For simple circuit with few transistors, however, we believe this extra amount of time needed for numerical solution is trivial. Second, generally SPICE parameters are extracted by matching the measured and simulated values of the drain current and the mutual transconductance. In a measurement setting, the measured current is that at the Drain node, and the measured g_m, for example, is equal to $@I_d=@V_{gs}$(still referring to Figure 2.5.(a)). The calculated drain current, which is the current at the Drain' node, will be the same current that flows through the Drain node. Therefore, extracting parameters by fitting the simulated current at the Drain' node against the measured current at the Drain node makes sense. However, the calculated g_m from BSIM3 is really $@I_{0d}=@V_{0gs}$, which often differs significantly from measured gm equaling to $@I_d=@V_{gs}$. Hence, unless a numerically intensive SPICE subroutines are incorporated to calculate the derivatives at the Drain' and

Source' nodes, SPICE parameters should not extracted by fitting the measured and simulated g'$_m$s.

Some formulas are proposed to correct this problem. With a certain small-signal approximation, it is possible to relate the measured conductances to intrinsic conductances:

$$g_d \approx \frac{g_{d,i}}{1 + g_{m,i}R_S + g_{d,i}(R_S + R_D) + g_{mb,i}R_S} \qquad (2.42)$$

$$g_m \approx \frac{g_{m,i}}{1 + g_{m,i}R_S + g_{d,i}(R_S + R_D) + g_{mb,i}R_S} \qquad (2.43)$$

$$g_{mb} \approx \frac{g_{mb,i}}{1 + g_{m,i}R_S + g_{d,i}(R_S + R_D) + g_{mb,i}R_S} \qquad (2.44)$$

where, for example, g_d is $@I_d=@V_{ds}$, the measured drain conductance, and $g_{d,i}$ is the intrinsic device conductance calculated in BSIM3, equal to $@I_d=@V_{0\,ds}$. After the application of Eq.(2.43), it is possible to extract parameters by fitting BSIM3 generated $g_{d,i}$ to the measured g_d. We caution that, although the approximation of g_d given in Eq.(2.43) is fairly good, using Eq.(2.42) to relate gm and $g_{m,i}$ can run into problems unless the current is fairly low. The equations expressed in Eqs.(2.42)-(2.44), after all, are derived with the small-signal assumption, which can sometimes fail at normal operating current levels.

BSIM3 offers another approach to model the parasitic source/drain resistances, basically by absorbing the parasitic resistances' effects on current and conductances into the intrinsic device. The equivalent circuit is shown in the right-hand side of Figure 2.5. In this absorbed-resistance approach, the nodes Drain' and Source' disappear. The drain current and mutual transconductance are calculated from a totally different set of equation

$$ID,2 = f2(VGS, VDS, RD + RS)$$

$$gd,2 = \frac{\partial ID,2}{\partial VDS} \qquad (2.45)$$

$$gm,2 = \frac{\partial ID,2}{\partial VGS}$$

$$gmb,2 = \frac{\partial ID,2}{\partial VBS}$$

We use f_2 to describe the function form of $I_{D,2}$, in order to stress that the function differs from f_1 used in the calculation of $I_{D,1}$. Basically, BSIM3 devises some sort of function f_2, which is a modified version of f_1 to account for the effects of the parasitic resistances. The amount of deviation from the original f_1 depends on the magnitude of R_D+R_S. The

larger the value of RD+RS, the more significant the deviation. The modification is made in ways such that somehow $I_{D,2}$ is approximately equal to $I_{D,1}$ and more importantly, $g_{d,2}$, $g_{m,2}$ and $g_{mb,2}$ are approximately equal to $g_{d,1}$, $g_{m,1}$ and $g_{mb,1}$, respectively. Note the keyword above is approximately. No matter how clever the BSIM3 modification may be, there is no way to replace the SPICE simulator's mathematical calculations of the two additional nodal voltages if the extract solution is desired. The approximation is most accurate when the drain current is small such that the voltage drop across R_S is small compared to the applied V_{GS}. However, despite some claims to the contrary, it is believed that the error can be quite high (exceeding 10 % at least) when the current flow is large. Setting the issues of dc accuracy aside, the absorbed-resistance approach is also discouraged for RF applications. When the second approach is used, the input resistance of the MOSFET will be purely imaginary, without seeing the effect of R_S. This is because BSIM3 makes an attempt to equilibrate only the drain current and the conductances at the two sides of Figure 2.5. The fact that the device y-parameters of the overall device are greatly altered when two extra nodes are added is not considered. Here are some details of the actual BSIM3 implementation. When the lumped-resistance approach is used, R_S and R_D are specified with the SPICE parameter *RSH* (sheet resistance of the source and drain contact), together with the fields *NRD* (number of squares in the drain contact) and *NRS* (number of squares in the source contact) found in the device statement. They are given by

$$R_S = RSH \times NRS; \quad R_D = RSH \times NRD \qquad (2.46)$$

RDSW, to be discussed shortly, should be zero in this *lumped-resistance approach*.

In the *absorbed-resistance approach*, we see that the function f_2 in Eq.(2.45) depends

on the sum of R_S and R_D, rather than each component individually. From this observation alone, we can infer that BSIM3 uses a completely new parameter for this approach, independent from the aforementioned *RSH*, *NRS* and *NRD*. It is *RDSW*, the sum of source and drain resistances per unit width. When this approach is used, *RSH* should be set to zero, and *RDSW* can be approximated from the measured R_S and R_D:

$$R_S + R_D \approx \frac{RDSW}{W} \qquad (2.47)$$

where W is the device's width. (The actual relationship between the parasitic resistances and *RDSW* includes other parameters such as *WR*, *PRWG* and *PRWB* to account for secondary effects. Eq.(2.47) is valid when *WF*, *PRWG*, and *PRWB* assume their default values of 1, 0, and 0, respectively.) For a RF circuit designer who would like to see nonzero real part input resitance due to the source resistance, the lumped-resistance approach is preferred and *RDSW* should be zero.

2.4 Modeling of the Extrinsic MOSFET

Although many MOSFET models, including MOS9, EKV and BSIM3v3, have been developed for digital, analog and mixed-signal applications, the RF MOSFET modeling accuracy of the existing MOSFET compact model is not satisfactory. It is because, at high frequency region, the parasitic components severely influence to device RF performance and it is difficult to predict these parasitics behavior only within a compact model. To make models more accurate at RF, sub-circuits are usually added to intrinsic transistor model, BSIM3v3 in this paper, as shown in Figure 2.6. Simple sub-circuits are preferred to reduce the simulation time and to make parameter extraction easier. For an

AC small signal model at RF, the modeling of sub-circuits components, i.e. the parasitic components, is very important. The models for these parasitic components should be physics-based and linked to process and geometry information to ensure the scalability and prediction capabilities of the model. In this section, the methodologies of the extrinsic parameter extraction, which surround the intrinsic MOSFET in Figure 2.6 will be described.

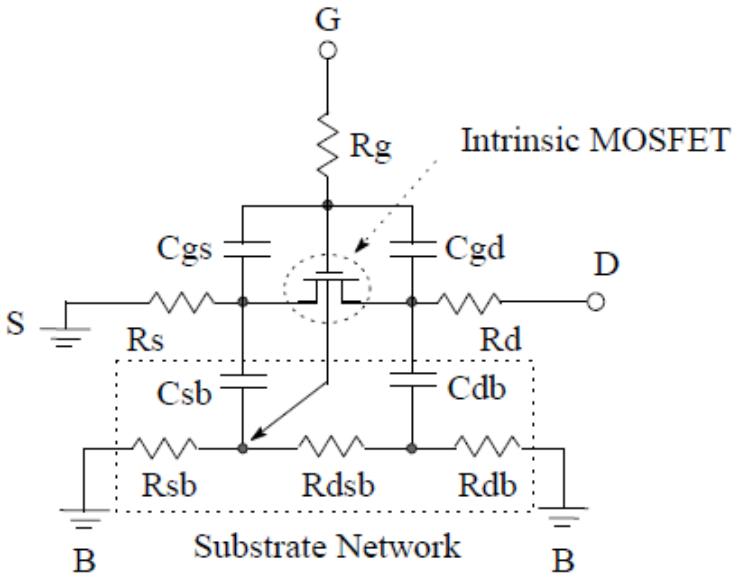


Figure 2.6 Sub-circuit model with intrinsic and extrinsic components [12]

2.4.1 Gate Resistance Model

The typical sheet resistance for a poly-silicon gate ranges between 20-40 Ω/square and can be reduced by a factor of 10 with a silicide process, and even more with a metal stack process. At DC and low frequency, the gate resistance consists mainly of the poly-silicon sheet resistance and is independent of bias. However, at high frequency, it becomes a bias-dependent component and two additional physical effects will affect the

effective gate resistance [19][20]: the distributed gate electrode resistance (R_{eltd} or R_{poly}) and non-quasi-static (NQS) effects (R_{ch}), as shown in Figure 2.7. [14],

$$R_g = R_{eltd} + R_{ch} \quad (2.48)$$

At first, the distributed gate electrode resistance (R_{eltd}) will be described. It will become more severe as the gate width becomes wider at higher operation frequency. So multi-finger devices are used in the circuit design with narrow gate width for each finger to reduce the influence of

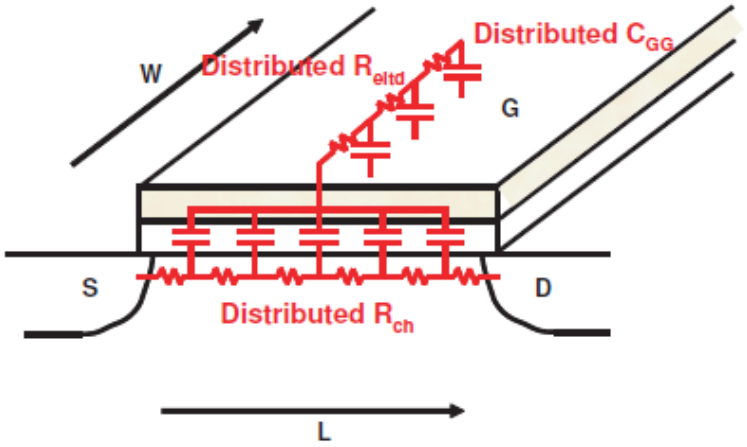


Figure 2.7 Distributed gate electrode resistance R_{eltd}, channel resistance R_{ch} and gate capacitance C_{gg}.

this effect. With multi-finger devices, gate resistance can separate, as shown in Figure 2.8 [19]. As R_{eltd} is insensitive to bias and freqency, its value can be obtained from the gate electrode sheet resistance ($R_{eltd\text{-}sh}$),

$$R_{eltd} = \alpha \frac{W_{total}}{LN_f^2} R_{eltd-sh} \quad (2.49)$$

$$= \alpha \frac{W_{unit}}{LN_f} R_{eltd-sh} \quad (2.50)$$

where α is 1/3 when the gate terminal is brought out from one side, or 1/12 when

connected on both sides [21]. The value of α accounts for the distributed nature of the RC line across the channel.

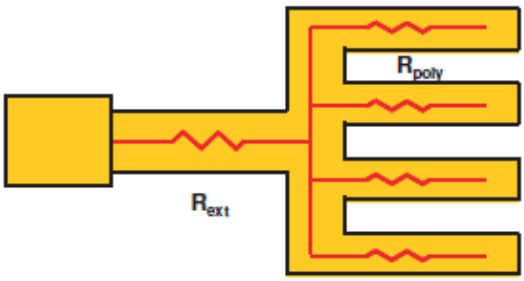


Figure 2.8 Divided R_{eltd} into R_{ext} and R_{poly} with multi-finger devices.

Next, NQS effects (R_{ch}) in the channel will be described. For the devices with NQS effects, additional bias and geometry dependences of the gate resistance are needed to account for the NQS effects. There are two mechanisms involved in R_{ch}: one is the static channel resistance (R_{st}), which accounts for the dc channel resistance and the other is the excess diffusion channel resistance (R_{ed}) due to the change of channel charge distribution by ac excitation of the gate voltage. R_{st} and R_{ed} together determine the time constant of the NQS effects. R_{st} is modeled by integrating the resistance along the channel under quasi-static assumption,

$$R_{st} = \int dR = \int \frac{dV}{I_d}$$

$$= \frac{V_{ds}}{I_d} \; @ \; triode \; region; \qquad (2.51)$$

$$= \frac{V_{dsat}}{I_d} \; @ \; saturation \; region, \qquad (2.52)$$

where V_{dsat} is the saturation drain voltage. Both I_d and V_{dsat} are available in BSIM3v3. R_{ed} can be derived from the diffusion current as

$$R_{ed} = \frac{qL}{\eta W \mu C_{ox} kT} \qquad (2.53)$$

where η is a technology-dependent constant. The overall channel resistance seen from the gate is

$$\frac{1}{R_{gch}} = \gamma\left(\frac{1}{R_{st}} + \frac{1}{R_{ed}}\right) \qquad (2.54)$$

where γ is a paremeter accounting for the distributed nature of the channel resistance and C_{ox} is oxide capacitance per unit area. γ equals to 12 if the resistance is uniformly distributed along the channel. Since this assumption is not valid in the saturation region, γ is left as a fitting parameter.

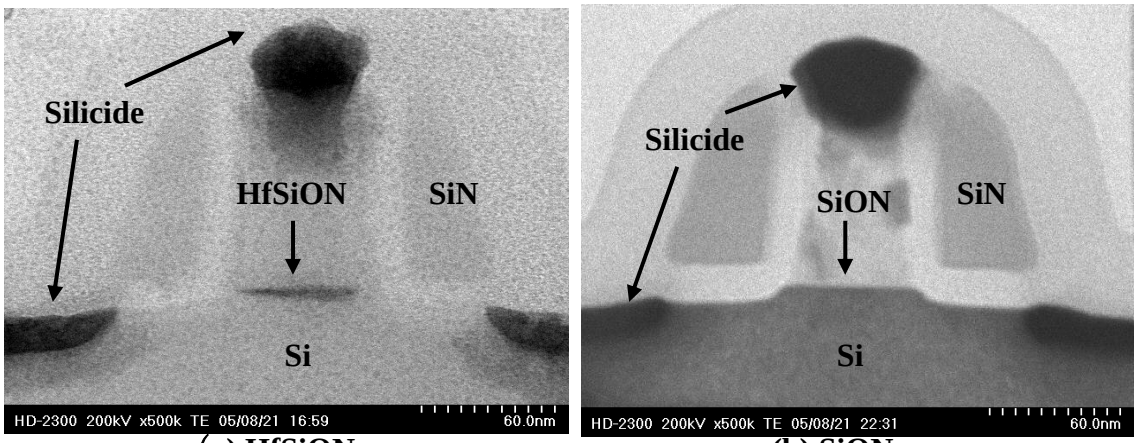
Chapter 3

RF Characteristics of High-k MOSFET

In this chapter RF characteristics of next generation sub-100nm high-k MOSFET are discussed as being related to DC characteristics and device structure. RF characteristics of high-k MOSFET is analyzed based mainly on gate resistance and capacitance extracted from measured S-parameter up to 40 GHz. In consequence RF application of high-k MOSFET is explored by examining various issues of high-k MOSFET.

3.1 Device structure

In this chapter two type of high-k MOSFET which have higher dielectric constant gate insulator than SiO_2; one is HfSiON and the other is SiON, were focused on. High-k technology is now researched and developed actively in device process research. There are a lot of papers about process technology on high-k. With down scaling of device gate leakage current has been significant problem because it leads to high electricity dissipation. High-k prevents gate leakage current caused by electron tunneling at gate insulator increasing. However, there are some concerns on high-k MOSFET. First is degradation of channel electron mobility by surface roughness. This may affect to RF characteristics of device. Second is fall of dielectric constant in RF region by dielectric dispersion. If this is truth high gate capacitance with a thick gate insulator, one of merits of high-k MOSFET, can not be kept in RF region. The merit of high-k MOSFET is lost.



(a) HfSiON **(b) SiON**

Figure 3.1 Transistor structure TEM

Cross section of transistor structure is indicated at Figure 3.1 and (a), (b) is HfSiON device and SiON device respectively (HfSiON device and SiON device is mentioned as HfSiON and SiON simply at the following). High-k gate insulator pile up on Si substrate and Silicide is done at electrodes. EOT is 1.5 [nm] on both device.

In this study multi gate finger structure is applied to reduce gate resistance. Gate resistance Rg is described by Eq. 3.1.

$$R_g, eff = \frac{1}{3} R_{sh} \frac{W_f}{LN_f} = \frac{1}{3} R_{sh} \frac{W_{total}}{LN_f^2} \qquad (3.1)$$

W_f: Finger length, N_f: Number of finger

As Eq. (3.1) indicates, as number of gate finger increase, Rg is reduced. Plane Figure is indicated at Figure 3.2. Unit device which is indicated at Figure 3.1 is arranged in parallel.

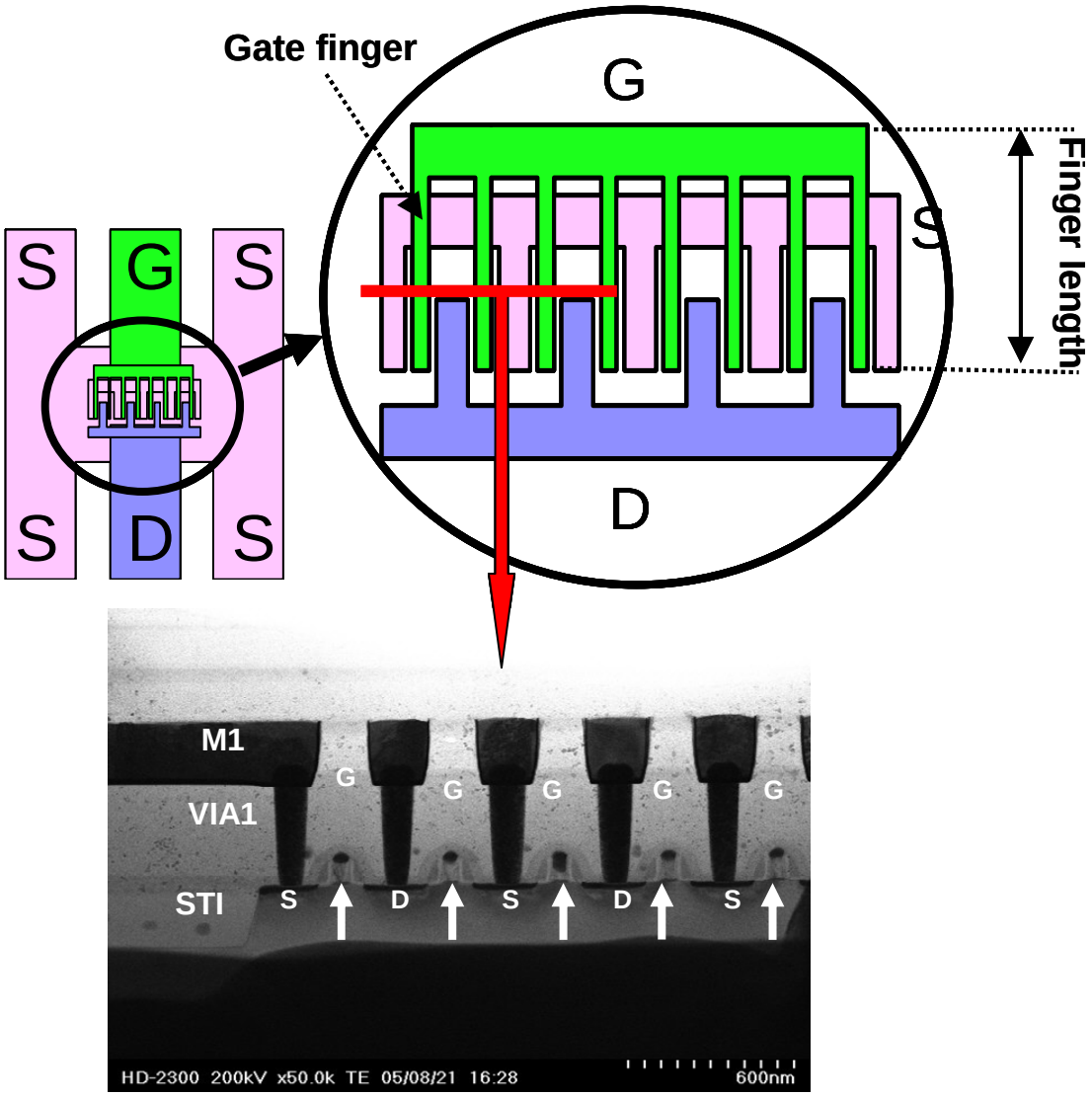
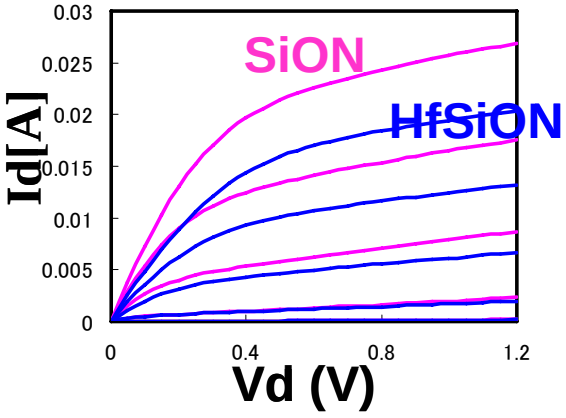


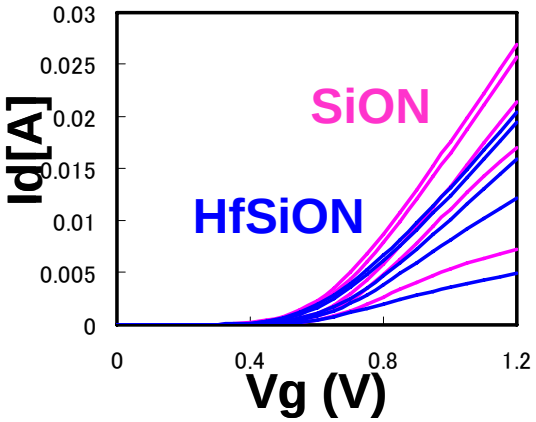
Figure 3.2 Multi gate finger structure

3.2 DC Characteristics

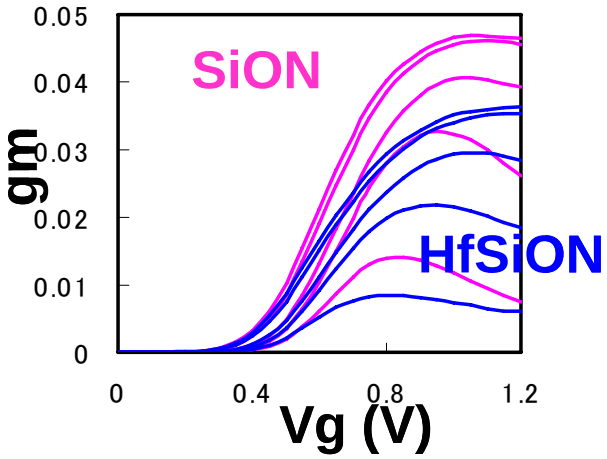
Figure 3.3 shows DC characteristics of high-k MOSFET. One is HfSiON device and another is SiON device. Both devices are fabricated in 90 nm technology node. Effective gate length of HfSiON device is 64 [nm] and that of SiON device is 51 [nm]. Number of gate fingers is 12 and finger width is 5 [um], this is equal to that gate width is 60 [um].



(a) Id-Vg characteristics
@ Vg = 0.6, 0.8, 1.0, 1.2, 1.5



(b) gm-Vg characteristics
@Vd = 0.6, 0.8, 1.0, 1.2 ,1.5



(c)Id-Vd charcteristics

Figure 3.3 DC characteristics

As this figure indicates, SiON device has better DC characteristics. It seems that this is due to the difference of gate length and electron mobility at channel. At Figure 3.3 (c), SiON device of transconductance g_m (Eq. (3.2)) is higher than that of HfSiON device. g_m is affected by gate length, gate width and mobility. This difference of g_m affects RF characteristics as mention later.

$$g_m = \frac{\partial Id}{\partial Vg} = \frac{W}{L}\mu C_{ox} Vd \qquad (3.2)$$

Figure 3.4 shows DC characteristics at different temperature condition. DC measurement was performed at various conditions in addition to room temperature.

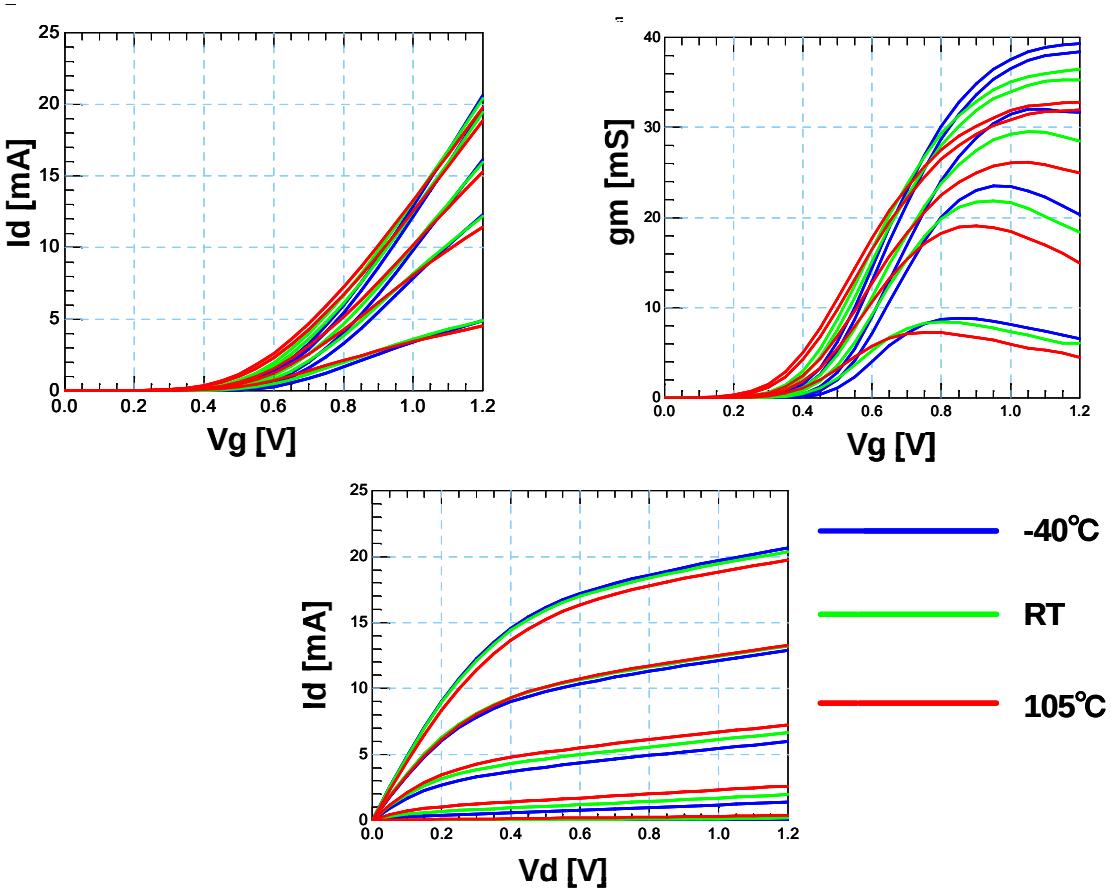


Figure 3.4 Temperature dependency of DC characteristics of HfSiON device

Trans conductance g_m improved at -40 ^oC. Mobility improvement at low temperature leads to g_m improvement.

3.3 RF Characteristics

3.3.1 Cutoff Frequency and Maximum Oscillation Frequency

S-parameter were measured up to 40GHz and cutoff frequency f_T and maximum oscillation frequency f_{max} are extracted from measured S-parameter. They are important figure of RF characteristics. Figure 3.5 indicates H_{21} which is 21 entry of H-parameter of device and Figure 3.6 indicates Unilateral gain which is described by Eq. (1.2). Those are gotten from measured S-parameter.

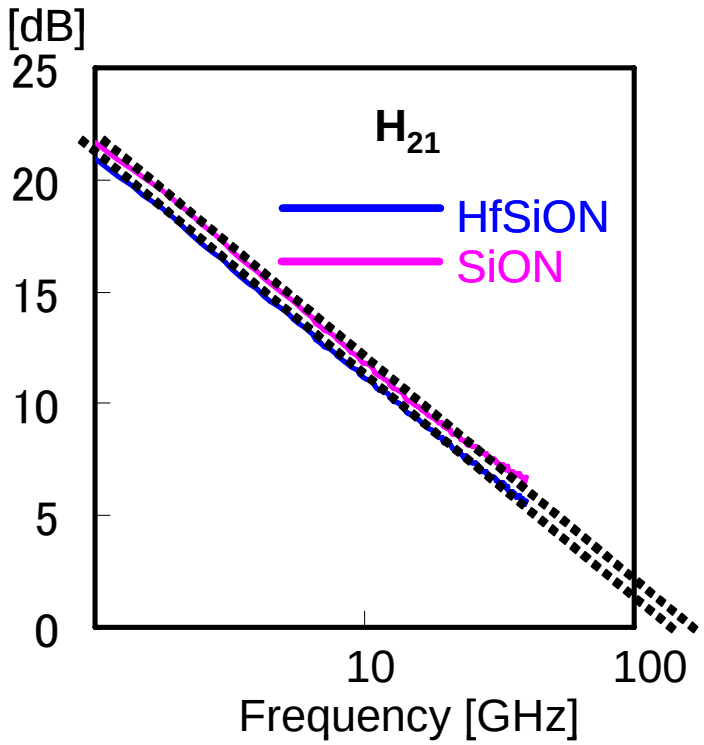


Figure 3.5 H_{21} @ gm peak bias; Vg = 1.2 [V], Vd = 1.2 [V]

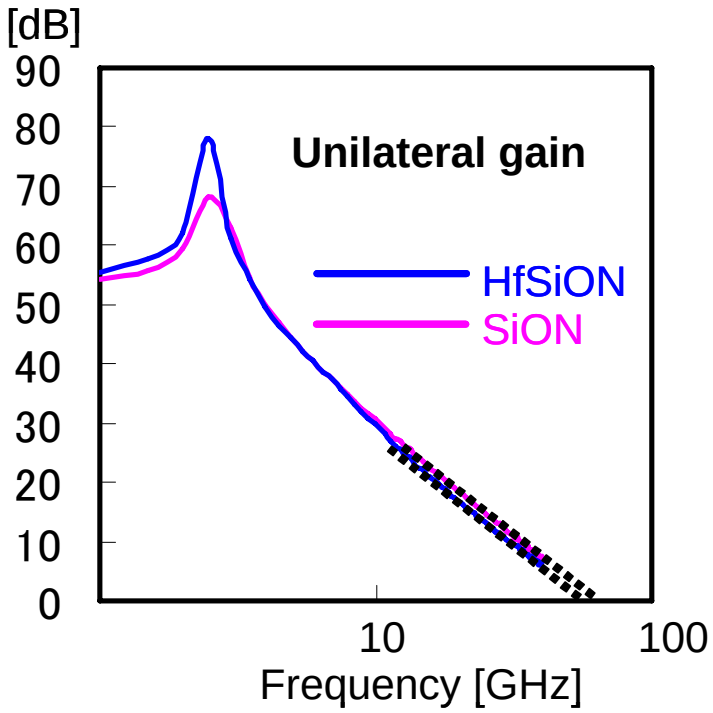


Figure 3.6 Unilateral gain @ gm peak biasVg = 1.2 [V], Vd = 1.2 [V]

f_T and f_{max} are the frequency at which H_{21} and unilateral gain is 0 [dB]. The value of f_T and f_{max} extracted from Figure 3.5 and 3.6 is shown at Table 3.1.

Table 3.1 f_T and f_{max} @ 5 [um] finger

	HfSiON	**SiON**
f_T [GHz]	**131**	**155**
f_{max} [GHz]	**58**	**53**

As for f_T, the value over 100 GHz were gotten on both devices. However, there are difference between two devices, f_T of SiON device is bigger than that of HfSiON device. This is due to the difference on g_m on DC characteristics shown in Figure 3.3. g_m of

SiON device is bigger than that of HfSiON device. Gate voltage dependency of g_m and f_T are shown in Figure 3.7.

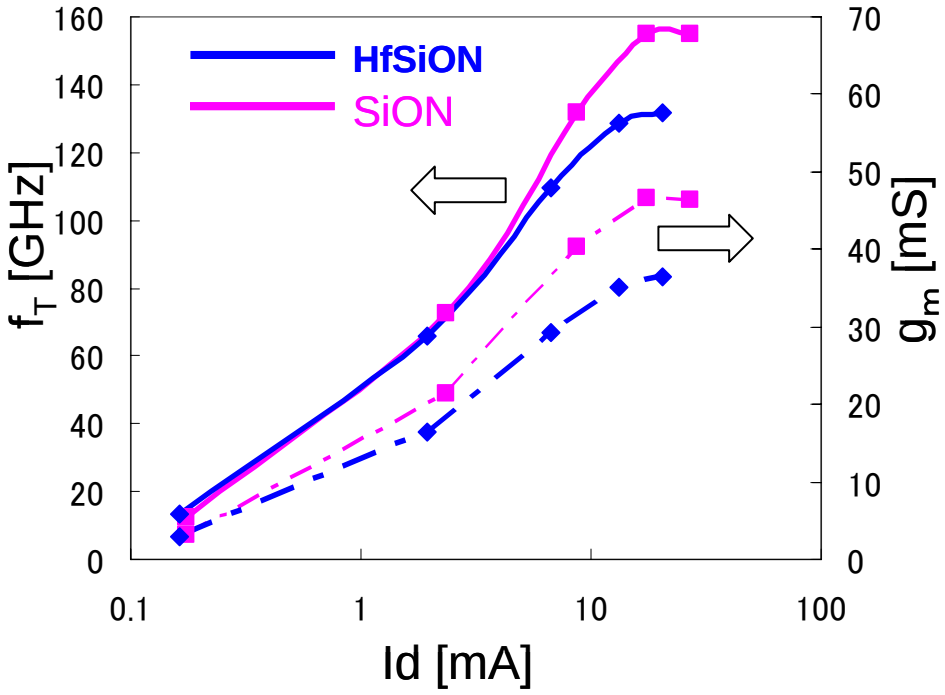


Figure 3.7 Gate voltage dependency of g_m and f_T @ Vd = 1.2

f_T reflects to the transition of g_m, depending on device structure and mobility

As for $f_{max,}$ extracted values were low and there are little difference between HfSiON and SiON. It is known that f_{max} is not scaled. However, this low f_{max} is affected by gate resistance. Extracted gate resistance from measured S-parameter is shown in Figure3.8.

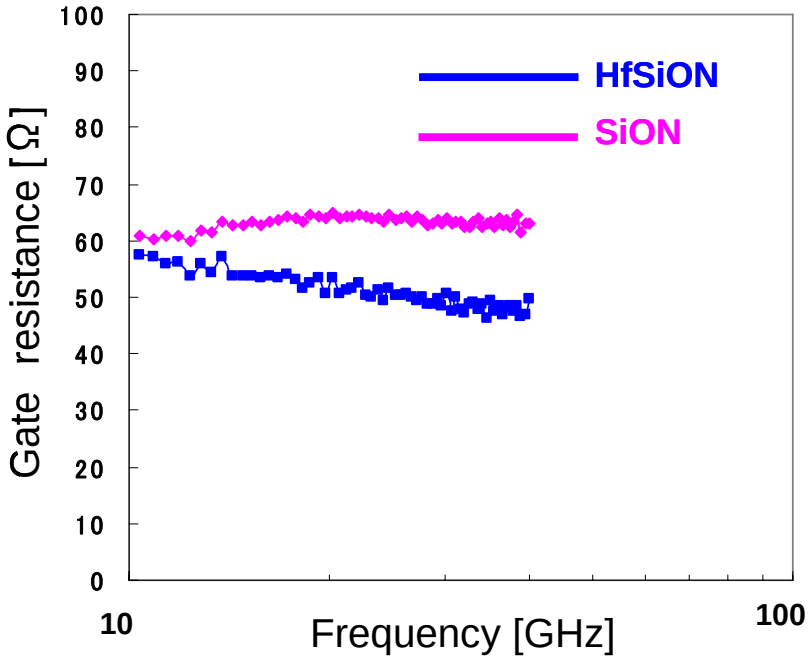
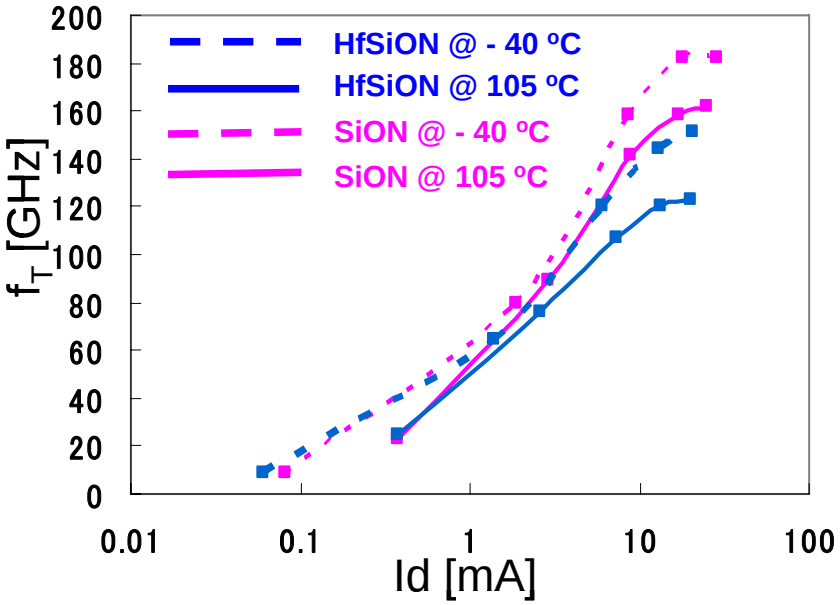


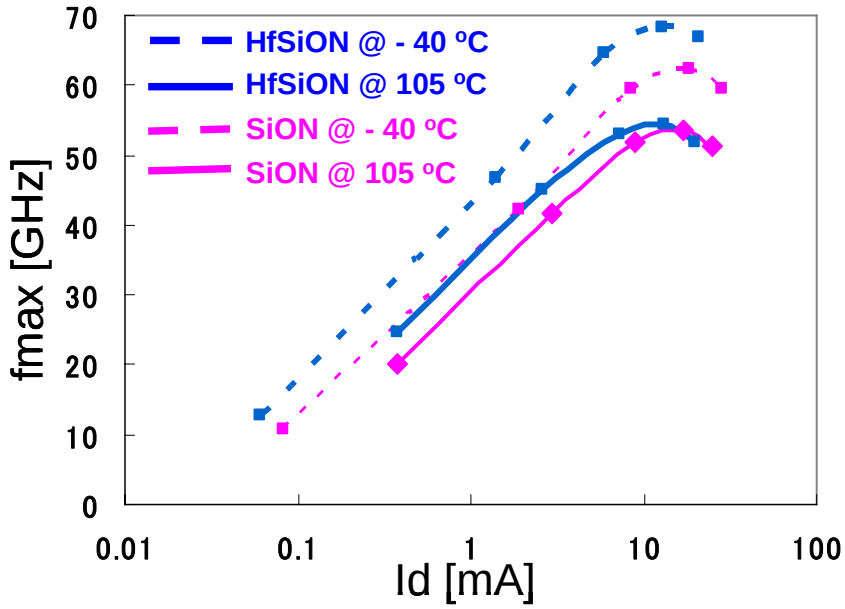
Figure 3.8 Extracted gate resistance Rg

As Figure 3.8 shows, gate resistance Rg is large. f_{max} is described by Eq. (1.3). Therefore large Rg leads to low f_{max}. And Figure 3.8 shows that Rg of SiON device is bigger than that of HfSiON device. Although there are a little difference on gate length among two devices, it can be thought that f_{max} of HfSiON device is bigger than that of SiON device because Rg of SiON device is bigger. Gate resistance Rg is analyzed later.

Temperature dependent of f_T, f_{max} is shown in Figure 3.9. f_T and f_{max} is reflected by temperature dependent of DC characteristics. Mobility improvement at low temperature affect RF characteristics.



(a) Temperature dependent of f_T



(b) Temperature dependent of f_{max}

Figure 3.9 Temperature dependent of f_T and f_{max}

On the other hand, device which has 2 [um] of finger length but the other structure is the same were also analyzed. H_{21} and unilateral gain of the device are shown in Figure 3.10 and 3.11. Figure 3.10 shows H_{21} and unilateral gain of HfSiON device, Figure 3.11 shows those of SiON device.

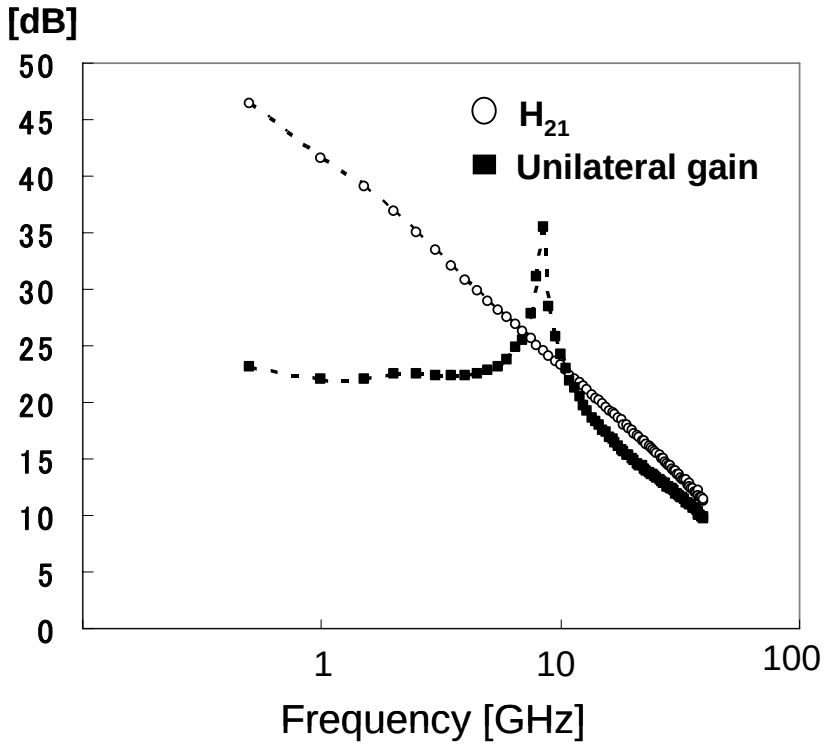


Figure 3.10 H_{21} and unilateral gain of HfSiON

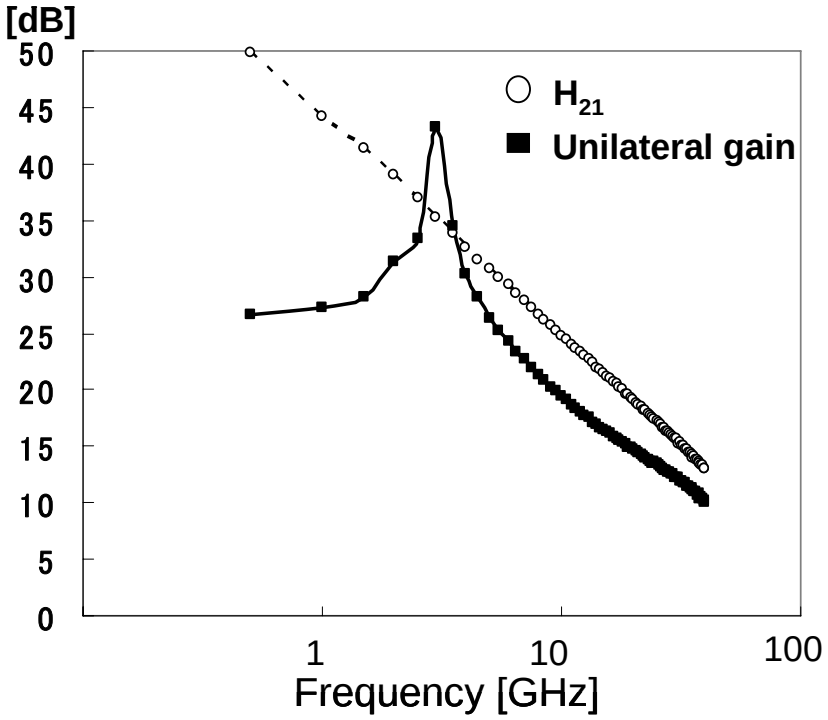


Figure 3.11 H_{21} and unilateral gain of SiON

f_T and f_{max} from extending H_{21} and unilateral gain at Figure 3.10 and 3.11 are shown in Table3.2.

Table 3.2 f_T and f_{max} @ 2 [um] finger

	HfSiON	**SiON**
f_T [GHz]	**147.91**	**177.83**
f_{max} [GHz]	**121.62**	**127.35**

As Table 3.2 shows, both f_T and f_{max} were improved at 2 [um] finger in comparison with 5 [um] finger. This corresponds with simulation result on gate finger length dependency of RF figure (f_T and f_{max}) which is indicated in [5]. Gate finger length has a optimum point. RF MOSFET has best performance in terms of f_T and f_{max} at the optimum point.

3.4 Parameter Extraction

3.4.1 Extraction of DC Parameter

Extraction of DC parameter by fitting using BSIM 3 was performed on HfSiON device and SiON devise. Both device have same structure; gate length is 58.6 [nm], number of finger is 48, finger length is 2 [um] (if not otherwise specified the same structure is applied in what follows). Measured DC data and simulation data of HfSiON by BSIM4 is shown in figure 3.12 and those of SiON is shown in Figure 3.13.

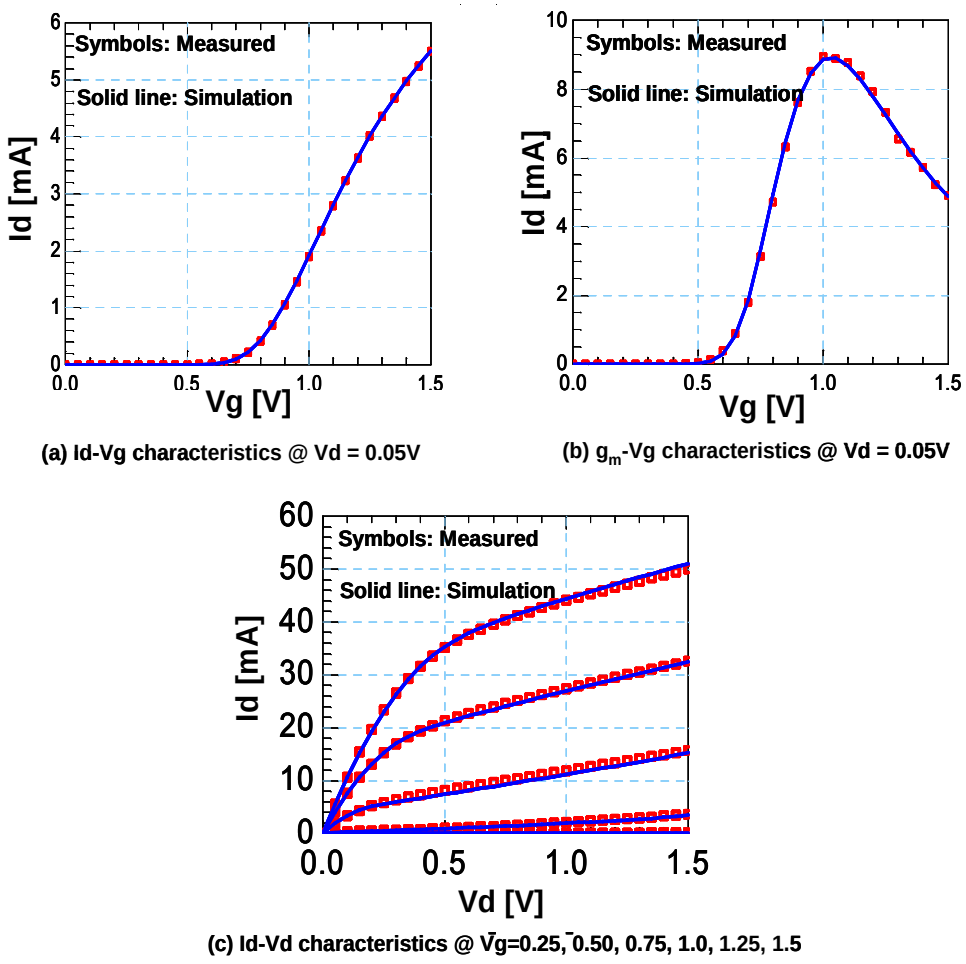


Figure 3.12 DC modeling of HfSiON device

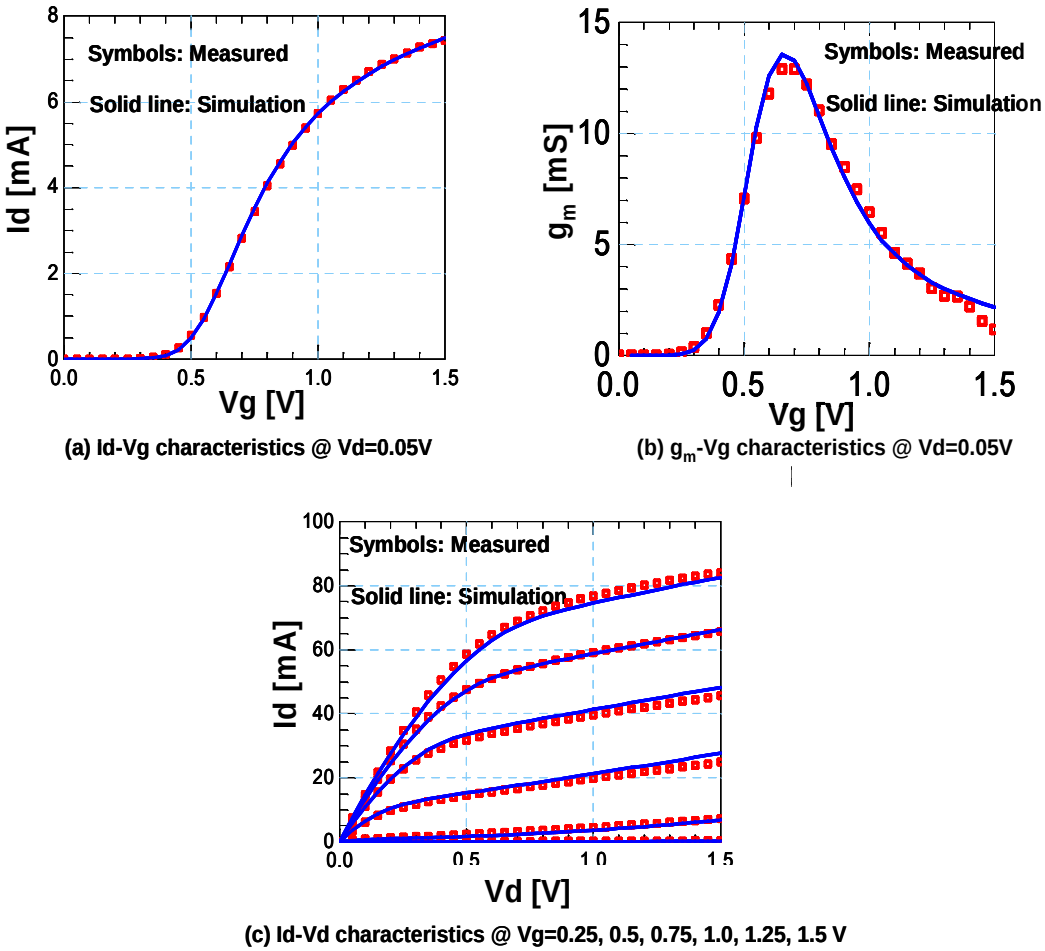


Figure 3.13 DC modeling of SiON device

Simulation data fits measured data well on both devices. Principal difference between two devices is threshold voltage. Vth of HfSiON is 0.7262 [V], Vth of SiON is 0.4582 [V]. As for channel mobility, there are a little difference between two devices. μ_0 of HfSiON is 356.5 [cm^2/V] and μ_0 of SiON is 319.2 [cm^2/V].

3.4.2 Extraction of Extrinsic Components by Using Equivalent Circuit

In this section, terminal resistances (gate resistance Rg, drain resistance Rs, source resistance Rs) are focused on. The extraction of the terminal resistances is done by performing Z-parameter analysis on the equivalent circuit at the linear region of the transistor. It is proposed that the extraction of the resistances is done at Vg=1.5 V and Vd = 0V. At this bias condition, the transconductance and transcapacitance are both close to zero and influence by substrate components can be neglected[13]. The simplified equivalent circuit of MOSFET at Vg=1.5 V and Vd=0 V is shown in Figure3.14.

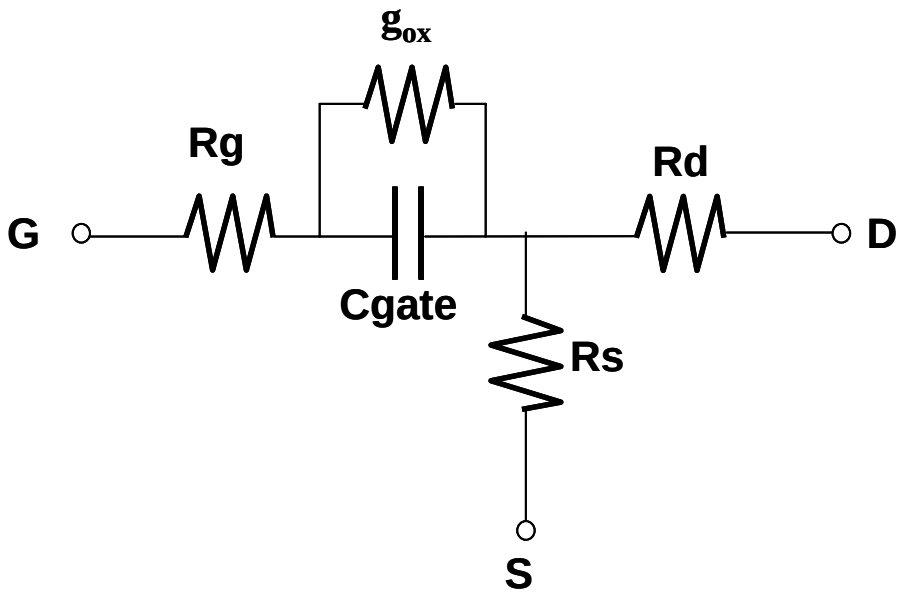


Figure 3.14 Equivalent circuit @ Vg =1.5 V and Vd=0V

The resistance Rg represents the effective lumped gate resistance, consisting of both the electrode resistance and the distributed channel resistance [14]. It has been reported that a simple gate resistance model has been found accurate up to 0.5 f_T [15]. The resistance Rd and Rs represent effective drain and source resistances that consist of the via, salicide, contact and LDD resistances [16]. The capacitance Cgate is gate capacitance consist of effective gate-to-drain capacitances and gate-to-source capacitances, intrinsic gate insulator capacitance and gate overlap capacitance. g_{ox} represents the conductance of gate insulator part, which means easiness of gate leakage current.

In Figure 3.12, Z-parameter can be written as below.

$$\begin{aligned} Z11 &= Rg + Rs + \frac{Rl}{j\omega Cgate \cdot Rl + 1} \\ Z12 &= Z21 = Rs \\ Z22 &= Rd + Rs \end{aligned} \qquad (3.3)$$

At Eq. (3.3), $Rl = 1/g_{ox}$. By using Eq.(3.3), components of equivalent circuit can be extracted from measured S-parameter. In this chapter, analyzed device is finger length is 2 [um], number of finger is 48, gate length is sub-100nm.

3.4.3 Influence of Gate Leakage Current to Gate Resistance

Gate leakage current of MOSFET is important factor in sub-100 nm generation. It causes increase of electrical dissipation. This is a motivation for adopting high-k MOSFET. Although two type of devices which have HfSiON and SiON as gate insulator are interest in this study, dielectric constant of HfSiON is larger than that of SiON. Therefore, gate leakage current of SiON is lareger than that of HfSiON. In this section, influence of gate leakage current to gate resistance is discussed. As mentioned previously, gate resistance is important parameter of RF MOSFET.

Gate leakage current is shown in Figure 3.15.

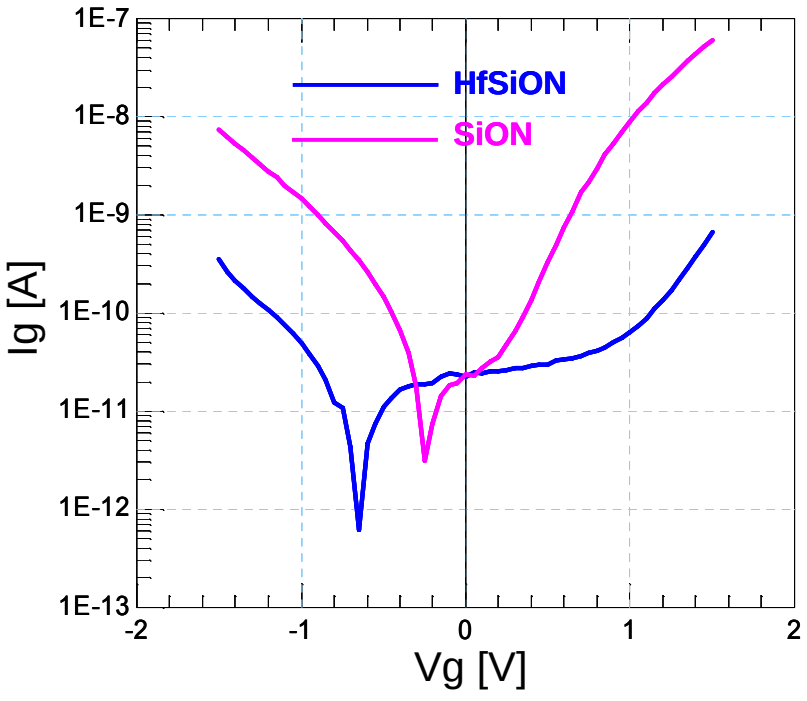


Figure 3.15. Gate leakage current of two devices

There is difference of gate leakage current, leakage current of SiON is larger than that

of HfSiON. This means that Rl ($=1/g_{ox}$) of HfSiON is larger than that of SiON. At Vg=1.5 V, the difference of gate leakage current between two devices is two columns.

In this section, Z-parameter analysis is performed. Real part of Z11 is described at Eq. (3.4) based on Figure 3.14.

$$real(Z11) = Rg + Rs + \frac{Rl}{1 + (\omega CgateRl)^2}$$
$$imag(Z11) = -\frac{\omega CgateRl^2}{1 + (\omega CgateRl)^2} \qquad (3.4),$$

Real part of Z11 and imaginary part of Z11 calculated from measured S-parameter up to 40GHz are shown in Figure 3.16 and 3.17.

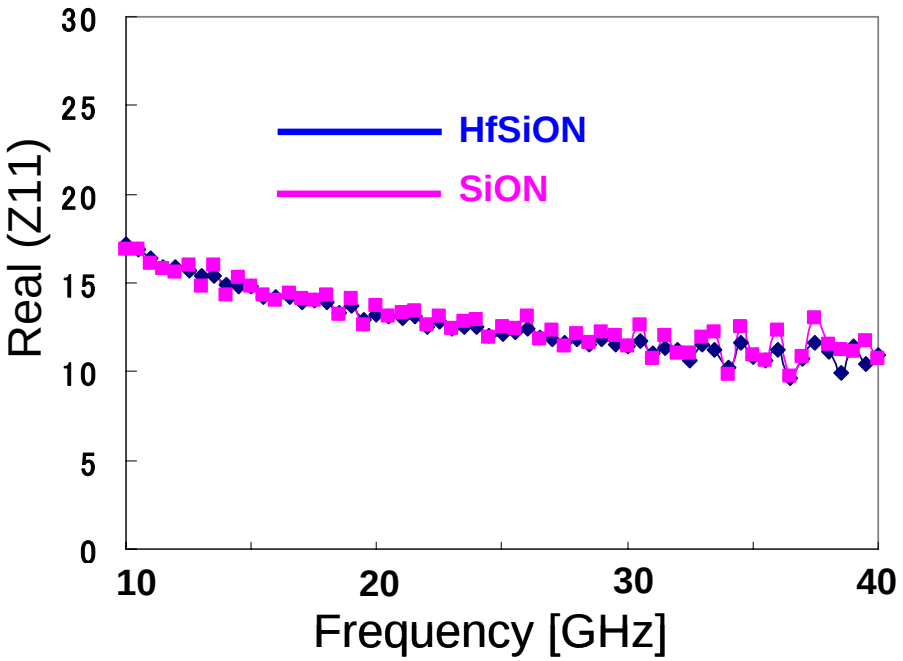


Figure 3.16 Real part of Z11 at Vg = 1.5 V

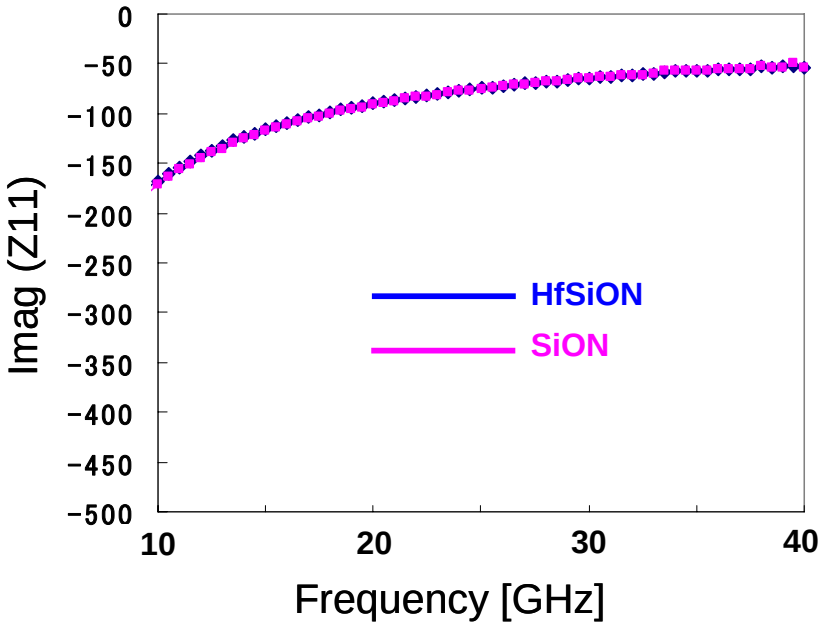


Figure 3.17 Frequency dependent of imaginary part of Z11

As for *real(Z11)* and *imag(Z11),* there are little difference between two devices.

Real part of Z12 which represents Rs by Eq. (3.3) is shown in Figure 3.18.

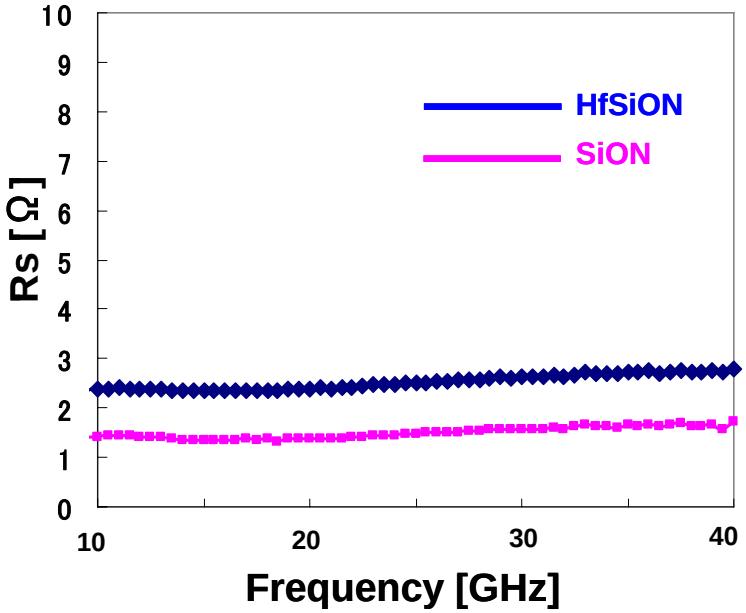


Figure 3.18 Real part of Z12 which represents Rs

There are a little difference between two devices on Rs.

Next, Rg is extracted from measured S-parameter. By using Eq. (3.3) and (3.4),

$$real(Z11) - real(Z12) = Rg + \frac{Rl}{1 + (\omega CgateRl)^2} \qquad (3.5).$$

At high frequency region, second term of Eq. (3.5) can be neglected. Therefore Eq. (3.5) represents Rg. By using *real(Z11)* shown in Figure 3.16 and *real(Z12)* shown in Figure 3.18, real part of series parameter of gate part "*real(Z11)-real(Z12)*" is shown in Figure 3.19.

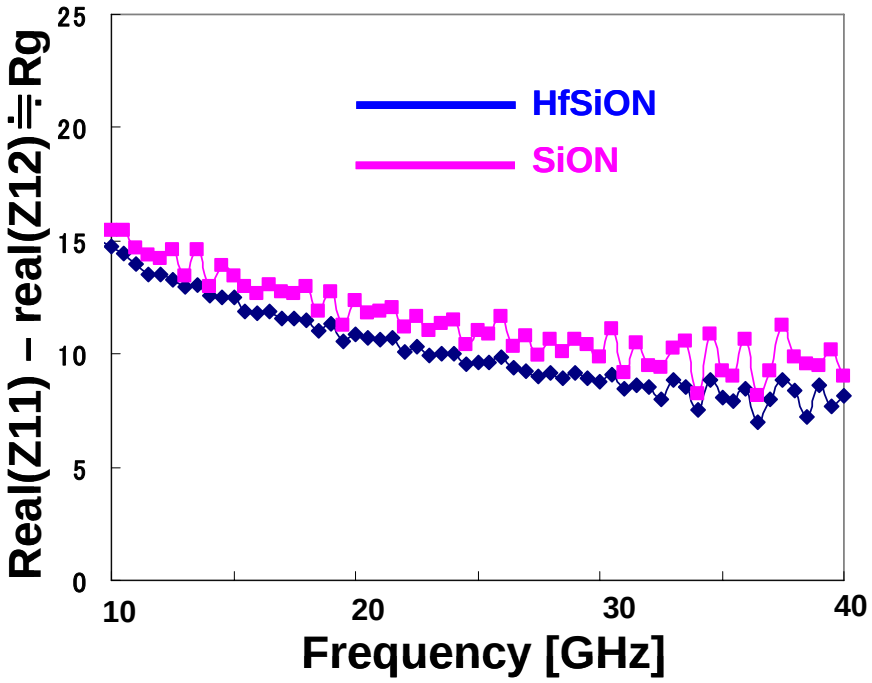


Figure 3.19 Real part of series parameter of Gate part

real(Z11)-real(Z12) is little different from *real(Z11)* because *real(Z12)* is small in comparison with *real(Z11)-real(Z12)*. And the difference between two devices on real(Z11)-real(Z12) can be seen.

Then, *ral(Z11)-real(Z12)* from measured S-parameter compare with calculated *real(Z11)-real(Z12)* and discuss if Rl can affect Rg.

How to calculate real(Z11)-real(Z12) is indicated as below. At first, g_{ox} can be extract by using Ig-Vg characteristics of MOSFET, Figure 3.15. g_{ox} represents Ig divided by Vg. Ig is 664.1 [pA] on HfSiON, 60100 [pA] on SiON at Vg=1.5 V, Vd=0 V. g_{ox} at the bias is shown in Table 3.3.

Table 3.3 Gate Leakage Component g_{ox} on both devices

	HfSiON	**SiON**
g_{ox}	**$4.43*10^{-10}$**	**$4.01*10^{-8}$**

By using Rg extracted from measured S-parameter and g_{ox} from DC characteristics, Cgate from device structure, *real(Z11)-real(Z12)* can be calculated. It is shown in Figure 3.20 where the calculated value of *real(Z11)-real(Z12)* when gate leakage current increase are plotted altogether.

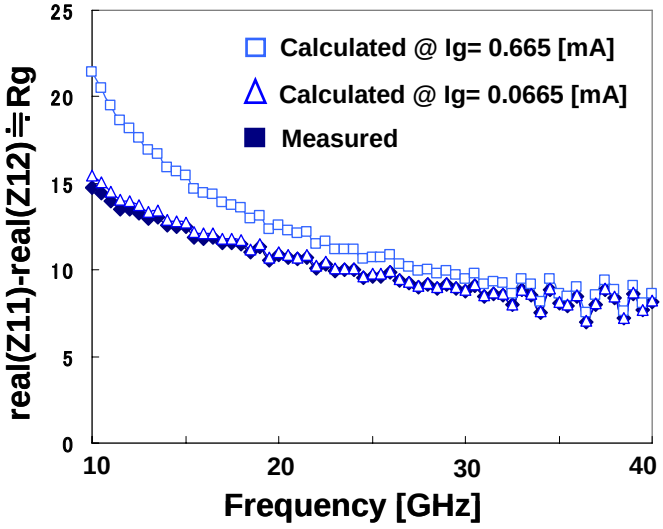


Figure 3.20 Calculated Rg at gate leakage current Ig variety

As figure 3.20 shows, gate leakage component can not be neglected when Ig is 10^{-1} mA order. Moreover the influence is bigger at low frequency region which is under 30 GHz in Figure 3.20. And a little increase of gate leakage current can not be affect to "real(Z11)-real(Z12)". Therefore, the difference of gate leakage current between two devices can not affect to Rg.

3.4.4 f_T and f_{max} in Conjunction with Gate Resistance

Three devices that gate lengths are different (37.8nm, 51.3nm, 58.9nm) were measured. The three devices have same structure, only gate length is different. Number of gate finger is 48, finger length is 2 [um]. EOT is 1.5 [nm]. Gate length dependency of f_T and f_{max} are shown in Figure 3.21.

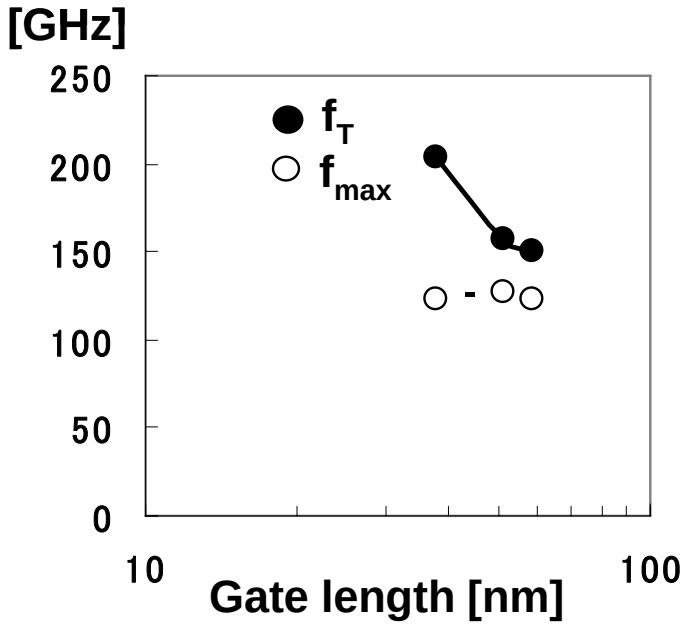


Figure 3.21 Gate length dependency of f_T and f_{max}

f_T is scaled with gate length although f_{max} is not scaled with gate length. This can be thought due to Rg. Gate length dependency of Rg is shown in Figure 3.22.

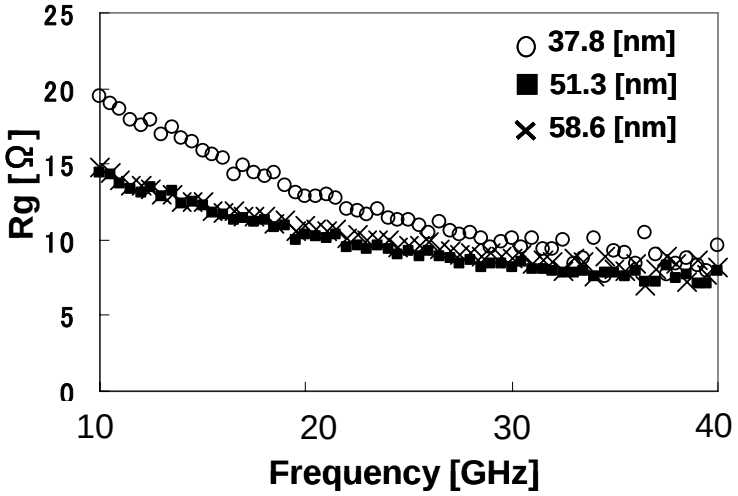


Figure 3.22 Gate length dependency of gate resistance

Although gate resistance Rg is frequency dependent in figure 3.22, trend of gate length dependency of Rg can be seen. Rg of 37.8 nm device is larger than those of the other two devices. It can be said that Rg increases as gate length shrinks. Therefore scaling of gate length does not always cause improvement of f_{max} although f_T is scaled.

3.4.5 Analysis of Gate Capacitance

Gate capacitance is discussed in this section. As mentioned previously, there is a concern that gate capacitance may decline by dielectric dispersion at RF region.

Therefore gate capacitance extracted measured S-parameter is analyzed. How to extract gate capacitance is described as below.

Gate capacitance was extracted at Vg = 1.5 V and Vd = 0 V. At this bias condition, simplified equivalent circuit which represents Z11 is shown in Figure 3.23.

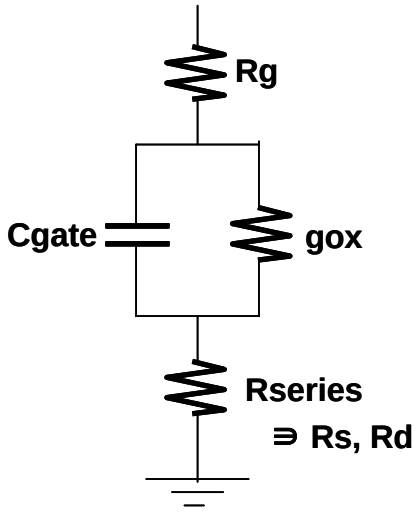


Figure 3.23 Simplified equivalent circuit

Therefore Z11 can be described by Eq. (3.6).

$$Z11 = Rg + Rseries + \frac{1}{j\omega Cgate + g_{ox}} \qquad (3.6)$$

Then Cgate can be extracted by de-embedding Rg and Rseries at Eq. (3.7),

$$Cgate = \frac{imaginary\left\{(Z11 - Rg - Rseries)^{-1}\right\}}{\omega} \qquad (3.7)$$

At Eq. (3.3), supposing g_{ox} can be neglected,

$$Rg = real(Z11) - real(Z12)$$
$$Rseries = Rd + Rs = real(Z22) \qquad (3.8)$$

Extracted gate capacitance based on Eq. (3.7) is shown in Figure 3.24.

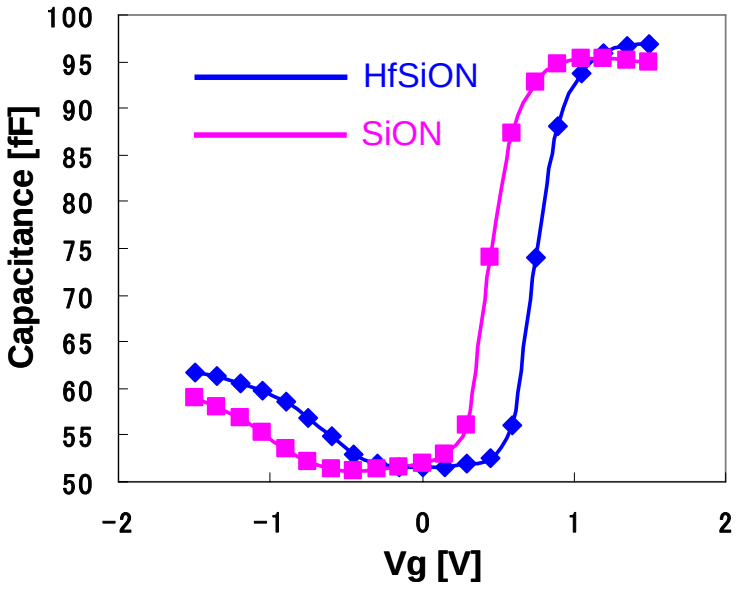


Figure 3.24 C-V characteristics @ 10GHz

As mentioned at DC modeling section, there is difference of threshold voltage between two devices. As Figure 3.24 indicates, the difference on Vth can be seen. The leading edge of capacitance corresponds to the Vth on both devices. Moreover capacitances at strong inversion region almost fit in because two devices have same EOT.

Extracted capacitance value up to 40 GHz is shown in Figure 3.25.

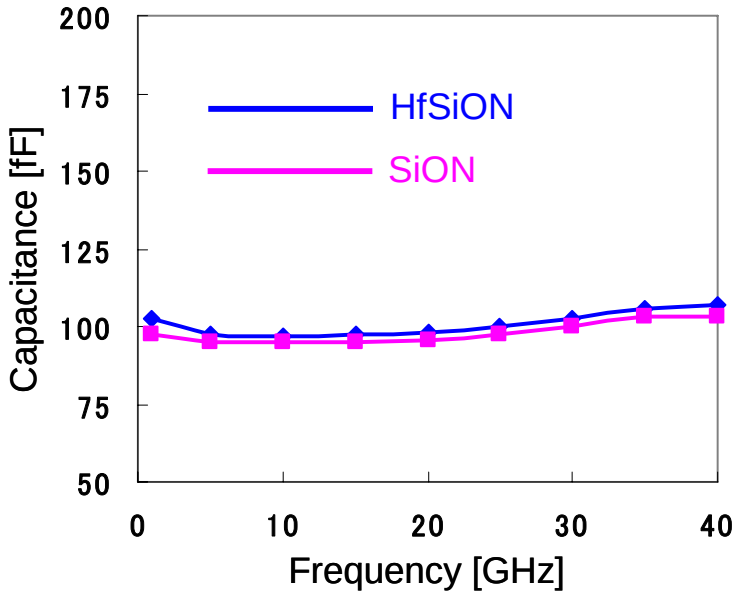


Figure 3.25 Extracted capacitance at wide-ranging frequency

As Figure 3.25 indicates, capacitance value is constant up to 40 GHz on both devices. It means that capacitance degradation caused by dielectric dispersion does not arise up to 40 GHz. At this point of view, the concern which high-k is not high-k at RF region is denied.

Chapter 4

Exploration for Optimum Device Structure

In this chapter, minimum noise figure and distortion behavior of conventional MOSFET which have silicon oxidation membrane are mainly analyzed. What is focused on is device structure which means gate finger length and how to arrange gate finger. In consequence, optimum device layout is examined.

4.1 Device structure

Figure 4.1 shows plane figure of analyzed device.

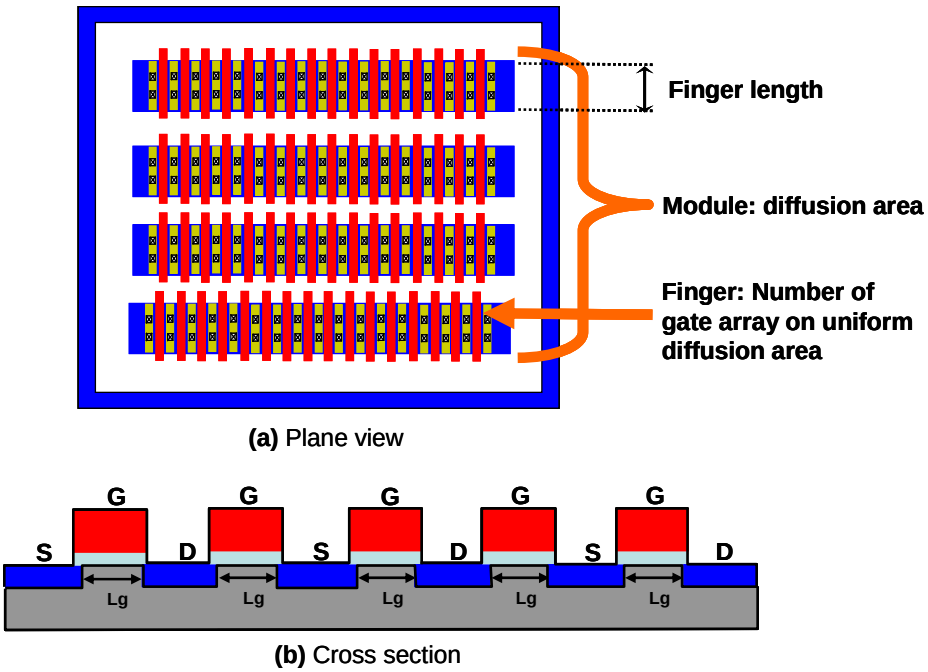


Figure 4.1 Device strucutre

Module means diffusion area; number of module is 4 in figure 4.1. Finger and finger length is same definition in chapter 3; number of finger represents number of gate array on uniform diffusion area, finger length represents unit gate array length. Gate insulator is conventional silicon oxidation membrane. Multi gate finger device has various parameters as just described. Among various parameters, finger length is focused on. As finger length is varied, RF analysis is performed.

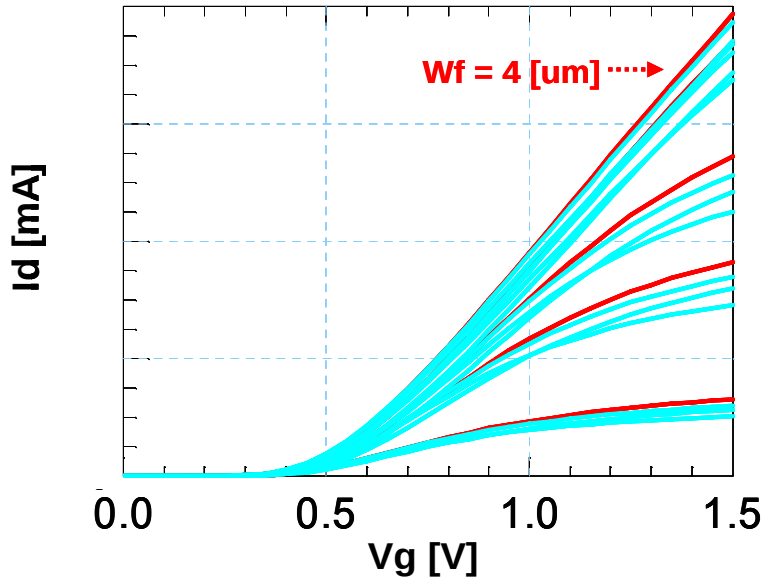
Finger length variety is shown in Table 3.4. Gate length is 0.18 [um], gate width is constant at 160 [um] on all devices.

Table 3.4 Device List

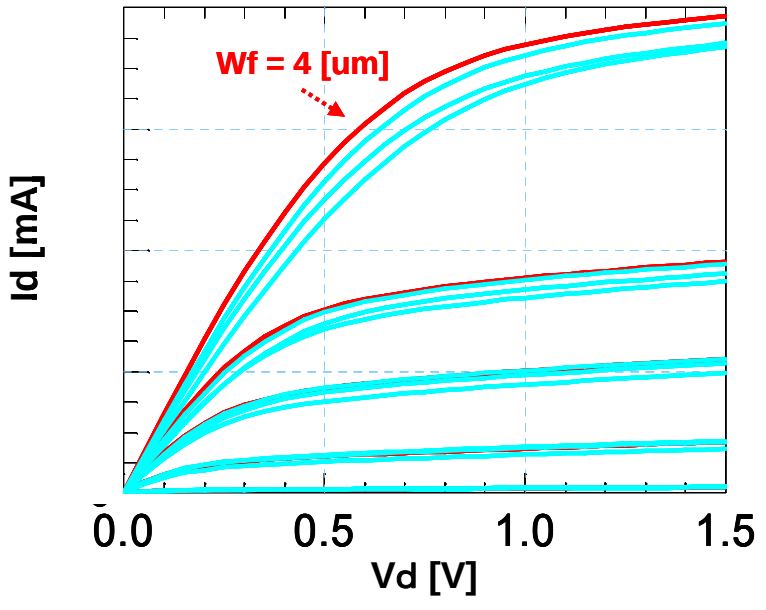
Wf [um]	Number of Finger	Number of Module
1	40	4
1.25	32	4
2	20	4
2.5	16	4
4	10	4
5	8	4
8	5	4
10	4	4
20	2	4

4.2 DC characteristics

Dc characteristics when finger length Wf is varied are shown in Figure 4.2.



(a) Id-Vg characteristics at various Wf



(b) Id-Vd characteristics at various finger length

Figure 4.2 DC characteristics at various Wf

It can be seen that there are a little difference among each DC characteristics at various finger length although total gate width is same. This is due to the difference on wiring resistance. At the assumption that gate width is constant, as finger length Wf increases wiring resistance decreases as shown in Figure 4.3.

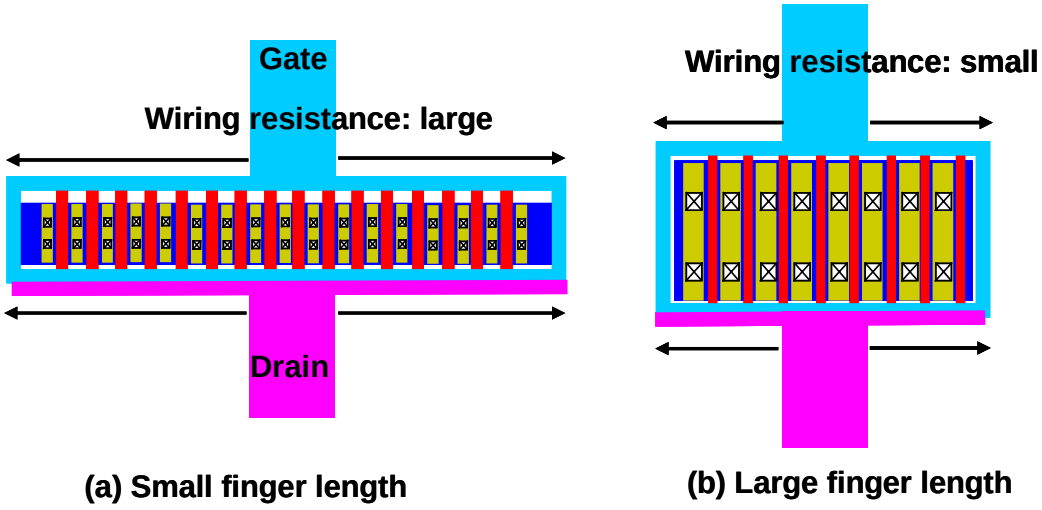


Figure 4.3 Relation with wiring resistance and finger length from plane view

Therefore finger length Wf, by decreasing which gate resistance can be decreased, trades off with wiring resistance which represents the resistance from gate pad to gate finger. This means that there is optimum finger length. In figure 4.2, DC characteristics at Wf = 4[um] has largest drain current among 9 devices.

Actually, resistance (Rd, Rs) in array is extracted from DC characteristics. How to extract is fitting simulation data with measured data optimizing Rd and Rs which are embedded to intrinsic BSIM model of MOSFET as sub circuit. Figure 4.4 shows the concept of intrinsic MOSFET and Rd and Rs as extrinsic components.

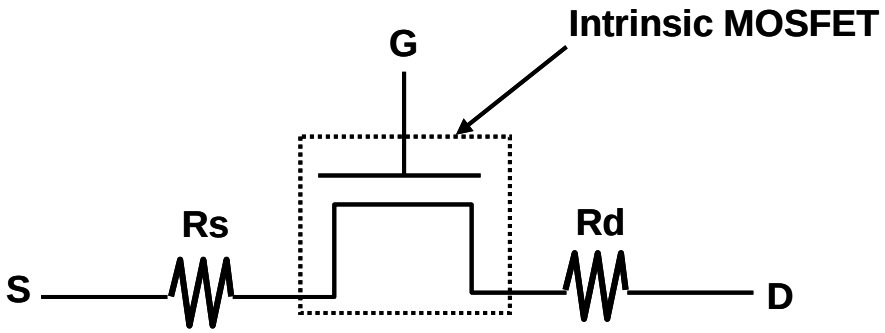


Figure 4.4 Illustration with intrinsic MOSFET and Rd and Rs

Simulation data by only intrinsic MOSFET model is shown in Figure 4.5. Moreover optimized simulation data when Rd and Rs as sub-circuit components are embedded as figure 4.4 shows is shown in Figure 4.6.

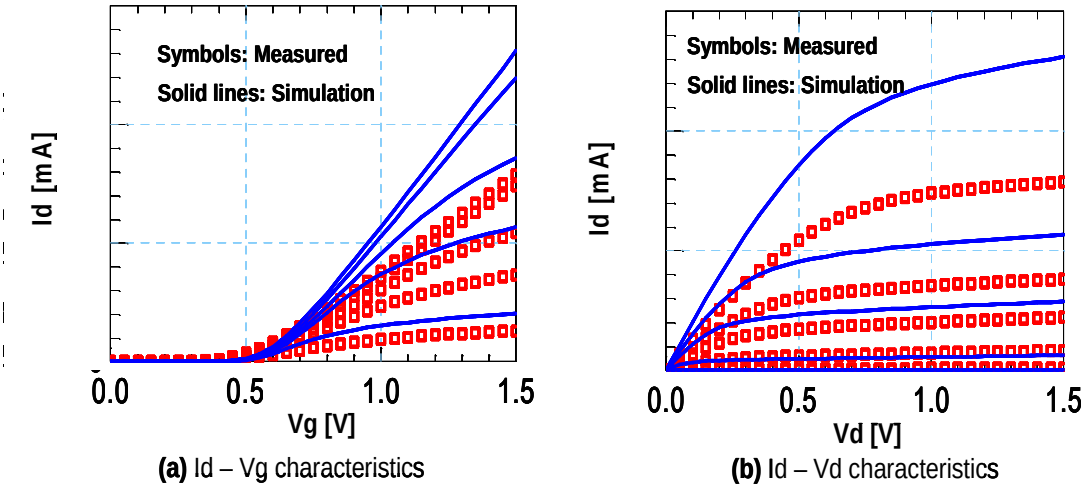


Figure 4.5 Intrinsic MOSFET model

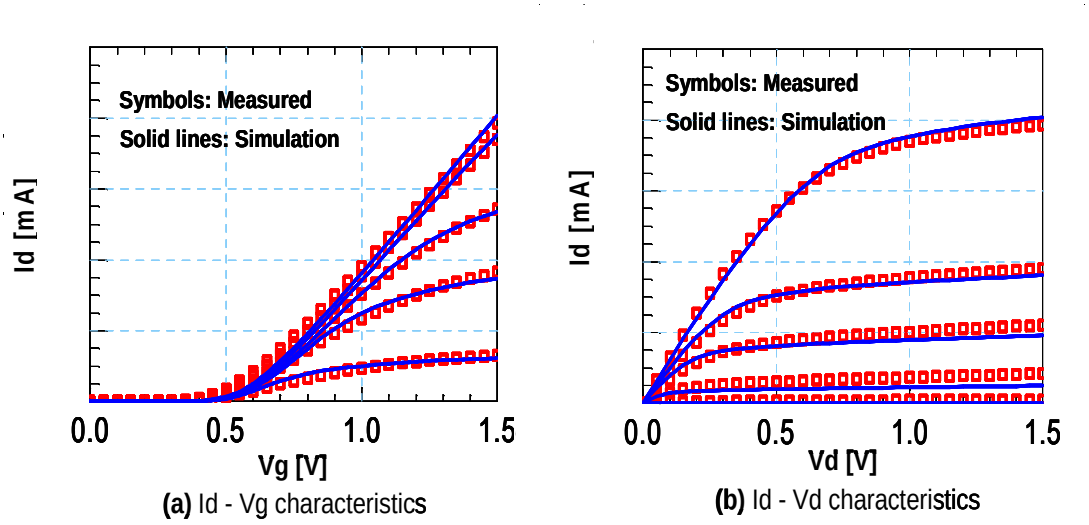


Figure 4.6 After embedding extrinsic components

After embedding Rd and Rs simulation data fits well. In this way, the extracted value of Rd and Rs by fitting to measured data is shown in Figure 4.7.

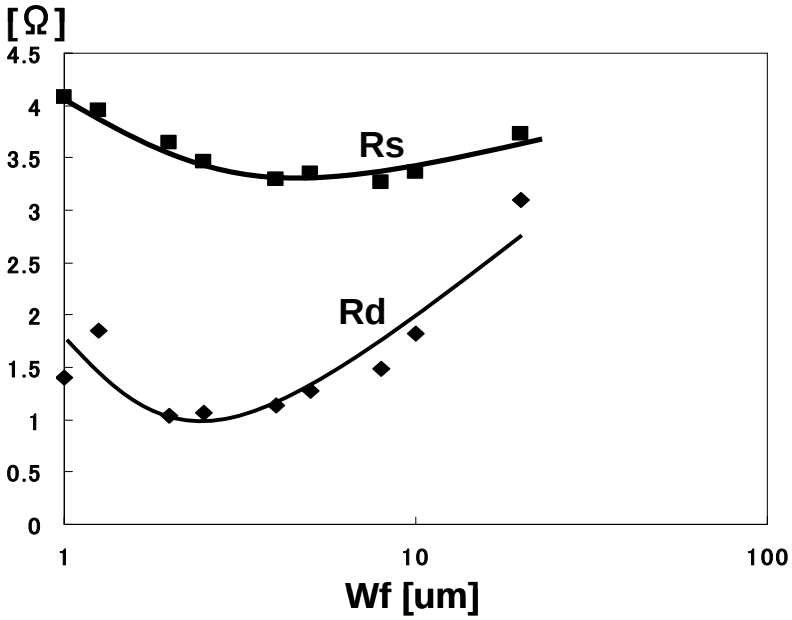


Figure 4.7 Finger length dependency of Extracted Rd and Rs

As Figure 4.7 indicates Rd and Rs have minimum point. The Value of Rd and Rs of the device of Wf = 4 [um] which have best performance on DC characteristics among 9 devices is lower. On the contrary, those of the device of Wf = 20 [um] which have worst performance among 9 devices is larger. At Vg=Vd=1.5 V, the drain current value of Wf=20 um device deteriorated by 6.5 % in comparison with that of Wf =4 um device. Figure 4.8 shows the comparison with best case and worst case.

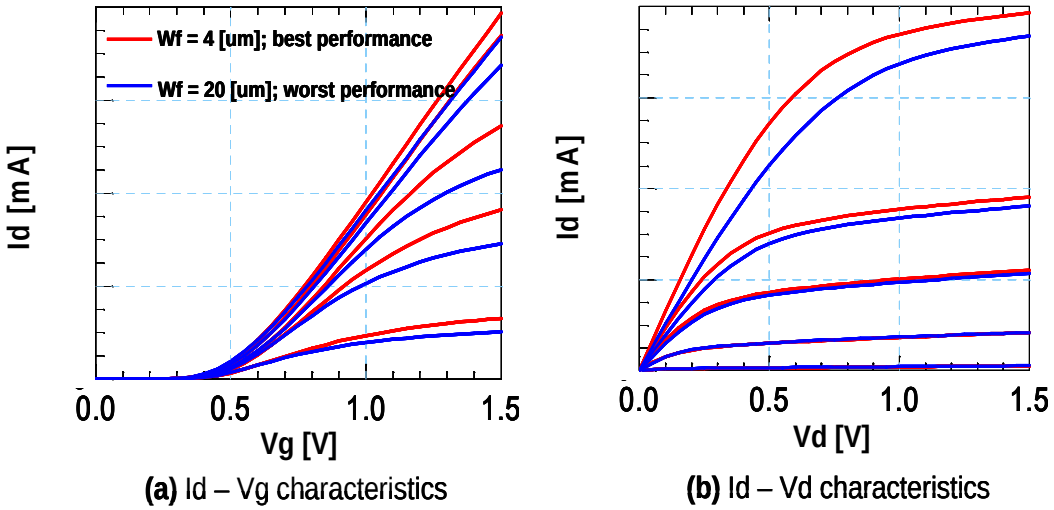


Figure 4.8 Comparison with best case and worst case

4.3 RF Characteristics

4.3.1 Finger Length Dependency of f_T and f_{max}

f_T and f_{max} when finger length are varied were extracted from measured S-parameter up to 40 GHz. Figure 4.9 shows drain current dependency of f_T and f_{max} when finger length are varied.

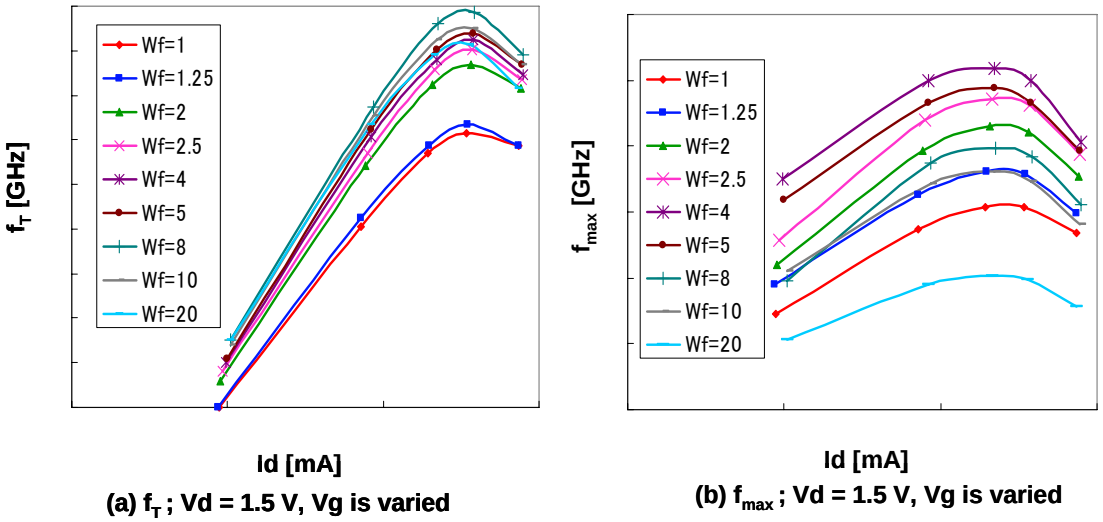


Figure 4.9 Finger length dependency of f_T and f_{max}

f_T and f_{max} are fluctuant depending on Wf although total gate width is constant. As for f_T, when Wf = 1, 1.25 um the value is very low in comparison with the other devices. The other values is not so fluctuant depending on Wf. As for f_{max}, when Wf = 20 um, the value is very low and when Wf = 4 um, the value is largest. About 2.5 times improvement was seen in the value of f_{max} of Wf=4 um device in comparison with that of Wf=20 um device.

4.3.2 Noise Characteristics

The measured NF_{min} (minimum Noise Figure) and Gav (Available Gain) on Wf = 2.5 um at different bias condition is plotted in figure 4.10. Measurement frequency is 5 GHz and 10 GHz.

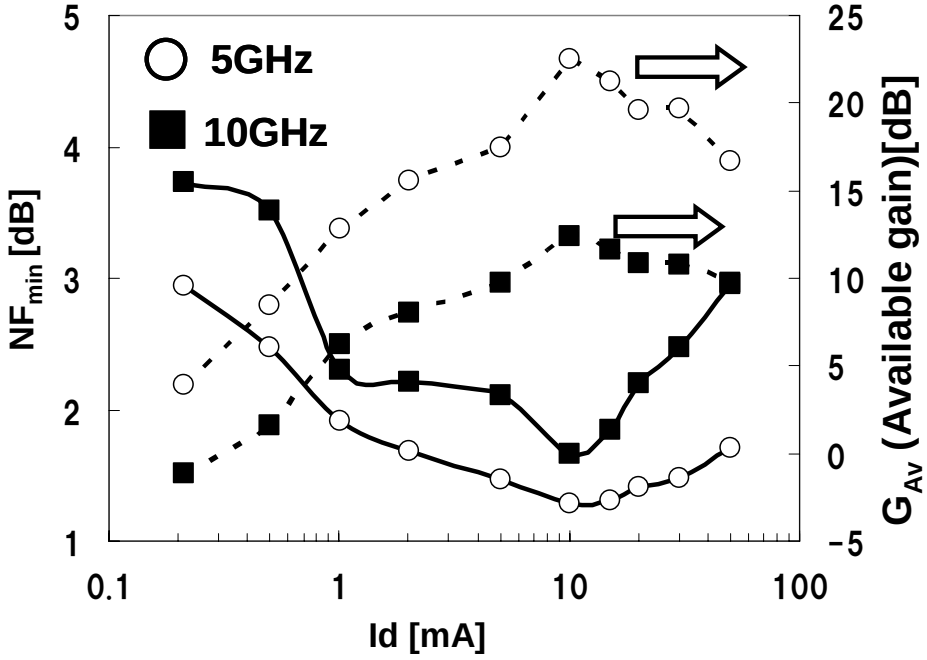


Figure 4.10 Noise Figure and Available gain versus drain current

Bias dependency of NF_{min} and Gav can be seen. Minimum value of measured NF_{min} is 1.29 @5GHz, 1.66 @10GHz at Vg=0.631 V, Vd=1.5 V. Moreover figure 4.10 indicates that as Gav increase, NF_{min} can be minimized. NF_{min} can be minimized when Gav become maximum. To conquer noise, gain of device needs to be large.

NF_{min} and gate resistance Rg are plotted in Figure 4.11. Rg was extracted by using Rd and Rs optimized at DC characteristics[12].

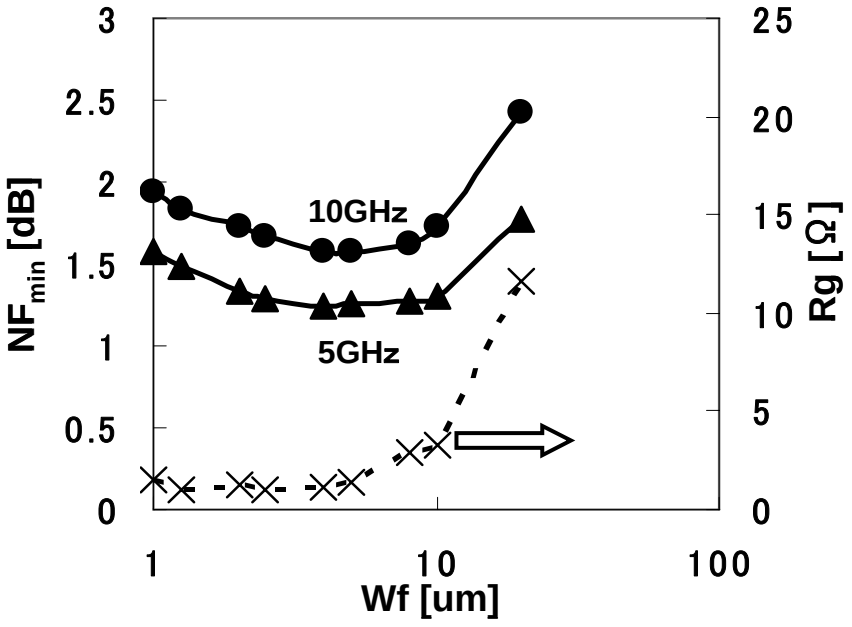


Figure 4.11 Gate length dependency of NF_{min} related with Rg

NF_{min} are also fluctuant depending on Wf. The value of NF_{min} at Wf=4 um is lowest. With the object of f_{max} and NF_{min}, it can be said that Wf=4 um is optimum finger length. And Figure 4.11 indicates that NF_{min} responds to Rg. Minimizing gate resistance leads to not only f_{max} improvement but also NF_{min} improvement.

Chapter 5

Conclusions and Future Issue

5.1 Conclusion

In this study, RF performance of high-k MOSFET and finger length varied multi finger MOSFET for next generation were analyzed based on extracted parameters.

As for high-k MOSFET, the f_T and f_{max} over 100 GHz were gotten on both devices, however, HfSiON device has lower f_T and f_{max} in comparison with SiON device. As for f_T, it is due to the difference of DC characteristics, mainly transconductance g_m. And scaling of device geometry causes the improvement. As for f_{max}, on the other hand, the difference of gate resistance affects to the f_{max} of two devices. And scaling does not always cause the improvement. Therefore it can be said that improvement of g_m and minimizing gate resistance leads to the improvement of RF performance. Moreover, RF analysis relating with gate leakage current was performed. In consequence, it was confirmed that gate leakage current does not affect to RF performance although there are 2 column difference on gate leakage current between HfSiON device and SiON device. It also can be said that low gate leakage current which is the merit of high-k device can not improve RF performance. However, low power consumption by the merit is very significant in RF circuits. In addition, fitting at DC was performed. Simulation data by BSIM fitted with measured data well. The values of mobility from optimizing was over 300 [cm^2/Vs] on both devices. Mobility degradation of high-k MOSFET was seen so much on these devices. And gate capacitance analysis at RF region was performed. In terms of the concern; degradation of insulator capacitance at RF region by dielectric dispersion, it was confirmed that the capacitance was constant

even if at RF region. As noted above, high-k MOSFET has potential ability at RF region.

As for discussion about gate finger structure, it was confirmed that Wf=4 um is optimum length at total gate width 160 um from the perspective of DC performance and f_{max}. This is due to the wiring resistance in gate array. In addition, NF_{min} also has optimum point depending on finger length and the relation with gate resistance was able to be seen.

5.2 Future Issue

As future issue, RF modeling needs to be performed. In this study DC modeling was performed. However, high-accuracy RF modeling is necessity for RF circuit simulation and RF circuit designing. Moreover, more accurate equivalent circuit is needed, although simplified equivalent circuit was adopted in this study. By doing this MOSFET performance can be figured out more precisely. And dielectric dispersion does not occur up to 40 GHz at gate insulator with small-signal in this study, however, large-signal analysis needs to be performed. As for Noise characteristics, more thorough analysis is needed including noise de-embedding. These leads to more exactly understanding for RF performance of next generation device and RF application of scaled CMOS including high-k device.

References

[1] Semiconductor Industry Association, et al., "*International Technology Roadmap for Semiconductors"* (ITRS)," 2003 Edition.

[2] P.R.Gray and R.G.Meyer, *"Future Directions in Silicon IC for RF Personal Communications,"* in Proc.*IEEE Custom Integrated Circuits Conference*, pp. 83-90, May, 1995.

[3] A.Abidi, *"Low-Power Radio-Frequency IC's for Portable Communications,"* in Proc.*IEEE*, vol.83, no.4, pp. 544-569, 1995.

[4] Semiconductor Industry Association, et al., "International Technology Roadmap for Semiconductors (ITRS)," 2005 Edition.

[5] E.Morifuji, H.S.Momose, T.Ohguro, H.Iwai, et al., *"Future perspective and scaling downroadmap for RF CMOS," Symp. VLSI Technology*, pp.163-164, 1999.

[6] H.Sauddin, *"Low-Frequency (1/f) Noise of NMISFET with La2O3 High-k Gate Dielectrics and Analysis of Electrical Properties of Ultra-Shallow p+/n Junctions Formed by Plasma Doping Method," Master thesis*, Feb, 2005.

[7]Y.Tominaga, *"Fundamental of Dielectric Dispersion and Physics of Microwave Domain"* in http://atom11.phys.ocha.ac.jp/ftp/pub/lecture/dielectric_relaxation.pdf

[8] C. J. F. Bottcher and P. Bordewijk, "*Theory of electric polarization*," vol. II. Elsevier, second ed., 1978.

[9] M.C.A.M.Koolen, J.A.M.Geelen, and M.P.J.G.Versleijen, *"An improvement deembedding technique for on-wafer high-frequency characterization,"* in Proc.*IEEE Bipolar Circuit Technology Meeting*, 1991, pp. 191-194.

[10] C.H.Chen and M.J.Deen, *"A general noise and S-parameter deembedding procedure foron-wafer high-frequency noise measurements of MOSFETs," IEEE Trans. Microw. Theory Techniques*, vol.49, no.5, pp.1004-1005, May 2001.

[11] H.Cho and D.E.Burk, *"A three-step method for the deembedding of high frequency Sparameter measurements," IEEE Trans. Electron Devices*, vol.38, no.6, pp.1371-1384, Jun 1991.

[12] Y.Cheng, M.J.Deen and C.H.Chen, *"MOSFET Modeling for RF IC Design," IEEE Trans. Electron Devices*, vol.52, no.7, July. 2005.

[13] A.F. Tong, K.S. Yeo, L. Jia, C.Q. Geng, J.-G. Ma and M.A. Do, *"Simple and accurate extraction methodology for RF MOSFET valid up to 20 GHz,"* IEEE Proc.-Circuits Devices Syst., Vol. 151, No.6,December 2004

[14] Jin, X., Ou, J.-J., Chen, C.-H., Liu, W., Deen, M.J., Gray, P.R., and Hu, C.: *"An effective gate resistance model for CMOS RF and noise modeling"*. Technical Digest of International Electron Devices Meeting, Dec 1998, pp. 961–964

[15] Cheng, Y., Chen, C.H., Enz, C., Matloubian, M., and Deen, M.J.: *'MOSFET modeling for RF circuit design'*. Proc. 3rd IEEE Int. Caracas Conf. on Devices, Circuits and Systems (ICCDCS 2000), Cancun, Mexico, Mar 2000, pp. D23/1–8

[16] Cheng, Y.H.: *'MOSFET modeling for RF IC design'*, Int. J. High Speed Electron Syst., 2001, 11, (4), pp. 1007–1084

[17] Y.Cheng et al., "*A Physical and scalabel BSIM3v3 I-V Model for Analog/Digital Circuit Simulation,*" *IEEE Trans. Electron Devices*, vol.44, pp.277-287, Feb, 1997.

[18] C.Hu *et al*, "BSIM3v3.2.2 MOSFET Model User's Manual," Univ. California Berkeley, 1999.

[19] M.Kang, I.M.Kang, and H.Shin, "Extraction and Modeling of Gate Electrode Resistance in RF MOSFETs,," in *IEEE Int.Conf.Integrated Circuit and Technology*, pp.207-210, 2005

[20] Y.Cheng, "MOSFET Modeling for RF IC Design," *Int. J. High Speed. Electron. Syst.*, vol.11, no.4, 2001.

[21] T.Matsuoka, “VLSI summer school ～ CMOS RF circut session ～,” in *http://www6.eie.eng.osaka-u.ac.jp/reference/VLSI summer20050817.pdf* , 2005.

[22] Noboru Ishihara and Toshihiko Shimizu, “*A Simple Equation Model for RF MOSFET*,” Silicon Monolithic Integrated Circuits in RF Systems, 2006,Jan.2006

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