Master Thesis

Thermal Stability of NiSi Improved by Post Silicidation Metal Doping Method.

Supervisor

Professor Hiroshi Iwai

Iwai Laboratory

Department of Electronics and Applied Physics,

Interdisciplinary Graduate School of Science and Engineering

Tokyo Institute of Technology

05M36387

Koji Nagahiro

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【Chapter 1】 Introduction

1.1 Advance of MOSFET

Recently, it is not too much to say that electronic device is used for every product. Especially, the product of Information Technology (IT) such as computers and cellular phone improves the quality of our life, and will surely continue to make our life more convenient. Therefore, the performances of electronic devices, especially silicon large scale integrated circuits (LSIs), should be progressed very rapidly. It's required for these devices to operate by high speed/frequency and low power consumption more. Now, Complementary Metal-Oxide-Semiconductor Large-Scale Integrated circuits (CMOS LSIs) are the most popular devices for electronics because of their capability for low power consumption. In order to make high performance LSIs, one of the most popular methods is downsizing of components such as Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). Because downsizing reduces capacitance, as a result, high performance and/or low power operation of circuit can be achieved. Furthermore, because downsizing increases the number of components in a circuit, less cost can also be achieved.

The downsizing of MOSFETs has been accomplished by the scaling method as shown in Fig.1.1 and Table1.1 [1]. To increase the drive current and to control the short channel effects, these scaled transistors have to be designed very carefully. In this method, lateral and vertical dimensions and supply voltage are scaled down by the same factor S, while impurity-doping concentration is increased by the factor S.

And as a concrete target, ITRS (International Technology Roadmap for Semiconductors) projection in the MOSFET and front-end process areas are driven by the overall chip requirement for design, speed, power dissipation, functional density, cost, lithography, etc. It should be noted that the trend of the down-scaling has been accelerated by every update of the ITRS, because of the very severe competitions between the rival LSI produces for high performance device, such as high clock

frequency operated microprocessors. In order to realize such high performance microprocessors, downsizing of the gate length becomes the most important issue.

For high-performance logic, physical gate length and EOT (Equivalent Oxide Thickness) value will decrease each year as shown in Table 1.2, where the data is reported by ITRS [2].

Lately a lot of researches for miniaturization of MOSFET are being made all over the world. It is important to find out the possibilities of technological advancement of MOSFETs for high performance LSI system.

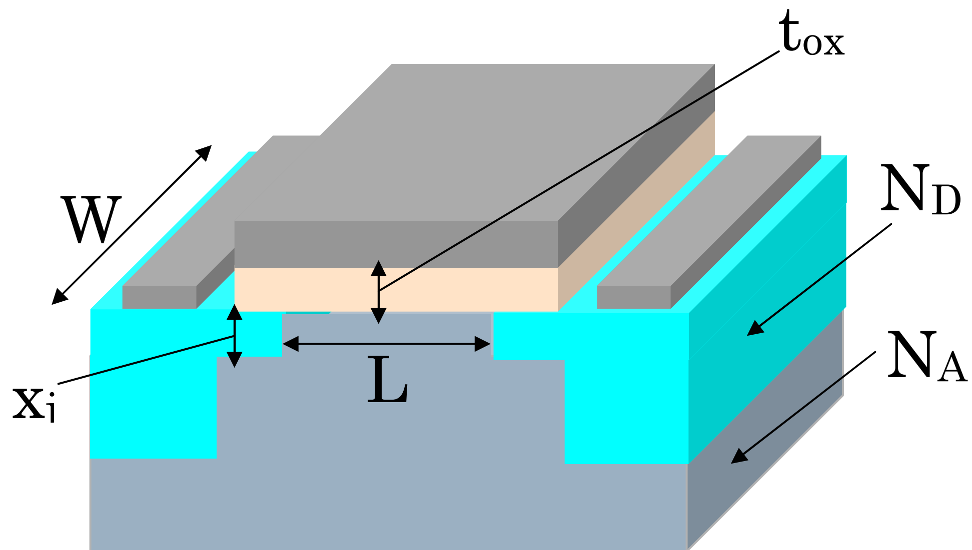


Fig.1.1 The image of MOSFET

Table1.1 Scaling of MOSFET by the scaling factor S.

Quantity	*Before Scaling*	*After Scaling*
Channel Length	L	L/S
Channel Width	W	W/S
Device Area	A	A/S^2
Gate Oxide Thickness	t_{ox}	t_{ox}/S
Gate Capacitance (unit area)	C_{ox}	$S*C_{ox}$
Junction Depth	x_j	xj/S
Power supply voltage	V_{DD}	V_{DD}/S
Threshold Voltage	V_{T0}	V_{T0}/S
Doping Concentration	N_A	$S*N_A$
	N_D	$S*N_D$

Table 1.2 High-performance Logic Technology Requirements

Year of Production	2005	2007	2010	2013	2015
DRAM 1/2 Pitch (nm)	90	65	45	32	25
Physical gate length (nm)	32	25	18	13	10
EOT (Å)	12	11	6.5	5	5
Gate Poly Depletion and Inversion-Layer Thickness (Å)	7.3	7.4	2.7	4	4
Gate leakage current limit (A/cm^2)	1.88E+2	8.00E+2	1.56E+3	2.23E+3	3.70E+3
Nominal power supply Voltage (V)	1.1	1.1	1.0	0.9	1.8
Saturation threshold voltage (mV)	195	165	151	167	166
Source/Drain Subthreshold Off-State Leakage Current (μA/μm)	0.06	0.2	0.28	0.29	0.37
effective NMOS Drive Current (μA/μm)	1.02E+3	1.20E+3	2.05E+3	2198	2188
Parasitic source/drain series resistance (.Ω−μm)	180	140	105	75	75

1.2 Limits of Ti or Co silicide as metal gate

The focus is placed on the use of metal silicide for MOS devices in the present article. Today, $TiSi_2$ is major material for MOSFET gate electrode. Silicides can be formed by either a solid-state reaction between a metal and Si, or by co-depositing the metal and Si. As shown in Table1.2, the gate length reached under 100 nm and it becomes hard to use $TiSi_2$. Because, when gate length is decreased below 100 nm, $TiSi_2$ becomes high resistant, high resistant due to thinning of the silicide at the edge of the lines[3] cause not only power consumption up but also the operation delay. Therefore, $TiSi_2$ gate must be replaced with an alternative material, which becomes low resistant silicide as gate length is decreased below 100 nm. Actually, the latest MOSFET gate is used $CoSi_2$. The resistivity and thermal stability of $CoSi_2$ are similar to those of $TiSi_2$. But the sheet resistance of $CoSi_2$ is relatively insensitive to decreasing line width, unlike $TiSi_2$ [4]. In addition, $CoSi_2$ can be used as a diffusion source to form shallow junction [4]. However, due to the relatively high amount of Si consumption when gate length is decreased below 65 nm, $CoSi_2$ becomes high resistant, too.

1.3 Requirements for Ni silicide and Physical properties of it

NiSi (Nickel mono-silicide) is paid to attention as increase of resistivity for narrow line structures is hard to occur comparing to the conventional $TiSi_2$ and $CoSi_2$. In addition, Si consumption during the silicidation is the smallest among the Ti, Co and Ni[6]. And the mechanical stress of the NiSi film on silicon substrate is also the smallest. Contact resistance to p-type silicon, which was a problem for $TiSi_2$, is the smallest due to its lowest barrier high, and that to n-type silicon was found to be also small[7]. Bridging failure between the gate electrode and source/drain hardly occurs for the NiSi as dominant diffusion species is metal. Unlike $TiSi_2$ and $CoSi_2$, NiSi can be formed with a one-step anneal (400-600°C), which provides a simpler silicide process. On the other hand, major concern for NiSi silicide was its low heat resistance due to the phase transition of NiSi to $NiSi_2$ or the local agglomeration of NiSi. In fact maximum allowable process temperature after the silicide is about 700°C. Thus improvement of thermal stability of NiSi is one of the key technologies to realize sub-65nm CMOS. Many approaches of introduction of different materials such as Pt, Pd, Ti, Mo, Co, C, etc. have been studied to control these phenomena and to improve thermal stability of NiSi [6, 8-23].

1. 4 Purpose of the study

In various studies have been investigated, many of methods were addition of other metals or elements. But there were few investigations to compare some additives under the same conditions. In this work, by comparing 4 metal additives in same conditions, we investigated on the mechanism of these additives and discussed from the view point of diffusion control mechanism. Based on this discussion, we propose a new process method named as post silcidation metal doping, PSMD.

So, the purpose of this study is improvement of thermal stability of NiSi by the new process PSMD.

【Chapter 2】 Fabrication process and Characterization Methods

2.1 Fabrication process for Ni silicide

2.1.1 Outline of fabrication process for Ni silicide gate

In this study, I discuss about heat resistance. So I make out not transistor but a part of electrode. Ni silicide is fabricated in the process shown in Fig.2.1. First, n-type silicon(100) substrate is cleaned chemically and dipped by SPM and diluted HF. After that, Second, Ni and Hf layers are deposited directly on the substrate by magnetron sputtering method, in which base pressure is less than 5 x 10^{-6} Pa. And N is deposited by reaction sputtering and by radical sputtering system. Layered structures are Ni/Si, Ni/Hf/Si, Hf/Ni/Si, NiN/Si. and N/Ni/Si. Vacuum of the growth chamber is around 7 x 10^{-1} Pa while deposition. Third, samples are annealed with rapid thermal annealing (RTA) for 60 seconds in Forming Gas (which is prepared with N_2 and H_2 in the ratio of 97: 3) ambient at 400 - 600 degrees. At the last, samples are measured by characterization methods.

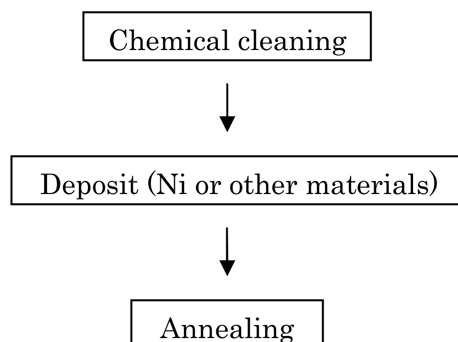


Fig. 2.1 Flowchart of fabrication process for Ni silicide gate

2.1.2 Chemical cleaning of silicon substrate and chemically oxidation

High quality thin films require ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

In this study, n-type Si wafer whose surface lattice plane is (100) is used. The sheet resistance of this n-Si-wafer is from 1 to 5 Ω/cm^2.

Fig. 2.2 shows the flowchart of Si-substrates cleaning. After the cleaning of Si-substrate by running DI (de-ionized) water for 10 minutes, contaminants such as organic substances on the surface are eliminated by SPM (which is prepared with 96%-H_2SO_4 and 30%-H_2O_2 in the ratio of 4: 1) for 5 minutes. After the cleaning by ultra-pure water for 10 minutes again, native SiO_2 layer of the surface is eliminated with diluted HF of 0.5% for 5 minutes. If native SiO_2 layer is lost, water repellence will appear in a substrate. Finally, the substrate is rinsed with ultra pure water for 5 seconds.

	Time	Purpose
Ultra-pure water	10 min.	
⇓		
SPM (96%-H_2SO_4 : 30%-H_2O_2 = 4 : 1)	5 min.	Elimination of organic substance
⇓		
Ultra-pure water	10 min.	
⇓		
0.5%-HF	5 min.	Elimination of SiO_2
⇓		
Ultra-pure water	5 sec.	

Fig. 2.2 Flowchart of chemical cleaning of Si-substrate and chemically oxidation

After cleaning, the substrate is immediately put into the loading chamber of sputtering equipment so as to avoid the growth of SiO_2.

2.1.3 A magnetron sputtering system

Sputtering is the phenomenon that a high potential particle goes to the surface of target gives momentum to the atom of target by elasticity conflict, and rebound atom conflict around atoms again, in short the atom of the surface of target discharge, and the atom discharged accumulates on the wafer. Fig. 2.3 shows the principle of sputtering. Sputtering is strong stick power of film and able to use the high melting point material and able to form the film is nearly equal with target. Generally, sputtering is plasma generate at electric discharge space by glow discharge between electrodes. Sputter plus (positive) ion in plasma is accelerated by potential fall around the electrode, and conflicts the surface of the target cathode, and sputter the surface of the target. A sputter particle deposits on the wafer established on the anode and forms thin film make of the target.

In the case of D.C. sputter, by using a high frequency power, glow discharge continue at the surface of the insulator target for that an ion and electron alternately conflict to the surface of it. For that mobility of an electron in plasma is larger than it of an ion, an excess electron accumulated on the surface of the insulator target, and we are able to sputter by the insulator target to bias the surface of it to minus potential by direct current. So by sputter equipment with a high frequency glow discharge every material can become thin film. [24]

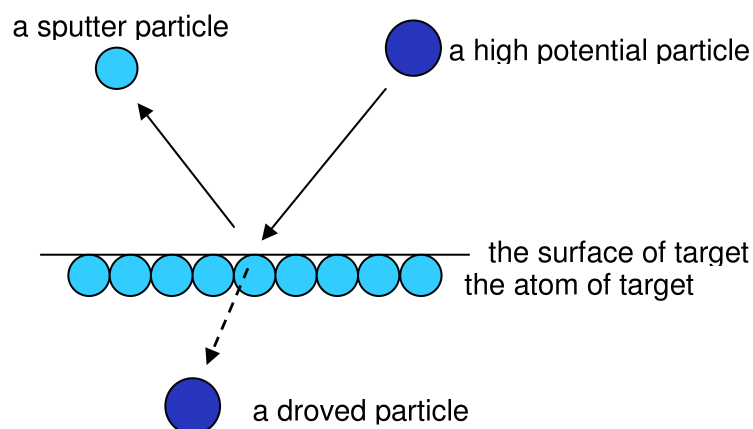


Fig. 2.3 the principle of sputtering

Fig. 2.4 shows sputter equipment. It is mainly composed of sputtering room, substrate exchange room, exhaust system, gas introduce system, and sputtering power. In this study, sputter gas is Ar of 99.999% but with N_2 of 99.999% in time of reaction sputtering. Through sputtering in sputtering room gas pressure is about 7.0*10^-1 Pa. In D.C. power unit, maximum output is 1000 W. In this study D.C. power is 150 W and the height from target to wafer is 150 mm and target is Ni of 99.99% and Hf of 99.99??%.

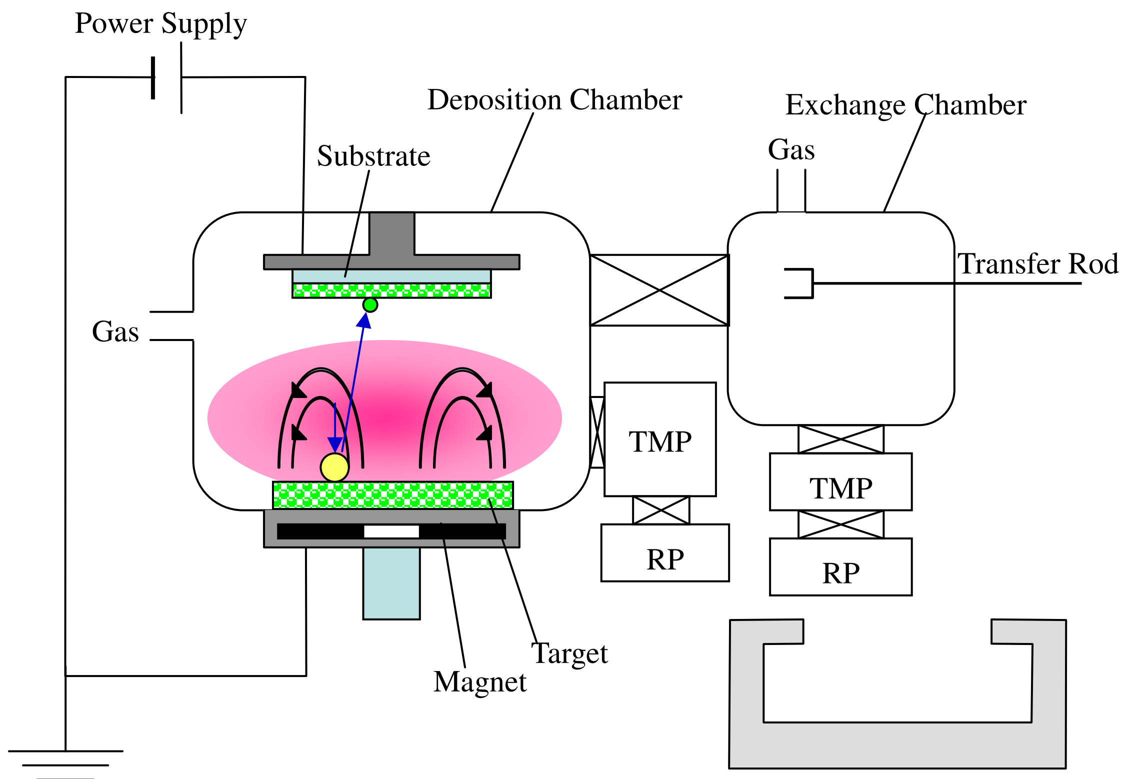


Fig. 2.4 sputtering system which is used in this study

2.1.4 Rapid Thermal Annealing (RTA)

After the deposition, samples are annealed by Rapid Thermal Annealing (RTA) equipment shown in Fig.2.6. This RTA system has an infrared lamp to heat sample in heating furnace. The furnace temperature is able to be raised to 1700 degrees centigrade. Rate of increasing temperature is 100 degrees/sec at a maximum. This RTA system is connected to pump and gas line to N_2, O_2 and Forming Gas (which is prepared with N_2 and H_2 in the ratio of 97: 3) gas cylinders. The furnace cannot be vacuumed prior to the gas running. Due to this system, the remaining air or moisture of the furnace cannot be completely replaced by the gas, although its content is assumed to be extremely small and gas concentration in heating furnace is kept nearly the concentration in the gas cylinders. In this study, the annealing process is operated (Annealing is carried out) in F.G. (Forming Gas) ambient by respective running gas into the furnace of which flow rate are about 1.0 l/min (and?) by two step annealing. First, temperature rise to 150 degree for 60 seconds. And the temperature keeps for 10 minutes. Second step is temperature rise to a target temperature (600 - 750 degrees) by 10 degrees/sec. And the temperature keeps for 60 seconds. After that, it is cooled down by the ability of machine.

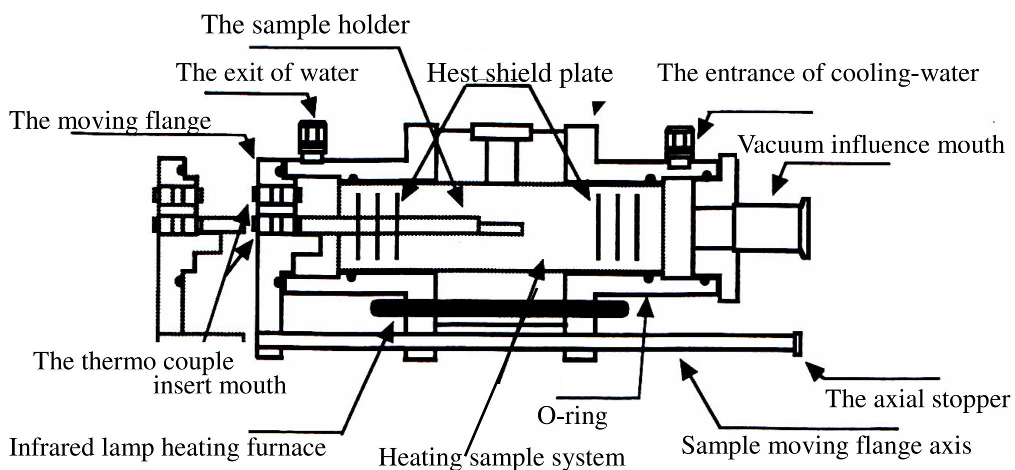


Fig. 2.6 Schematic overview of RTA system

2.2 Characterization Methods

2.2.1 Measurement of Electric Characteristics

Samples were analyzed by the four-point probe method, and as necessary by Atomic Force Microscopy (AFM), scanning electron microscopy (SEM), Transmission Electron Microscope (TEM), Rutherford backscattering spectroscopy (RBS), X-ray Diffraction (XRD), Raman Spectroscopy and Auger Electron Spectroscopy (AES).

To know the temperature of exchange from low resistance to high resistance, I used the four-point probe method. To know the surface morphology it mainly shows to be agglomeration, I used SEM and AFM. TEM was used to know not only surface but also interface morphology it mainly shows the state of silicidation at interface. To identify material, I used RBS, XRD, Raman Spectroscopy and AES. RBS and AES indicate the position of material, too.

2.2.2 4-Point Probe

Four-point probe shown in Fig.2.7 is used to measure sheet resistance of sample. The way to measure sheet resistance (R_s) is shown below. At first, a small current (I) is applied between probe A and probe D. And next, the potential difference between probe B and probe C (V) is measured by voltmeter. If the specing between the probes is mach greater than the film thickness but much smaller than the size of the conducting film, R_s can be calculated by this I and V. R_s is commonly given by

$$R_s = \frac{V}{I} \times C$$

where C is correction factor that depends on the sample geometry. Assuming the length between probe B and probe C is completely smaller than the size of sample, C equals to π/ln2=4.53.

In this study, the radius of curvature of the probe is 40 μm and the length between each probe is 1 mm. And four probes are pressed by the weight of 150 grams when I and V are measured.

Ammeter

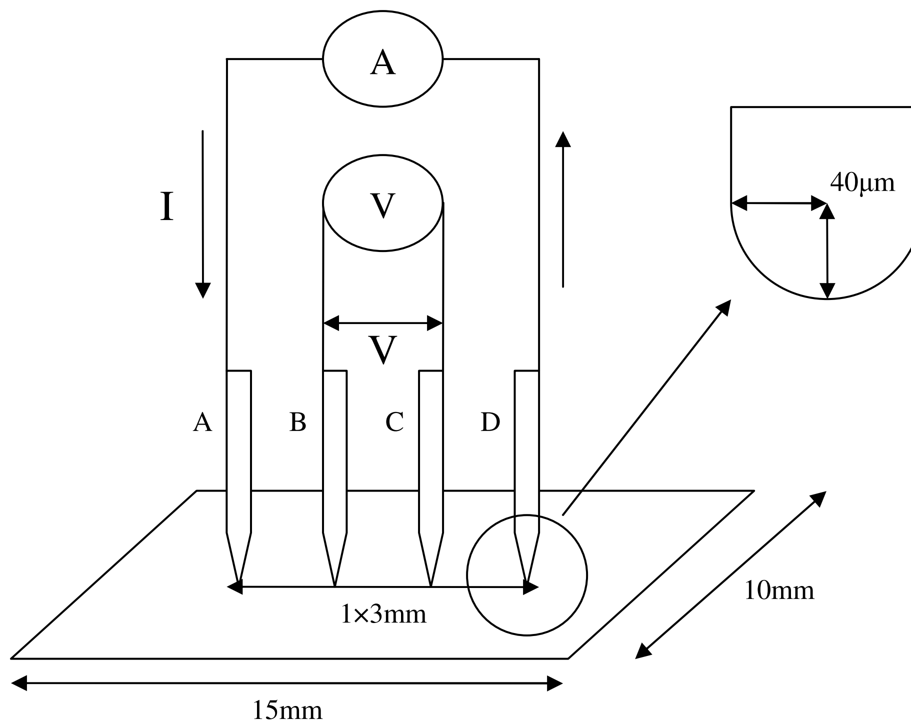


Fig. 2.7 Schematic of four-point probe

2.2.3 Atomic Force Microscopy (AFM)

The roughness of the surface of the film is evaluated by Atomic Force Microscopy (AFM, Nano Scope III, Digital Instrument Co. Ltd.) in tapping mode. AFM is microscopic equipment for observing surface of a sample with high magnification. Fig. 2.10 shows the principle of AFM. As the sample approaches the probe of AFM slowly and the distance between them becomes a certain value, attractive or repulsive force is generated between them. A cantilever to which the probe is attached distorts because of the force. The distortion is detected by a variation of reflection angle of laser beam which is irradiated to the cantilever. The distance is controlled to keep the distortion constant while scanning the surface of the sample with the probe. An image of the surface is obtained by the scanning in x and y directions and the control of the distance in z direction. Spatial resolution of AFM used in this study is around 1.0 nm.

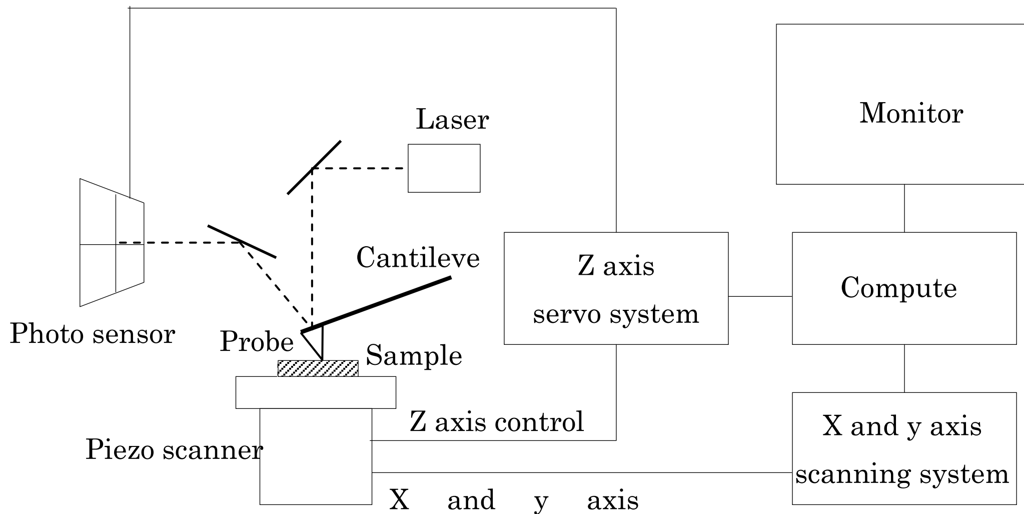


Fig. 2.8 Principle of AFM

2.2.4 Scanning Electron Microscopy (SEM)

SEM is the microscope that electron beam or light generated by being irradiated electron beam stopped down and accelerated by 10000 eV and scanning 2-D to surface of solid detect and amplify and irregularly.

When the electron beam strikes the sample, both photon and electron signals are emitted. Principally low-energy secondaries but also elastically scattered primaries and cathodoluminescence show surface topography. Principally X-ray emission (primary energy -30keV) but also elastically scattered primaries for specimens of low atomic number and sometimes cathodoluminescence show material analysis. Transmitted primaries show specimen thickness. Voltage contrast modulation of low energy secondaries shows electric fields in specimen. Internal currents and voltages show electrical properties of specimen, especially Voltage contrast modulation shows it in semiconductor devices.

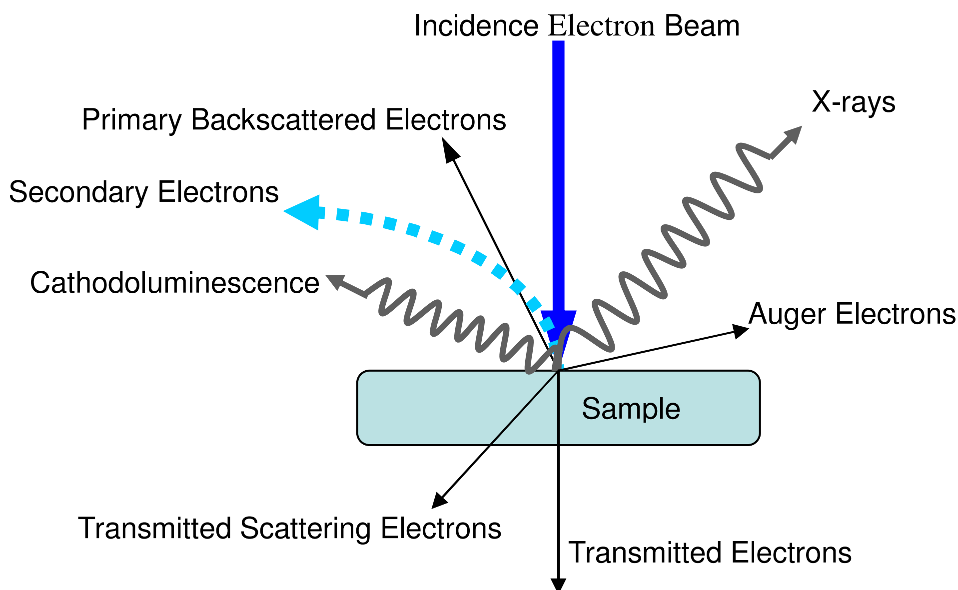


Fig. 2.9 Generation of various signals by incidence beam

SEM was the equipment to observe the surface morphology of sample as electron beams was irradiate to the sample. Focused incidence electron beam was scanned to the surface of the sample, and generated secondary electrons were detected, and for the amount of them converts to signal of brightness, we can see an image of SEM. As secondary electrons of convex area were more than they of concave area, in an image of SEM convex area was bright, and concave area was dark. It means the three-dimensional rough can be shown as a two-dimensional image like a display or picture.

1. The electron beam was irradiated from the electron gun to apply the acceleration voltage.
2. The irradiated electron beam was focused by electron lens.
3. The electron beam was scanned by bias coil and was irradiated to a sample.
4. Secondary Electrons generate from the sample. And it was found by the secondary electrons detector.
5. The amount of secondary electrons converts to brightness of CRT, and the electron beam was synchronized with the scanning of CRT. And the expansion image was displayed.

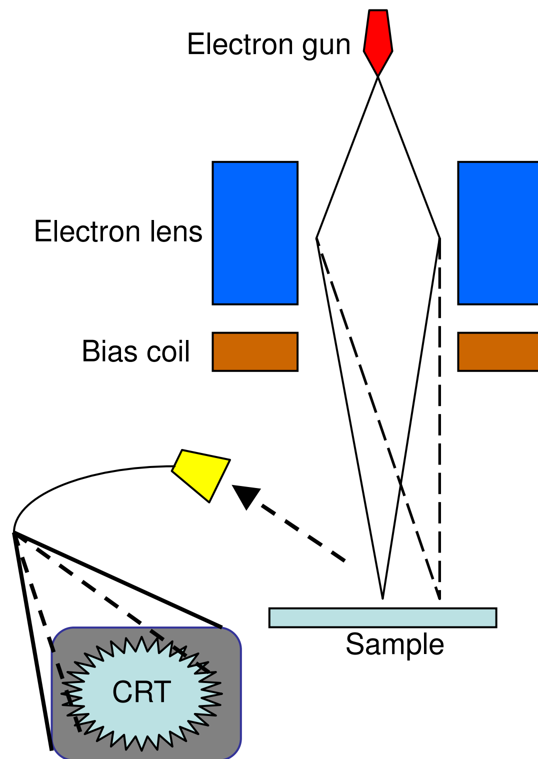


Fig. 2.10 The principle of SEM

2.2.5 Transmission Electron Microscope (TEM)

Cross-section TEM image is the most important analysis method to characterize physical thickness, film quality and interface condition.

Figure 2-4 Shows TEM system. First, focus lenses change convergent angle and beam size. The electron beam transmitted through the thin fragment sample passes objective lens and projective lens, and finally projected on fluorescent screen. Recording oh the image is performed by direct exposure on exclusive film for electron microscope set lower part of the fluorescent screen.

Electron interacts strongly with lattice by scattering. Thus, sample has to be very thin fragment. Required thickness of the sample is 5 to 500 nm at 100 kV. TEM images are obtained in very high resolution such as 0.2 to 0.3 nm at 200 kV.

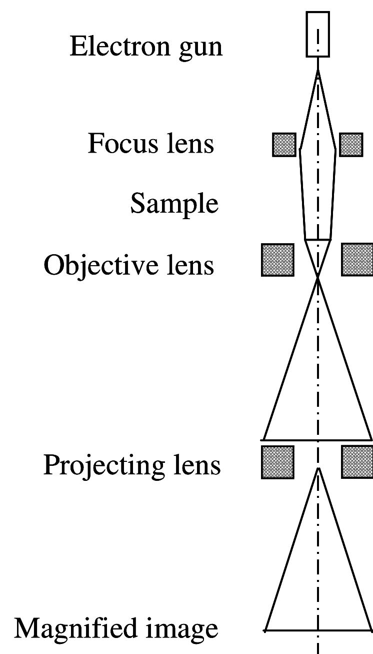


Fig.2.4 A schematic diagram for TEM (Transmission Electron Microscopy) observation. Several magnetic lenses are used to magnify the object image.

2.2.6 Rutherford Backscattering Spectrometry (RBS)

Rutherford backscattering spectrometry (RBS) is based on bombarding a sample with energetic ions-typically He ions of 1 to 3 MeV energy-and measuring the energy of the backscattered ions. It allows determination of the masses of the elements in a sample, their depth distribution over distance from 100 angstrom to a few microns from the surface, and crystalline structure in a non-destructive manner.

Fig.2.11 shows RBS schematic. Ion of mass M_1, atomic number Z_1, and energy E_0 are incident on a solid sample or target composed of atoms of moss M_2 and atomic number Z_2. Most of the incident ions come to rest within the solid losing their energy through interactions with valence elements. The incident ions lose energy, traversing the sample until they experience a scattering event and then lose energy again as they travel back to the surface leaving the sample with reduced energy. For those incident ions scattered by surface atoms, conservation of energy and momentum leads to a relationship of their energy after scattering E_1 to the incident energy E_0 through the kinematic factor K

$$K = \frac{E_1}{E_0} = \frac{\left(\sqrt{1-(R\sin\theta)^2} + R\cos\theta\right)^2}{(1+R)^2} \approx 1 - \frac{2R}{(1+R)^2}(1-\cos\theta)$$

where R= M_1/M_2 and ? is the scattering angle. The kinematic factor is a mesure of the primary ion energy loss. The unknown mass M_2 is calculated from the measured energy E_1 though the kinematic factor.

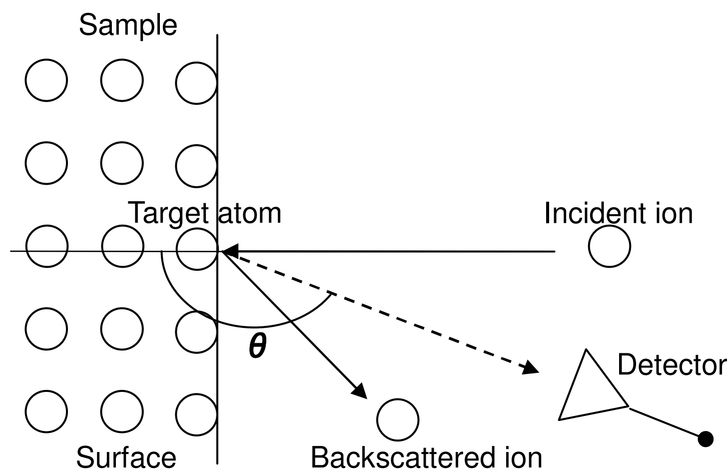


Fig. 2.11 Rutherford backscattering schematic

2.2.7 X-ray diffraction (XRD)

X-ray Diffraction (XRD) is a powerful non-destructive technique for characterizing crystalline materials. It provides information on structures, phases, preferred crystal orientations (texture) and other structural parameters such as average grain size, crystallinity, strain and crystal defects. X-ray diffraction peaks are produced by constructive interference of monochromatic beam scattered from each set of lattice planes at specific angles. The peak intensities are determined by the atomic decoration within the lattice planes. Consequently, the X-ray diffraction pattern is the fingerprint of periodic atomic arrangements in a given material. An on-line search of a standard database for X-ray powder diffraction pattern enables quick phase identification for a large variety of crystalline samples.

X rays diffract in crystal lattice when the azimuth angle meets Bragg diffraction condition. Bragg diffraction condition is represented as follows:

$$2d \sin\theta = n\lambda$$

where, d is the distance of lattice planes, θ is the angle of incidence, n is a integer number, and λ is the wavelength of incidence X rays.

2.2.8 Raman Spectroscopy

Raman spectroscopy is a method of chemical analysis that enables real-time reaction monitoring and characterization of compounds in a non-contact manner. The sample is illuminated with a laser and the scattered light is collected. The wavelengths and intensities of the scattered light can be used to identify functional groups in a molecule. It has found wide application in the chemical, polymer, semiconductor, and pharmaceutical industries because of its high information content and ability to avoid sample contamination.

2.2.9 Auger Electron Spectroscopy (AES)

Auger Electron Spectroscopy (*Auger spectroscopy* or AES) was developed in the late 1960's, deriving its name from the effect first observed by Pierre Auger, a French Physicist, in the mid-1920's. It is a surface specific technique utilizing the emission of low energy electrons in the *Auger process* and is one of the most commonly employed surface analytical techniques for determining the composition of the surface layers of a sample.

【Chapter 3】 Characterization of Ni silicide by using additional different materials as gate

3.1 Characterization of NiSi (no additive metal)

3.1.1 Introduction

I investigate to improve heat resistance of Ni silicide by additional different metal. In this section, we investigated Ni silicide with no additive metal.

3.1.2 Fabrication process

P-type (100)Si substrates with B concentration of ~$10^{20}/cm^3$, whose density is expected for the 45nm node, were used in this study.

After the substrates are chemically cleaned by SPM and diluted HF treatments in section2.1.2, Ni layers are deposited on the substrates by using a magnetron sputtering system in section2.1.3. The layered structure was based on the 12-nm-thick Ni layer, and in section3.1.4 I investigate Ni layer with 10 and 25 nm in thickness, too. These deposited samples were annealed for 60 seconds at various temperatures in forming gas (3%-H_2) ambient using a RTA system in section2.1.5.

Then sheet resistance of the silicide layers was measured by the four point probe method. And some samples were observed by TEM, XRD, Raman Spectroscopy.

3.1.3 Sheet resistance measurements by using the four point probe method

At first, pure Ni(12nm) thin film was investigated. Figure 3.1.1 shows transformation curves of sheet resistance measured by four-point probe shown in chapter 2.2.2 for the Ni silicide without any additives as a function of silicidation temperature from 200°C to 950 °C once every 25°C.

In the case of no additive metal, we can clearly distinguish 5 stages according to the change in sheet resistance [25]. The first one was the region from 200 to 300°C at which the main Ni phase was Ni_2Si according to the XRD analysis of Fig.3.1.4.

The second one which exhibited both the lowest and constant sheet resistance was the region form 300 to 700°C at which the Ni phase was NiSi, which was also supported by the XRD analysis of Fig.3.1.4 and Raman Spectroscopy measurement result as shown in Fig. 3.1.2. The TEM observations revealed that uniform NiSi layer was obtained as shown in Fig. 3.1.5.

The third one was the region from 700 to 750°C where NiSi was on the way to transform to $NiSi_2$. The reason why no $NiSi_2$ peak was observed neither in Fig. 3.1.2 nor in Fig. 3.1.4 above the temperature of 700°C was probably the signal corresponding to $NiSi_2$ phase is too weak to detect. So, NiSi and $NiSi_2$ must be coexisted in this temperature region. This stage featured by the peak in the sheet resistance curve Fig.3.1.1 agreed with a recent publication [26], [27], verifying the accuracy of the temperature. The TEM observations revealed that a part of NiSi Silicide layer become pyramid structures as shown in Fig. 3.1.5. But the thickness of Ni Silicide layer is almost as thick as it of NiSi layer.

The forth one was the region from about 750 to 925°C where the main phase was $NiSi_2$ which was a high resistivity material. At this temperature region, pyramid structures were observed according to the TEM figure 3.1.5. And the thickness of Ni Silicide layer becomes equivalent of $NiSi_2$ layer.

The last one was the region above 925°C where the thin film was not continuous any more and sheet resistance increased dramatically.

The degration at high annealing temperature results from the phase transformation from NiSi to $NiSi_2$ and agglomeration.

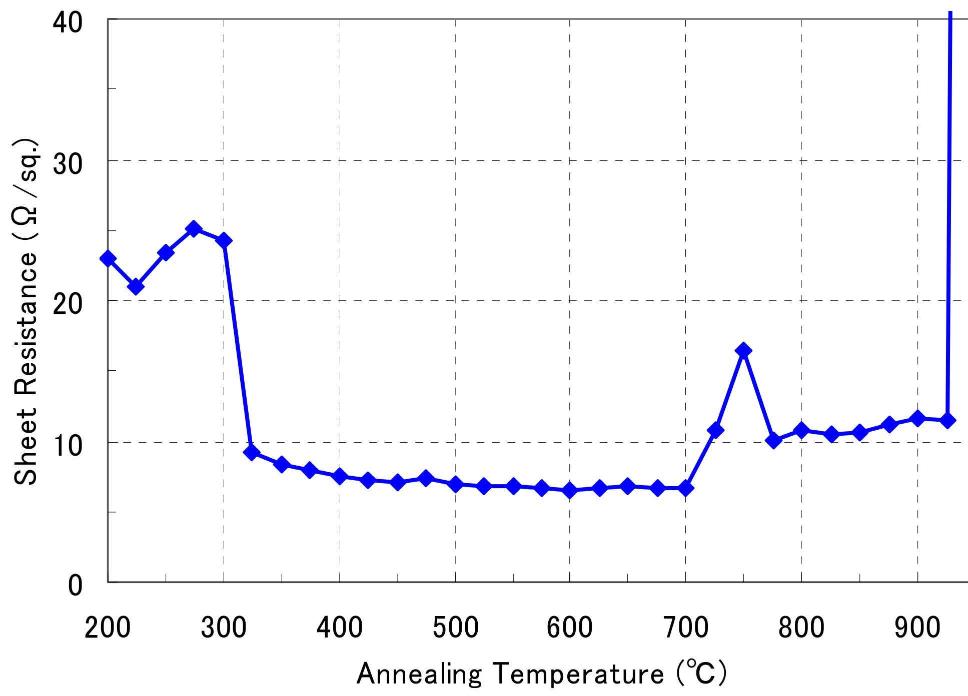


Fig. 3.1.1 Transformation curve of Ni silicide as a function of silicidation temperature for Ni(12nm)/Si structure.

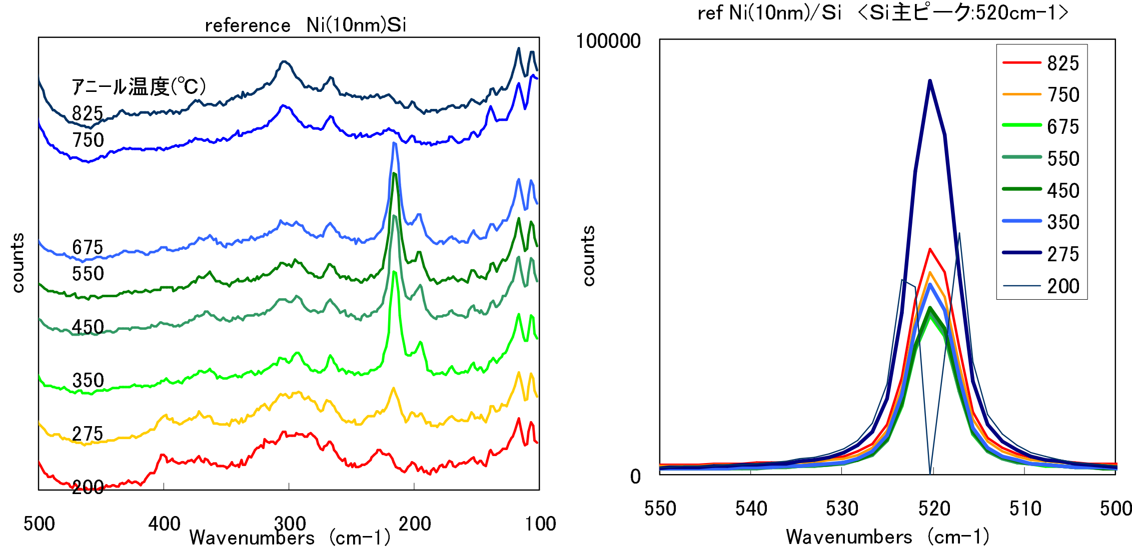


Fig. 3.1.2 Raman measurements for Ni(10nm)/Si structure with different silicidation temperature. (NiSi peak: 214cm^{-1}, Si peak: 520cm^{-1})

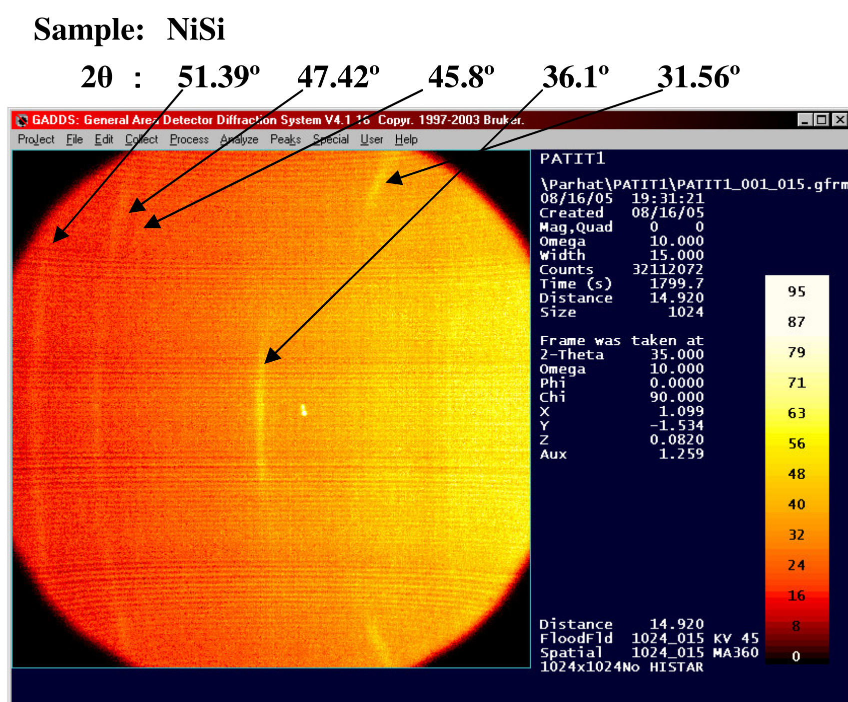
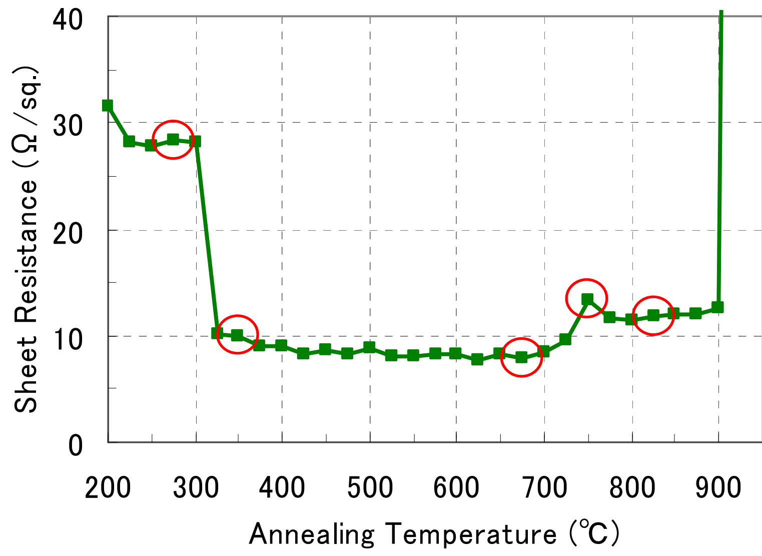
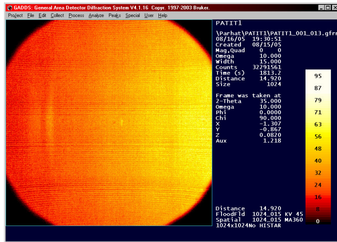


Fig. 3.1.3 NiSi measured for XRD.



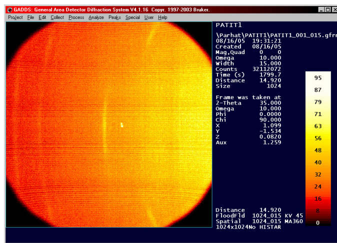
275°C



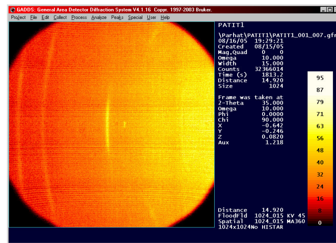
[peak] 45.5°、48.0°

Ni_2Si 121, 002

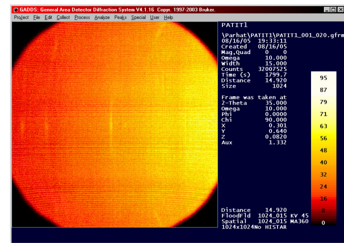
325°C



675°C



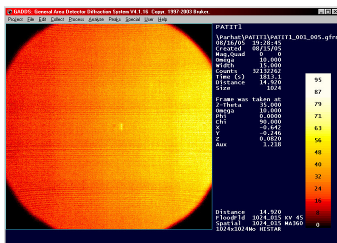
750°C



[peak] 31.56°、36.1°、45.8°、47.42°、51.39°

NiSi 101, 111, 211, 121or220, 310(?)

825°C



[peak] nothing

Fig. 3.1.4 X-ray diffraction reveals of Ni(10nm)/Si samples when annealed at each temperature.

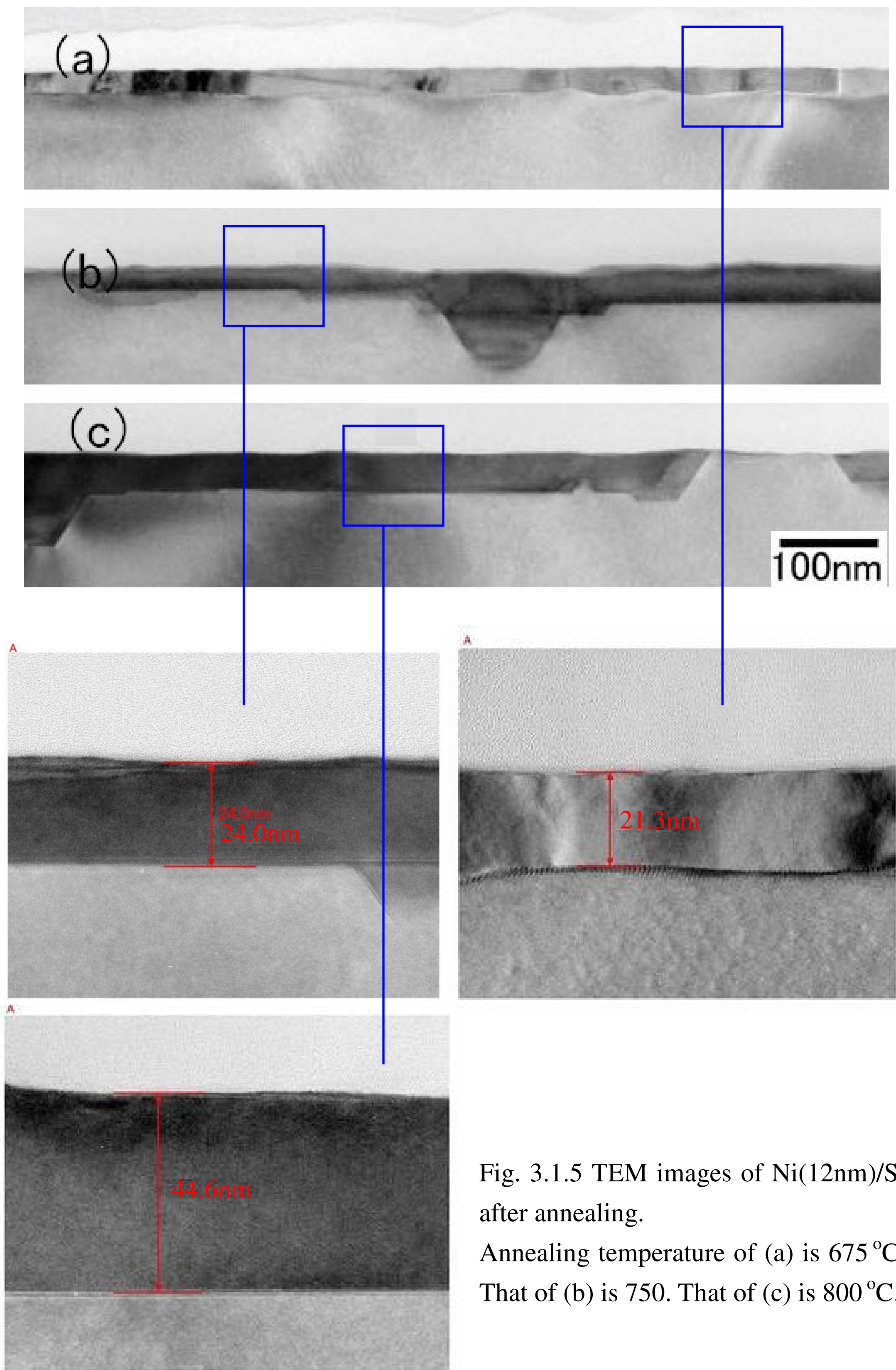


Fig. 3.1.5 TEM images of Ni(12nm)/Si after annealing.
Annealing temperature of (a) is 675 °C. That of (b) is 750. That of (c) is 800 °C.

3.1.4 Dependence of the Ni thickness

The sheet resistances of these samples are measured by four-point probe. Figure 3.1.6 shows sheet resistance of Ni silicide as a function of silicidation temperature for every deposited structure.

To get the reliability of the sheet resistance peak, Ni thin film with different thicknesses of 10nm, 12nm and 25nm was examined. Fig. 3.1.6 shows that the phenomenon existed among all of these samples after annealing process. However, as for the annealing temperature which sheet resistance peak appeared, Ni(25nm)/Si was 50°C higher than Ni(10nm)/Si and Ni(12nm)/Si. In other word, the thermal stability of Ni thin film became strong with increase of thickness.

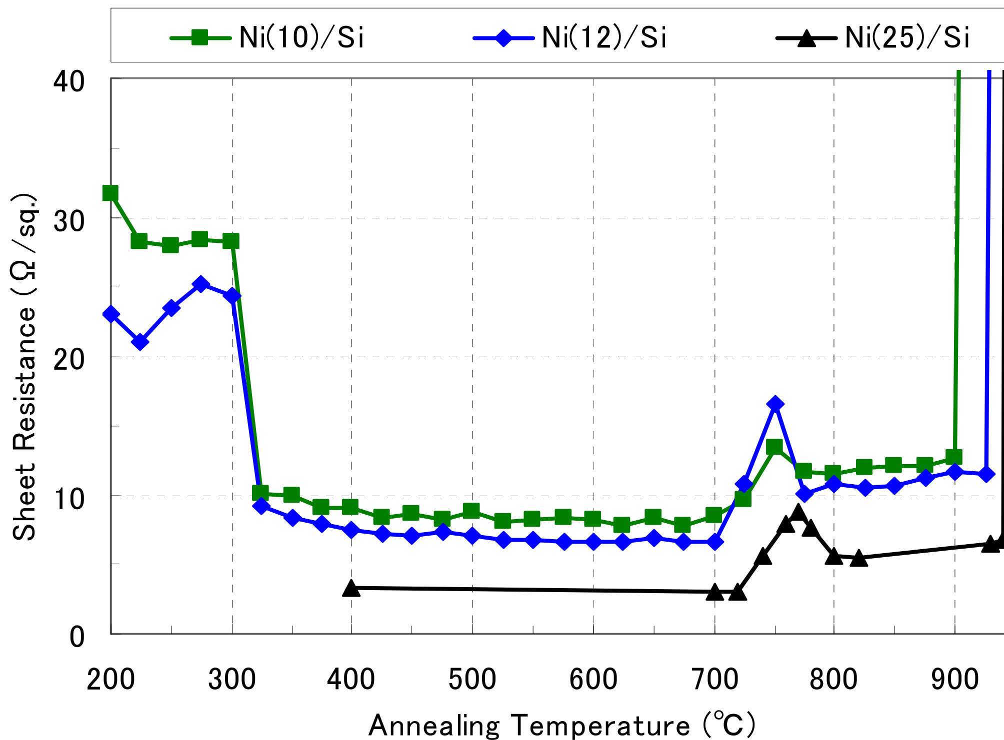


Fig. 3.1.6 Transformation curves of Ni silicide as a function of silicidation temperature for Ni(10nm)/Si, Ni(12nm)/Si and Ni(25nm)/Si structures.

3.2 Effect of additional metals by bi-layer deposition method.

3.2.1 Introduction

To improve heat resistance of Ni silicide, introduction of various metal or element were investigated. In this section, I investigate introduction of V, Hf, Ru and Pt as additive metal. The thin (almost 2 nm) additive layer was deposited on or under 10 nm thick Ni on a Si substrate so that M/Ni/Si (M: additive metal) and Ni/M/Si layered structure was formed. Pt was often known effective additive to improve heat resistance of Ni silicide.

3.2.2 Fabrication process

After the boron implanted p^+-Si substrates are chemically cleaned by SPM and diluted HF treatments in section 2.1.2, Ni and additive layers ware deposited on the substrates by using a magnetron sputtering system, in which base pressure was less than 5 x 10^{-6} Pa on the Si substrates in section 2.1.3. The thickness of Ni was 12 nm for the experiments using only pure Ni layers. The layered structure was based on the 10-nm-thick Ni layer, and additive layer with 1-4 nm in thickness is introduced on or under Ni shown in Fig.3.2.1. These deposited samples were annealed for 60 seconds at various temperatures in forming gas (3%-H_2) ambient using an RTA system in section 2.1.5 and silicided. Any chemical etching was not performed after the annealing.

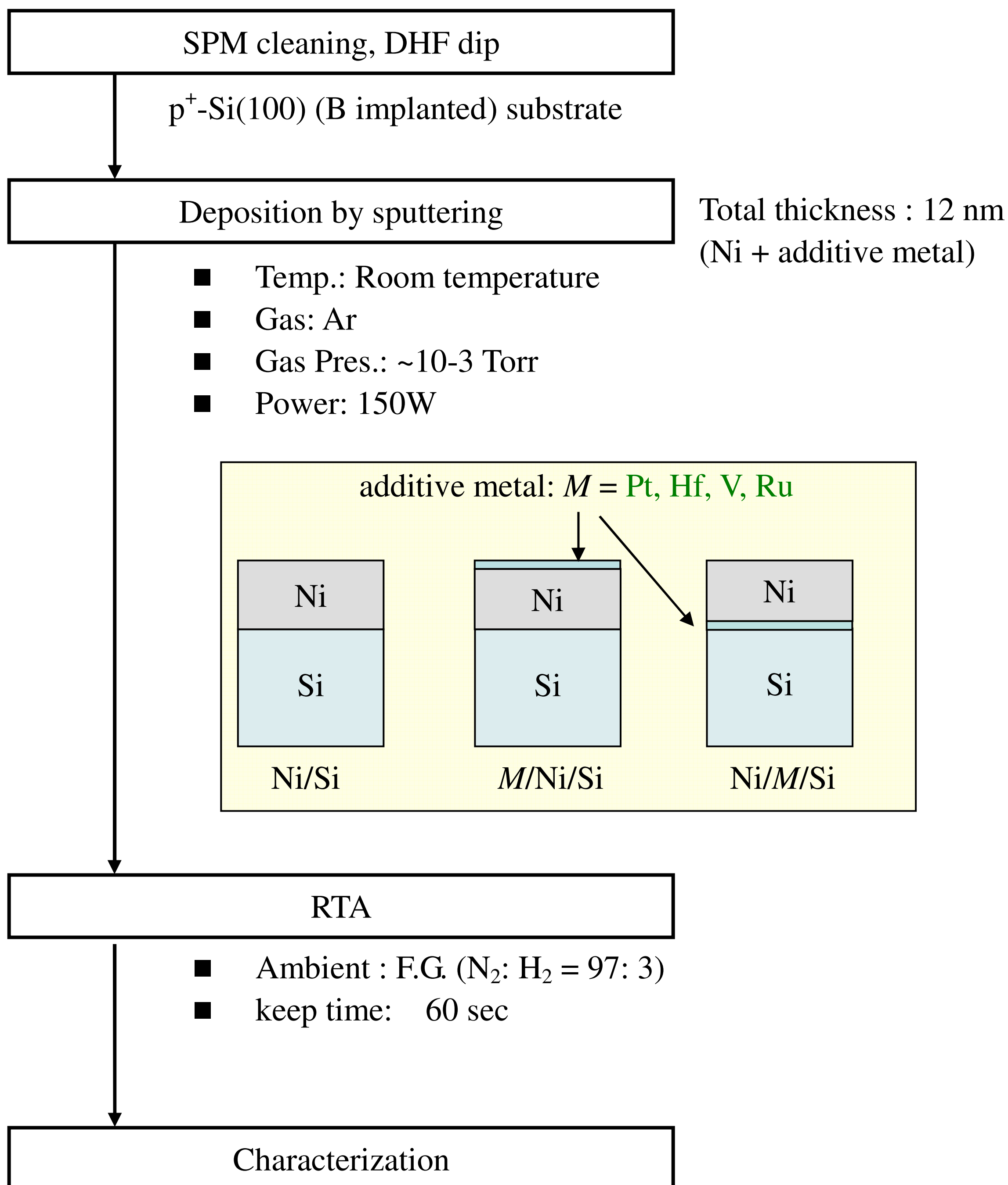


Fig.3.2.1 Process flow for fabrication of bi-layer method.

3.2.3 Sheet resistance measurements by using the four point probe method

There are some common features when V, Hf, Ru and Pt were used as metal additives in course of Ni silicide thin film formation. However, there is no improvement in the thermal stability of Ni silicide with these additives for every deposited structure.

A result in case of V is shown as Figure 3.2.2. Three kinds of structures were compared, Ni(12nm)/Si, V(1nm)/Ni(12nm)/Si and Ni(12nm)/V(1nm)/Si. The thicknesses of Hf layer was 1nm. (I was depositing 2nm-thin-V layer. But the thickness of V was 1nm.) In the case of V addition by V layer above Ni, it seems that NiSi layer is formed up from 350 to 600 ^{o}C. Above 600 ^{o}C, the sheet resistance starts to increase, presumably due to the lower temperature transition to $NiSi_2$ because of the V diffusion into the Ni film suppressing the Ni supply to the Si substrate or the lower temperature agglomeration. On the other hand, in the case of V addition by V layer under Ni, significant increase in the sheet resistance was observed in entire temperature range. The V layer between the Ni and Si suppresses the Ni supply into the Si substrate, resulting in the shift of the sheet resistance peak of Ni-rich silicide phase (such as Ni_2Si) around 300 ^{o}C. This poor supply of Ni in the medium temperature range below 700 ^{o}C forms NiSi2 layer rather than NiSi. These will confirm by Auge electron spectroscopy and X-ray diffraction in section3.2.4.

A result in case of Hf is shown as Figure 3.2.3. The result is much like V addition case. The shift of the sheet resistance peak of Ni-rich silicide phase is extreme.

A result in case of Ru is shown as Figure 3.2.4. The result is much like V addition case, too. But It is different from V and Hf that above 600 ^{o}C, the sheet resistance don't starts to increase so much in Ru/Ni/Si structure.

A result in case of Pt is shown as Figure 3.2.5. The Pt addition by Pt layer under Ni showed the similar effects as the V case. Pt suppresses the Ni supply and very similar curve as that of the V layer under Ni was observed. However the Pt addition by Pt layer above Ni showed the similar effects as the V additive under Ni, too. Pt diffuses into Ni more easily than Hf. Thus, in the case of Pt layer above Ni, suppression effects of the Ni supply would occur at lower temperature, enhancing $NiSi_2$ formation.

On the other hand, Hf exhibited characteristics more resemble to the V case, because their diffusivity into Ni is not as large as that of Pt

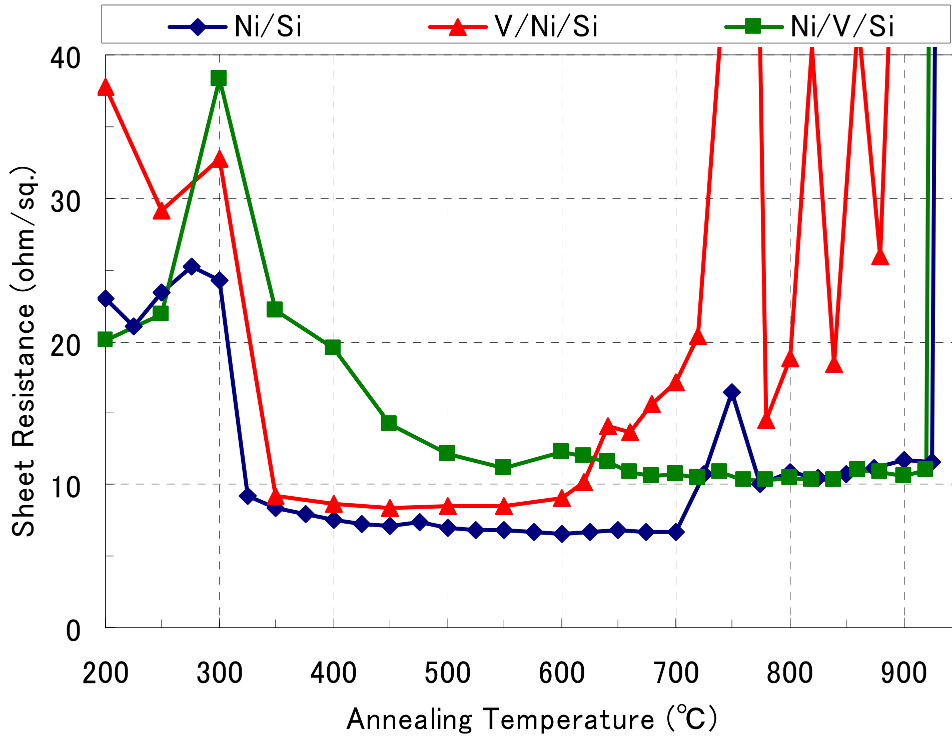


Fig. 3.2.2 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12nm)/Si, V(1nm)/Ni(10nm)/Si and Ni(10nm)/ V(1nm)/Si structures.

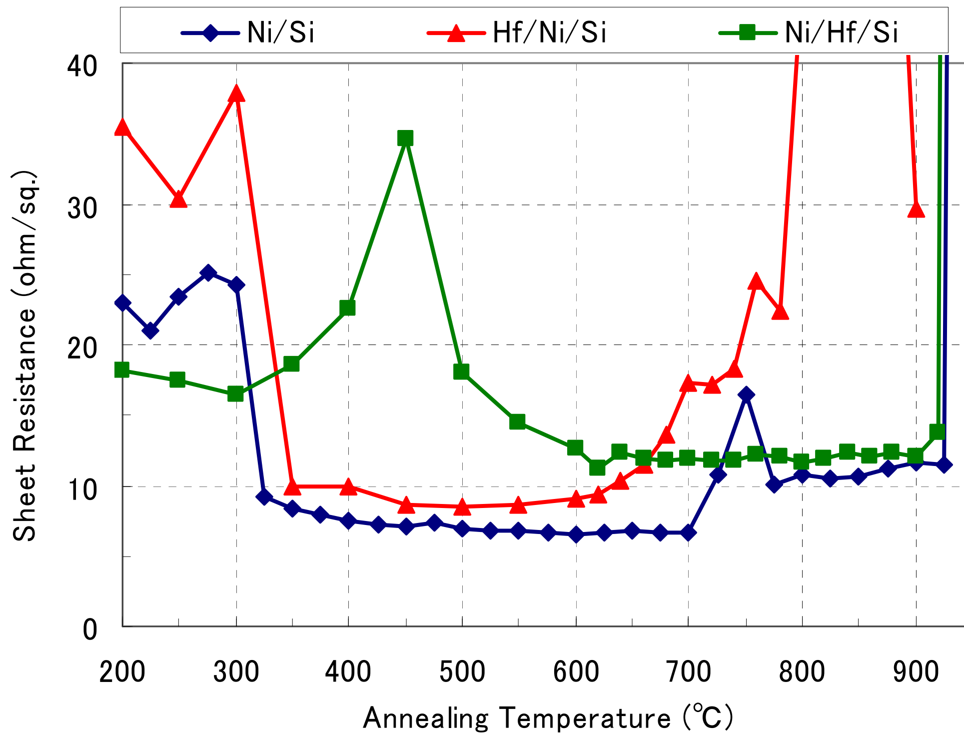


Fig. 3.2.3 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12nm)/Si, Hf(2nm)/Ni(10nm)/Si and Ni(10nm)/Hf(2nm)/Si structures.

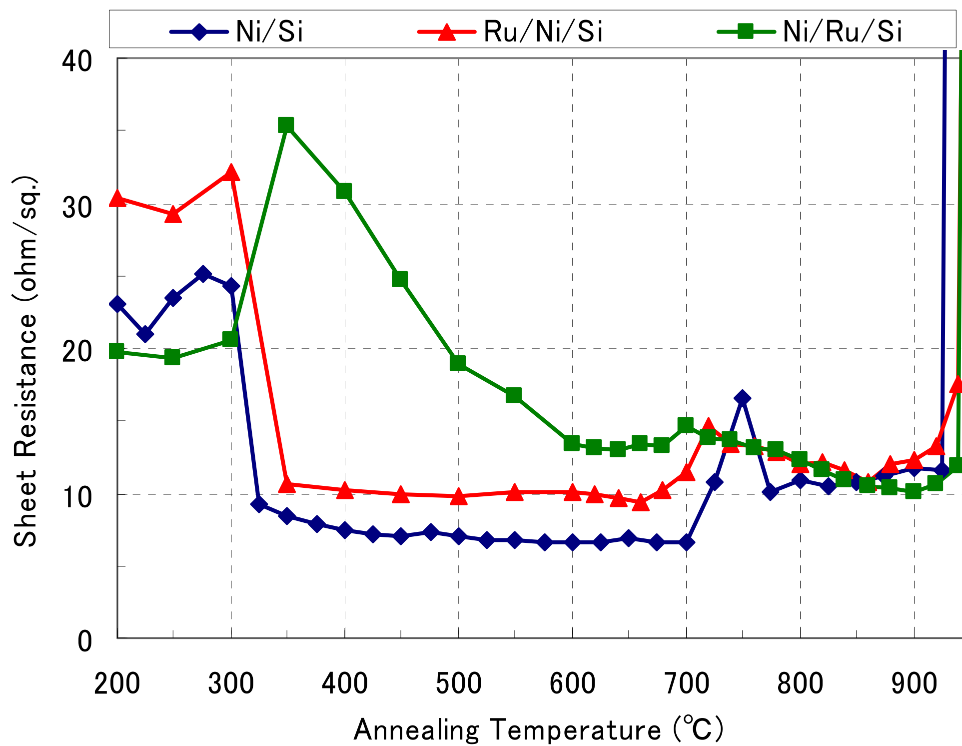


Fig. 3.2.4 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12nm)/Si, Ru(2nm)/Ni(10nm)/Si and Ni(10nm)/Ru(2nm)/Si structures.

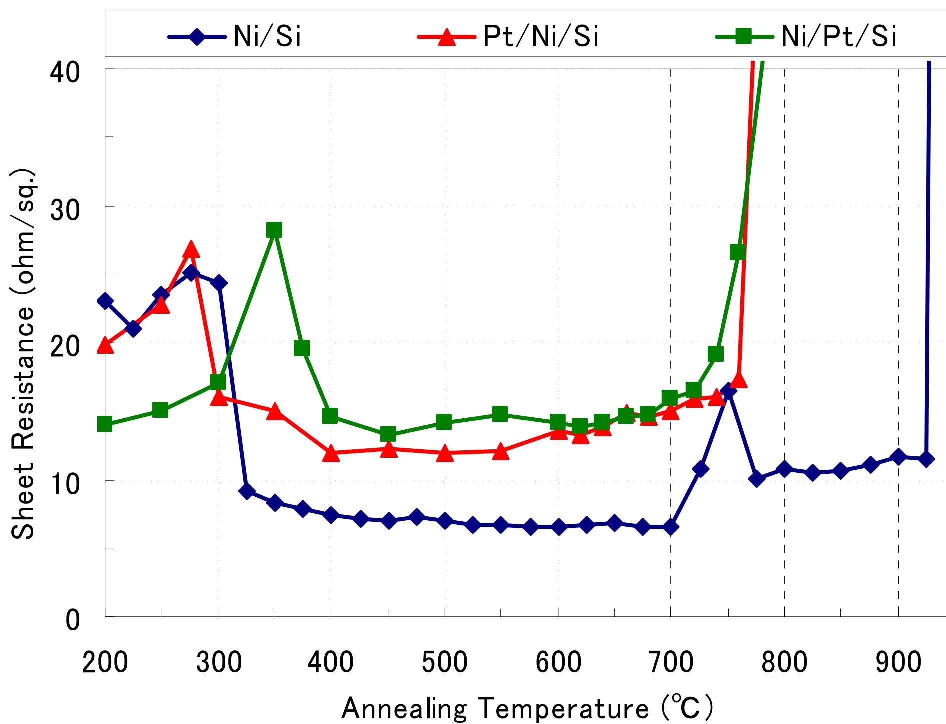


Fig. 3.2.5 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12nm)/Si, Pt(4nm)/Ni(10nm)/Si and Ni(10nm)/Pt(4nm)/Si structures.

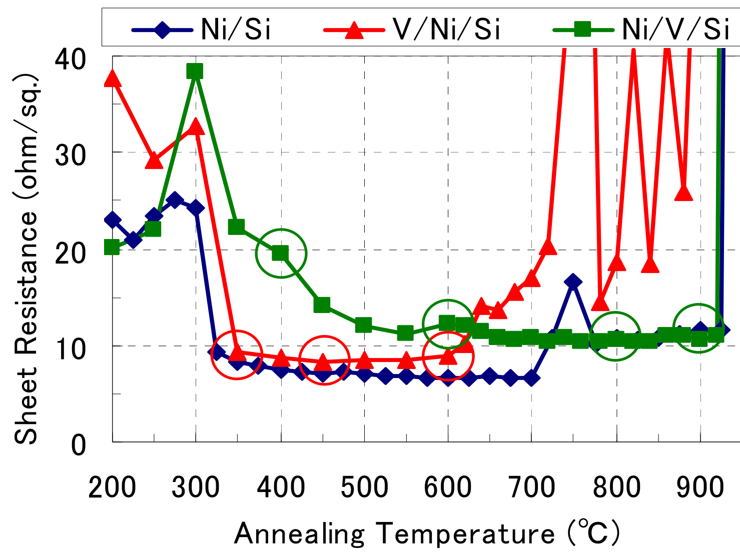
3.2.4 Analysis of the phase of Ni Silicide

Figure 3.2.6 shows XRD reveals of V(1nm)/Ni(10nm)/Si and Ni(10nm)/ V(1nm)/Si samples. In the case of V addition by V layer above Ni, it seems that the region from 350 to 600°C which exhibited both the lowest and constant sheet resistance is NiSi. On the other hand in the case of V addition by V layer under Ni, it seems that the region above 400°C which exhibited start to decrease sheet resistance is $NiSi_2$. Raman spectra of V(1nm)/Ni(10nm)/Si and Ni(10nm)/ V(1nm)/Si samples as Fig.3.2.7 shows a similar outcome, too.

Figure 3.2.8 shows Raman spectra of Hf(2nm)/Ni(10nm)/Si and Ni(10nm)/ Hf(2nm)/ Si samples. The result is much like V addition case. And it seems that the left region of the sheet resistance peak of Ni-rich silicide phase, not only 250°C of Hf(2nm)/ Ni(10nm)/Si but also 400 ^{o}C of Ni(10nm)/ Hf(2nm)/Si is Ni-rich Silicide, $NiSi_2$.

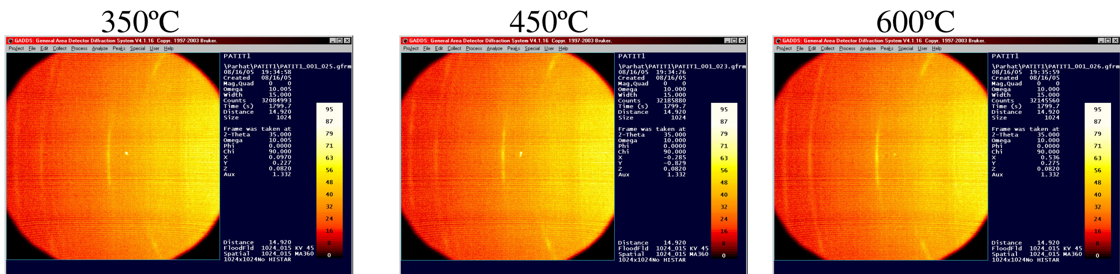
Figure 3.2.9 shows Raman spectra of Ru(2nm)/Ni(10nm)/Si and Ni(10nm)/ Ru(2nm)/ Si samples. The result is much like V addition case. But in the region from 350 to 600°C of Ru(2nm)/Ni(10nm)/Si NiSi peak is weak. So in this region sheet resistance is a little higher than that of V and Hf. And Above 780 ^{o}C of Ru(2nm)/Ni(10nm)/Si it seem that silicide phase is $NiSi_2$.

Figure 3.2.10 shows Raman spectra of Pt(4nm)/Ni(10nm)/Si and Ni(10nm)/ Pt(4nm)/ Si samples. From only transformation curve it seems that the effect of Pt addition do not depend on structure so. But Raman spectra shows difference of these. In the case of Ni(10nm)/ Pt(4nm)/ Si the result is much like V addition case. On the other hand in the case of Pt(4nm)/Ni(10nm)/Si at both 600 and 720°C Raman spectra shows about 200cm^{-1} close to NiSi peak 214cm^{-1}. It seems to be created new phase to mix Pt with NiSi.



(a) V/Ni/Si

350ºC 450ºC 600ºC



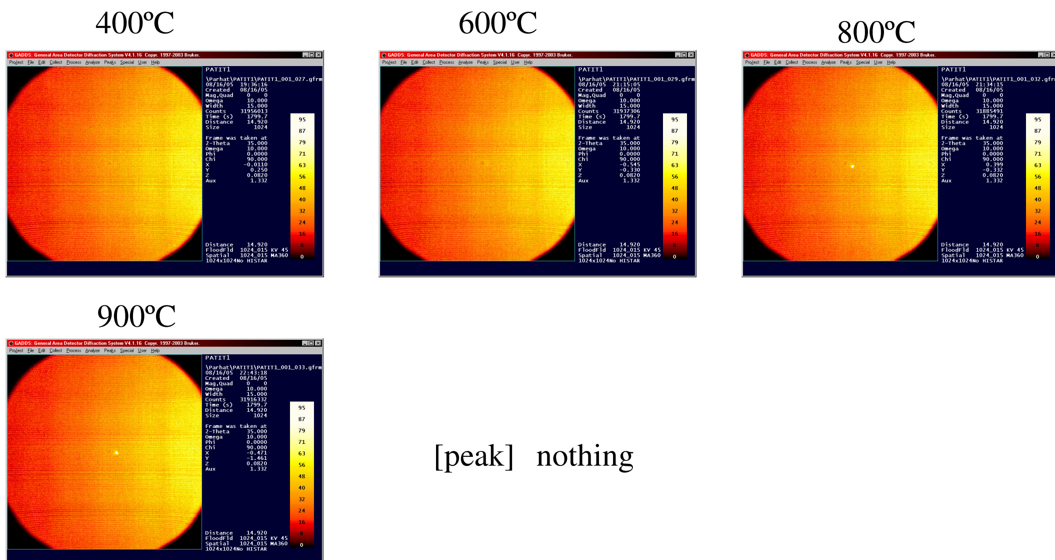
[peak] 31.48º、35.98º、45.83º、47.17º、51.29º

NiSi 101, 111, 211, 121or220, 310(?)

(b) Ni/V/Si

400ºC 600ºC 800ºC

900ºC



[peak] nothing

Fig. 3.2.6 X-ray diffraction reveals of (a) V(1nm)/Ni(10nm)/Si and (b) Ni(10nm)/V(1nm)/Si samples when annealed at each temperature.

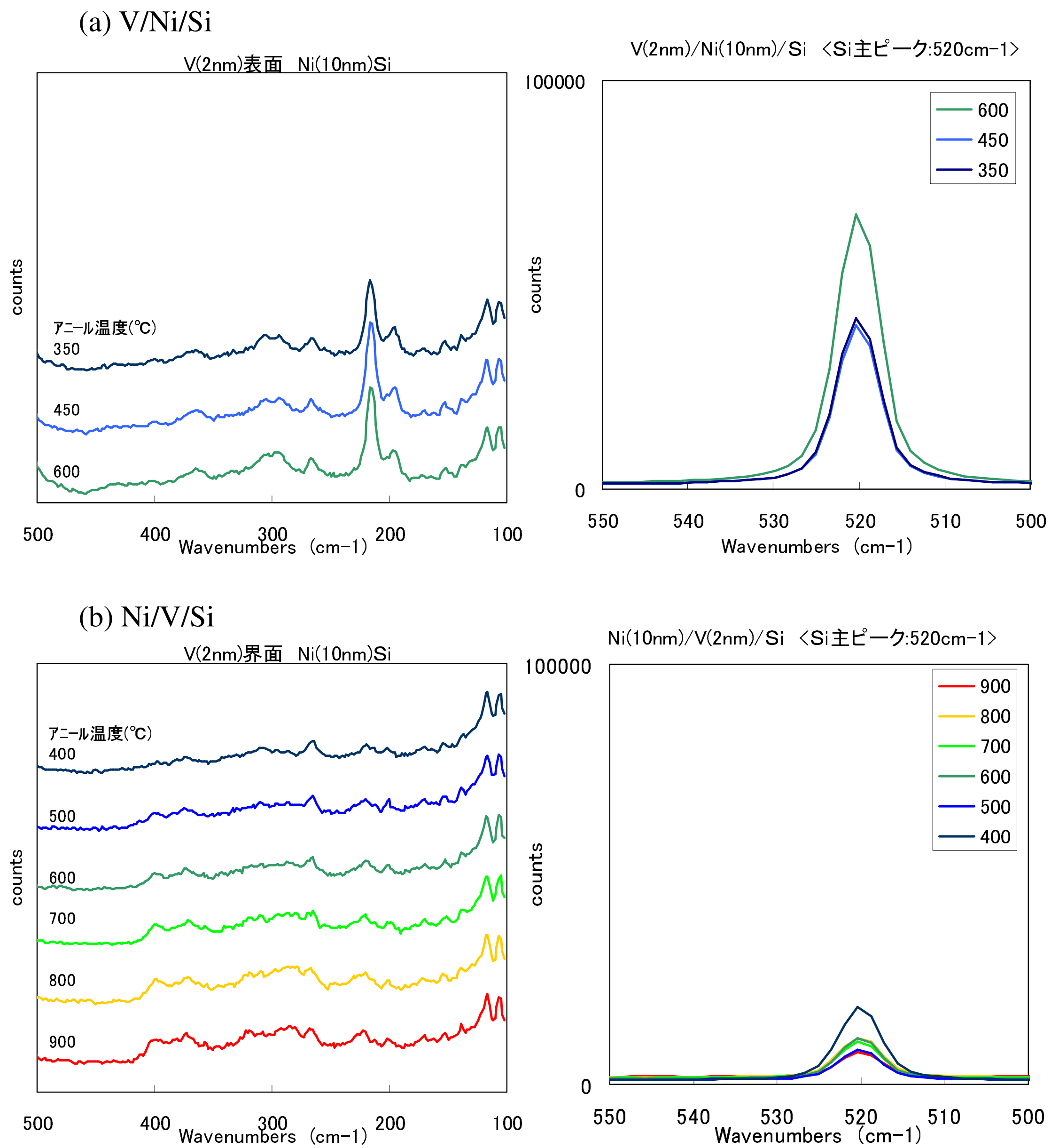
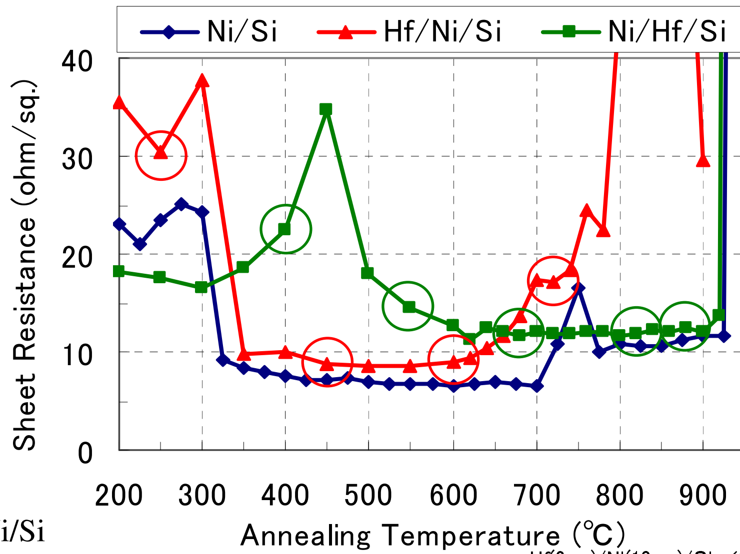
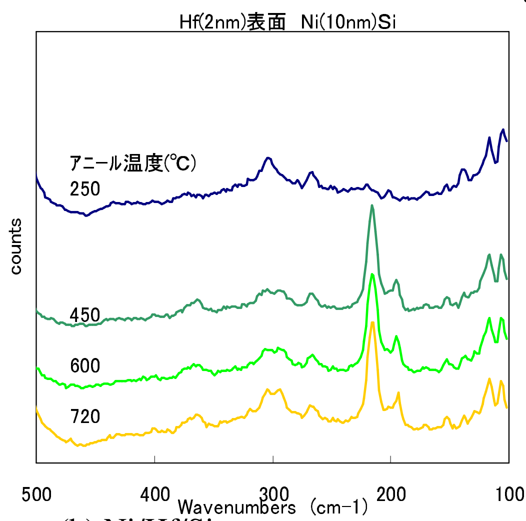
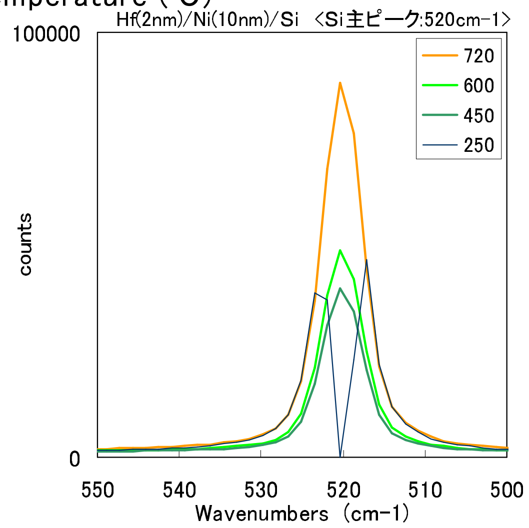


Fig. 3.2.7 Raman spectra of (a) V(1nm)/Ni(10nm)/Si and (b) Ni(10nm)/ V(1nm)/Si samples. (NiSi peak: 214cm^{-1}, Si peak: 520cm^{-1})

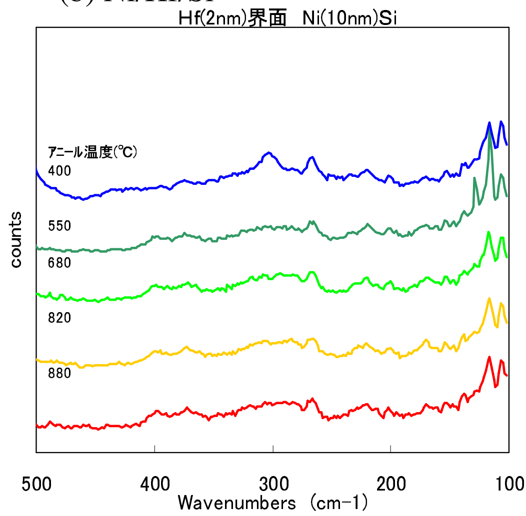


(a) Hf/Ni/Si





(b) Ni/Hf/Si



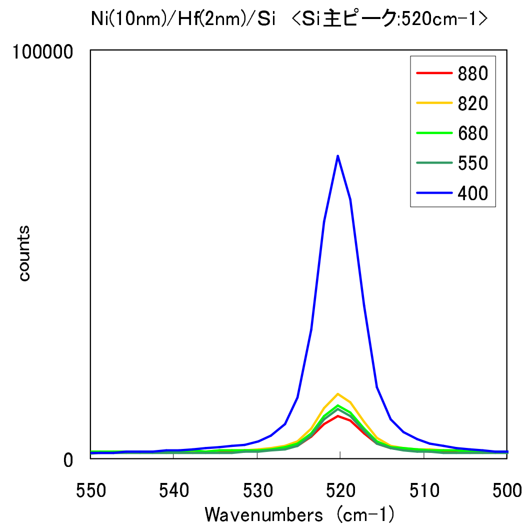
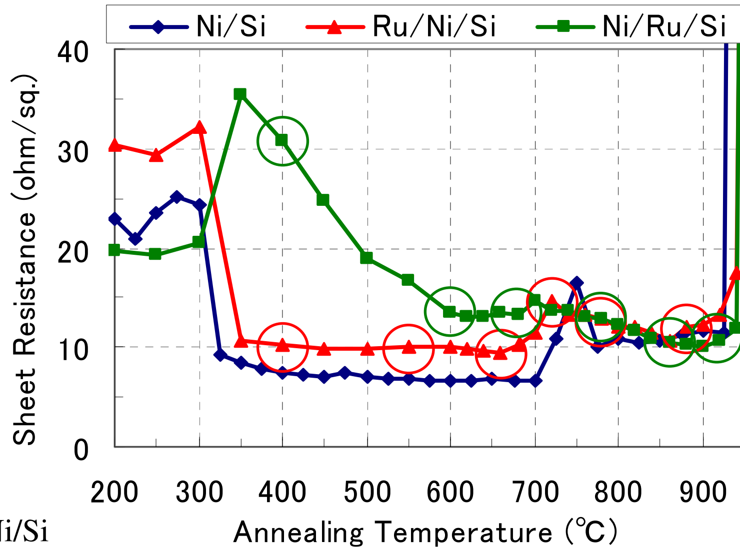
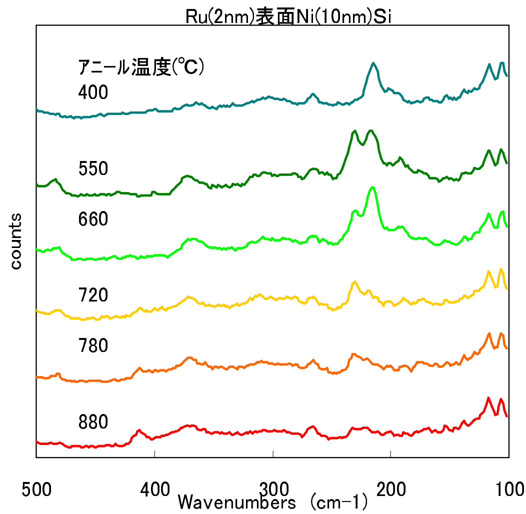
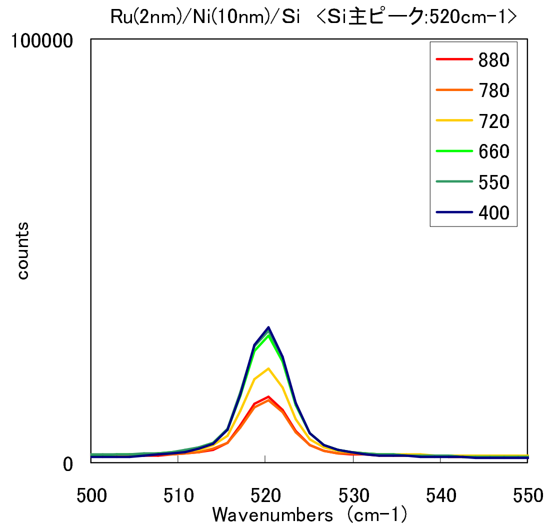


Fig. 3.2.8 Raman spectra of Hf(2nm)/Ni(10nm)/Si and Ni(10nm)/Hf(2nm)/Si structures.
(NiSi peak: $214cm^{-1}$, Si peak: $520cm^{-1}$)

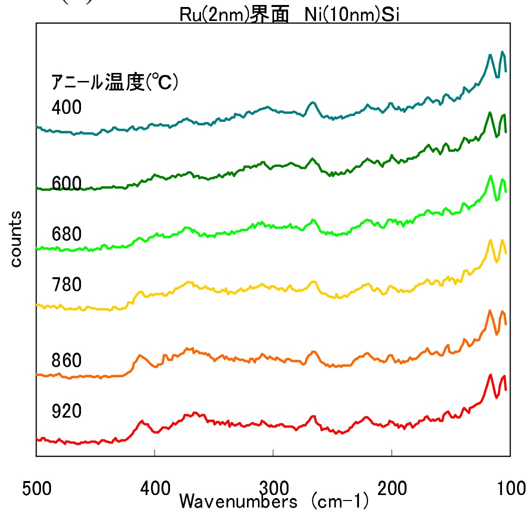


(a) Ru/Ni/Si





(b) Ni/Ru/Si



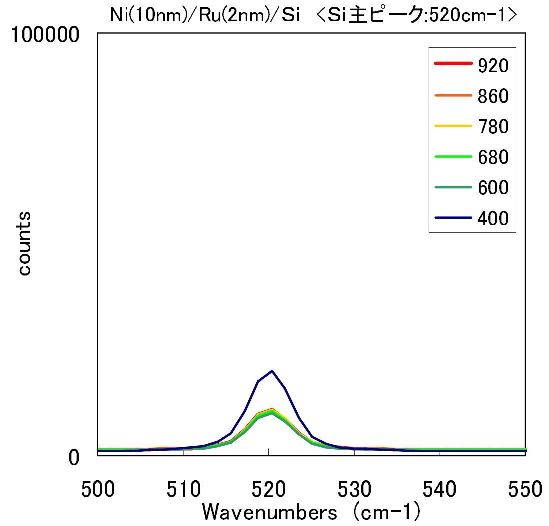
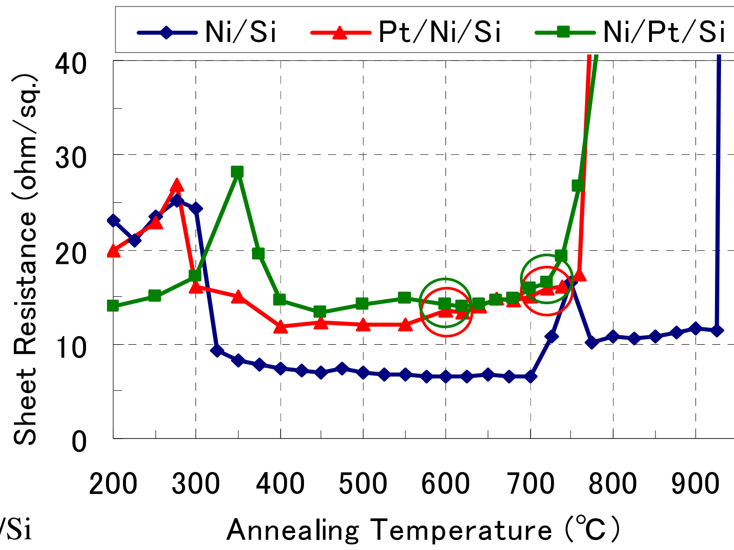
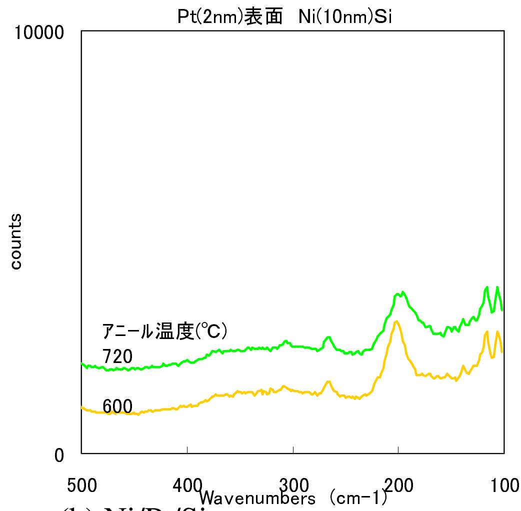
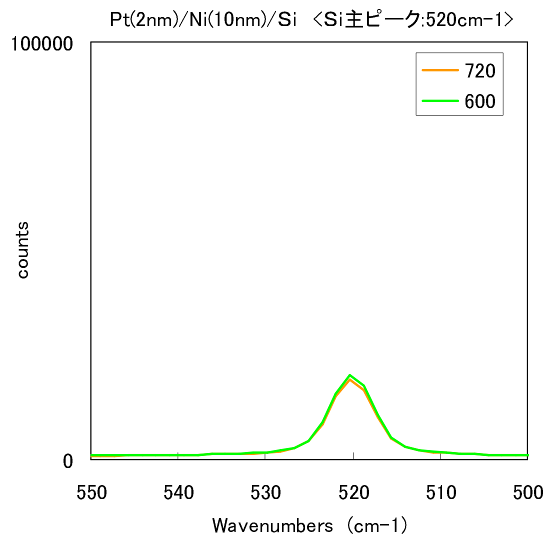


Fig.3.2.9 Raman spectra of Ru(2nm)/Ni(10nm)/Si and Ni(10nm)/Ru(2nm)/Si structures.
(NiSi peak: 214cm^{-1}, Si peak: 520cm^{-1})

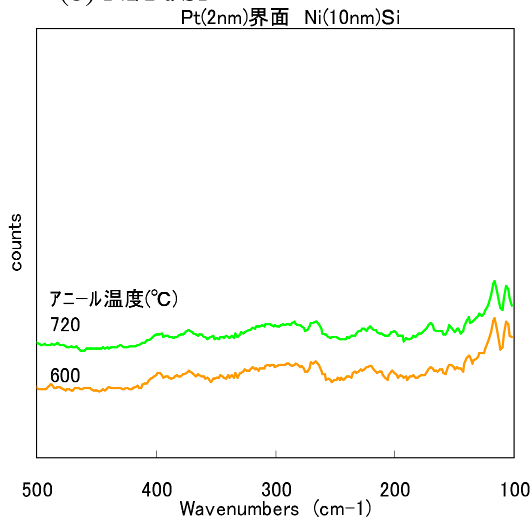


(a) Pt/Ni/Si





(b) Ni/Pt/Si



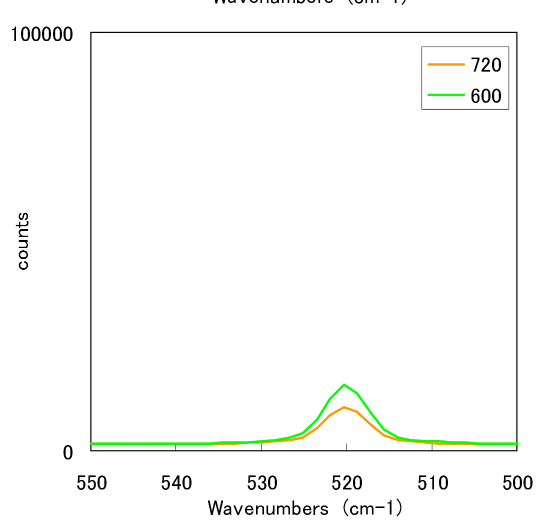


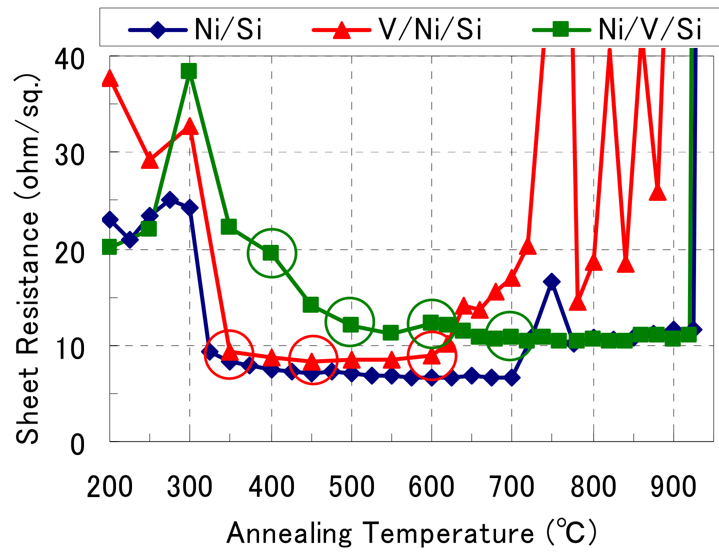
Fig. 3.2.10 Raman spectra of Pt(4nm)/Ni(10nm)/Si and Ni(10nm)/Pt(4nm)/Si structures. (NiSi peak: 214cm^{-1}, Si peak: 520cm^{-1})

3.2.5 Morphology on surface and at interface

Figure 3.2.11 shows cross-sectional SEM images of V(1nm)/Ni(10nm)/Si and Ni(10nm)/ V(1nm)/Si samples. In the case of V addition by V layer above Ni, it seems that the silicide layer is uniform on the surface and at the interface to Si at the region from 350 to 600°C which exhibited both the lowest and constant sheet resistance. In the case of V addition by V layer under Ni, it seems the silicide layer is very uniform on the surface and a little rough at the interface to Si at the region from 400 to 700°C.

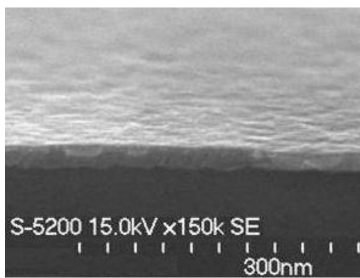
Figure 3.2.12 shows cross-sectional SEM images of Hf(2nm)/Ni(10nm)/Si and Ni(10nm)/ Hf(2nm)/ Si samples. The result is much like V addition case. Addition to that it seems that at the region from 720 to 880°C the silicide layer is kept good uniformity.

Figure 3.2.13 shows cross-sectional SEM images of Ru(2nm)/Ni(10nm)/Si and Ni(10nm)/ Ru(2nm)/ Si samples. The result is different from V addition case. In the case of V addition by V layer above Ni, it seems that the silicide layer is uniform on the surface, but at the interface to Si it looks rough. And at 880°C it seems to start to agglomeration on the surface. On the other hand in the case of V addition by V layer under Ni, it seems the silicide layer is uniform on the surface and a little rough at the interface to Si at the region from 400 to 860°C. But annealed temperature higher, the interface to Si roughness becomes better.

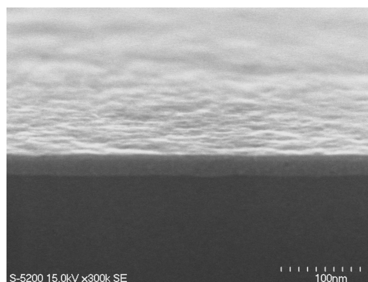


(a) V /Ni /Si

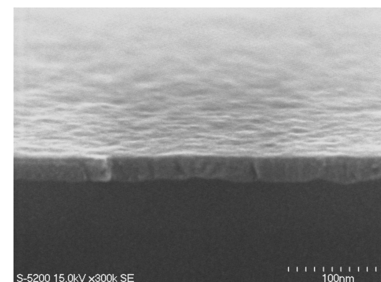
350°C



450 °C

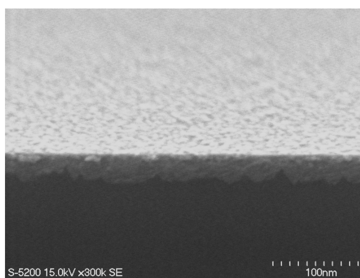


600 °C

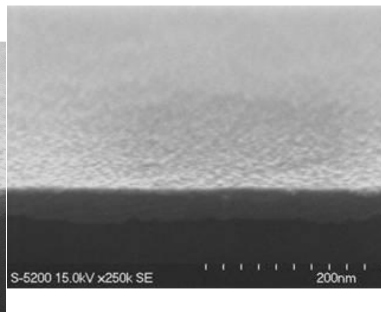


(b) Ni /V /Si

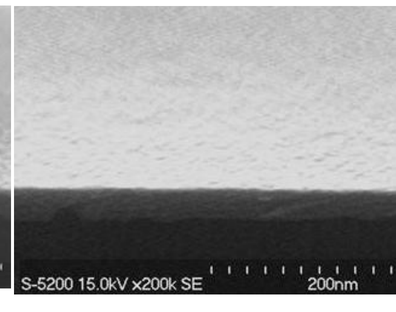
400°C



500°C



600°C



700°C

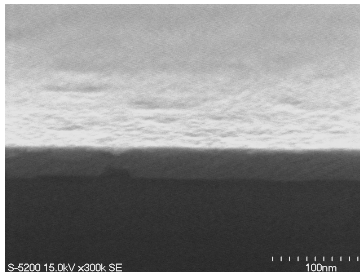
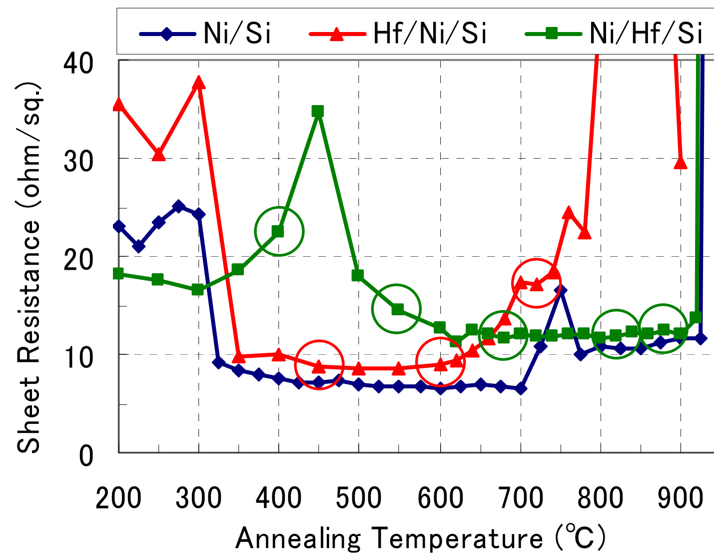
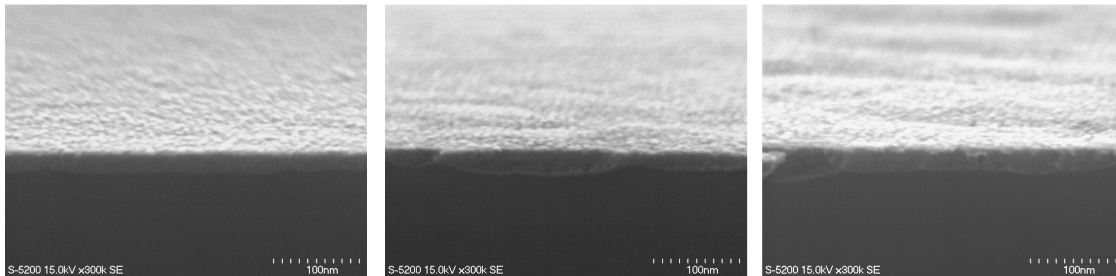


Fig. 3.2.11 Cross-section SEM images of V(1nm)/Ni(10nm)/Si and Ni(10nm)/V(1nm) /Si structures at each annealing temperature.



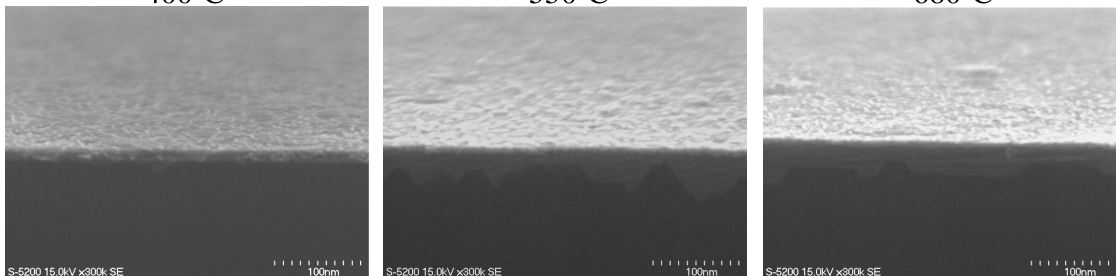
(a) Hf /Ni /Si

450°C 600°C 720°C



(b) Ni /Hf /Si

400°C 550°C 680°C



820°C 880°C

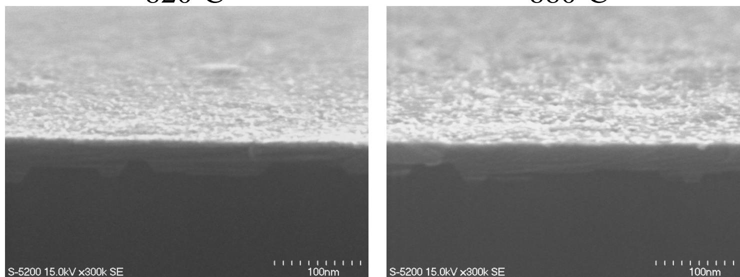
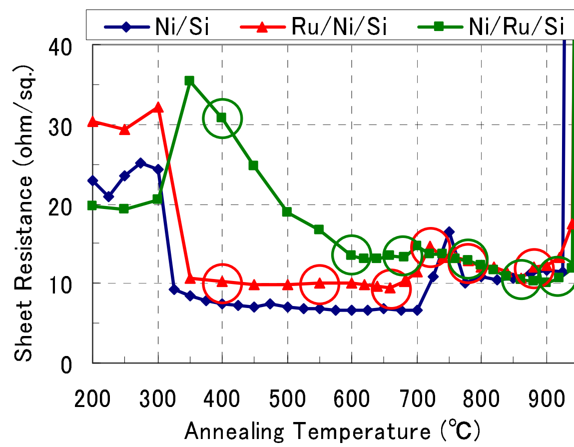
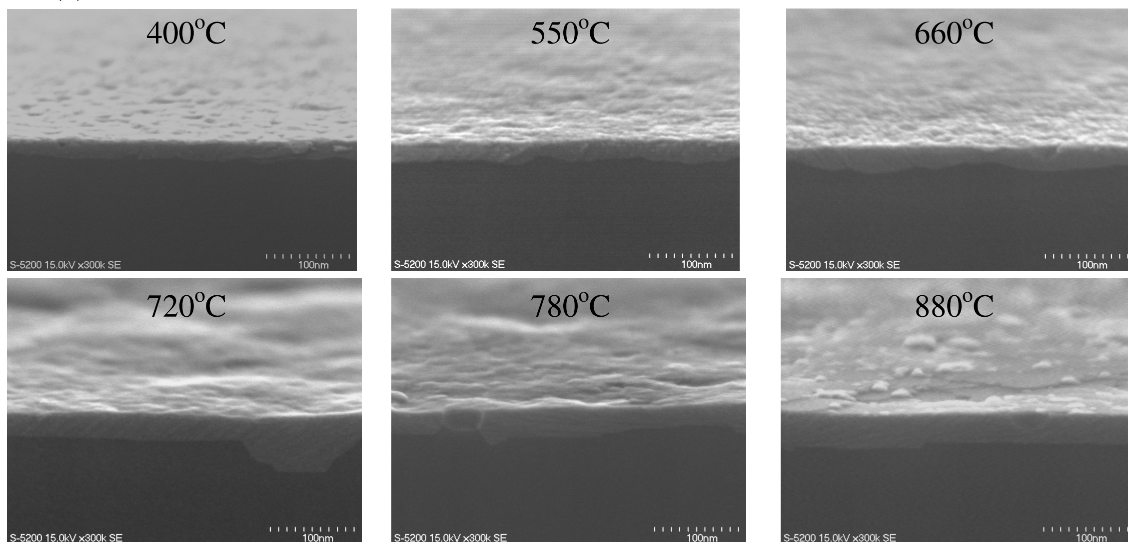


Fig. 3.2.12 Cross-section SEM images of Hf(2nm)/Ni(10nm)/Si and Ni(10nm)/Hf(2nm) /Si structures at each annealing temperature.



(a) Ru /Ni /Si



(b) Ni /Ru /Si

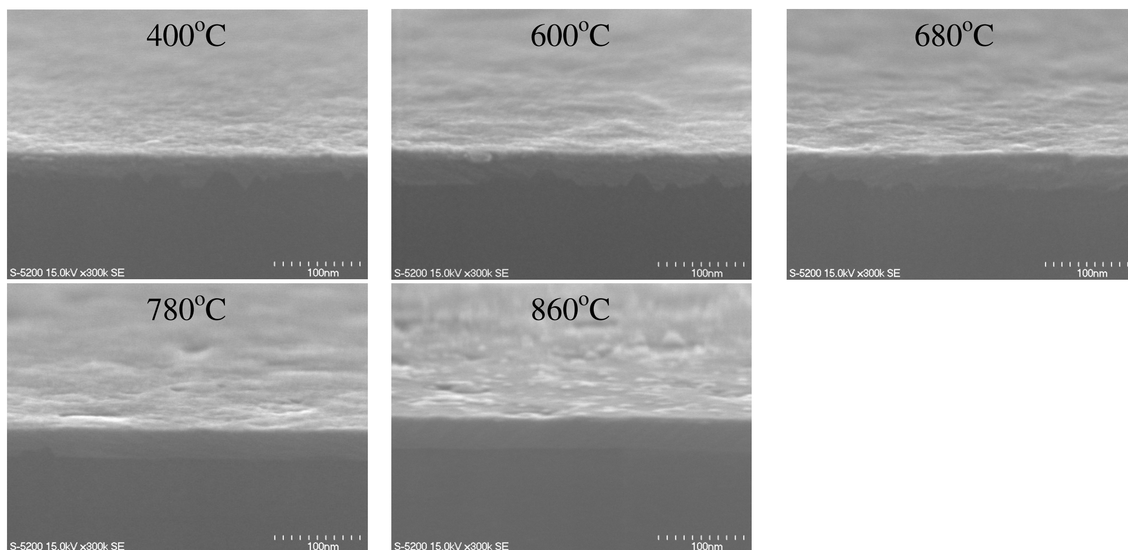


Fig. 3.2.13 Cross-section SEM images of Ru(2nm)/Ni(10nm)/Si and Ni(10nm)/Ru(2nm)/Si structures at each annealing temperature.

3.2.6 Sheet resistance depending on amount of Pt addition

In section2.1.3 I indicate creation of new phase to mix Pt with NiSi. So in this section I examine characteristics of Ni Silicide changing amount of additional Pt. The result is shown in Fig. 3.2.14. And fig3.2.15 shows sheet resistance average at the region which exhibited both the lowest and constant sheet resistance as a function of Pt concentration for each sample. It seems to create new phase which is different from NiSi depending on amount of Pt not to depend on additional position.

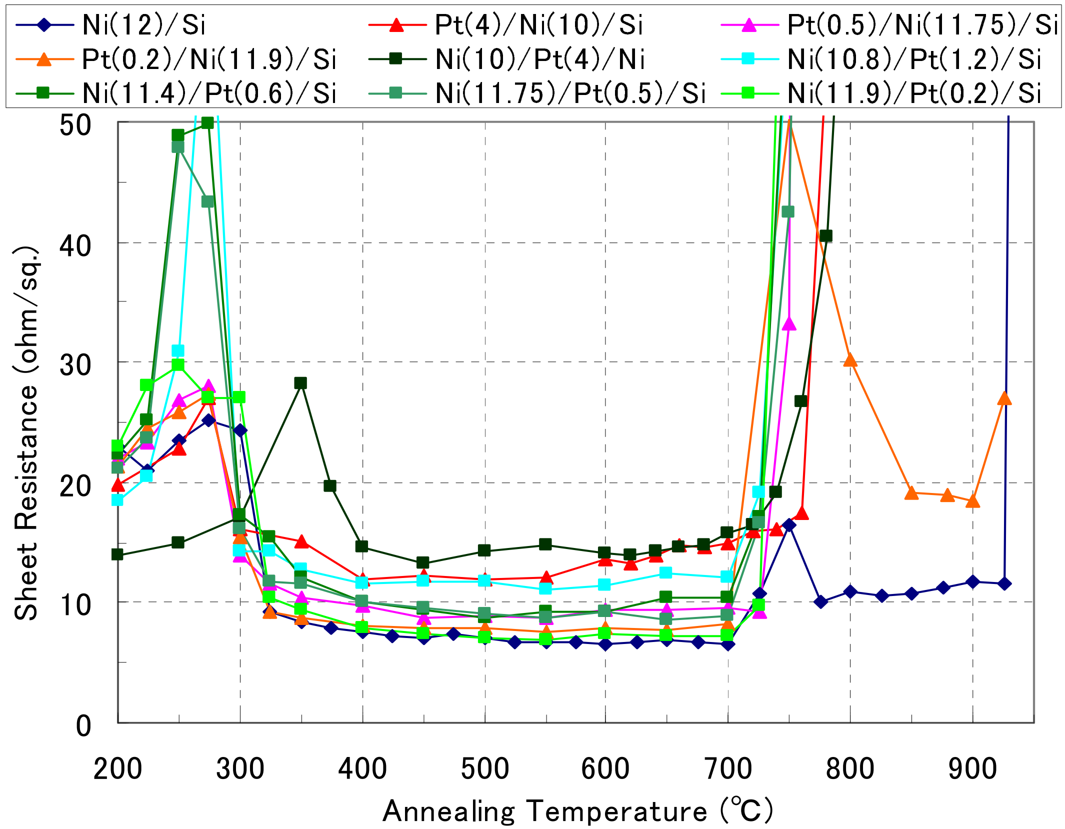


Fig. 3.2.14 Transformation curves of Ni silicide for Ni/Si Pt/Ni/Si and Ni/Pt/Si structures. The thicknesses of Pt layer are 0.2-4.0nm.

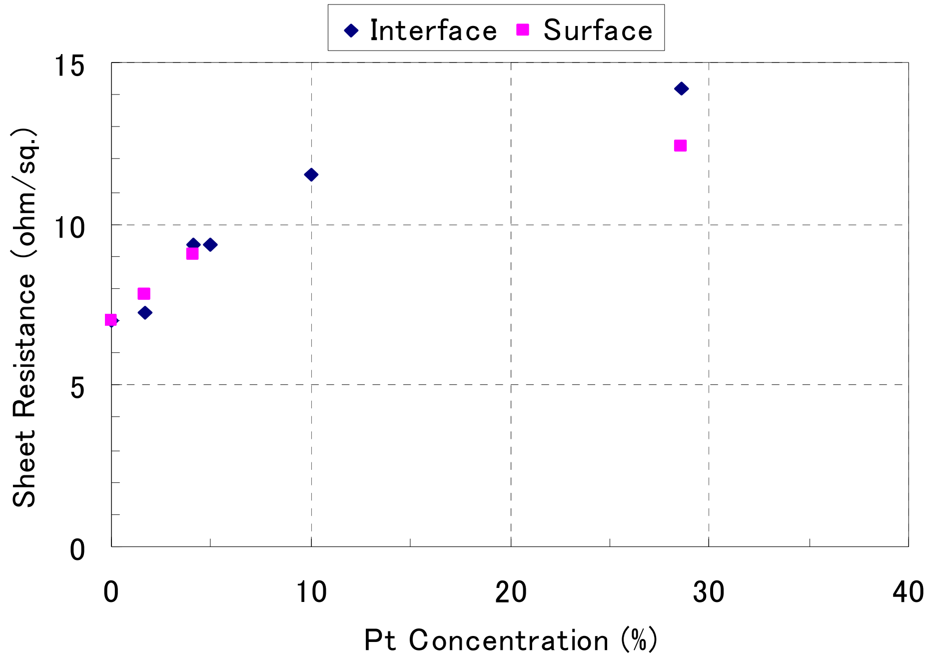


Fig. 3.2.15 Sheet resistance of Ni silicide as a function of Pt ratio of deposition metal for Ni/Si, Pt/Ni/Si and Ni/Pt/Si structures.

3.3 Phase transition model and concept of the PSMD method

3.3.1 Phase transition model

Based on the above results, a model is considered as shown in Fig.3.3.1. Flow (A) in Fig.3.3.1 shows the typical phase transition of non-additive Ni silicide. In this case, Ni diffuses into Si to form NiSi with elevating annealing temperature in the fist stage. Further Ni diffusion at higher annealing temperature leads the phase transition from NiSi to $NiSi_2$. This causes to increase sheet resistance. By adding the additives, we expected the phase transition flow (B-1) in which the additive suppresses the phase transition from NiSi to $NiSi_2$ due to reducing Ni diffusion. However, in reality, in our experiment, flow (B-2) took place in which $NiSi_2$ layer was formed before NiSi by the suppression of Ni supply.

3.3.2 Concept of the PSMD method

To overcome this problem, I propose new process shown the flow (C) in Fig.3.3.1, "post silicidation metal doping" (PSMD) method, in which these additive metals are introduced to the pre-formed NiSi. The additive metal in the pre-formed NiSi is expected to suppress the phase transition from NiSi to $NiSi_2$ not to suppress formation of NiSi.

Phase transition model and concept of the PSMD method

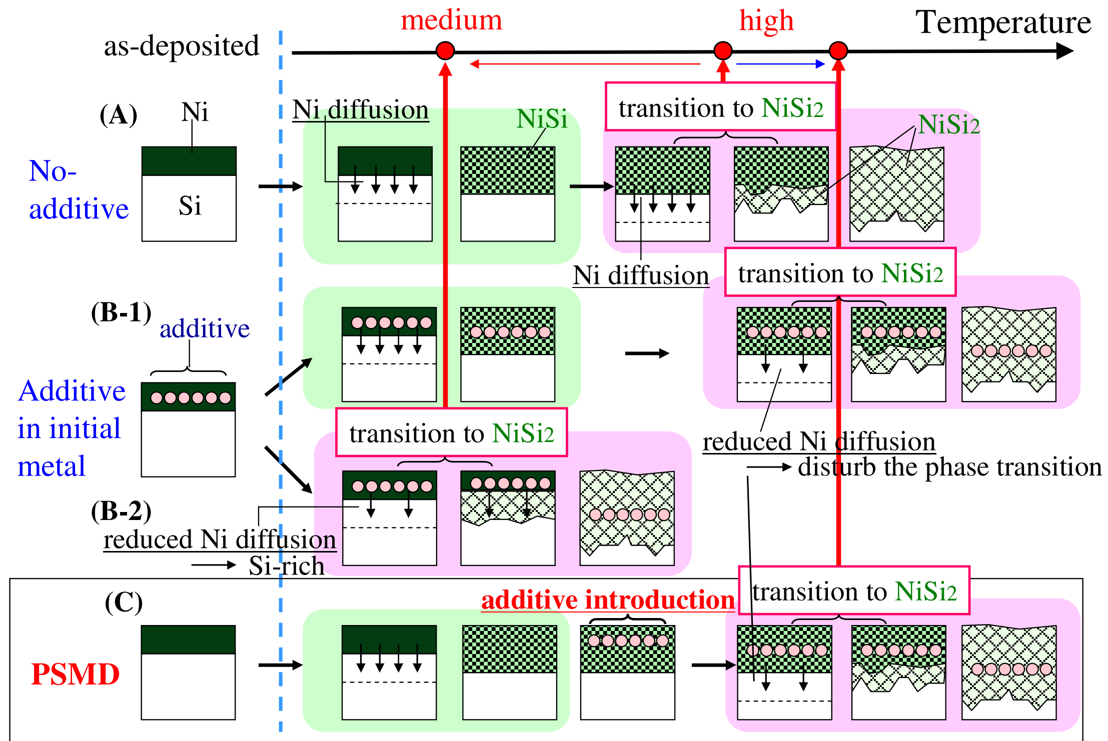


Fig. 3.3.1 Model of phase transitions and concept of the PSMD method comparing to the conventional ones.

3.3.3 Fabrication process

After the substrates are chemically cleaned by SPM and diluted HF treatments, Ni layer is deposited on the substrates by using a magnetron sputtering system.

I showed a new doping method of the additives – “post silicidation metal doping” (PSMD) –. In this method, Ni films without any additives were deposited in the same way as that described above first. The Ni deposited substrate was annealed at 400°C for 5 min *in situ* in the sputtering chamber to form NiSi layer, and then, small amount of additive metals was deposited *in situ* on the NiSi films. Finally, the sample was annealed *ex situ* by RTA in the same way as that described above. Fig.3.3.2 shows process flow and the difference of ordinary process. And for examining the effect of additive metal, I try PSMD method not to add additive, called “*in-situ*” process. The ordinary process called “*ex-situ*” process.

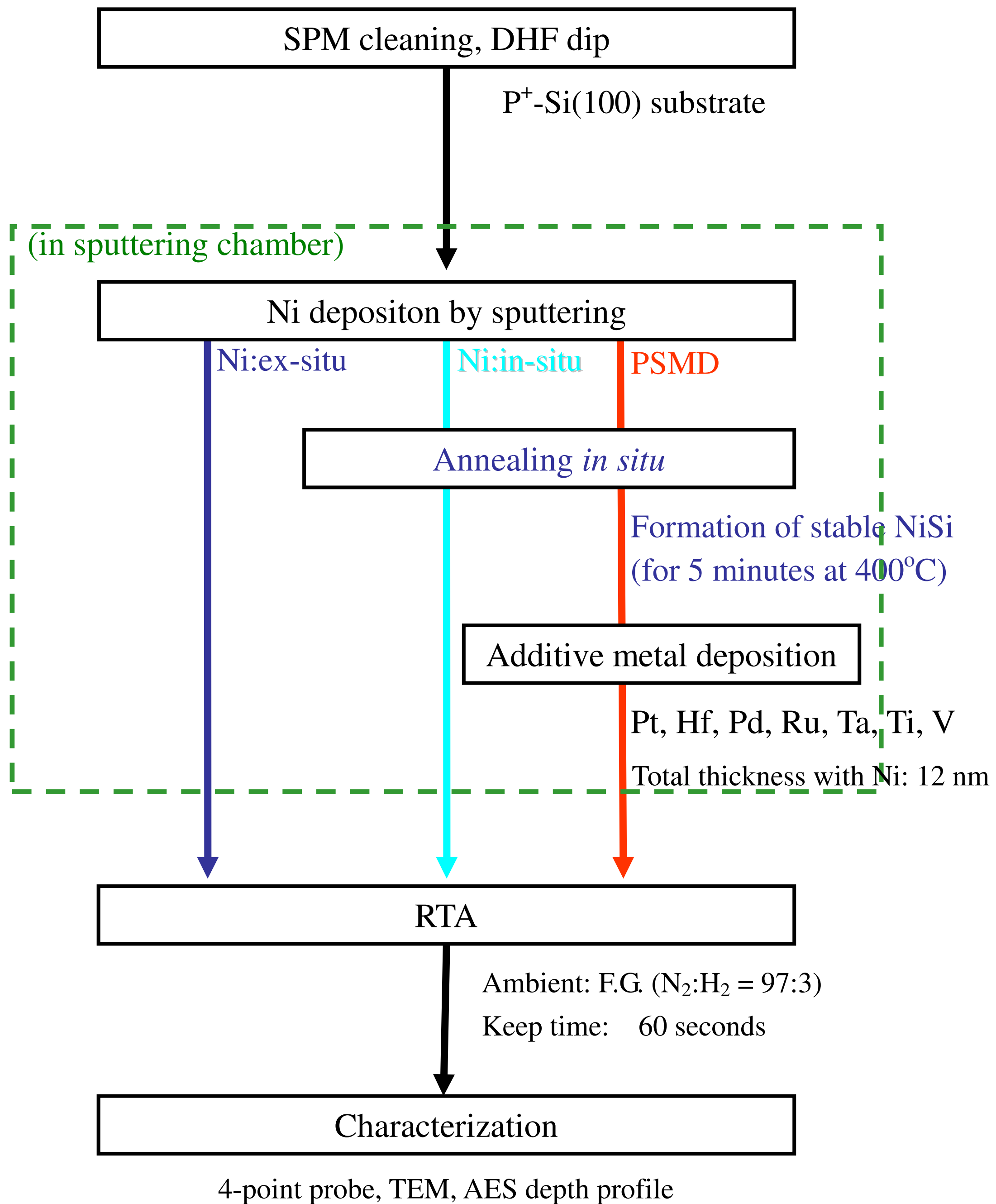


Fig. 3.3.2 Process flow of “in-situ” and the PSMD method comparing to the conventional ones.

3.4 Effect of *in-situ* annealing (no additive metals)

3.4.1 Introduction

In this section, I investigate the effect of *in-situ* annealing in sputtering chamber after Ni deposition. This is important to confirm the pure effect of additive to heat resistance of Ni silicide. So except deposition of additive, “*in-situ*” process is same to PSMD method.

3.4.2 Transformation curves

Fig. 3.4.1 shows transformation curves of Ni silicide without any additives for both the pre-formed NiSi and the non-pre-formed conventional NiSi formed by the RTA process already shown Fig.3.1.1 It should be noted that thermal stability of the pre-formed NiSi shows 30°C improvement. But the sheet resistance of the pre-formed NiSi becomes a little bit higher than conventional NiSi. This is caused to in-situ anneal diagram. Heat rate is very slow 100 °C every 7minutes by sputtering machine compareing 100 °C every 10 seconds by annealing machine. About relationship between annealing diagram and sheet resistance of NiSi, please refer to master thesis of my collaborator Mr. Xiang. The sheet resistance peak from 700 to 750°C where NiSi was on the way to transform to $NiSi_2$ becomes weak.

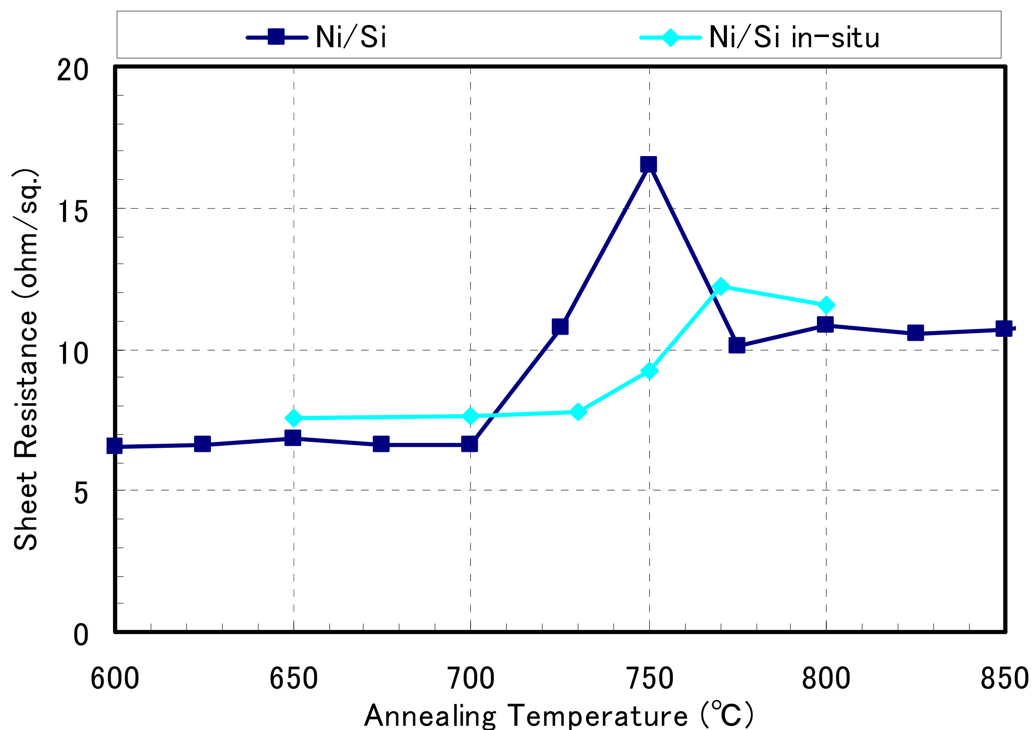


Fig. 3.4.1 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12nm)/Si structure (with or without "*in-situ* annealing").

3.4.3 Analysis of the phase of Ni Silicide

Figure 3.4.2 shows AES depth profile of Ni(12nm)/Si samples formed by conventional process ("*ex-situ*") and by "*in-situ*" process at 750 °C where NiSi was on the way to transform to $NiSi_2$. In the case of *ex-situ* sample, it seems that Si ratio of Ni is about 2. It means Ni silicide phase is $NiSi_2$. On the other hand in the case of *in-situ* sample, it seems that Si ratio of Ni is about 1.5. It means Ni silicide phase is coexistence of NiSi and $NiSi_2$.

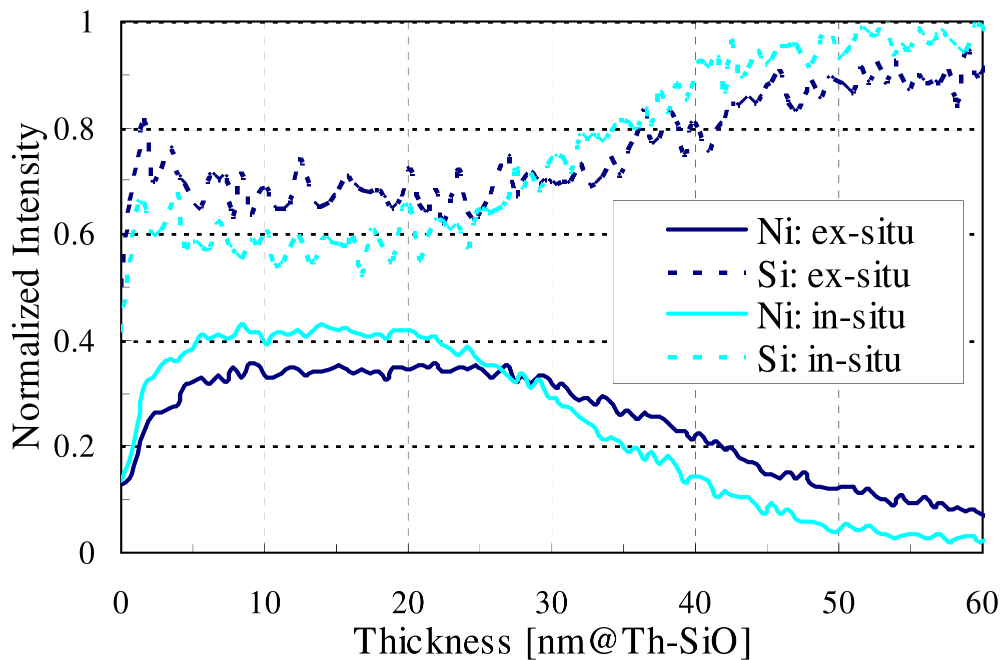


Fig. 3.4.2 AES Depth Ptrolfile of Ni(12nm)/Si structures (with or without "*in-situ* annealing") at 750°C.

3.4.4 Morphology on surface and at interface

Figure 3.4.3 shows cross-sectional TEM images of Ni(12nm)/Si samples formed by conventional process ("*ex-situ*") at 675 °C and by "*in-situ*" process at 650 °C. In both case, it seems that the silicide layer is uniform on the surface and at the interface to Si. It seems that the difference of these is practically nought about morphology.

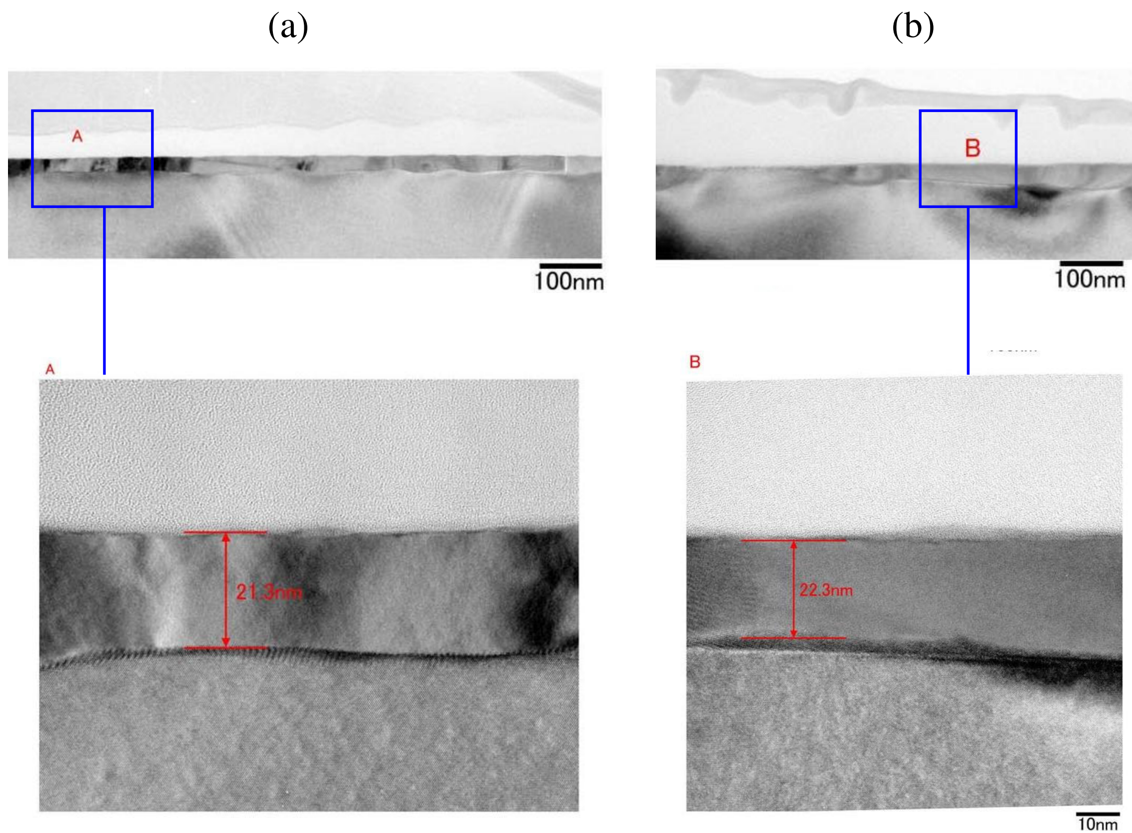


Fig. 3.4.3 TEM images of Ni(12nm)/Si structures.
(a) is formed by conventional process and annealed at 675°C.
(b) is formed by *in-situ* process and annealed at 650°C.

3.5 Effect of additive metals by PSMD method

3.5.1 Introduction

In this section, I investigate the effect of additive by PSMD method. As an additive I examine Hf, Pt, Pd, Ru, Ta, Ti and V. To make sure the pure effect of additive to heat resistance of Ni silicide, I compare the results of PSMD method with the result of "*in-situ*" process.

3.5.2 Transformation Curves

I examine Hf, Pt, Pd, Ru, Ta, Ti and V were used as metal additives. And there is improvement in the thermal stability of Ni silicide with Hf and Pt. To make comparisons, the data from the "*in-situ*" method was plotted together in each figure.

A result in case of Hf addition is shown as Figure 3.5.1. The thicknesses of Hf layer were 0.16-0.54nm. In the case of Hf 0.18nm addition in the PSMD, maximum 40°C improvement from the "*in-situ*" (pre-formed non additive) NiSi was observed. And the sheet resistance is as high as "*in-situ*" NiSi. However Hf additives of other thickness introduced in the same process did not provided any improvement in the thermal stability. The optimum Hf thickness range was very narrow.

A result in case of Pt addition is shown as Figure 3.5.2. The thicknesses of Pt layer were 0.16-1.2nm. In the case of Pt 0.16-0.60nm addition in the PSMD, maximum 40°C improvement from the "*in-situ*" NiSi was also observed. And the sheet resistance is as high as "*in-situ*" NiSi, except 0.60nm addition.

A result in case of Pd addition is shown as Figure 3.5.3. The thicknesses of Pd layer were 0.24-0.81nm. In the case of Pd addition in the PSMD, any improvement from the "*in-situ*" NiSi could not be observed well.

A result in case of Ru addition is shown as Figure 3.5.4. The thicknesses of Ru layer were 0.16-0.54nm. In the case of Ru addition in the PSMD, any improvement from the "*in-situ*" NiSi could not be observed.

A result in case of Ta addition is shown as Figure 3.5.5. The thicknesses of Ta layer were 0.24-0.81nm. In the case of Ta addition in the PSMD, any improvement from the "*in-situ*" NiSi could not be observed.

A result in case of Ti addition is shown as Figure 3.5.6. The thicknesses of Ti layer were 0.24-0.81nm. In the case of Ti addition in the PSMD, any improvement from the "*in-situ*" NiSi could not be observed.

A result in case of V addition is shown as Figure 3.5.7. The thicknesses of V layer were 0.08-0.27nm. In the case of V addition in the PSMD, any improvement from the "*in-situ*" NiSi could not be observed.

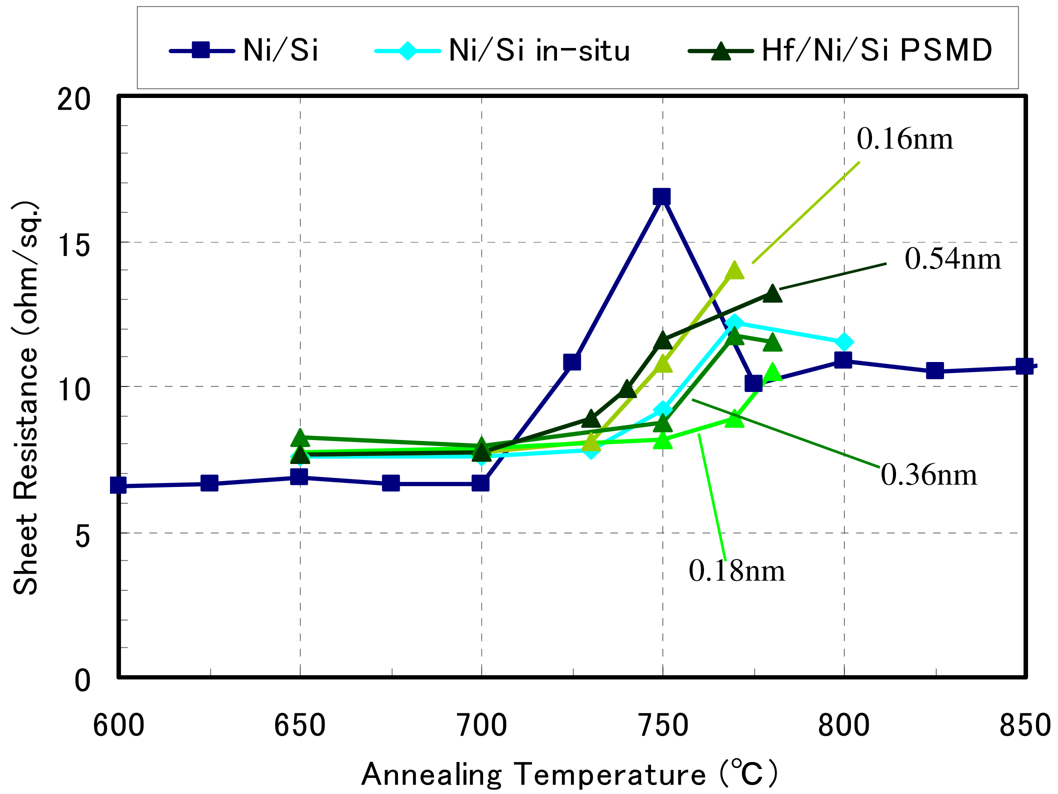


Fig. 3.5.1 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12nm)/Si (without or with *in-situ* annealing) and Hf(0.16-0.54nnm)/Ni/Si (PSMD) structures.

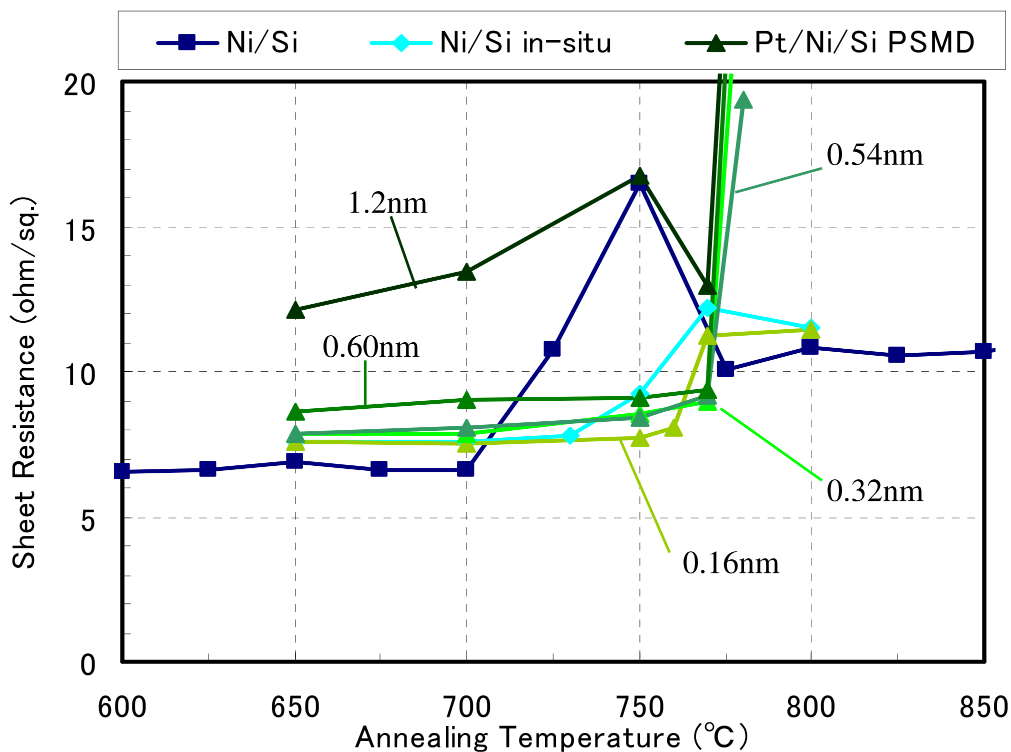


Fig. 3.5.2 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and Pt(0.16-1.2nnm)/Ni/Si (PSMD) structures.

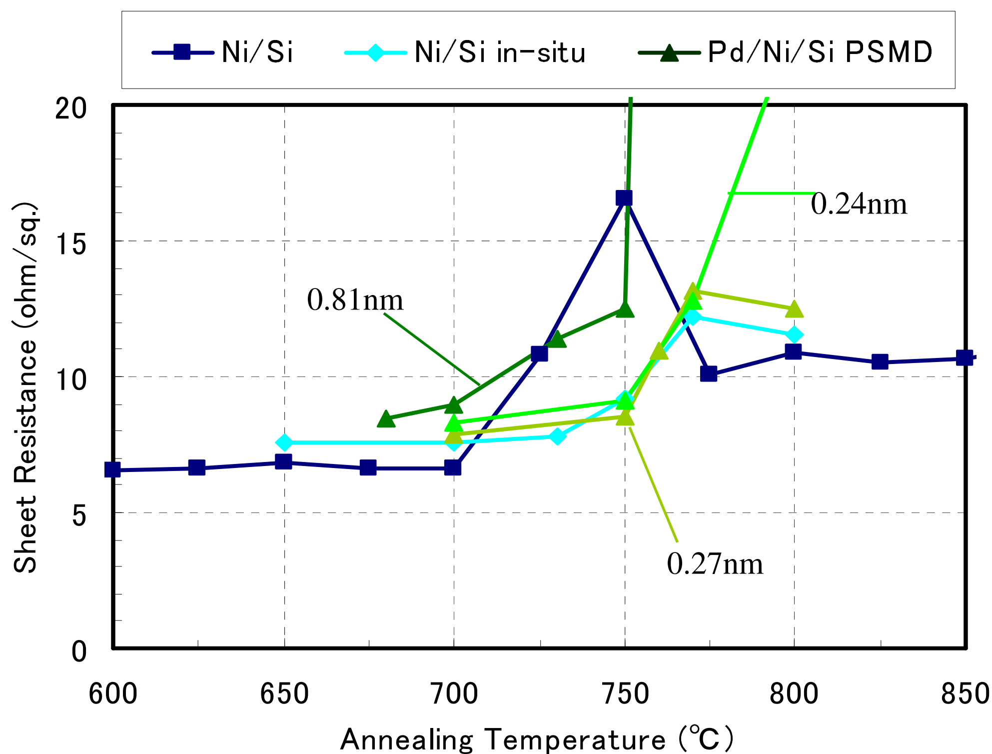


Fig. 3.5.3 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and Pd(0.24-0.81nnm)/Ni/Si (PSMD) structures.

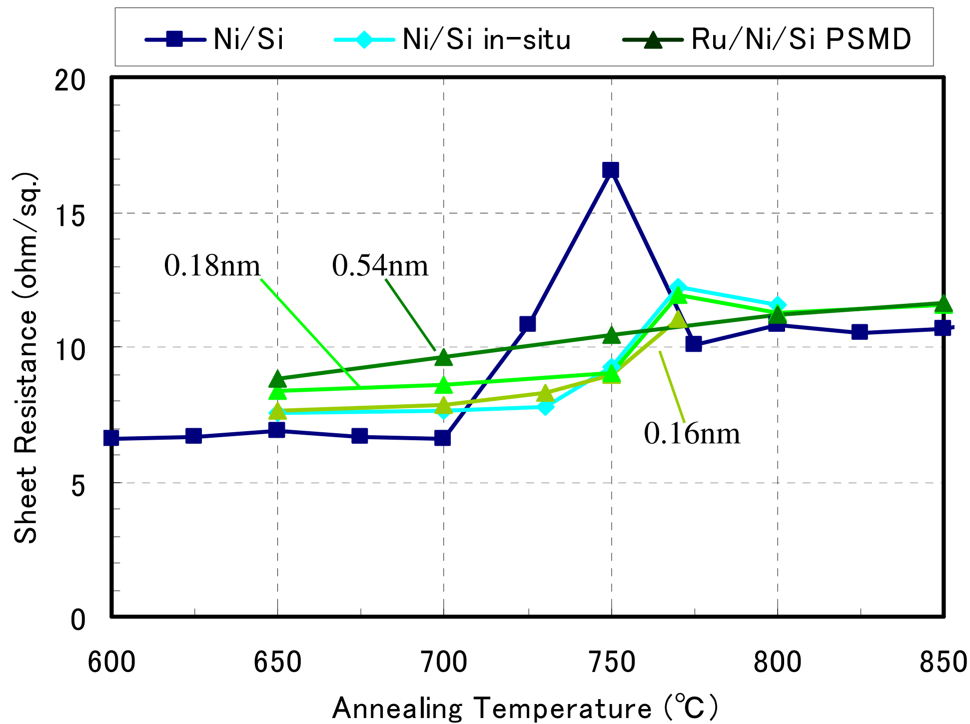


Fig. 3.5.4 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and Ru(0.16-0.54nnm)/Ni/Si (PSMD) structures.

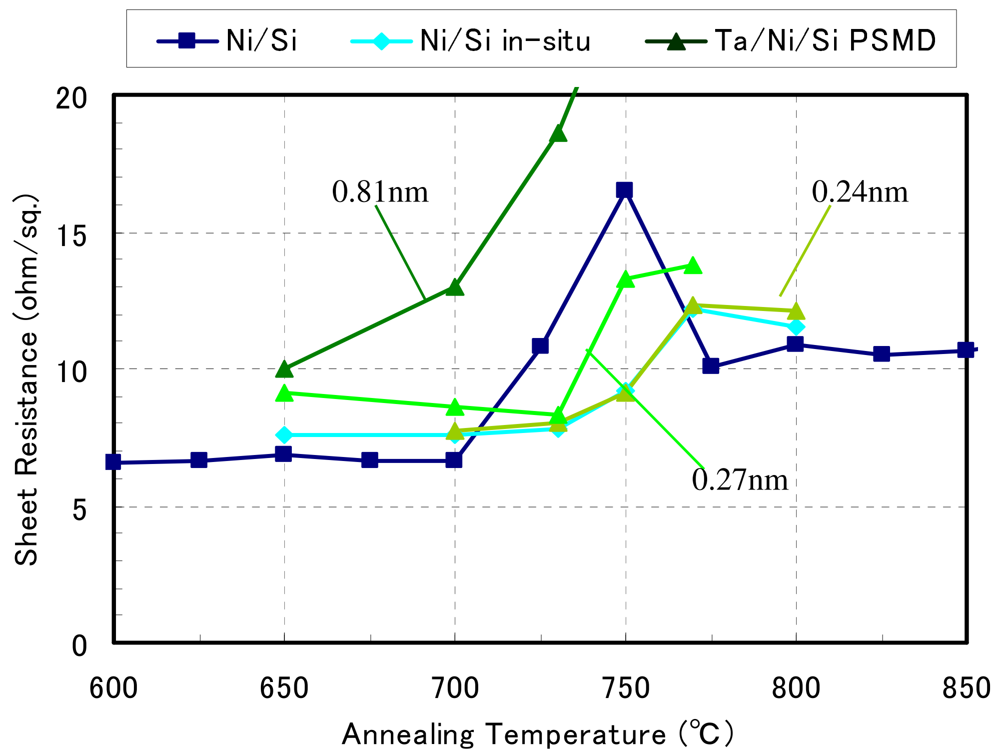


Fig. 3.5.5 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and Ta(0.24-0.81nnm)/Ni/Si (PSMD) structures.

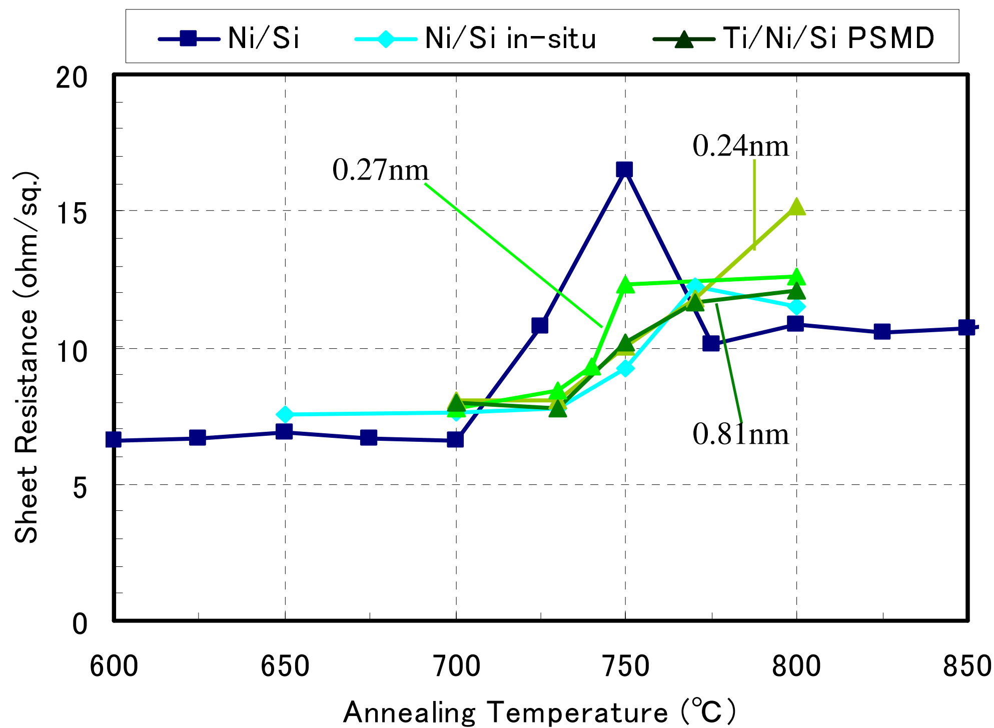


Fig. 3.5.6 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and Ti(0.24-0.81nnm)/Ni/Si (PSMD) structures.

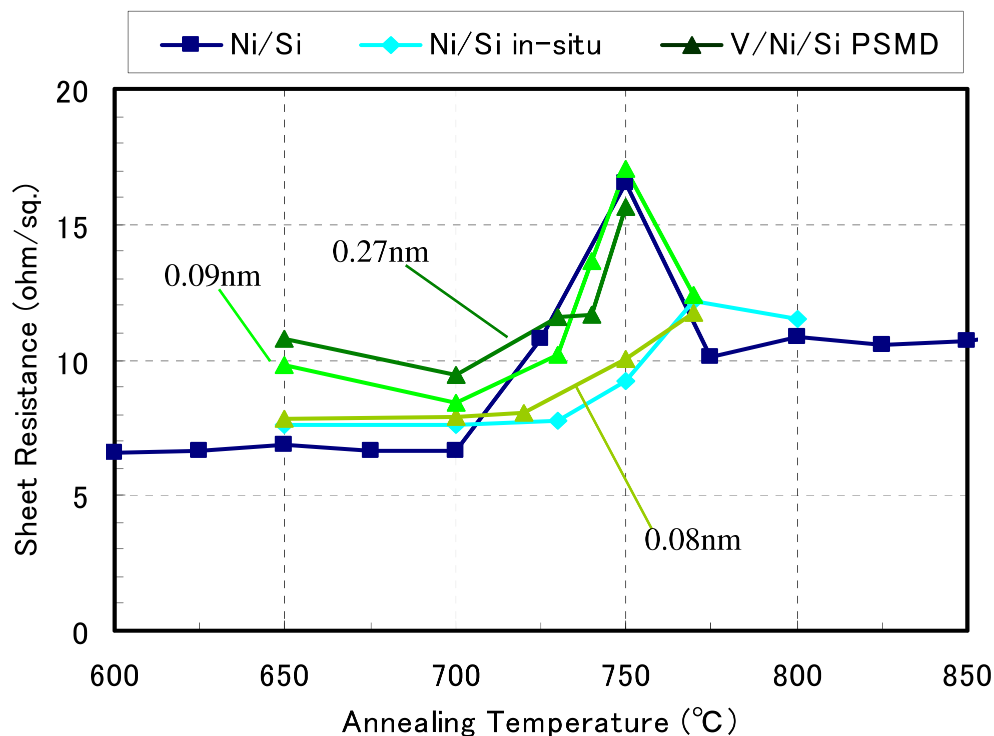


Fig. 3.5.7 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and V(0.08-0.27nnm)/Ni/Si (PSMD) structures.

3.5.3 Analysis of the phase of Ni Silicide

Figure 3.5.8 shows AES depth profile of Pt additions in PSMD process at 750 ^{o}C where NiSi was on the way to transform to $NiSi_2$ changing thickness of Pt additive. It is said that the silicide phase at 750 ^{o}C does not almost depend on thickness. But on thichest sample Si ratio of Ni is a little higher. So in fig.3.5.9 only Pt 0.16nm addition sample is compared with “*ex-situ*” NiSi. In the case of “*ex-situ*” NiSi, it seems that Si ratio of Ni is about 2. It means Ni silicide phase is $NiSi_2$. On the other hand in the case of Pt 0.16nm addition in PSMD sample, it seems that Si ratio of Ni is about 1.2. It means Ni silicide phase is coexistence of NiSi and $NiSi_2$. But it is mainly NiSi.

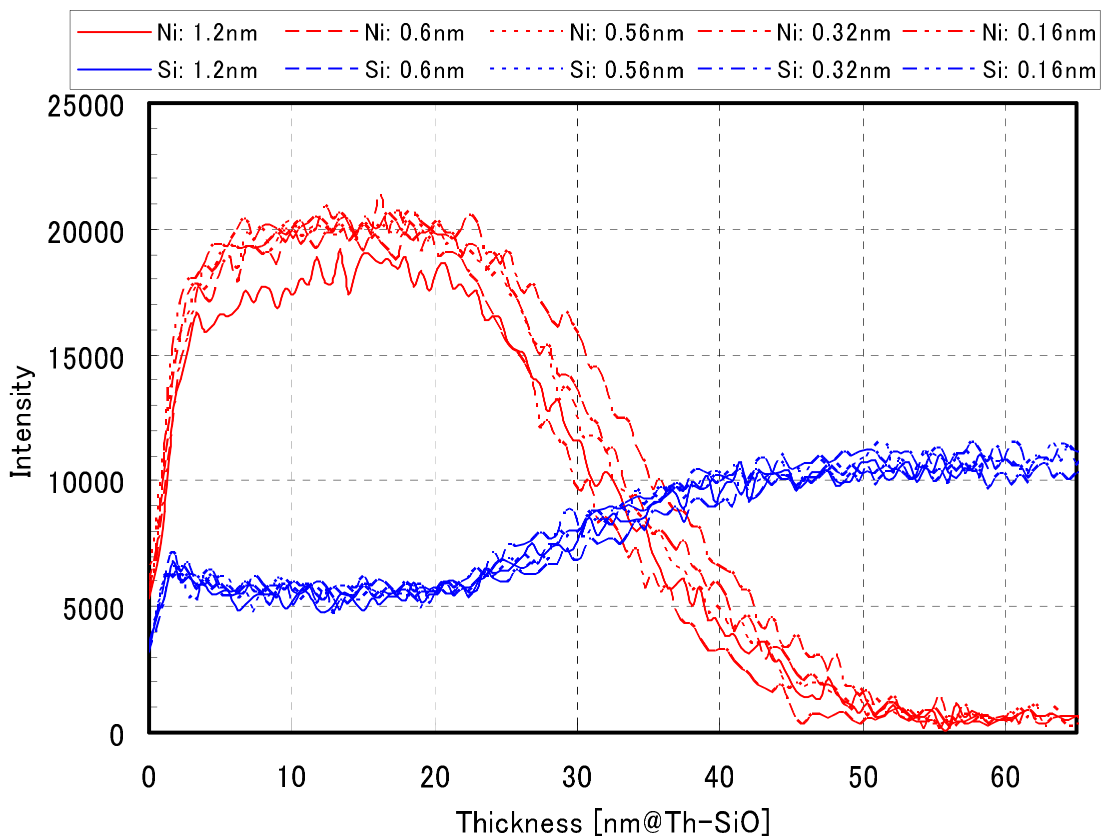


Fig. 3.5.8 AES Depth Ptrolfile of Pt/Ni/Si structures formed by PSMD process annealed at 750°C. The thicknesses of Pt layer were 0.16-1.2 nm.

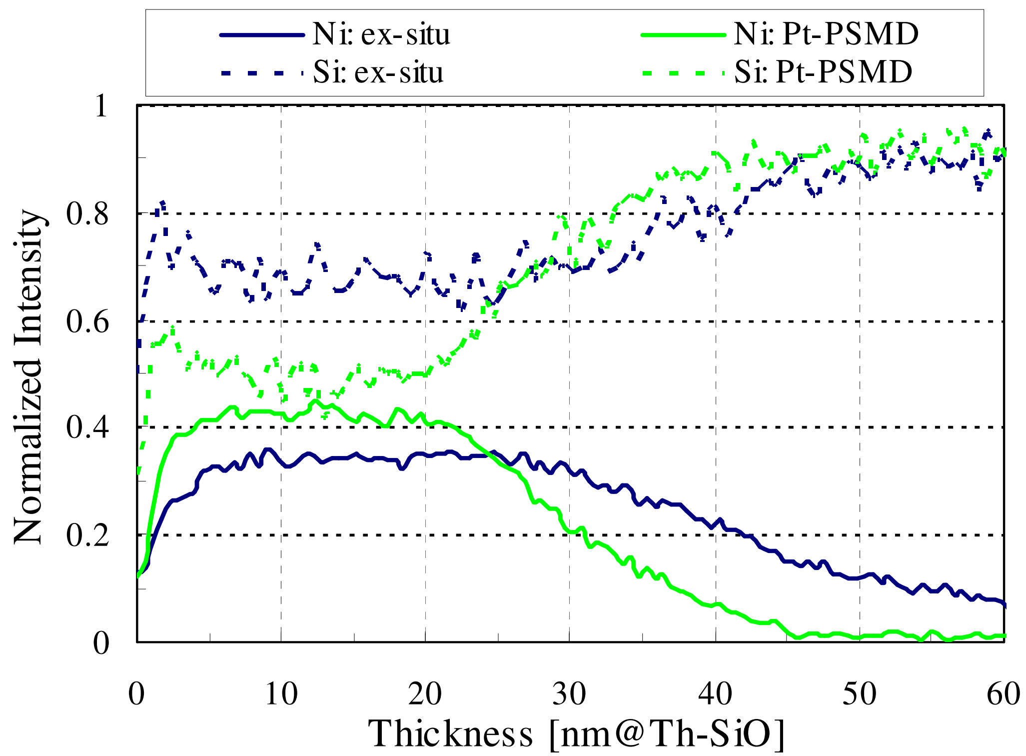
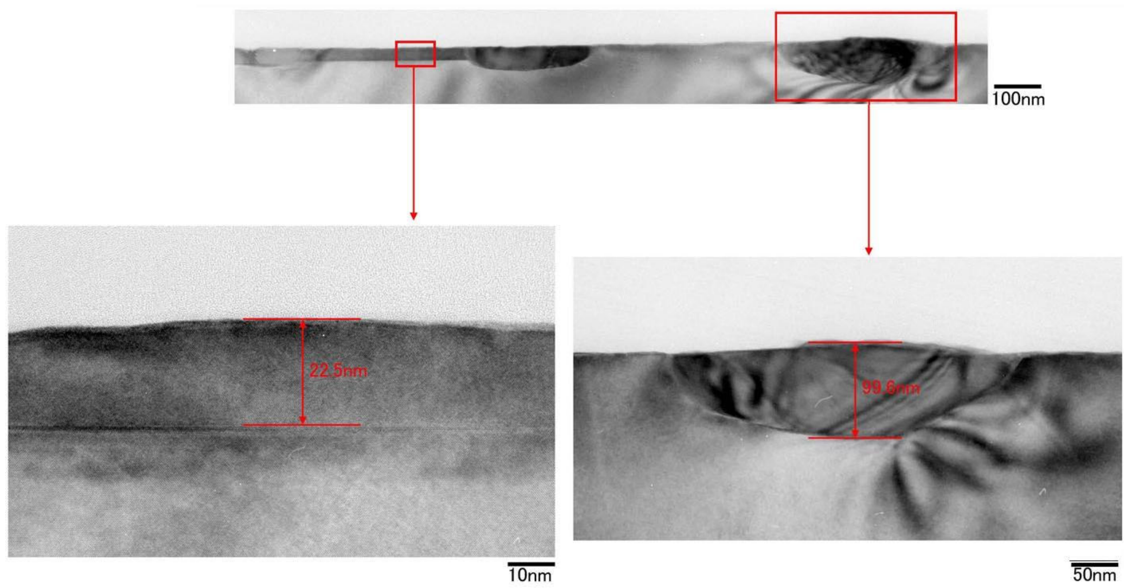


Fig. 3.5.9 AES Depth Ptrolfile of Ni(12nm)/Si formed by ex-situ (conventional) process and Pt(0.16nm)/Ni(12nm)/Si formed by PSMD process annealed at 750°C.

3.5.4 Morphology on surface and at interface

Figure 3.5.10 shows cross-sectional TEM images of Ni(12nm)/Si samples formed by conventional process ("*ex-situ*") and Pt(0.16nm)/Ni(12nm)/Si formed by PSMD process at 750 ^{o}C. The TEM observation verified the suppression of agglomeration for the Pt additive samples in contrast with the agglomeration for the non additive sample. So the silicide layer is very uniform on the surface and at the interface to Si.

(a) Ni/Si (ex-situ process)



(b) Pt/Ni/Si (PSMD process)

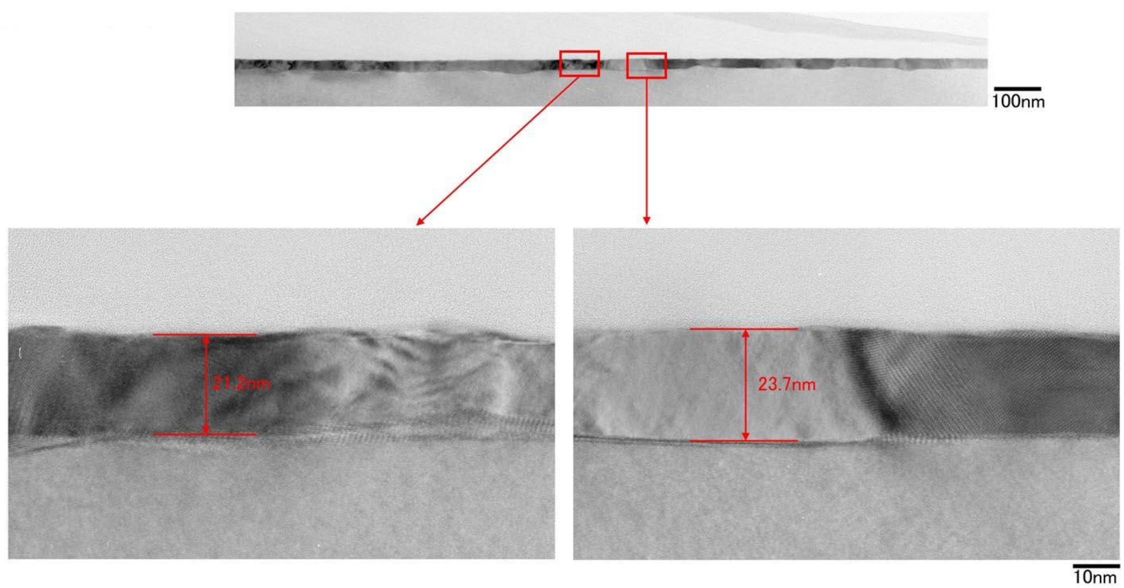


Fig. 3.5.10 TEM images of (a) Ni(12nm)/Si formed by ex-situ (conventional) process and (b) Pt(0.16nm)/Ni(12nm)/Si formed by PSMD process annealed at 750°C.

3.5.5 Transformation Curves in the latest investigation

Though I examined Hf, Pt, Pd, Ru, Ta, Ti and V as metal additives in PSMD process, I investigated also Al and Sn. In this study, I show only transformation curve about those samples. And in the case of those samples, the thickness of Ni layer is 12nm regardless of the thickness of additive layer. Because the thickness of Ni layer effect alittle heat resistance and sheet resistance of NiSi indicated in section 3.1.4. And I eximine Pt addition which improved heat resistance, again

A result in case of Pt addition is shown as Figure 3.5.11. The structure of added sample is Pt(0.32nm)/Ni(12nm)/Si. Compared with above results in Fig. 3.5.1 the heat resistance of NiSi phase improve another 5°C and sheet resistance of NiSi phase lower than "*in-situ*" NiSi.

A result in case of Al addition is shown as Figure 3.5.12. The thicknesses of Al layer were 0.32-4.0nm. In the case of Al 0.32-2.0nm addition in the PSMD, maximum 30°C improvement from the "*in-situ*" NiSi was also observed. And the sheet resistance is as high as "*ex-situ*" NiSi, except 2.0nm addition. It is particularly worth noting that this additive shows not only improvement of heat resistance but also an insignificant effect on sheet resistance at other region. It is said that heat resistance doesn't depend on thickness so.

A result in case of Sn addition is shown as Figure 3.5.13. The thicknesses of Sn layer were 0.32 and 0.65nm. In the case of Sn addition in the PSMD, about 50°C improvement from the "*in-situ*" NiSi was also observed. And the sheet resistance is higher than "*ex-situ*" NiSi but lower than "*in-situ*" NiSi.

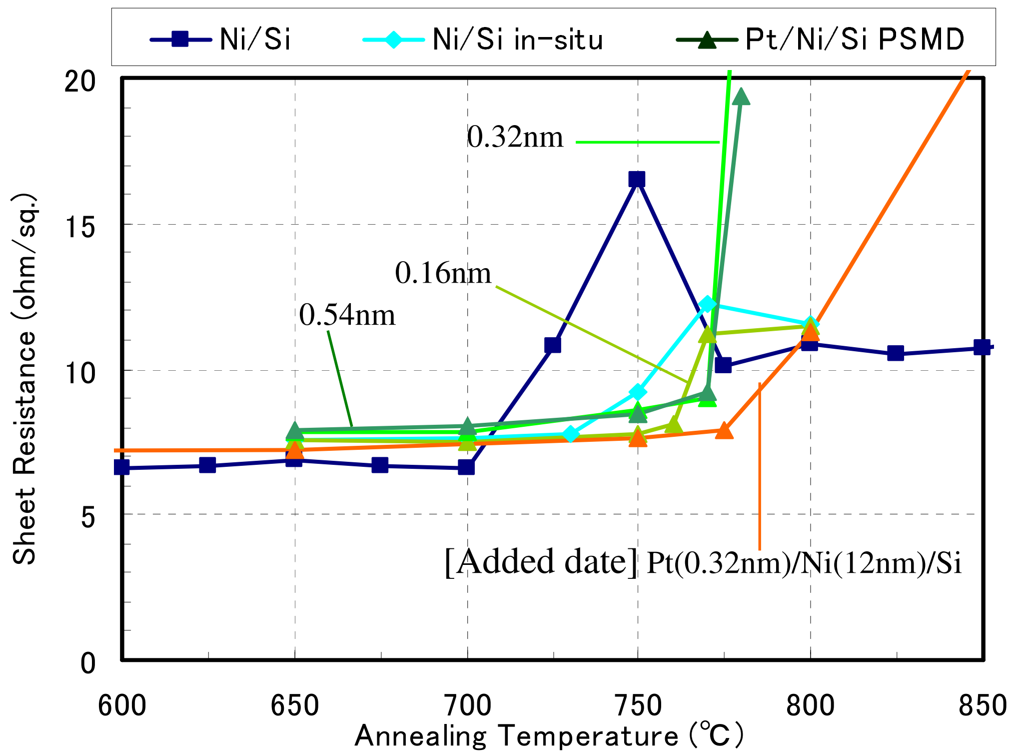


Fig. 3.5.11 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and Pt(0.16-0.54nm)/Ni/Si (PSMD) structures.

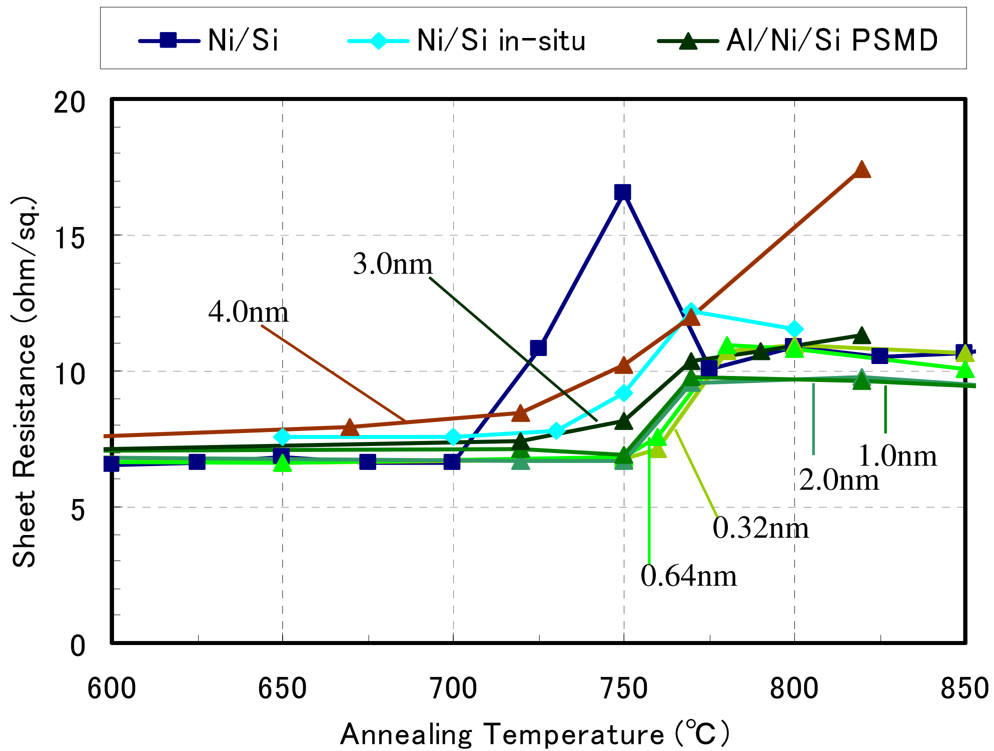


Fig. 3.5.12 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and Al(0.32-4.0nnm)/Ni(12nm)/Si (PSMD) structures.

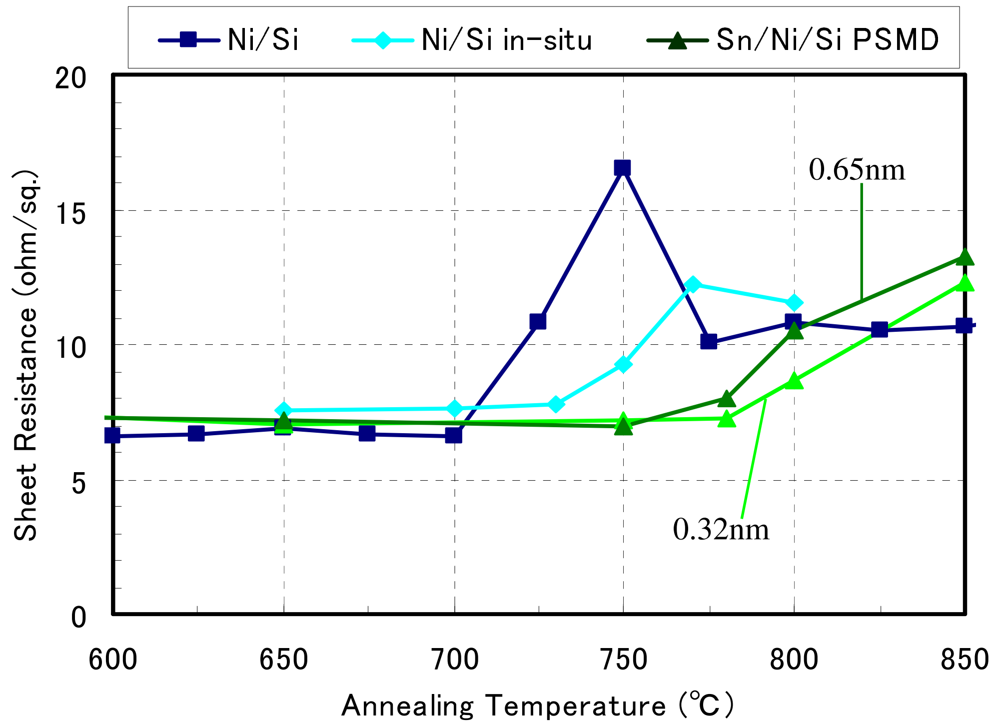


Fig. 3.5.13 Tranformation curve of Ni silicide for Ni(12nm)/Si (without or with *in-situ* annealing) and Sn(0.32, 0.65nnm)/Ni(12nm)/Si (PSMD) structures.

3.6 Effect of additive metals by PSMD method on narrow line

3.6.1 Introduction

In this section, based on the above results on large-area substrate, I investigate on narrow line for the 45 nm node CMOS process. As an additive I examine Hf, Pt and Ta. all the while I investigated on P^+ substrate. But on a 45 nm CMOS TEG structure there are N+ diffusion area and both P^+- and N^+- poly-Si lines.

3.6.2 Fabrication process

At first TEGs are chemically cleaned by diluted HF treatments to remove natural oxide. Next Ni is deposited about 12nm (depended on the thickness of additive to become the total thickness 12nm) on TEGs by using a magnetron sputtering system. Those samples are annealed at 400°C to form stable NiSi. After that, unreactive metal was etched by SPM. So additive metals are deposited by sputtering. These samples are annealed for 60 seconds at various temperatures in forming gas (3%-H_2) ambient.

3.6.3 Sheet Resistance on narrow line

Based on the above results, I examine on a 45 nm CMOS TEG structure. At first Fig. 3.6.1 shows sheet resistance on each patterned narrow line of P^+ and N^+ area on diffusion (called OD in figure) and poly-Si (called GA) lines as a function of silicidation temperature. The results show that the NiSi endurance temperatures for the P^+ diffused lines is about 50°C higher than for large-area P^+ substrate. And it for P^+ poly-Si is a little higher than for the P^+ diffused layer, but on narrow line under 100nm it for P^+ poly-Si is lower than for the P^+ diffused layer. On the other hand it for N^+ poly-Si is about 20°C lower than for the N^+ diffused layer.

Fig. 3.6.1 show Pt, Hf and Ta PSMDs were applied on a 45 nm CMOS TEG structure. It was found that only Pt PSMD shows the thermal stability improvement for both N^+- and P^+- diffusion and poly-Si lines with 25-75°C without narrow line effects. On the contrary, however, Hf PSMD shows degradation of the thermal stability presumably because of the narrow Hf thickness window as shown in Fig. 3.5.1. It was found that Ta PSMD shows the thermal stability improvement for N^+- diffusion and poly-Si lines with 25-50°C without narrow line effects.

Fig. 3.6.1 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12)/Si structure on both N^+- and P^+- diffusion (OD) and poly-Si (GA) lines from 60 to 1000nm.

	Si		500	600	625	650	675	700	725	750	775	800
P-type	GA	Ni ex-situ	○	○	○	△	▲	△	△	△	×	×
		Pt: 0.16nm		○	▲	○	○	△				
		Pt: 0.32nm				○	○	○	×	△	×	
		Hf: 0.18nm			○	○	×	△	△	×		
		Hf: 2.0nm		△	△	×	×	×				
		Ta: 2.0nm		△	○	×	×	×				
	OD	Ni ex-situ	○	○	○	○	○	○	○	○	×	×
		Pt: 0.16nm		○	○	○	△	△				
		Pt: 0.32nm				○	○	○	○	○	×	
		Hf: 0.18nm			○	○	○	○	△	×		
		Hf: 2.0nm		○	▲	×	×	×				
		Ta: 2.0nm		○	▲	×	×	×				
N-type	GA	Ni ex-situ	○	○	○	○	×	×	×	×	×	×
		Pt: 0.16nm		○	○	○	▲	×				
		Pt: 0.32nm				○	○	×	×	×	×	
		Hf: 0.18nm			○	○	×	×	×	×		
		Hf: 2.0nm		○	○	○	×	×				
		Ta: 2.0nm		○	○	○	▲	×				
	OD	Ni ex-situ	○	○	△	○	×	×	×	×	×	×
		Pt: 0.16nm		○	○	○	○	×				
		Pt: 0.32nm				○	▲	▲	×	×	×	
		Hf: 0.18nm			○	○	▲	×	×	×		
		Hf: 2.0nm		○	○	○	▲	×				
		Ta: 2.0nm		○	○	○	○	▲				

Fig. 3.6.2 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12nm)/Si, Pt(0.16, 0.32nm)/Ni(12nm)/Si, Hf(0.18nm)/Ni(12nm)/Si, Hf(2.0nm)/ Ni(10nm)/Si and Ta(2.0nm)/Ni(10nm)/Si structures on both N^+- and P^+- diffusion (OD) and poly-Si (GA) lines.

○ : lower than the sheet resistance of "$NiSi_2$ on large-area substrate"

△ : slightly higher than the sheet resistance of "$NiSi_2$ on large-area substrate" in the case of narrow line

▲ : slightly higher than the sheet resistance of "$NiSi_2$ on large-area substrate"

× : much higher than sheet resistance of "$NiSi_2$ on large-area substrate"

【Chapter 4】
Conclusion

4.1 Conclusion of this study

The effect of silicidation process and metal doping on the NiSi thermal stability were studied for the 45 nm node CMOS process.

At first, pure Ni(12nm) thin film was investigated. Examined transformation curves for detail from 200°C to 950 ^{o}C, I can clearly distinguish 5 stages according to the change in sheet resistance. And I focus on improvement of heat resistance of the second stage which exhibited both the lowest and constant sheet resistance was the region form 300 to 700°C at which the Ni phase was NiSi. This means to suppress to phase transition from NiSi to $NiSi_2$ and agglomeration.

Next, additions of V, Hf, Ru and Pt by bi-layer structure commonly used were examined. However, there is no improvement in the thermal stability of Ni silicide with these additives for every deposited structure. In the case of the additive metal interface between Ni and Si, Ni/M/Si, the phase transition to $NiSi_2$ occurred at low temperature. Because the additive layer between the Ni and Si suppresses the Ni supply into the Si substrate and this poor supply of Ni caused $NiSi_2$ layer rather than NiSi. On the other hand in the case of the additive metal cap structure, M/Ni/Si, around 700 ^{o}C the agglomeration occurred (and presumably due to the lower temperature transition to $NiSi_2$ because of the Hf diffusion into the Ni film, suppressing the Ni supply to the Si substrate.). But in the case of the Pt additive, the new phase a little different from NiSi is confirmed regardless of structure because Pt diffuses into Ni easily.

So, the model for the degradation mechanism was studied based on the experiments with different silicidation conditions. It was assumed that the thermal stability degradation by the additive metals occurs due to the suppression of Ni supply into the Si. We proposed “post silcidation metal doping” (PSMD) method in order to solve the problem. Only in-situ annealing in sputtering chamber after Ni deposition improved the stability about 30°C and caused a little increase of sheet resistance, because of slow

annealing diagram be sputtering machine. The combination of pre-formed NiSi and Pt, Hf, Al or Sn addition improved the stability about 80°C at maximum for P^+ Si layer. Because the phase transition to $NiSi_2$ and agglomeration were suppressed. On the other hand Pd, Ru, Ta, Ti and V did not show any improvement.

Last, based on the above results, I examine on a 45 nm CMOS TEG structure. In the case of only Ni (no additive), the NiSi endurance temperatures for the P^+ diffused layer is about 50°C higher than for large-area P^+ substrate. And it for P^+ poly-Si is a little higher than for the P^+ diffused layer, but on narrow line under 100nm it for P^+ poly-Si is lower than for the P^+ diffused layer. On the other hand it for N^+ poly-Si is about 20°C lower than for the N^+ diffused layer. Hf PSMD shows degradation of the thermal stability presumably because of the narrow optimum thickness of Hf addition. On the contrary, however, Ta PSMD shows the thermal stability improvement for both N^+-diffusion and poly-Si lines with 25-50°C without narrow line effects. And Pt PSMD shows the thermal stability improvement for both N^+- and P^+- diffusion and poly-Si lines with 25-75°C without narrow line effects. These comprehensive study of various additive metals on the same condition would be useful for designing the thermal process for future CMOS.

4.2 Subject to the future

About the results by PSMD method analysis is needed, for example around temperature to become high sheet resistance, the phase of Ni Silicide and morphology on the surface and at the interface between Ni Silicide and Si. It will make the mechanism clear and PSMD method optimization. In this study, leakage current or transistor characteristics were not examined they are very important.

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Koji Nagahiro

Yokohama, January 2006

Appendix

Here, each equipment used for this study is shown in from Fig.A-1 to Fig.A-3.

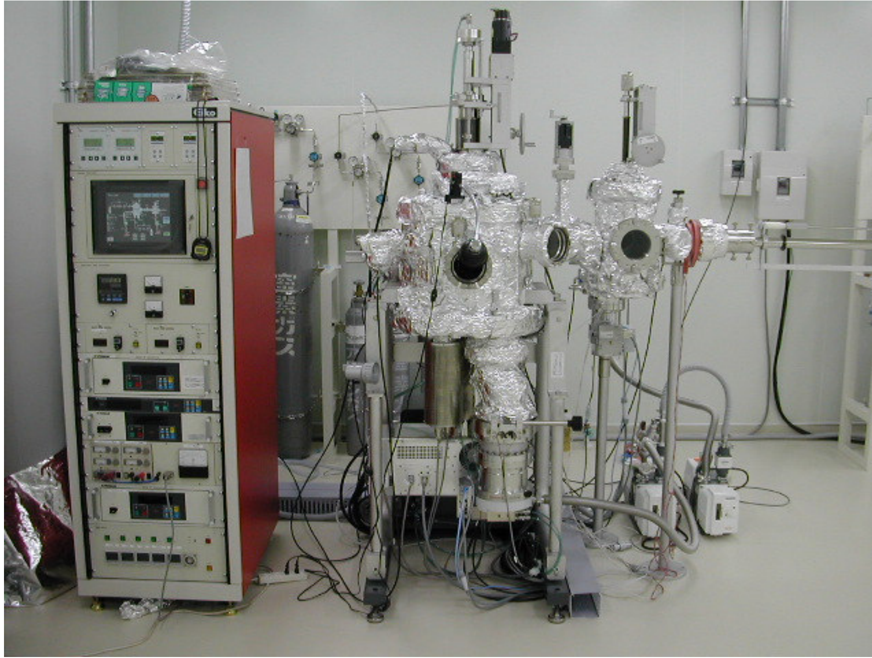

Fig.A-1 A magnetron sputter equipment for deposition of Ni and Hf
(Multi-target sputtering system, EIKO・Engineering Co. Ltd.)

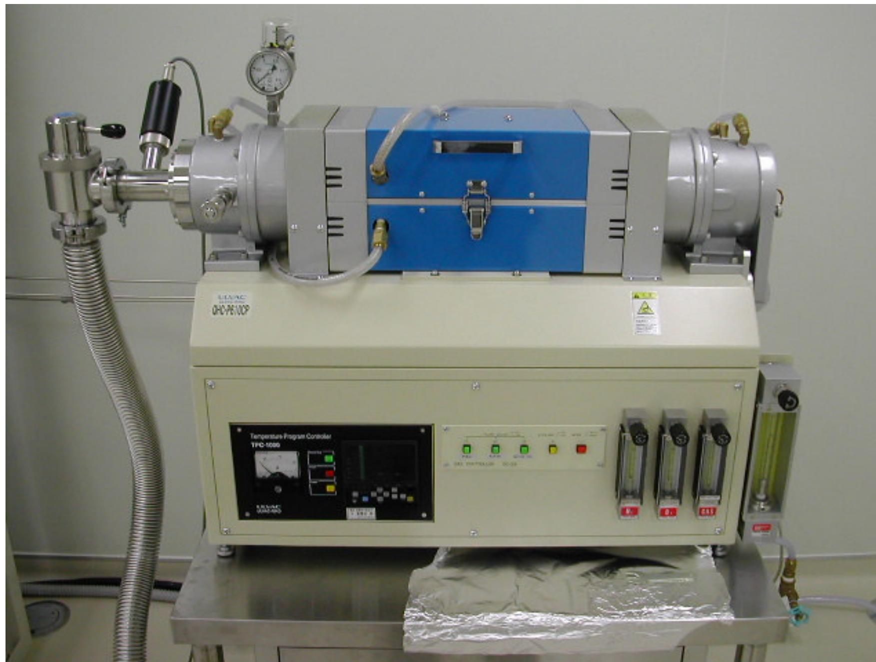

Fig.A-2 Rapid Thermal Annealing (RTA) equipment
(QHC Series, ULVAC-RIKO Co. Ltd.)

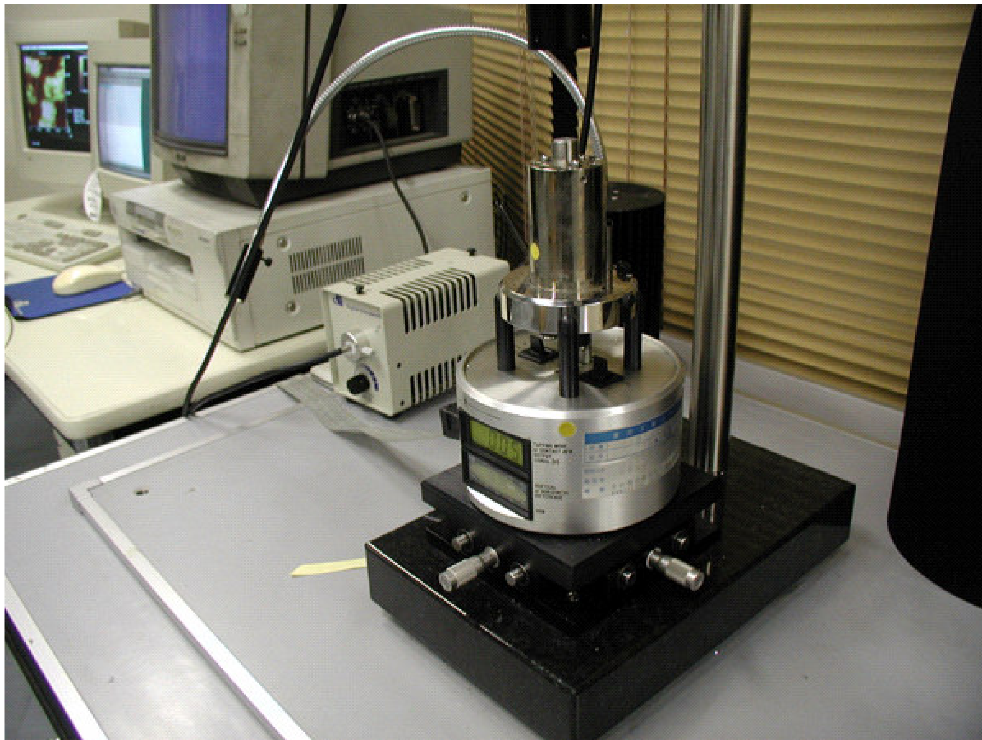

Fig.A-3 AFM equipment for observation of surface morphology
(AFM, Nano Scope , Digital Instrument Co. Ltd.)

tyoe	Si	width	500	600	620	625	640	650	660	675	680	700	720	725	740	750	760	775	800
P	GA	1000	○	○	○	○	○	○	○	△	○	○	○	○	○	○	○	○	
		500	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		400	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	△	
		300	○	○	○	○	○	○	○	○	○	○	○	○	○	○	×	△	
		200	○	○	○	○	○	○	○	○	○	○	○	○	△	○	○	△	
		100	○	○	○	○	○	△	○	△	○	○	×	△	×	×	×	×	
		60	○	○	○	○	○	×	○	△	○	○	△	△	△	×	×	×	
	OD	1000	○	○	○	○	○	○	○	○	○	○	○	○	○	○	×	×	
		500	○	○	○	○	○	○	○	○	○	○	○	○	○	○	△	×	
		400	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	△	
		300	○	○	○	○	○	○	○	○	○	○	○	○	○	○	△	×	
		200	○	○	○	○	○	○	○	○	○	○	○	○	○	○	×	○	
		100	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
		80	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
N	GA	1000	○	○	○	○	○	○	△	△	×	×	×	×	×	×	×	×	
		500	○	○	○	○	○	○	○	△	×	×	×	×	×	×	×	×	
		400	○	○	○	○	○	○	○	△	×	×	×	×	×	×	×	×	
		300	○	○	○	○	○	○	○	△	×	×	×	×	×	×	×	×	
		200	○	○	○	○	○	○	△	×	×	×	×	×	×	×	×	×	
		100	○	○	○	○	○	○	△	×	×	×	×	×	×	×	×	×	
		60	○	○	○	○	○	○	○	△	△	×	×	×	×	×	×	×	
	OD	1000	○	○	○	○	○	○	○	×	○	×	×	×	×	×	×	×	
		500	○	○	○	○	○	○	○	△	△	×	×	×	×	×	×	×	
		400	○	○	○	○	○	○	○	△	△	×	×	×	×	×	×	×	
		300	○	○	○	○	○	○	○	△	○	△	×	×	×	×	×	×	
		200	○	○	○	○	○	○	○	△	○	×	×	×	×	×	×	×	
		100	○	○	○	○	○	○	○	○	△	△	×	×	×	×	×	×	
		80	○	○	○	○	○	○	○	○	○	○	△	×	×	×	×	×	

○ : lower than the sheet resistance of "$NiSi_2$ on large-area substrate"

△ : slightly higher than the sheet resistance of "$NiSi_2$ on large-area substrate"

× : much higher than the sheet resistance of "$NiSi_2$ on large-area substrate"

Fig. 3.6.1 Sheet resistance of Ni silicide as a function of silicidation temperature for Ni(12)/Si structure on both N^+- and P^+- diffusion (OD) and poly-Si (GA) lines from 60 to 1000nm