Study on Characterization and Modeling of RF MOSFET

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To my mother, father and brothers

Chapter 1. Introduction

1.1 General Review of CMOS Technology

Recently, with the rapid growth of CMOS(Complementary Metal Oxide Semiconductor) technology, it comes to be considered as the mainstream due to its low cost, low power and high integration, etc. CMOS technology is also employed for RF applications. RF CMOS application is discussed in section 1.1.1.

However, with aggressive scaling down of device, several serious issues, e.g. short-channel and narrow width effects, impact ionization and gate leakage current, etc. have come out. Especially, gate leakage current is the most serious issue, because it makes difficult to realize Low Stand-by Power (LSTP) of CMOS devices. To control this, materials with high dielectric constant, so-called High-k, for gate oxide as replacement for SiO_2 have attracted attention. High-k technology is discussed in section 1.1.2.

Furthermore, modeling and simulation technology is also important for developing every areas such as device fabrication and/or circuit design, to reduce cost and time. Requirements for modeling and simulation technology is discussed in section 1.1.3.

1.1.1 RF CMOS Applications

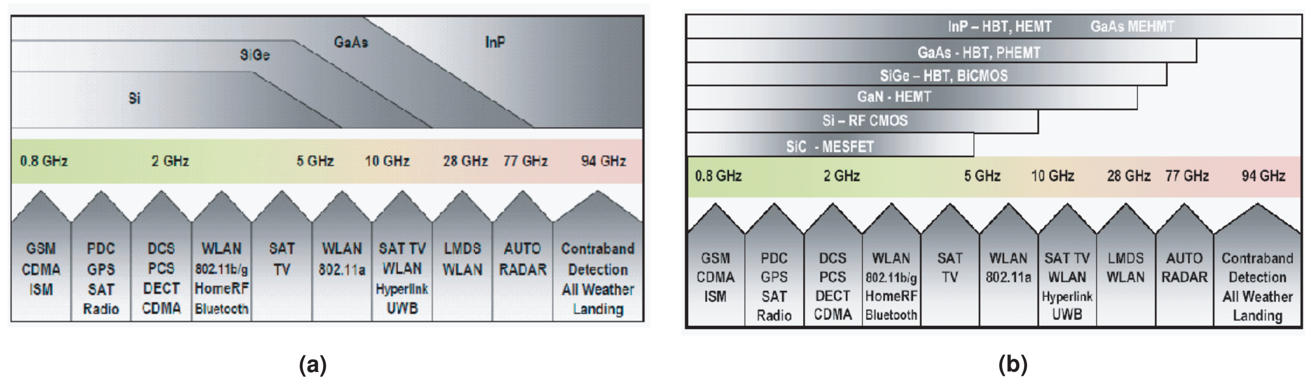


Figure 1: Application spectrum : (a) ITRS2003 Edition and (b) ITRS2005 Edition

Recently, with the developement of a highly-information-oriented society, the radio-frequency (RF) wireless communications market dramatically grows up. In the future, the demands of RF wireless technology will continue to increase all the more in various area, e.g. our daily life,

industrials and medicals. These demands are realized by the developement of semiconductor products.

Beforetime, the compound semiconductors composed of elements from group and in the periodic table such as SiGe, GaAs and InP had mainly dominated for high-speed communications and RF applications as shown in Figure 1-(a) [1]. However, RF CMOS application has been researched and developed by Universities in Europe and the United States cheifly [2][3], and then RF CMOS technology gets to be considered as the mainstream due to its low cost, low power, high integration and easy access to the technology, even though the compound semiconductors still dominate out of 5GHz as shown in Figure 1-(b) [4]. Since RF characteristics, such as the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}), of Si ULSI come to advance up to several dozen GHz (see Tabel 1[1]), available bandwidth increases and the signal frequency transmitted to interconnection of LSI comes to over GHz. Thus, CMOS technology comes to be important for both the RF technology of wireless applications and digital LSI applications. The feature that CMOS circuit configuration and multi-layer interconnections are available for RF applications are also attractive. However, there are some challenges for RF CMOS applications in the following:

1. The necessity of optimization at semi-restricted process conditions.

2. The difficulty of adopting high resistive substrate.

The solution of these challenges is necessary for RF CMOS applications.

Table 1: The roadmap of RF CMOS characteristics [5]

Year	1995	1997	1999	2001	2003	2005	2007	2009
Gate length [nm]	250	180	140	120	100	70	50	35
Gate width [um]	200	150	110	100	80	80	50	35
f_T [GHz]	39	50	65	80	105	145	205	420
f_{max} [GHz]	39	42	46	50	60	62	68	85
NF_{min} @2GHz [2]	0.3	0.26	0.22	0.17	0.14	0.13	0.1	0.08

[1] NF_{min} is the minimum noise figure. For evaluating RF device characteristics, the cutoff frequency (f_T), the maximum oscillation frequency (f_{max}) and the minimum noise figure (NF_{min}) are usually emoloyed. In this paper, f_T and f_{max} are only discussed.

1.1.2 High-k Gate Materials

As stated previously, with its agressive scaling-down of CMOS devices, CMOS technology come to play a important role in digital and/or analog applications. However, MOS structure device have a rule, so-called *the scaling rules*, which make physical effects on device complex and difficult. Table 2. shows the scaling rules for various device parameters. In this table, scaling factor is $k>1$.

Table 2: Miniaturization with scaling factor of k [6].

Parameter	**Initial**	**Scaled**
channel length	L	L/k
channel width	W	W/k
total device area	A	A/k^2
gate oxide thickness	T_{ox}	T_{ox}/k
gate capacitance	C_{ox}	$C_{ox}\times k$
junction depth	X_j	X_j/k
power supply voltage	V_{dd}	V_{dd}/k
threshold voltage	V_{th}	V_{th}/k
substrate doping concentration	N_{SUB}	$N_{SUB}\times k$
S/D doping concentration	$N_{S/D}$	$N_{S/D}\times k$

As to gate oxide thickness T_{ox} which plays an important role in MOS structure device, with scaling aggressively, T_{ox} become too thin and the gate leakage current density will become increase as shown in Figure 2. This is the most serious issue in Si MOS device.

To control the gate leakage current, many materials as replacaement for SiO_2 which have a high dielectric constant, have been researched. Other keywords for High-k are its band gap, band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility and reliability. In this thesis, sub-100 nm RF CMOS with HfSiON high-k gate dielectrics will be evaluated.

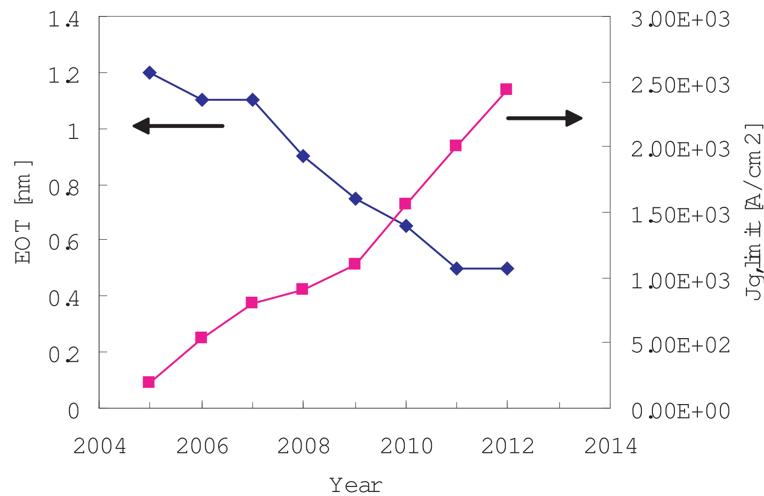


Figure 2: Prediction of equivalent oxide thickness and the maximum gate leakage current density variation [4]

1.1.3 Requirements for Modeling and Simulation

To reduce development cycle times and costs which are pretty important factors in a commercial sense, modeling and simulation are one of the few enabling methodologies. With the continuous developing of device modeling and simulation, it will realize to reduce costs shown in Figure 3. predicted by [4].

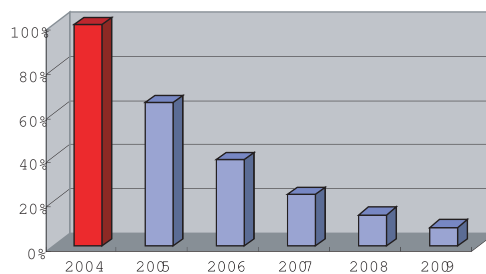


Figure 3: Technology-development cost reduction (due to TCAD)

The flowchart from device fabrication to circuit design is simply shown in Figure 4. Device parameters are extracted from fabricated device, and then extracted parameters are used for

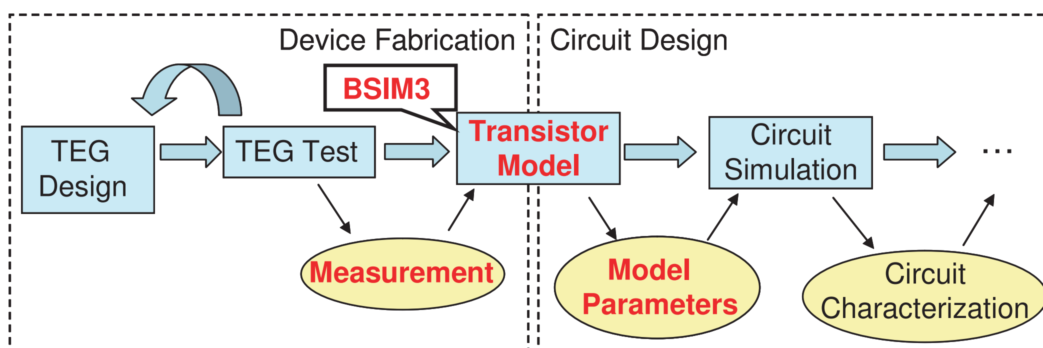


Figure 4: Illustration of the flowchart from device fabrication to circuit design

circuit design if available.

The purpose of parameter extraction is to obtain the most accurate model parameters possible directly from the measured data. Over 100 transistor models, including Level 1, Level 2, Level 3, BSIM, HSPICE Level 28, BSIM2, BSIM3, Model 9, EKV Model and BSIM4, has already existed and developed for digital, analog and mixed-signal applications. The model for the intrinsic device should be derived with the inclusions of most, if not all, important physical effects in a modern MOSFET, such as normal and reverse short-channel and narrow width effects, channel length modulation, drain induced barrier lowering (DIBL), velocity saturation, mobility degradation due to vertical electric field, impact ionization, band-to-band tunneling, polysilicon depletion, velocity overshoot, self-heating, channel quantization. Also, the continuities of small signal parameters such as transconductance G_m, channel conductance G_{ds} and the intrinsic transcapacitances must be modeled properly.

Recently, these models all are extended for use in RF applications. However, at RF region, as the parasitic componets influence to device performance severely, it is difficult to predict device behavior accurately compared to the MOSFET modeling for both digital and analog applications at DC and low frequencies. Therefore the RF modeling accuracy of the existing CMOS compact model in commercial circuit simulators is not satisfactory. As stated previously, with the fast growth in wireless communication market, RF designers have begun to explore the use of CMOS devices in RF circuits. Thus, accurate and efficient RF MOSFET models are required. A common modeling approach for RF applications is to build sub-circuits based on MOSFET models that are suitable for analog applications. The accuracy of such a model

depends on how to establish a sub-circuit with the correct understanding of the device physics in high frequency operation, and how to extract parameters appropriately for the elements of the sub-circuit. Only problem is simulation time become so long.

1.2 Motivation of This Study

In this thesis, the RF performance of a 0.18 um CMOS logic technology and sub-100 nm High-k MOSFET is assessed by evaluating the cutoff and maximum oscillation frequencies (f_T and f_{max}).

As to a 0.18 um RF CMOS evaluation, five different layout devices are campared with, and verified what affects to device RF performance. In conclusion, we will propose the adequate layout device for RF application.

Secondly, sub-100 nm High-k RF MOSFET with SiON and HfSiON gate dielectric are evaluated. Up to now, RF performance for High-k RF CMOS have been hardly reported. In this work, test device measured up to 40 GHz and is also assessed by evaluating f_T and f_{max}.

1.3 Outline of the Thesis

This thesis is composed of six chapters. In this chapter, we describe the background of this study, perspective on CMOS technology, futere requirements of gate dielectrics technology(High-k) and requirements for modeling and simulation, and motivation of this study. In chapter 2, we will discuss the methodologies of two-step de-embedding and modeling with a compact model BSIM3v3. Furthermore, the methodologies of extrinsic paramter extraction for a RF CMOS transistor are also discussed. In chapter 3, the RF performance of a 0.18 um CMOS logic technology, which has already been adopted in products, will be assessed by evaluating the cutoff and maximum oscillation frequencies (f_T and f_{max}). And next, the leading-edge High-k RF CMOS will be assessed by the same method in chapter 3. for the different laid-out RF CMOS devices. In the last chapter, we will summarize our works and the conclusions will be stated with further issues and expectation for the future works.

Chapter 2. Methodology of RF Measurement and Modeling

2.1 RF Measurement

Recently, with the growth of radio-frequency (RF) wireless communications market, the requirements for RF applications increase. Therefore, at that stage of development, accurate RF measurement must be performed. It is well-known that accurate RF measurement on wafer is difficult due to system and device parasitics. So two-step correction procedure has to be done as below:

1. Calibration
   - The measurement system has to be calibrated, defining a reference plane for the S-parameter measurements at the probe tips using a standard calibration technique (SOLT, LRM etc.).

2. De-embedding
   - The on wafer parasitics have to be characterized, so that from the measurement the actual transistor two-port parameters can be obtained.

If calibration is performed exactly, S-parameters of inner reference plane can be obtained. Secondly, device parasitics must be de-embeded, which methodology is discussed in the next section.

2.1.1 De-embedding

Resistance, capacitance or inductance included in the interconnect lines or bonding pads, which could neglect approximately in DC measurements (not completely neglect as concerns the interconnect lines resistance), largely influence to device RF performance. To evaluate intrinsic device at high frequency, these parasitic components must be removed. De-embedding is the method of removing parasitic componets.

For sub-micron transistors, the extraction is very sensitive to the input/output pads de-embedding. If the de-embedding is not complete, the correct values of the equivalent circuit components from direct extraction results may not be obtained. Different de-embedding techniques have

been developed based on different calibration test structures [7]-[10]. In this section, the de-embedding procedure based on the *OPEN* and *SHORT* calibration test structures shown in Figure 5. which has been widely used in RF measurements for different technologies is introduced.

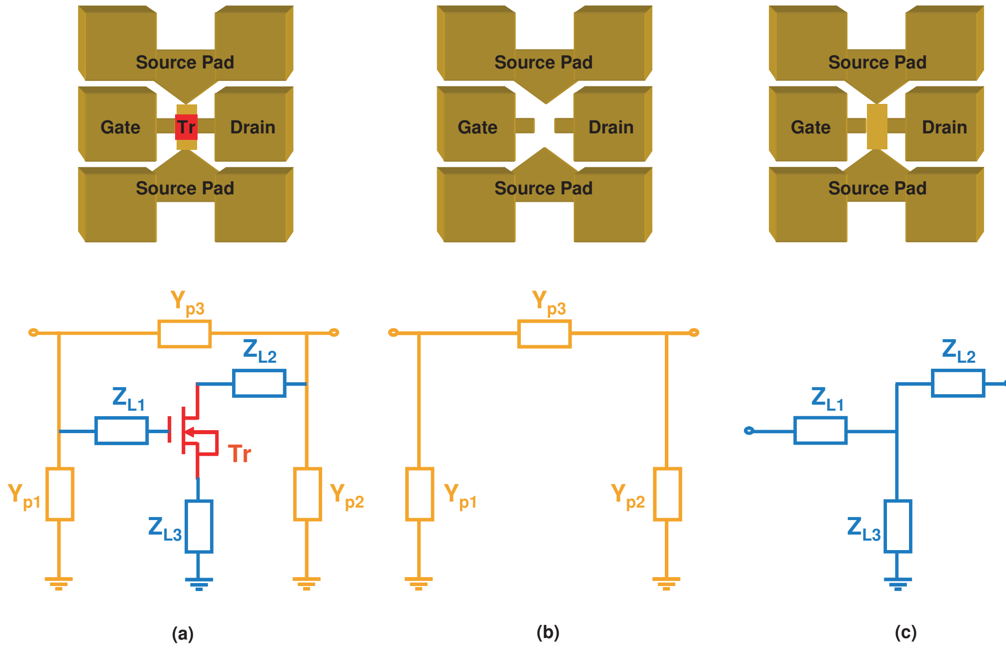


Figure 5: Illustrations of the test structures for a two-step calibration of S-parameter measurements; (a) test structure with DUT and equivalent circuit used for the two-step method including all parasitics surrounding the transistor. ; (b) *OPEN* test structure and equivalent circuit used for the two-step method including the parallel parasitics Y_{p1}, Y_{p2} and Y_{p3}. ; (c) *SHORT* test structure and equivalent circuit used for the two-step method including the series parasitics Z_{L1}, Z_{L2} and Z_{L3}.

A suitable equivalent circuit illustration of a DUT with its surroundings is given in Figure 5-(a). It shows the actual transistor as a two-port, embedded in parasitics of the interconnect lines and bonding pads, i.e. both the parallel parasitics Y_{p1}, Y_{p2} and Y_{p3} and the series parasitics Z_{L1}, Z_{L2} and Z_{L3} surrounding the transistor.

An *OPEN* interconnect pattern as is shown in Figure 5-(b). This measurement provides us with the *OPEN* Y-parameters, Y_{OPEN}. As a transistor measurement includes all parasitics surrounding the transistor, Y_{DUT} are obtained. As first step, to remove the parallel parasitics, Eq.(2-1) is done.

$$Y_{Tr} = Y_{DUT} - Y_{OPEN} \tag{2–1}$$

For low impedance or high transconductance devices, the series parasitics in the interconnect lines must be taken into account, even at fairly low frequencies. Thus, an *SHORT* pattern shown in Figure 5-(c) must be measured, providing the *SHORT* Y-parameters, Y_{SHORT}. This result is used to determine losses and phase rotation in the interconnect lines.

Assuming such an equivalent circuit, the series impedances can now easily be found from the short measurement by assuming a T-network model with impedances Z_{L1}, Z_{L2} and Z_{L3} as shown in Figure 5-(c). The *SHORT* Y-parameters are first corrected for parallel parasitics obtained from the *OPEN* measurement and transformed to Z-parameters:

$$\begin{pmatrix} Z_{L1} + Z_{L3} & Z_{L3} \\ Z_{L3} & Z_{L2} + Z_{L3} \end{pmatrix} = (Y_{SHORT} - Y_{OPEN})^{-1} \tag{2–2}$$

Simple mathematics show that for a configuration as in Figure 5-(a) with impedances Z_{L1}, Z_{L2} and Z_{L3} in series with a linear two-port the Z-parameters of the two-port can be found by subtraction of the Z-parameter matirix for the T-network from that of the total.

The actural transistor Y-parameters can be obtained from:

$$Y_{Tr} = ((Y_{DUT} - Y_{OPEN})^{-1} - (Y_{SHORT} - Y_{OPEN})^{-1})^{-1} \tag{2–3}$$

with Y_{DUT} as the measured Y-parameter matrix of the transistor together with parasitics and Y_{Tr} as the actual transistor Y-parameter matrix. In this paper, this procedure is refered to as the two-step method.

2.1.2 RF Characteristic

In evaluating device RF performance, some indicators are employed such as the cut-off frequency f_T, the maximum oscillation frequency f_{max}, the minimum noise figure NF_{min} (and sometimes 1/f noise). Since f_T and f_{max} are considered as qualitative indicators of the frequency response of a transistor, there are many other elements that can affect the device performance. In this section, f_T and f_{max} are discussed especially.

2.1.2.1 The cut-off frequency : f_T

f_T is defined as the transition frequency which small-signal current gain drops to unity. It is a measure of the maximum useful frequency of a transistor when it is used as an amplifier.

f_T can be easily obtained by converting measured S_{21} parameter to H_{21} parameter.

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{2–4}$$

2.1.2.2 The maximum oscillation frequency : f_{max}

f_T is surely a good indicator of the low-current forward transit time. However, as a performance indicator, it does not include the effects of gate resistance R_g, which are very important in determining the transient response of a transistor. So a indicator including R_g effects have been proposed, f_{max}. f_{max} is the frequency at which the unilateral power gain becoms unity.

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \tag{2–5}$$

2.2 Modeling of DC Model

Since BSIM3v3 (Berkley Short-channel IGFET Model 3 version 3) develped by UCB (University of California, Berkley) had been chosen for a standard compact model in 1995, this model have been widely used for digital and analog circuit design. A philosophy embedded in the BSIM3 model is to find a physically accurate functional form to describes a physical phenomenon and then use fitting parameters and even empirical terms to achieve quantitative match with the device characteristics.

In this chapter, several models for DC parameter extraction such as thresholod voltage model and I-V models etc. in BSIM3v3 are described. In addition to this, extrinsic parameters extraction methodologies for a sub-circuit model are also described. With recent fast growth in the radio-frequency (RF) wireless communications market, the requirements for an accurate RF compact model rapidly increase. As the parasitic influences at high frequency are described in section 1.1.3, extrinsic parameters should be extracted accurately.

2.2.1 Threshold Voltage Model

Accurate modeling of the threshold voltage (V_{th}) is one of the most important requirements for the precise description of a device electrical characteristics. By using the threshold voltage, the device operation can be divided into three operational regions. If the gate voltage is much larger than V_{th}, the MOSFETs is operating in the strong inversion region and the drift current is dominant. If the gate voltage is much less than V_{th}, the MOSFET operates in the weak inversion or subthreshold region and diffusion current is dominant. If the gate voltage is very close to V_{th},

the MOSFET operates in the transition region called moderate inversion where both diffusion and drift currents are important.

The complete V_{th} expression in BSIM3v3 is as following [12]:

$$V_{th} = VTH0 + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs}$$

$$+K1(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1)\sqrt{\phi_s} + (K3 + K3B \cdot V_{bs})\frac{TOX}{W'_{eff} + W0}\phi_s$$

$$-DVT0(\exp(-DVT1\frac{L_{eff}}{2l_t}) + 2\exp(-DVT1\frac{L_{eff}}{l_t}))(V_{bi} - \phi_s)$$

$$-(\exp(-DSUB\frac{L_{eff}}{2l_{t0}}) + 2\exp(-DSUB\frac{L_{eff}}{l_{t0}}))(ETA0 + ETABV_{bs})V_{ds}$$

$$-DVT0W(\exp(-DVT1W\frac{W'_{eff}L_{eff}}{2l_{tw}}) + 2\exp(-DVT1W\frac{W'_{eff}L_{eff}}{l_{tw}}))(V_{bi} - \phi_s) \quad (2–6)$$

In this equation, the second and third terms are used to model the verical non-uniform doping effect, the fourth term is for the lateral non-uniform doping effect, the fifth term is for the narrow width effect, the sixth and seventh terms are related to the short channel effect due to DIBL, and the last term is to descibe the small size effect in devices with both small channel length and small width. A simpler model for V_{th} would be preferred if it could offer the same adequate accuracy.

In this work, since the fifth, sixth and last terms are not considered for DC parameter extraction, only considering terms will be introduced.

2.2.1.1 Modeling of the Vertical Non-uniform Doping Effects

$$V_{th} = V_{th0} + \gamma(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) \quad (2–7)$$

From Eq.(2-7), the threshold voltage depend linearly on $\sqrt{\phi_s - V_{bs}}$, with a slope known as γ. However, experimental data in general displays a non-linear dependence. The slope γ becomes smaller as the body bias V_{bs} becomes more negative for NMOS. This non-linearity comes from the non-uniform substate doping in the vertical direction of the body.

The doping concentration may be higher or lower at the interface of the gate oxide and the body than deep in the body due to the choice of the energies of ion implantation for the channel and well. This non-uniform body doping will make γ in Eq.(2-7) a function of the substate bias. An approximate step-doping profile can be used to obtain an analytical expression of V_{th} as a function of V_{bs}. If the depletion width is less than X_T, N_A in Eq.(2-9) is equal to N_{CH}, otherwise it is equal to N_{SUB}. Therefore, we have

$$V_{th} = VTH0 + \gamma_1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}), \;\; |V_bs| < |V_bx| \tag{2–8}$$

$$V_{th} = VTH0 + \gamma_1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) + \gamma_2(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s - V_{bx}}), \;\; |V_bs| \geq |V_bx| \tag{2–9}$$

ϕ_s^b is the surface potential at threshold, as follows:

$$\phi_s = 2v_t \ln(\frac{N_a}{n_i}) \equiv 2\phi_B \tag{2–10}$$

and γ_1 and γ_2 are given as

$$\gamma_1 = \frac{\sqrt{2q\epsilon_{si}NCH}}{C_{ox}} \tag{2–11}$$

$$\gamma_2 = \frac{\sqrt{2q\epsilon_{si}NSUB}}{C_{ox}} \tag{2–12}$$

V_{bx} is the body bias at which the depletion width is equal to X_T. Therefore, V_{bx} satisfies

$$\frac{qNCHX_T^2}{2\epsilon_{si}} = \phi_s - V_{bx} \tag{2–13}$$

To unify the V_{th} expression in Eqs.(2-8),(2-9), a general expression of V_{th} under differnt body bias is proposed as

$$V_{th} = VTH0 + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_bs \tag{2–14}$$

K1 and K2 are usually determined by fitting Eq.(2-14) to the measured V_{th} data. For theoretical discussions, they can be determined by the criteria that the V_{th} values given bu Eqs.(2-9),(2-14) and their derivatives versus V_{bs} should be the same at V_{bm}, where V_{bm} is the maximum substrate bias voltage. At V_{bs}=V_{bm}, let Eqs.(2-9) and (2-14) be equal:

$$\gamma_1(\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s}) + \gamma_2(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s - V_{bx}}) = K1(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) - K2V_{bm} \tag{2–15}$$

We can get a second equation by letting the derivative of Eqs.(2-9) and (2-14) be equal at V_{bs}=V_{bm} and obtaining

$$K1 = \gamma 2 - 2K2\sqrt{\phi_s - V_{bm}} \tag{2–16}$$

Solving Eqs.(3-10) and (3-11) gives

$$K2 = (\gamma_1 - \gamma_2)\frac{\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s}}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}} \tag{2–17}$$

K1 can be obtained from Eq.(2-16) with K2 given in Eq.(2-17).

It has been found that using K1 and K2 as fitting parameters yields better accuracy than calculating K1 and K2 with Eq.(2-16) and Eq.(2-17).

2.2.1.2 Modeling of the RSCE dut to Lateral Non-uniform Channel Doping

To account for the lateral non-uniform doping effect due to the higher doping concentration near the drain and the source than in the middle of the channel, a step doping profile along the channel length direction may be used as a first order approximation to obtain a V_{th} expression. As a further approximation, the average channel doping can be clculated as follows:

$$N_{eff} = \frac{NCH(L - 2L_x) + N_{pocket} \cdot 2L_x}{L} = NCH(1 + \frac{2L_x}{L}\frac{N_{pocket} - NCH}{NCH})$$
$$\equiv NCH(1 + \frac{NLX}{L}) \tag{2–18}$$

where $NLX = 2L_x\frac{N_{pocket}-NCH}{NCH}$. In BSIM3v3, NLX is treated as a fitting parameter extracted from the measured data.

With the introduction of NLX to accoutn for the lateral non-uniform doping, Eq.(2-14) may be modified into

$$V_{th} = VTH0 + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs} + K1(\sqrt{1 + \frac{NLX}{L}} - 1)\sqrt{\phi_s} \tag{2–19}$$

Eq.(2-19) can be best be understood by first setting V_{bs}=0. At V_{bs}=0, Eq.(2-19) models the dependence of V_{th} on L due to the lateral non-uniform doping. Eq.(2-19) shows that the threshold voltage will increase as channel length decreases. In summary, NLX is the only parameter to represent the lateral non-uniform doping effect. It models the reverse short channel effects (RSCE).

2.2.1.3 Modeling of the Short Channel Effect due to Drain Induced Barrier Lowering

The drain-induced barrier lowering (DIBL) effect is analyzed by solving a quasi two-demension Poisson equation along the channel. By applying Gauss's law to a rectangular box of height X_{dep} and length $\triangle$y in the channel depletion region assuming an equation for the electric potential may be set up and solved, leading to

$$\triangle V_{th} = \theta_{th}(L)[2(V_{bi} - \phi_s) + V_{ds}] \tag{2–20}$$

where V_{bi} is the built-in voltage of the substrate/source junction. V_{bi} is given by

$$V_{bi} = \frac{K_B T}{q} \ln(\frac{NCH \cdot NDS}{n_i^2}) \tag{2–21}$$

where NDS in Eq.(2-21) is the source/drain doping concentration and NCH is the channel doping concentration. In Eq.(3-15),

$$\theta_{th}(L) = [\exp(-L/2l_t) + 2\exp(-L/l_t)] \tag{2–22}$$

l_t is a characteristic length and is given by

$$l_t = \sqrt{\frac{\epsilon_{si} TOX \cdot X_{dep}}{\epsilon_{ox}\eta}} \tag{2–23}$$

X_{dep} is the depletion width in the substrate and is given by

$$X_{dep} = \sqrt{\frac{2\epsilon_{si}(\phi_s - V_{bs})}{qNCH}} \tag{2–24}$$

η in Eq.(2-23) is a fitting parameter that accounts for the numerous approximations behind Eq.(2-23). For example, X_{dep} is not constant from the source to the drain and is not equal to the quantity in Eq.(2-24). Also the electric field is not uniform from the top to the bottom of the depletion region.

As channel length L decreases $\triangle V_{th}$ will increase, and in turn V_{th} will decrease. If a MOSFET has a LDD stracture, NDS in Eq.(2-21) is the doping cocentration in the lightly doped region. V_{bi} in a LDD-MOSFET will be smaller than in a single drain MOSFETs, therefore the threshold voltage reduction due to the short channel effect is smaller in LDD-MOSFETs.

Eq.(2-20) shows that $\triangle V_{th}$ depends linearly on the drain voltage. V_{th} decreases as V_{ds} increases. This is an important aspect of the DIBL phenomenon. The severity of the DIBL effect has a strong dependence on L. If L$\gg l_t$, the DIBL effect is very weak.

The influences of DIBL on V_{th} can be described by Eq.(2-22). However, in order to make the model fit a wide range of L, V_{ds} and V_{bs}, several additional paramters such as DVT0, DVT1, DVT2, DSUB, ETA0 and ETAB are introduced,

$$V_{th} = VTH0 + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs} + K1(\sqrt{1 + \frac{NLX}{Leff}} - 1)\sqrt{\phi_s}$$

$$-DVT0(\exp(-DVT1\frac{L_{eff}}{2l_t}) + 2\exp(-DSUB\frac{L_{eff}}{l_t}))(V_{bi} - \phi_s)$$

$$-(\exp(-DSUB\frac{L_{eff}}{2l_{t0}}) + 2\exp(-DSUB\frac{L_{eff}}{l_{t0}}))(ETA0 + ETAB \cdot V_{bs})V_{ds} \quad (2\text{–}25)$$

where

$$l_t = \sqrt{\epsilon_{si}X_{dep}/C_{ox}}(1 + DVT2 \cdot V_{bs}) \quad (2\text{–}26)$$

$$l_{t0} = \sqrt{\epsilon_{si}X_{dep0}/C_{ox}} \quad (2\text{–}27)$$

$$X_{dep} = \sqrt{\frac{2\epsilon_{si}(\phi_s - V_{bs})}{qNCH}} \quad (2\text{–}28)$$

$$X_{dep0} = \sqrt{\frac{2\epsilon_{si}\phi_s}{qNCH}} \quad (2\text{–}29)$$

DVT1 replaces $1/(\eta)^{1/2}$ in Eq.(2-23). DVT2 is introduced to account for the dependence of the doping concentration on substrate bias since the doping concentration in the body is not uniform in the vertical direction. Compared with Eq.(2-20), (2-25) allows different L dependencies of V_{th} on V_{ds}, and on V_{bs}, i.e. different l_t and l_{t0}, in order to achieve better accuracy of matching the V_{th} data. DVT0, DVT1, DVT2, ETA0, ETAB and DSUB are determined experimentally. Although Eqs.(2-20) and (2-25) have many differences, they have the same basic double exponential functional forms.

2.2.2 Essential Equation for I-V Characteristics

A DC MOSFET model is derived based on

$$J_n = q\mu_n nE + qD_n\nabla n \quad (2\text{–}30)$$

$$J_p = q\mu_p pE + qD_p\nabla n \quad (2\text{–}31)$$

J_n and J_p are the current dinsities for electrons and holes respectively, q is the electron charge, μ_n, μ_p are the mobilities of electrons and holes respectively, n and p are the electorn and hole

concentrations, E is the electric field and D_n and D_p are the diffusion coefficients of electrons and holes, respectively. D_n and D_p are linked to μ_n and μ_p with the following Einstein's relationship:

$$D_n = v_t \mu_n \tag{2–32}$$

$$D_p = v_t \mu_p \tag{2–33}$$

where v_t is the thermal voltage.

The terms of E in Eqs.(2-30),(2-31) represent the drift current components due to the electric field E. The second terms of Eqs.(2-30),(2-31) describe the diffusion current components due to the carrier cancentration gradient. In the strong inversion region, the current is dominated by the drift current. In the subthreshold region, the diffusion current component dominates. However, in the transition region (moderate inversion region) from subt-hreshold to s-trong inversion, both drift and diffusiion currents are important.

As shown in Eqs.(2-30),(2-31), carrier density and the velocity-field relationship are two fundamental factors determining the I-V characteristics. We need to model the channel charge and mobility as well as the velocity-field relationship carefully to describe the current characteristics accurately and physically. We discuss the modeling of channel charge and mobility next before we introduce the modeling the I-V behavior.

2.2.3 Channel Charge Density Model

For the weak inversion and the strong inversion regions, separate expressions for channel charge density have been given respectively:

$$Q_{inv} \approx \sqrt{\frac{q\epsilon_{si}N_a}{4\phi_B}} v_t \exp(\frac{V_{gs} - V_{th} - V_{OFF}}{nv_t}) \ in \ weak \ inversion \tag{2–34}$$

$$Q_{inv} = C_{ox}(V_{gs} - V_{th}) \quad in \ strong \ inversion \tag{2–35}$$

We can combine these expressions in the following form:

$$Q_{chs0} = C_{ox} V_{gsteff} \tag{2–36}$$

$$V_{gsteff} = \frac{2nv_t \ln[1 + \exp(\frac{V_{gs} - V_{th}}{2nv_t})]}{1 + 2nC_{ox}\sqrt{\frac{2\phi_s}{q\epsilon_{si}N_{CH}}} \exp(-\frac{V_{gs} - V_{th} - 2V_{OFF}}{2nv_t})} \tag{2–37}$$

As shown in Figure 6. and 7., V_{gsteff} becomes V_{gs}-V_{th} in the strong inversion region, and follows $\sqrt{\frac{q\epsilon_{si}N_{CH}}{4\phi_B}} \frac{v_t}{C_{ox}} \exp(\frac{V_{gs} - V_{th} - V_{OFF}}{nv_t})$ in the subthreshold region.

The form of Eq.(2-37) was chosen to obtain a continuous equation for the channel charge and to match the measured Q_{chs}-V_{gs} characteristics in the moderate inversion (transition) region. The channel charge expression, Q_{chs0}, will be used in subsequent sections of this chapter to model the drain current.

Furthermore, the model accurately predicts the charge in the transition (moderate inversion) region. The continuous and accurate nature of the model makes it very attractive and promising in circuit simulation since the moderate inversion resion is becoming more important for low voltage/power circuit application.

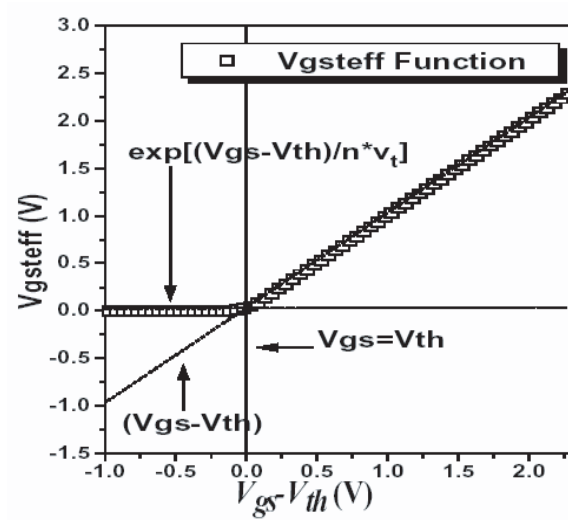


Figure 6: V_{gsteff} vs. V_{gs}-V_{th} in a linear plot [25].

2.2.4 Mobility Model

A good model for the carrier surface mobility is critical to the accuracy of a MOSFET model. The scattering mechanisims responsible for the surface mobility include phonons, coulombic scattering, and surface roughness scattering. For good quality interfaces, phonon scattering is the dominant scattering mechanism at room temperature. In general, mobility depends on many process parameters and bias conditions. For example, mobility depends on the gate oxide thickness, doping concentration, threshold voltage, gate voltage and substate voltage, etc.

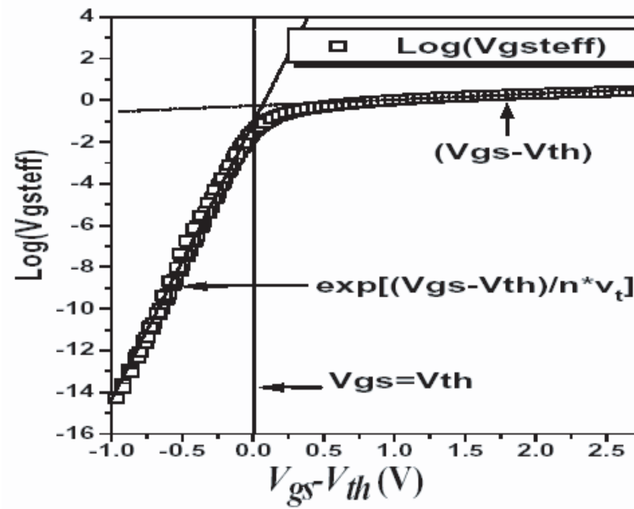


Figure 7: V_{gsteff} vs. V_{gs}-V_{th} in a semi-logarithmic plot [25].

The continuity of mobility model is also required to ensure the continuity of the I-V model. To achieve continuity in the mobility model, BSIM3v3 uses a unified mobility expression based on the V_{gsteff} expression of Eq.(2-37),

$$\mu_{eff} = \frac{\mu_0}{1 + (U_A + U_C V_{bseff})(\frac{V_{gsteff}+2V_{th}}{T_{OX}}) + U_B(\frac{V_{gsteff}+2V_{th}}{T_{ox}})^2} \tag{2–38}$$

where

$$V_{bseff} = V_{bc} + 0.5\left[V_{bs} - V_{bc} - \delta_1 + \sqrt{(V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 V_{bc}}\right] \tag{2–39}$$

It can be seen that Eq.(2-38) follows Eq.(2-37) in strong inversion, and becomes a constant in the subthreshold region.

Several mobility model options are provided for users to choose in BSIM3v3. a selector parameter called *mobMod* is introduced for this purpose. The mobility expression in Eq.(2-38) has been designated as *mobMod*=1.

The following empirical mobility model option (*mobMod*=2) is better suited for depletion mode devices:

$$\mu_{eff} = \frac{\mu_0}{1 + (U_A + U_C V_{bseff})(\frac{V_{gsteff}}{T_{OX}}) + U_B(\frac{V_{gsteff}}{T_{ox}})^2} \tag{2–40}$$

BSIM3v3 also introduced a third mobility model option (*mobMod*=3):

$$\mu_{eff} = \frac{\mu_0}{1 + [U_A(\frac{V_{gsteff+2V_{th}}}{T_{ox}}) + U_B(\frac{V_{gsteff}}{T_{ox}})^2](1 + U_C V_{bseff})} \qquad (2\text{–}41)$$

It is clear that all of the mobility models given above approach constant values that are independent of V_g when V_{gs}¡V_{th}.

It should be pointed out that all of the mobility models given above account for only the influence of the vertical electrical field. The influence of the lateral electrical field on the mobility will be considered when discussing the velocity saturation effect in the next section.

2.2.5 I-V Model in the Strong Inversion Region

2.2.5.1 I-V Model in the linear (triode) Region

1. Intrinsic case (Rds=0)

In the strong inversion region, the current equation at any point y along the channel is

$$I_{ds} = W_{eff} C_{ox}(V_{gst} - A_{bulk} V_{(y)}) v(y) \qquad (2\text{–}42)$$

where V_{gst}=(V_{gs}-V_{th}), W_{eff} is effective device channel width. C_{ox} is the gate capacitance per unit area. V(y) is the potential difference between the channel and the source. A_{bulk} is the codfficient accounting for the bulk charge effect and v(y) is the velocity of carriers.

BSIM3 I-V formulaition starts with a simple piece-wise saturation velocity model,

$$v(y) = \mu E_y \qquad E_y < E_{sat} \qquad (2\text{–}43)$$

$$v(y) = v_{sat} \qquad E_y > E_{sat} \qquad (2\text{–}44)$$

where E_y is the magnitude of the lateral electric field and E_{sat} is the critical electric field at which the carrier velocity becomes satureted. μ is the mobility including the influence of the lateral electric field E_y and is given by

$$\mu = \frac{\mu_{eff}}{1 + (E_y/E_{sat})} \qquad (2\text{–}45)$$

In order to have a continuous velocity model at E_y=E_{sat}, E_{sat} satisfies

$$E_{sat} = \frac{2v_{sat}}{\mu_{eff}} \qquad (2\text{–}46)$$

Thus, before the electric field reaches E_{sat} the drain current can be expressed

$$I_{ds} = W_{eff} C_{ox}(V_{gs} - V_{th} - A_{bulk} V_{(y)}) \frac{\mu_{eff} E_y}{1 + E_y/E_{sat}} \qquad (2\text{–}47)$$

Eq.(2-47) can be rewritten as

$$E_y = \frac{I_{ds}}{\mu_{eff} W_{eff} C_{ox}(V_{gst} - A_{bulk} V_{(y)}) - I_{ds}/E_{sat}} = \frac{dV_{(y)}}{dy} \tag{2–48}$$

By integratin Eq.(2-48) from y=0 to y=L_{eff}, the effective channel length, and V(y)=0 to V(y)=V_{ds}, we arrive at

$$I_{ds} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \frac{1}{1 + V_{ds}/E_{sat} L_{eff}} (V_{gs} - V_{th} - A_{bulk} V_{ds}/2) V_{ds} \tag{2–49}$$

The drain current model in Eq.(2-49) is valid before the carrier velocity saturates, that is, in the linear of the triode region.

2. Extrinsic case (Rds>0)

The parasitic source/drain resistance is an important device parameter which can affect MOSFET performance significantly in short channel devices. The most straightforward and accurate way of modeling the parasitic resistance effect is to use a circuit with resistors in series with the intrinsic MOSFET. This leads to a complicated drain current expression. In order to make the model efficient, the drain cuurent in the linear region can be modeled by extending Eq.(2-49).

$$I_{ds} = \frac{I_{ds0}}{1 + R_{ds} I_{ds0}/V_{ds}} \tag{2–50}$$

where I_{ds0} is the inctrinsic current expression given by Eq.(2-49). R_{ds} is a variable to account for the influence of the parasitic resistances at the source and drain.

2.2.5.2 Drain Voltage at Current Saturation, V_{sat}

1. Intrinsic case (Rds=0)

If the drain voltage (and hence the lateral electric field) is sufficiently high, the carrier velocity near the drain saturates. The channel may be divided into two portions: one adjacent to the source where the carrier velocity is field-dependent and the others adjacent to the drain where the velocity has satureted. At the boudary between the two portions, the channel voltage is the saturation voltage (V_{dsat}) and the lateral delctric field is equal to E_{sat}. We can substitute v=v_{sat} and V_{ds}=V_{dsat} into Eq.(2-42) to obtain the saturation current:

$$I_{dsat} = W_{eff} C_{ox} (V_{gst} - A_{bulk} V_{dsat}) v_{sat} \tag{2–51}$$

By equating Eq.(2-42) and (2-51) at V_{ds}=V_{dsat}, we can solve for the saturation voltage V_{dsat}:

$$V_{dsat} = \frac{E_{sat}L_{eff}(V_{gs} - V_{th})}{A_{bulk}E_{sat}L_{eff} + (V_{gs} - V_{th})} \tag{2–52}$$

2. Extrinsic case (Rds>0)

Due to the parasitic resistance, the saturation voltage V_{dsat} will be larger than what is predicted by Eq.(2-52). Equating Eq.(2-50) with Eq.(2-51), V_{dsat} with parasitic resistance R_{ds} will be

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \tag{2–53}$$

$$a = A_{bulk}^2 R_{ds}C_{ox}W_{eff}v_{sat} + (\frac{1}{\lambda} - 1)A_{bulk} \tag{2–54}$$

$$b = -[V_{gst}(\frac{2}{\lambda} - 1) + A_{bulk}E_{sat}L_{eff} + 3A_{bulk}R_{ds}C_{ox}W_{eff}v_{sat}V_{gst}] \tag{2–55}$$

$$c = E_{sat}L_{eff}V_{gst} + 2R_{ds}C_{ox}W_{eff}v_{sat}V_{gst}^2 \tag{2–56}$$

$\lambda = A_1V_{gst} + A_2$ is introduced to account for he non-saturating effect of the device I-V which will be discussed in section 2.2.6.

2.2.6 Subthreshold I-V Model

In the subthreshold region, the potential in the channel exhibits a peak between the source and the drain. At or near the peak of the potential, the lateral electric field can be considered zero because the potential gradient is zero. Thus, the drift current can be ignored in the subthreshold region. According to the current density equation given in Eqs.(2-30) and (2-31), we have:

$$J_n = qD_n\nabla_n \tag{2–57}$$

We would like to use the charge sheet dinsity expression Q_{inv} in modeling the I-V characteristics. If we integrate Eq.(2-57) from the Si-SiO_2 interface to the edge of the depletion layer (X_{dep}) in the bulk, the current in the subthreshold region can be given as

$$I_{ds} = W_{eff}\mu_n v_t \frac{dQ_{inv}}{dy} \tag{2–58}$$

The current expression can be obtained by integrating Eq.(2-58) along the channel from source to drain,

$$I_{ds} = \frac{W_{eff}}{L_{eff}}\mu_n v_t(Q_{dinv} - Q_{sinv}) \tag{2–59}$$

where Q_{dinv} and Q_{sinv} are the channel inversion charge at the drain and source.

The channel charges at the source and drain can be written as,

$$W_{sinv} = \sqrt{\frac{q\epsilon_s i N_{CH}}{4\phi_B}} v_t \exp(\frac{V_{gs} - V_{th} - VOFF}{nv_t}) \tag{2–60}$$

$$W_{dinv} = \sqrt{\frac{q\epsilon_s i N_{CH}}{4\phi_B}} v_t \exp(\frac{V_{gs} - V_{th} - VOFF - V_{ds}}{nv_t}) \tag{2–61}$$

Therefore, the current expression becomes

$$I_{ds} = I_{s0}(1 - \exp(-\frac{V_{ds}}{nv_t})) \exp(\frac{V_{gs} - V_{th} - VOFF}{nv_t}) \tag{2–62}$$

$$I_{s0} = \mu_n \frac{W_{eff}}{L_{eff}} \sqrt{\frac{q\epsilon_s i N_{CH}}{4\phi_B}} v_t^2 \tag{2–63}$$

v_t is the thermal voltage (K_BT/q) and VOFF is the offset.

2.2.7 General issue of I-V Model and I-V Model of BSIM3v3

Each model expressions for linear, saturation, subthreshold and storng inversion region is discussed in the previous sections. Although these expressions can describe the device behavior accurately in each operation region, problems are likely to occur in a transition region between two well-described regions. In order to address this persistent problem, a unified model should be synthesize to preserve region-specific accuracy and to ensure the continuities of current (I_{ds}) and conductance (G_x) and their derivatives in all transition regions. This was accomplishied in BISM3v3.

This section will describe the unified BSIM3v3 I-V modl equations. Based on the continuous channel charge and mobility models, a single equation I-V expression is obtained:

$$I_{ds} = \frac{I_{ds0}}{1 + \frac{R_{ds} I_{ds0}}{V_{dseff}}}(1 + \frac{V_{ds} - V_{dseff}}{V_A})(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}) \tag{2–64}$$

where

$$I_{ds0} = \frac{W_{eff} C_{ox} \mu_{eff} V_{gsteff} V_{dseff}(1 - \frac{V_{dseff}}{2V_b})}{L_{eff}(1 + \frac{V_{dseff}}{E_{sat} L_{eff}})} \tag{2–65}$$

$$V_A = V_{Asat} + (1 + \frac{P_{VAG} V_{gsteff}}{E_{sat} L_{eff}})(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}})^{(-1)} \tag{2–66}$$

$$V_{Asat} = \frac{E_{sat} L_{eff} + V_{dsat} + 2R_{ds} v_{sat} C_{ox} W_{eff} V_{gsteff}[1 - \frac{A_{bulk} V_{dsat}}{2(V_{gsteff} + 2v_t)}]}{2/\lambda - 1 + R_{ds} v_{sat} C_{ox} W_{eff} A_{bulk}} \tag{2–67}$$

$$V_{ACLM} = \frac{A_{bulk}E_{sat}L_{eff} + V_{gsteff}}{PCLM \cdot A_{bulk}E_{sat}l}(V_{ds} - V_{dseff}) \tag{2–68}$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout}(1 + PDIBLCB \cdot V_{bseff})}(1 - \frac{A_{bulk}V_{dsat}}{A_{bulk}V_{dsat} + V_{gsteff} + 2v_t}) \tag{2–69}$$

$$\theta_{rout} = PDIBLC1[\exp(-D_{ROUT}\frac{L_{eff}}{2l_{t0}}) + 2\exp(-D_{ROUT}\frac{L_{eff}}{l_{t0}})] + PDIBLC2 \tag{2–70}$$

$$\frac{1}{V_{ASCBE}} = \frac{PSCBE2}{L_{eff}}\exp(\frac{-PSCBE1 \cdot l}{V_{ds} - V_{dseff}}) \tag{2–71}$$

when R_{ds}=0,

$$V_{dsat} = \frac{E_{sat}L_{eff}(V_{gsteff} + 2v_t)}{A_{bulk}E_{sat}L_{eff} + V_{gsteff} + 2v_t} \tag{2–72}$$

For $R_{ds}>0$,

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \tag{2–73}$$

$$a = A_{bulk}^2 W_{eff}v_{sat}C_{ox}R_{ds} + (\frac{1}{\lambda} - 1)A_{bulk} \tag{2–74}$$

$$b = -\left\{(V_{gsteff} + 2v_t)(\frac{2}{\lambda} - 1) + A_{bulk}E_{sat}L_{eff} + 3A_{bulk}(V_{gsteff} + 2v_t)^2 W_{eff}v_{sat}C_{ox}R_{ds}\right\} \tag{2–75}$$

$$c = (V_{gsteff} + 2v_t)E_{sat}L_{eff} + 2(V_{gsteff} + 2v_t)^2 W_{eff}v_{sat}C_{ox}R_{ds}) \tag{2–76}$$

$$\lambda = A_1 V_{gsteff} + A_2 \tag{2–77}$$

The parameter E_{sat} and v_t can be introdeuced as below:

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \tag{2–78}$$

$$a = A_{bulk}^2 R_{ds}C_{ox}W_{eff}v_{sat} + (\frac{1}{\lambda} - 1)A_{bulk} \tag{2–79}$$

$$b = -\left[V_{gst}(\frac{2}{\lambda} - 1) + A_{bulk}E_{sat}L_{eff} + 3A_{bulk}R_{ds}C_{ox}W_{eff}v_{sat}V_{gst}\right] \tag{2–80}$$

$$c = E_{sat}L_{eff}V_{gst} + 2R_{ds}C_{ox}W_{eff}v_{sat}V_{gst}^2 \tag{2–81}$$

V_{dseff} is

$$V_{dseff} = V_{dsat} - \frac{1}{2}(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{sat} - V_{ds} - \delta)^2} + 4\delta V_{dsat}) \tag{2–82}$$

where δ is a user specified parameter with a default value of 0.01. The V_{dseff} function is introduced to guarantee continuities of I_d and its derivatives at V_{sat}.

2.2.8 Other Important Parameters

1. The V_{OFF} Parameter

The theoretical threshold voltage $V_{th,sub}$ needed to fit the subthreshold current is different form V_{th} that is used to fit strong inversion I-V. One explanation is that the surface potential corresponding to the V_{th} in strong inversion is actually higher than $2\phi_B$. The difference between the threshold voltages discussed above is several v_t. To account for this fact, a parameter called VOFF is introduced so that

$$V_{th,sub} = V_{th} + VOFF \tag{2–83}$$

V_{OFF} is determined experimentally from the measured I-V characteristics and is expected to be negative. Due to the physical meaning of VOFF, overly large absolute values of VOFF are not recommended in the model. The recommended range for VOFF is between -0.06 and -0.12V.

2. Drain and Source Parasitic Resistance, R_{ds}

In BSIM3v3, the parasitic resistance of drain and source is modeld with th e following expression:

$$R_{ds} = \frac{RDSW\left[1 + PRWG \cdot V_{gsteff} + PRWB(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})\right]}{(10^6 W_{eff})^{WR}} \tag{2–84}$$

where WR is a fitting paramter and RDSW has the units of Ω-μm^{WR}. PRWB is the body effect coefficient, and PRWG is the gate-bias effect coefficient.

4. The n Parameter for Subthreshold Swing

The n parameter can be called the subthreshold swing factor or the subthreshold slope factor because the traditional gate voltage swing of subthreshold slope can be defined as

$$S = \frac{dV_{ds}}{d\log I_{ds}} \approx 2.3nv_t \tag{2–85}$$

The subthreshold swing is the change in the gate voltage V_{gs} required to reduce the subthreshold current I_{gs} by one decade. Accordeing to Eq.(2-85), the n paramter is the key paramter in determining the subthreshold swing of the device. For long channel devices, n can be modeled as

$$n = 1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{it}}{C_{ox}} \tag{2–86}$$

where C_{dep} and C_{it} are the deplition layer capacitance and interface charge capacitance. However, Eq.(2-86) does not consider the influence of short cahnnel effects. In short channel devices, the potential at the surface of the channel will be determinde by both the gate bias and the drain bias through the coupling of C_{ox} and C_{dsc}, respectively, instead of the gate bias only. The coupling capacitance $C_{dsc}(L)$ is an exponential function of the channel length. To reflect this phenomenon in BSIM3v3, the n paramater for the subthreshold swing is described in the following form:

$$n = 1 + NFACTOR\frac{C_{dep}}{C_{ox}} + \frac{C_{IT}}{C_{ox}} + \frac{(CDSC + CDSCD \cdot V_{ds} + CDSCB \cdot V_{bseff})(\exp(-DVT1\frac{L_{eff}}{2l_t}) + 2\exp(-DVT1\frac{L_{eff}}{l_t}))}{C_{ox}} \tag{2–87}$$

5. The A_{bulk} Parameter for the Bulk Charge Effect

When the drain voltage is large and when the channel length is long, thie depletion region thickness of the channel is not uniform along the channel length. This will cause the threshold voltage to vary along the channel. This effect is called the bulk charge effect.

In BSIM3v3, the parameter A_{bulk} is used to account for the bulk charge effect, including both the short channel effects and narrow width effects, as shown in Eq.(2-88). Swveral extracted paramters such as A0, AGS, B0 and B1 are introduced in BSIM3v3 to account for the channel length and width dependencies of the bulk charge parameter. In addition, the parameter KETA is introduced to model the change in the bulk charge effect at high body bias conditions.

$$A_{bulk} = (1 + \frac{K_{1ox}}{2\sqrt{\phi_s - V_{bseff}}}\left\{\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}\left[1 - AGS \cdot V_{gsteff}(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}})^2 + \frac{B0}{W'_{eff} + B1}\right]\right\}) \frac{1}{1 + KETA \cdot V_{bseff}} \tag{2–88}$$

In Eq.(2-88), A0, AGS, B0,B1 and KETA are extended from experimental I-V data. K_{1ox} is given in

$$K1OX = K1\frac{TOX}{TOXM} \tag{2–89}$$

It is known that A_{bulk} is close to 1 if the channel length is small, and rises as channel length increases.

2.2.9 Source / Drain Series Resistance

The extrinsic parasitic resistances are important parameters which influence MOSFET performance largely. In deep sub-micron device, it becomes much more important because the parasitic resistances are independence even if scaled down.

Ideally, in the discussion of MOSFET current, we consider the source and drain regions as conductor. However, in reality, as the current flows from the channel to the terminal contact, there is a small voltage drop in the source and drain regions due to the finite silicon resistivity and metal contact resistance. In a long-channel device, the source and drain parasitic resistances are negligible compared with the channel resistance. In a short-channel device, however, the source and drain series resistances can be an appreciable fraction of the channel resistance and can therefore cause significant current degradation.

To model these parasitic resistances accurately, there are two approaches to model the parasitic source and drain resistances in BSIM3: (a) *lumped-resistance approach* and (b) *absorbed-resistance approach*. It shows in Figure .

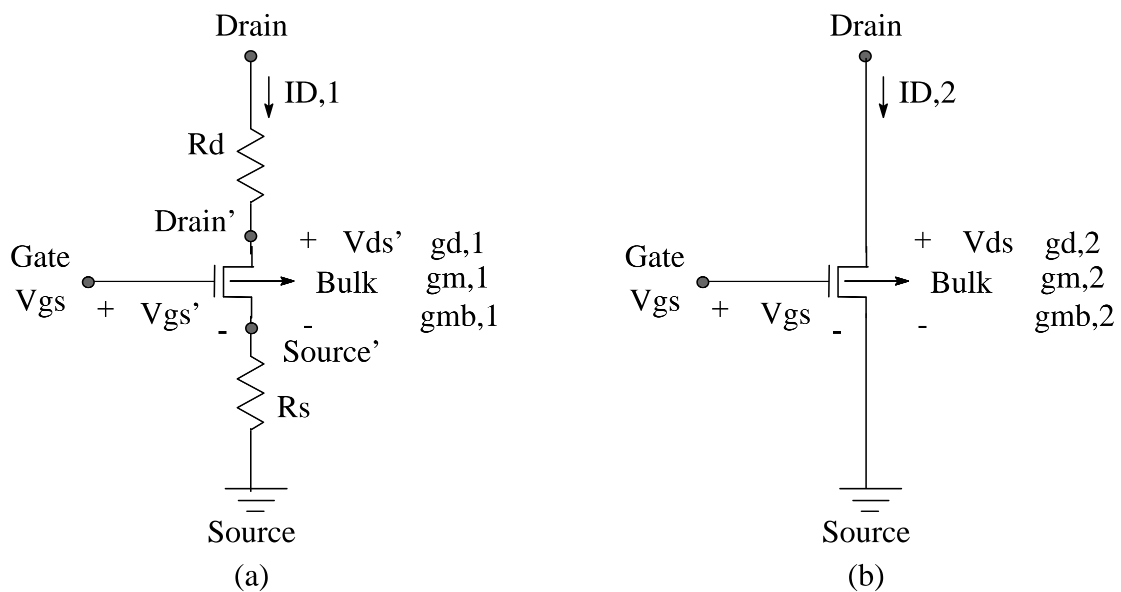


Figure 8: The parasitic source and drain resistances: (a) *lumped-resistance approach* and (b) *absorbed-resistance approach*.

The *lumped-resistance approach*, while being conceptually simple and, in fact, more accurate

than the to-be-discussed second approach, has some drawbacks. First, there are two more nodal voltages which need to be solved for each transistor; namely, the Source' and the Drain' nodes. This translates to lengthened computation time in a SPICE simulation. For simple circuit with few transistors, however, we believe this extra amount of time needed for numerical solution is trivial. Second, generally SPICE parameters are extracted by matching the measured and simulated values of the drain current and the mutual transconductance. In a measurement setting, the measured current is that at the Drain node, and the measured g_m, for example, is equal to $\partial I_d/\partial V_{gs}$(still referring to Figure 8.(a)). The calculated drain current, which is the current at the Drain' node, will be the same current that flows through the Drain node. Therefore, extracting parameters by fitting the simulated current at the Drain' node against the measured current at the Drain node makes sense. However, the calculated g_m from BSIM3 is really $\partial I'_d/\partial V'_{gs}$, which often differs significantly from measured gm equaling to $\partial I_d/\partial V_{gs}$. Hence, unless a numerically intensive SPICE subroutines are incorporated to calculate the derivatives at the Drain' and Source' nodes, SPICE parameters should not extracted by fitting the measured and simulated g'_ms.

Some formulas are proposed to correct this problem. With a certain small-signal approximation, it is possible to relate the measured conductances to intrinsic conductances:

$$g_d \approx \frac{g_{d,i}}{1 + g_{m,i}R_S + g_{d,i}(R_S + R_D) + g_{mb,i}R_S} \tag{2–90}$$

$$g_m \approx \frac{g_{m,i}}{1 + g_{m,i}R_S + g_{d,i}(R_S + R_D) + g_{mb,i}R_S} \tag{2–91}$$

$$g_{mb} \approx \frac{g_{mb,i}}{1 + g_{m,i}R_S + g_{d,i}(R_S + R_D) + g_{mb,i}R_S} \tag{2–92}$$

where, for example, g_d is $\partial I_d/\partial V_{ds}$, the measured drain conductance, and $g_{d,i}$ is the intrinsic device conductance calculated in BSIM3, equal to $\partial I_d/\partial V'_{ds}$. After the application of Eq.(2-91), it is possible to extract parameters by fitting BSIM3 generated $g_{d,i}$ to the measured g_d. We caution that, although the approximation of g_d given in Eq.(2-91) is fairly good, using Eq.(2-90) to relate gm and $g_{m,i}$ can run into problems unless the current is fairly low. The equations expressed in Eqs.(2-90)-(2-92), after all, are derived with the small-signal assumption, which can sometimes fail at normal operating current levels.

BSIM3 offers another approach to model the parasitic source/drain resistances, basically by absorbing the parasitic resistances' effects on current and conductances into the intrinsic device. The equivalent circuit is shown in the right-hand side of Figure 8. In this absorbed-resistance

approach, the nodes Drain' and Source' disappear. The drain current and mutual transconductance are calculated from a totally different set of equation:

$$ID,2 = f2(VGS, VDS, RD + RS)$$

$$gd,2 = \frac{\partial ID,2}{\partial VDS} \tag{2–93}$$

$$gm,2 = \frac{\partial ID,2}{\partial VGS}$$

$$gmb,2 = \frac{\partial ID,2}{\partial VBS}$$

We use f_2 to describe the function form of $I_{D,2}$, in order to stress that the function differs from f_1 used in the calculation of $I_{D,1}$. Basically, BSIM3 devises some sort of function f_2, which is a modified version of f_1 to account for the effects of the parasitic resistances. The amount of deviation from the original f_1 depends on the magnitude of R_D+R_S. The larger the value of RD+RS, the more significant the deviation. The modification is made in ways such that somehow $I_{D,2}$ is approximately equal to $I_{D,1}$ and more importantly, $g_{d,2}$, $g_{m,2}$ and $g_{mb,2}$ are approximately equal to $g_{d,1}$, $g_{m,1}$ and $g_{mb,1}$, respectively. Note the keyword above is approximately. No matter how clever the BSIM3 modification may be, there is no way to replace the SPICE simulator's mathematical calculations of the two additional nodal voltages if the extract solution is desired. The approximation is most accurate when the drain current is small such that the voltage drop across R_S is small compared to the applied V_{GS}. However, despite some claims to the contrary, it is believed that the error can be quite high (exceeding 10 % at least) when the current flow is large. Setting the issues of dc accuracy aside, the absorbed-resistance approach is also discouraged for RF applications. When the second approach is used, the input resistance of the MOSFET will be purely imaginary, without seeing the effect of R_S. This is because BSIM3 makes an attempt to equilibrate only the drain current and the conductances at the two sides of Figure 8. The fact that the device y-parameters of the overall device are greatly altered when two extra nodes are added is not considered.

Here are some details of the actual BSIM3 implementation. When the lumped-resistance approach is used, R_S and R_D are specified with the SPICE parameter *RSH* (sheet resistance of the source and drain contact), together with the fields *NRD* (number of squares in the drain

contact) and *NRS* (number of squares in the source contact) found in the device statement. They are given by

$$R_S = RSH \times NRS; \quad R_D = RSH \times NRD \tag{2–94}$$

RDSW, to be discussed shortly, should be zero in this *lumped-resistance approach*.

In the *absorbed-resistance approach*, we see that the function f_2 in Eq.(2-93) depends on the sum of R_S and R_D, rather than each component individually. From this observation alone, we can infer that BSIM3 uses a completely new parameter for this approach, independent from the aforementioned *RSH*, *NRS* and *NRD*. It is *RDSW*, the sum of source and drain resistances per unit width. When this approach is used, *RSH* should be set to zero, and *RDSW* can be approximated from the measured R_S and R_D:

$$R_S + R_D \approx \frac{RDSW}{W} \tag{2–95}$$

where W is the device's width. (The actual relationship between the parasitic resistances and *RDSW* includes other parameters such as *WR*, *PRWG* and *PRWB* to account for secondary effects. Eq.(2-95) is valid when *WF*, *PRWG*, and *PRWB* assume their default values of 1, 0, and 0, respectively.) For a RF circuit designer who would like to see nonzero real part input resitance due to the source resistance, the lumped-resistance approach is preferred and *RDSW* should be zero.

2.3 Modeling of the extrinsic MOSFET

Although many MOSFET models, including MOS9, EKV and BSIM3v3, have been developed for digital, analog and mixed-signal applications, the RF MOSFET modeling accuracy of the existing MOSFET compact model is not satisfactory. It is because, at high frequency region, the parasitic components severely influence to device RF performance and it is difficult to predict these parasitics behavior only within a compact model. To make models more accurate at RF, sub-circuits are usually added to intrinsic transistor model, BSIM3v3 in this paper, as shown in Figure 9. (The small-signal equivalent circuit of Figure 9. is also shown in Figure 17.) Simple sub-circuits are preferred to reduce the simulation time and to make parameter extraction easier. For an AC small signal model at RF, the modeling of sub-circuits components, i.e. the parasitic components, is very important. The models for these parasitic components should be physics-

based and linked to process and geometry information to ensure the scalability and prediction capabilities of the model.

In this section, the methodologies of the extrinsic parameter extraction, which surround the intrinsic MOSFET in Figure 9. will be described.

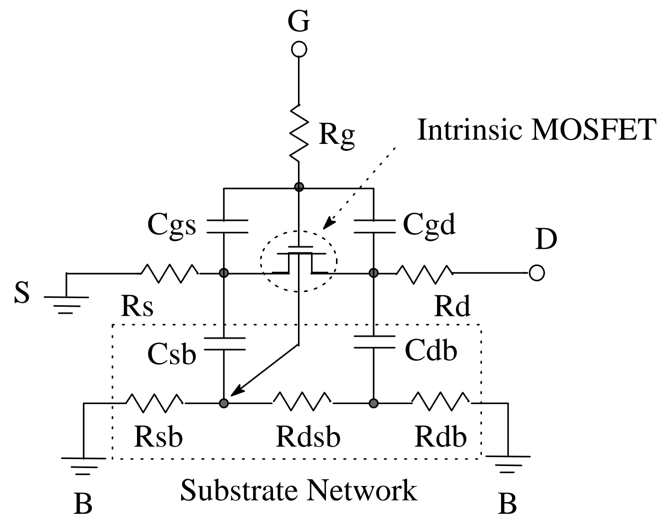


Figure 9: Sub-circuit model with intrinsic and extrinsic components [10][28].

2.3.1 Gate Resistance Model

The typical sheet resistance for a poly-silicon gate ranges between 20-40 Ω/square and can be reduced by a factor of 10 with a silicide process, and even more with a metal stack process. At DC and low frequency, the gate resistance consists mainly of the poly-silicon sheet resistance and is independent of bias. However, at high frequency, it becomes a bias-dependent component and two additional physical effects will affect the effective gate resistance [13][28]: the distributed gate electrode resistance (R_{eltd} or R_{poly}) and non-quasi-static (NQS) effects (R_{ch}), as shown in Figure 10. [14],

$$R_g = R_{eltd} + R_{ch} \tag{2–96}$$

At first, the distributed gate electrode resistance (R_{eltd}) will be described. It will become more severe as the gate width becomes wider at higher operation frequency. So multi-finger devices are used in the circuit design with narrow gate width for each finger to reduce the influence of

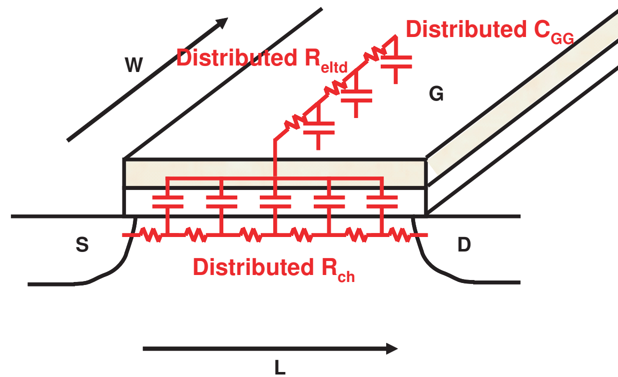


Figure 10: Distributed gate electrode resistance R_{eltd}, channel resistance R_{ch} and gate capacitance C_{gg}.

this effect. With multi-finger devices, gate resistance can separate, as shown in Figure 11 [13]. As R_{eltd} is insensitive to bias and freqency, its value can be obtained from the gate electrode sheet resistance ($R_{eltd\text{-}sh}$),

$$R_{eltd} = \alpha \frac{W_{total}}{LN_f^2} R_{eltd-sh}$$

$$= \alpha \frac{W_{unit}}{LN_f} R_{eltd-sh} \tag{2–97}$$

where α is 1/3 when the gate terminal is brought out from one side, or 1/12 when connected on both sides [30]. The value of α accounts for the distributed nature of the RC line across the channel.

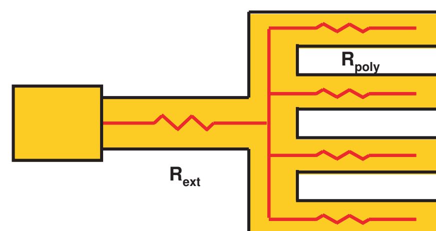


Figure 11: Divided R_{eltd} into R_{ext} and R_{poly} with multi-finger devices.

Next, NQS effects (R_{ch}) in the channel will be described. For the devices with NQS effects, additional bias and geometry dependences of the gate resistance are needed to account for the NQS effects. There are two mechanisms involved in R_{ch}: one is the static channel resistance

(R_{st}), which accounts for the dc channel resistance and the other is the excess diffusion channel resistance (R_{ed}) due to the change of channel charge distribution by ac excitation of the gate voltage. R_{st} and R_{ed} together determine the time constant of the NQS effects. R_{st} is modeled by integrating the resistance along the channel under quasi-static assumption,

$$R_{st} = \int dR = \int \frac{dV}{I_d}$$

$$= \frac{V_{ds}}{I_d} \,@\, triode\ region; \tag{2–98}$$

$$= \frac{V_{dsat}}{I_d} \,@\, saturation\ region, \tag{2–99}$$

where V_{dsat} is the saturation drain voltage. Both I_d and V_{dsat} are available in BSIM3v3. R_{ed} can be derived from the diffusion current as

$$R_{ed} = \frac{qL}{\eta W \mu C_{ox} kT} \tag{2–100}$$

where η is a technology-dependent constant. The overall channel resistance seen from the gate is

$$\frac{1}{R_{gch}} = \gamma\left(\frac{1}{R_{st}} + \frac{1}{R_{ed}}\right) \tag{2–101}$$

where γ is a paremeter accounting for the distributed nature of the channel resistance and C_{ox} is oxide capacitance per unit area. γ equals to 12 if the resistance is uniformly distributed along the channel. Since this assumption is not valid in the saturation region, γ is left as a fitting parameter.

2.3.2 Substrate Resistance Model

The influence of the substrate resistance R_{sub} is ususally ignored in compact models for digital and analog circuit simulation at DC and low frequency. However, the high-frequency impact of the substrate resistance is well-known [15]-[17]. The substrate resistance influences mainly the output characteristics, whereas gate resistance influences the input characteristics, and can contribute as much as 20 % or more of the total output admittance [18],[19]. It is difficult to predict the substrate resistance scales nonlinearly with channel length, finger width, number of fingers and the actual placement of substrate taps in relation to the device. So far, some substrate resistance models have been developed and reported [20][21]. In this section, substrate network model is described simply.

The different equivalent circuits for the part of substrate network in Figure 9. are shown in Figure 12.-16. The four and five resistor networks are more accurate and can be vaild up to higher frequency, but the analysis and parameter extraction of the components are very complex. The one and two resistor networks introduce fewer components and are easier for the analysis and parameter extraction. However, they may be less accurate when the operating frequency goes to higher. The three resistor network is a compromise among these substrate networks. It can ensure the accuracy up to 10 GHz while maintaining a simple analysis and parameter extraction. However, it should be pointed out that the intrinsic bulk has been shifted to the end of R_{dsb}, as shown in Figure 14., instead of located somewhere along the resistor R_{dsb}. It has been concluded that this approximation does not influence much the simulation accuracy.

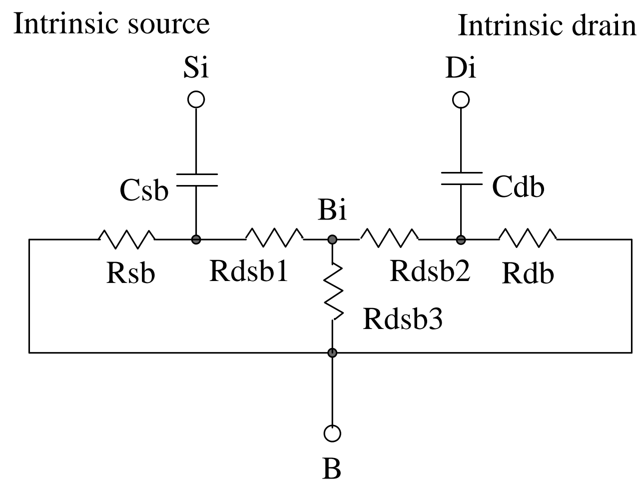


Figure 12: Five-resistor substrate network

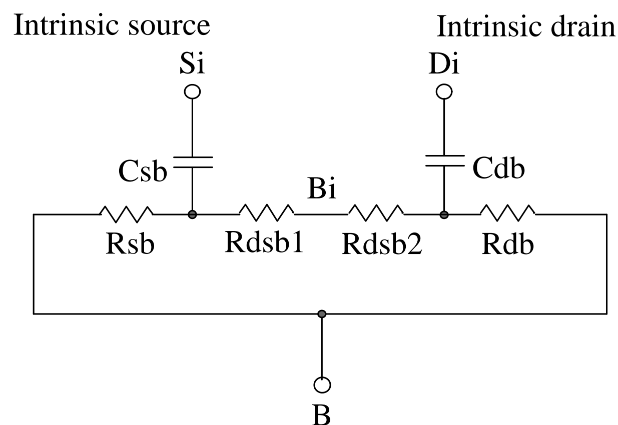


Figure 13: Four-resistor substrate network

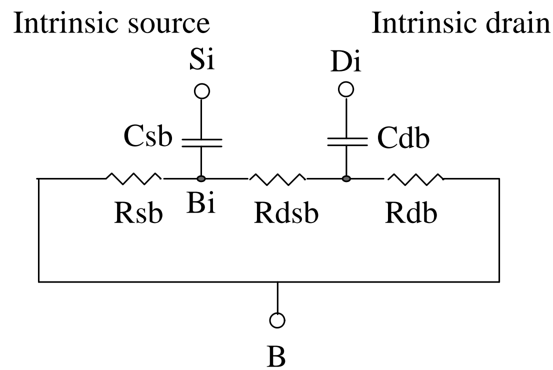


Figure 14: Three-resistor substrate network

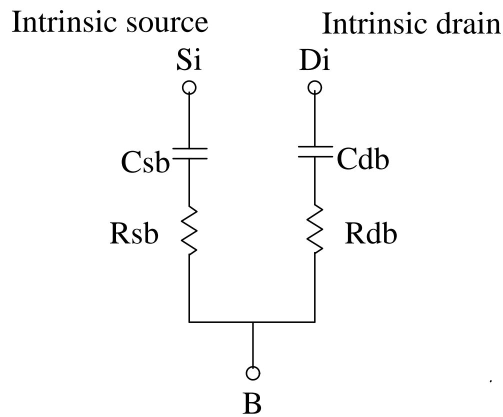


Figure 15: Two-resistor substrate network

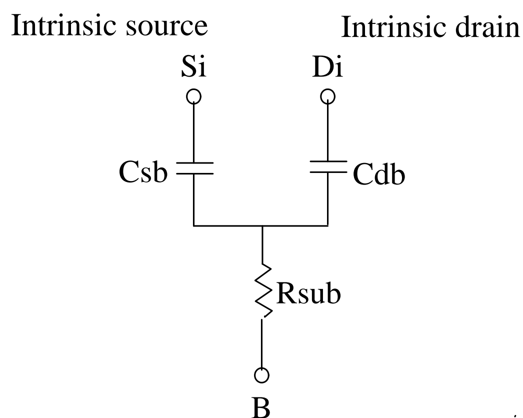


Figure 16: One-resistor substrate network

2.3.3 Extrinsic Parameter Extraction with Y-parameter analysis

Y-parameter analysis of the equivalent circuit is usually adopted to obtain the necessary equations to extract the values of some resistive and capacitive components. An equivalent circuit of sub-circuit model with intrinsic and extrinsic components is given in Figure 17. [3]. It has been well-known that R_g will influence to the input impedance Y_{11}, and R_{sub} will influence to the output impedance Y_{22}, of RF MOSFETs. So both resistances are crucial to the RF CMOS and closely related to the development of accurate device and cicuit models.

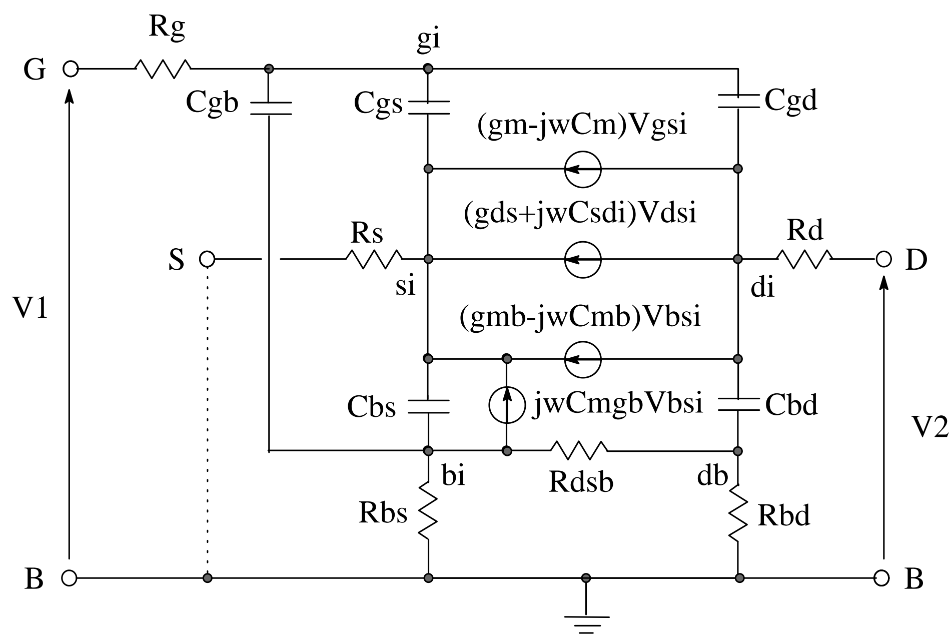


Figure 17: The small-signal equivalent circuit of Figure 9. [10][18][28].

This equivalent circuit contains too many components, espaecially current sources, which make the Y-parameter analysis very complex and difficult (if not impossible) to obtain any useful analytical expressions for the parameter extraction. In order to extract the AC parameter, the influence from the intrinsic components must be minimized. By considering the transistor biased in the strong inversion mode with V_{ds}=0V by shorting the output (drain) port, the intrinsic behavior of the transistor becomes symmetric in terms of drain and source, that is $Cgs \approx Cgd$, $Rs \approx Rd$. Therefore, the effects of the transconductances and the transcapacitances become

[3]Source and bulk are usually common and grounded in RF CMOS.

very small and can be neglected, i.e. $g_m \approx 0$, $g_{mb} \approx 0$, $C_m \approx 0$, $C_{mb} \approx 0$, $g_{sd} \approx 0$ and the small-signal equivalent circuit in Figure 17. can be simplified as shown in Figure 18., where $R_{ds}=1/g_{ds}$.

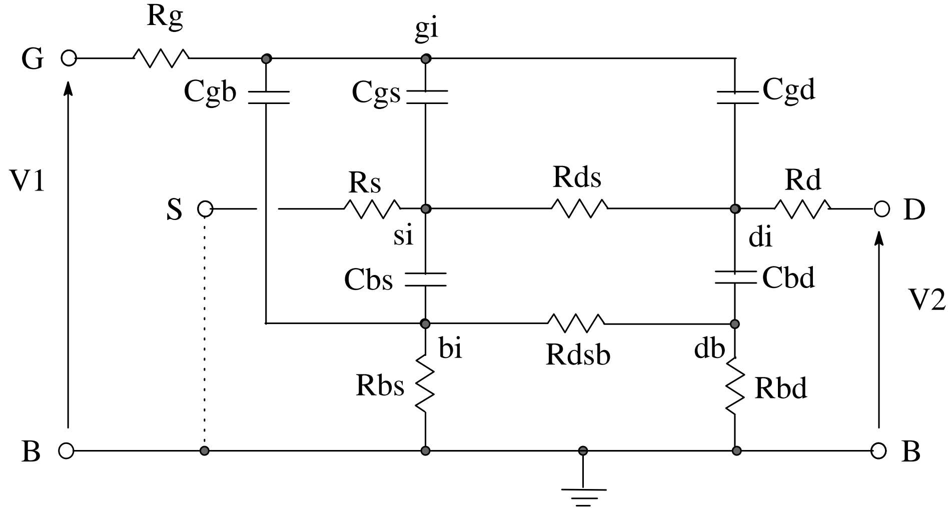


Figure 18: An equivalent circuit for the Y_{11} parameter analysis, which can obtain to short the output port i.e. drain in Figure 9. [10][18][28].

Note that the gate bias V_{gs} has to be chosen high enough, i.e. in strong inversion regime, in order for the intrinsic gate-to-bulk capacitance C_{gbi} to be small enough and neglected. However, V_{gs} is limited to a value such that the channel resistance R_{ds} stays high enough in order not to affect the values extracted for R_s and R_d. For such a gate bias, the simplified two-port network has only the resistances and capacitances, and the equivalent circuit for the Y_{11} parameter analysis is obtained.

By considering the RC time constants of the network, the equivalent circuit can be simplified further using the following assumptions.

(a) R_g, R_s and R_d are dominated by the resistive poly-silicon and diffusion layers and treated as bias- and frequency-independent.

(b) The equivalent impedance from the intrinsic source/drain nodes to the external source/drain nodes are dominated by the terminal resistances R_s and R_d

$$\left| \; j\omega C_{sb} R_s \; \right| = \omega \cdot \left(\frac{N_s}{N_F} \cdot 2H_{DIF} \cdot c'_{jsb} + L_G \cdot c'_{bsi}\right) \cdot H_{DIF} \cdot r'_s \ll 1 \qquad (2\text{–}102)$$

$$\left| \; \frac{1}{j\omega C_{sb}} \; \right| \gg R_s \qquad (2\text{–}103)$$

and

$$\left| \frac{1}{j\omega C_{db}} \right| \gg R_d; \quad (2–104)$$

(c) The relevant operation frequency is considered up to roughly 10 GHz, resulting in the following simlpifications:

$$(\omega C_{gd} R_d)^2 = (\omega \cdot (L_G \cdot c'_{gdi} + L_{ov} \cdot c'_{gdo}) \cdot H_{DIF} \cdot r'_d)^2 \ll 1 \quad (2–105)$$

$$(\omega C_{gs} R_s)^2 \ll 1,$$

$$\omega^2 C_{gs} C_{gd} (R_d + R_s) R_g \ll 1 \quad (2–106)$$

and

$$\frac{1}{1 + j\omega C_{gg} R_g} \cong 1 - j\omega C_{gg} R_g \quad (2–107)$$

where C_{gg} is defined as the total gate capacitance $C_{gg}=C_{gd}+C_{gs}+C_{gb}$.

Based on these assumptions, the following approximate equations for Y-parameters can be obtained,

$$Y_{11} \approx \omega^2 (C_{gg}^2 R_g + C_{gs}^2 R_s + C_{gd}^2 R_d) + j\omega C_{gg} \quad (2–108)$$

$$Y_{12} \approx -\omega^2 C_{gg} C_{gd} R_g - j\omega C_{gd} \quad (2–109)$$

$$Y_{21} \approx g_m \omega^2 C_{gg} C_{gd} R_g - j\omega (C_{gd} + g_m R_g C_{gg}) \quad (2–110)$$

The above expressions for Y_{11}, Y_{12} and Y_{21} contain all the information required for extracting the series resistances and intrinsic capacitances in the linear region. By taking the related Y-parameters, the extracted values for V_{ds}=0V are determined as [10][28]

$$C_{gg} = \left| \frac{Imag(Y_{11})}{\omega} \right| \quad (2–111)$$

$$C_{gd} = \left| \frac{Imag(Y_{12})}{\omega} \right| \quad (2–112)$$

$$C_{gs} = C_{gd} \quad (2–113)$$

$$C_{gb} = C_{gg} - C_{gd} - C_{gs} \quad (2–114)$$

$$R_g = \left| \frac{Real(Y_{12})}{Imag(Y_{12}) \cdot Imag(Y_{11})} \right| \quad (2–115)$$

$$R_d = \left| \frac{Real(Y_{21}) - Real(Y_{12})}{Imag(Y_{12})^2} \right| \quad (2–116)$$

$$R_s = \left| \frac{Real(Y_{11})}{Imag(Y_{11})^2} - R_g - \frac{C_{gd}^2}{C_{gg}^2} R_d \right| \cdot \frac{C_{gg}^2}{C_{gs}^2} \tag{2–117}$$

This R_g extraction model in Eq.(2-115) is not acturally sufficient, because this model ignore the high order terms and total gate capacitance. As channel length is scaled, these elements can not be ignored. So new R_g extraction model had been proposed in [22],

$$R_g = \frac{Real(Y_{11})}{Imag(Y_{11})\omega C_{gg}} = \frac{Real(Y_{11})}{Imag(Y_{11})^2} \tag{2–118}$$

This new model is considerable steady even if at high frequency. And if this model applied, R_s model in Eq.(2-117) will be also simplyfied and R_d=R_s can be obtained.

And next, measured Y_{22} analysis can make substrate resistance be extracted. However, the measured Y_{22} includes at least the contribution from the gate resistance R_g, drain series resitance R_d, source series resistance R_s, chennel resistance R_{ds}, gate-to-source capacitance C_{gs}, gate-to-drain capacitance C_{gd} and gate-to-bulk capacitance C_{gb} besides the substrate components. To extract the substrate components, the contributions of other components such as R_g and C_{gd}, etc., should be de-embedded from measured Y_{22}.

Eq.(2-111)-(2-118) are derived from measured Y-paramters biased in linear region (V_{ds}=0V) to extract the series resistances using a simplified equivalent circuit, as shown in Figure 18. Since only the imaginary parts are needed for determining the intirinsic capacitances, this extraction method for C_{gg} and C_{gd} can also be applied to the saturation region.

In the saturation region, the depletion charge is not affetcted by a charge of the drain voltage. Therefore, the capacitance $C_{bdi}\cong 0$ can be separated from the substrate effects, and C_{bd} in the equivalent circuit will be dominated by the junction capacitance C_{jdb}. To extract the equivalent admittance of the substrate coupling network, the series resistances R_g and R_d from imput and output ports are subtracted first to simplify the equivalent circuit prior to analysis.

$$Z'_{11} = Z_{11} - R_g \tag{2–119}$$

$$Z'_{12} = Z_{12} \tag{2–120}$$

$$Z'_{21} = Z_{21} \tag{2–121}$$

$$Z'_{22} = Z_{22} - R_d \tag{2–122}$$

where Z_{ij} are Z-parameters converted from measured S-paramters.

By performing Y-paramter analysis for the equivalnet circuit shown in Figure 19, equations can be obtained as below:

$$Real\left\{Y_{sub}\right\} = Real\left\{Y'_{22}\right\} - R_g(\omega C_{gd})^2 - \frac{1}{R_{ds}} \tag{2–123}$$

$$Imag\left\{Y_{sub}\right\} = Imag\left\{Y'_{22}\right\} - j\omega C_{gd} \tag{2–124}$$

where $R_{ds} = 1/g_{ds}$ and $g_{ds} = \left(\frac{1}{Real(Y'_{22})-Rs}\right)^{-1}$ where Y_{22}' is converted from Z_{22}', and Y_{sub} is the output admittance of the substrate network in Figure 20. In above analysis, the contributions of transconductances G_m and G_{mb} are ignored since no obvious current flows in the channel at the given bias conditions. Also, the influence of R_s on total admittance is not taken into account in the analysis; this is reasonable because of the dominant contribution of C_{gs}. Furthermore, the assumptions of $\omega^2(C_{gs}+C_{gb})^2R_g^2 \ll 1$ and $(\omega C_{gd})^2R_g^2 \ll 1$ are used, which are generally vaild in the frequency range up to 10 GHz.

The paramters of C_{gd} and R_g can be obtained as discussed earlier. Thus, the Y_{sub} data de-embedded from the measured Y_{22} data according to the above equations represents the contribution of the substrate network.

To extract the substrate components, such as the substrate resistance and junction capacitances, we further derive the following equation by doing a Y-parameter analysis of the substrate network in Figure 21.

$$Y_{sub} = \frac{R_{db}(R_{sb}+R_{dsb})}{R_{db}+R_{sb}+R_{dsb}}(\omega C_{db})^2 + j\omega C_{db} = R_{sub}(\omega C_{db})^2 + j\omega C_{db} \tag{2–125}$$

where, $\frac{(\omega C_{sb})^2R_{sb}^3}{R_{db}+R_{sb}+R_{dsb}} \ll 1$, $\frac{(\omega C_{sb})^2R_{db}R_{sb}^2}{R_{db}+R_{sb}+R_{dsb}} \ll 1$ and $(\omega C_{sb})^2R_{sb}^2 \ll 1$. These assumptions are valid in the frequency range up to 10 GHz. Therefore,

$$C_{db} = \frac{Imag\left\{Y_{sub}\right\}}{\omega} \tag{2–126}$$

$$R_{sub} = \frac{Real\left\{Y_{sub}\right\}}{Imag\left\{Y_{sub}\right\}} \tag{2–127}$$

Introduced parameter extraction methodologies above can be simply summerized as shown in Figure 22.

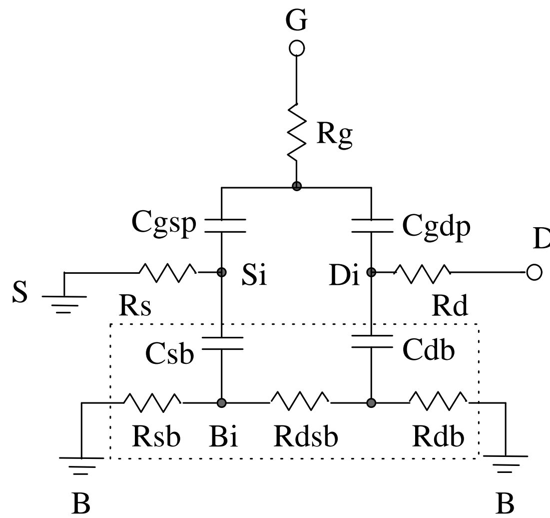


Figure 19: Equivalent circuit used for Y-parameter analysis to extract the RF model parameters.

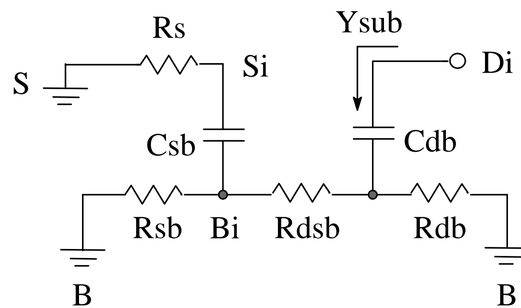


Figure 20: A simplified equivalent circiuit of the substrate network.

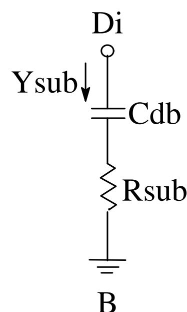


Figure 21: One resistor equivalent circuit for the substrate network.

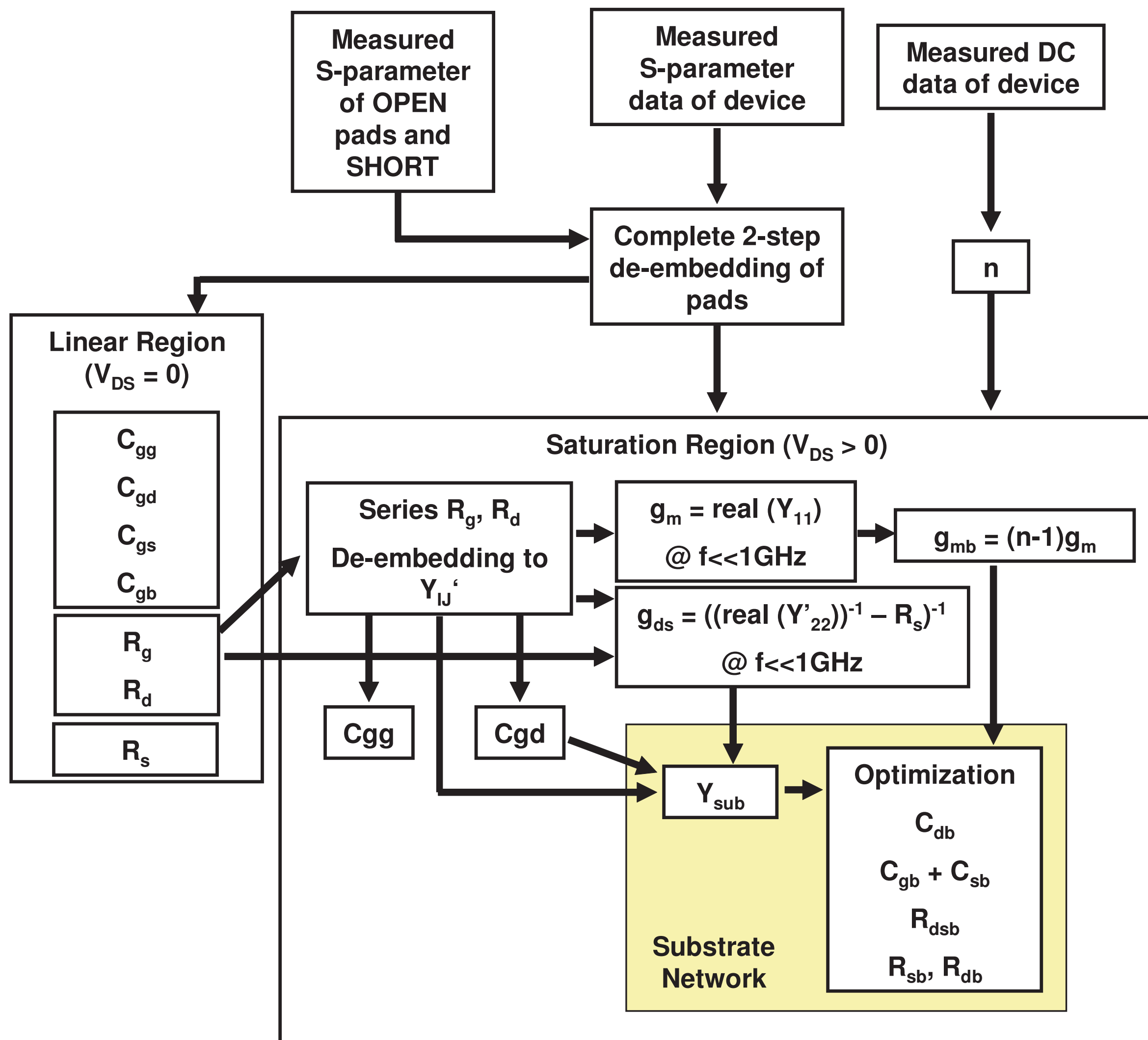


Figure 22: Parameter Extraction Flowchart

Chapter 3. Modeling of RF MOSFET with Different Layout

In this chapter, the RF performance of a 0.18 um CMOS logic technology which is adopted to the present digital and analog products, e.g. mobile telephone or personal computer etc, are assessed by evaluating the cutoff and maximum oscillation frequencies (f_T and f_{max}) of the different layed-out RF CMOS devices. Furthermore, at high frequency, as the parasitic components influence to RF performance severely, these extrinsic components such as R_g or R_{sub} or some capacitances had been extracted from measured Y-parameters directly. In conclusion, comparing with these extracted compontents, we lead to proper layout for RF CMOS.

3.1 Test Device

There are five types of different layed-out devices, as shown in Figure 23. Additionally the open and short pad for de-embedding had been prepared respectively. Test devices were fabricated with gate length (L_g) of 0.18 um, unit gate width (W_{unit}) of 2.5 um in all cases, number of finger (F) of 16 and module(M) of 4.

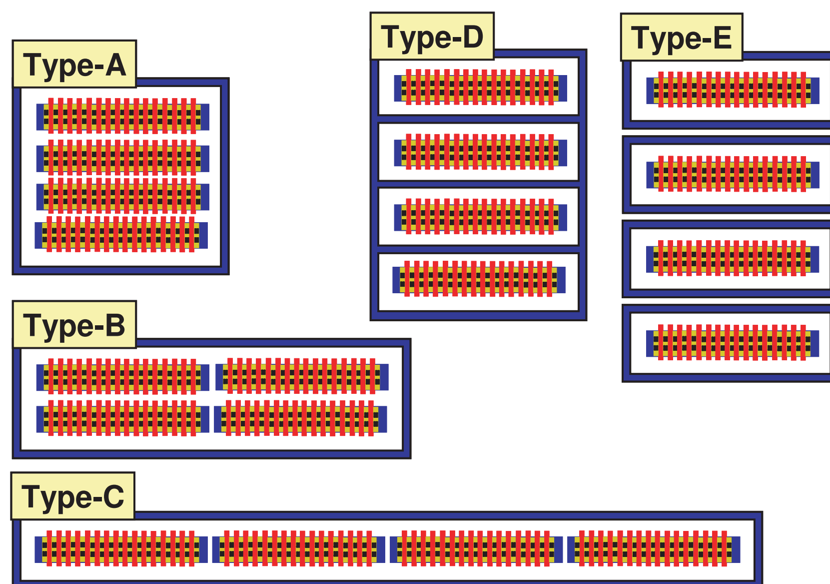


Figure 23: Test Device layout

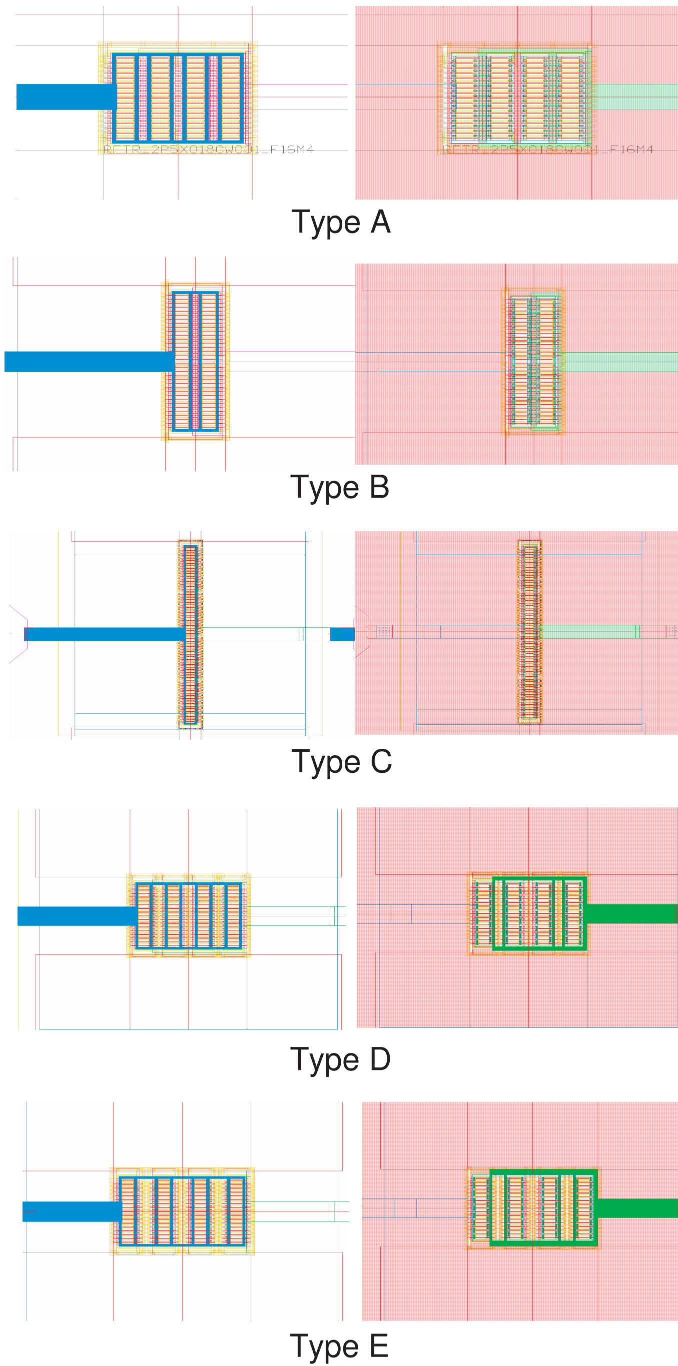


Figure 24: Interconnection lines

The schematic diagram of the interconnection lines are shown in Figure 24. Gate metal lines are shown as blue lines and drain metal are shown as green lines. Source is in common with bulk. Three layers metal (gate, drain and source) and multi-finger configuration are employed.

And the guard-ring is (are) dispensed for all devices. Type A, Type D and Type E are for verification of the guard-ring effects.

3.2 Measurement and Extrinsic Parameter Extraction

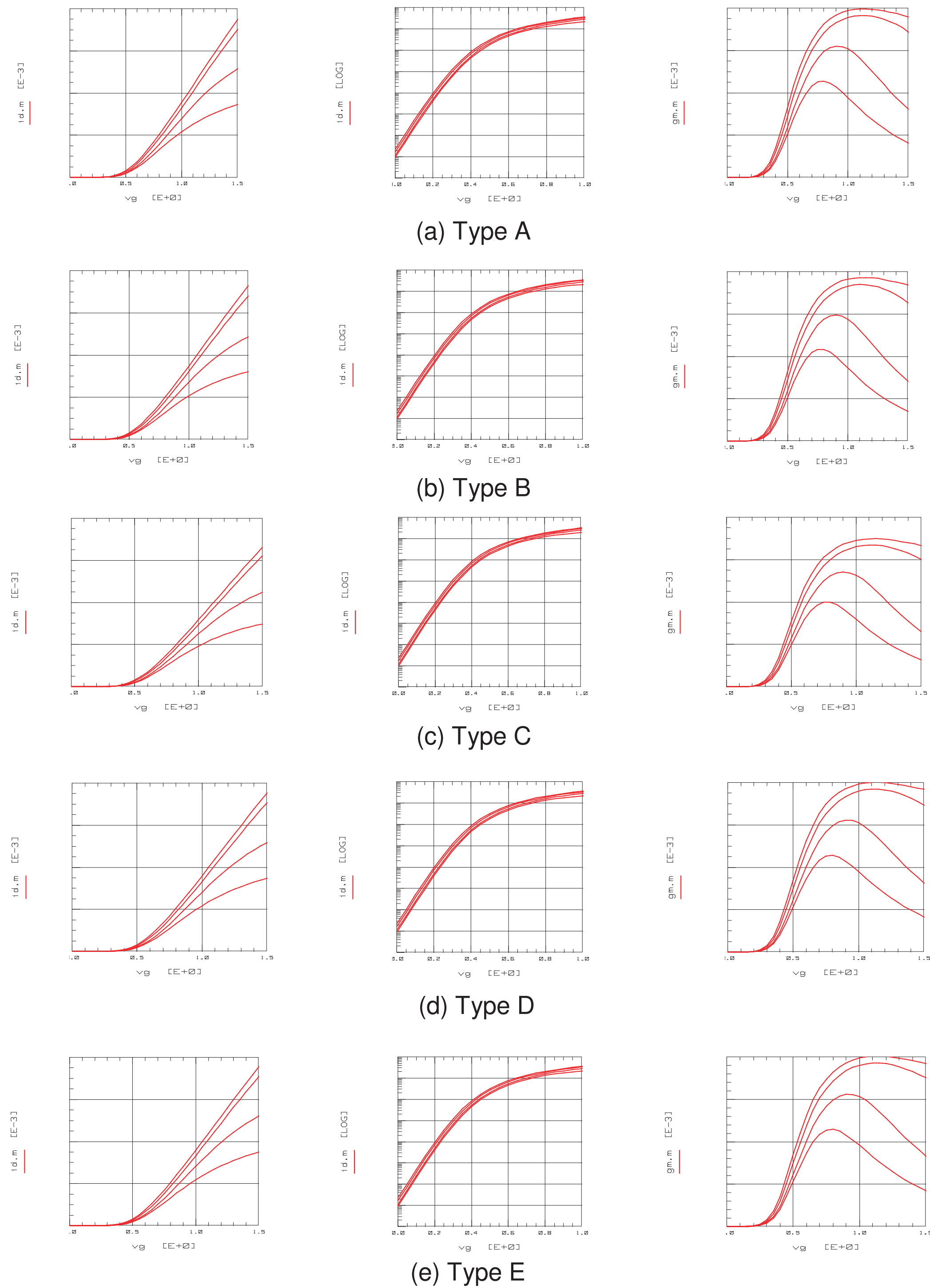
3.2.1 DC Measurement

DC measurement, I_d-V_g and I_d-V_d for various values of V_{ds} and V_{gs} as shown in Table 3, had performed against each type of devices. Figure 25.and 26. shows the result of DC measurement.

Table 3: DC measurement bias conditions

	Vg	Vd
I_d-V_g	0-1.5V	0.3/0.5/1.0/1.5V
I_d-V_d	0.4/0.6/0.8/1.0/1.5V	0-1.5V

Ideally, DC performance should be all the same, even if device layout would be different. However, only in the case of *Type C*, a little bit of drain current degradation can be found for V_g=1.0V, as shown in Figure 27. We believe that is because the effect of the interconnection resistors such as source resistance R_s and drain resistance R_d. Extrinsic resistance is critically important component and affects to MOS transistor performance largely. In deep sub-micron device, it becomes much more important because parasitic resistances are independence even if scaled down. Therefore, especially extrinsic source and drain resistance which are parasitic on interconnection lines should be considered even in DC.



(a) Type A

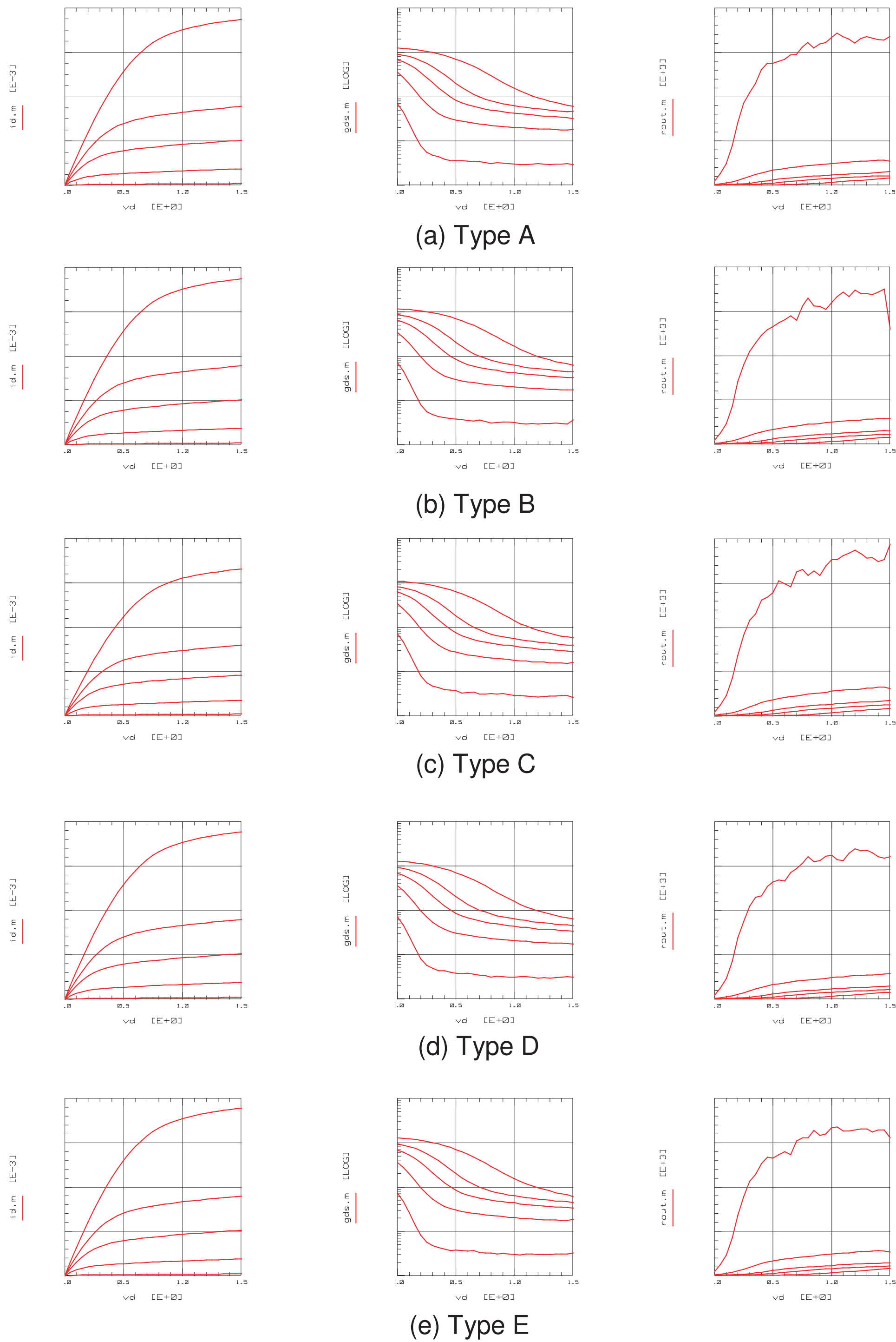
(b) Type B

(c) Type C

(d) Type D

(e) Type E

Figure 25: I_d-V_g, $\log_{10}(I_d)$-V_g and g_m-V_g of each layout type are aligned from left-side. Bias conditions ; V_g=0-1.5V / V_d=0.3, 0.5, 1.0, 1.5V



(a) Type A

(b) Type B

(c) Type C

(d) Type D

(e) Type E

Figure 26: I_d-V_d, g_{ds}-V_g and r_{out}-V_g of each layout type are aligned from left-side. Bias conditions ; V_g=0.4, 0.6, 0.8, 1.0, 1.5V / V_d=0-1.5V

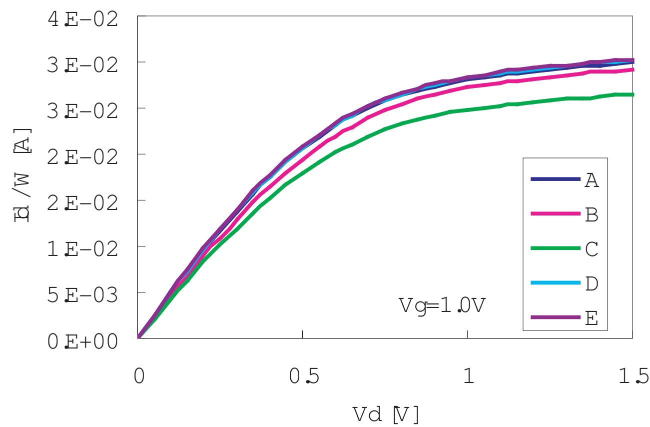


Figure 27: Gate voltage dependency of drain current at V_g=1.0V.

To compare with each extrinsic components fairly, the condition of V_g=1.0V should not be applied. So the condition of V_g=0.4V which has no drain current drop as shown in Figure 28. is applied to compare with each extrinsic components.

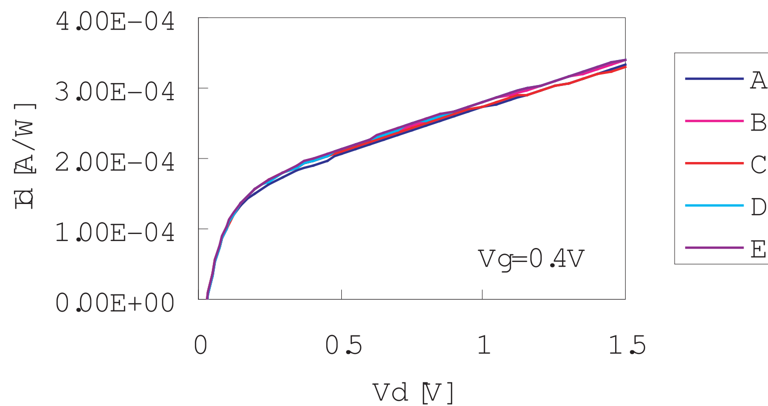


Figure 28: Gate voltage dependency of drain current at V_g=0.4V.

3.2.2 RF Measurement and De-embedding

S-parameter had measured up to 40 GHz and de-embeded for each type of devices. Here, the de-embedding procedure based on the open and short calibration test structures (see Section 2.1.1)

which had been prepared for each type of device was performed. The effects of de-embedding in S_{11} and S_{22} which express the reflection of each port are shown in Figure 29.- Figure 33. for V_g=1V and V_d=0.3/0.5/1.0V.

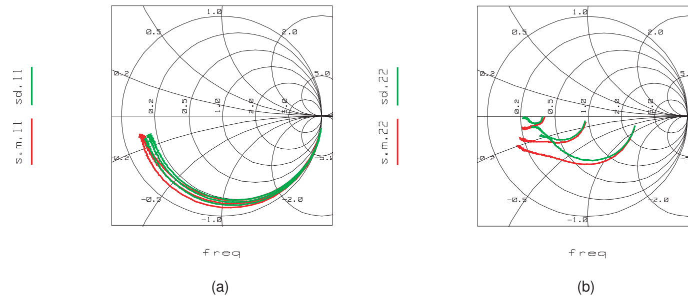


Figure 29: 【Type A】The graph of (a)S_{11} and (b)S_{22} comparing the measured raw data(red-line) with after de-embedding data with *OPEN*/*SHORT*(green-line).

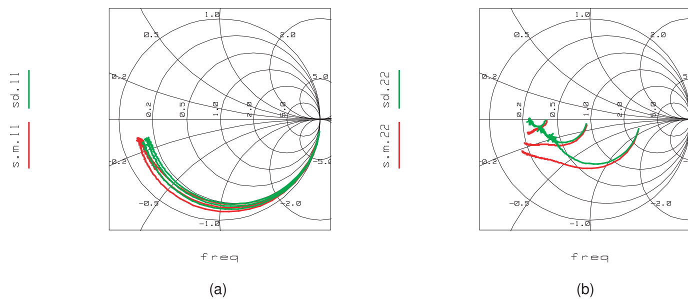


Figure 30: 【Type B】The graph of (a)S_{11} and (b)S_{22} comparing the measured raw data(red-line) with after de-embedding data with *OPEN*/*SHORT*(green-line).

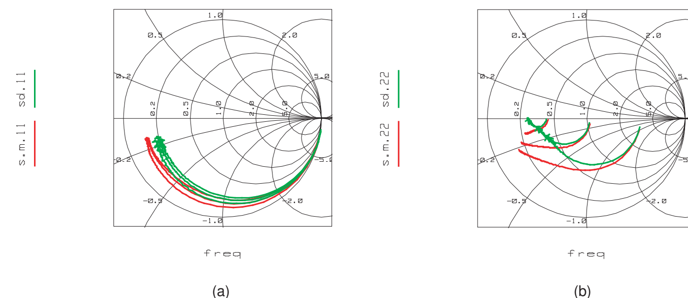


Figure 31: 【Type C】The graph of (a)S_{11} and (b)S_{22} comparing the measured raw data(red-line) with after de-embedding data with *OPEN*/*SHORT*(green-line).

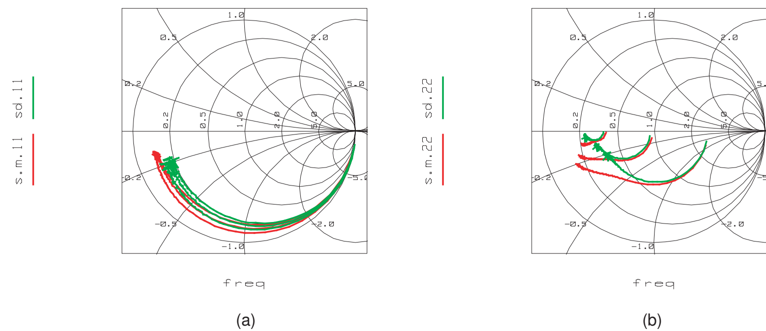


Figure 32: 【Type D】The graph of (a)S_{11} and (b)S_{22} comparing the measured raw data(red-line) with after de-embedding data with *OPEN*/*SHORT*(green-line).

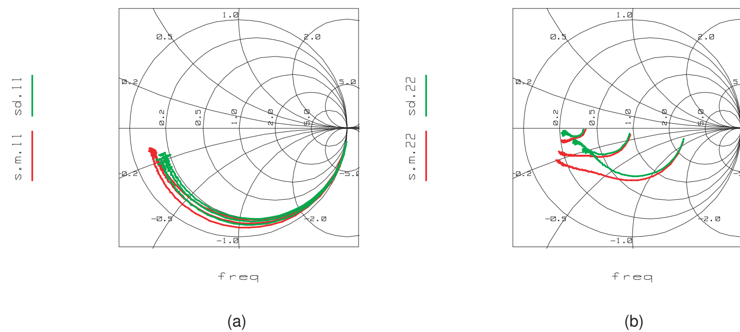


Figure 33: 【Type E】The graph of (a)S_{11} and (b)S_{22} comparing the measured raw data(red-line) with after de-embedding data with *OPEN*/*SHORT*(green-line).

After de-embedding, RF performance of intrinsic part of a transistor can be assessed by evaluating the cutoff frequency f_T and the maximum available gain f_{max} as shown in Figure 34.-43. : Figure 34, 36, 38, 40, 42. gives the value of f_T, and Figure 35, 37, 39, 41, 43. gives the value of f_{max}, which also shows the unilateral gain corresponding with f_{max} at zero gain.

f_T and f_{max} are made a comparison between each type of devices in Figure 44. and 45. There is not so much different as to f_T each figure. However, f_{max} of Type C obviously degrate due to some parasitics effects such as source and drain resistances.

【TYPE A】

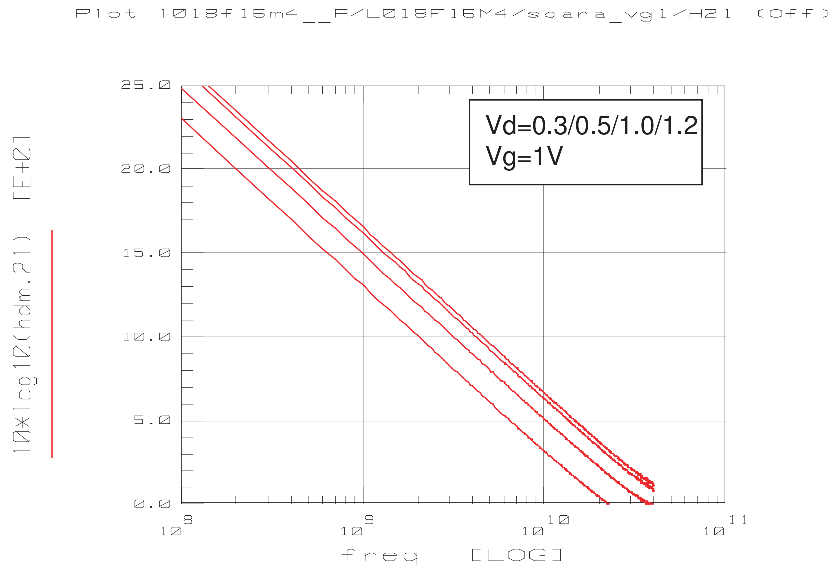


Figure 34: Frequency dependence of the cut-off frequency.

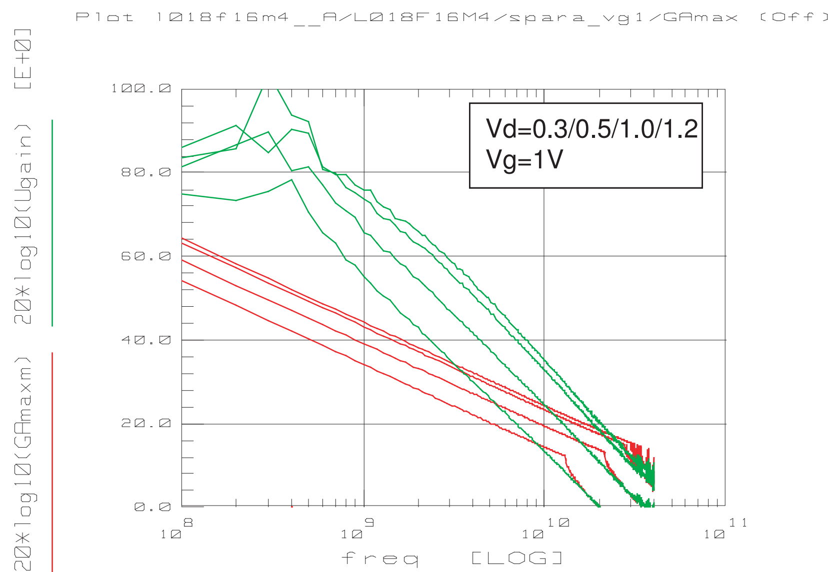


Figure 35: Frequency dependence of the maximum available gain.

【TYPE B】

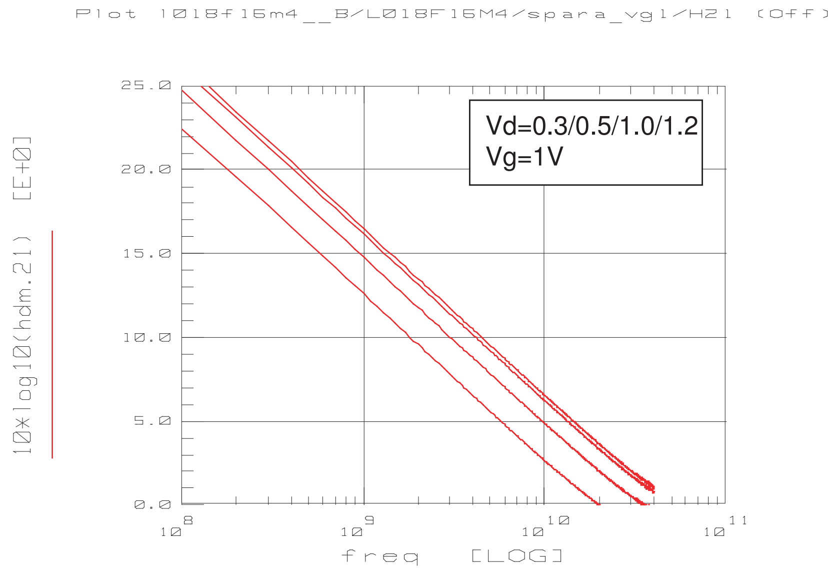


Figure 36: Frequency dependence of the cut-off frequency.

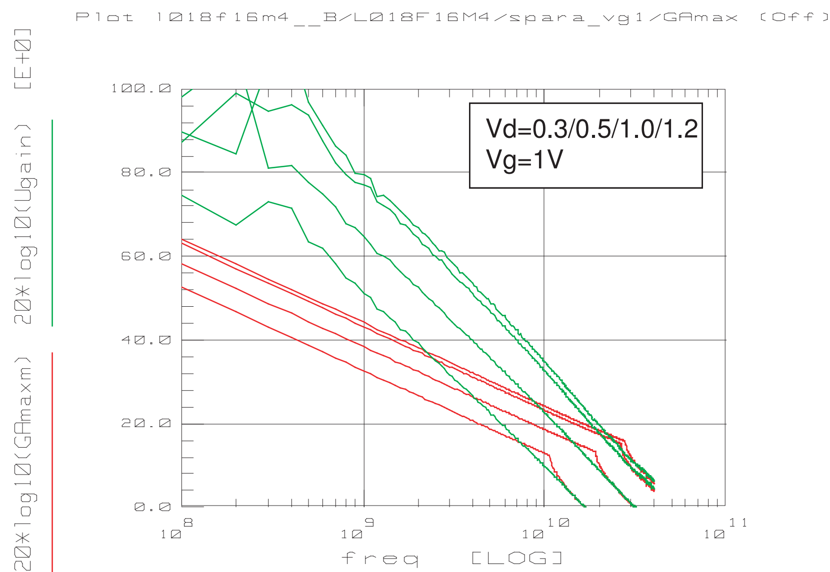


Figure 37: Frequency dependence of the maximum available gain.

【TYPE C】

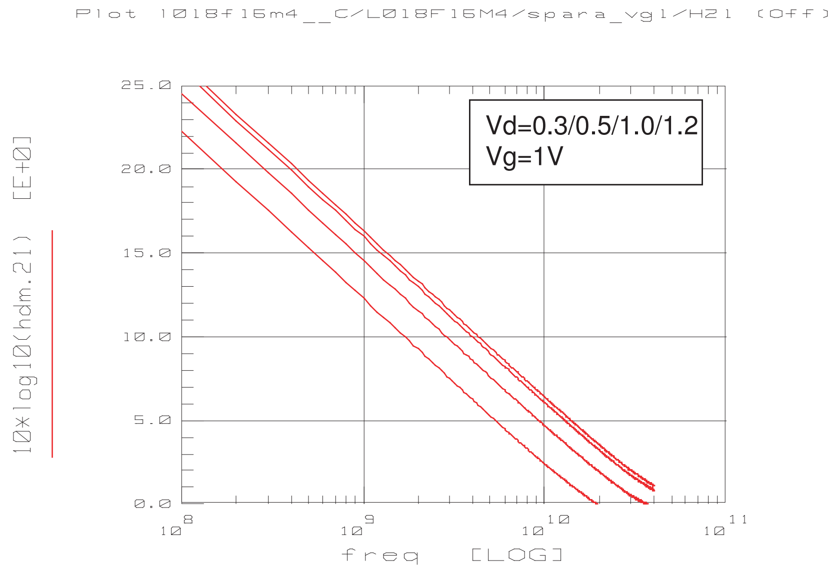


Figure 38: Frequency dependence of the cut-off frequency

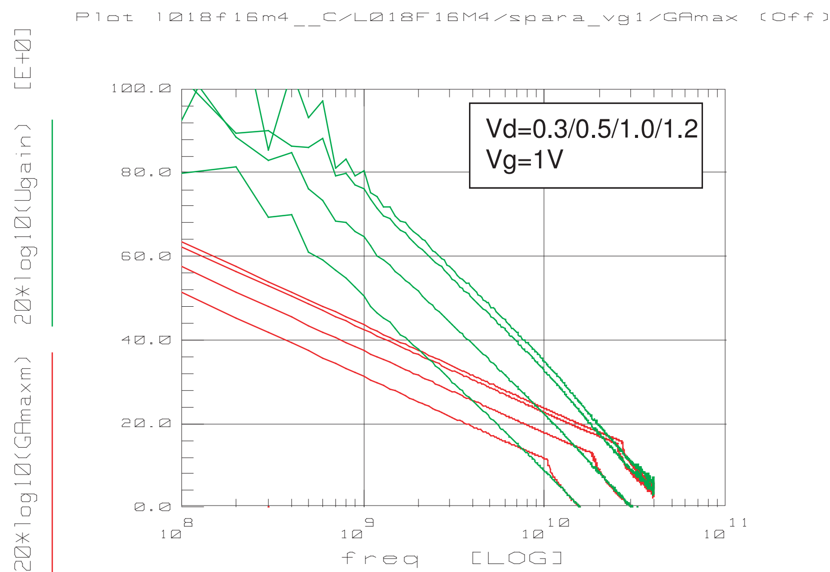


Figure 39: Frequency dependence of the maximum available gain

【TYPE D】

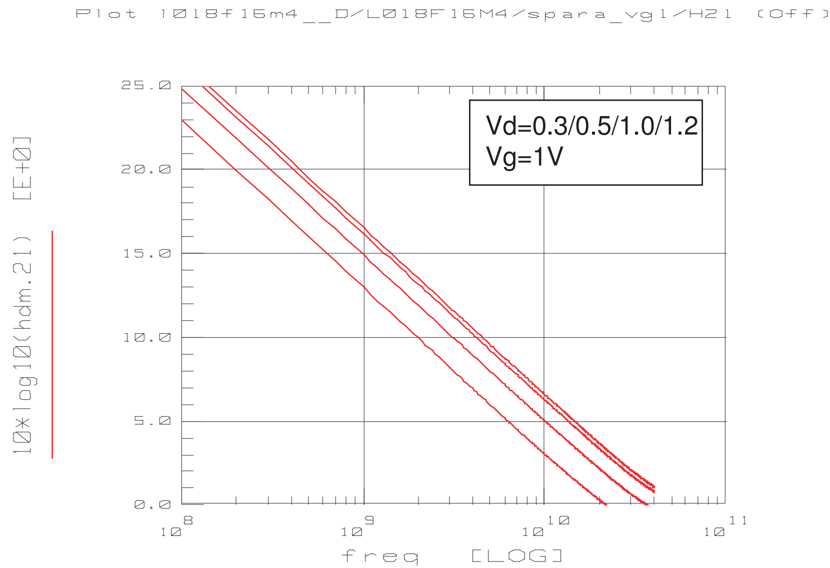


Figure 40: Frequency dependence of the cut-off frequency

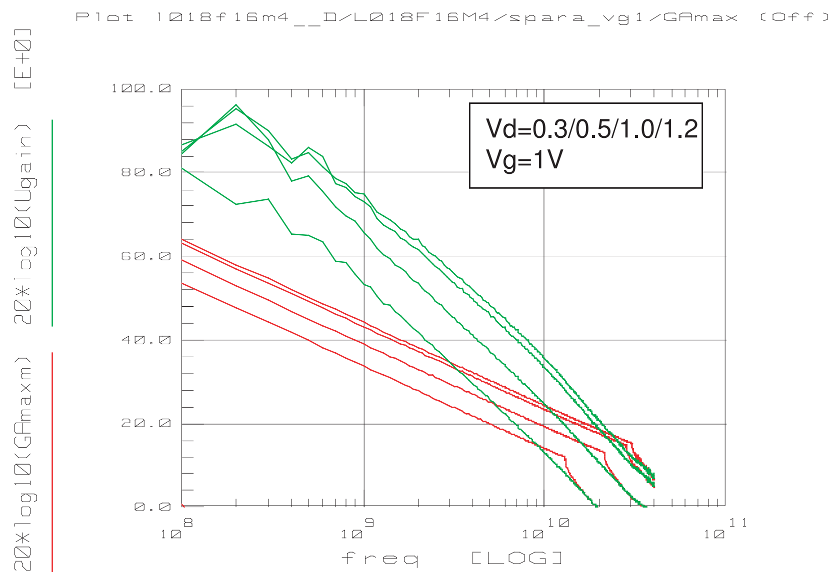


Figure 41: Frequency dependence of the maximum available gain

【TYPE E】

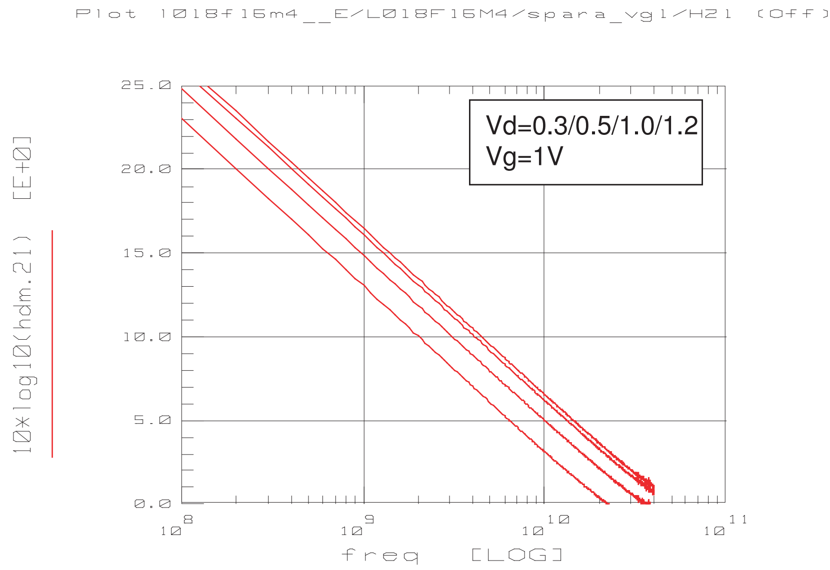


Figure 42: Frequency dependence of the cut-off frequency

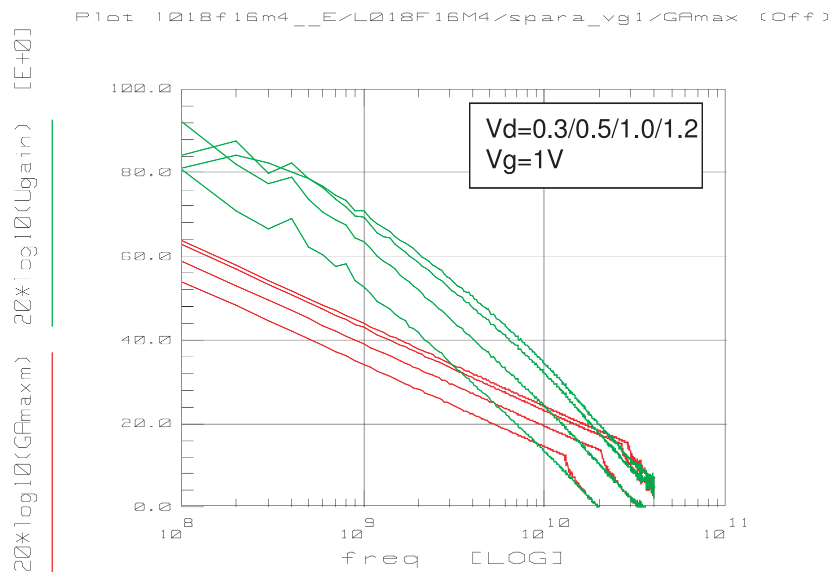


Figure 43: Frequency dependence of the maximum available gain

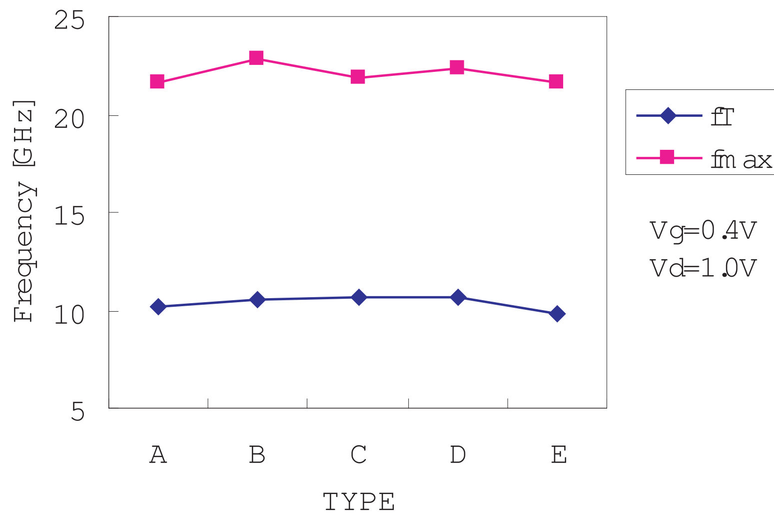


Figure 44: Comparison each type of devices with f_T and f_{max} at V_g=0.4V.

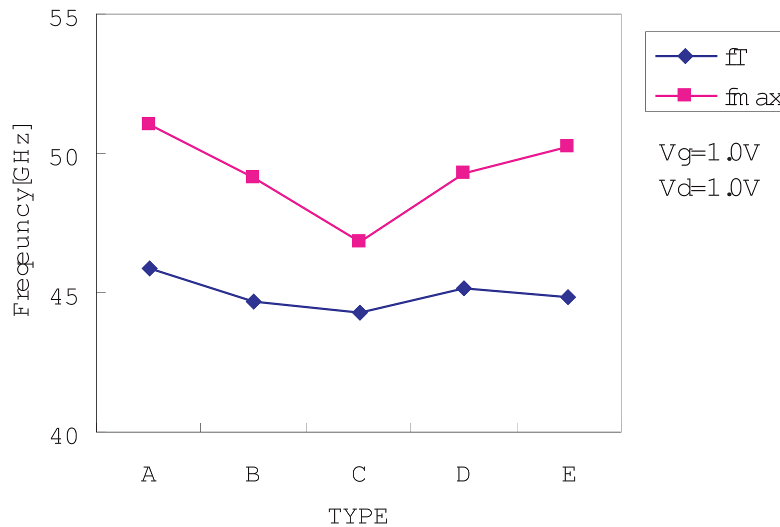


Figure 45: Comparison each type of devices with f_T and f_{max} at V_g=1.0V.

3.2.3 Extrinsic Parameter Extraction

Several extrinsic parameters discussed in section 2.3 had been directly extracted from measured Y-parameter, which had been converted from measured S-parameter, respectively.

3.2.3.1 Gate Resistance Extraction

Gate resistance had been extracted by equation (2-118) and two graphs for each device are given respectively in Figure 46.-55.: (a) frequency and gate bias dependency of the extracted gate resistance at V_{ds}=0V (see Figure 46, 48, 50, 52, 54.) and (b) gate bias dependency of the extracted gate resistance and R_g in triode and saturation region (see Figure 47, 49, 51, 53, 55.).

As shown in (a), gate resistance is sensitive to bias, but relatively independent of frequency. Although R_g had been extracted up to 15 GHz in [22], there is no statement in terms of the accuracy of over 15 GHz. However, it can be found that a stable R_g can be extracted relatively in considerable high frequency. As a little increase of extracted R_g at higher frequency can be found, it is considered as due to much further parasitics influence, which would not affect less 15 GHz. And it can be found that as gate voltage V_g increases, R_g will be saturated.

Secondly, extracted R_g relation with gate voltage V_g is shown in (b) in the case of 20 GHz. As gate voltage V_g increases, gate resistance R_g adversely decreases. As stated previously, gate electrode resistance R_{eltd} (or R_{poly}) is independent of bias, so the distributed channel resistance R_{ch}, i.e. NQS effects, contributes to this decrease and becomes zero.

R_g are made a comparison between each type of devices in triode and saturation region, as shown in Figure 56. and 57. Whereas R_g of Type D is the smallest both in triode and saturation region, R_g of Type C is the largest in both region. Extracted R_g in triode for various V_g are also shown in Figure 58. The same result can be found in this figure.

And R_g are compared with f_T and f_{max} in Figure 59. and 60. As stated previously, f_{max} has a relationship with R_g as shown in Eq.(2-5) and we can find a little gate resistance effects for f_{max}.

【TYPE A】

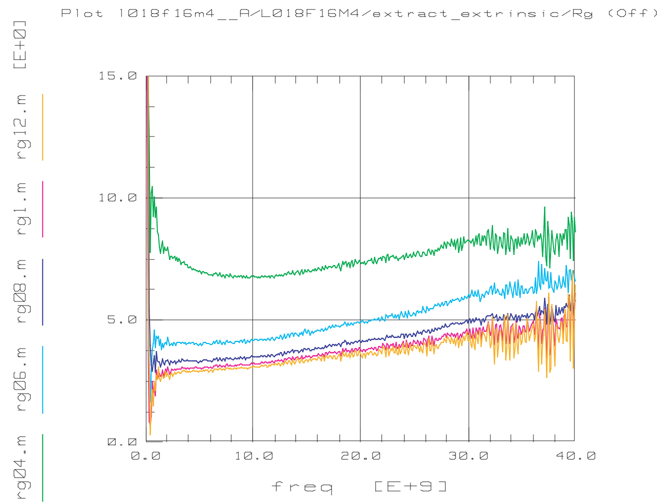


Figure 46: Frequency and gate bias dependency of the extracted gate resistance. [V_{ds}=0V]

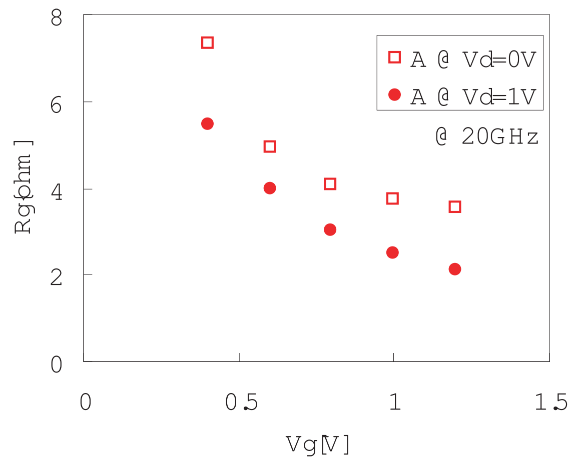


Figure 47: Gate bias dependency of the extracted gate resistance and R_g in triode and saturation region.

【TYPE B】

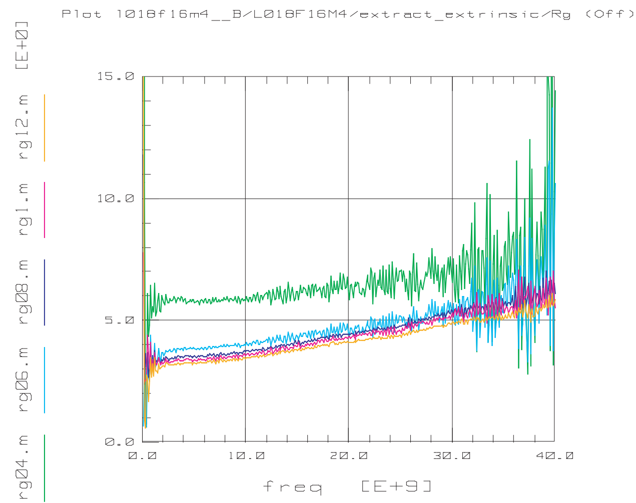


Figure 48: Frequency and gate bias dependency of the extracted gate resistance. [V_{ds}=0V]

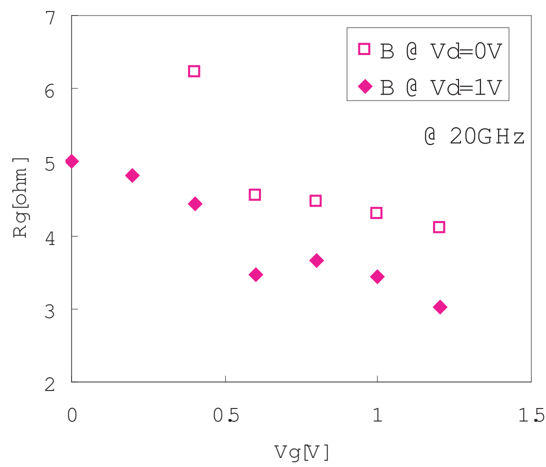


Figure 49: Gate bias dependency of the extracted gate resistance and R_g in triode and saturation region.

【TYPE C】

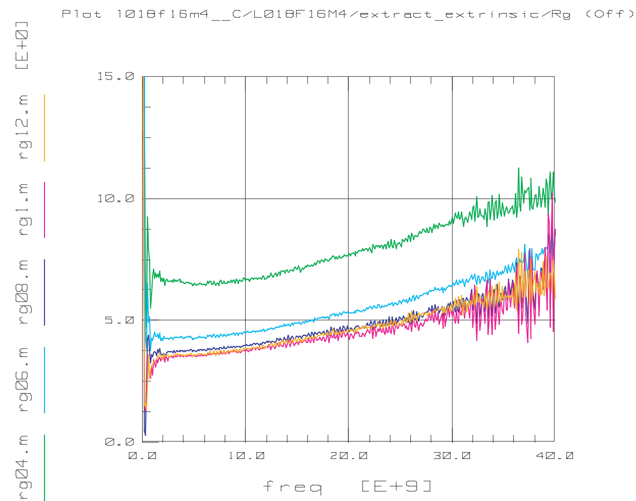


Figure 50: Frequency and gate bias dependency of the extracted gate resistance. [V_{ds}=0V]

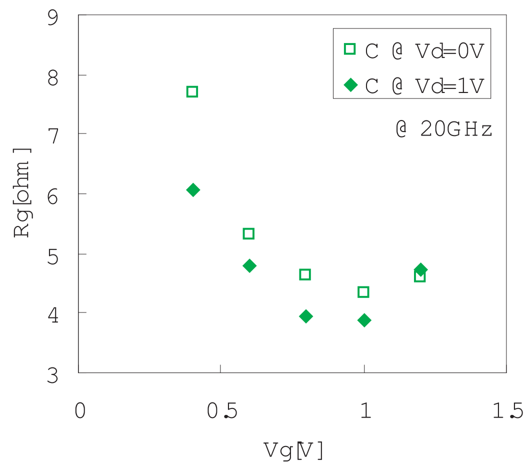


Figure 51: Gate bias dependency of the extracted gate resistance and R_g in triode and saturation region.

【TYPE D】

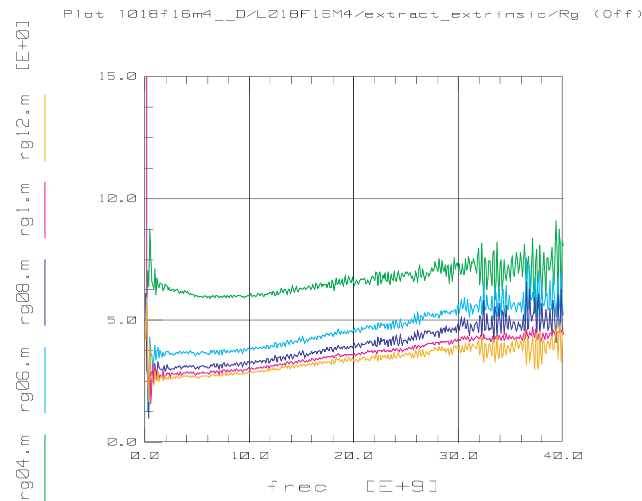


Figure 52: Frequency and gate bias dependency of the extracted gate resistance. [V_{ds}=0V]

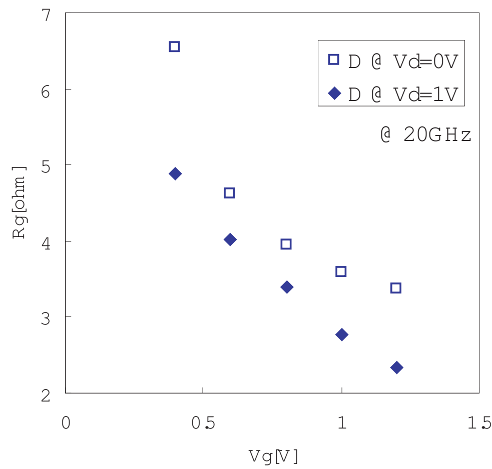


Figure 53: Gate bias dependency of the extracted gate resistance and R_g in triode and saturation region.

【TYPE E】

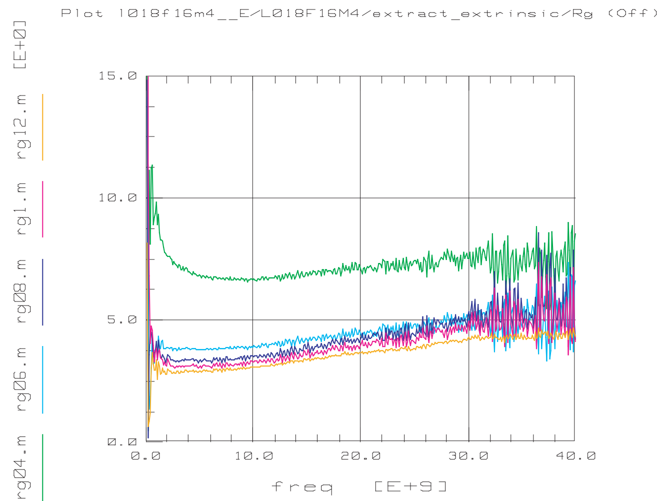


Figure 54: Frequency and gate bias dependency of the extracted gate resistance. [V_{ds}=0V]

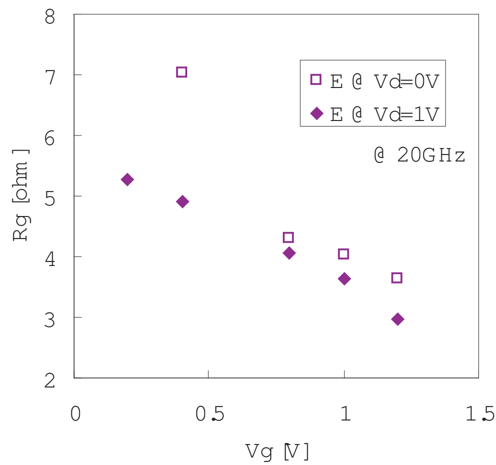


Figure 55: Gate bias dependency of the extracted gate resistance and R_g in triode and saturation region.

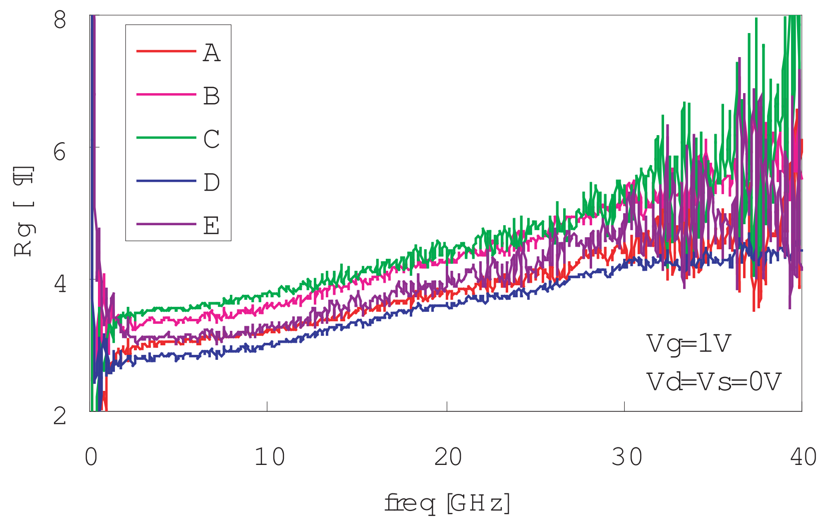


Figure 56: Frequency dependence of each device extracted R_g in the triode region.

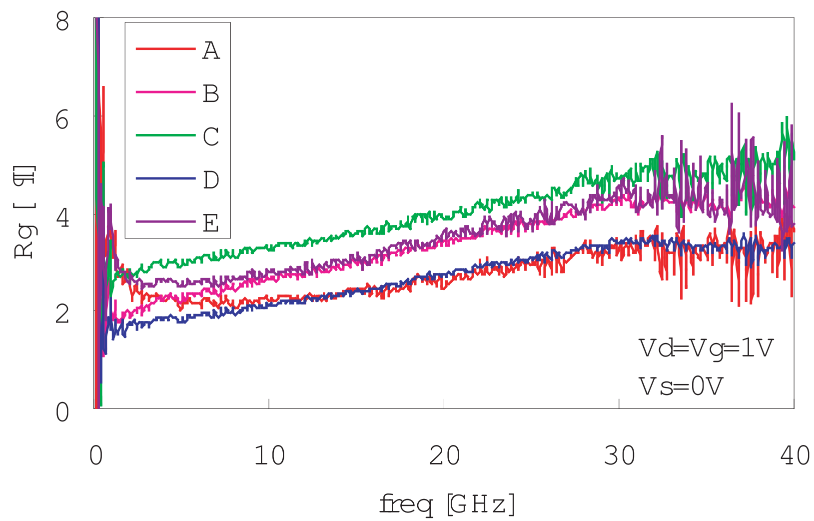


Figure 57: Frequency dependence of each device extracted R_g in the saturation region.

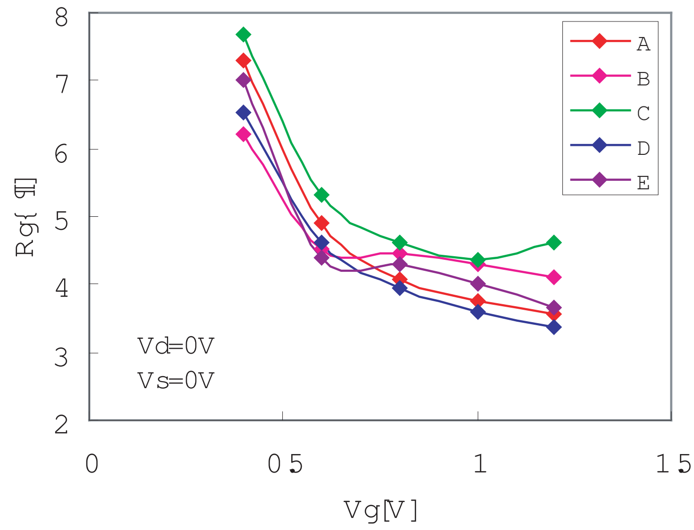


Figure 58: V_g dependence of R_g for each type of devices.

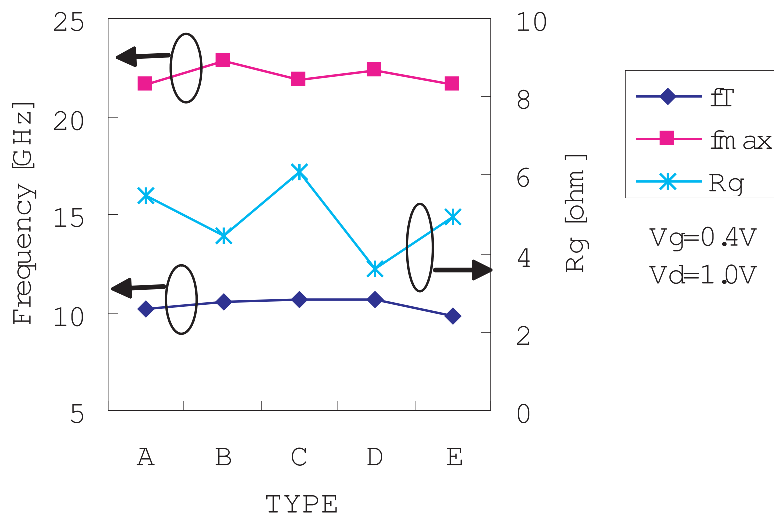


Figure 59: Comparison R_g at 20GHz with f_T and f_{max} biased V_g=0.4V, V_d=1.0V.

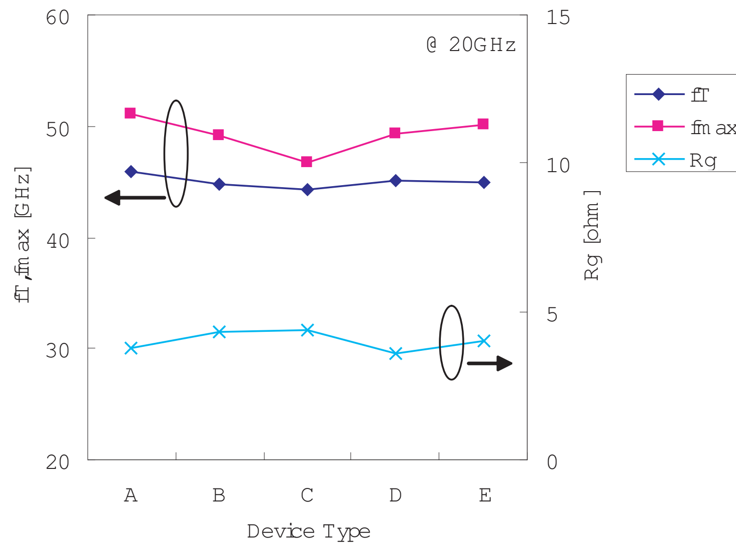


Figure 60: Comparison R_g at 20GHz with f_T and f_{max} biased V_g=1.0V, V_d=1.0V.

3.2.3.2 Gate Capacitance Extraction

Gate capacitance C_{gg} (=C_{gd}+C_{gs}+C_{gb}), C_{gd}, C_{gs} and C_{gb} had been extracted from Y-parameter analysis in the linear region (V_{gs}=1V and V_{ds}=0V). As to total gate capacitance C_{gg} at higher frequency, a little increase can be found except type E due to C_{gb} or another parasitic effects. If some other parasitics affect this increase, this C_{gg} model must be more developed for higer frequency. However, at least, it can be said that dielectric relaxation does not yield. And as to R_s and R_d, it is relatively stable even at high frequency.

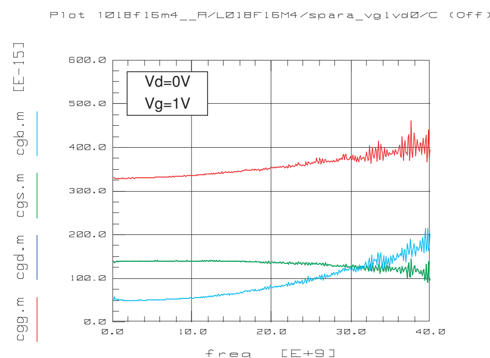


Figure 61: 【Type A】Extracted values of C_{gg}, C_{gd}, C_{gs} and C_{gb} at a given bias condition.

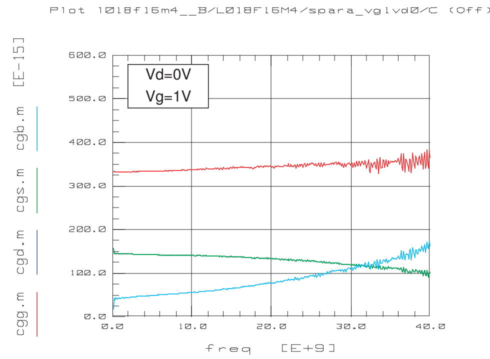


Figure 62: 【Type B】Extracted values of C_{gg}, C_{gd}, C_{gs} and C_{gb} at a given bias condition.

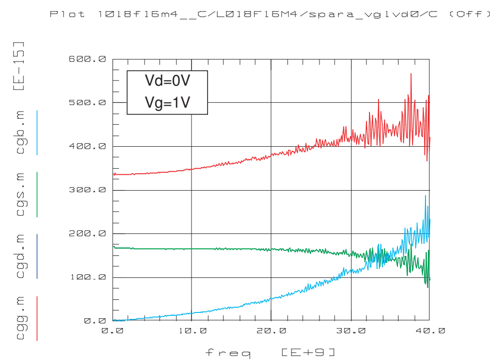


Figure 63: 【Type C】Extracted values of C_{gg}, C_{gd}, C_{gs} and C_{gb} at a given bias condition.

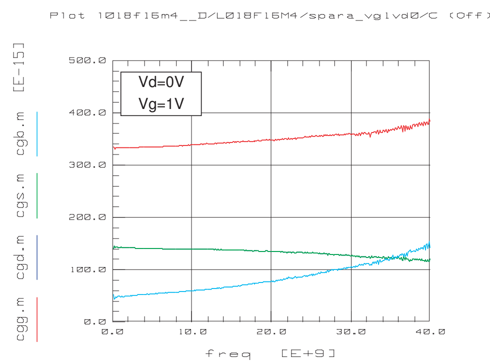


Figure 64: 【Type D】Extracted values of C_{gg}, C_{gd}, C_{gs} and C_{gb} at a given bias condition.

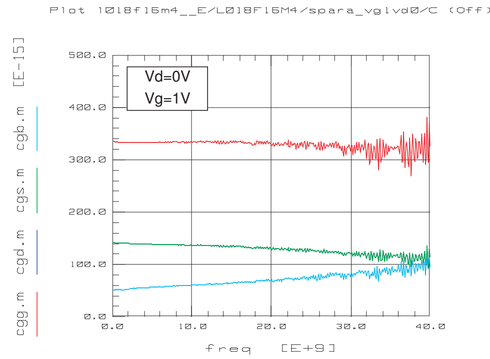


Figure 65: 【Type E】Extracted values of C_{gg}, C_{gd}, C_{gs} and C_{gb} at a given bias condition.

Frequency dependence of C_{gg} for various values of V_g, 0/0.2/0.4/0.6/0.8/1.0/1.2V, are shown in Figure 66.- 70. and C_{gg} are made a comparison between each type of devices in triode region, as shown in Figure 71.

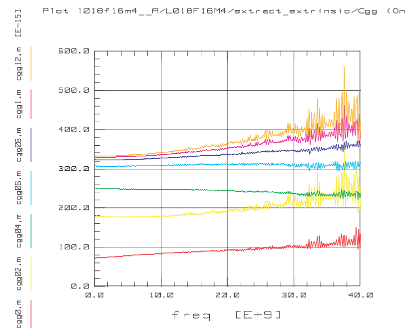


Figure 66: 【TYPE A】Frequency dependence of the extracted total gate Capacitance C_{gg}.

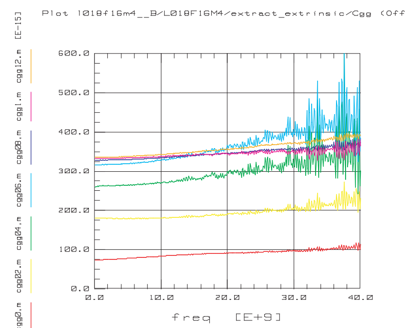


Figure 67: 【TYPE B】Frequency dependence of the extracted total gate Capacitance C_{gg}.

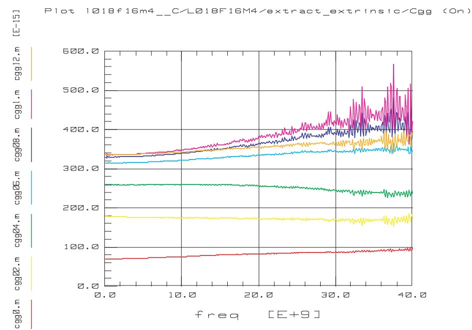


Figure 68: 【TYPE C】Frequency dependence of the extracted total gate Capacitance C_{gg}.

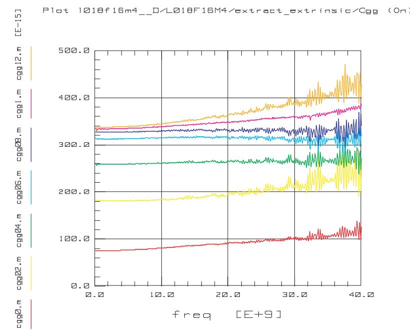


Figure 69: 【TYPE D】Frequency dependence of the extracted total gate Capacitance C_{gg}.

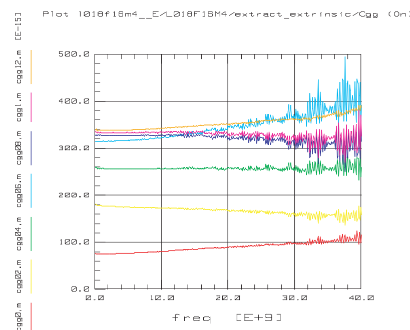


Figure 70: 【TYPE E】Frequency dependence of the extracted total gate Capacitance C_{gg}.

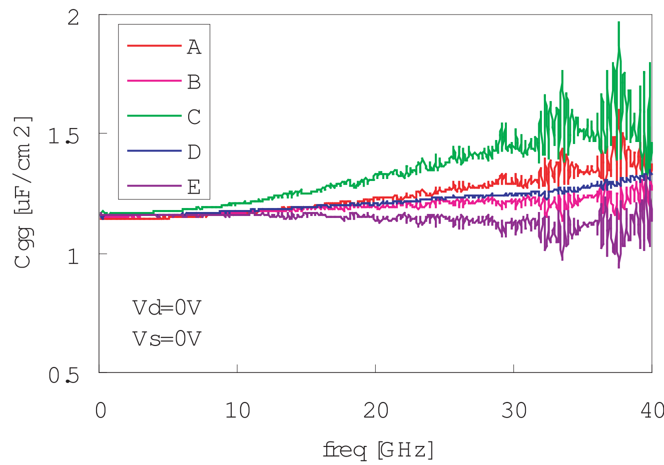


Figure 71: Frequency dependence of C_{gg} for each type of devices.

3.2.3.3 Substrate Network Analysis

Substrate resistance R_{sub} had been extracted from analyzing measured Y_{22} parameter. In the linear region, although substrate resistance R_{sub} is independent of bias, substrate resistance starts to increase at $V_g \geq V_{th}$.

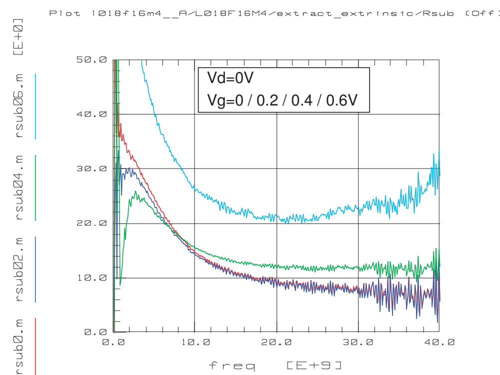


Figure 72: 【TYPE A】Frequency dependence of extracted substrate resistance R_{sub}.

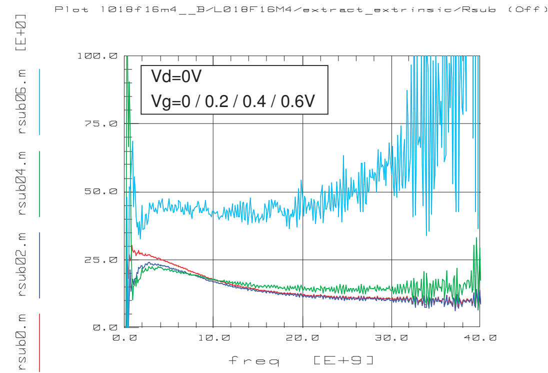


Figure 73: 【TYPE B】Frequency dependence of extracted substrate resistance R_{sub}.

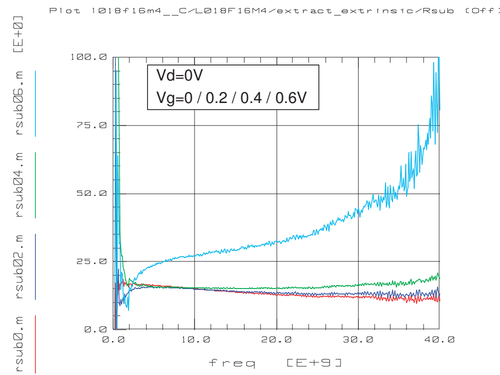


Figure 74: 【TYPE C】Frequency dependence of extracted substrate resistance R_{sub}.

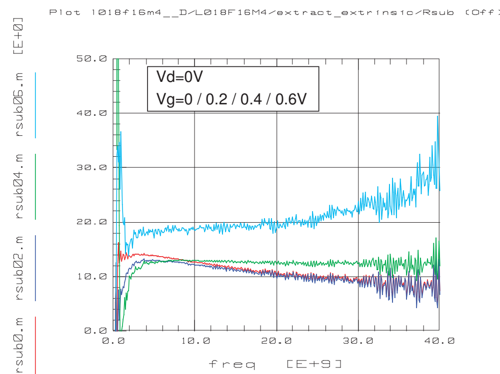


Figure 75: 【TYPE D】Frequency dependence of extracted substrate resistance R_{sub}.

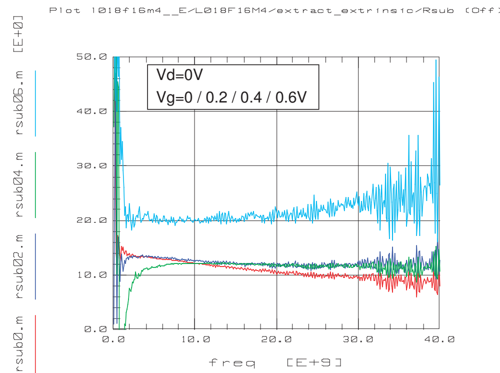


Figure 76: 【TYPE E】Frequency dependence of extracted substrate resistance R_{sub}.

Each type of devices are made a comparison between R_{sub} in Figure 77. Even though R_{sub} of type A and B are not stable at low frequency, R_{sub} of type C, D and E can be obtained a stable extracted value. Over at 20 GHz region, R_{sub} of Type C is the largest and of Type E is the smallest. To compare with an each stable extracted data, the values at 20 GHz will be discussed in Figure 78., which displays the comparison R_{sub} with f_T and f_{max}.

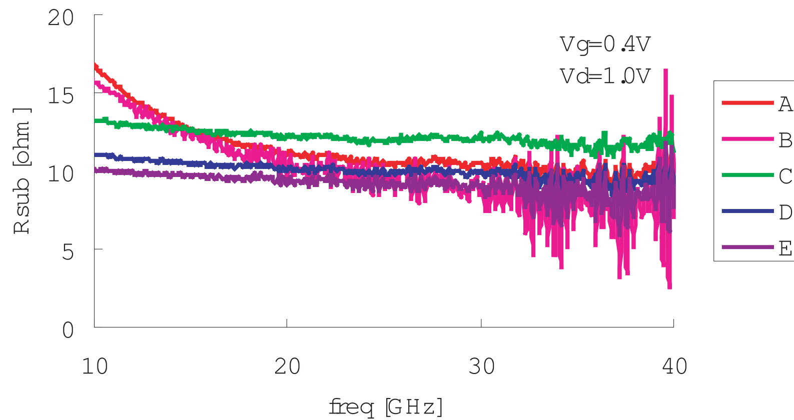


Figure 77: Frequency dependence of R_{sub} for each type of devices.

We can find that f_{max} is in disagreement with substrate resistance R_{sub} except Type E. We consider that the substrate resistance of Type D and E should be same ideally. We can guess effects of the substrate resistance from Figure 79. as below:

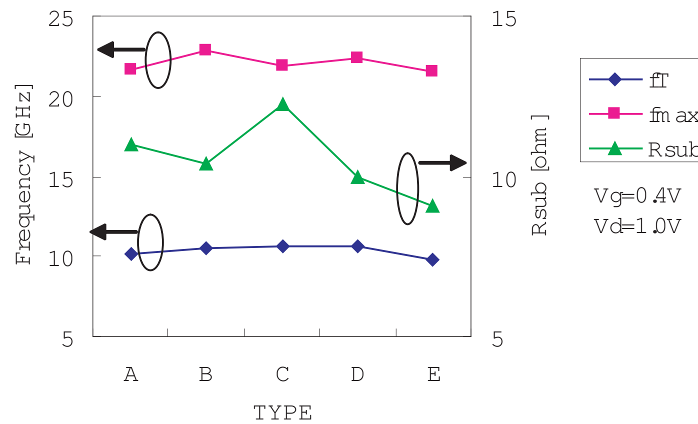


Figure 78: Comparison substrate resistance at 20GHz with f_T and f_{max}.

- Type A : Vertical resistance increase.
- Type B : Both vertical and horizontal resistance increase.
- Type C : Horizontal resistance increase.
- Type D and E : Both vertical and horizontal resistance minimize.

According to this guess, the substrate resistance of each devices can be considered as (D or E)<(A or B)<C. The results as shown in Figure 78. are like, E<D<B<A<C. Therefore, we can consider this guess is roughly proper. However, we should analyse more physically.

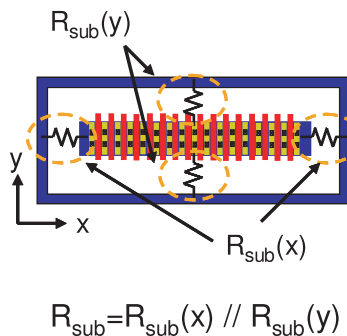


Figure 79: Effect of geometric

We summarize each extracted extrinsic components and RF characteristic f_T, f_{max} in Figure 80. Since gate voltage is around threshold voltage, f_T and f_{max} represent not so much difference, however we can find gate resistance and substrate network resistance largely affetct device RF performance.

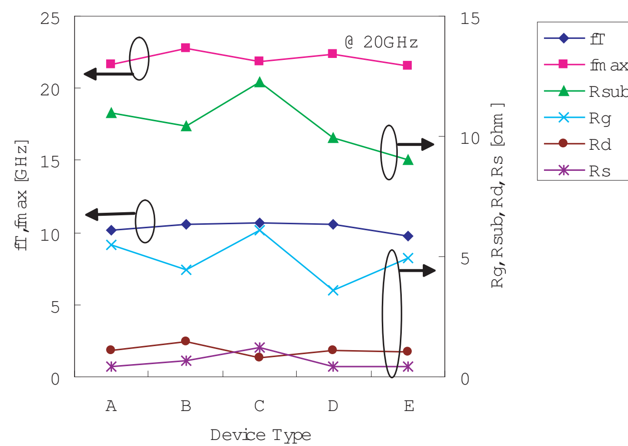


Figure 80: Comparison gate, source/drain and substrate resistance at 20GHz with f_T and f_{max} biased V_g=0.4V, V_d=1.0V.

3.3 Modeling of Test Device

3.3.1 DC Parameter Extraction

DC parameter extraction of test device had been performed as following. As stated previously, source and drain resistances must be considered due to its critical effects. Two approaches to model the parasitic source and drain resistances were introduced in section 2.2.9: (a) *lumped-resistance approach* and (b) *absorbed-resistance approach*. In this works, the *lumped-resistance approach* was chosen due to in the following: (1) To extract DC parameters more accurately. and (2) To obtain intrinsic transistor parameters, i.e. not including the parasitic components (resistances only in the case of DC). This is because in modeling of RF MOSFETs, as de-embedding is usually performed, intrinsic part of transistor will be only discussed.

After adding source/drain series resistances as shown in Figure 81., DC parameters were ex-

tracted with the compact model BSIM3v3 [4]. By using this model, DC simulation had been performed. As source and drain resistance, R_s and R_d, were added to the intrinsic part of transistor respectively, all same DC parameters were used for each devices in this simulation. The results of I_d-V_g simulations are shown in Figure 82. - Figure 86. and the results of I_d-V_d simulations are shown in Figure 87. - Figure 91.

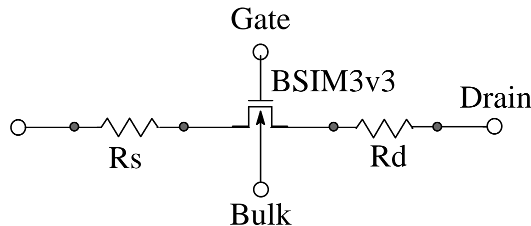


Figure 81: DC model including source and drain line resistances.

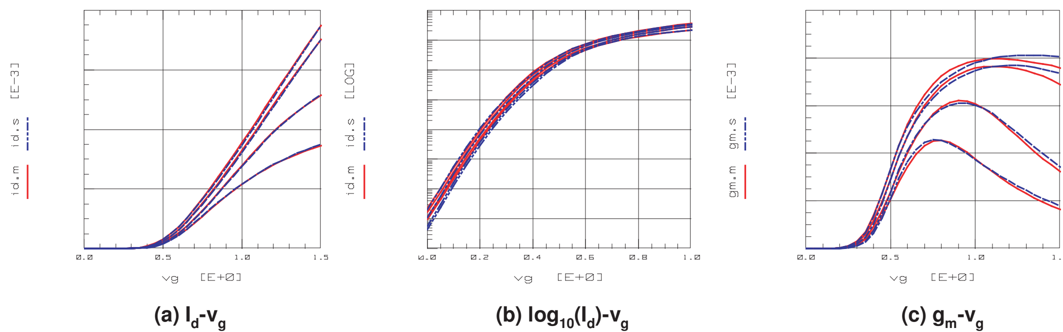


Figure 82: 【Type A】(a)I_d-V_g, (b)$\log_{10}(I_d)$-V_g and (c)g_m-V_g had been simulated with DC model.

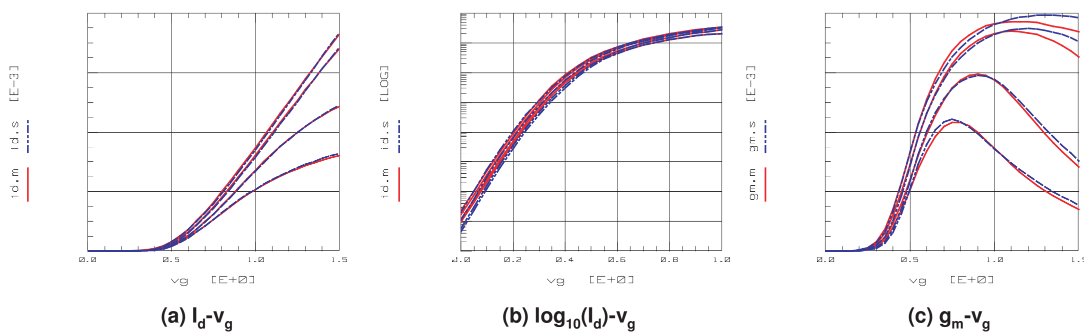


Figure 83: 【Type B】(a)I_d-V_g, (b)$\log_{10}(I_d)$-V_g and (c)g_m-V_g had been simulated with DC model.

[4]Note that the model shown in Figure 81. is intrinsic part of transistor, i.e. after de-embedded part.

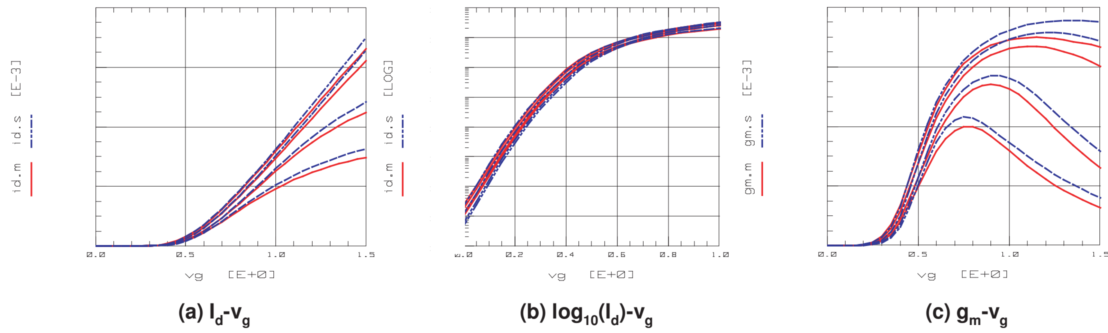


Figure 84: 【Type C】(a)I_d-V_g, (b)$\log_{10}(I_d)$-V_g and (c)g_m-V_g had been simulated with DC model.

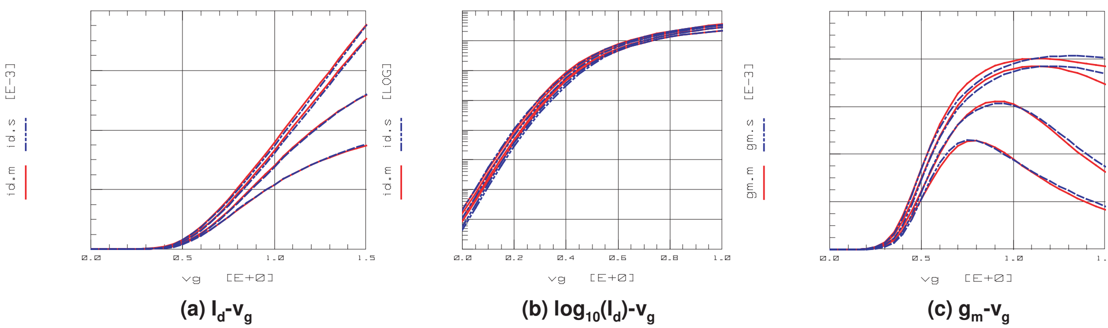


Figure 85: 【Type D】(a)I_d-V_g, (b)$\log_{10}(I_d)$-V_g and (c)g_m-V_g had been simulated with DC model.

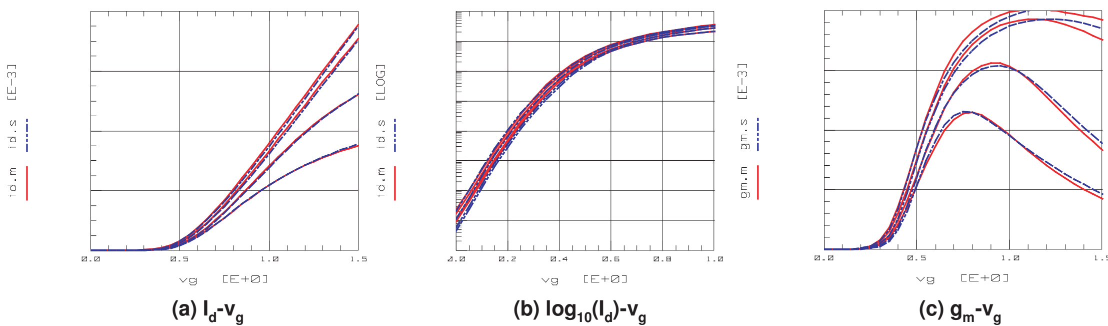


Figure 86: 【Type E】(a)I_d-V_g, (b)$\log_{10}(I_d)$-V_g and (c)g_m-V_g had been simulated with DC model.

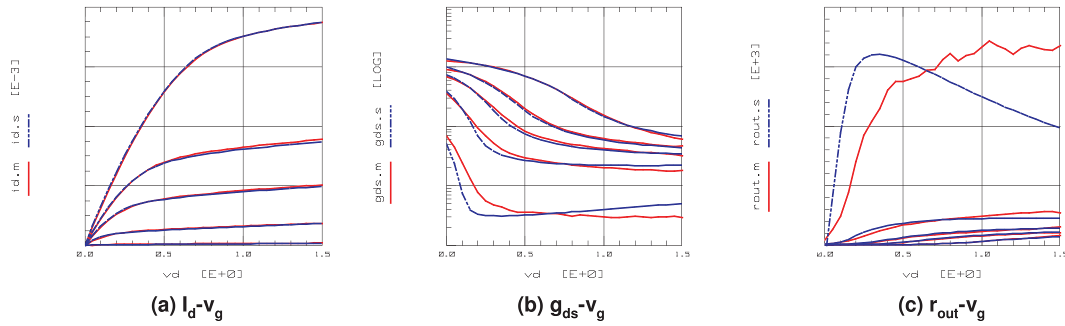


Figure 87: 【Type A】(a)I_d-V_d, (b)g_{ds}-V_g and (c)r_{out}-V_g had been simulated with DC model.

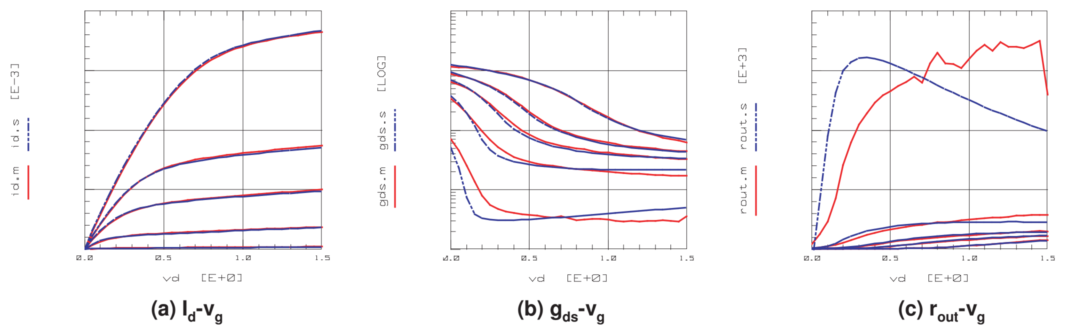


Figure 88: 【Type B】(a)I_d-V_d, (b)g_{ds}-V_g and (c)r_{out}-V_g had been simulated with DC model.

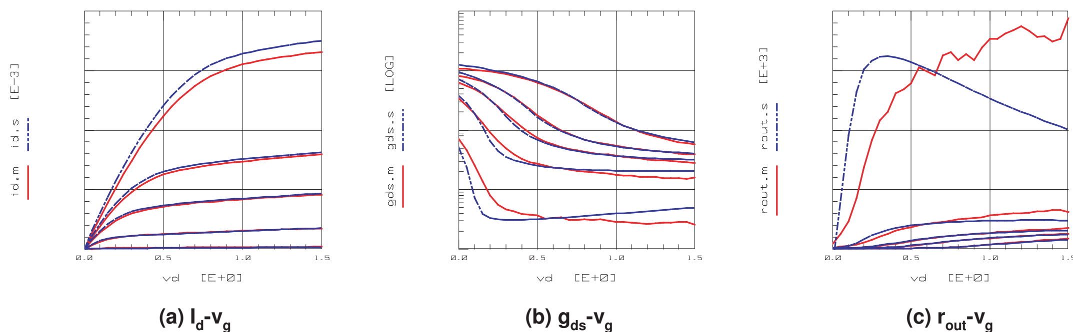
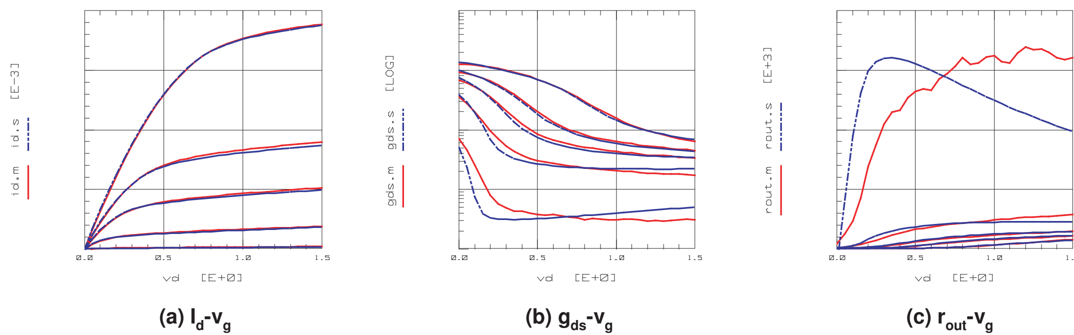


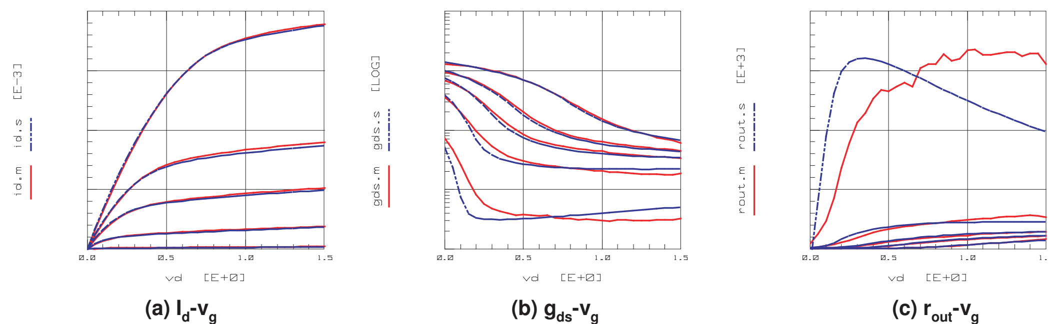
Figure 89: 【Type C】(a)I_d-V_d, (b)g_{ds}-V_g and (c)r_{out}-V_g had been simulated with DC model.

Although the each results of DC simulation consistent with DC characteristics at higher gate voltage, a little difference can be found at lower gate voltage. It may consider the limit of BSIM3v3. Therefore, although I_d drop will occur at Type C, we modeled at higher gate voltage region, V_g=1V and V_g=1V, in next section.



(a) I_d-V_g (b) g_{ds}-V_g (c) r_{out}-V_g

Figure 90: 【Type D】(a)I_d-V_d, (b)g_{ds}-V_g and (c)r_{out}-V_g had been simulated with DC model.



(a) I_d-V_g (b) g_{ds}-V_g (c) r_{out}-V_g

Figure 91: 【Type E】(a)I_d-V_d, (b)g_{ds}-V_g and (c)r_{out}-V_g had been simulated with DC model.

3.3.2 RF Equivalent Circuit Model

By using extracted extrinsic parameters, sub-circuit model is proposed. In modeling, not only extraction but also optimize must be performed and had been done. Although we have not already completed, we propose the RF compact model as shown in Figure 92. As shown in Figure 93., S11 has been simulated well relatively. However S22 shows bad fitting. This means that the input port components such as R_g, R_s, C_{gs}, and C_{gd}, had been optimized well, but the output port components such as substrate network resistance, substrate capacitance and/or some other components, had not been optimized yet. Therefore, we should analyse which components

influence to the output port in detail.

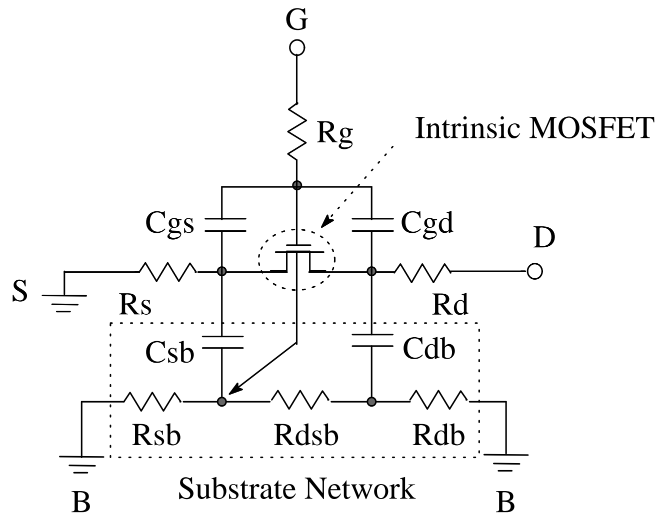


Figure 92: Sub-circuit model

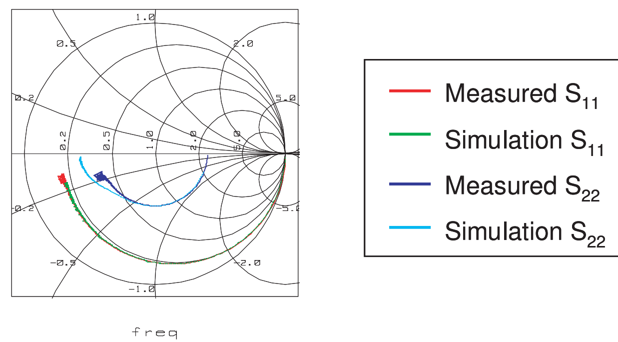


Figure 93: Measured and simulated S-parameter of S11 and S22.

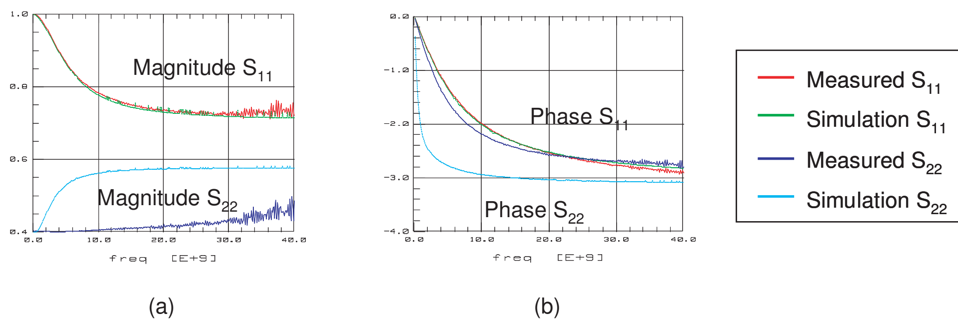


Figure 94: Measured and simulated S-parameter: (a)the magnitude of S11 and S22, (b)the phase of S11 and S22.

3.4 Summary of This Chapter

Five RF CMOS with different layout had been measured and assessed by evaluating the extrinsic components for V_g=0.4V, V_d=1.0V, and device RF characteristic such as the cutoff and maximum oscillation frequencies (f_T and f_{max}) for V_g=1.0V, V_d=1.0V.

Its intrinsic and extrinsic parameters had been extracted. Extracted intrinsic parameters, i.e. DC parameters could be obtained a good fitting at higher gate voltage. Fitting of g_m differentiated i_d and v_g, and g_{ds} differentiated i_d and v_d is important. However, it could not be extracted accurately at lower gate voltage because of BSIM3v3 model limit probably.

Extracted extrinsic paramters such as gate resistance R_g, source resistance R_s, drain resistance R_d, total gate capacitance C_{gg}, gate-to-drain capacitance C_{gd}, gate-to-source capacitance C_{gs}, gate-to-bulk capacitance C_{gb} and substrate resistance R_{sub}, had been compared for each type of devices. We can find that R_g and R_{sub} largely affect these device RF performance as shown in Figure 80. On the other hand, R_d and/or R_s does not have much effect on f_T and f_{max}. Forcused on only f_{max} and substrate network resistance R_{sub}, we can find that the value of f_{max} is in disagreement with the value of R_{sub} and R_g, and R_{sub} of Type C is largest (or f_{max} of Type C is worst). Therefore, we can consider that substrate network resistance R_{sub} largely effect on these devices RF performance for different layout devices. It will be necessary to analyse the substrate network including substrate resistance and capacitance more.

Furthermore, RF modeling had also performed. Although it could not establish a complete sub-circuit model, only input port model had been established. Thus, we must analyse and model the output port effects such as the effects of substrate resistance and capacitance.

In conclusion, we summarize that Type C is the worst layout for RF CMOS due to its substrate resistance and Type D and E are good layout for RF CMOS.

Chapter 4. Characterization of Sub-100 nm High-k RF MOSFET

In this chapter, the leading-edge sub-100 nm High-k RF CMOS will be assessed by evaluating the cutoff and maximum oscillation frequencies (f_T and f_{max}). Up to now, RF performance for High-k RF CMOS have been hardly reported [29]. So we will measure and evaluate for RF CMOS with SiON and HfSiON gate dielectrics.

4.1 Device

4.1.1 Test Device

SiON (ϵ_{SiON} = 6) and HfSiON (ϵ_{HfSiON} = 15) are employed as High-k gate oxide, to make oxide thickness more thick physically. RF CMOS structure is shown in Figure 95, and each MOSFETs with SiON and HfSiON are shown in Figure 96. Test device with SiON is capped SiN to increase mobilty and thermal fastness. Except for this structure, both test devices with SiON and HfSiON are all same structure.

Test devices were fabricated with gate length (L_g) of 90 nm, unit gate width (W_{unit}) of 5 um, number of finger (F) of 12 and equivalent oxide thickness (EOT) is both 1.5 nm. Note that actual gate lentgh is approximately 61～66 nm as shown in Figure 97.

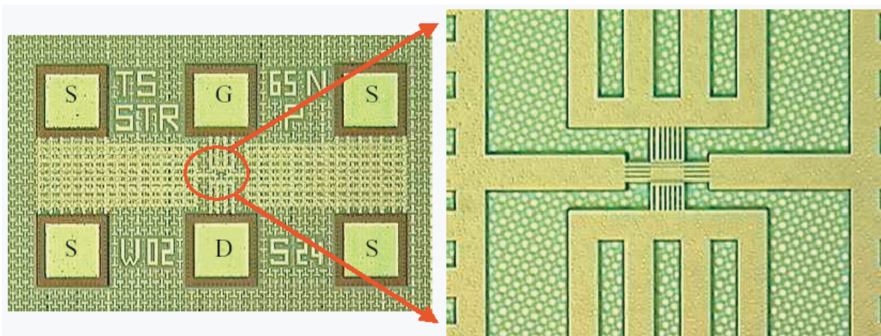


Figure 95: RF CMOS structure

4.1.2 Multi-Finger Straucture for RF MOSFET

As shown in Figure 96., RF MOSFETs are usually laid out as multi-finger devices, because in deep-sub-micrometer CMOS processes the maximum finger length is limited and source/drain

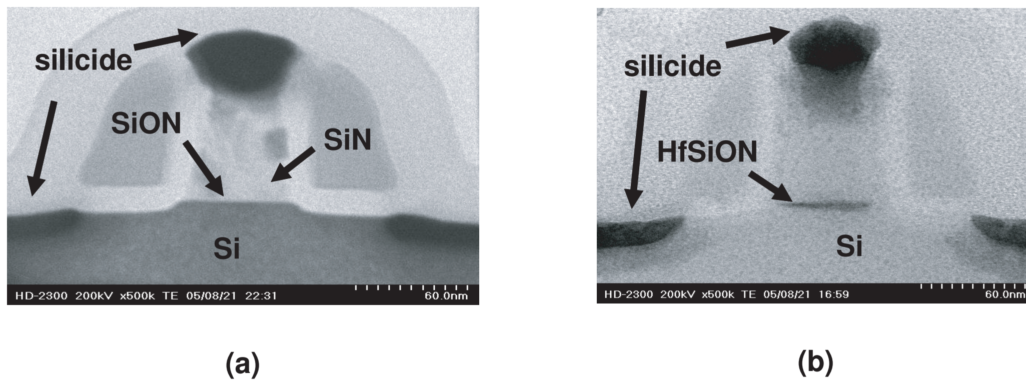


Figure 96: Cross section diagram of test device : (a)SiON and (b)HfSiON

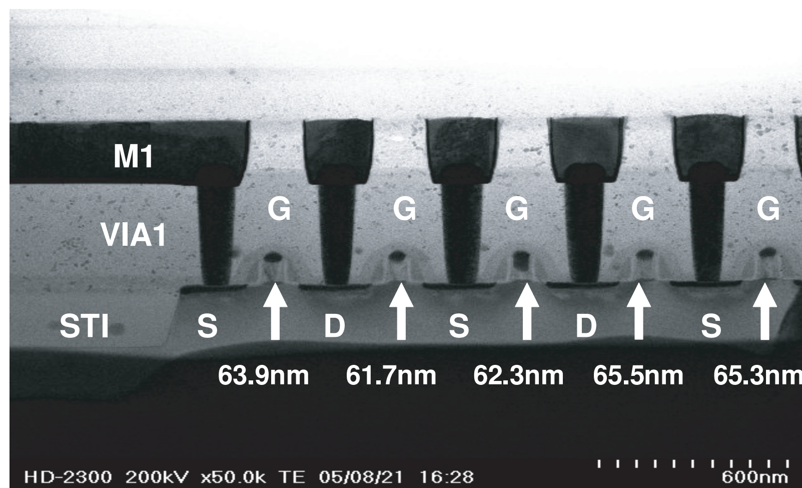


Figure 97: Cross section diagram of test device.

parasitic resistance or gate resistance could reduce. It is clear that if the number of fingers increase, gate resistance could reduce.

$$R_{g,eff} = \frac{1}{3} R_{sh} \frac{W_f}{L N_f} \quad (4–1)$$

$$= \frac{1}{3} R_{sh} \frac{W_{total}}{L N_f^2} \quad (4–2)$$

As the finger width decreases polyside sheet resistance increases due to grain boudary problems. This is the so called narrow line effect. Typical devices have more than 10 fingers, and this test device has 12 fingers. The total transistor effective width W_{eff} is then simply $N_f W_f$.

4.2 Measurement

4.2.1 DC Measurement

DC measurement, I_d-V_g and I_d-V_d for various values of V_{ds} and V_{gs} as shown in Table 4, had performed against each type of devices. Figure 98.and 99. shows the result of DC measurement.

Table 4: DC measurement bias conditions

	Vg	Vd
I_d-V_g	0-1.5V	0.1-1.5V per 0.1V
I_d-V_d	0/0.3/0.6/0.9/1.2/1.5V	0-1.5V

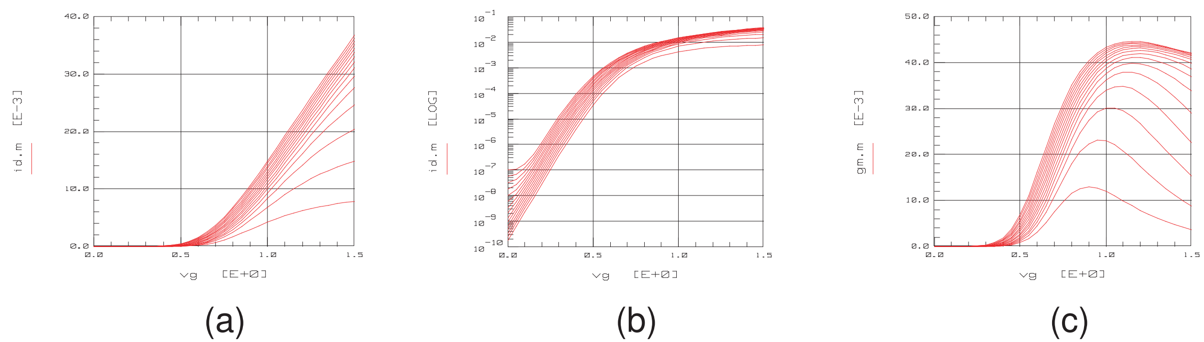


Figure 98: 【SiON】(a)I_d-V_g, (b)$\log_{10}I_d$-V_g, and (c)g_m-V_g for various value of V_g=0-1.5V and V_d=0.1-1.5V

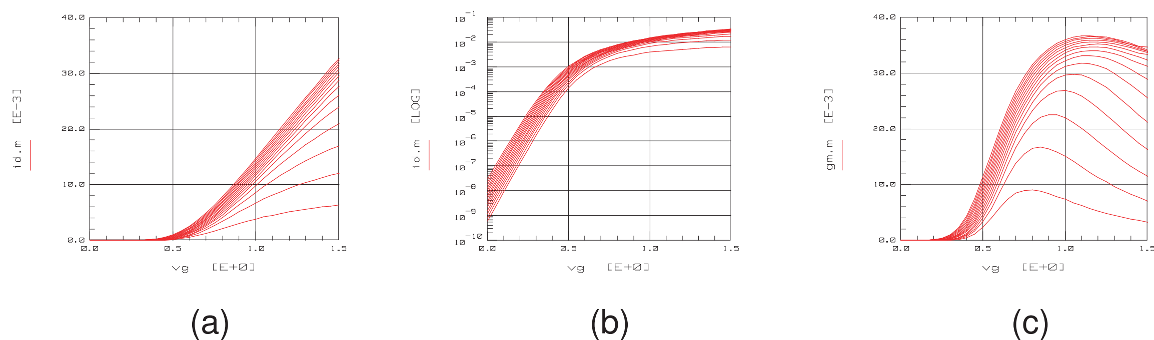


Figure 99: 【HfSiON】(a)I_d-V_g, (b)$\log_{10}I_d$-V_g, and (c)g_m-V_g for various value of V_g=0-1.5V and V_d=0.1-1.5V

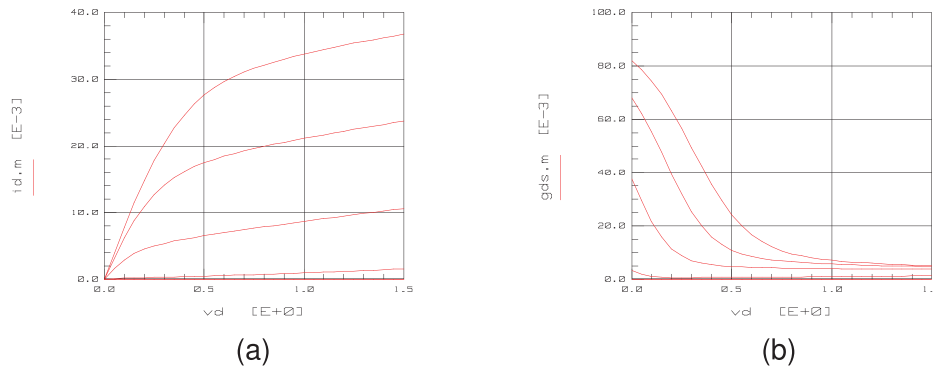


Figure 100: 【SiON】(a)I_d-V_d, and (b)g_{ds}-V_g for various value of V_g=0/0.3/0.6/0.9/1.2/1.5V and V_d=0-1.5V

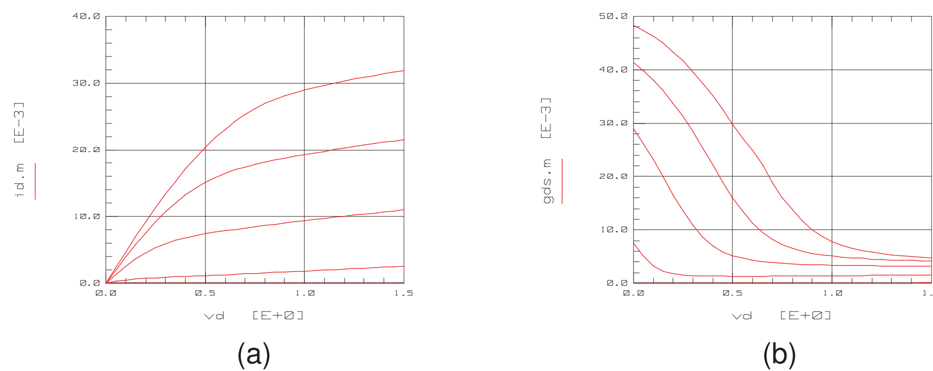


Figure 101: 【HfSiON】(a)I_d-V_d, and (b)g_{ds}-V_g for various value of V_g=0/0.3/0.6/0.9/1.2/1.5V and V_d=0-1.5V

The *punch-through* can be found in Figure 100. and 101. like p-MOS due to short channel effects.

4.2.2 RF Measurement and De-embedding

S-parameter had measured up to 40 GHz. Here, the de-embedding procedure based on the open and short calibration test structures (see Section 2.1.1) was performed for each devices. The effects of de-embedding in S_{11} and S_{22} are shown in Figure 102. and 103. for V_g=1.5V and V_d=1.5V.

After de-embedding, RF performance of intrinsic part of a transistor can be assessed by evaluating the cutoff frequency f_T (see Figure 104. and 106.) and the maximum available gain f_{max}

(see Figure 105. and 107.). Since we measured only up to 40 GHz for V_{ds}=0.6/0.9/1.2/1.5V and V_{gs}=1.5, f_T and f_{max} must be predicted by extrapolating for over 40 GHz as shown in the blue line of Figure 104.- 107. From the result of this prediction, $f_{T,SiON}$≈234.2 GHz, and $f_{T,HfSiON}$≈175.6 GHz could be obtained. As to f_{max}, $f_{max,SiON}$≈61.94 GHz, and $f_{max,HfSiON}$≈69.20 GHz could be obtained. Both maximum f_T and f_{max} could be obtained at V_{ds}=1.2V and V_{gs}=1.5. Figure 108. shows drain current dependent of f_T, f_{max} and transconductance g_m. We can easily find that the relation to f_T, f_{max} and transconductance g_m. As biased $g_{m,peak}$, f_T and f_{max} also increase due to device mobilty.

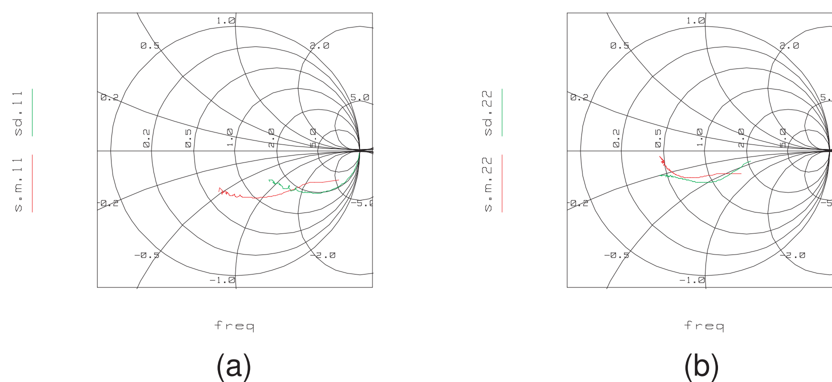


Figure 102: 【SiON】(a)S_{11} and (b)S_{22} comparing the measured raw data(red-line) with after de-embedding data with *OPEN*/*SHORT*(green-line).

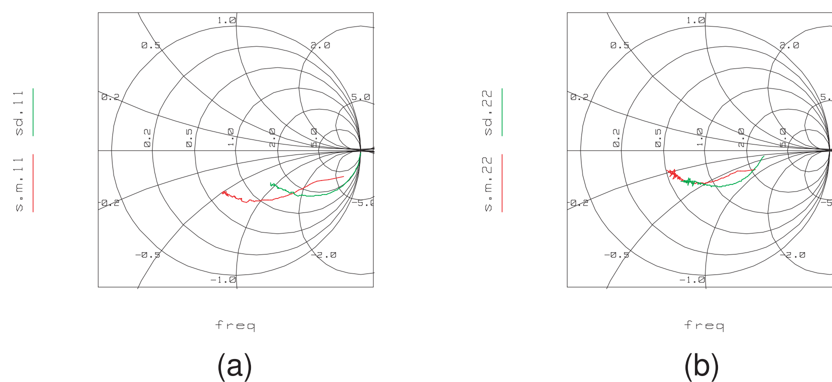


Figure 103: 【HfSiON】(a)S_{11} and (b)S_{22} comparing the measured raw data(red-line) with after de-embedding data with *OPEN*/*SHORT*(green-line).

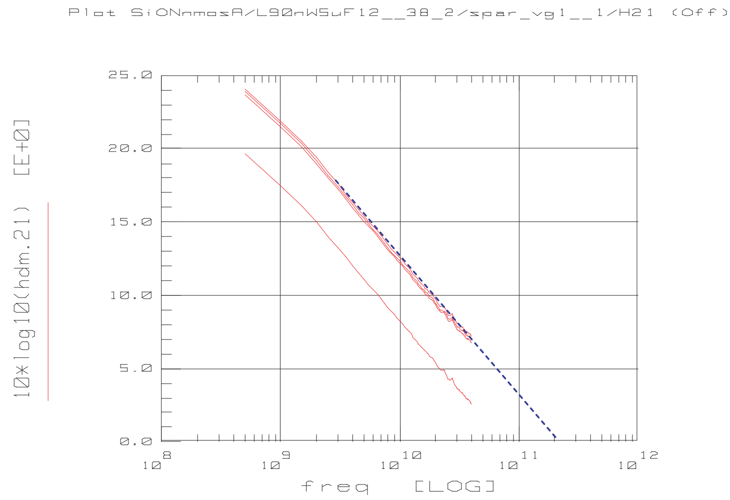


Figure 104: Frequency dependence of the cut-off frequency for CMOS with SiON gate dielectrics.

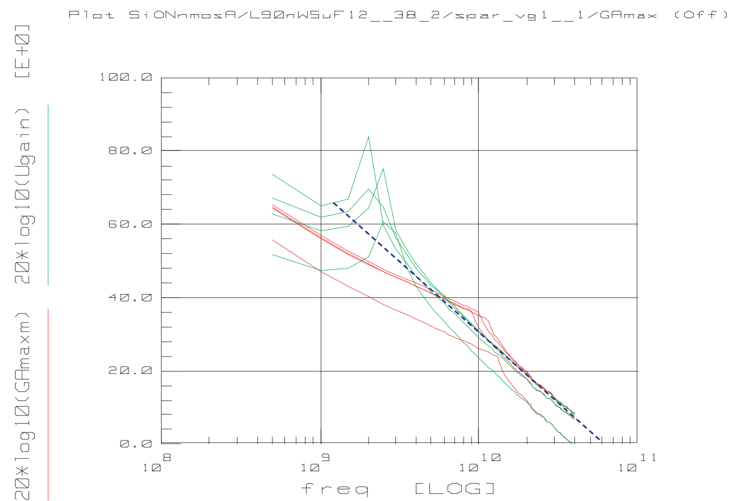


Figure 105: Frequency dependence of the maximum available gain for CMOS with SiON gate dielectrics.

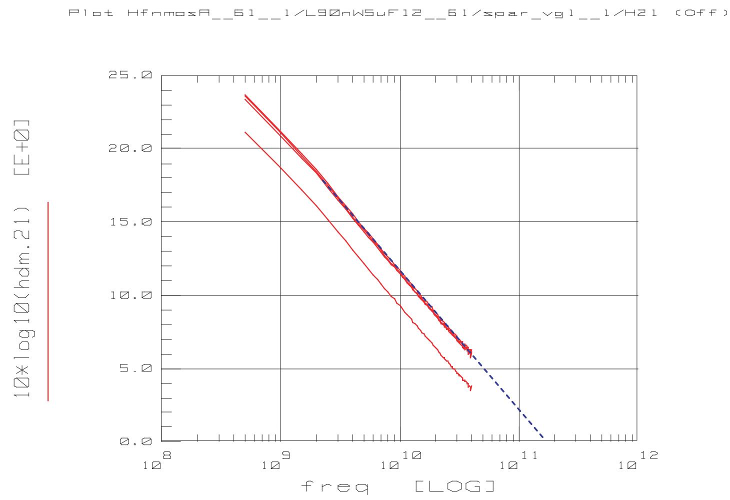


Figure 106: Frequency dependence of the cut-off frequency for CMOS with HfSiON gate dielectrics.

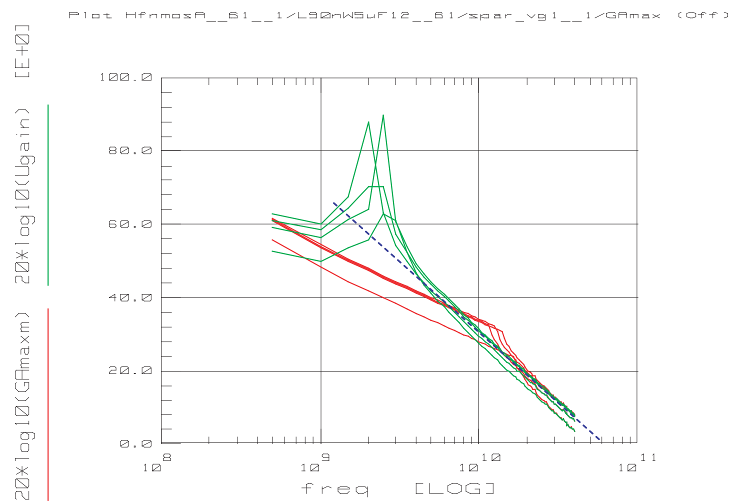


Figure 107: Frequency dependence of the maximum available gain for CMOS with HfSiON gate dielectrics.

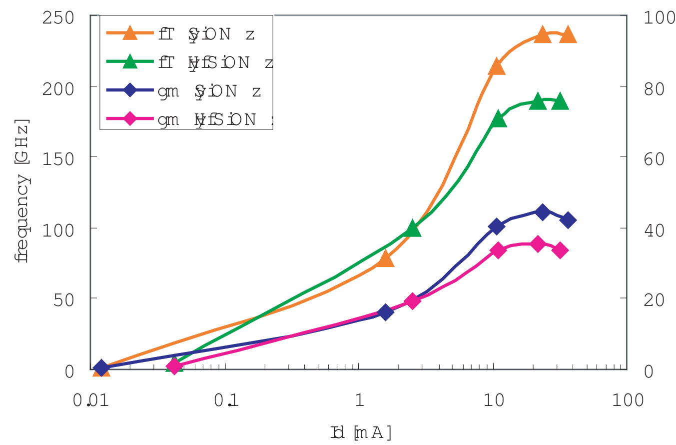


Figure 108: Drain current dependent of f_T, f_{max} and transconductance g_m.

4.2.3 Extrinsic Parameter Extraction

Extrinsic parameters such as R_g, C_{gg} and R_{sub}, etc., had been extracted and applied to evaluate its RF performance. The methodologies of extraction are shown in section 2.3.

4.2.3.1 Gate Resistance Extraction

Each gate resistance R_g had extracted as shown in Figure 109. We can find that R_g of SiON is larger than R_g of HfSiON and, as frequency increase, R_g also increase simultaneously because of NQS effects.

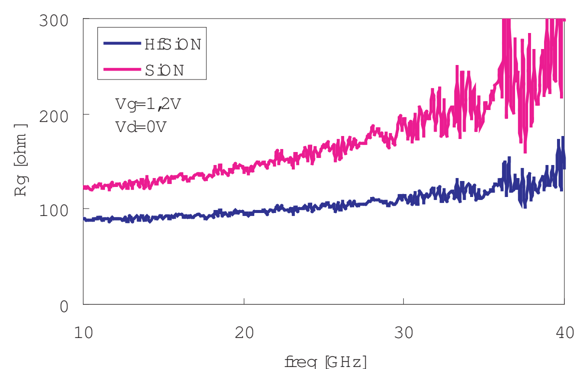


Figure 109: Frequency dependency of extracted gate resistance [V_{ds}=0V]

4.2.3.2 Gate Capacitance Extraction

Gate capacitance had also extracted by Eq.(2-111)-(2-114). C_{gg} is total gate capacitance, that is $C_{gg}=C_{gd}+C_{gs}+C_{gb}$. Each gate capacitance such as C_{gg}, $C_{gd}+C_{gs}$, and C_{gb}, are compared with in Figure 110. and 111. We can find that although as frequency increase, every gate capacitances also increase, all gate capacitance of HfSiON are larger than of SiON. It can consider that these capacitances also affect RF MOSFET with HfSiON performance badly. Especially, with comparing $C_{gs}+C_{gd}$ to C_{gb} in Figure 111., it can be found that C_{gs} and C_{gd} mainly effect.

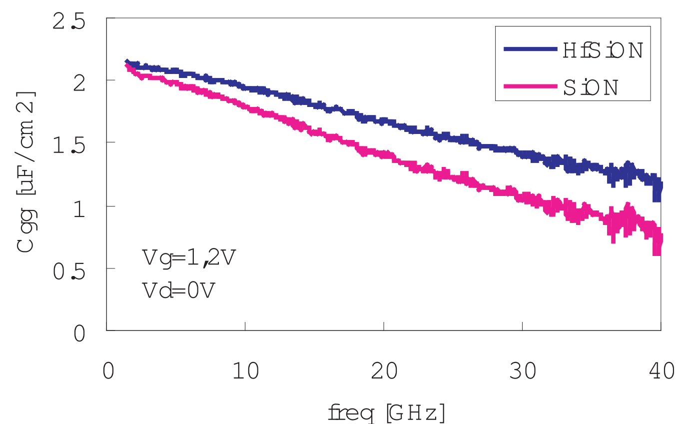


Figure 110: Frequency dependency of extracted C_{gg}.

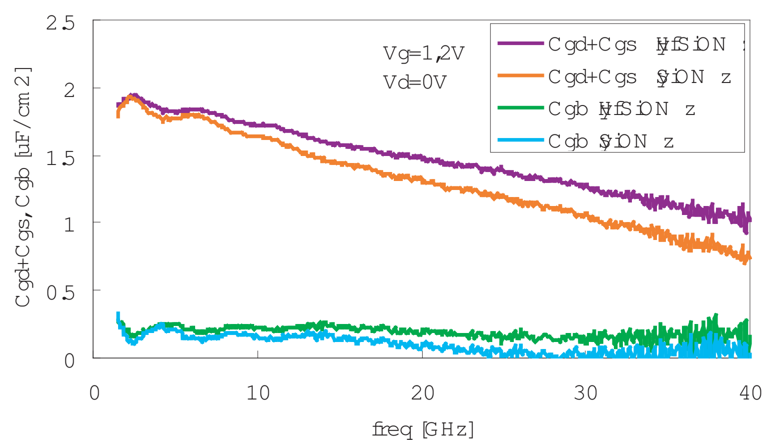


Figure 111: Frequency dependency of extracted $C_{gd}+C_{gs}$ and C_{gb}.

4.2.3.3 Substrate Network Analysis

There is little difference between R_{sub} of HfSiON and of SiON. It can consider that R_{sub} makes little difference to each device RF performance as shown in Figure 112.

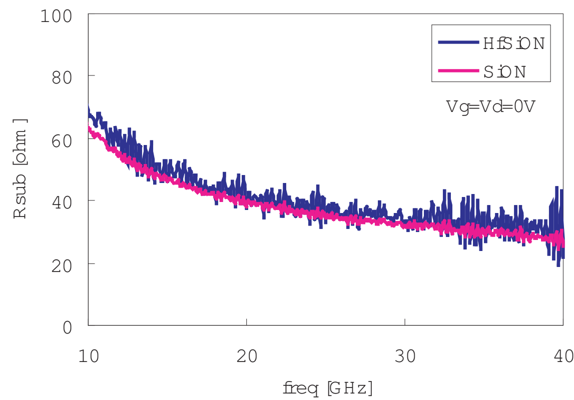


Figure 112: Frequency dependency of extracted substrate resistance [V_{gs}=V_{ds}=0V]

4.3 Summary of This Chapter

In this chapter, sub-100 nm High-k RF MOSFET with SiON and HfSiON gate dielectrics had been measured and assessed by evaluating the cutoff and maximum oscillation frequencies (f_T and f_{max}). Both devices show considerably high RF performance as shown in Figure 113. and 114. Compared the obtained values of f_T and f_{max} to the values in Figure 113. and 114., we can find that the obtained values of f_T are considerable good values over the last 10 years. However, as to f_{max}, its value is not so reasonable.

Furthermore, extrinsic parameters also had extracted and made a comparison. RF performance of test devices such as f_T and f_{max}, and extrinsic resistances such as R_g and R_{sub}, are compared with in Figure 115. We can find that the value of f_{max} is in disagreement with gate resisitance R_g. As each values of substrate network resistance R_{sub} are almost same, it can consider that R_{sub} hardly make RF performance different. This means that gate resistance R_g largely make device RF performance worse, not substrate network resistance R_{sub} in these devices. Therefore, gate resisntance R_g must be reduced for more higher RF performence.

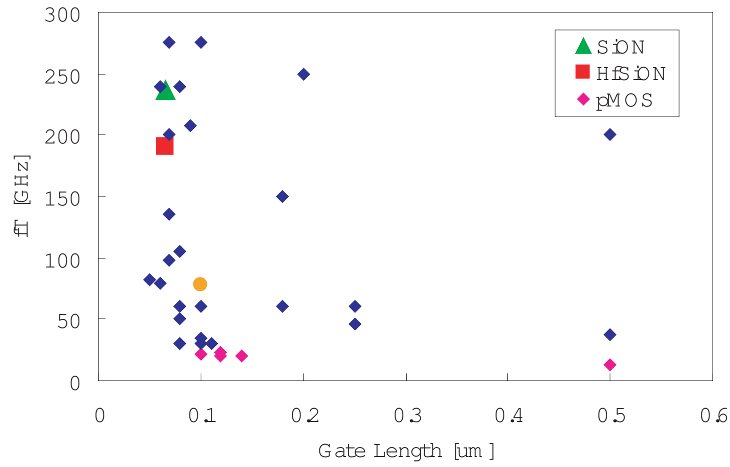


Figure 113: Reported values of f_T in IEDM and VLSI, 1995-2004.

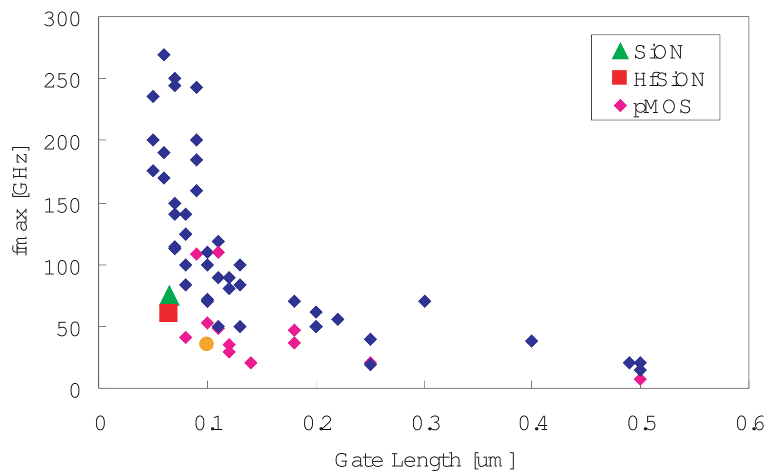


Figure 114: Reported values of f_{max} in IEDM and VLSI, 1995-2004.

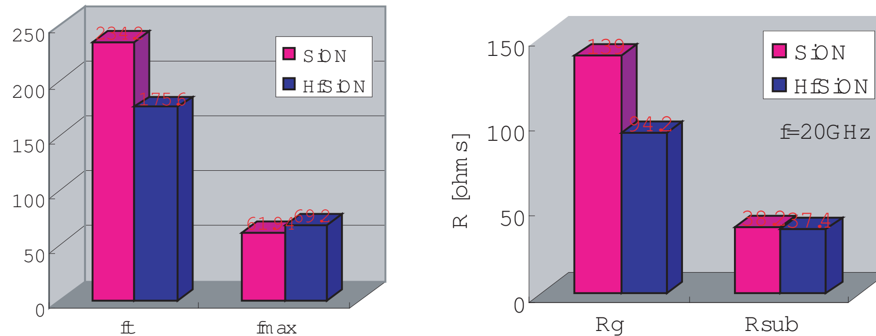


Figure 115: RF performance and extrinsic resistances, R_g and R_{sub}.

Extrinsic capacitances such as total gate capacitance C_{gg}, gate-to-drain/gate-to-source capacitance C_{gd}+C_{gs} and gate-to-bulk capacitance C_{gb}, are shown in Figure 116., comparing with f_T and f_{max}. We can find that each gate capacitances of HfSiON are larger than of SiON. So we can consider that these capacitances badly affect RF MOSFET with HfSiON performance, such as f_T and f_{max}. Especially, gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd} mainly affect as shown in Figure 111. To reduce these effects, the structure of source and drain should be changed, for example asymmetry source/drain structure.

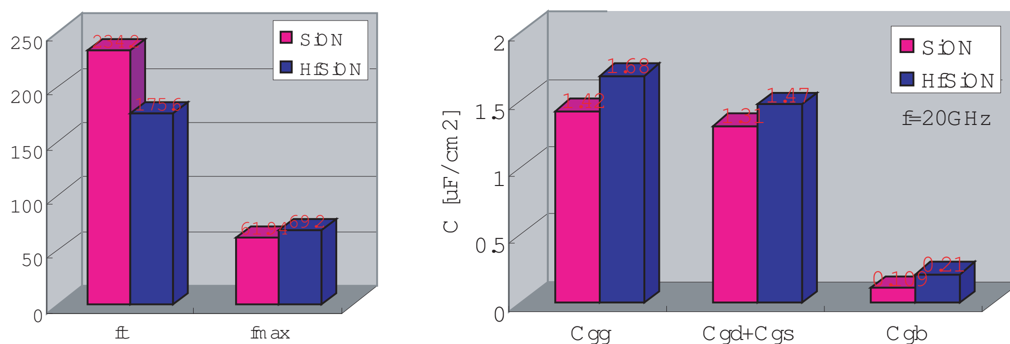


Figure 116: RF performance and extrinsic capacitances, C_{gg}, C_{gd}+C_{gs} and C_{gb}.

Chapter 5. Conclusions and Future Issues

5.1 Conclusions

5.1.1 Modeling of RF MOSFET with Different layout

Five RF CMOS with different layout had been measured and assessed by evaluating the cutoff and maximum oscillation frequencies (f_T and f_{max}). And intrinsic and extrinsic parameters had been extracted. At higher frequency, since device operation are influenced by some parasitic components, extrinsic parameter extraction and evaluation are really meaningful for verfying RF effects and had been done. Especially, it could be found that gate resistance and substrate resistance make device RF performance worse significantly. In conclusion, a transistor surrounding guard ring such as Type D and E is well to reduce the substrate network resistance, and the parallel aligned transistor such as Type C is the worst layout for RF application. However, the substrate resistance effects may be much more complex, so it will be necessary to analyse the substrate network even more.

Furthermore, RF modeling had also performed. Although it could not establish a complete sub-circuit model, only input port model had been established. Thus, we must analyse and model the output port effects such as the effects of substrate resistance and capacitance.

5.1.2 Characterization of sub-100nm High-k RF MOSFET

Sub-100 nm High-k RF MOSFET with SiON and HfSiON gate dielectrics had been also measured and assessed by evaluating the cutoff and maximum oscillation frequencies (f_T and f_{max}). The cutoff frequencies f_T of both devices show considerably high RF performance over the last 10 years, as shown in Figure 113. and 114. However, as to f_{max}, its value is not so reasonable due to gate resistance effects. We must reduce the gate resistance to obtain higher maximum available gain, i.e. maximum oscillation frequencies f_{max}.

Another factors of interrupting to obtain higher RF performance are the parasitic capasitances, such as gate-to-drain C_{gd}, gate-to-source capacitance C_{gs}, (and gate-to-bulk capacitance C_{gb},) must be reduce to change structure, for example asymmetry source/drain structure.

5.2 Future Issues

As discussed in chapter 2. actively, an accurate compact RF model are required. However, as accurate modeling still has many problem such as g_{ds} (chapter 3), extrinsic parameter extraction model for gate resistance, gate capacitance, etc., it must be improved to obtain stable and accurate values at RF.

As we could make sure that gate resistance really affects to device RF performance, reducing gate resisntance will make RF CMOS much higher RF performance.

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