Master Thesis

Formation of Heat Resistant Ni Silicide Using Metal Additive for Nanoscale CMOS

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LIST OF CONTENT

Chapter 1

INTRODUCTION………………………………… …….1

1. Background…………………………………………….2

1.1 Low-Resistivity Materials

for Nanoscale CMOS……………………………………...5

1.2 Transition of Silicide Technology ……………………..…6

1.3 Comparison of Silicide Materials………………………7

1.4 Purpose of This Study…………………………………..…11

Chapter 2

FABRICATION AND MEASUREMENTS……….42

2. Flow of Experiments……………………………………43

2.1 Si Substrate Cleaning Process………………………43

2.2 UHV Sputtering System……………………………..……44

2.3 Infrared Annealing Furnace……………………………47

2.4 Four-point Probe Technique………………………… 49

2.5 Atomic Force Microscopy (AFM)..........................50

2.6 X-ray Diffraction (XRD) 51

2.7 Rutherford Back scattering Spectroscopy (RBS).....52

2.8 Auger Electron Spectroscopy...............................53

2.9 Raman Spectroscopy 53

Chapter 3

EXPRIMENT RESULTS.....................................55

3.1 Study of Experimental Conditions........................56

3.1.1 Thin Film Deposition Conditions...........................56

3.1.1.1 Pre-Sputtering Time...56

3.1.1.2 Gas Pressure during Deposition..........................60

3.1.2 Remodeling of Annealing Furnace.......................63

3. 2 Experimental Results..72

3.2.1 Conventional bi-layer Deposition.........................73

3.2.1.1 Thermal Stability of Pure Ni Silicide..................74

3.2.1.2 Thermal Stability of Ni silicide

with the Existence of Metal additives..................82

3.2.2 Post-Silicidation Doping 83

Chapter 4

CONCLUSIONS..86

4.1 Results of This Study..87

4.2 Future Issues..88

Acknowledgements.. 89

References 91

Chapter 1

INTRODUCTION

1 Background

About half a century ago, Shockley, Bardeen and Brattain invented the first transistor. Since then, the semiconductor technologies advanced rapidly. After the invention of the integrated circuit, the number of transistors included in a chip increased according to Moore's law.

CMOS (Complementary Metal Oxide Semiconductor) technology evolution in the past years has followed the path of device scaling for achieving density, speed, and power improvements. MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) scaling was propelled by the rapid advancement of lighographic techniques for delineating fine lines of 1 μm width and below.

In constant-field scaling, it was proposed that one can keep short-channel effects under control by scaling down the vertical dimensions (gate insulator thickness, junction depth, etc.) along with the horizontal dimensions, while also proportionally decreasing the applied voltages and increasing the substrate doping concentration (decreasing the depletion width). This is shown schematically in Fig. 1-1. The principle of constant-field scaling lies in scaling the device voltages and the device dimensions (both horizontal and vertical) by the same factor, $\kappa(>1)$, so that the electric field remains unchanged. This assures that the reliability of the scaled device is not worse than that of the original device.

Table 1-1 shows the scaling rules for various device parameters and circuit performance factors. The doping concentration must be increased by the scaling factor κ in order to keep Poisson's equation invariant with respect to scaling.

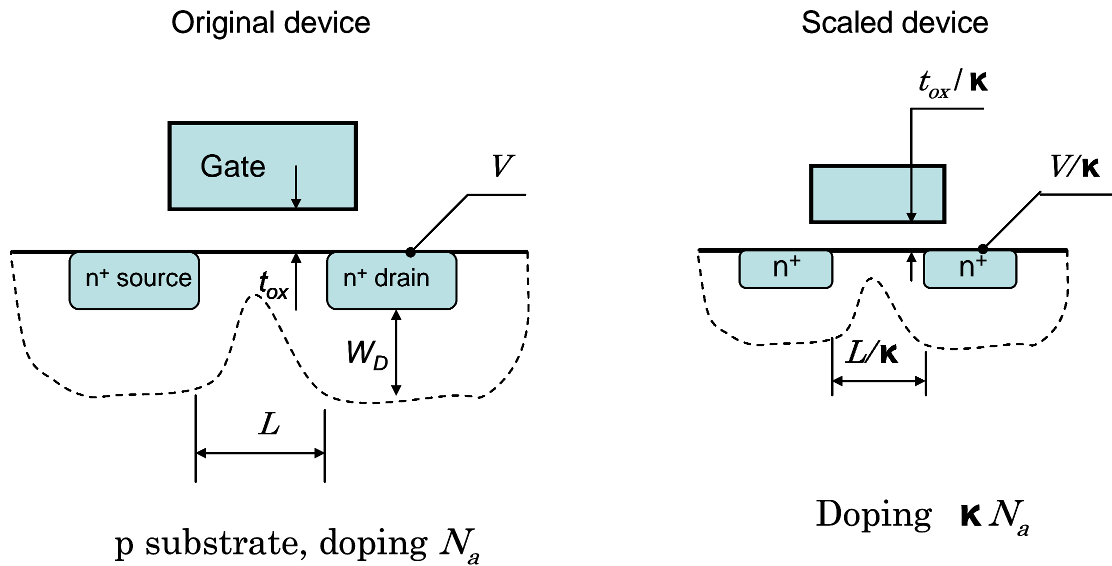


Fig. 1-1 priciples of MOSFET constant-electric-field scaling

Table 1-1 Scaling of MOSFET Device and Circuit Parameters

	MOSFET Device and Circuit Parameters	Multiplicative acor (κ>1)
Scaling assumptions	Device dimensions(t_{ox}, L, W, χ_j)	1/κ
	Doping concentration (N_a, N_d)	κ
	Voltage (V)	1/κ
Derived scaling behavior fo device parameters	Elecric field (ξ)	1
	Carrier velocity (υ)	1
	Depletion –layer width (W_d)	1/κ
	Capacitance ($C=\varepsilon A/t$)	1/κ
	Inversion-layer charge density (Qi)	1
	Current, drift (I)	1/κ
	Channel resistance (R_{ch})	1
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	1/κ
	Power dissipation per circuit ($P \sim VI$)	$1/\kappa^2$
	Power-delay product per circuit ($P\tau$)	$1/\kappa^3$
	Circuit density (∞ $1/A$)	κ^2
	Power density (P/A)	1

The gate length of MOSFET came to be lower than 100nm since the year of 2000 and 32nm for the year of 2005 as shown in Fig. 1-2 according to the ITRS roadmap 2004 update [1]. With continuous scaling of device dimensions, IC performance is becoming more and more dependent upon the parasitic series resistance of the source/drain junctions and their contacts.

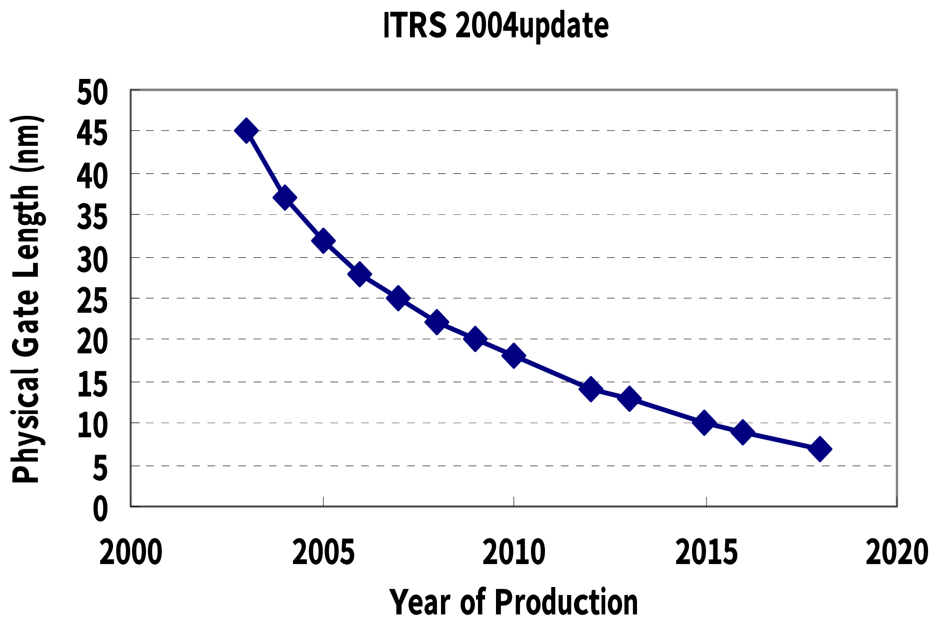


Fig.1- 2 the International Technology Roadmap for Semiconductors (2004 update)

1.1 Low-Resistivity Materials for Nanoscale CMOS

The primary thrust of very large scale integration (VLSI) has resulted in devices that are smaller and faster and that consume less power. The continued evolution of smaller and smaller devices has aroused a renewed interest in the development of new metallization schemes for low-resistivity gates, interconnections, and ohmic contacts. This is interest in new metallization arose because as the device sizes are scaled down, the linewidth gets narrower and the sheet resistance contribution to the RC delay increases.

The conventional polysilicon whose sheet resistance is about 30 to 60 Ω/sq, is too high to be applied to modern VLSI. Aluminum, tungsten, and molybdenum are notable among the metals proposed for gate and interconnect metallization. The use of aluminum, however, requires all postgate processing of the devices to be limited to very low temperatures, preferably below 500°C. The use of the refractory metals tungsten and molybdenum requires complete passivation of these metals from oxidizing ambients, deposition by means that will not lead to unwanted traps in the gate oxide, and reliable etching of the metals for pattern generation. The uncertainties associated with the stability of these metal films have led to search for alternatives.

The silicides have attracted attention because of their low and metal-like resistivities and their high temperature stability. The use of silicides, with resistivity about one-tenth of the polysilicon, have greatly improved the speed of the circuits.

Scaling down the size of the device also means reduced junction depths, which can lead to contact problems. In particular, shallow junctions limit the use of aluminum due to its known penetration in silicon. Forming silicides in the contact windows by reaction between the silicon substrate and a thin metal layer offers a possibility of forming contacts with lower contanct resistances.

1.2 Transition of Silicide Technology

Silicide was first introduced to LSI devices as a polycide (stacked silicide /poly Si gate electrode) as shown in Fig. 1-3. $MoSi_2$ polycide word line in 256 K DRAM in early 1980s was one of the first applications of polycide to LSI production. Then, WSi_2 polycide was popularly used for the gate electrode of logic LSIs from the middle of the 1980s because the sheet resistance of WSi_2 is smaller than that of $MoSi_2$. Salicide was popularly introduced into mass production using $TiSi_2$ in the early 1990s. $TiSi_2$ was selected as the material for salicide, because the sheet resistance is further smaller than WSi_2. However, $TiSi_2$ was eventually found to be a relatively difficult material to treat depending on thermal process. For example, sheet resistance of $TiSi_2$ often increases by the agglomeration of the silicide film during high temperature thermal process of the CMOS fabrication. Thus, $TiSi_2$ has been eventually replaced by $CoSi_2$ from the late 1990s making the process more suitable towards deep-sub micron CMOS [3]. In December 1991, NiSi-salicide was proposed for the first time with the demonstration of nice characteristics of a 0.4-mm NiSi salicided CMOS [2]. Moreover, NiSi is lower

resistance and consumes less Si than that of $CoSi_2$. Now NiSi is considered to be a promising silicide material for nanoscale CMOS. The progress of silicide technologies summarized as Fig. 1-3[3].

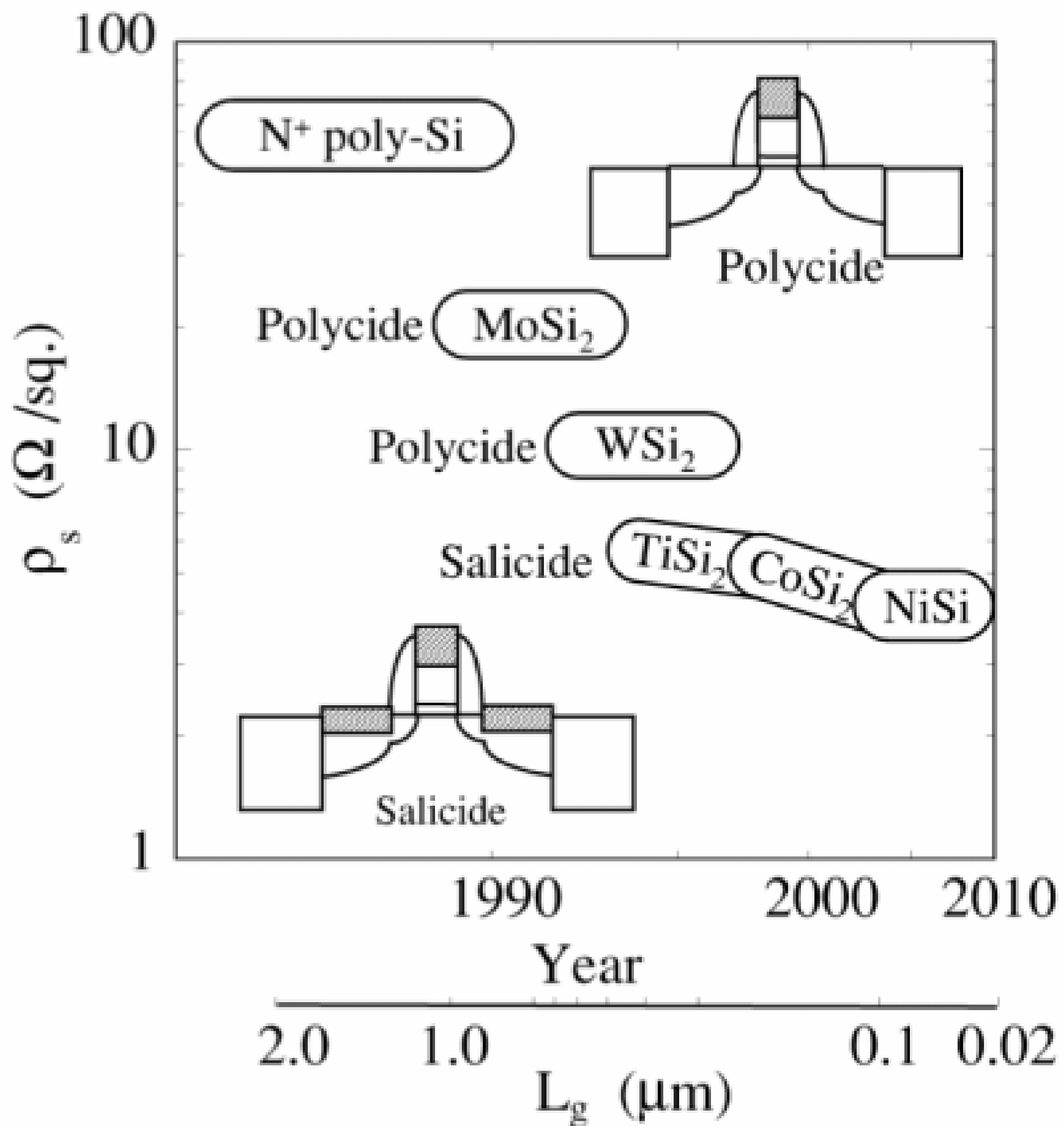


Fig. 1-3 Progress of silicate materials

1.3 Comparison of Silicate Materials

The main driver for the continuous advancement in VLSI has been the search for electronic circuits of higher performance and lower cost. In

particular, the speed of an electronic circuit is one of the major concerns. For this purpose of reaching higher speed, metal silicates have been utilized for contact metallization and local wiring. The choice of metal silicates in LSIs technology is quite natural, because they meet the basic requirements: low specific resistively, low contact resistively to both types of LSIs, high thermal stability, and excellent process compatibility with standard Si technology. Today, metal silicides are an inseparable part of an electronic device. Here are some comparisons about silicide materials. Fig. 1-4 shows the dependence of sheet resistance on line width for various silicide materials. Ni silicide possesses not only the lowest sheet resistance but also the best width independence among $TiSi_2$(Conventional process), $TiSi_2$(Pre-amorphization) and $CoSi_2$ as well.

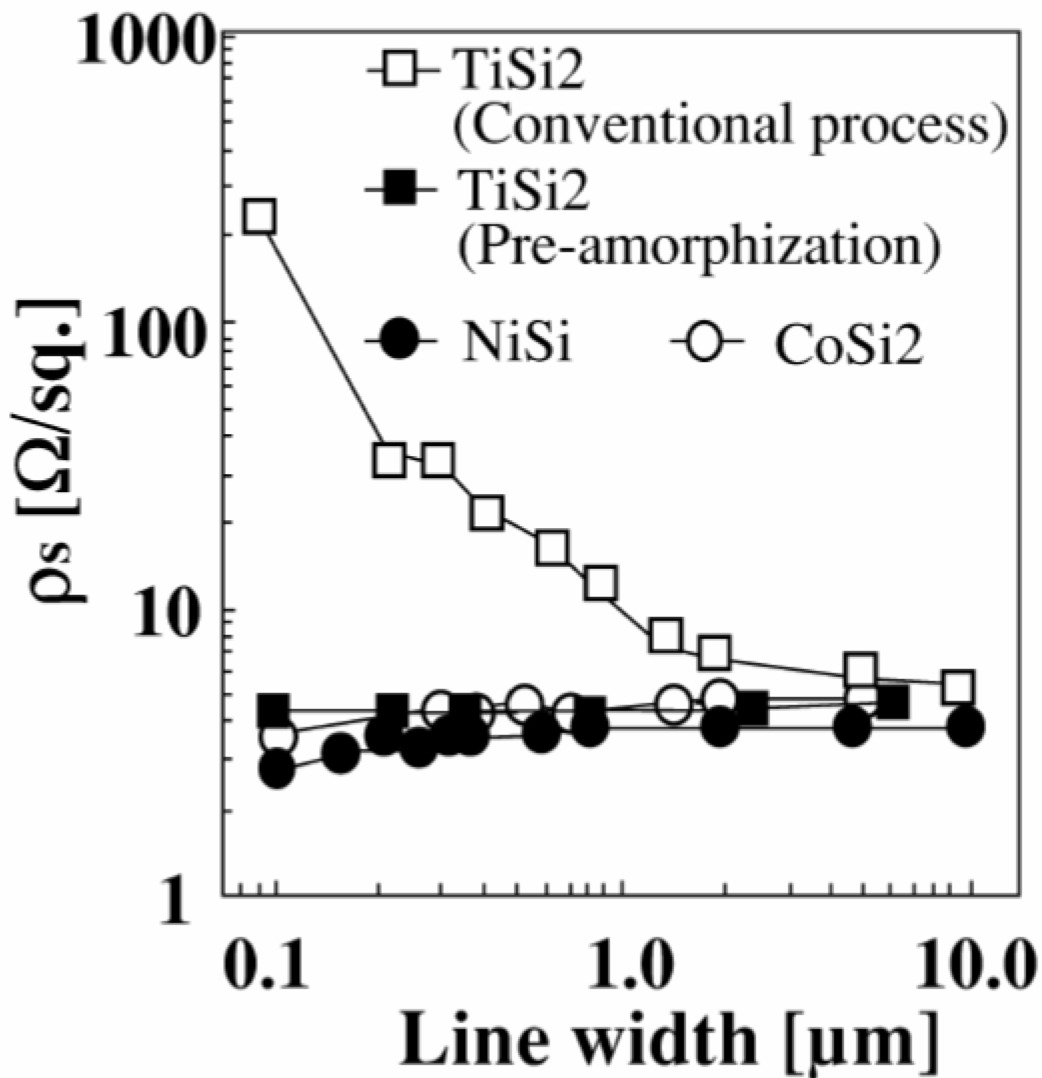


Fig. 1-4 Dependence of sheet resistance on line width for various silicide materials

Ni silicide shows the lowest sheet resistance also can be confirmed from table 1-2. However, at higher temperature or more than 700°C, Ni silicide begins to transform to $NiSi_2$ whose resistivity is 2 or 3 times as high as that of NiSi. In other words, Ni silicide is poor at thermal stability. Table 1-3 indicates some physical properties of Ti, Co, Ni silicide

Table 1-2 Parameters for Silicide Processing Using Ti, Co, or Ni[4]

Silicide	T_f (°C)	ρ (μΩcm)	Φ_{Bn} (eV)[d)]	DDS[e)]
C49 $TiSi_2$	350-700[a)]	60-80	?	Si
C54 $TiSi_2$	750[b)]	15-20	0.60	Si
Co_2Si	350	110	?	Co
CoSi	375	147	0.68	Si
$CoSi_2$	500	15-20	0.64	Co
NiSi	250-400	10.5-15	0.65	Ni
$NiSi_2$	700-800[c)]	34	0.66	Ni

a) Upper limit depending on thickness, feature size and doping level.
b) Depending on thickness, feature size and doping level.
c) When formed from NiSi through a nucleation controlled process.
d) Φ_{Bn}: Schottky barrier height to n-type Si.
e) DDS – Dominant diffusion species during formation.

Metal	Temperature 1st RTP (°C)	Phase to form after 1st RTP	Wet selective etching	Temperature 2nd RTP (°C)	Phase to form after 2nd RTP
Ti	650-730	C49 $TiSi_2$	H_2SO_4:H_2O_2 + NH_4OH:H_2O_2:H_2O	>850	C54 $TiSi_2$
Co	400-600	CoSi	H_2SO_4:H_2O_2	>700	$CoSi_2$
Ni	400-550	NiSi	H_2SO_4:H_2O_2	-	-

Table 1-3 Some Physical Properties of Ti, Co, Ni Silicides

Metal	Silicide phase	Crystal structure	T_m (K)	Lattice constant (Å)		
				A	b	c
Ti	Ti_3Si	Tetragonal	1440	10.196	-	5.097
	Ti_5Si_3	Hexagonal	2400	7.429	-	5.139
	Ti_5Si_4	Tetragonal	2190	6.702	-	12.174
	TiSi	Orthorhombic	1840	3.618	6.492	4.973
	C49 $TiSi_2$[a)]	Base-centered orthorhombic	?	3.562	13.531	3.550
	C54 $TiSi_2$	Face-centered orthorhombic	1750	8.2687	8.5534	4.7983
Co	Co_3Si	Hexagonal	1480	4.976	-	4.069
	Co_2Si	Orthorhombic	1600	4.918	3.738	7.109
	CoSi	Cubic	1700	4.4443	-	-
	$CoSi_2$	Cubic	1600	5.365	-	-
Ni	Ni_3Si	Cubic	1440	3.504	-	-
	Ni_2Si	Orthorhombic	1580	5.00	3.73	7.04
	NiSi	Cubic	?	4.446	-	-
	NiSi	Orthorhombic	1265	5.18	3.34	5.62
	$NiSi_2$	Cubic	1298	5.406	-	-
Si	Si	Cubic	1683	5.4306	-	-

1.4 Purpose of This Study

As mentioned in 1.3, the thermal stability of Ni silicide is very poor. Compared with other silicide materials as shown in Fig. 1-5, Ni silicide is so sensitive to heat that its degradation temperature is only 500-600°C. Ni silicide forms at about 300°C and turns to be a high resistance material called $NiSi_2$ at the temperature of about 700 °C. During the high temperature heat process, agglomeration occurs at the surface of Ni silicide film. This fact results in high resistance. In a word, the phase transition and agglomeration lead to high resistance of Ni silicide.

To apply Ni silicide to the practice of downscale CMOS, the drawback of Ni silicide should be overcome. To improve the heat stability of Ni silicide, lots of additives have been conducted during the process of fabrication of Ni silicide films as shown in Table 1-6. Table 1-4 is a Periodic Table of the

Elements. Here, the marked elements were reported as additives to Ni silicide[6-29]. However, the reported data were so much scattered depending on the experimental conditions and no common knowledge for the NiSi stability has been established yet as shown in Table 1-5. The purpose of this study is to examine and compare the NiSi thermal stability with 7 additive metals (Hf, Pd, Pt, Ru, Ta, Ti and V), accurately and fairly in the same conditions expected for the 45 nm node, with accurate and minute temperature measurements.

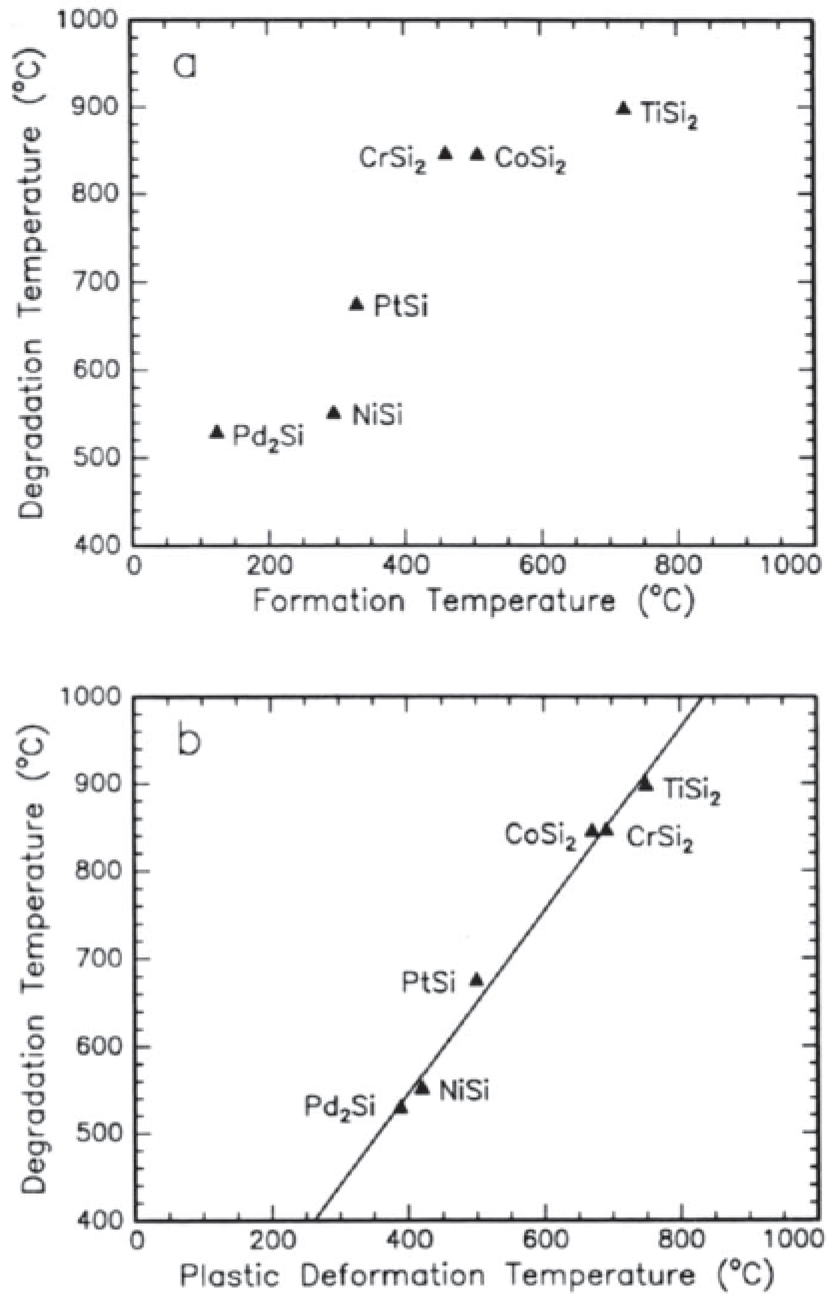


Fig. 1-5 Silicide degradation temperature vs.(a) silicide formation temperature and (b) deformation temperature for six silicides[5]

Table 1-4 a Periodic Table of the Elements

H																	He
Li 179 10.7 11.8	Be 1287 30.3 18											B	**C 4100**	N	O	F	Ne
Na 881 21.2 23	Mg 650 23.8 25			**(mark)**	mark for using as additive to Ni silicide to improve its thermal stability							Al 660 37.4 40	Si 1420 9.6	P	S	Cl	Ar
K 636.2 14.7 15.9	Ca 839 27 23.5	Sc 1539 1.5	**Ti 1667 1.8 1.2**	V 1915 0.5	Cr 1857 7.5 6.5	Mn 1244 0.6	Fe 1535 9.9 11.2	**Co 1495 15.7 16**	**Ni 1455 14.5 16**	Cu 1083 59 64.5	Zn 419.5 16.8 18.1	Ga 29.7	**Ge 945**	As 816	Se 220 8.3	Br	Kr
Rb 39 8.2	Sr 768 4.4	Y 1520 1.8	**Zr 1857 2.2**	Nb 2468 6.2	**Mo 2620 17.5**	Tc 2140	Ru 2282 13	Rh 1966 21.2	**Pd 1552 9.2**	Ag 961 61.4 66.7	Cd 321 13.7 15	In 156.6 11.3	Sn 232 7.9 10	Sb 630.7 2.4	Te 449.8	I	Xe
Cs 28.5 5	Ba 990 2 1.7	*	Hf 2231 3.1	**Ta 2980 7.4**	W 3380 18.5	Re 3100 5.3	Os 3045 11.4	**Ir 2443 19.6**	**Pt 1769 9.4**	**Au 1064 45.5 49**	Hg -39 1	Tl 303.5 6	Pb 327 4.8 5.2	Bi 271.4 0.9 1	Po 255	At	Rn
Fr [?]	Ra 700																
La 918	Ce 804	Pr 935	Nd 1024	Pm 1168	Sm 1072	Eu 822	Gd 1312	Tb 1356	Dy 1407	Ho 1461	Er 1529	Tm 1545	Yb 824	Lu 1663			
Ac 1050	Th 1750	Pa 1575	U 1132	Np 640	Pu 640	Am 850	Cm [?]	Bk [?]	Cf [?]	Es [?]	Fm [?]	Md [?]	No [?]	Lr [?]			

Note:

Ti	element name
1667	Melting point
1.8	Electrical conductivity [$\times 10^6$S/m]@20°C
1.2	Electrical conductivity [$\times 10^6$S/m]@ 0°C

Table 1-5 Scatter among literatures
(Investigated by Associate Professor Kazuo Tsutsui)

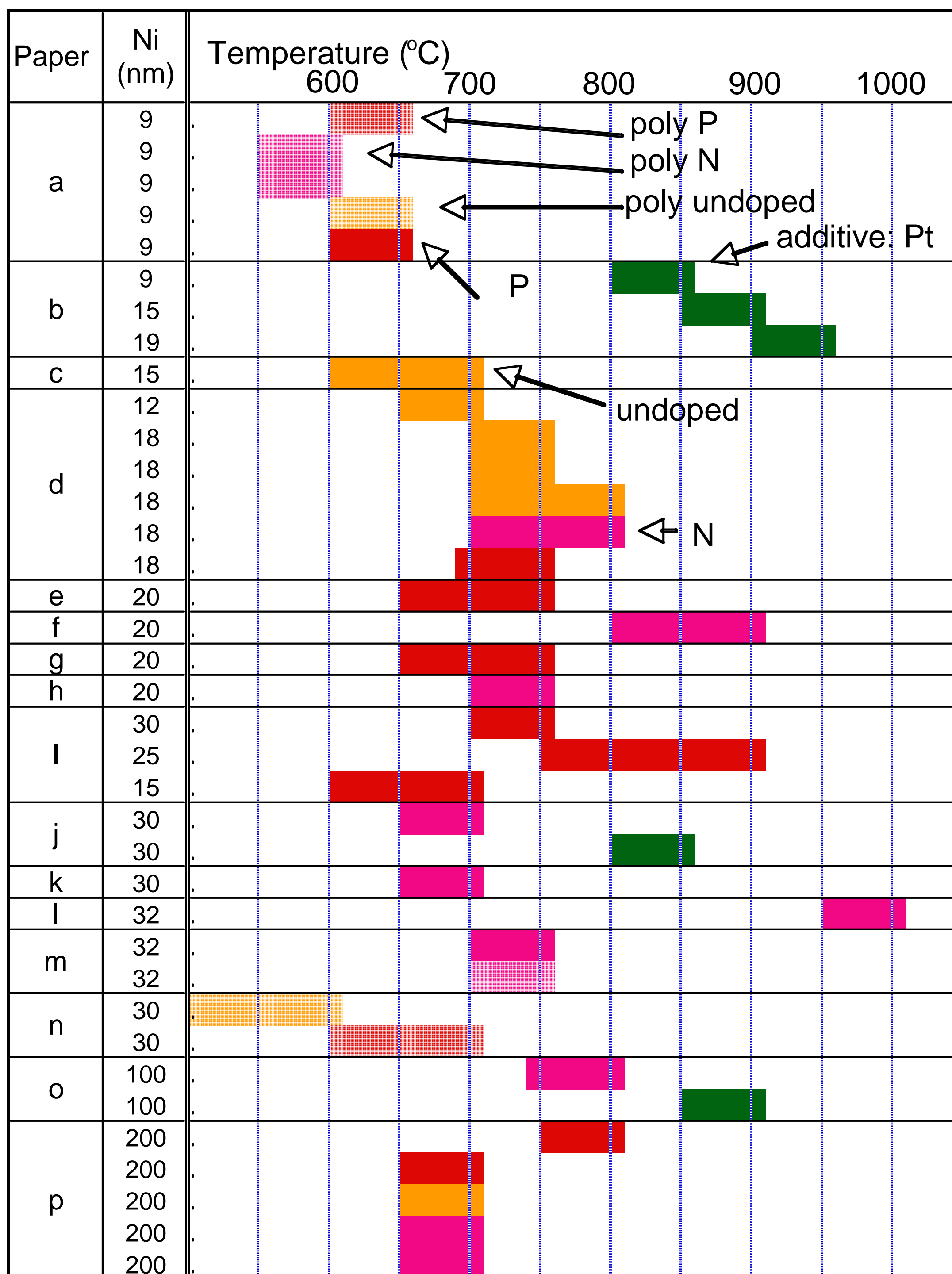


Table 1-6 investigation of literatures concerning Ni silicide

(Investigated by Tokyo Institute of Technology Yoichi Kobayashi, Ruifei Xiang, Koji Nagahiro, Kazuo Tsutsui)

No.	Title	Author	Affiliation	Journal	Comments	effectiveness	Additive
1	Interfacial reaction and electrical properties in Ni/Si and Ni/Si Ge (C) contacts	Shigeaki Zaima,Osamu Nakatsuka, Akira Sakai,Yukio Yasuda		Applied Surface Science, xxx (2003) xxx_xxx	The temperature where NiSi transited to NiSi2 increased when Ge was added to Ni/Si system. The addition of C can keep sheet resistance at low level even at high annealing temperature because its addition makes NiSi difficult to agglomerate.	Yes	Ge
2	Effect of interlayer on thermal stability of nickel silicide	Jer-shen Maa, Yoshi Ono, Douglas J. Tweet, Fengyan Zhang, and Sheng Teng Hsu (Sharp Laboratories of America)		J. Vac. Sci. Technol. A, 19(4), 1595-1599 (2001)	Ir and Co were used as interlayer of Ni/Si system. Both of them can suppress the increase in sheet resistance. The leakage current of Shallow junction and its thermal stability were improved by the addition of Ir. Ti, Mg, Al were examined (No good effect?)	Yes	Ir, Co

3	Effects of Mo Interlayer on the Electrical and Structural Properties of Nickel Slicides	Young-Woo Ok,Chel-Jong Choi,and Tae-Yeon Seong	Dep. of Materials Science and Engineering,Kwangju Institute of Science and Tech. (K-JIST), Korea	Journal of The Electrochemical Society,150 (7)G385-G388(2003)	Compared with Ni/Si, the annealing temperature where sheet resistance increased dramatically increased when interlayer Mo was added, Ni/Mo/Si. This is because the creation of agglomeration was delayed when Mo was added. According to the observation results of TEM, AES, Mo appeared on the surface when samples were annealed above 500℃. Fig. 1 Annealing temperature versus sheet resistance of Ni(30nm)/Si, Ni(28nm)/Mo(1.5nm)/Si Fig. 3 SEM images of Ni(30nm)/Si,Ni(28nm)/Mo(1.5nm)/Si Fig. 4 TEM images of Ni(30nm)/Si,Ni(28nm)/Mo(1.5nm)/Si Below were references that thermal stability of NiSi was improved because agglomeration was suppressed when N ions implanted into Si substrate before Ni deposited on it. 1.P.S.Lee,K.L.Pey,D.Mangelinck,J.Ding,A.T.S.Wee,and L.Chan, IEEE Electron Device Lett.,21,566(2000) 2.L.W.Cheng,S.L.Cheng,J.Y.Chen,L.J.Chen,and B.Y.Tsui, Thin Solid Films, 355-356,412(1999). The increase in resistance was suppressed when interlayer Mo was added. Its addition also suppressed the creation of agglomeration, and greatly improved roughness between NiSi and Si.(?) references about the addition of Pt to Ni/Si system 1.L.W.Cheng,S.L.Cheng,L.J.Chen,H.C.Chien,H.L.Lee, and F.M.Pan, J.Vac.Sci.Technol.A,18,1176(2000). 2.D.Z.Chi,D.Mangelinck,S.K.Lahiri,P.S.Lee,and K.L.Pey, Appl. Phys. Lett., 78,3256(2001) Below is a reference about SiO2 which used as capping layer, SiO2/Ni/Si. The thermal stability of NiSi was improved because the creation of agglomeration was suppressed. C.J.Choi,Y.W.Ok,T-Y.Seong,and Lee,Jpn.J.Appl.Phys.,41, 1969(2002)	Yes	Mo

4	Thermal stability, phase and interface uniformity of Ni-silicide formed by Ni–Si solid-state reaction	Xin-Ping Qua,*, Yu-Long Jianga, Guo-Ping Rua, Fang Lua, Bing-Zong Lia, C. Detavernierb, R.L. Van Meirhaegheb	a Dep. Microelectronics, Fudan Univ., Shanghai, China b Dep. of Solid State Sciences, Univ. of Gent, Ghent, Belgium	Thin Solid Films , Vo.462-463, 2004 pp. 146-150	A study about Ni/Pd/Si.Ni(10nm)/Pd(0.3nm)/Si(duration time 20sec.) .Pd2Si and Ni2Si created at 340℃.NiSi created at 500℃ while Pd diffused to whole film. Ni x Pd(1-x)Si created at 750℃ while NiSi2 did not observe despite the fact that NiSi2 created at this temperature without the addition of Pd. the temperature where NiSi2 formed was 50℃ higher or at 850 with the increase in Pd thickness, Ni(10nm)/Pd(5nm)/Si and up to 900℃ for Ni(10 nm)/Pd(7 nm)/Si and Ni(10 nm)/Pd(10 nm)/Si. The role of Pd in NiSi system was explained by classical nucleation theory.	Yes	Pd
5	Comparison of the thermal stability of NiSi films in Ni/Pt/(111)Si and Ni/Pt/(100)Si systems	J. F. Liu, J. Y. Feng,a) and J. Zhu		J. Appl. Phys., 90(2) 745-749 (2001)	This is a study about thermal stability of NiSi when Pt was added at different position, that is, Ni/Pt/(111)Si and Ni/Pt/(100)Si. Comparison of sheet resistance is not available in this study.	Yes	Pt
6	Improvement of the thermal stability of NiSi films by using a thin Pt interlayer	J. F. Liu, H. B. Chen, J. Y. Feng, and J. Zhu,		Appl. Phys. Lette., 77(14), 2177-2179 (2000)	Data about the relationship between sheet resistance and annealing temperature and the phase transition at corresponding annealing temperature are available.	Yes	Pt

7	Formation of Ni Silicides on (001)Si with a thin interposing Pt layer	L. W. Cheng, S. L. Cheng, and L. J. Chen, H. C. Chien, H. L. Lee, and F. M. Pan		J. Vac. Sci. Technol. A, 18(4), 1176-1179 (2000)	This is a study about the transition of NiSi by the addition of Pt. TEM images of NiSi and NiSi2 are available.	Yes	Pt
8	Coexistence of hexagonal and orthorhombic structures in NiSi filmscontaining Pt	J. Y. Dai,a) D. Mangelinck, and S. K. Lahiri	Institute of Materials Research and Engineering, Singapore	APPLIED PHYSICS LETTERS,Vol. 75, No15,1999 pp.2214-2216	References that the thermal stability of NiSi was improved by the addition of Pt were mentioned. The addition of Pt in NiSi can create hexagonal structure by low temperature annealing.	Yes	Pt
9	Enhancement of thermal stability of NiSi films on (100)Si and (111)Si by Pt addition	D. Mangelinck, a) J. Y. Dai, J. S. Pan, and S. K. Lahiri	Institute of Materials Research and Engineering, Singapore	APPLIED PHYSICS LETTERS, Vol.75, No.12, 1999 pp.1736-1738	No information about sheet resistance versus annealing temperature is available. Phase transition of NiSi with annealing temperature was indicated. NiSi2 starts to create at 900℃ with the existence of NiSi.	Yes	Pt

10	Explanation of the enhancement of NiSi thermal stability according to TFD equations and Miedema's model	R.N. Wang, Y. He, J.Y. Feng *	Key Laboratory of Advanced Materials, Dep. of Materials Science and Engineering,Tsinghua University, PR China	Nuclear Instruments and Methods in Physics Research , Vol.222 Issues 3-4, 2004 pp. 462-468	Graphs about annealing temperature versus sheet resistance of Ni(100nm)/Si(111) and Ni(100nm)/Pt(8nm)/Si(111) are available. Sheet resistance increased dramatically at 750 for Ni(100nm)/Si case and 100℃ higher or at 850℃ for Ni(100nm)/Pt(8nm)/Si(111) case. (deposition rate 0.4A/s for Pt,2A/s for Ni, annealing time 2 min.) The role of Pt to the phase transition of NiSi was also explained by means of growth energy between atomic.	Yes	Pt
11	Phase and Layer Stability of Ni-and Ni(Pt)-Silicides on Narrow Poly-Si Lines	P.S.Lee,[a]K.L.Pey,[b]D. Mangelinck,[c]J.Ding,[a] D.Z.Chi,[d]J. Y.Dai,[e]and L..Chan[e]	[a]Dep. of Materials Science [b]Dep. of Electrical and Computing Engineering [c]L2MP-CNRS,Faculte de Saint-Jerome-case 151,13397 Marsaille Cedex 20,France [d]Institute of Materials Research and Engineering,National Univ. of Singapore 119260 [e]Chartered Semiconductor Manufacturing Limited,Singapore 738406	Journal of The Electrochemical Society,149(6) G331-G335(2002)	Comparison between Ni/poly-Si and Ni(Pt)/poly-Si were held below: Fig. 1 Raman spectroscopy observation results of different annealing temperature Fig. 2 RBS observation results for Ni- at 600, 700℃, for Ni(Pt)- at 700℃, 750℃ Fig. 3 Raman observation results with a scope of 0.25μm of 100μm poly-Si for Ni- at 750℃, for Ni(Pt)- at 800℃ Fig. 4 XTEM images of Ni- at 750℃	Yes	Pt

12	Layer Inversion of Ni(Pt)Si on Mixed Phase Si Films	P.S.Lee,[a]K.L.Pey,[b]D.Mangelinck,[c]J.Ding,[a]T.Osipowicz,[d]and A.See[e]	[a]Dep. of Materials Science, National Univ. of Singapore, [b]Dep. of Electrical Engineering,National Univ. of Singapore, [c]L2MP-CNRS,Faculte de Saint-Jerome-case 151,13397 Marsaille Cedex 20,France [d]Dep. of Physics,National University of Singapore, [e]Chartered Semiconductor Manufacturing Limited,738406 Singapore	Electrochemical and Solid-State Letters,5(3) G15-G17(2002)	results for Ni(Pt)Si Fig. 2 Raman spectroscopy results at 600, 750, 800℃. wavenumber(cm^-1)×counts(arb.unit) Fig. 3 RBS spectrum at 600, 700, 750℃ Fig. 4 XTEM images at 600℃ according to Fig. 2 NiSi looks to exist even at 800℃.	Yes	Pt
13	Film thickness dependence of the NiSi-to-NiSi2 transition temperature in the Ni/Pt/Si(100) syitem	J.F.Liu, J.Y.Feng, and J.Zhu	Dep. Materials Science and Engineering,Key Laboratory of Advanced Materials,Tsinghua Univ.,Beijing 100084,China	APPLIED PHYSICS LETTERS Vol.80,No.2, 2002,pp.270-272	Ni/Pt/Si structure: sample A[Ni(50nm)/Pt(4nm)/Si(100)]、sample B[Ni(25nm)/Pt(2nm)/Si(100)]、sample C[Ni(12.5nm)/Pt(1nm)/Si(100)] Fig. 1 XRD images at 800, 840, 880℃(NiSi2 did not create at 800℃ for A, and up to 880℃ for B and C cases. Fig. 2 sheet resistance of sample A, B and C versus annealing temperature with an interval of 20℃ raging from 750℃ to 800℃ The creation temperature of NiSi2 became higher by the addition of Pt. The role of Pt became weak and sheet resistance increases if total film thickness decreased at the condition of same rate of Pt.	Yes	Pt

14	Influence of Pt addition on the texture of NiSi on Si(001)	C.Detavernier and C.Lavoie	IBM T.J. Watson Research Center,Yorktown Heights,New York 10598	APPLIED PHYSICS LETTERS,Vol.84, No.18, 2004 pp.3549-3551	a study about the structure of $Ni_{1-x}Pt_xSi(001)$ thin film Fig. 1 Observation result of XRD, RBS Below are papers that thermal stability of NiSi was improved with the addition of Pt. 1 D.Z.Chi,D.Mangelinck,J.Y.Dai,S.K.Lahiri,K.L.Pey,and C.S. Ho, Appl. Phys. Lett. 76,3385(2000) 2 D.Z.Chi,D.Mangelinck,S.K.Lahiri,P.S.Lee,and K.L.Pey, Appl.Phys.Lett. 78,3256(2001)	Yes	Pt
15	Thermally robust Ta-doped Ni SALICIDE process promising for sub-50 nm CMOSFETs	Sun, M.C.; Kim, M.J.; Ku, J.-H.; Roh, K.J.; Kim, C.S.; Youn, S.P.; Jung, S.-W.; Choi, S.; Lee, N.I.; Kang, H.-K.; Suh, K.P.;		VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on , 10-12 June 2003 Pages:81 - 82	NiSi which applied to 50nm gate length MOSFET was stable up to 600℃ when Ta was added. NiTa silicide may retain the agglomeration of Co silicide, the phase transition of NiSi. P.S.Lee et al..J.Electrochem.Soc.,vol.149,pG331,2002.	Yes	Ta

16	High Thermal Stability of Ni Monosilicide from Ni-Ta Alloy Films on Si(100)	Min-Joo Kim,[a]Hyo-Jick Choi,[a]Dae-Hing Ko,[a]Ja-Hum Ku,[b]Siyoung Choi,[b] Kazuyuki Fujihara,[b]and Cheol-Woong Yang[c]	[a]Dep. of Ceramic Engineering, Yonsei Univ.,South Korea [b]Samsung Electronics Co. LTD., Semiconductor Research and Development Division, Process Development Team, Korea [c]School of Metallurgical and Materials Engineering, Sungkyunkwan Univ., Korea	Electrochemical and Solid-State Letters, 6(10)G122-G125(2003)	Fig. 1 TEM images of Ni/Si and Ni0.90Ta0.10/Si Fig. 2 TEM images of Ni/Si and Ni0.90Ta0.10/Si after annealed at 500℃ for 30sec. Fig. 3 RBS spectrum of Ni-Ta silicide after annealed at 500℃ for 30sec and RUMP simulation result Fig. 5 XRD spectrum of Ni1-xTax/Si(x=0,5,10) after annealed at 600℃ for 120min. Fig. 6 RBS spectrum of Ni/Si and Ni0.90Ta0.10/Si after annealed at 600℃ for 30min. and 120min.. Fig. 7 TEM images of Ni/Si, Ni0.95Ta0.05/Si, Ni0.90Ta0.10/Si after annealed in N2 ambient at 600℃ form 120min.	Yes	Ta
17	Effect of titanium cap in reducing interfacial oxides in the formation of nickel silicide	W.L.Tan and K.L.Pey,[a] Simon Y.M.Chooi, [b]J.H.Ye, [c]T.Osipowicz[d]	[a]Center for Integrated Circuit Failure Analysis and Reliability,Faculty of Engineering,National Univ. of Singapore, [b]Dep. of Tech. Development, Chartered Semiconductor Manufacturing Limited,Singapore [c]Institute of Materials Research and Engineering,3 Research Link,Singapore [d]Dep. of Physics,Faculty of Science,National Univ. of Singapore	JOURNAL OF APPLIED PHYSICS, Vol.91, No.5,2002, pp.2901-2909	Titanium was deposited on the surface of Ni/nature oxide layer/Si, Ni/oxide layer by intentional chemical reaction/Si. The offset temperature of NiSiTi differs with the quantity of Ti. Oxidation reaction occurs if Ti layer is too thin.	Yes	Ti

18	Materials aspects electrical performance,and scalability of Ni silicide towards sub-0.13μm technologies	Anne Lauwers, An Steegen, Muriel de Potter, Richard Lindsay, Alessandra Satta, Hugo Bender, and K. Maex	IMEC,Kapeldreef 75,3001 Leuven, Belgium	J. Vac. Sci. Technol. B 19(6), Nov/Dec 2001,pp.2026-2037	Comparison between Ni and Co with Ti cap or not. Fig. 1 RTP annealing temperature versus sheet resistance of Ni(12nm, 18nm)/Si with Ti cap Fig. 2 XRC spectrum of Ni(12nm)/Si annealed at 300, 400, 700℃ Fig. 3 RTP annealing temperature versus sheet resistance of Ni(18nm)/undoped Si, As doped Si, B doped Si substrate	Yes	Ti

19	Effects of Ti Interlayer on Ni/Si Reaction systems	S.L.Chiu,[a] Y.C.Chu,[a] C.J.Tsai,[a] and H.Y.Lee[b]	[a]Dep. of Materials Science and Engineering,National Tsing Hua Univ.,Hsinchu,Taiwan [b]National Synchrotron on Radiation Research Center,Hsinchu,Taiwan	Journal of The Electrochemical Society,151(7)G452-G455(2004)	Effects of Ti Interlayer on Ni/Si Reaction were studied by changing the rate of Ti/Ni. The effect of Ti interlayer on Ni/Si reaction was to disturb the diffusion of Ni to Si. Fig. 2 XRD observation result of Ni（30nm）/Ti（3nm）/Si after annealed at 396℃~875℃ Fig. 3 TEM images of Ni(30nm)/Ti(3nm)/Si at 359℃, 700℃, 825℃ Fig. 5 XRD results of Ni(30nm)/Si and Ni(30nm)/Ti（3nm）/Si after annealed at 794℃ C.Detavernier,X.P.Qu,R.L..Van Meirhaeghe,B.Z.Li,and M.Maex,J.Mater.Res.,18.1668(2003). references about Ni/Pt/Si 1 J.F.Liu,H.B.Chen,J.Y.Feng,and J.Zhu,Appl.Phys.Lett.,77,2177(2000) 2 J.F.Liu,J.Y.Feng,and J.Zhu,Appl.Phys.Lett.,80,270(2002) 3 L.W.Cheng,S.L.Cheng,L.J.Chen,H.C.Chien,H.L.Lee,and F.M.Pan,J.Vac.Sci.Technol.A,18,1176(2000) 4 D.Mangelinck,J.Y.Dai,J.S.Pan,and S.K.Lahiri,Appl.Phys.Lett.,75,1736(1999) 5 R.N.Wang,J.Y.Feng,and Y.Huang,Appl.Surf.Sci.,207,139(2003) reference about Ni/Pd/Si 1 P.Gergaud,O.Thomas,and B.Chenevier,J.Appl.Phys.,94,1584(2003). 2 P.Gergaud,M.Megdiche,O.Thomas,and B.Chenevier,J.Appl.Phys.,83,1334(2003). 3 C.J.Tsai,P.L.Chung,and K.H.Yu,Thin Solid Films,365,72(2000). reference about Ni/Ir/Si ,Ni/Co/Si J.-s.Maa,Y.Ono,D.J.Tweet,F.Zhang,and S.T.Hsu,J.Vac.Sci.Technol.A,19,1595(2001)	Yes	Ti

20	Characterization of reactions at titanium/nickel silicide interface using X-ray photoelectron spectroscopy and transmission electron microscopy	Jin Zhao*, Jiong-Ping Lu, Yu-Qing Xu, Yu-Ji R. Kuan, Lancy Tsung	Texas Instruments, USA	Applied Surface Science, Vol.211 (2003) pp.367–372	Ni/Si is oxidized in air. So, TiN/Ti was deposited on the surface of Ni/Si. Ti would take Si from NiSi to creat high resistivity material TiSix over 550℃. The remaining Ni would take Si from substrate. In the end, Si consumption became large.	Yes	Ti, Ti/N
21	Highly Reliable Nickel Silicide Formation with a Zr Capping Layer	Tsung Lin Lee,Jam Wem Lee,Mei Chi Lee,Tan Fu Lei,and Chung Len Lee	Dep.of Electronics Engineering,National Chiao-Tung Univ.,Hsin-Chu,Taiwan	Electrochemical and Solid-State Letters,6(5)G66-G68 (2003)	Zr(10nm)/Ni(30nm)/Si structure can not only prevent oxygen contamination but also heighten the temperature where NiSi transits to NiSi2. Moreover, it can suppress the surface roughness. Therefore, its sheet resistance keeps at low level at 850℃. Fig. 1 annealing temperature versus sheet resistance of Ni(30nm)/Si,Ti(10nm)/Ni(30nm)/Si,Zr(10nm)/Ni(30nm)/Si Fig. 2 TEM image of Ti(10nm)/Ni(30nm)/Si,Zr(10nm)/Ni(30nm)/Si annealed at 850℃ Fig. 3 XRD spetrum of Ti(10nm)/Ni(30nm)/Si,Zr(10nm)/Ni(30nm)/Si annealed at 650℃, 850℃ W.L.Tan,K.L.Pey,S.Y.M.Chooi,J.H.Ye,and T.Osipowicz, J.Appl.Phys.,91,2901(2002) (NiSi is extremely sensitive to oxygen contamination. Cap layer can be used to suppress oxygen contamination.) Zr was added as capping layer. Comparison with Ti was also held. The role of Zr was mainly to prevent from oxidation. At the same time, it had effect on decrease surface roughness and agglomeration. Sheet resistance kept at low level at 850℃(NiSi2 had created for Ti. However no NiSi2 was observed in case of Zr)	Yes	Zr

22	Degradation mechanism of NiSi thin films with annealing process	K.Okubo, Y.Tsuchiya, O.Nakatsuka, A.Sakai, S.Zaima, and Y.Yasuda	Nagoya Univ.	Extended Abstracts(the 50th Spring Meeting, 2003),The Japan Society of Applied Physics and Related societies,No.2 p900	A study concerns the degradation of NiSi thin film dependence on time of thermal process. Fig. 1 shows sheet resistance versus annealing time with temperature raging from 550℃ to 850℃	Yes	No
23	Phase transition suppression effect of Ni silicide by SiGe	M.Izuha, K.Miyano, T.Iinuma, I.Mizushima and K.Suguro	Toshiba Corp. Semiconductor Co. Process & Manufac. Eng., Center	Extended Abstracts(the 63rd Autumn Meeting, 2002),The Japan Society of Applied Physics,No.2 p756	Agglomeration and phase transition to NiSi2 was suppressed if Ni deposited on poly-SiGe instead of the poly-Si substrate.	Yes	No

24	A novel nickel SALICIDE process technology for CMOS devices with sub-40 nm physical gate length	Lu, J.P.; Miles, D.; Zhao, J.; Gurba, A.; Xu, Y.; Lin, C.; Hewson, M.; Ruan, J.; Tsung, L.; Kuan, R.; Grider, T.; Mercer, D.; Montgomery, C.;		Electron Devices Meeting, 2002. IEDM '02. Digest. International , 8-11 Dec. 2002 Pages:371 - 374	This novel nickel SALICIDE process technology for CMOS devices with sub-40 nm physical gate length is in-situ anneal method, which can achieve Ni-rich NiSi and control salicidation.	Yes	No
25	Toward implementation of a nickel silicide process for CMOS technologies	* C. Lavoie , F.M. d'Heurle,C. Detavernier, C. Cabral Jr.		Microelectronic Engineering, 70, 144_157 (2003)	There are data about the comparison between CoSi and NiSi. The method that how to avoid the phase transition from NiSi to NiSi2 after high temperature process was also mentioned.	Yes	No
26	Comparative study of current-voltage characteristics of Ni and Ni(Pt)-alloy silicided p+/n diodes	D. Z. Chi,a) D. Mangelinck, and S. K. Lahiri, P. S. Lee,K. L. Pey		Appl. Phys. Lette., 78(21), 3256-3258 (???)	mainly about I-V characteristics. Relation about temperature was also mentioned.	Yes	No

27	Concentration-controlled phase selection of silicide formation during reactive deposition	A. Vantomme,a), b) S. Degroote, J. Dekoster,b) and G. Langouche R. Pretorius	Institute voor Kern-en Stralingsfysica, Katholieke Universiteit Leuven, Belgium Van de Graaff Group, National, South Africa	APPLIED PHYSICS LETTERS, Vol.74, No.21, 1999 pp.3137-3139	Reaction of phase transition was explained by the view of energy with an example of CoSi.	Yes	No
28	Role of the substrate strain in the sheet resistance stability of NiSi deposited on Si(100)	Eliane Maillard-Schaller,a) B. I. Boyanov, S. English, and R. J. Nemanich	Dep.of Physics, North Carolina State Univ., North Carolina	JOURNAL OF APPLIED PHYSICS, Vol.85, No.7, 1999 pp.3614-3617	Ni was deposited on strained Si(100) substrate and bulk Si(100). The temperature where sheet resistance increased dramatically was at 600℃ for Ni/bulk Si and 100℃ higher for Ni/strained Si. This fact was caused not by the phase transition from NiSi to NiSi2 (because this temperature is too low to occur) but by the agglomeration.	Yes	No
29	Contact metallization on strained-Si	A.R. Saha a,*, S. Chattopadhyay b, C.K. Maiti a	a)Dep. of Electronics and ECE, IIT Kharagpur, India b)School of Electrical, Electronic and Computer Engineering, Univ. of Newcastle upon Tyne, UK	Solid-State Electronics 48 (2004) pp.1391–1399.	Relationship between annealing temperature and sheet resistance of Co, Ti, Ni were available. Graphs about the relationship between barrier heigt and measurement temperature of NiSi/strained Si and NiSi/bulk-Si were also available. Barrier height increased with measurement temperature	Yes	No

30	Thermal stability study of NiSi and NiSi2 thin films	F.F. Zhao a,*, J.Z. Zheng a, Z.X. Shen a, T. Osipowicz a, W.Z. Gao b, L.H. Chan b	a Dep. of Physics, 2 Science Drive 3, National Univ. of Singapore, b Chartered Semiconductor Manufacturing Limited, Singapore	Microelectronic Engineering 71 (2004) pp.104–111	Ni was deposited on p-(100)Si with thickness of 20nm,16nm,8nm,4nm and heat process was held in N2 ambient for 30 sec. raging from 450°C～850°C. Annealing temperature versus sheet resistance of various thicknesses was available. The temperature where sheet resistance increased dramatically was same (750°C) for thickness from 8nm to 20nm and 50°C lower or 700°C for **4** nm case. Increase gradient for sheet resistance decrease with Ni thickness.	Yes	No
31	Investigation on the barrier height and phase transformation of nickel silicide Schottky contact	Shihua Huang, Yun Tian, Fang Lu*	Surface Physics Lab., Fudan Univ., China	Applied Surface Science, Vol.234, Issues 1-4, 2004, pp. 362-368	Investigation concerns the transition of barrier height of NiSi after annealed. Barrier height relates to annealing temperature. Analysis of experimental result was based on Gaussian distribution of Schottky barrier height.	Yes	No
32	Enhanced growth of low-resistivity NiSi on epitaxial $Si_{0.7}Ge_{0.3}$ on (001)Si with a sacrificial amorphous Si interlayer	W.W.Wu,S.L.Cheng,S.W.Lee,and L.J.Chen	Dep.of Materials Science and Engineering,National Tsing Hua Univ.,Hsinchu,Taiwan, Republic of China	J.Vac.Sci.Technol. B 21(5),Sep/Oct 2003,pp.2147-2150	Fig. 1 TEM images of Ni(30nm)/Si0.7Ge0.3 annealed at 700°C for 30sec.	Yes	No

33	Thermal reaction of nickel and $Si_{0.75}Ge_{0.25}$ alloy	K.L.Pey,[a] W.K.Choi,[b] E.A.Fitzgerald,[c] D.A.Antoniadis,[c] and P.S.Lee[d]	[a]Dep. of Electrical and Computer Engineering,National Univ. of Singapore and Advanced Materials for Micro-and Nano-systems Programme,Singapore-MIT Alliance,4 Engineering Drive,Singapore [b]Dep. of Electrical and Computer Engineering, National Univ. of Singapore, and Advanced Materials for Micro-and Nano-systems Programme, Singapore-MIT Alliance,4 Engineering Drive, Singapore [c]Massachusetts Institute of Tech.,Cambridge,Massachusetts and Advanced Materials for Micro-and Nano-systems Programme,Singapore-MIT Alliance,4 Engineering Drive,Singapore [d]Dep. of Materials Science,National Univ. of Singapore	J.Vac.Sci.Technol.A 20(6),Nov/Dec 2002, pp.1903-1910	Sheet resistance of Ni(25nm)/$Si_{0.75}Ge_{0.25}$ increased dramatically when annealing temperature increased above 800℃. Fig. 1 annealing temperature versus sheet resistance of Ni(25nm)/Si0.75Ge0.25 Fig. 2 XRD of Ni(25nm)/Si0.75Ge0.25 at different annealing temperature Fig. 3 Raman spectrum of Ni(25nm)/Si0.75Ge0.25 at different annealing temperature Fig. 4 SEM image of Ni(25nm)/Si0.75Ge0.25 at (a)700℃ (b)900℃ Fig. 5 SEM image of Ni(25nm)/Si0.75Ge0.25 at (a)500℃ (b)800℃ studies about nickel-monosilicide 1. Z.Jin,G.A.Bhat,M.Yeung,H.S.Kwok,and M.Wong,Jpn.J.Appl.Phys.,Part2 36,L1637(1997) 2. S.J.Naftel,I.Coulthard,T.K.Shan,S.R.Das,and D.X.Xu,Phys.Rev.B57,9179(1998) 3. J.Y.Dai,D.Mangelick,and S.K.Lahiri,Appl.Phys.Lett.75,2214(1999) 4. H.Hou,T.F.Lei,and T.S.Chao,IEEE Trans.Electron Device 20,572(1999)	Yes	No

34	Evaluation of Nickel Silicide Using Flash Lamp Equipment	I.Nishimura, M.Noguchi, K.Yamashita, N.Kasai, T.Arikado, K.Yamada, K.Okumara	Selete Inc., Waseda Univ., Tokyo Univ.	Extended Abstracts(the 64th Autumn Meeting, 2003),The Japan Society of Applied Physics, No.2 p751	Surface condition, sheet resistance, junction leackage current of NiSi formed by flash lamp were analyzed detailedly.	No	No
35	Low temperature formation of epitaxial NiSi2 by solid phase reaction of Ni/Ti/Si structure	K.Okubo, Y.Tsuchiya, O.Nakatsuka, A.Sakai, S.Zaima, and Y.Yasuda	Nagoya Univ.	Extended Abstracts(the 64th Autumn Meeting, 2003),The Japan Society of Applied Physics ,No.2 p751	Epitaxial NiSi2 was created at unusually low temperature by the solid reaction of Ni/Ti/Si system. Fig. 1 cross section TEM images of Ni(18nm)/Ti(2nm)/Si annealed at 350℃ for 30min.	No	No
36	Study on Ni/p+-Si1-x-yGexCy/Si(100) Contacts	O.Nakatsuka, H.Ikeda, A.Sakai, S.Zaima, J.Murota, and Y.Yasuda	Nagoya Univ, Tohoku Univ.	Extended Abstracts(the 49th Spring Meeting, 2002),The Japan Society of Applied Physics and Related societies,No.2 p774	A study about solid reaction and electrical characteristics of Ni/p+-Si1-x-yGexCy/Si(100) structure. Fig. 1 XRD profile of Ni/Si and Ni/p+-Si1-x-yGexCy/Si after annealed at 850℃.	No	No

37	Formation mechanism of NiSi/Si Ohmic contact with low resistivity	O.Nakatsuka, Y.Tsuchiya, A.Sakai, S.Zaima, and Y.Yasuda	Nagoya Univ	Extended Abstracts(the 49th Spring Meeting, 2002),The Japan Society of Applied Physics and Related societies,No.2 p775	A report that NiSi contact resistivity in an order of $10^{-8}\Omega cm^2$ was achieved for both n+-Si and p+-Si case was made last time. The observation and consideration concerning the formation mechanism of the low contact resistivity were done this time Fig. 1 depth section SIMS profile of NiSi/n+-Si	No	No
38	Pattern dependent crystallization in Ni-MILC of a-Si	H.Nozaki, K.Makihira, T.Asano, M.Miyasaka	Kyushu Institute of Tech. Seiko Epson Corp.	Extended Abstracts(the 62nd Autumn Meeting, 2001),The Japan Society of Applied Physics,No.2 p676	Images of crystal growth after samples were annealed in N2 ambient were available.	No	No
39	Mechanism of Ni-enchanced low-temperature Si epitaxy	Y.Uchida, N.Katsumata and K. Ishida	Teikyo Univ. of Sci. & Tech.	Extended Abstracts(the 62nd Autumn Meeting, 2001),The Japan Society of Applied Physics ,No.2 p683	Cross section TEM image about NiSi was available here.	No	No

40	65 nm CMOS technology (CMOS5) with high density embedded memories for broadband microprocessor applications	Yanagiya, N.; Matsuda et al.		Electron Devices Meeting, 2002. IEDM '02. Digest. International , 8-11 Dec. 2002 Pages:57 - 60	Ni salicide is applied to the source, drain of MOSFET to get low leakage current and low resistance. Fig. 8 shows the relationship between sheet resistance and gate length made from Ni silicide. Sheet resistance kept at 7Ω/sq with gate length as low as 20nm.	No	No
41	In situ high-temperatur e synchrotron-radi ation diffraction studies of Ni and Co-Ni silicidation processes	J. Rinderknecht,H. Prinz,T. Kammler, F. Berberich,E. Zschech		Microelectronic Engineering, 64 , 143_149(2002)	analysis about phase transition of NiSi at different annealing temperatures	No	No
42	NiSi salicide technology for scaled CMOS	Hiroshi Iwai,Tatsuya Ohguro,Shun-ichi ro Ohmi		Microelectronic Engineering, 60, 157_169 (2002)	the introduction of NiSi technology, compared with MoSi2,WSi2,TiSi2,CoSi2	No	No
43	In situ transmission electron microscopy study	V. Teodorescu and L. Nistor,H. Bender, A. Steegen, A.		J. Appl. Phys., 90(1) 167-174 (2001)	Phase transition of NiSi was investigated. Lots of TEM images were available. But, No data about sheet resistance here.	No	No

	of Ni silicide phases formed on (001) Si active lines	Lauwers, and K. Maex, J. Van Landuyt					
44	Investigation of Polycrystalline Nickel Silicide Films as a Gate Material	Ming Qin, Vincent M. C. Poon, and Stephen C. H. Ho		J. Electrochem. Soc., 148(5), G271-G274 (2001)	This paper is about investigation about the work function of NiSi and its DPE effect.	No	No
45	In situ real-time studies of nickel silicide phase formation	M. Tinani, A. Mueller, Y. Gao, and E. A. Irene, Y. Z. Hu and S. P. Tay		J. Vac. Sci. Technol. B, 19(2), 376-383 (2001)	Transition of NiSi was observed in detail. Information about Surface roughness was available.	No	No
46	Micro-Raman Spectroscopy Investigation of Nickel Silicides and Nickel(Platinum) Silicides	P. S. Lee, D. Mangelinck,K. L. Pey, Z. X. Shen, J. Ding,a T. Osipowicz,d and A. See		Electrochemical and Solid-State Lett., 3(3), 153-155 (2000)	Annealing temperature versus NiSi intensity-wavenumber graph was available here.	No	No

47	Electrical Properties and Solid-Phase Reactions in Ni/Si(100) Contacts	Yoshinori Tsuchiya, Akihiro Tobioka,Osamu Nakatsuka, Hiroya Ikeda,Akira Sakai, Shigeaki Zaima and Yukio Yasuda		Jpn.J.Appl.Phys., 41(4B), 2450-2454 (2002)	There are lots of XRD, AFM, TEM observation results.	No	No
48	Ni Precursor for Chemical Vapor Deposition of NiSi	Masato Ishikawa, Takeshi Kada,Hideaki Machida, Yoshio Ohshita and Atsushi Ogura		Japn. J. Appl. Phys., 43(4B), 1833-1836 (2004)	the latter half was information about NiSi. Fig. 4 XRD spectrum of (MeCp)2Ni annealed at 300℃. Fig. 5 TEM image of sample mentioned in Fig. 4. Fig. 7 TEM image of (MeCp)2Ni with a mixture of 1% Si3H8 annealed at 600℃. Fig. 8 TEM image shows that a uniform thin-film of NiSi achieved.	No	No
49	Effects of Ti Interlayer on Ni/Si Reaction Systems	S. L. Chiu, Y. C. Chu, C. J. Tsai and H. Y. Lee (Nat. Tsing Hua Univ., Nat. Synchrotron Radiation Res. Cent.)		J. Electrochem. Soc., 151(7), G452-G455 (2004)	Ti was used as interlayer on Ni/Si. No good effect in thermal stability of NiSi was observed.	No	No

50	Electronic structure of nickel silicide in subhalf-micron lines and blanket films: An x-ray absorption fine structures study at the Ni and Si L3,2 edge	S. J. Naftel, I. Coulthard, and T. K. Sham D.-X. Xu, L. Erickson, and S. R. Das	Dep.Chemistry, Univ. of Western Ontario, Canada Institute for Microstructural Sciences, National Research Council Ottawa K1A 0R6, Canada	APPLIED PHYSICS LETTERS, Vol.74, No.19, 1999 pp.2893-2895	irrelevant to thermal stability	No	No
51	Silicidation on Chemical Mechanical Polished Electrode Process for Metal-Silicide/Polysilicon Gate Application	Hyeon-Soo Kim,z Se-Aug Jang, Tae-Kyun Kim, In-Seok Yeo, and Sahng-Kyoo Lee	Hyundai Electronics Industries Company Limited, Semiconductor Advanced Research Division, Korea	Electrochemical and Solid-State Letters, 2 (5) 244-246 (1999)	MOSFET with 0.2μm gate length was fabricated with Ti silicide. The electrical characteristics were mainly described.	No	No
52	Formation of silicided shallow p+ n junctions by BF2+ implantation into thin amorphous-Si or Ni/amorphous-Si films on Si substrates and subsequent Ni silicidation	M. H. Juanga) and M. C. Hu C. J. Yang	Dep. of Electronics Engineering, National Taiwan Univ. of Science & Technology,Taiwan Dep. of Electronics Engineering, National Chiao-Tung University, Taiwan,	J. Vac. Sci. Technol. B 17(2), 1999, pp.392-396	Shallow doping can be achieved by the annealing of Ni silicide. But this process can lead to strengthen the leakage current. Relationship between annealing temperature and leakage current is available in this study.	No	No

53	Schottky barrier height measurement of swift heavy ion intermixed Ni–Silicide interface	Veenu Sisodia a,*, D. Kabiraj b, I.P. Jain a,*	a Centre for Non-Conventional Energy Resources, University of Rajasthan, India b Nuclear Science Centre, India	Nuclear Instruments and Methods in Physics Research, Vol.225,Issue 3, 2004 pp.256-260	irrelevant to thermal stability	No	No
54	Corrosion resistance of laser clad Cr-alloyed Ni2Si/NiSi intermetallic coatings	L.X. Cai, H.M. Wang*, C.M. Wang	Laboratory of Laser Materials Processing and Surface Engineering, School of Materials Science and Engineering, Beihang University (formerly Beijing University of Aeronautics and Astronautics), PR China	Surface and Coatings Technology,182 (2004) pp.294–299	irrelevant to thermal stability	No	No
55	Effects of Hydrogen Implantation on the Structural and Electrical Properties of Nickel Silicide	Chel-Jong Choi,[a] Young-Woo Ok,[a] Shiva S.Hullavarad,[a] Tae-Yeon Seong,[a] Key-Min Lee,[b] Joo-Hyoung Lee,[b]and Young-Jin park[b]	[a]Dep. of Materials and Engineering,Kwangju Institute of Science and Tech.,Kwangju 500-712,Korea [b]Hynix Semiconductor,Incorporated, Memory Research and Development Division,Cheongju 362-725,Korea	Journal of The Electrochemical Society,149(9)G517-G 521(2002)	Lots of TEM, AFM, XPS of Ni/Si with/without the implantation of Hydrogen were available. However no good effect to the thermal stability of NiSi.	No	(H)

<table>
<tr>
<td>56</td>
<td>Effect of Ion Implantation on Layer Inversion of Ni Silicided Poly-Si</td>
<td>P.S.Lee,[a]K.L.Pey,[b]D.Mangelinck,[c]J.Ding,[a]D.Z.Chi,[d]T.Osipowicz,[e]J.Y.Dai,[c]and L..Chan[f]</td>
<td>[a]Dep. of Materials Science
[b]Dep. of Electrical and Computer Engineering
[c]L2MP-CNRS,Faculte de Saint-Jerome-case 151,13397 Marsaille Cedex 20,France
[d]Institute of Materials Science and Engineering
[e]Dep. of Physics,National Univ. of Singapore, [f]Chartered Semiconductor Manufacturing,Limited,Singapore 738496</td>
<td>Journal of The Electrochemical Society,149(9)G505-G509(2002)</td>
<td>comparison of Ni silicide with dapant (no, BF2+, N2+)
Fig. 1 XTEM images of Poly-Si annealed at 500℃, 700℃.
Fig. 2 RBS observation of Ni deposited on poly-Si at annealing temperature of 500, 600, 700, 800℃.
Fig. 3 RBS observation of Ni/poly-Si with implantation of BF2+ at annealing temperature of 500, 600, 700, 800℃.
Fig. 4 RBS observation of Ni/poly-Si with implantation of N2+ at annealing temperature of 500, 700, 750℃.
Fig. 5 Raman spectroscopy observation of Ni/poly-Si annealed at 600, 700℃ and Ni/poly-Si annealed at 700℃ with implantation of BF2+ or N2+.
Fig. 6 SEM images of Ni/poly-Si annealed at 600℃ with implantation of BF2+ or N2+ or nothing.
Fig. 7 relation between sheet resistance and annealing temperature when Ni/poly-Si was implanted BF2+ or N2+ or nothing.</td>
<td>No</td>
<td>(BF2+, N2+)</td>
</tr>
</table>

57	$NiAi_{1.74}Al_{0.26}$ and $NiSi_{1.83}Ga_{0.17}$:Two materials with perfect lattice match to Si	Klaus W.Richter,[a]and Kurt Hiebl[b]	[a]Institute of Inorganic Chemistry,University of Vienna,Austria [b]Institute of Physical Chemistry,University of Vienna,Austria	APPLIED PHYSICS LETTERS,Vol.83,No. 3, 2003 pp.497-499	this paper is irrelevant to thermal stability。 references（Ni/Sisystem with additive of Co,Au,Pt） J.M.Gay,D.Mangelinck,P.Stocker,B.Pichaud,and P.Gas,Physica B 221,90 (1996) D.Mangelinck,P.Gas,J.M.Gay,B.Pichaud,and O.Thomas,J.Appl.Phys.84,2583 (1998)	No	No
58	High-resolution investigation of atomic interdiffusion during Co/Ni/Si phase transition	A.Alberti,C.Bongiorno,F.La Via,and C.Spinella	CNR-IMM Sezione di Catania,Stradale Primosole 50,95121 Catania,Italy	JOURNAL OF APPLIED PHYSICS.,Vol.94, No.1, 2003, pp.231-237	No infromation about thermal stability was available in this paper. Figure 3 shows a spectrum of Co/Ni/Si annealed at 400℃. Paper concerns Co/Ni/Si: A.Lauwers,A.Steegen,M.de Potter,R.Lindsay,A.Satta,H.Bender,and K.Maex,J.Vac.Sci.Technol.B19,2026(2001) Compared with Co/Si system, Co/Ni/Si system reacts at lower temperature. Below are those papers: 1.T.G.Finstad,D.D.Anfiteatro,V.R.Deline,F.M.D`Heurle ,P.Gas,V.L.Moruzzi,K.Schwarz,and J.Tersoff,Thin Solid Films 135,229(1986) 2.F.M.D`Heurle,D.D.Anfiteatro,V.R.Deline,and T.G.Finstad, Thin Solid Films 128,107(1985) 3.C.Detavernier,R.L..VanMeirhaeghe,F.Cardon,andK. Maex, Phys.Rev.B62,12045(2000)	No	No

59	Reaction sequence of Co/Ni/Si(001) system	S.S.Guo,[a]and C.J.Tsai[b]	[a]Dep. of Materials Engineering,National Chung Hsing Univ.,Taichung,Taiwan,Republic of China [b]Dep. of Materials Science and Engineering,National Tsing Hua Univ.,HsinChu,Taiwan,Republic of China	J.Vac.Sci.Technol. A 21(3),May/Jun 2003,pp.628-633	a paper concerns Co silicide. The reaction sequence of Co(90nm)/Ni(9nm)/Si at different annealing temperatures was investigated by TEM, XRD,AES. The addition of interlayer Ni can decrease the surface tress despite no effect to reaction sequence.	No	No

Chapter 2

FABRICATION AND MEASUREMENTS

2 Flow of Experiments

In this chapter, experiment instruments which were used in this study were introduced. Before these introductions, flow of experiments was presented in brief.

P-type (100)Si substrates with B concentration of ~$10^{20}/cm^3$, whose density is expected for the 45nm node, were used in this study.

After Si substrate was cleaned by SPM and diluted HF, film structures M/Ni/Si, Ni/M/Si (Here M is a metal additive except Ni.) and Ni/Si were deposited on Si (100) substrates by using an UHV-sputtering system after substrate cleaning process. Then these samples were annealed in forming gas (3%-H_2) ambient using a rapid thermal annealing (abbreviated as RTA) system. Sheet resistance of the silicide layers was measured by the four point probe method. Structures of the layers were observed by AFM, XRD, RAMAN Spectroscopy, etc.

2.1 Si Substrate Cleaning Process

At first, high quality thin films require ultra clean Si surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩcm at 25°C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩcm at

resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle (fΦ0.1μm) per milliliter.

In this study, the Si substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The flow of the Si clean process was shown as Fig.2.1. The first step, which use a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4: H_2O_2=4:1), was performed to remove any organic material and metallic impurities. After that, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:100). Then the cleaned wafer was dipped in DI water. Finally, the cleaned Si substrate was loaded to chamber to deposit as soon as it was dried by air gun.

2.2 UHV-Sputtering System

After cleaned by chemicals, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive except Ni.) and Ni/Si were formed by an UHV-sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. It is performed by applying a high voltage across a low-pressure gas (usually argon at about 5 millitorr)to create a “plasma,” which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike a “target,” composed of the desired coating material, and cause atoms from that target to be ejected with enough energy to travel to, and bond with the substrate.

An UHV-sputtering system is used for thin film formations of

electronic devices, for experiments of GMR, and for creating new materials of high temperature superconductors. In this study, UHV Multi Target Sputtering System ES-350SU shown as Fig. 2-2 was conducted. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. As for other details, Table 2-1 is attached for reference.

Fig. 2-2 Photo of UHV Multi Target Sputtering System ES-350SU

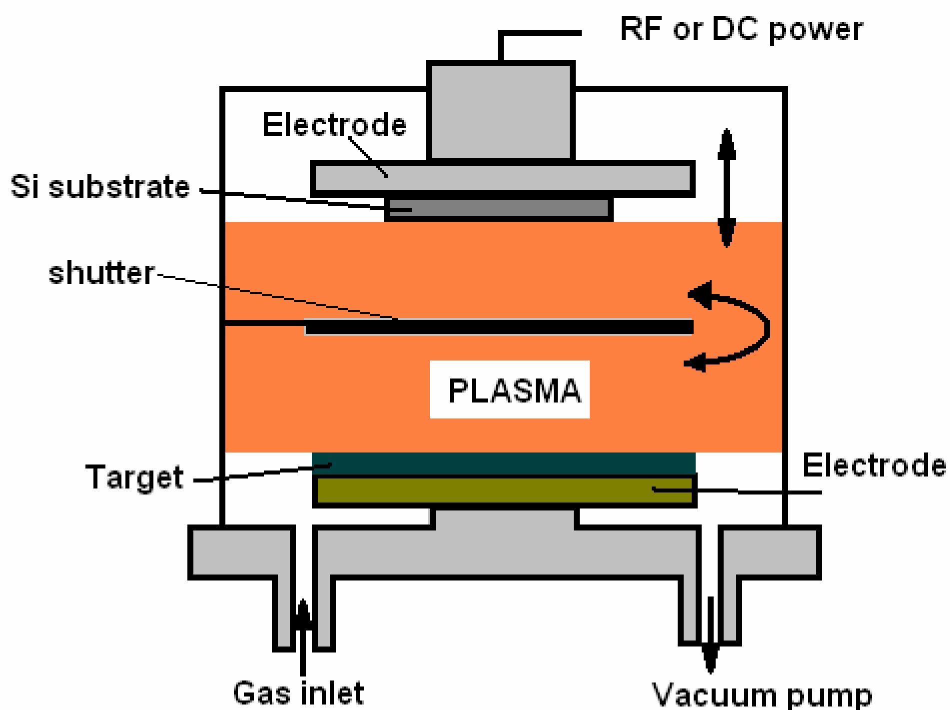


Fig. 2-3 structure of UHV sputtering system

Table 2-1 Specifications for UHV Multi Target Sputtering System ES-350SU

Growth chamber	1. Ultimate pressure	1.5 x 10^{-6}Pa
	2. Substrate size	2 inch in diameter
	3. Heating temperature	600ºC
	4. Heater type	Lamp type heater
	5. Target	3 inch x 5 pieces (motor-driven)
Load lock chamber	6. Vacuum pumps	TMP 500L/sec and RP 250L/min
	7.Ultimate pressure	6.6 x 10^{-5}Pa
	8. Vacuum pumps	TMP60L/sec and RP90L/min
	9. Substrate holder with cooling function / Substrate holder with heating function /Cleaning function / Radical beam source	

2.3 Infrared Annealing Furnace

After formation from UHV sputtering system, thin films of Ni/Si, Ni/M/Si, M/Ni/Si were moved to annealing furnace to hold thermal process.

In order to obtain high quality films, annealing process after deposition is required. The annealing after deposition is considered to bring the suppression of leakage current because of the defects in the films and surface roughness. In this study, thermal process leads to the reaction of Ni with Si.

The equipment for annealing used in this investigation was QHC-P610CP (ULVAC RIKO Co. Ltd). Fig. 2-4 is the photo of the infrared annealing furnace, whose schematic illustration was shown as Fig. 2-5. The annealing was performed by six infrared lamps surrounding the sample stage which were made of carbon and coated by SiC. The heating temperature was controlled by thermocouple feedback.

Fig. 2-4 Photo of infrared annealing furnace

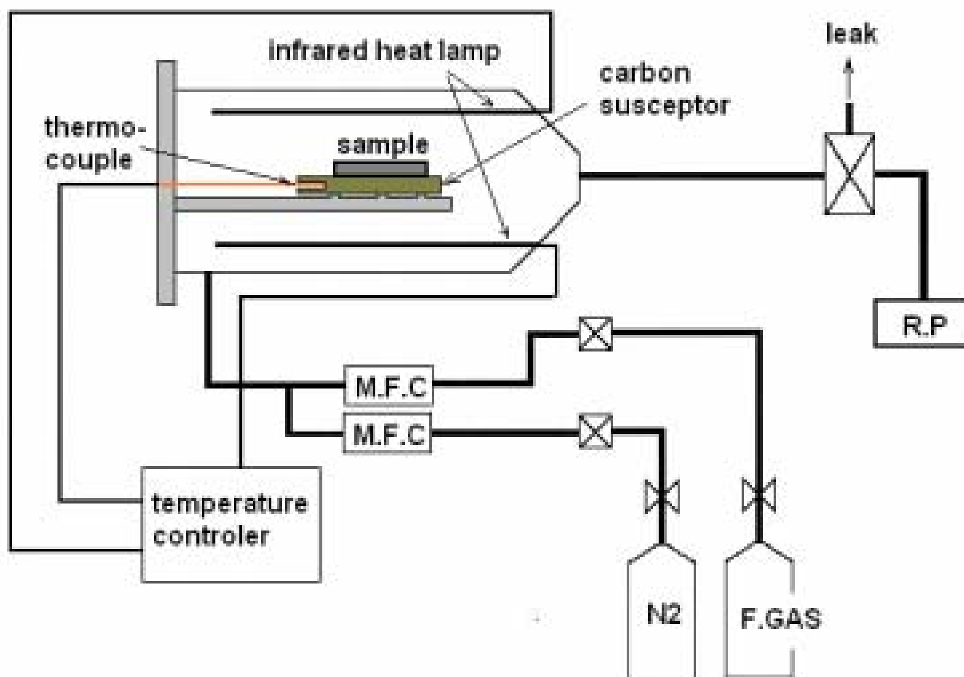


Fig. 2-5 schematic image of infrared annealing furnace

2.4 Four-point Probe Technique

The sheet resistance of Ni silicide was measured by four-point probe technique. The phase of Ni can be ascertained according to the sheet resistance of Ni silicide thin film, because the sheet resistance of $NiSi_2$ is greatly different from that of Ni monosilicide (NiSi) or other phase such as Ni_2Si.

The four-point probe technique is one of the most common methods for measuring the semiconductor resistivity because two-point probe method is difficult to interpret. The sheet resistance is calculated form potential difference between inside 2 terminals (between B probe and C probe) after applying the current between outside 2 terminals (between A probe and D probe) as shown in Fig.2-6. The resistance by two-probe technique is higher than accurate resistance because it includes the contact resistance (*Rc*) between metal probe and semiconductor surface and spreading resistance (*Rsp*) of each probe. Neither *Rc* nor *Rsp* can be accurately calculated so that semiconductor resistance (*Rs*) cannot be accurately extracted from the measured resistance. On the other hand, four-probe technique can neglect these parasitic resistances because the current value which flows between terminals is very small and potential drop can be disregarded. In this study, sheet resistance was measured by four-probe technique.

For an arbitrarily shaped sample the sheet resistance (ρ_{sh}) is given by

$$\rho_{sh} = \frac{V}{I} \times CF \qquad (2\text{-}1)$$

where *CF* is correction factor that depends on the sample geometry. If the

distance among probes (s; in this study, s=1 mm) is greatly shorter than the width of a sample (d), *CF* equals to π/ln(2)=4.53.

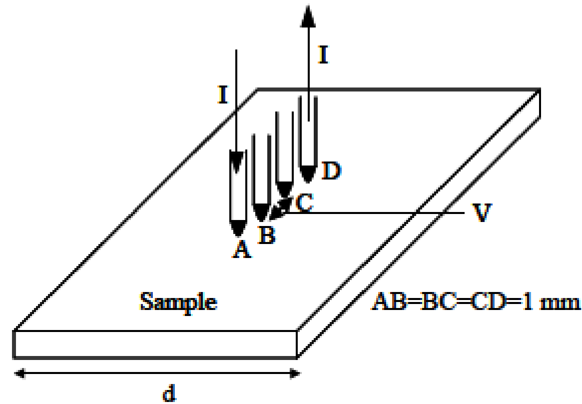


Fig. 2-6 illustration of four point probe system

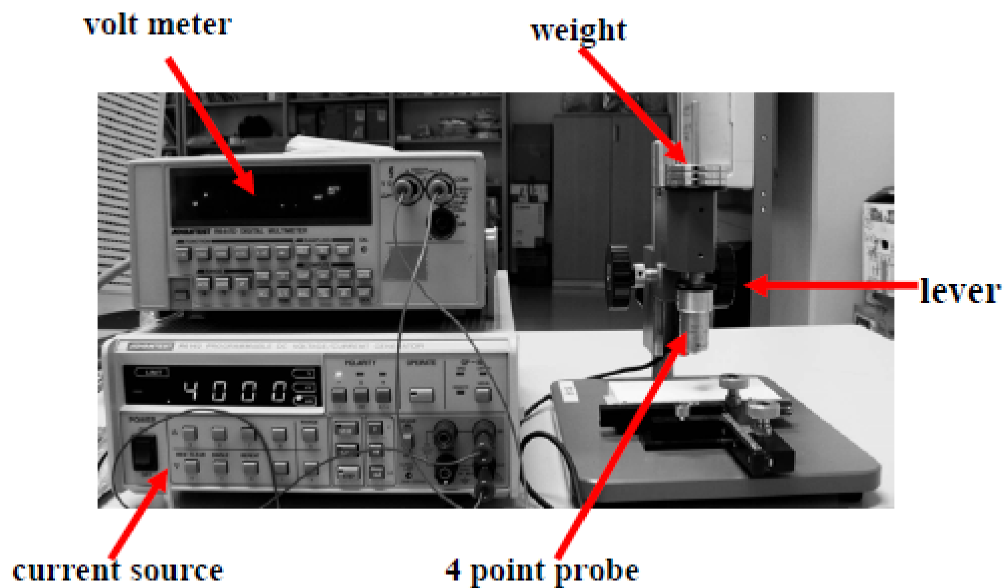


Fig. 2-7 Photo of four point probe system

2.5 Atomic Force Microscopy (AFM)

AFM enables to measure surface morphology by utilizing force between atoms and approached tip. The roughness of sample surface is observed precisely by measurement of x-y plane and z. Fig. 2-7 shows the principle of AFM. Tip is vibrated during measurement, and displacement of z direction is

detected. This method is called tapping mode AFM (TM-AFM). Resolution limit for normal AFM is 5~10nm depending on distance between surface and tip. On the other hand, resolution limit for TM-AFM is depended on size of tip edge. Thus, resolution limit for TM-AFM is about 1nm.

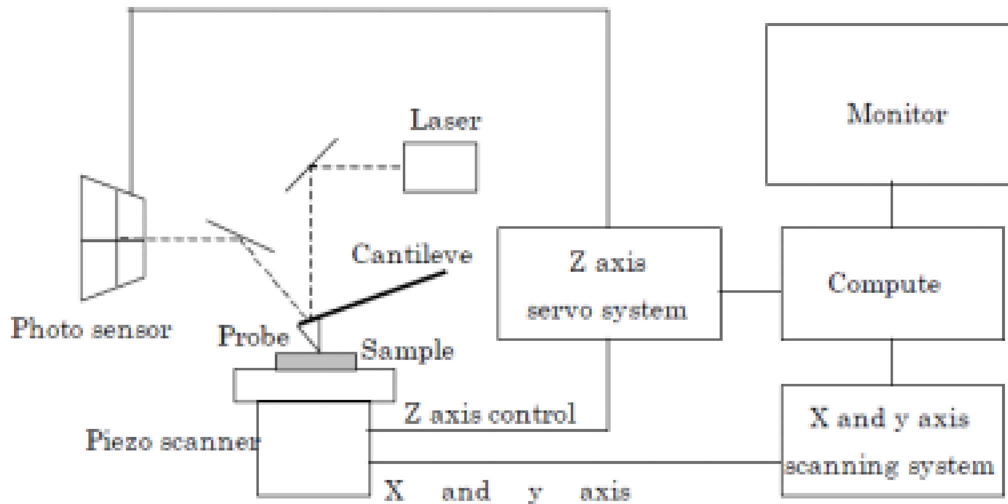


Fig. 2-7 Principle of AFM

2.6 X-ray Diffraction (XRD)

X-ray Diffraction (XRD) is a powerful non-destructive technique for characterizing crystalline materials. Figure 2-8 is a XRD instrument. It provides information on structures, phases, preferred crystal orientations (texture) and other structural parameters such as average grain size, crystallinity, strain and crystal defects. X-ray diffraction peaks are produced by constructive interference of monochromatic beam scattered from each set of lattice planes at specific angles. The peak intensities are determined by the atomic decoration within the lattice planes. Consequently, the X-ray diffraction pattern is the fingerprint of periodic atomic arrangements in a

given material. An on-line search of a standard database for X-ray powder diffraction pattern enables quick phase identification for a large variety of crystalline samples.

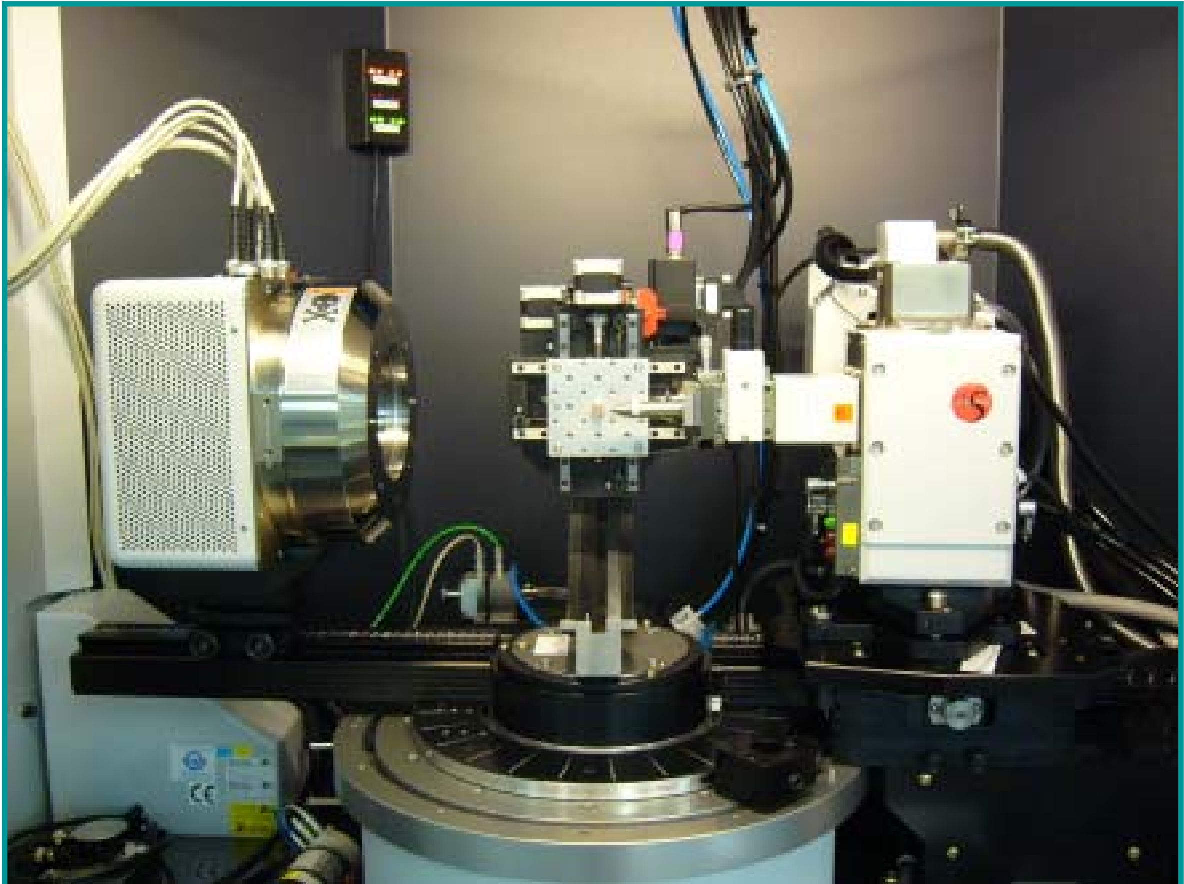


Fig. 2-8 Bruker D8 Discover

2.7 Rutherford Backscattering Spectroscopy (RBS)

Rutherford Backscattering Spectroscopy (RBS) is an analytical tool that gives very useful information regarding compositional and structural analysis of the films, as well as a precise measurement of the film's layer thickness.

As projectiles approach a target nucleus, strong repelling coulomb forces are acting. In the energy range that is used in our experiments (some 100 keV to some MeV) of the projectiles, the projectile and the nucleus don't get close enough so that the short range nuclear forces act. The scattering process can therefore be described as impact of two hard balls.

Using Rutherford back scattering as an analytical technique, one measures the energy of the backscattered particles. From the energy one can calculate the depth in which the scattering occurred. With known scattering geometry one can gain depth profile of the sample.

2.8 Auger Electron Spectroscopy

Auger Electron Spectroscopy (*Auger spectroscopy* or AES) was developed in the late 1960's, deriving its name from the effect first observed by Pierre Auger, a French Physicist, in the mid-1920's. It is a surface specific technique utilizing the emission of low energy electrons in the *Auger process* and is one of the most commonly employed surface analytical techniques for determining the composition of the surface layers of a sample.

2.9 Raman Spectroscopy

Raman spectroscopy is a method of chemical analysis that enables real-time reaction monitoring and characterization of compounds in a non-contact manner. The sample is illuminated with a laser and the scattered light is collected. The wavelengths and intensities of the scattered

light can be used to identify functional groups in a molecule. It has found wide application in the chemical, polymer, semiconductor, and pharmaceutical industries because of its high information content and ability to avoid sample contamination.

Chapter 3

EXPERIMENT RESULTS

3.1 Study of Experimental Conditions

The study of Ni silicide thermal stability was started from Jan. 2004. From the beginning, Lots of experiments were held to get better experimental conditions. In this subsection, deposition conditions for better thin film were introduced. At the same time, to control annealing temperature precisely, annealing furnace was remodeled.

3.1.1 Thin Film Deposition Conditions

3.1.1.1 Pre-sputtering Time

After cleaned by SPM and remove oxide by 1% Hf, Si substrate was moved to UHV sputtering system to deposit thin Ni film. To gain better quality of thin film, there were 3 minutes pre-sputtering. That was, the shutter between the target and samples was closed at the appearance of plasma for 3 minutes to avoid the instability of plasma at the beginning. Fig. 3-1 (b) is a photo of sputtering Ni with shutter open. Fig. 3-2 shows the photo of Ni/Si samples. Lots of blurs can be observed even with bare eyes. The sheet resistances of these samples were measured and list in Fig. 3-2. Tolerances were existed even in a same sample, which means that the thickness was different in position. This was supported by the RBS results shown in Fig. 3-3.

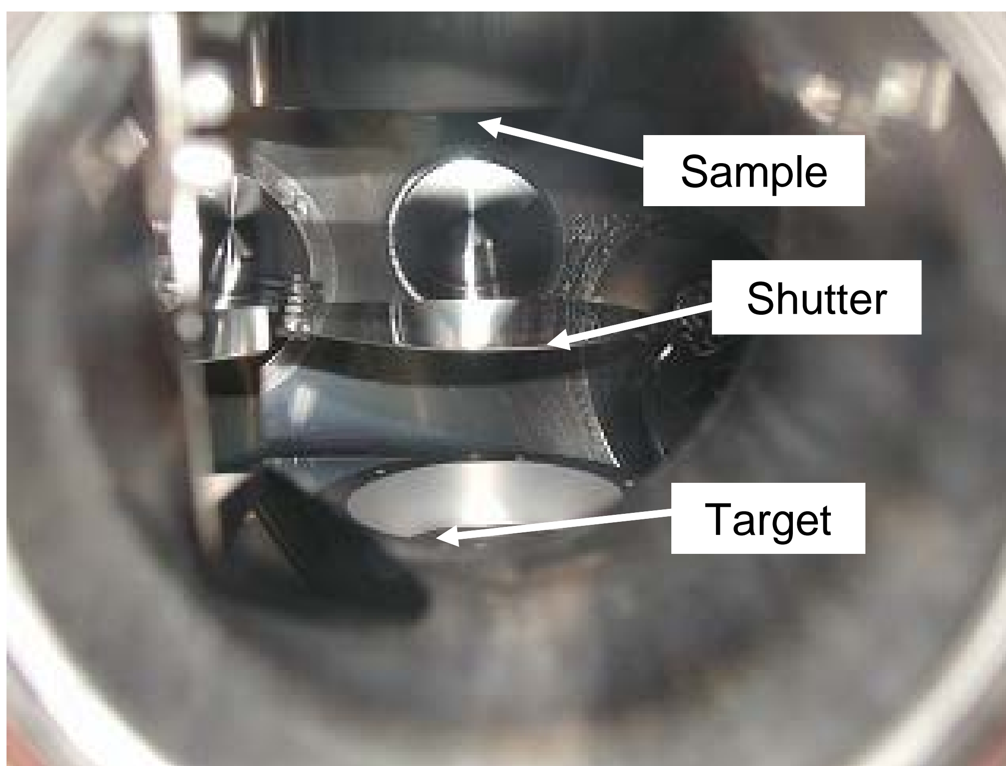


Fig. 3-1 (a) Structure of film growth chamber

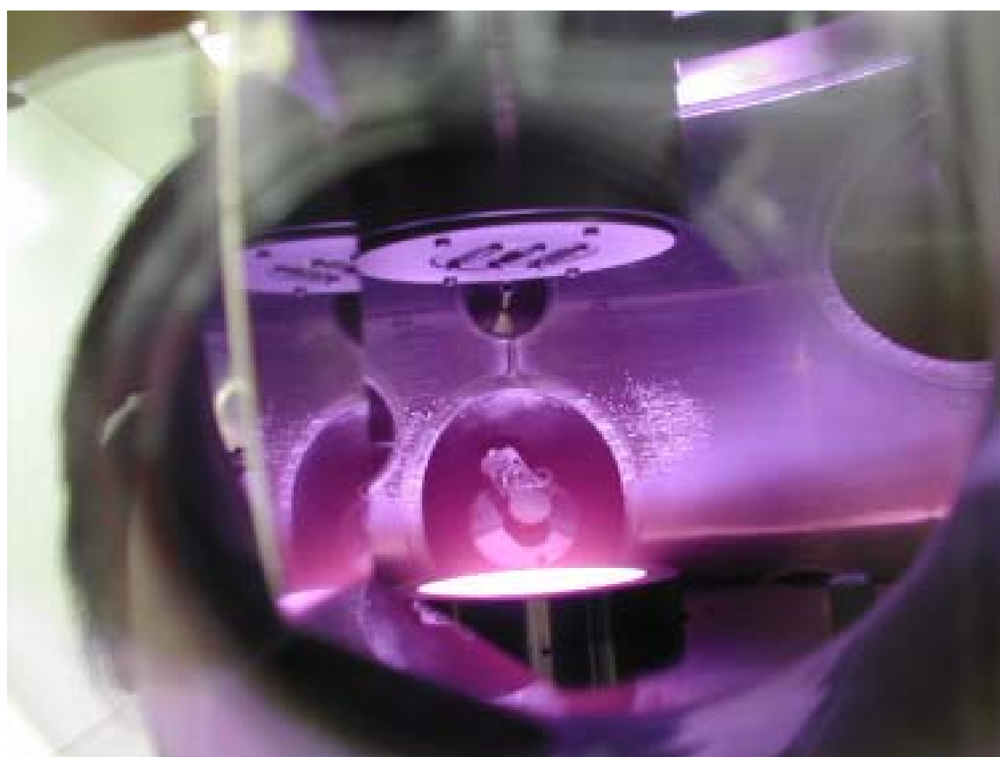


Fig. 3-1 (b) Photo of sputtering Ni

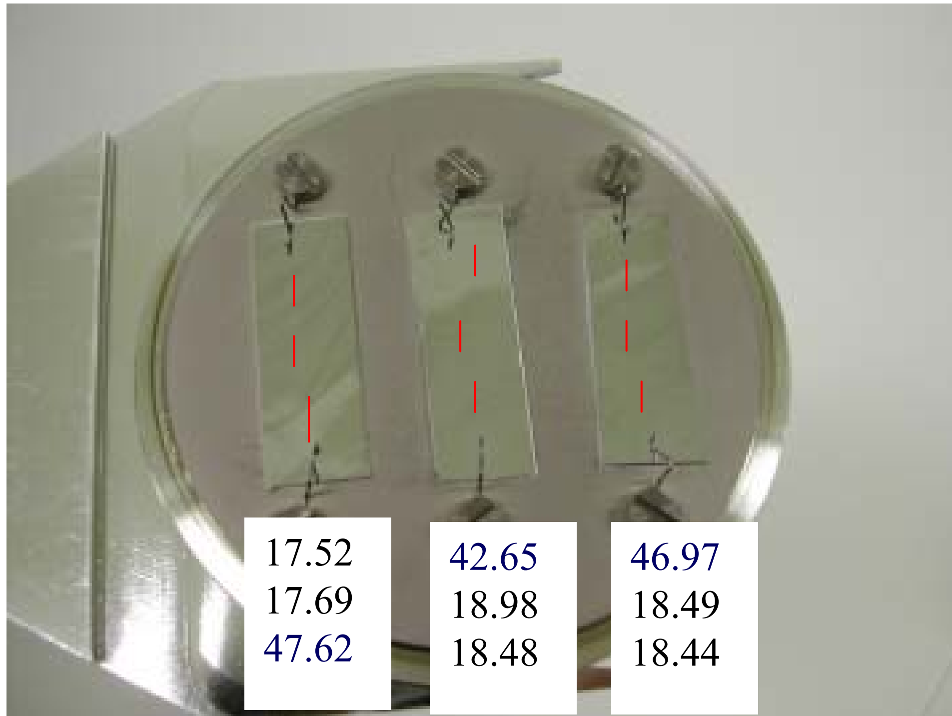


Fig. 3-2 Photo of Ni/Si samples (The straight lines marked in this figure were the positions of 4-point probe technique carried out, the values corresponding to those positions were list below.)

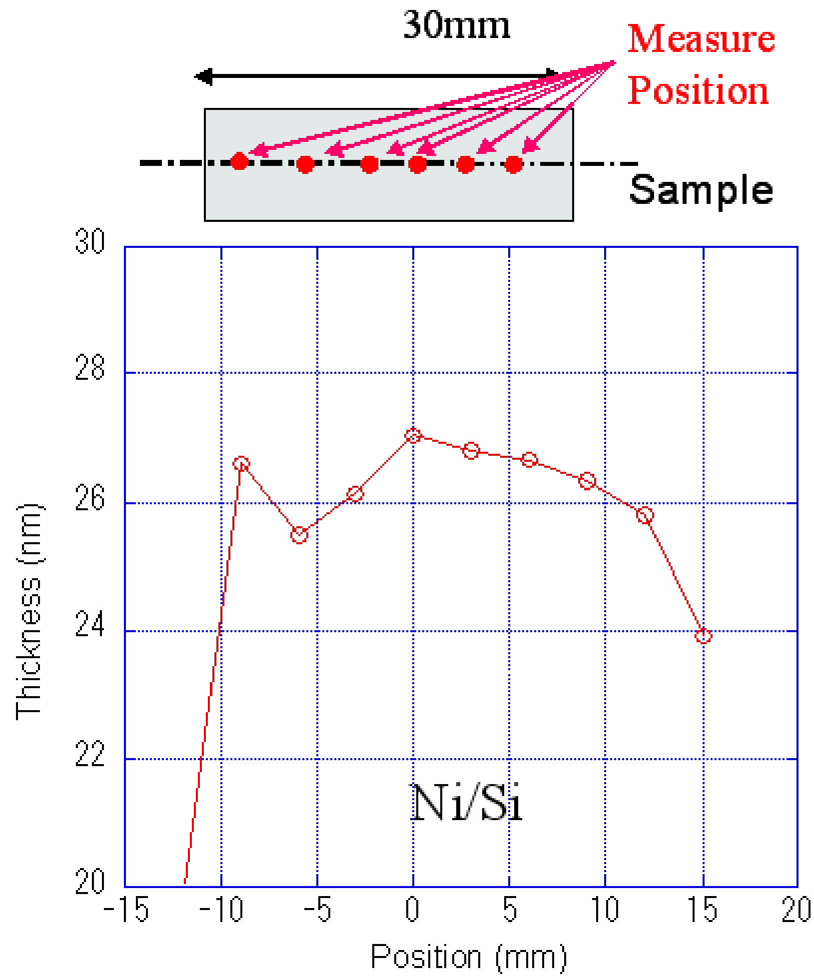


Fig. 3-3 RBS result of Ni/Si

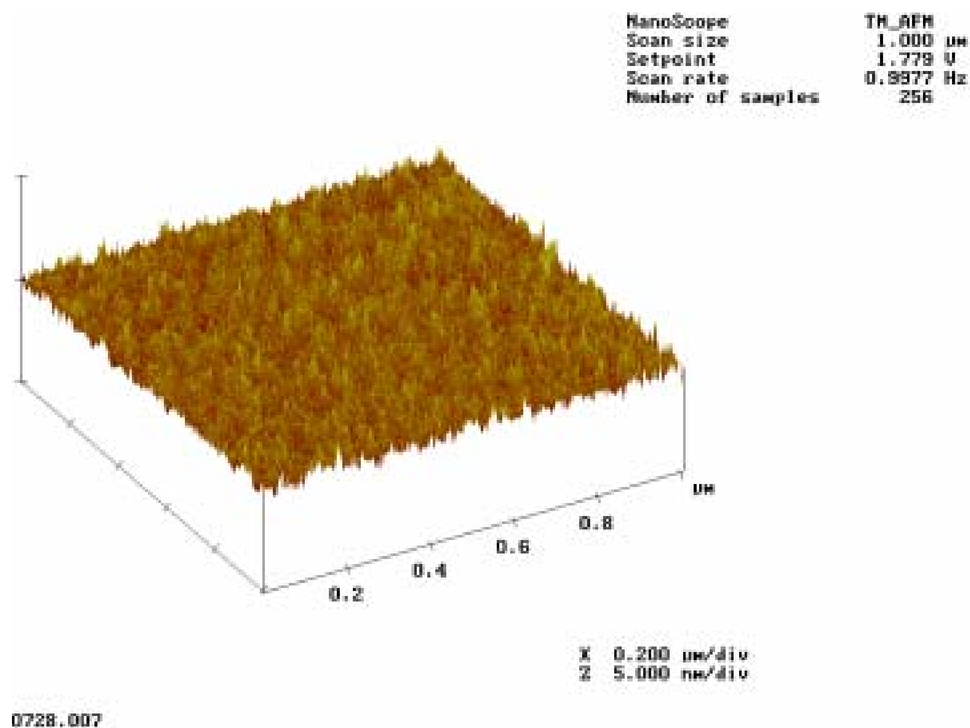
Further study revealed that 30-minute pre-sputter with shutter closed only can deposit 6.8 nm.

Experiments with shorter pre-sputter time, such as 30 seconds, showed that no blur was observed on the surface of thin film any longer. At the same time, the tolerance of sheet resistances in a same sample became reasonable (below several percentages).

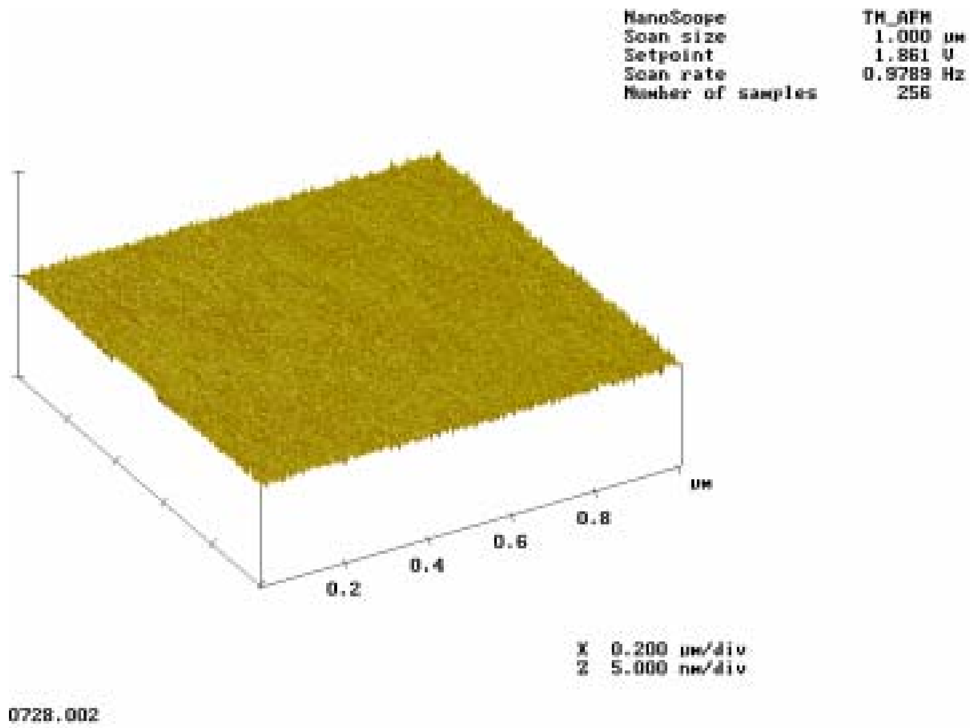
3.1.1.2 Gas Pressure during Deposition

Experiments were also carried out to investigate relation between thin film quality and gas pressure during film formation. Table 3-1 was the results under different Ar gas pressure. The thin film structure is Ni/p-(100)Si. All the experiments were held at same deposition condition expect the Ar gas pressure. The sputtering time of all the experiments was same. Under 0.48Pa, plasma was very difficult to occur. The gas pressure between 0.5Pa and 0.6Pa achieved lower roughness and tolerance in sheet resistance than that of 0.7Pa and 0.85 Pa.

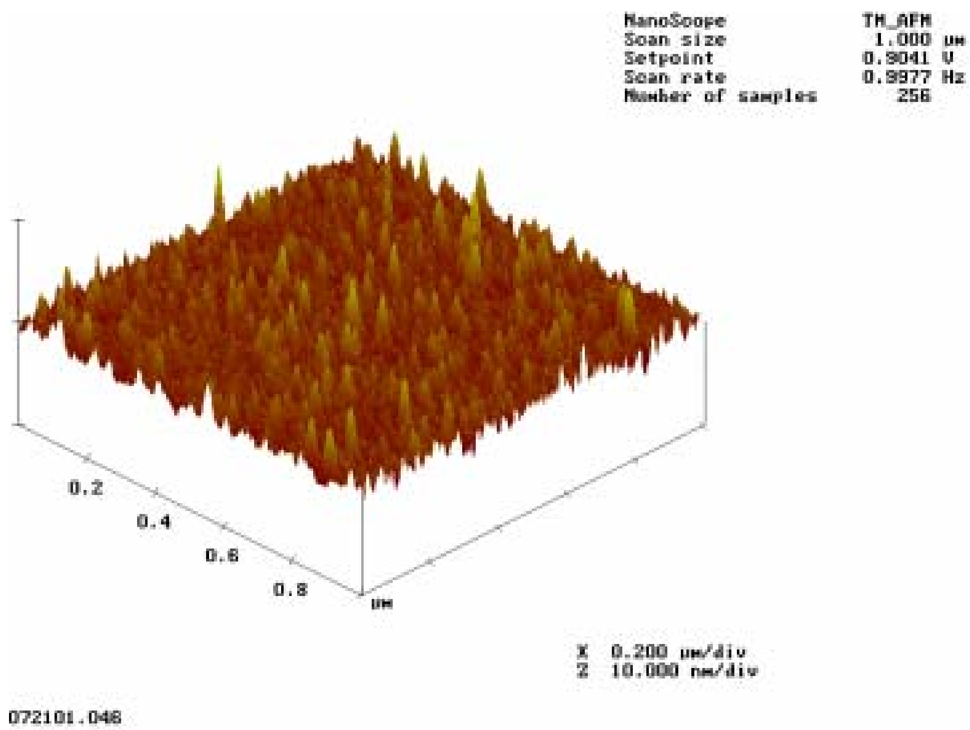
Ar gas pressure of 0.55Pa was adopted as one of the film formation conditions thereafter.



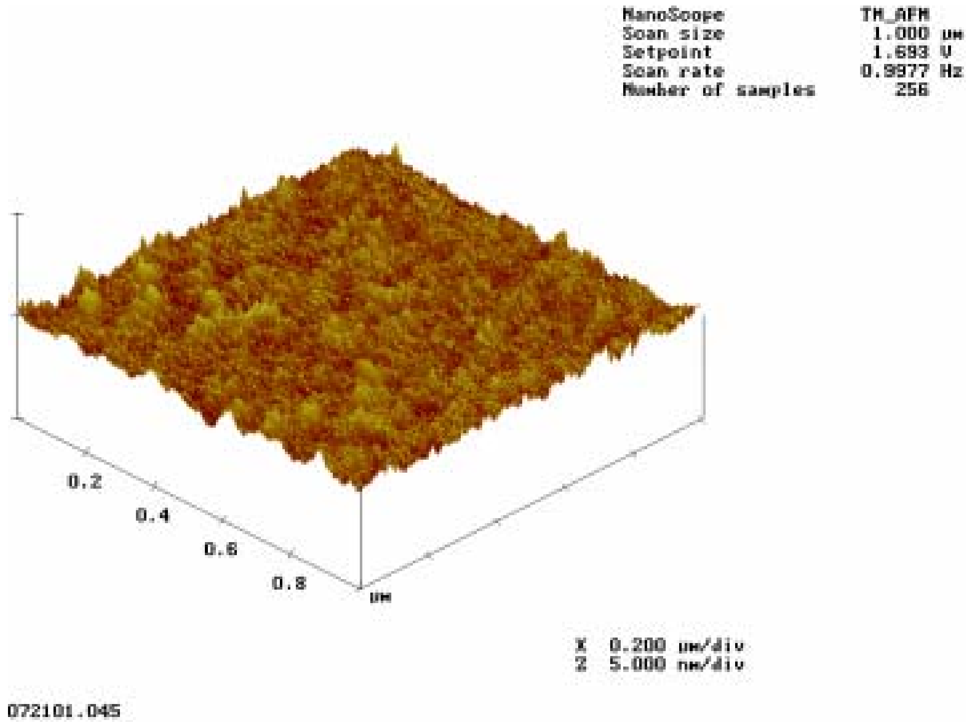
(a) 0.5Pa



(b)　0.6Pa



(c)　0.7Pa



(d) 0.85Pa

Fig. 3-4 AFM images of Ni/Si formed under Ar gas pressure of (a) 0.5Pa (b) 0.6Pa (c) 0.7Pa (d) 0.85Pa

Table 3-1 results of different Ar gas pressure

		Ar gas pressure (Pa)				
		0.48	0.5	0.6	0.7	0.85
Ni thickness (nm)		1.07	11.12	11	10.41	10.05
sheet resistance	Ideal value (ohm/sq.)		6.21	6.27	6.63	6.87
	Measurement value(ohm/sq.)	139.33 ±7.43	22.39 ±0.2	27.02 ±0.15	28.21 ±0.34	36.15 ±4.46
ideal value/measurement value			3.61	4.31	4.26	5.27
mean roughness (nm)			0.44	0.407	0.66	0.646

Note: 1. Ni thickness was obtained from measurement of XRF (X-ray fluorescence spectroscopy).

2. The structure of thin film was Ni/p-(100)Si without annealing process.

3. Resistivity of Ni is 6.9µΩcm@25°C.

4. Ideal value of sheet resistance is obtained from the resistivity of Ni over Ni thickness.

3.1.2 Remodeling of Annealing Furnace

In order to make annealing temperature accurate, the carbon susceptor was moved out of the furnace and the thermo-couple floated in the air as shown in Fig. 3-5. To test the feasibility of this structure, experiment was carried out as below.

In this experiment, n-type (100)Si wafers were used for substrates. After the substrates were chemically cleaned by SPM and diluted HF treatments, Ni layer was deposited on the substrates using the UHV-sputtering system mentioned above. After 25nm Ni film was formed under Ar gas pressure of 0.55Pa, annealing process was held at various temperatures in forming gas (3%-H_2) ambient using a RTA system. Any chemical etching was not performed after the annealing. Characteristic of annealing temperature versus sheet resistance was shown in Fig. 3-6.

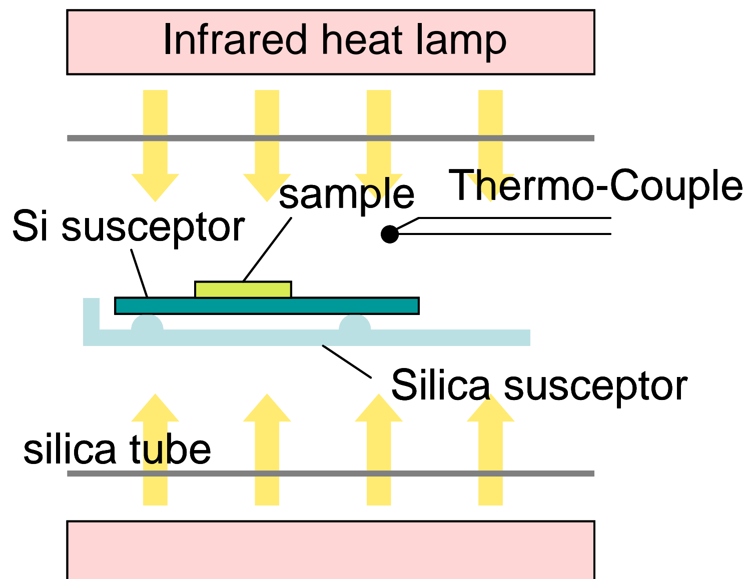


Fig. 3-5 Illustration of remodeled annealing furnace

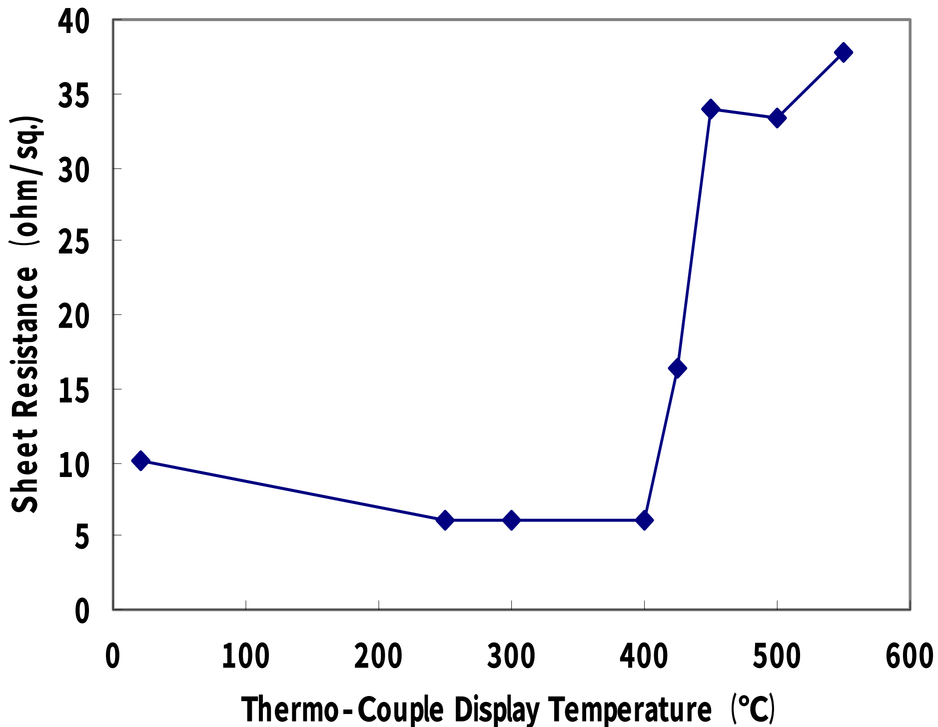
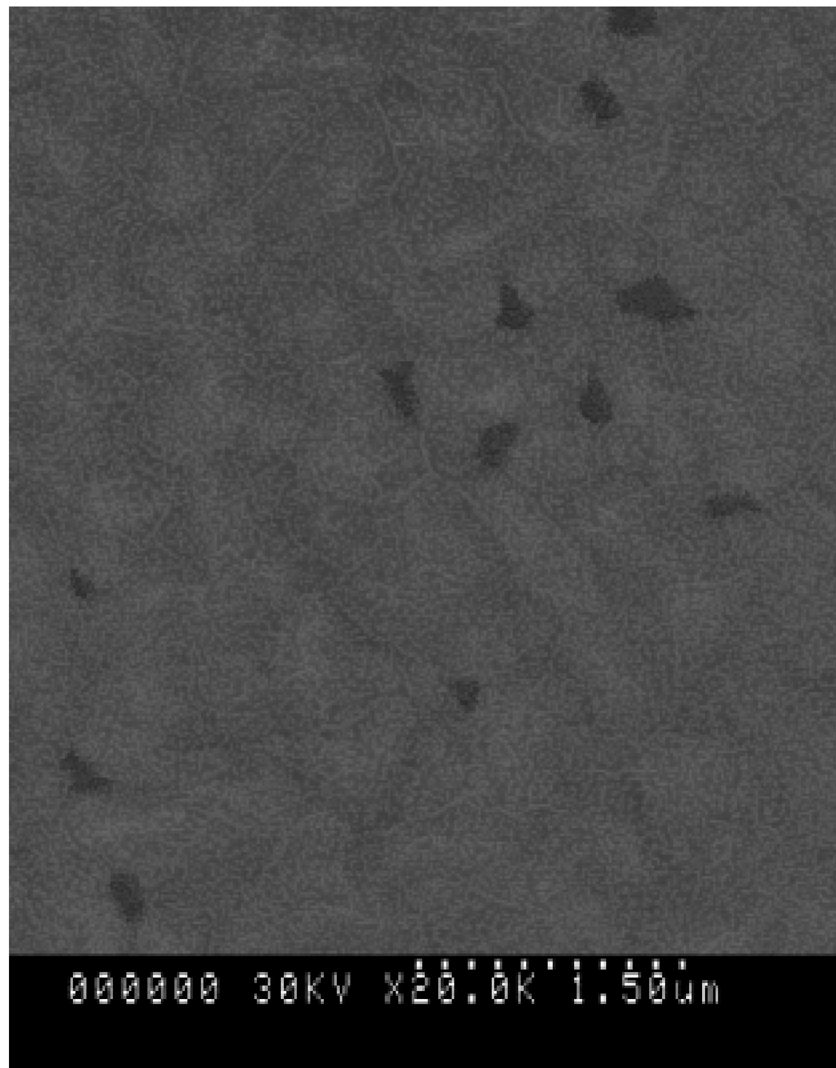


Fig.3-6 annealing temperature versus sheet resistance of Ni(25nm)/n-(100)Si in forming gas ambient for 60 seconds by a RTA system

Fig. 3-6 shows Ni silicide was very thermal instable. The sheet resistance began to increase dramatically at temperature of 400°C. Ni phase at low sheet resistance region or 250-400 °C maybe NiSi and NiSi2 may appear at high sheet resistance region or above 450 °C. There are some strange points in Fig. 3-6.The first one was that the sheet resistance of Ni silicide would increased at around annealing temperate of 700°C according to references[5-29]. The second one was that the resistivity of NiSi and NiSi2 was 10.5-15 μΩcm and 34 μΩcm respectively according to Table 1-1. In other word, the resistivity of NiSi2 is about 2-3 times of NiSi. This was not consistent with Fig. 3-6.

The surface images of annealing temperature at 400 °C or low sheet resistance region, 450 °C or high sheet resistance region were shown in Fig. 3-7. Agglomeration occurred even in the low sheet resistance region. The thin film was not continuous at 450 °C any longer.



(a) 400 °C

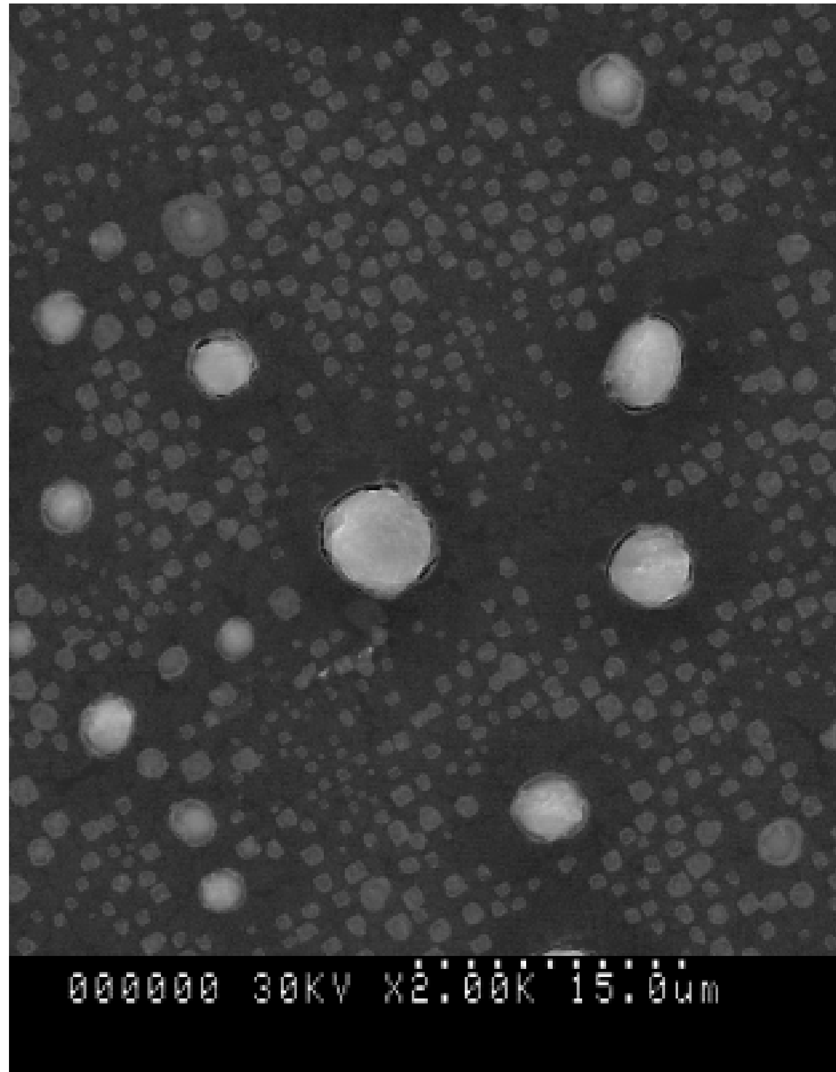


Fig. 3-7 SEM Images of Ni(25)/n-Si after RTA at temperature of
(a) 400°C or low sheet resistance region
(b) 450°C or high sheet resistance region

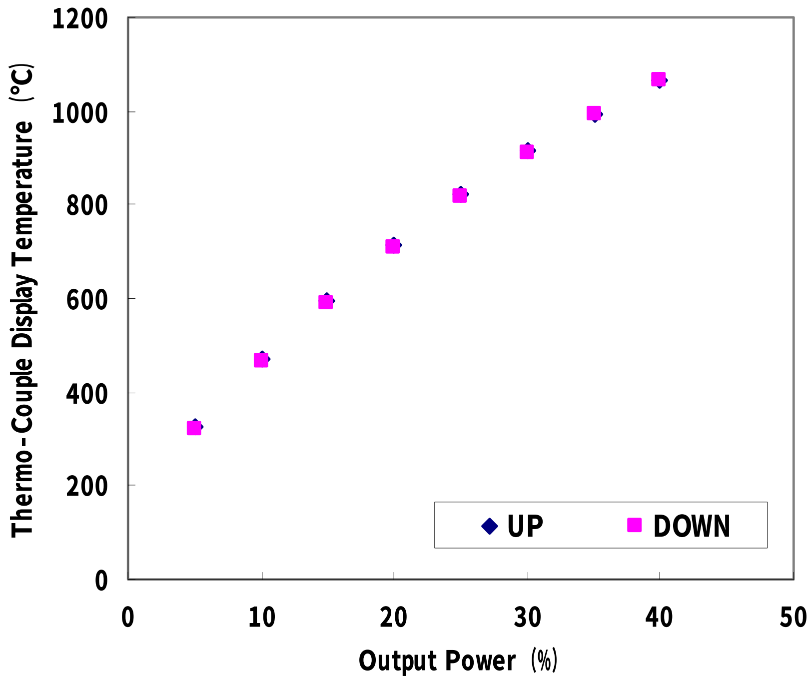
The above experiment relieved that remodeling annealing furnace had not a good control of temperature. The thermo-couple displayed temperature was not actual annealing temperature. Correction in the thermo-couple displayed temperature was necessary.

Fig. 3-8 was the results of temperature correction experiment. Here

UP curve and DOWN curve were stood for temperature increase, temperature decrease respectively. There was not different between UP curve and DOWN curve shown as Fig. (a) and Fig.(b) of Fig. 3-8. Fig. 3-9 was deferred from the combination of Figure (a) and Figure (b). This figure relieved the relationship as approximation curve y=1.22x. So, the critical temperature where the sheet resistance of Ni silicide increased rapidly in Fig.3-6 became 480 ^{o}C. But, this temperature was still far lower than that of reference.

Here another susceptor adhered to thermo-couple (here shorten as susceptor TC thereafter) was inserted into annealing furnace shown as Fig. 3-10. One other temperature display unite was conducted to connect with susceptor TC. By comparing the displayed temperatures of Upper thermo-couple (or TC) and susceptor TC, it was found that there was 197.8 ^{o}C difference shown as Fig. 3-11.

All temperatures thereafter were referred to the displayed temperature connected to the susceptor TC.



(a) Characteristic of thermo-couple display temperature versus output power at the presence of carbon susceptor

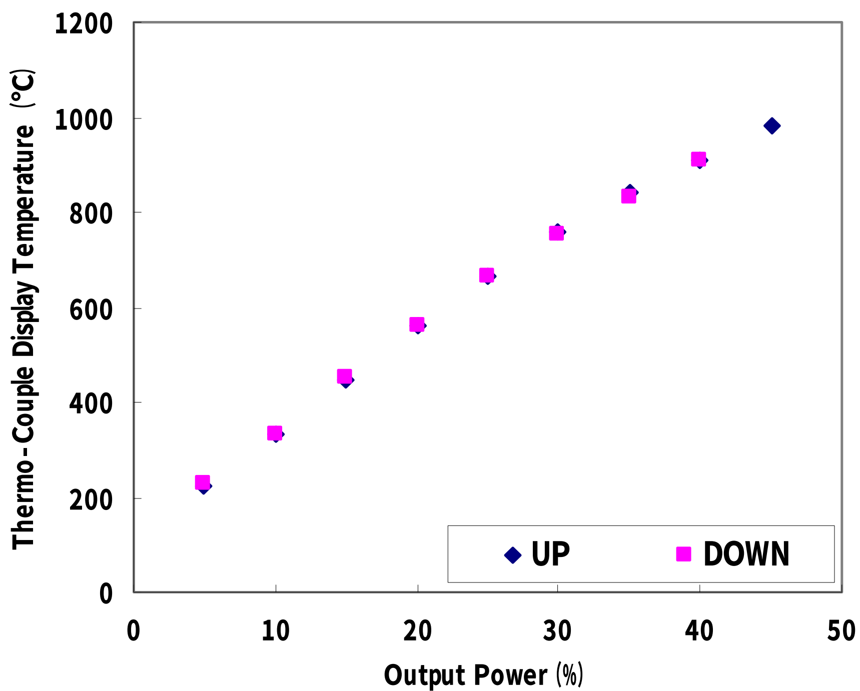


Fig. 3-8 Characteristic of thermo-couple display temperature vs. output power
(a) at the presence of carbon susceptor (b) at the absence of carbon susceptor

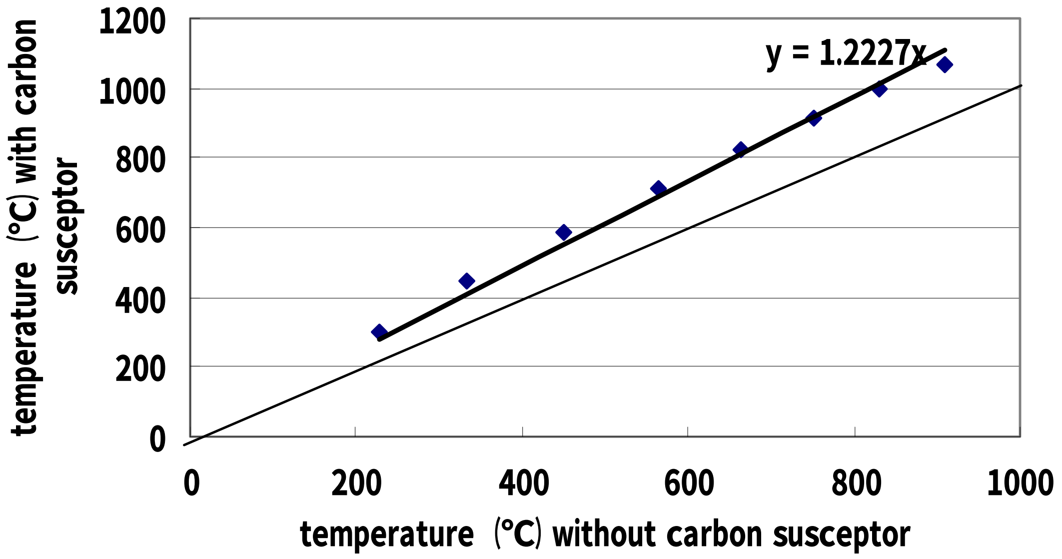
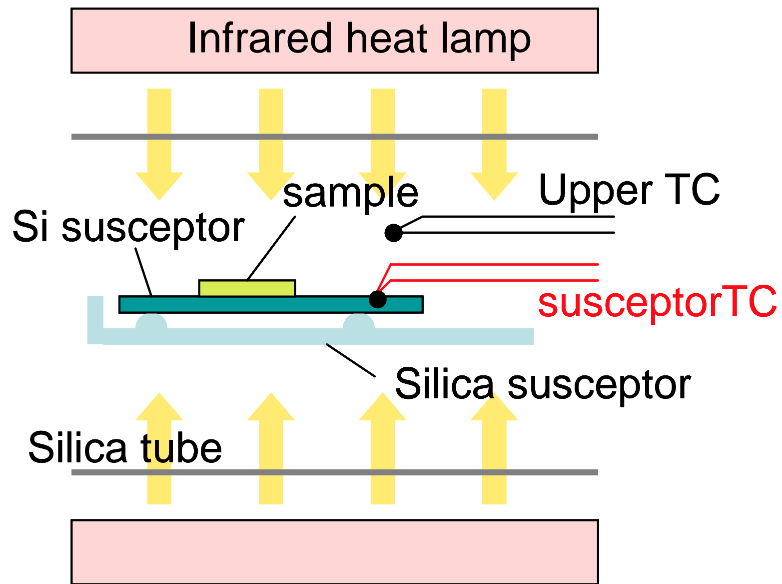
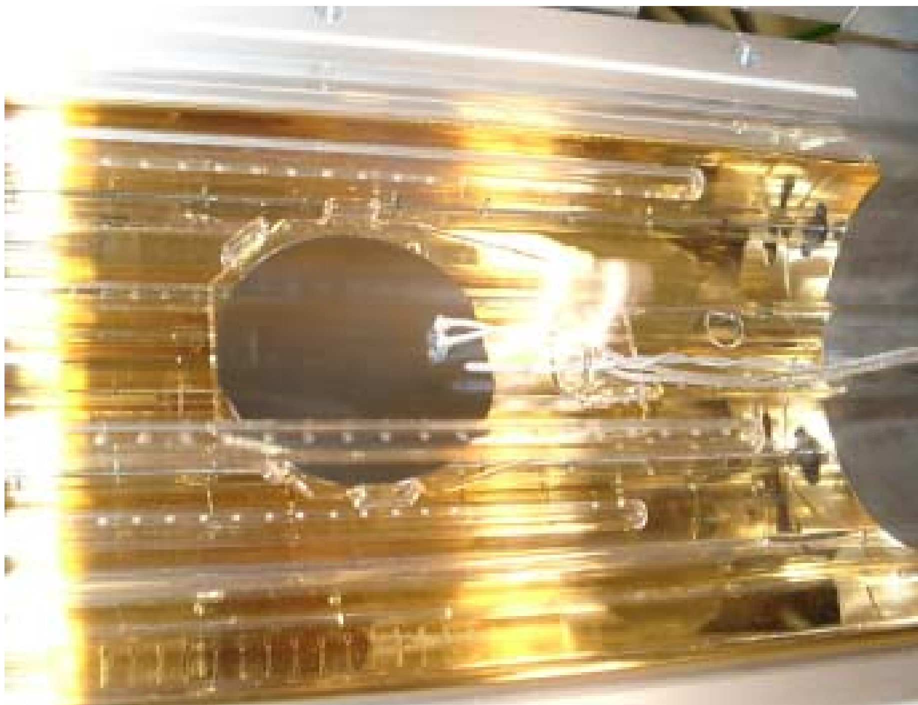


Fig. 3-9 Correction temperature between the absence of carbon susceptor and the presence of carbon susceptor



(a) Illustration of welded Si susceptor



(b) Photo of annealing furnace after remodeled

Fig. 3-10 thermo-couple was welded to Si susceptor

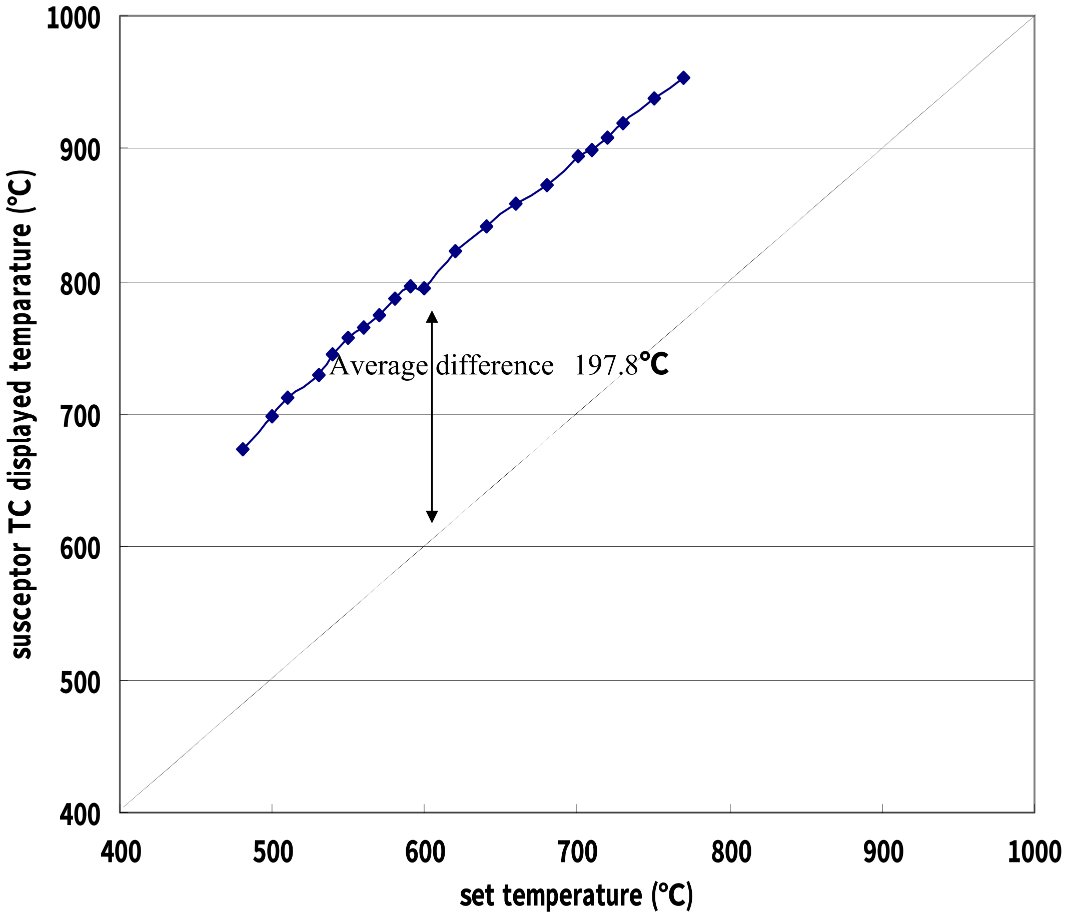


Fig. 3-11 relationship of set temperature (or the displayed temperature of upper TC) and susceptor TC displayed temperature

3. 2 Experimental Results

In this subsection, Ni silicide with metal additives such as Pt, Hf, V, Pd, Ru, and Ti were systematically studied with two different experiment methods. Based on different deposition of thin film, two experiment methods were separated. The first one was conventional bi-layer deposition and the second one was the new "post-silincidation doping" method as shown in Fig. 3-12. Here "M" was different metal additives.

The total thickness of thin film in all these experiments was kept constant, 12nm. The thickness of "M" (metal additives) was a function. Different thicknesses of Metal additives were examined to gain the best effect to Ni thermal stability.

As for thermal process, all these samples were held in Forming Gas (N_2:H_2=97:3) with same temperature profile.

In the end, Electrical characteristics were measured by 4-piont probe technique and surface morphology was analyzed by such as TEM, AFM, XRD, Raman Spectroscopy etc.

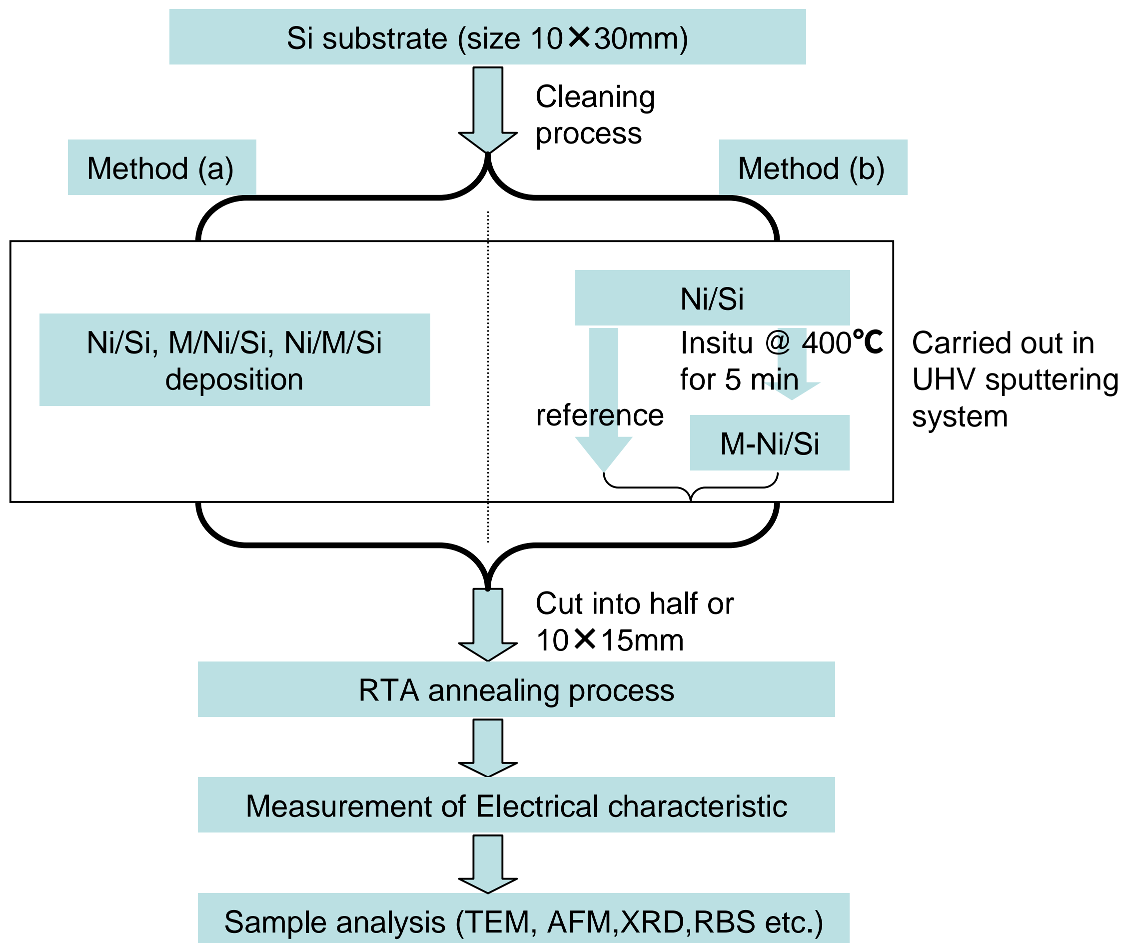


Fig. 3-21 experiment method: (a) conventional bi-layer deposition, (b) post-silincidation doping. Here M was different metal additives.

3.2.1 Conventional bi-layer Deposition

In these experiments, p-type Si(100) wafers were used for substrates. After the substrates were chemically cleaned by SPM and diluted HF treatments, Ni layer was deposited on the substrates using the UHV-sputtering system mentioned in Fig. 2-2. Various thin film structures such as M/Ni/Si, Ni/M/Si samples was formed under Ar gas pressure of 0.55Pa. To make a comparison, Ni/Si samples was also prepared at same sputtering condition. Then, annealing process was held at various

temperatures in forming gas (3%-H_2) ambient for 60 seconds using a RTA system with heating rate of 10°C/sec.

Any chemical etching was not performed after the annealing.

3.2.1.1 Thermal Stability of Pure Ni Silicide

At first, pure Ni(12nm) thin film was investigated. The result was shown in Fig. 3-13, whose annealing temperature ranged from 200 to 950°C at interval of 25°C. This figure could be divided into 5 stages according to the change in sheet resistance. The first one was the region from 200 to 300°C at which the main Ni phase was Ni_2Si according to the XRD analysis of Fig.3-16. The second one which exhibited both the lowest and constant sheet resistance was the region form 300 to 700°C at which the Ni phase was NiSi or Ni silicide, which was also supported by Raman Spectroscopy measurement result as shown in Fig. 3-17. The third one was the region from 700 to 750°C where NiSi was on the way to transform to $NiSi_2$. The reason why no $NiSi_2$ peak was observed neither in Fig. 3-15 nor in Fig. 3-17 above the temperature of 700°C was probably the signal corresponding to $NiSi_2$ phase is too weak to detect. So, NiSi and $NiSi_2$ must be coexisted in this temperature region and the sheet resistance kept increasing because more and more $NiSi_2$ created. The forth one was the region from about 750 to 925°C where the main phase was $NiSi_2$ which was a high resistivity material. At this temperature region, pyramid structures were observed according to Figure 3-14 and became large in shape with temperature. The last one was the region above 925°C where the thin film was not continuous any more and

sheet resistance increased dramatically.

After annealing process, these samples were measured by AFM. Surface morphologies relieved that sheet resistance and corresponding surface roughness were in proportion. That was, agglomeration of thin film was also the reason caused high sheet resistance.

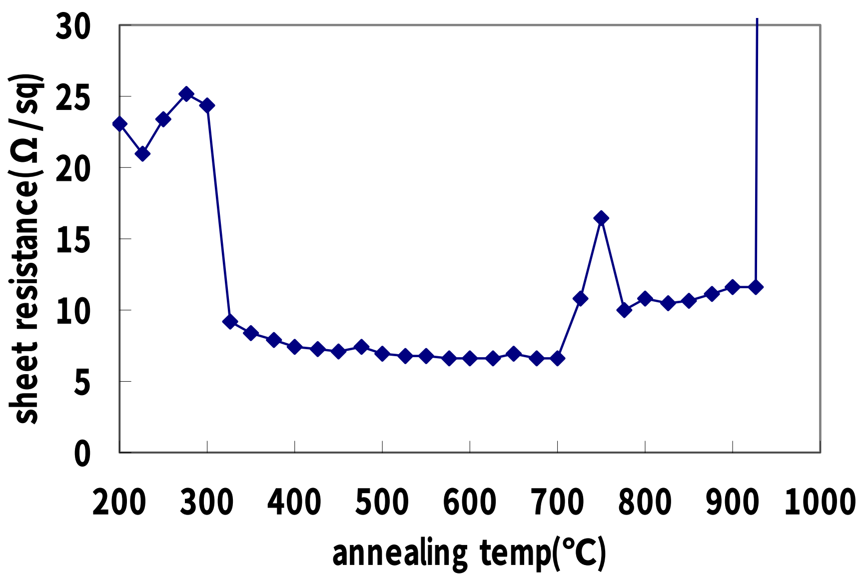


Fig. 3-13 Characteristic of annealing temperature versus sheet resistance of Ni (12nm)/p-(100) Si.

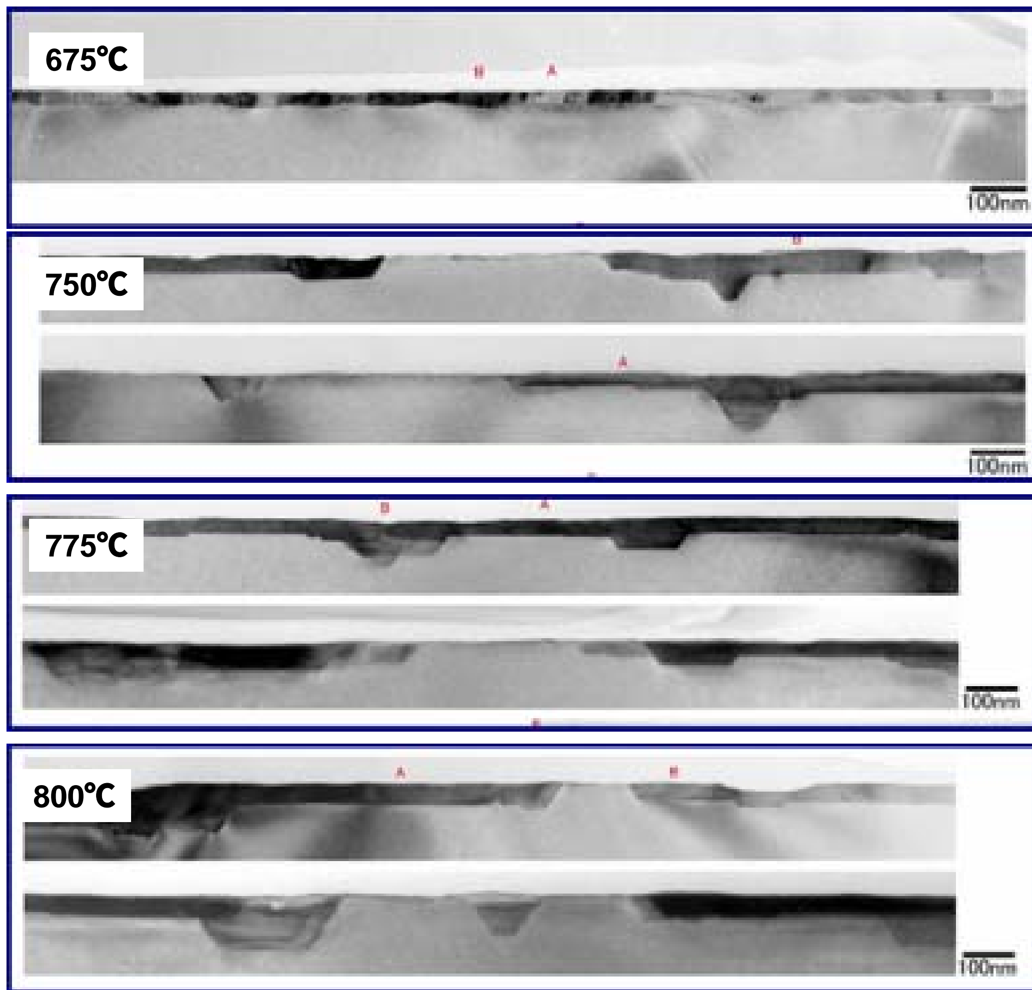


Fig. 3-14 cross sectional TEM images of pure Ni(12nm)/p-(100)Si formed by conventional bi-layer method after RTA at 675°C (or low resistance region),750°C (or resistance peak), 775°C (or high resistance region),800°C (also high resistance region).

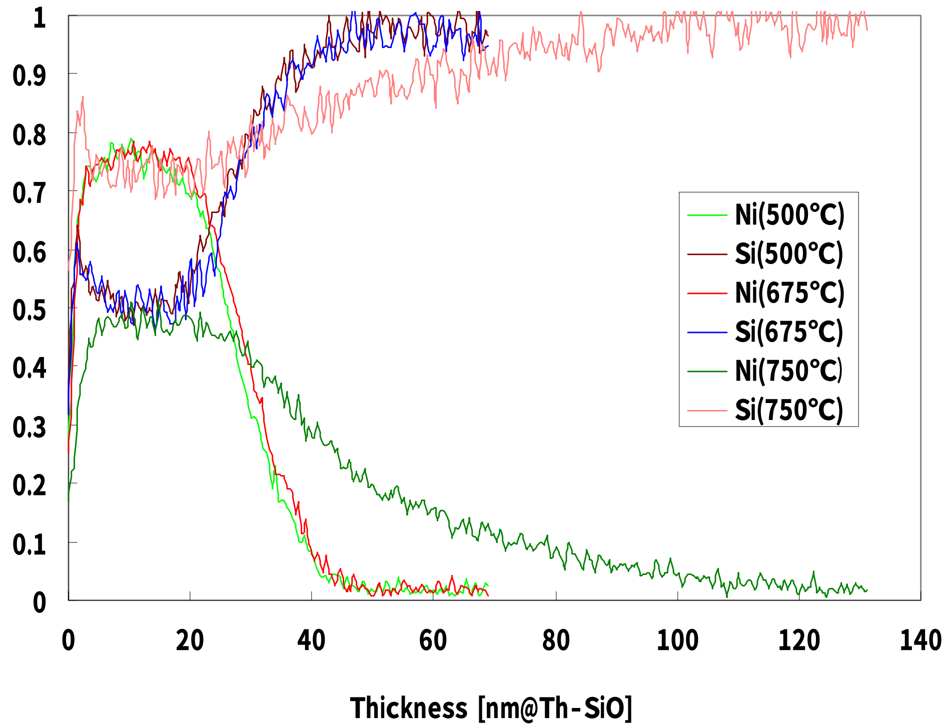


Fig. 3-15 Auger observatory results

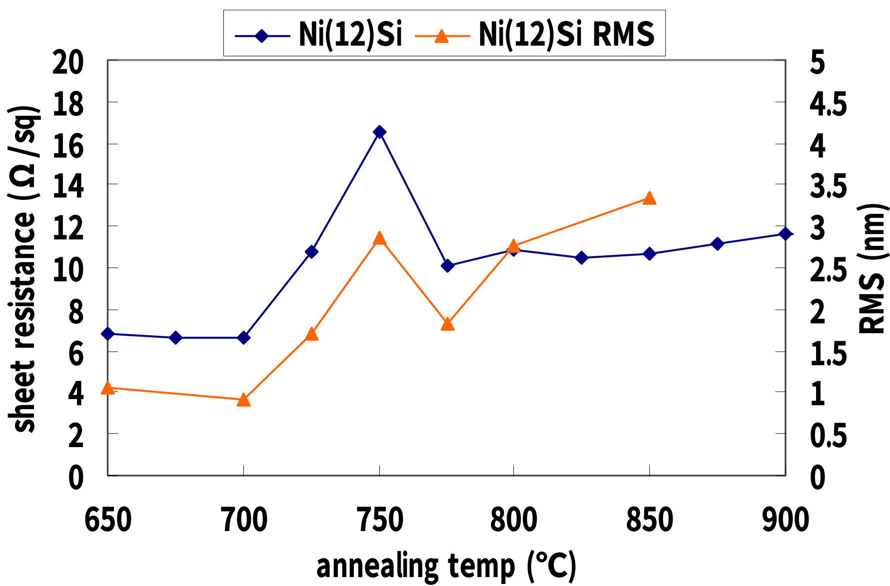


Fig. 3-16 Characteristic of annealing temperature versus sheet resistance and corresponding roughness

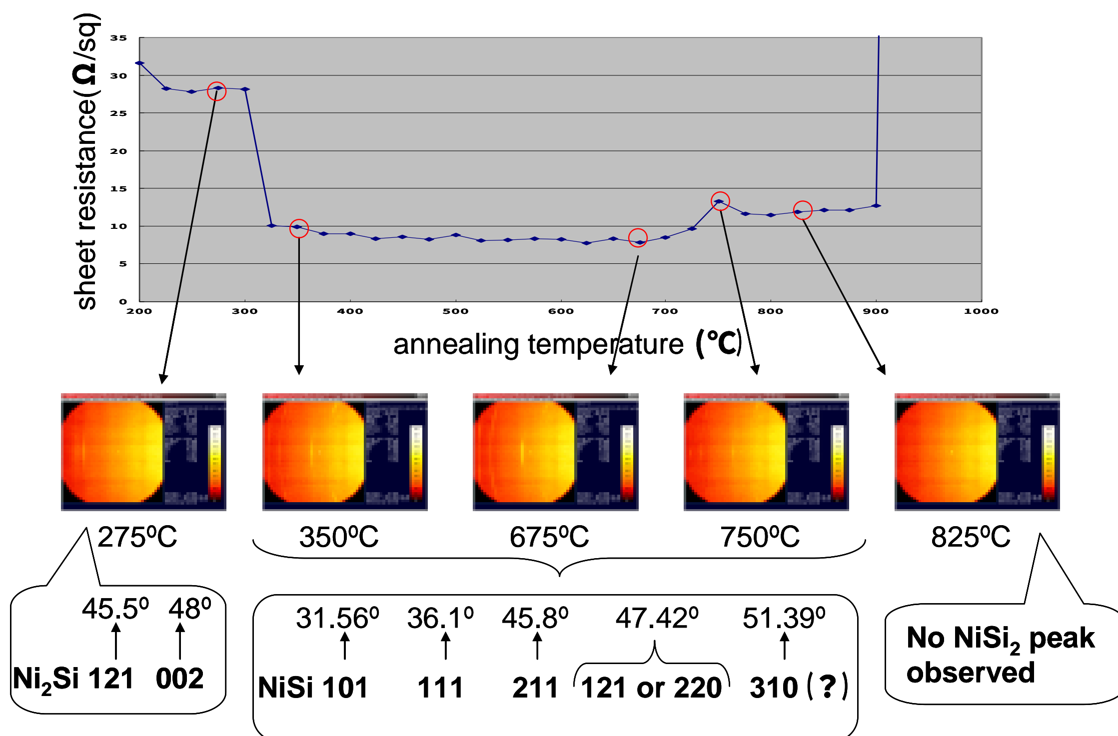


Fig. 3-17 XRD measurement results

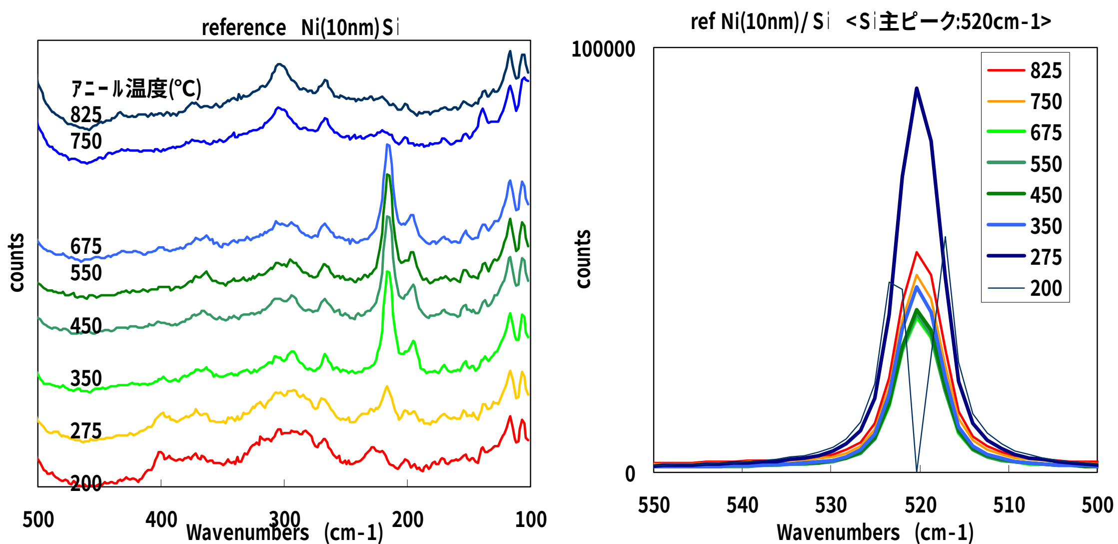


Fig. 3-18 Raman Spectroscopy measurement result
(NiSi peak: about 220cm^{-1}, Si peak: 520cm^{-1})

It was noticed that the sheet resistance for $NiSi_2$ phase, corresponding to 775-900°C region, showed lower resistance than that of the peak resistance at 750°C, in spite of passing through the critical temperature of 750°C.

To get the reliability of the sheet resistance peak, Ni thin film with different thicknesses of 10nm, 12nm, 14, and 25nm was examined. Fig. 3-19 shows that the phenomenon existed among all of these samples after annealing process. However, as for the annealing temperature which sheet resistance peak appeared, Ni(25nm)/Si was 50°C higher than Ni(10nm)/Si, Ni(12)/Si, and Ni(14nm)/Si. In other word, the thermal stability of Ni thin film became strong with increase of thickness.

In order to investigate the condition for appearance of the irregular resistance peak, we examined various temperature profiles in the RTA as shown in Fig. 3-20. The results are summarized in Fig. 3-21. It was found that the two-step annealing, as shown in dotted line in Fig.3-20, resulted in high sheet resistance close to the peak resistance (No.3 in Figs. 3-20 and 3-21). This means that the rough structure formed at 750°C for 60 sec could not be recovered by the following higher temperature annealing. Therefore, the fact that the single step RTA at higher temperature exhibited lower resistances indicates that the agglomeration occurred in the phase transition region should be suppressed if the time to through the critical temperature region in which the agglomeration occurs is short enough. So, we examined slow ramping rate around the critical temperature region. The result showed that even for the slowest case, 0.1°C/sec, the resistance was lower as shown in Fig.3-21 (No.5).

Figure 3-22 shows the sheet resistance as a function of duration time of RTA at 750°C in the single step RTA. It was found that it took 30-40 seconds to increase the resistance obviously. This time is corresponding to the temperature range of the critical temperature region is only 3-4°C in the case of 0.1°C/sec ramping rate. The temperature region seems to be too narrow. The other possibility is that the appearance of the high resistance is depending not on ramping rate for just passing the critical temperature but on that before reaching there (<750 °C). The relatively long time annealing below 750°C can contribute to suppress the agglomeration in the transition region.

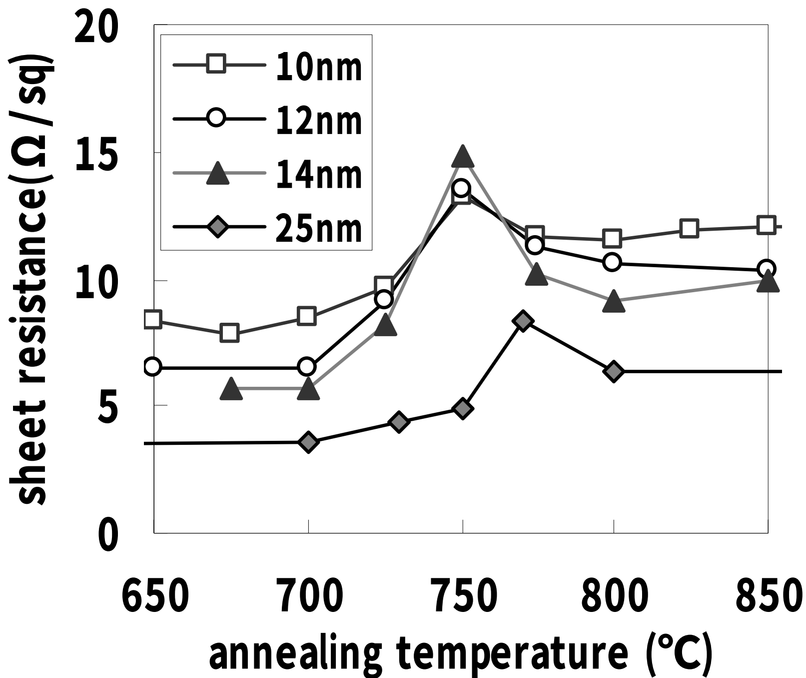


Fig. 3-19 Characteristics of annealing temperature vs. sheet resistance of NiSi with thicknesses of 10nm, 12nm, 14nm and 25nm

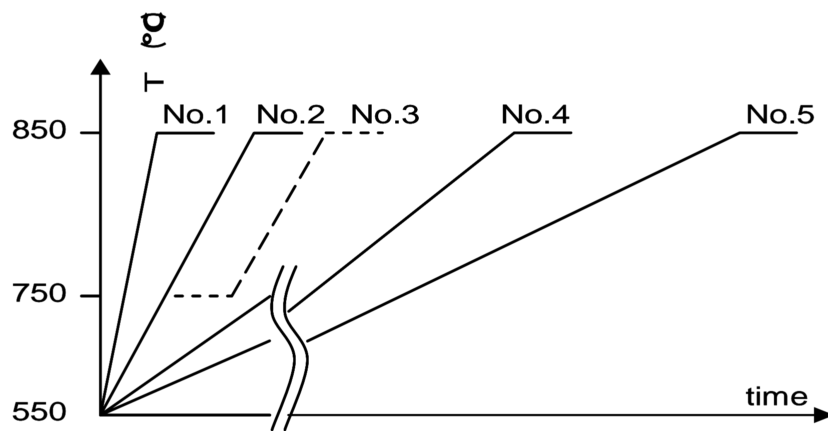


Fig. 3-20 Schematic of temperature profiles in RTA. Single step at 850°C for 60 sec-duration with ramping rate over 550°C of

No.1: 20°C/s No.2: 10°C/s

No.4: 0.4°C/s No.5: 0. 1°C/sec,

and two-step, No.3, at 750°C and 850°C for 60sec-duration each with ramping rate of 10°C/s.

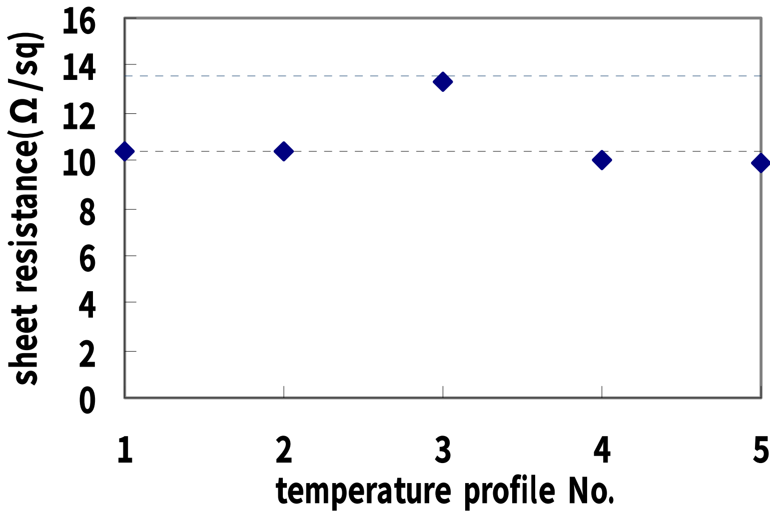


Fig. 3-21 sheet resistances of Ni silicide (Ni:12nm) obtained after each RTA process shown in Fig. 3-17. The lower and upper broken lines indicate the sheet resistances after RTA at 750 °C and 850 °C with ramping rate of 10°C/s, respectively.

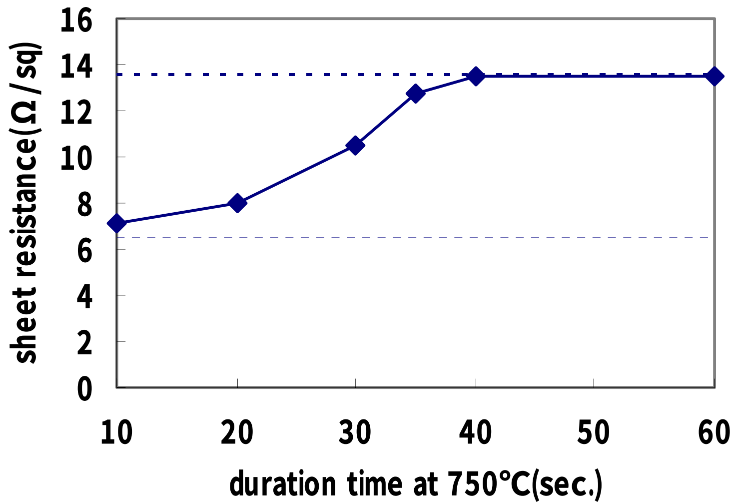


Fig. 3-22 Sheet resistance of Ni silicide layers as a function of duration time at 750 °C with ramping rate of 10°C/s. The lower and upper broken lines indicate the sheet resistances after RTA at 700 °C and 750 °C with ramping rate of 10°C/s, respectively.

3.2.1.2 Thermal Stability of Ni silicide with the Existence of Metal additives

Experiments about Ni silicide with additives of Pt, Hf, Ru, and V were carried out in collaboration with Mr. Koji Nagahiro and Mr. Takashi Shiozawa. For details, please refer to their master theses.

There are some common features when Pt, Pd, Hf, Zr, Ru, Ta, Ti and V were used as metal additives in course of Ni silicide thin film formation. However, there is no improvement in the thermal stability of Ni silicide with these additives. A result in case of Pt is shown as Figure 3-23.

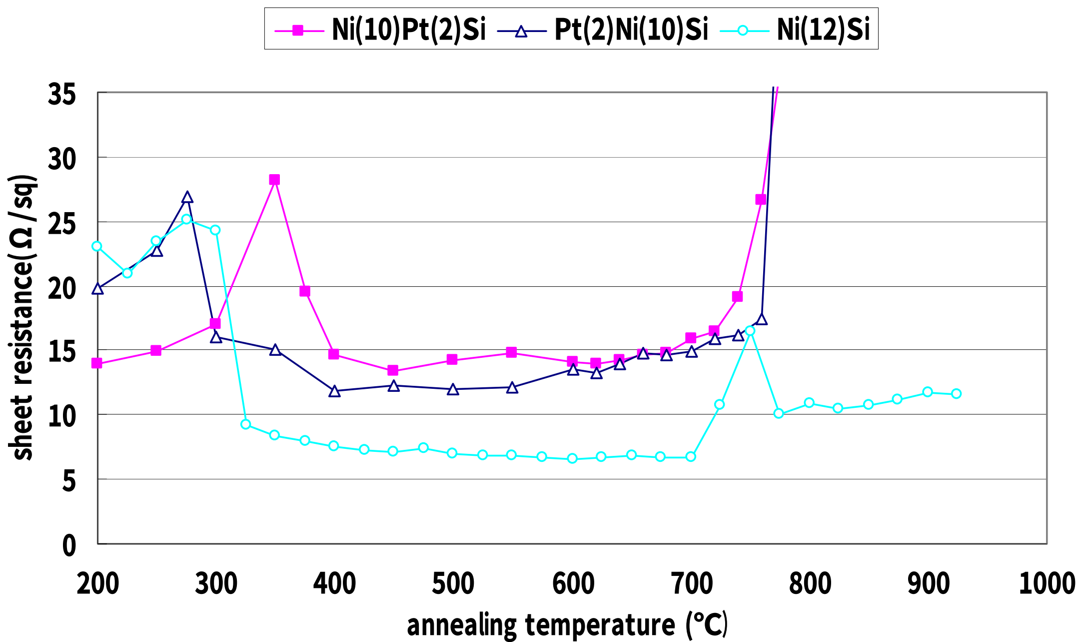


Fig. 3-23 annealing temperature versus sheet resistance with the addition of Pt in different position

3.2.2 Post-silicidation Doping

Based on the above results, a model is considered as shown in Fig.3-24. Flow (A) shows the typical phase transition of non additive Ni silicide. By adding the additives, we expected the phase transition flow (B-2) in which the additive suppresses the phase transition from NiSi to $NiSi_2$. However, in reality, in our experiment, flow (B-1) took place in which $NiSi_2$ layer was formed before NiSi by the suppression of Ni supply. To overcome the problem, we propose flow (C), "post NiSi-silicidation doping", in which these additive metals are introduced to the pre-formed NiSi. The additive metal in the pre-formed NiSi is expected to suppress the phase transition.

Fig. 3-25 is one of results achieved by "post NiSi-silicidation doping" method. To make comparisons, the data from the conventional bi-layer method

was plotted together. It should be noted that thermal stability of the pre-formed NiSi shows 25°C improvement. Addition of Pt improved 50°C.

Lots of analysis was carried out by TEM, AFM etc. Results of Ni silicide film with other metal additives such as Pt, Hf, Ru, V, Pd, Ti, and Ta had achieved. These results will be presented by my collaborators Mr. Koji Nagahiro and Mr. Takashi Shiozawa. Please refer to their Master these for details.

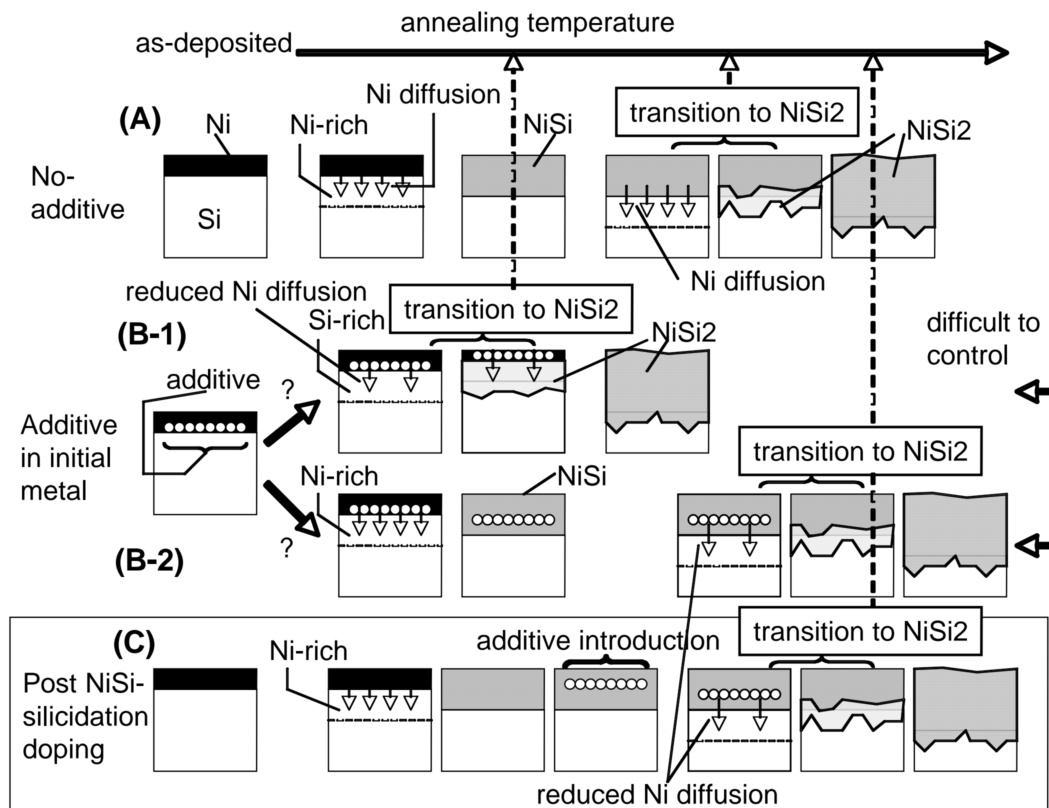


Fig. 3-24 Model of phase transitions and concept of “Post-silisidation doping” method comparing to the conventional ones
(Origin from Associate Professor Kazuo Tsutsui)

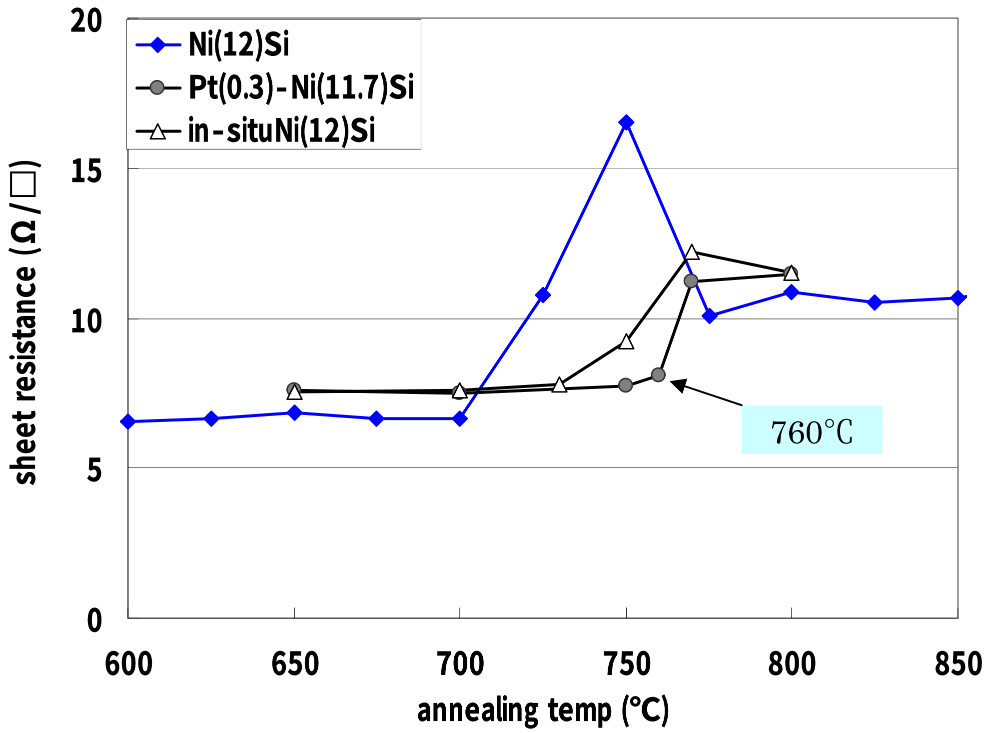


Fig. 3-25 sheet resistance versus annealing temperature of Ni thin film with Pt formed by conventional bi-layer method and post-silicidation doping method: bi-layer series were data from conventional bi-layer method and in-situ series were data from post-silicidation method.

Chapter 4

CONCLUSIONS

4.1 Results of This Study

In my study, the thermal stability of Ni silicide was investigated by both conventional bi-layer method and post silicidation doping. Lots of metal additives were systematically investigated under same experimental conditions and comparisons between metal additives were also made.

The phenomenon of irregular increase in sheet resistance of Ni silicide layer occurred relating to phase transition form NiSi to $NiSi_2$ was investigated, and the annealing conditions to produce the phenomenon were revealed. The origin of the higher resistance was considered to be the agglomeration occurred in the temperature region of phase transition from NiSi to $NiSi_2$. The annealing at a critical constant temperature produced the phenomenon, but ramping up through this temperature was found to be hard to produce it even with very slow ramping rate.

The new method of “Post-silicidation doping” was demonstrated to be superior for obtaining higher temperature of phase transition of Ni silicide to the conventional method in which additives were introduced before the initial silicidation. This method and concept will be beneficial to improve thermal stability of Ni silicide processes.

It was found that Pt and Hf had a good effect to strengthen the thermal stability of Ni silicide by about 50℃ by using post silicidation doping method while Pd, V, Ta, Ti, Ru had not brought good advantage to Ni silicide using either the conventional bi-layer method or post silicidation doping method.

4.2 Future Issues

Ni silicide exhibits high sheet resistance with increasing process temperature due to phase transformation from NiSi to $NiSi_2$ and/or agglomeration. The instability for thermal process is depending on various conditions such as film thickness, dopant in Si, temperature profile in annealing process, etc. So, other metal additives should be conducted to investigate. At the same time, TEG must be conducted to test if additive is proved to be effective to Ni silicide.

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Yokohama, Japan

Jan.14th,2006

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