

Master Thesis

2006

Study on Y_2O_3 Buffer Layer for
High-temperature Processed La_2O_3 MOSFET

Supervisor

Prof. Hiroshi Iwai

Tokyo Institute of Technology

Interdisciplinary Graduate School of Science and Engineering

Department of Advanced Applied Electronics

Iwai laboratory

04M36272

Kentaro Nakagawa

Contents

1 INTRODUCTION	1
1.1 Aggressive miniaturization driving Moore's law	2
1.2 Scaling Limits of Traditional SiO ₂ Gate Dielectric	6
1.3 Advanced Metal-Gate/High-k stacks for High Performance MOSFET	8
1.4 Search for Next Generation High-k Gate Dielectric	11
1.5 Problems with La ₂ O ₃ Dielectric	15
1.5.1 Decreasing Dielectric Constant	15
1.5.2 Water absorption	16
1.5.3 Oxygen Deficiency	17
1.6 The Requirement for Thermal Stability	18
1.7 Purpose of the Study	21
2 FABRICATION AND CHARACTERIZATION	
METHODS	23
2.1 Fabrication Methods	24
2.1.1 Silicon Substrates Cleaning Process	24
2.1.2 Electron-Beam Evaporation	25
2.1.3 Rapid Thermal Annealing (RTA) Method	27
2.1.4 Vacuum Evaporation of Gate Electrodes	28
2.1.5 Fabrication of n-channel MOSFETs	30
2.2 Characterization Methods	32
2.2.1 Spectroscopic Ellipsometry	32
2.2.2 Capacitance - Voltage (C-V) Characteristics	35
2.2.3 Gate Leakage Current - Voltage (J-V) Characteristic	39

2.2.4	Atomic Force Microscopy (AFM)	40
2.2.5	X-ray Photoelectron Spectroscopy (XPS)	41
2.2.6	Advanced XPS Analyses by Super Photon ring- 8 GeV (SPring-8)	43
2.2.7	Split C-V Method for Effective Mobility Measurements . .	45
2.2.8	Charge Pumping Methods	47

3 THE ELECTRICAL CHARACTERISTICS OF N-MOS CAPACITORS 52

3.1	Al gated n-MOS Capacitors	53
3.1.1	Introduction	53
3.1.2	La ₂ O ₃ Monolayer	53
3.1.3	Y ₂ O ₃ Monolayer	58
3.1.4	La ₂ O ₃ /Y ₂ O ₃ Stack	63
3.1.5	The Comparison Between Three Dielectrics	68
3.2	Pt gated n-MOS Capacitors	74
3.3	Control Experiment of Other Stack Structures	83
3.3.1	Introduction	83
3.3.2	Y ₂ O ₃ /La ₂ O ₃ structure	84
3.3.3	Y ₂ O ₃ /La ₂ O ₃ /Y ₂ O ₃ structure	86
3.4	PMA effect on the Al-gate/Y ₂ O ₃ interface	88
3.4.1	Introduction	88
3.4.2	Results and Discussion	89
3.5	Optimum Conditions for Dielectric Deposition	91
3.5.1	Introduction	91
3.5.2	Results and Discussion	92

3.6	Conclusion	97
4	STRUCTURAL ANALYSES	98
4.1	Morphological Analyses	99
4.1.1	Introduction	99
4.1.2	Results and Discussion	99
4.2	XPS analyses	103
4.2.1	Introduction	103
4.2.2	Results and Discussions	103
4.3	Conclusion	118
5	THE ELECTRICAL CHARACTERISTICS	
	OF N-MOSFETS	119
5.1	Introduction	120
5.2	Current - Voltage (I-V) Characteristics	120
5.3	The Effective Mobility	126
5.4	Characterization of Interface States by Charge Pumping Method	130
5.5	Conclusion	138
6	GENERAL CONCLUSIONS	139
6.1	Conclusions	140
6.2	For Future Works	141
	Acknowledgements	142
	References	144

Chapter 1

INTRODUCTION

1.1 Aggressive miniaturization driving Moore's law

Since the realization of MOSFET (Metal Oxide Semiconductor Field Effect Transistor) in 1960s, silicon integrated circuits have made a tremendous progress and indispensable for our modern society with advanced information technology. Today, it is becoming that the worldwide demand for the electrical products, especially for personal communication or portable products with high-technology instead of conventional PCs, such as 3rd generation cellular phone with mobile computing products (Personal Digital Assistants -PDAs) and digital still camera, internet video phone, digital TV, internet audio player, digital video recorder, etc. These products include a huge number of transistors.

The performance of these products, especially the processing speed and electrical power dissipation, depends on the geometrical size of MOSFET. In 1965, Gordon Moore who is one of the founder of Intel Corporation, in his article, described exponential growth in the number of transistors per integrated circuit and predicted this trend would continue. His prediction is popularly known as "Moore's Law". Moore's law states that the number of transistors on integrated circuits doubles approximately every 24 months resulting the high performance and low cost. That is the miniaturization of MOSFET is indispensable in driving the Moore's Law.

The miniaturization of MOSFET follows the scaling law. Figure 1.1 and table 1.1 explain the scaling law of MOSFET. Each parts of the MOSFET are downsized with the same coefficient S . As a result of downsizing, LSI system as a whole will get the S times better performance, in theory.

ITRS (International Technology Roadmap for Semiconductors) projection in the MOSFET and front-end process areas are driven by the overall chip requirement for speed, power dissipation, functional density, cost, etc. There are two main application categories for logic chip: high-performance and low-power logic.

Since each of these application areas have different overall chip requirements, the scaling goals are different. High performance logic such as for microprocessor unit (MPU) chips, where the main goal is maximum chip speed, with the tradeoff of relative high MOSFET leakage current. In contrast, low-power logic is used for mainly mobile systems, where the main goal is to preserve the battery life as long as possible.

For high-performance logic, physical gate length and EOT (Equivalent Oxide Thickness) value will decrease each year as shown in table 1.2, where the data is reported by ITRS[1].

Lately a lot of researches for miniaturization of MOSFET are being made all over the world. It is important to find out the possibilities of technological advancement of MOSFETs for high performance LSI system.

1.1 Aggressive miniaturization driving Moore's law

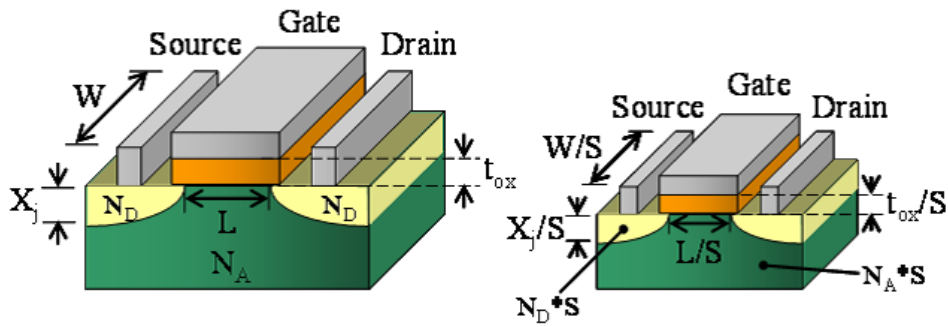


Figure 1.1: The scaling law for MOSFET

Table 1.1: The scaling on MOSFET with scaling factor S

Quantity	Before scaling	After scaling
Channel Length	L	$L' = L/S$
Channel Width	W	$W' = W/S$
Device Area	A	$A' = A/S^2$
Gate Oxide Thickness	t_{ox}	$t'_{ox} = t_{ox}/S$
Junction Depth	X_j	$X'_j = X_j/S$
Power Supply Voltage	V_{DD}	$V'_{DD} = V_{DD}/S$
Threshold Voltage	V_{th}	$V'_{th} = V_{th}/S$
Gate Capacitance per Unit Area	C_{ox}	$C'_{ox} = C_{ox}/S$
Doping Densities	N_A	$N'_A = N_A \cdot S$
	N_D	$N'_D = N_D \cdot S$

Table 1.2: High-performance Logic Technology Requirements

Year of Production	2006	2007	2008	2010	2015
Physical gate length (nm)	28	25	22	18	10
EOT (nm)	1.0	0.9	0.8	0.7	0.6
Gate leakage current limit (A/cm ²)	600	930	1100	1900	10000
Nominal power supply V _{DD} (V)	1.1	1.1	1.0	1.0	0.8
Saturation threshold voltage (V)	0.21	0.18	0.17	0.15	0.12
NMOS subthreshold leakage current ($\mu\text{A}/\mu\text{m}$)	0.05	0.07	0.07	0.1	0.3
Mobility/transconductance improvement factor	1.4	2.0	2.0	2.0	2.0
Subthreshold slope adjustment factor	1.0	1.0	0.8	0.6	0.5
Effective saturation n carrier velocity enhancement factor	1.0	1.0	1.0	1.1	1.3
Parasitic source/drain series resistance ($\Omega/\mu\text{m}$)	171	162	153	135	88
High-performance NMOS intrinsic delay τ (ps)	0.75	0.64	0.54	0.39	0.18
Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003	1.60	1.86	2.20	3.06	6.8
NMOSFET static power dissipation ($\text{W}/\mu\text{m}$)	6.05E-7	8.47E-7	7.70E-7	1.10E-6	2.60E-6

1.2 Scaling Limits of Traditional SiO₂ Gate Dielectric

As mentioned in the previous section, the MOS transistors, which are main part of LSI system, must be miniaturized to get better performance and bring down costs. And the gate dielectric, which separates the gate electrode from carrier passage, must also be thinner following the scaling law. Silicon dioxide (SiO₂) has been used for transistor gate dielectrics for nearly 30 years because SiO₂ is compatible with silicon substrate: SiO₂ formed perfect gate dielectric material for silicon. For three decade, SiO₂ has successfully scaled from a thickness of 100 nm 30 years ago to a mere 1.2nm at the present. However, as transistor geometries scale to the point where the traditional SiO₂ gate dielectric film becomes just a few atomic layers thick, direct tunneling current leakage and the resulting increase in power dissipation and heat become critical issues. This direct tunneling current leakage is proportional to the equation as follow.

$$I \propto \exp\{-(m\phi) \cdot D\} \quad (1.1)$$

m :electron effective mass ϕ :barrier height

D :physical thickness of gate oxide

This equation indicates that the thicker gate dielectric film becomes, the lower gate tunneling current. Conversely, if a thickness of gate dielectric film becomes thinner, the gate tunneling current leakage increases. Figure 1.2 shows the relationships between gate leakage current density and EOT (Equivalent Oxide Thickness). The gate leakage current density reaches 600 [A/cm^2] as a thickness of SiO₂ thins down to 1nm. Furthermore, the gate leakage current becomes 1 [kA/cm^2] in the case of 0.8nm. As shown in table 1.2, EOT value in high performance logic technology will get 1nm in 2006. Consequently, SiO₂ as a gate

1.2 Scaling Limits of Traditional SiO₂ Gate Dielectric

oxide film reaches its limit so that new materials for gate dielectrics are required to continue geometrical scaling down of MOS transistors.

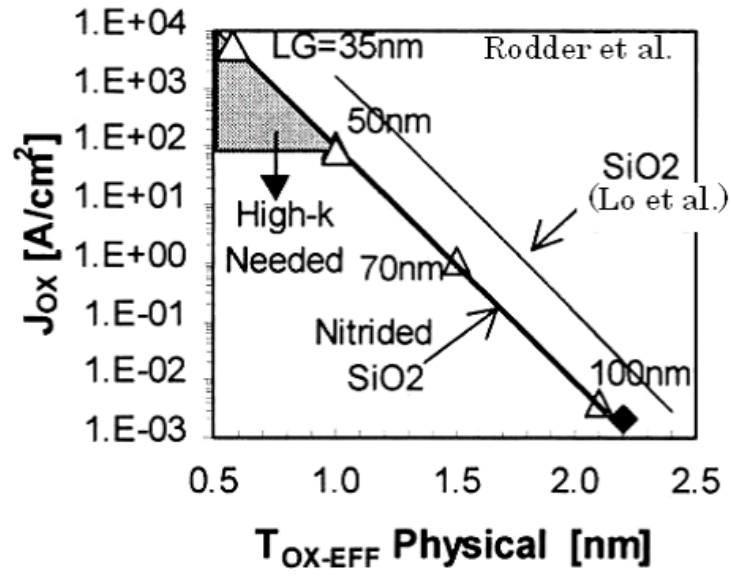


Figure 1.2: The relationships between the gate leakage current density and EOT. Gate leakage current continues to increase as far as SiO₂ is used for gate dielectric.

1.3 Advanced Metal-Gate/High-k stacks for High Performance MOSFET

A quite thin EOT with less than 1nm is required for high performance and low power consumption LSI system. In order to get such a thin EOT and reduce the gate leakage current, high-k material is likely to replace today's SiO₂, and also metal gate to suppress the poly-silicon depletion which corresponds to the additional series gate capacitance[2]. One of the problems associated with thinning a gate dielectric is a susceptibility to boron penetration, which is due to the uncontrolled diffusion of boron from the heavily doped P⁺ poly gate through the gate oxide and into the MOSFET channel. This boron penetration induces the threshold voltage shift and becomes hard to control. Lightly doping the gate oxide with nitrogen generally solves this problem.

One approach to reduce gate leakage current is to use gate dielectric film with a higher relative dielectric constant k than the 3.9 value of thermal SiO₂. Dielectric constant is the measure of how much charge a material can hold. For such a gate dielectric film with physical thickness of t_{phy} , the equivalent oxide thickness(EOT) value is expressed as follow.

$$EOT = t_{phy} \cdot (3.9/k) \quad (1.2)$$

If a gate dielectric film with larger k value is used, it is possible to make t_{phy} thicker. For instance, as shown in figure 1.3, if a k is 15.6, the EOT and t_{phy} are 1.0nm and 4.0nm, respectively. Since direct tunneling current strongly depends on t_{phy} , the gate leakage current will generally become smaller for the high-k gate dielectric film than the SiO₂ dielectric.

Before the year 2005, heavily nitrogen-doped oxy-nitride gate dielectric, which has a relative dielectric constant of 6.5, will meet ITRS requirements and be suf-

1.3 Advanced Metal-Gate/High-k stacks for High Performance MOSFET

ficient for both the high performance and low operating power chips. For the years beyond 2005, however, the oxy-nitride film becomes quite thin, and there are serious problems about oxy-nitride's reliability and large gate leakage current, particularly for high performance logic. Figure 1.4 shows the annual simulated and limits of gate leakage current for oxy-nitride film reported by ITRS. According to this figure, simulated gate leakage current crosses the limit in 2005. Hence, high-k material will be required.

Another major issue of front-end is poly-silicon depletion in the gate electrode. As in figure 1.5, when gate voltage is applied to turn on a MOSFET, a depletion region thickness of W_d forms adjacent to poly-silicon/oxide interface. This depletion region increases the effective electric thickness of a gate oxide film by an amount proportional to W_d , and as a result, both the electric field in the gate oxide film and the inversion layer charge for any given gate voltage are reduced. Hence, threshold voltage pinning, known as "Fermi-level pinning," occurs and it reduces drive current. Furthermore, phonon scattering which results from the inherent polarization interferes with electron mobility in the transistor channel. The impact of poly-silicon depletion becomes more severe with the smaller values EOT and device performance. Since W_d is proportional to the poly-silicon doping, increased doping of the poly-silicon ameliorates the depletion issue, but with solubility of dopants, this solution will eventually become inadequate. An alternate solution of metal gate is being developed. For any metal gates, there is virtually no depletion and no boron penetration, and the gate electrodes have very low sheet resistance. Metal gate is entering the mainstream of gate electrode, and active development is being carried out on metal gate.

1.3 Advanced Metal-Gate/High-k stacks for High Performance MOSFET

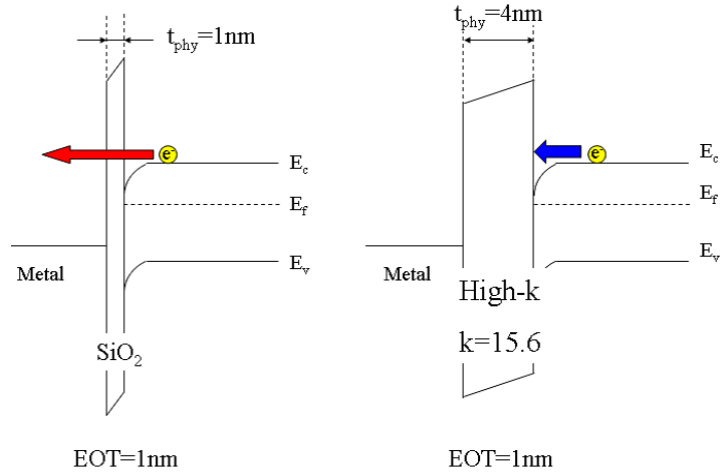


Figure 1.3: Band diagram of direct tunneling mechanism for SiO₂ and high-k films with the same EOT of 1nm. Physical thickness of high-k film with relative dielectric constant of 15.6 becomes 4 times thicker than that of SiO₂ film without increasing EOT value.

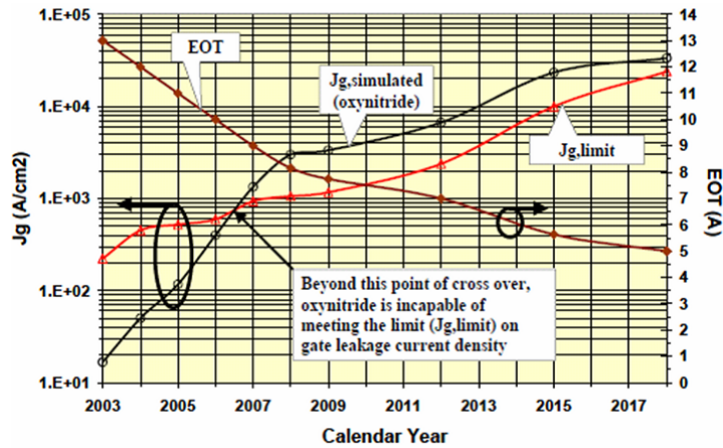


Figure 1.4: Annually simulated and limits of gate leakage current density for oxy-nitride film. The simulated gate leakage current cross over its limit during 2005.

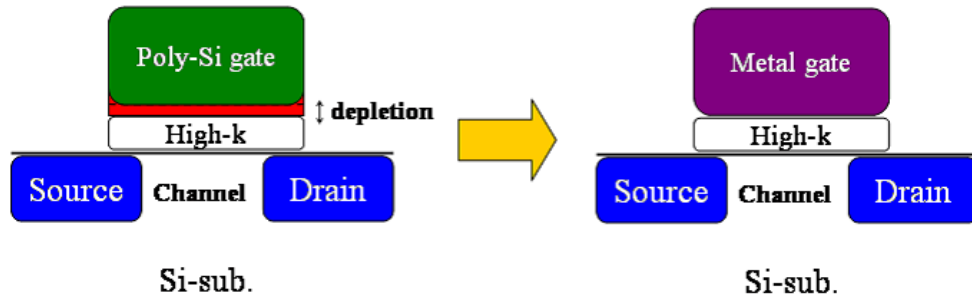


Figure 1.5: The depletion region of thickness W_d forms adjacent to the poly-Si/oxide interface. Metal-gates would solve this problem.

1.4 Search for Next Generation High-k Gate Dielectric

Since the limits of SiO_2 were realized, new materials with the capability for increasing thickness due to a higher k value for next generation gate dielectric film have been studied. Without these high-k materials, the miniaturization of MOSFET would inevitably hit a wall. The effort to find an alternative material in both industry and academia has gone on for more than 10 years. During initial phase of high-k investigation, STO (SrTiO_3) or BST (BaSrTiO_3) had been a mainstream for subject of research. However, these materials react with Si substrate resulting the SiO_2 interfacial layer and the barrier lowering effect induced by fringing field. Although Al_2O_3 has a higher barrier, dielectric constant is small so that it can not provide sufficient advantages of alternative gate dielectric. ZrO_2 has also been investigated for high-k gate dielectric, but it is likely to be excepted from the candidates for alternative material because of its thermal instability. Today, HfO_2 and its family, such as HfSiON and HfAlO , are established as the next generation gate dielectric. Particularly, HfSiON gate dielectric film is being expected to debut for the low stand-by power products in a few years. Table 1.3 shows the

1.4 Search for Next Generation High-k Gate Dielectric

relative dielectric constants of representative gate dielectric.

Besides these materials, the rare earth metal oxides have also been researched in the early stage. Figure 1.7 is periodical table of the elements. Rare earth metals belong to III A group elements in periodical table. Recently, excellent properties of rare earth oxides, such as La_2O_3 , Ce_2O_3 , Pr_2O_3 , Gd_2O_3 and Dy_2O_3 , have been reported[3]-[11]. Among these rare earth oxides, La_2O_3 is the most hopeful dielectric film. In fact, La_2O_3 has a larger dielectric constant, band gap and higher band offset than any other materials including HfO_2 . La_2O_3 is expected to be the third generation gate dielectrics, next to HfO_2 .

Table 1.3: Relative dielectric constant of the representative High-k materials

Relative dielectric constant	The representative materials
3.9	SiO_2
5 ~ 6	SiON $\text{Si}_3\text{N}_4/\text{SiO}_2$ stack
~ 7	Si_3N_4
~ 10	Al_2O_3
10 ~ 20	HfSiON , ZrSiO , HfSiO , AlSiO , ZrAlO , ZrNO
15 ~ 30	ZrO_2 , HfO_2 , La_2O_3 , Pr_2O_3 , Gd_2O_3
~ 30	crystal Pr_2O_3

1.4 Search for Next Generation High-k Gate Dielectric

● = Not a solid at 1000 K
 ○ = Radioactive
 ① = Failed reaction 1: $\text{Si} + \text{MO}_x \rightarrow \text{M} + \text{SiO}_2$
 ② = Failed reaction 2: $\text{Si} + \text{MO}_x \rightarrow \text{MSi}_x + \text{SiO}_2$
 ⑥ = Failed reaction 6: $\text{Si} + \text{MO}_x \rightarrow \text{M} + \text{MSi}_x\text{O}_y$

●																	●	
H																	He	
Li	Be											●	●	●	●	●	●	●
①												●	●	●	●	●	●	●
Na	Mg											Al	Si	P	S	Cl	Ar	
●	●	●	②	①	①	①	①	①	①	①	①	①	①	●	●	●	●	
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr	
●	●	●	●	①	①	●	①	①	①	●	①	①	①	①	①	●	●	
Rh	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rb	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe	
●	⑥	●	●	①	①	①	①	①	●	●	●	●	①	①	○	○	○	
Cs	Ba	R	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn	
○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	
Fr	Ra	A	Rf	Ha	Sg	Ns	Hs	Mt										

R	La	Ce	Pr	Nd	○	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
A	Ac	Th	Pa	U	○	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

Figure 1.6: Periodical table of the elements.

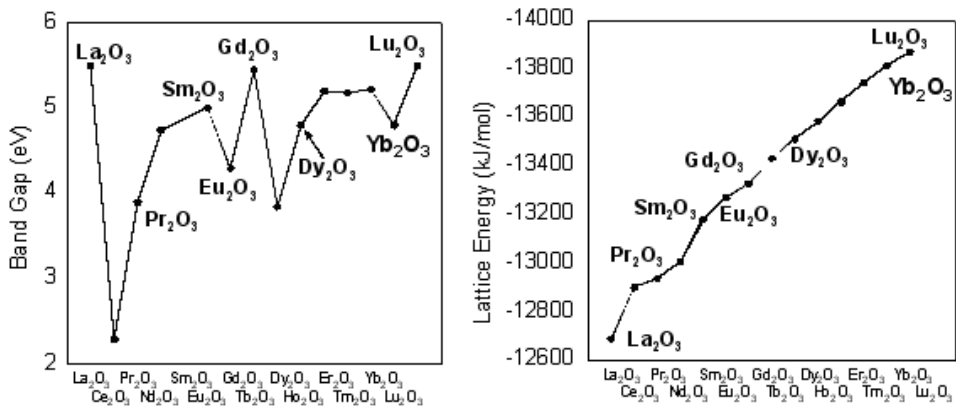


Figure 1.7: Bandgap and lattice energy for rare earth metal oxides.

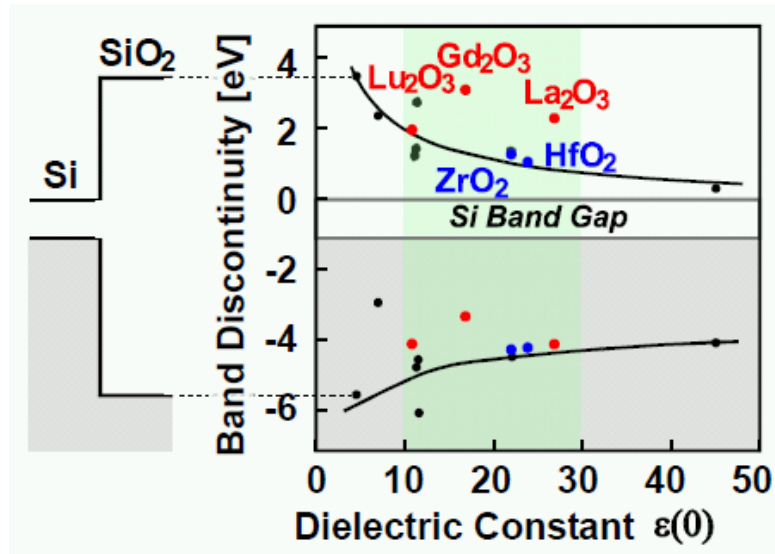


Figure 1.8: Relationship between band gap and relative dielectric constant. La_2O_3 has a large band gap and dielectric constant.

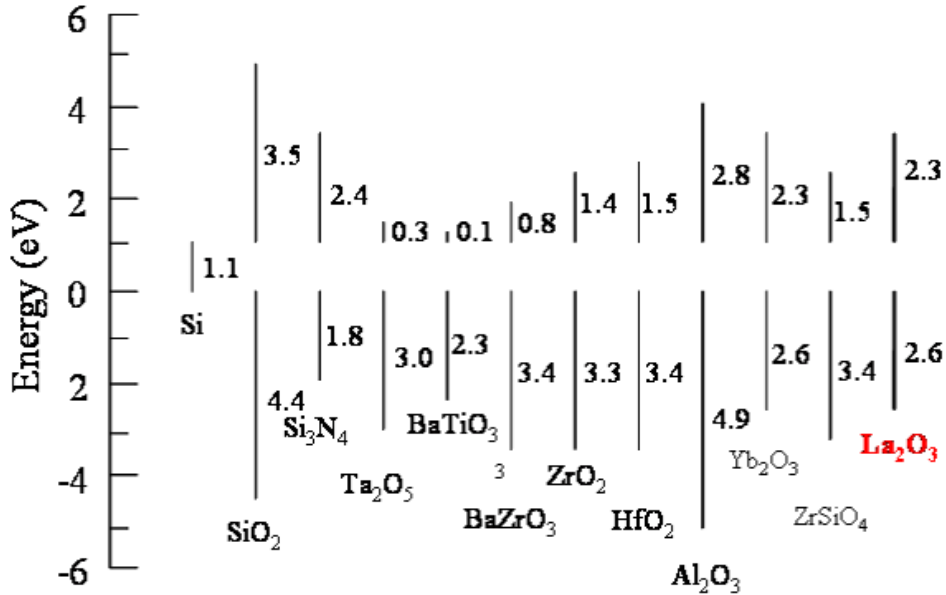


Figure 1.9: Band offset for high-k dielectrics on Si.

1.5 Problems with La_2O_3 Dielectric

In this section, I would like to enumerate some of the problems with La_2O_3 dielectric.

1.5.1 Decreasing Dielectric Constant

La_2O_3 dielectric would be very hopeful due to its high dielectric constant. However, at the interface between silicon substrate and La_2O_3 , La_2O_3 reacts with silicon substrate and formed the interfacial layer which is mixture of silicon oxides (SiO_x) and lanthanum-silicate (La-O-Si) by heat treatment[12]. Dielectric constant of produced interfacial layer is lower than La_2O_3 itself. And what is worse is that silicon atoms diffuse into La_2O_3 film and bind to La atoms via oxygen. These phenomena, depicted in figure 1.10, induce the decrease of the effective permittivity of La_2O_3 dielectric film as a whole i.e. lead to the increase of EOT value.

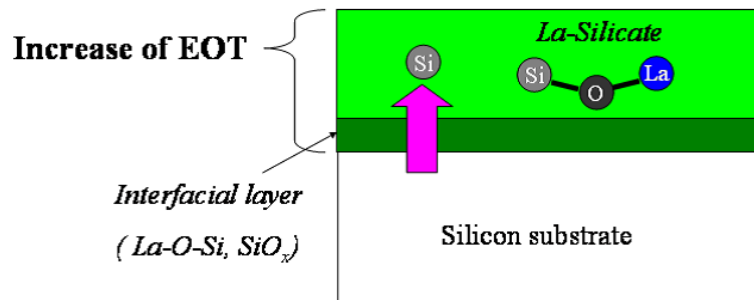


Figure 1.10: The growth of interfacial layer and the formation of lanthanum-silicate. These would decrease the permittivity of dielectric film.

1.5.2 Water absorption

Water absorption issue is very severe because wet processes are essential for fabricating MOSFETs. It is known that La_2O_3 has a poor water-resisting property even when exposing in air[13]-[15]. In fact, La_2O_3 film thickness of 4.1nm, which was measured immediately after deposition, increased to 4.6nm after 12 hours. Figure 1.11 illustrates the water absorption of La_2O_3 film. La_2O_3 hydrates resulting from absorbing moisture in the air. The presence of OH^- ions in place of O^{2-} sites would behave as a positive fixed charge and induce several problems, such as flatband voltage shift and degradation of carrier mobility etc.

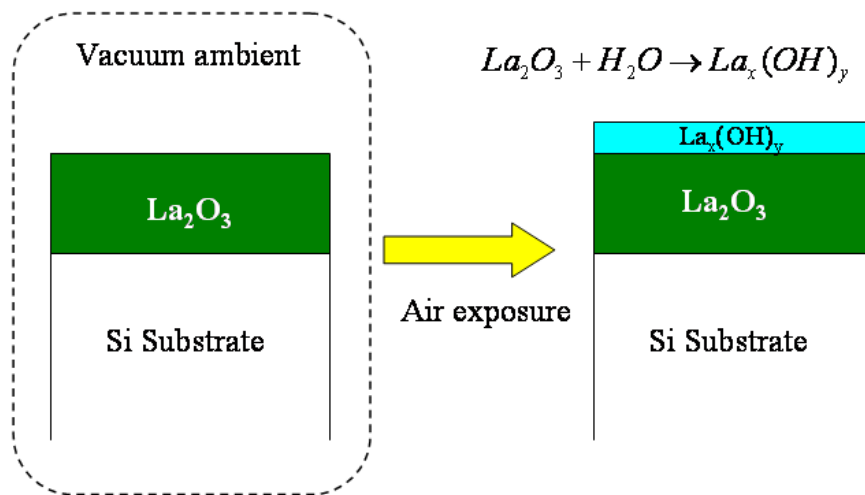


Figure 1.11: Water absorption mechanism of La_2O_3 film. $(\text{OH})^-$ ions in place of O^{2-} sites behave as a positive charge.

1.5.3 Oxygen Deficiency

As stated in previous section, La_2O_3 dielectric causes a large flatband shift in the direction of negative side, indicating the presence of positive fixed charge. There are two possibilities for this. The first would be related to the moisture sensitivity of La_2O_3 film. The second is oxygen vacancies, which are expected to be positively charged and, indeed, nonstoichiometric La_2O_3 has been reported to be oxygen deficient[16]. This oxygen defect would arise both at the interface between silicon substrate and La_2O_3 and in the La_2O_3 film. Figure 1.12 shows the likely oxygen deficiency and generations of positive fixed charge mechanisms. The generated positive charges, in turn, result in trapping sites efficient for electron. The trapped electrons have a great impact on the channel mobility of MOSFETs. Preventing the oxygen deficiency is significant challenge for improving the performance of MOSFET with La_2O_3 dielectric.

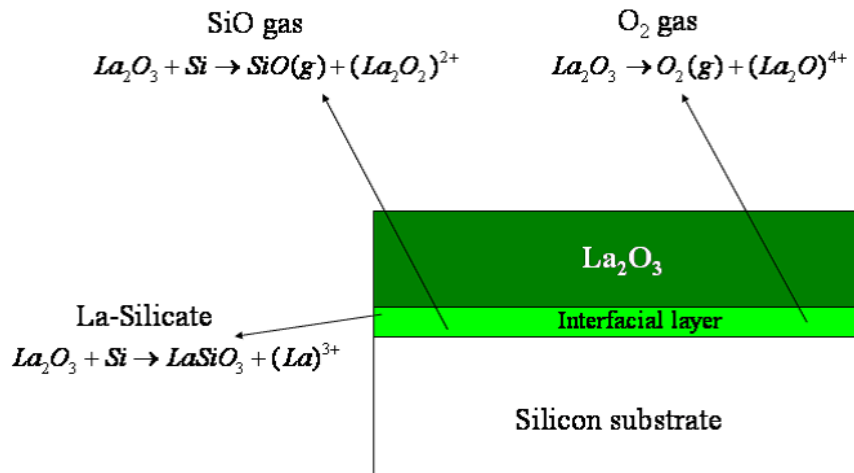
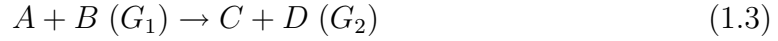


Figure 1.12: The mechanisms of generating positive fixed charges.

1.6 The Requirement for Thermal Stability

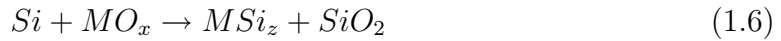
Thermal stability on silicon is momentous affair as considering the alternative gate dielectrics. One of the best way to understand a thermal stability is to have the understandings of the Gibbs free energy[17]. Suppose, for example, there is a following reaction formula, a difference in Gibbs free energy (ΔG) between before and after rection is important.



$$\Delta G = G_2 - G_1 \quad (1.4)$$

The magnitude and the sign of ΔG decide on whether the reaction is thermodynamically stable or not.

In the Ref.[17], several key reactions were indentified by considering the phase diagram of a M-Si-O system, where M is (metal) binary oxides, to narrow down the list of binary oxides that could be stable in contact with silicon at 1000K. Among these reactions, most binary oxides were concluded whether to be stable or not in contact with silicon by following reaction path.



For each reaction (appropriately balanced for the particular binary oxide, MO_x , with coefficients ν) $\Delta G_{f,1000}^o$ for the complete reaction was determined by subtracting the sum of the free energies of formation of the reactants from the sum of the free energies of formation of the products.

$$\Delta G_{1000}^o = \sum_{Products} \nu \Delta G_{f,1000}^o - \sum_{Reactants} \nu \Delta G_{f,1000}^o \quad (1.7)$$

1.6 The Requirement for Thermal Stability

The magnitude of $\Delta G_{f,1000}^o$ indicates the direction of the reaction. $\Delta G_{f,1000}^o$ for the reaction [Eqs. 1.5 and 1.6] for each of the well-known binary oxides are given in table 1.4. A negative value for $\Delta G_{f,1000}^o$ indicates that it is thermodynamically favorable for the reaction to proceed to its products. Thus, when it was determined that $\Delta G_{f,1000}^o$ for one of the above reactions was negative, indicating that silicon and MO_x are not thermodynamically stable in contact with each other. Conversely, if a sign of $\Delta G_{f,1000}^o$ is a positive, MO_x is compatible with silicon. In addition, a larger magnitude of $\Delta G_{f,1000}^o$ value, the more unfavorable for the reaction to proceed to its products. In other words, the formation of silicon oxides and metal silicides are expected to be reduced.

In table ??, La_2O_3 has a relatively large $\Delta G_{f,1000}^o$ and other rare earth oxides, such as Y_2O_3 , Sc_2O_3 have a larger value than La_2O_3 . These materials are expected to be thermally stable on silicon.

1.6 The Requirement for Thermal Stability

Table 1.4: The Gibbs free energies for the well-known binary oxides

Binary oxide (MO_x)	$\Delta G_{f,1000}^o$ per MO_x for Reaction 1.5 (kcal/mol)	$\Delta G_{f,1000}^o$ per MO_x for Reaction 1.6 (kcal/mol)
ZrO ₂	+42.326	+5.914
HfO ₂	+47.648	-
Al ₂ O ₃	+63.399	No known silicides
TiO	+17.849	unstable
Ti ₂ O ₃	+35.432	unstable
TiO ₂	+7.527	unstable
WO ₂	-77.126	unstable
WO ₃	-121.814	unstable
Ta ₂ O ₅	-52.533	unstable
GeO ₂	-82.124	unstable
Sc ₂ O ₃	+123.105	+91.297
Y ₂ O ₃	+116.823	-
La ₂ O ₃	+98.470	+66.372
Ce ₂ O ₃	+104.946	+17.896
Nd ₂ O ₃	+101.692	+76.974
Pr ₂ O ₃	+105.768	-
Gd ₂ O ₃	+101.549	+88.582
Dy ₂ O ₃	+112.435	-
Er ₂ O ₃	+122.030	-
Yb ₂ O ₃	+103.830	-
Lu ₂ O ₃	+116.965	-

1.7 Purpose of the Study

So far, motivation for alternative gate dielectric and general properties of high- k materials were discussed. Although La_2O_3 has excellent properties, there are some of the problems resulting in the performance decrement of MOSFET. It is especially important for MOSFET to obtain thinner EOT and better interface states between silicon and gate dielectric. However, the increase of EOT and the interface trap density for La_2O_3 film, especially with high-temperature treatment, were reported[9].

The objective of this study is to maximize the dielectric constant of La_2O_3 and obtain good interface states with silicon, especially in high-temperature treatment. Y_2O_3 , which is as well as the rare earth oxide, would meet these requirement because Y_2O_3 dielectric has following attractive features[18]-[20].

- A wide energy band gap of 5.5eV
- High dielectric constant of ~ 18
- Good thermal stability
- A strong affinity for oxygen
- Lattice constant well-matched with silicon ($a(\text{Y}_2\text{O}_3)=1.06\text{nm}$, $a(\text{Si}) \times 2=1.086\text{nm}$)

And also, compatibility with silicon[21], significant reduction of gate leakage current by using Y_2O_3 dielectric[15] and about water absorption[22] have been reported.

In terms of Gibbs free energy, in table 1.4, Y_2O_3 has a large positive value, indicating that the reaction for $\text{Si} + \text{MO}_x \rightarrow \text{M} + \text{SiO}_2$ is hard to proceed and the contact with silicon is thermally stable. Thus, one would expect the reduction of silicon oxides rich interfacial layer formation. In fact, there is a report about the reduction of interfacial SiO_2 by utilizing Y_2O_3 as a gate dielectric[23].

1.7 Purpose of the Study

In view of these reports and properties of Y_2O_3 , one would employ Y_2O_3 as a buffer layer for La_2O_3 dielectric to minimize the EOT value, reduce the gate leakage current and stabilize the interface states. Figure 1.13 shows the schematic La_2O_3/Y_2O_3 stack dielectric. Y_2O_3 could serve as a deterrent to formation of lanthanum-silicate and the growth of interfacial layer.

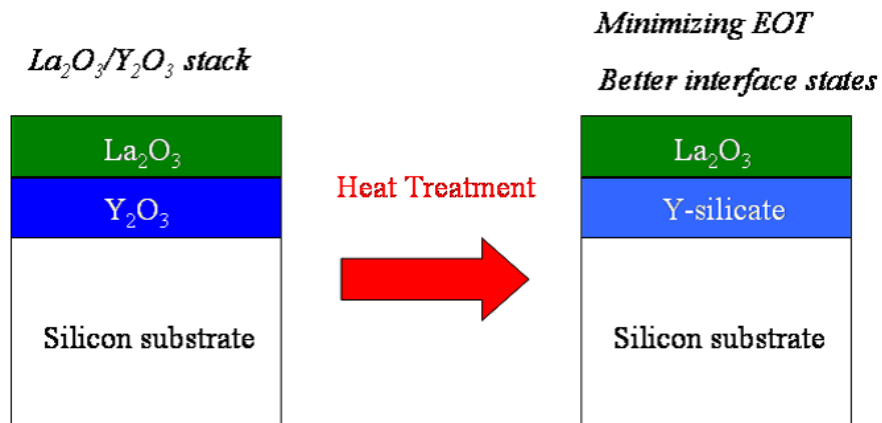


Figure 1.13: La_2O_3/Y_2O_3 stack dielectric

Chapter 2

FABRICATION AND CHARACTERIZATION METHODS

2.1 Fabrication Methods

2.1.1 Silicon Substrates Cleaning Process

Prior to deposition of gate dielectric film, ultra clean silicon surface is required without contamination, such as particle, organic and ionic. The cleaning process adopted in the study was based on the RCA method proposed by W. Kern et al. in 1970's. First, silicon substrates were liquored in SPM solution, mixed 4 parts $H_2SO_4(96\%)$ with 1 part $H_2O_2(30\%)$, generating heat helping organic materials oxidize. And then, dipped in hydrofluoric acid diluted at 1% to remove chemical or natural oxide layers and obtain hydrogen-terminated surface. Hydrogen-terminated surface is stable and a preventive oxidation.

Besides, ultra-pure water (UPW) used for silicon substrates rinse was with resistivity of more than $18.2 M\Omega/cm$, fewer than 1 colony of bacteria and 1 particle per milliliter.

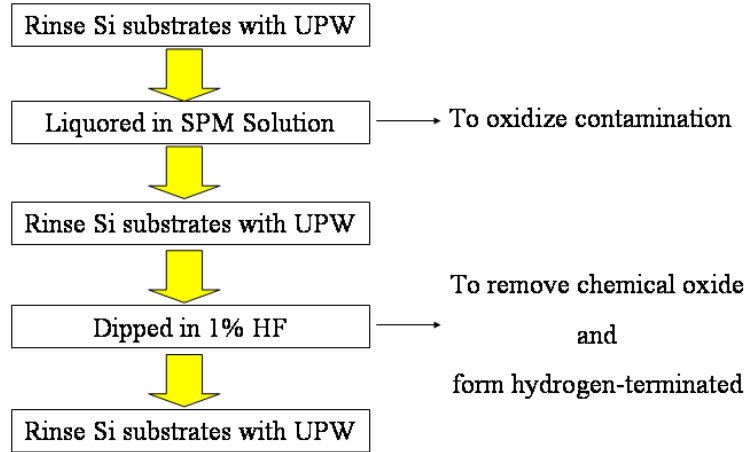


Figure 2.1: Silicon cleaning process for ultra-clean surface.

2.1.2 Electron-Beam Evaporation

After cleaning process, silicon substrates were introduced into the Molecular Beam Epitaxy (MBE) chamber immediately. La_2O_3 and Y_2O_3 dielectrics were deposited in ultra high vacuum by electron-beam evaporation method.

There are two main types of deposition method. One is Physical Vapor Deposition (PVD), such as vacuum evaporation, sputtering and laser ablation. The other is Chemical Vapor Deposition (CVD) utilizing chemical reaction. Electron-beam evaporation method used in the study belongs to PVD method.

Figure 2.2 and 2.3 shows the schematic and a photo of MBE equipment. MBE chamber consists of two chambers, loading and growth chamber. Each chambers have two pumps. Turbo-molecular pump (TMP) and rotary pump (RP) in loading chamber. Titanium sublimation pump (TSP) and ion pump (IP) in growth chamber. These pumps make it possible to deposit the oxides in ultra high vacuum atmosphere. The background pressure in growth chamber was around 10^{-10} Torr and was approximately 10^{-8} Torr during deposition. There are four types of oxide sources in the bottom side of chamber. La_2O_3 or Y_2O_3 source is heated by electron-beam and begin to evaporate. In the case of structuring La_2O_3 / Y_2O_3 stack, deposited Y_2O_3 firstly and then La_2O_3 deposition.

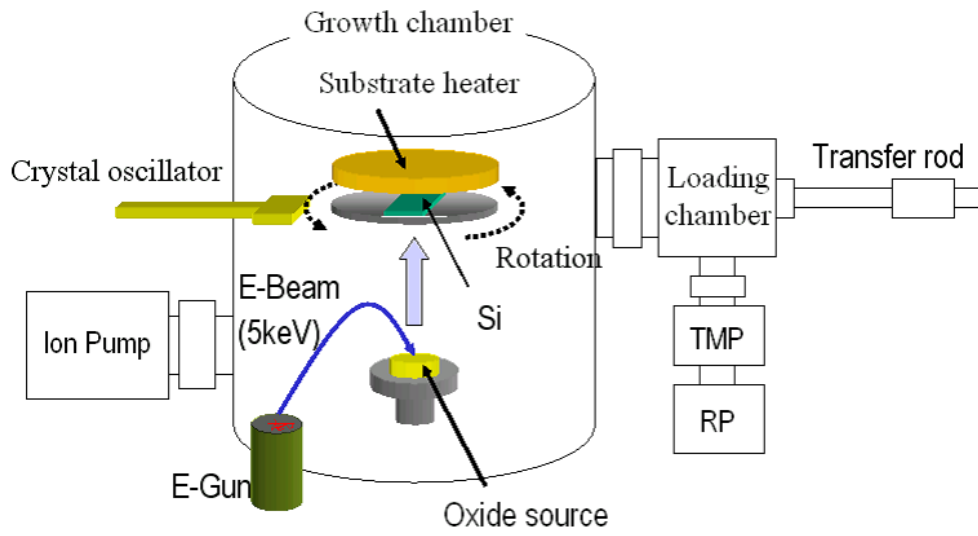


Figure 2.2: Schematic overview of MBE chamber.

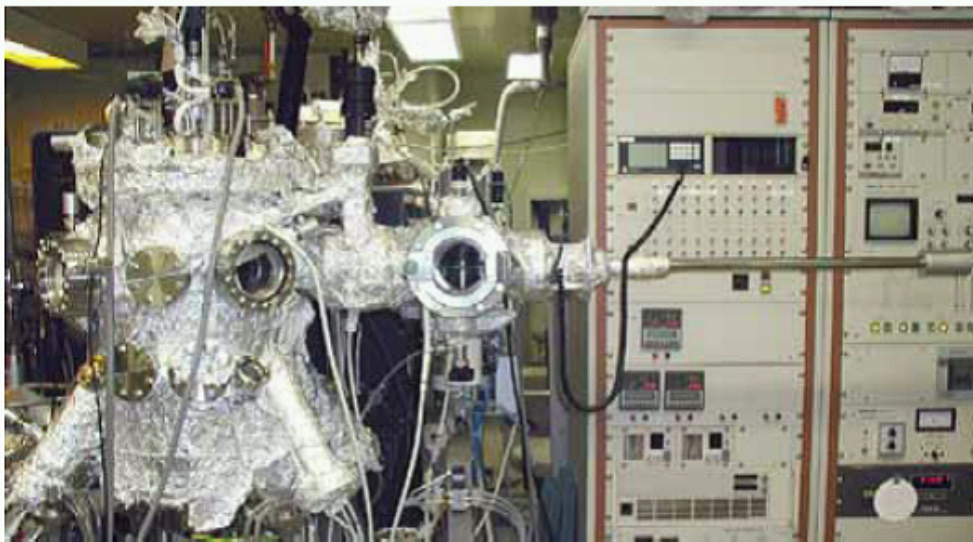


Figure 2.3: A photo of MBE chamber.

2.1.3 Rapid Thermal Annealing (RTA) Method

RTA method was employed for the heat treatments after depositing dielectric films. The annealing process is indispensable to improving defects in dielectric film and at the interface.

The schematic RTA system and process flowchart are shown in figure 2.4. The samples with gate dielectric were put on silicon susceptor and inserted into heat-treating furnace. The ambience in furnace was vacuumed adequately by rotary pump for highly-pure nitrogen or oxygen substitution. And then, nitrogen or oxygen (in accordance with the purpose) were provided with flow rate of 1.0 l/min and the samples were annealed at atmospheric pressure. In order to evaluate the electrical or chemical properties, the annealing temperatures ranging from 300 °C to 1000 °C were made an attempt.

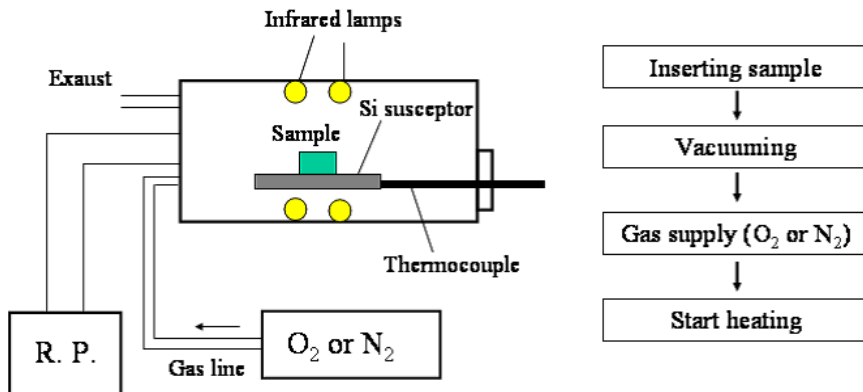


Figure 2.4: Schematic illustration of RTA system and annealing process flowchart

2.1.4 Vacuum Evaporation of Gate Electrodes

Aluminum (Al) and Platinum (Pt) gate electrodes were deposited by high-vacuum evaporation method. The advantages of evaporation method are simplicity and smaller damage to dielectric film compared with sputtering method.

Al evaporation equipment is depicted in figure 2.5. Al sources fixed on tungsten filament were heated by emission current and began to evaporate at more than a melting point of 660 through stencil shadow mask to form gate electrodes. The shape of electrodes were circle with the diameter of 100, 200, 400 and 1000 μm . The degree of vacuum was around 10^{-5} torr level.

A melting point of Pt is so high (1776 °C) that Pt source was heated by electron beam. Pt evaporation equipment is depicted in figure 2.6. As in the case of Al deposition, Pt gate electrodes were deposited through stencil shadow mask. The degree of vacuum was around 10^{-6} torr level.

The reason why one has chosen Pt as a gate electrode is to suppress alumina (Al_2O_3) interfacial layer, which has a low dielectric constant, resulting from the reaction between gate electrode and dielectric films and to evaluate dielectric films themselves without interfacial layer.

Al was deposited for the backside electrode because the backside electrode is less sensitive to the electrical characteristics than gate electrode. Besides, the oxide layer on the backside of silicon substrate was removed with a swab dipped in HF solution before depositing Al.

2.1 Fabrication Methods

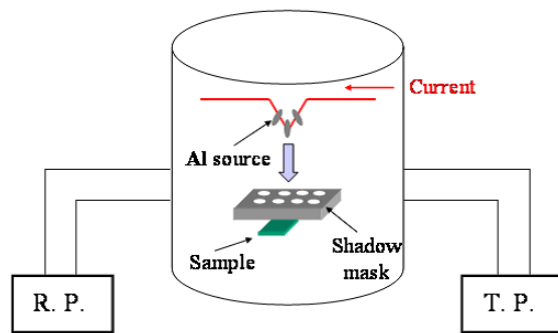


Figure 2.5: Al evaporation system

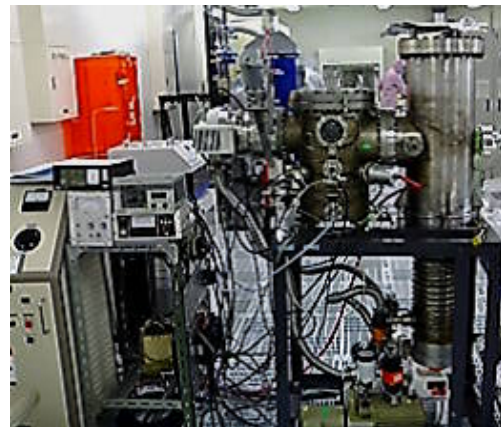
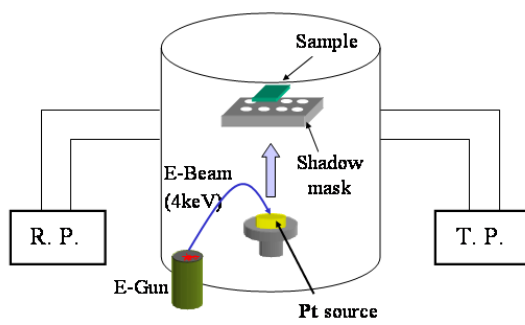


Figure 2.6: Pt evaporation system

2.1.5 Fabrication of n-channel MOSFETs

In the fabrication of n-channel MOSFETs, p type silicon substrates, which were previously doped impurity, formed field oxide and SiO₂ gate dielectric, were used (provided by TOSHIBA Corp.). Hence, the fabrication process started with substrates cleaning.

After depositing Al on dielectric film, Al was etched to shape gate electrodes through photolithography process. Figure 2.7 shows schema of the photolithography process for gate electrodes etching. Samples were coated with the positive type photoresist OFPR and spread resist evenly across the surface by spinning samples (1). Samples coated with photoresist were set in mask aligner and the marks on the photomask were aligned with the marks on substrates. Then, coated photoresist was exposed to ultraviolet radiation (2). Only exposed areas through photomask are soluble in photographic developer. NMD-3 was used as a developer (3). After developing samples, Al was etched with H₃PO₄ as a etching agent (4).

Figure 2.8 shows schema of the continuous photolithography process for forming source and drain electrodes. Gate etched samples were coated with photoresist, aligned a photomask, exposed (5) and developed (6). HCl solution diluted by 0.36% was used for etching La₂O₃ and/or Y₂O₃ and 1% HF was for removing interfacial layer (7). After that, Al was deposited on the whole surface (8). Al on photoresist was lifted off in acetone fluid by ultrasonic oscillation (9). The backside Al electrodes were deposited after the backside HF treatment.

2.1 Fabrication Methods

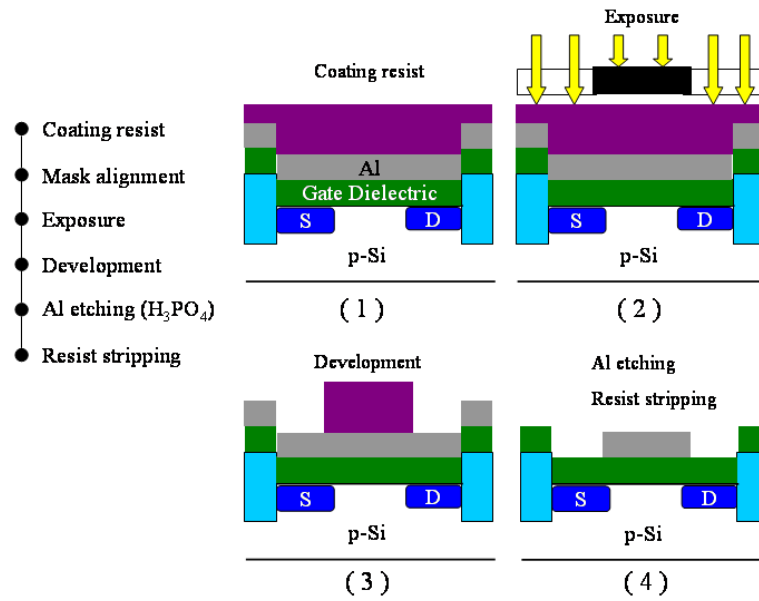


Figure 2.7: Photolithography process for gate electrodes etching

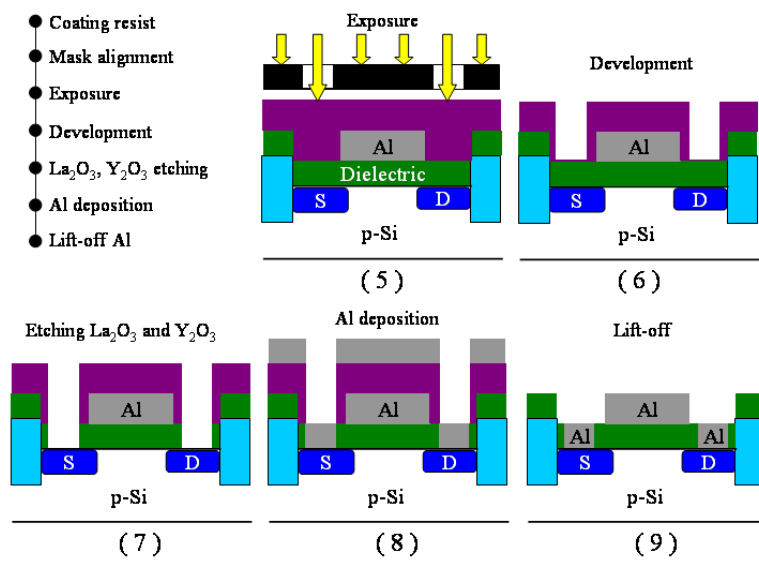


Figure 2.8: Photolithography process for source and drain electrodes

2.2 Characterization Methods

2.2.1 Spectroscopic Ellipsometry

The physical thickness was optically extracted by FE-5000 ellipsometer using a Cauchy model and a single layer approximation.

Generally, the polarization of light consists of two component S and P. One is the vertical component and the other is horizontal component. If the phase lag between S and P polarization is zero, 90° and Ψ , the polarization states correspond to "Linearly-polarized", "Circularly-polarized" and "Elliptically-polarized", respectively. In figure 2.9, when linearly-polarized (at 45°) light whose intensities of S and P are the same each other falls on a surface, the polarization of the reflected light turns into the elliptic polarization due to the phase lag. As a result, the differences in the intensities between S and P component arise. S and P components in the electric field vector of reflected light are given by

$$E_S = a_S \cos(\omega t - \delta_S) \quad (2.1)$$

$$E_P = a_P \cos(\omega t - \delta_P) \quad (2.2)$$

where, a_S and a_P are the amplitudes of S and P polarization respectively. δ_S and δ_P express the phase deviations in the each components. Introducing $\delta_P - \delta_S = \Delta$, following equation is obtained.

$$\left(\frac{E_P}{a_P}\right)^2 + \left(\frac{E_S}{a_S}\right)^2 - 2\frac{E_P}{a_P}\frac{E_S}{a_S}\cos\Delta = \sin^2\Delta \quad (2.3)$$

The elliptically polarized light is expressed by this equation. The states of elliptically polarized light are determined by the phase lag Δ and the amplitudes ratio of S and P polarization. Taking the tangent, the amplitudes ratio is expressed by the angle Ψ formed by the meeting of S with P components. $\cos\Delta$ and $\tan\Psi$ are measured and determined by ellipsometer.

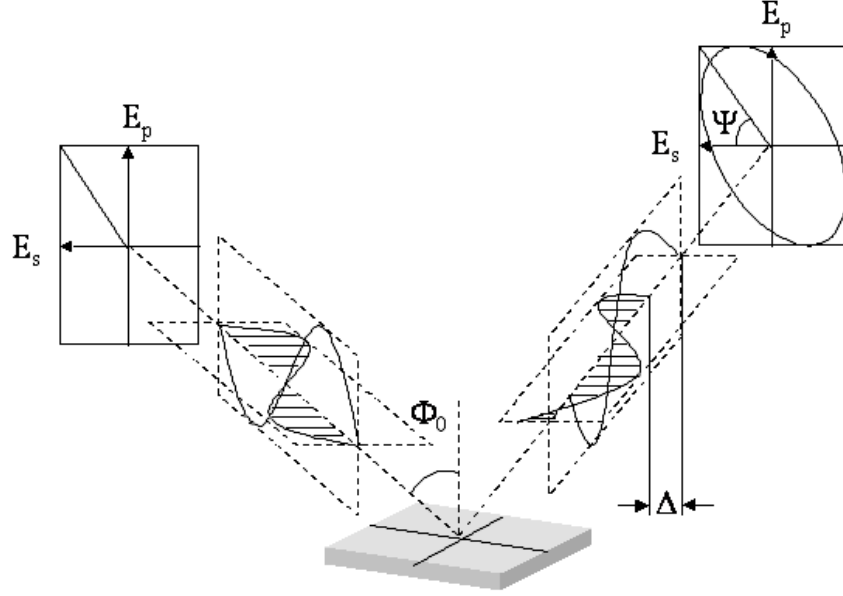


Figure 2.9: The phase lag arises between incident and reflected light.

A typical measurement environment as shown in figure 2.10 are assumed. Structure of measuring object is composed of ambient, thin dielectric film and silicon substrate.

The relationship between S and P components of the reflected light is expressed as

$$\tan\Psi e^{j\Delta} = \frac{R_P}{R_S} \quad (2.4)$$

where, R_P and R_S are complex reflection constant (Fresnel Constant). Giving complex refraction $N_i = n_i - jk_i$, Fresnel constants at each interfaces are given by

$$r_{i,i+1p} = \frac{N_i \cos\Phi_{i-1} - N_{i-1} \cos\Phi_i}{N_i \cos\Phi_{i-1} + N_{i-1} \cos\Phi_i} \quad (2.5)$$

$$r_{i,i+2s} = \frac{N_{i-1} \cos\Phi_{i-1} - N_i \cos\Phi_i}{N_{i-1} \cos\Phi_{i-1} + N_i \cos\Phi_i} \quad (2.6)$$

2.2 Characterization Methods

The phase angle β_i in the i layer film is

$$\beta_i = 2\pi \left(\frac{d_i}{\lambda} \right) N_i \cos \Phi_i \quad (2.7)$$

where d_i is a thickness of i layer, λ is wavelength of incident light and Φ_i is incident angle into the i layer. Using these parameter,

$$R_P = \frac{r_{01p} + r_{12p}e^{-j2\beta_1}}{1 + r_{01p}r_{12p}e^{-j2\beta_1}} \quad (2.8)$$

$$R_S = \frac{r_{01s} + r_{12s}e^{-j2\beta_1}}{1 + r_{01s}r_{12s}e^{-j2\beta_1}} \quad (2.9)$$

Complex refraction in each layer, incident angle and wavelength were substituted, physical thickness of d_1 could be calculated.

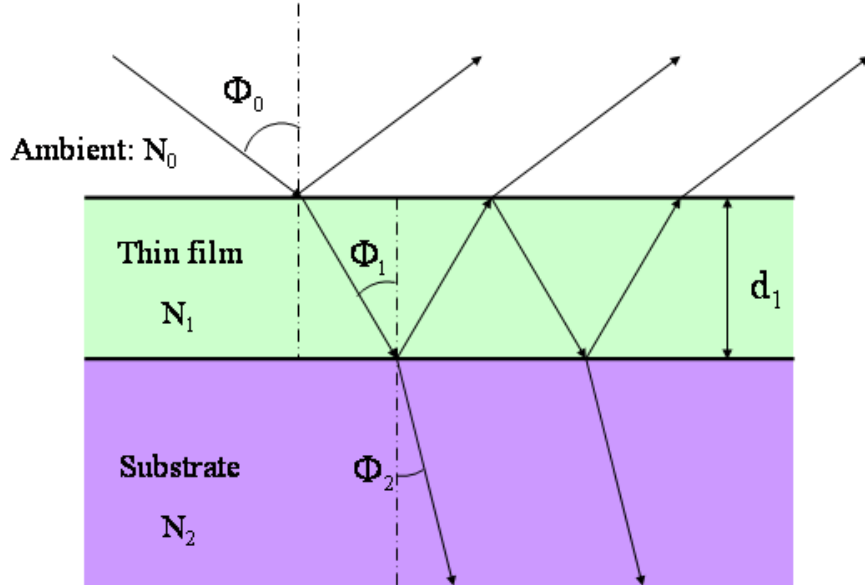


Figure 2.10: The structure of measuring object.

2.2.2 Capacitance - Voltage (C-V) Characteristics

C-V characteristic measurements were performed with various frequencies (1kHz \sim 1MHz) by precision LCR Meter (HP 4284A, Agilent).

The energy band diagram of an MOS capacitor on a p-type substrate is shown in figure 2.11. The intrinsic energy level E_i is taken as the zero reference potential. The surface potential Φ_i is measured from this reference level. Looking at an MOS capacitor from the gate, the gate capacitance is defined as

$$C = \frac{dQ_G}{dV_G} \quad (2.10)$$

where Q_G and V_G are the gate charge and the gate voltage, respectively. That is the change of charge due to a change of voltage. During capacitance measurement, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Since the total charge in the device must be zero, assuming no oxide charge, $Q_G = -(Q_S + Q_{it})$, where Q_S is the semiconductor charge, Q_{it} the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_{FB} + V_{OX} + \Phi_S$, where V_{FB} is the flatband voltage, V_{OX} the oxide voltage, and Φ_S the semiconductor voltage or surface potential, allowing Eq.2.10 to be rewritten as

$$C = -\frac{dQ_S + dQ_{it}}{dV_{OX} + d\Phi_s} \quad (2.11)$$

The semiconductor charge Q_S , in general, consists of hole charge Q_p , space-charge region bulk charge Q_b , and electron charge Q_n . With $Q_S = Q_p + Q_b + Q_n$, Eq.2.11 becomes

$$C = -\frac{1}{\frac{dV_{OX}}{dQ_S + dQ_{it}} + \frac{d\Phi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \quad (2.12)$$

Utilizing the general capacitance definition of Eq.2.10, Eq.2.12 becomes

$$C = \frac{C_{OX}(C_p + C_b + C_n + C_{it})}{C_{OX} + C_p + C_b + C_n + C_{it}} \quad (2.13)$$

Eq.2.13 is represented by the equivalent circuit in figure 2.12(a). For negative gate voltages, the surface is heavily accumulated and Q_p dominates. C_p is very high, approaching a short circuit. Hence, the four capacitances are shorted as shown in 2.12(b). For small positive gate voltages, the surface is depleted and the space-charge region charge, $Q_b = -qN_AW$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of C_{ox} in series with C_b in parallel with C_{it} . In weak inversion C_n begins to appear. Figure 2.12(c) shows the equivalent circuit for weak inversion. For strong inversion, C_n dominates because Q_n is very high. If Q_n is able to follow the applied ac voltage, the low-frequency equivalent circuit (figure 2.12(b)) becomes the oxide capacitance again. This gives the low-frequency C-V curve. When the inversion charge is unable to follow the ac voltage, the circuit in figure 2.12(d) applies in inversion.

The flatband voltage V_{FB} is determined by the metal-semiconductor work function difference Φ_{MS} and the various oxide charges through the relation

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \gamma \frac{Q_m}{C_{ox}} - \gamma \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} \quad (2.14)$$

where Q_m is the mobile oxide charge, Q_{ot} the oxide trapped charge and Q_f the fixed oxide charge. The fixed charge Q_f is located very near the Si-insulator interface and can be considered to be at that interface. Mobile and oxide charges, however, may be distributed throughout the oxide. The effect on flatband voltage is greatest, when the charge is located at the oxide-semiconductor substrate interface, because then it images all of its charge in the semiconductor. When the charge is located at the gate-insulator interface, it images all of its charge in the gate and has no effect on the flatband voltage.

In the study, principally, EOT values and flatband voltage were extracted from C-V characteristics. EOT values were calculated from the corrected C-V data with taking quantum effect into account. The permittivities of gate dielectrics

2.2 Characterization Methods

were estimated as below.

$$\varepsilon_{high-k} = \varepsilon_{SiO_2} \frac{t_{phy}}{EOT} \quad (2.15)$$

where, ε_{high-k} is the permittivity of high-k dielectrics (La₂O₃, Y₂O₃ and their stack in this study), ε_{SiO_2} is the SiO₂ permittivity of 3.9 and t_{phy} is a physical thickness of dielectric film measured by ellipsometer.

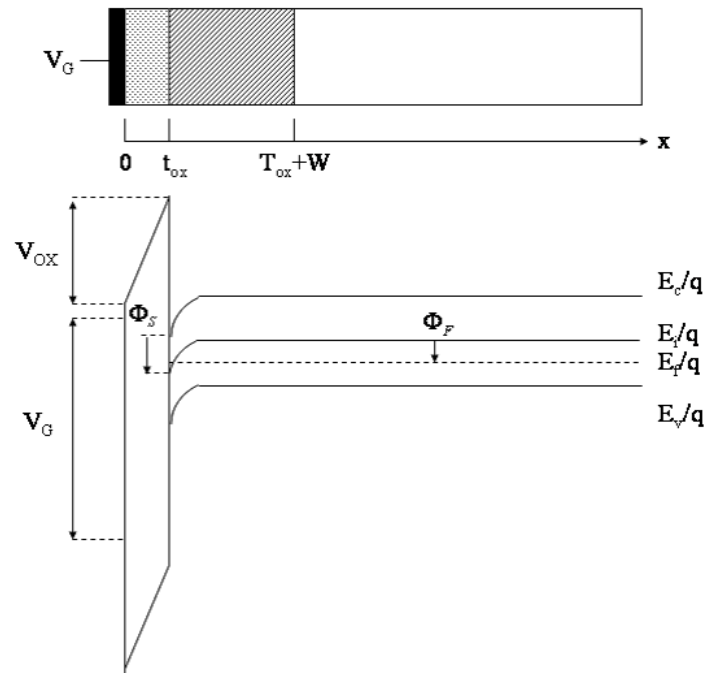


Figure 2.11: Cross section and potential band diagram of an MOS capacitor.

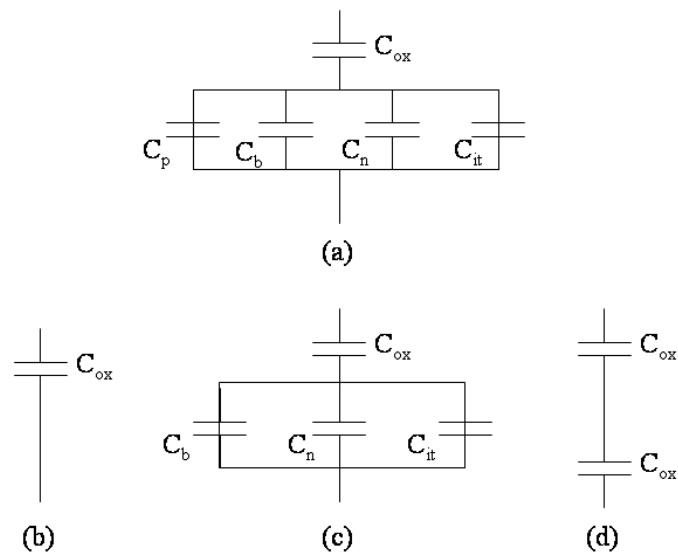


Figure 2.12: Capacitances of an MOS capacitor for various bias conditions.

2.2.3 Gate Leakage Current - Voltage (J-V) Characteristic

It is known that there are several types of conduction mechanism: Fowler Nordheim (F-N) conduction, Direct tunneling, Pool-Frenkel (PF) and Space Charge Limited currents (SCLC) etc. The main conduction mechanisms are the SCLC at low oxide field region and F-N conduction at high oxide field region[24]-[27] (figure 2.13). In the case of thin oxide film, the direct tunneling current dominates as mentioned in section 1.2.

Although further consideration to conduction mechanisms has not been made in this study, it pays to know the leakage current mechanisms.

The SCLC mechanism relies on the trap density distributed energetically and spatially in the oxide film. F-N conduction occurs when electrons tunnel into the conduction band of the dielectric film. F-N tunneling current is characterized by a straight line in a plot of $\log(J/E_{ox})$ versus $1/E_{ox}$. More important thing is leakage current caused by these conduction mechanisms are partially contributed by the electron concentration due to oxygen Frenkel defect and oxygen vacancy i.e. leakage current is correlated with trap density at the interface and in the oxide.

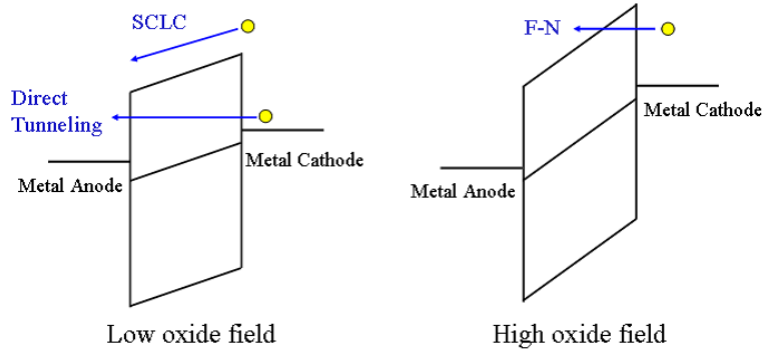


Figure 2.13: Main conduction mechanisms in La_2O_3 dielectric

2.2.4 Atomic Force Microscopy (AFM)

AFM measurement enables to characterize the surface morphology by utilizing the force between atoms and approached tip. The surface roughness was obtained precisely by observing x-y plane and z direction. Figure 2.14 illustrates the principle of AFM measurement.

Tip was being vibrated during measurement, then displacement of z direction was detected. This method is known as tapping mode AFM (TM-AFM). Ordinarily resolution limit for normal AFM is about 5nm ~ 10nm depending on the distance between sample surface and tip. On the other hand, since the limit for TM-AFM depends on size of tip edge, resolution limit is approximately 1nm. Hence, TM-AFM makes more precise measurements possible.

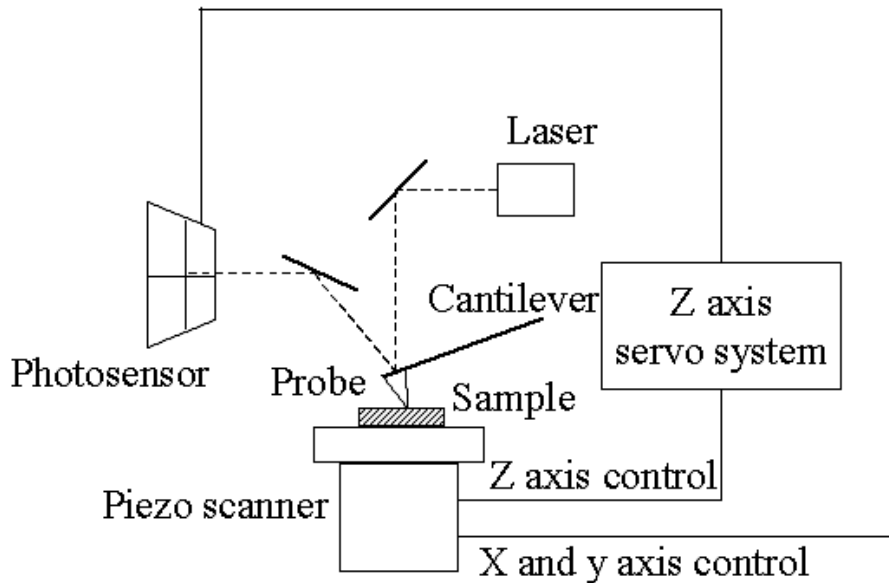


Figure 2.14: Schematic AFM principle.

2.2.5 X-ray Photoelectron Spectroscopy (XPS)

XPS, also known as the Electron Spectroscopy for Chemical Analysis (ESCA), is one of the useful methods to evaluate chemical bindings in the oxide or at the interface.

XPS equipments are shown in figure 2.15. The degree of pressure in the main chamber during the measurements was maintained at approximately 10^{-9} torr by turbo pump. Samples were irradiated with monoenergetic soft X-ray and the emitted photoelectrons with kinetic energy KE were detected. Measured KE was given by

$$KE = h\nu - BE - \phi_s \quad (2.16)$$

where $h\nu$ is the photon energy, BE the binding energy of the atomic orbital from which the electron generates and ϕ_s the spectrometer work function of 4.8 eV. Non-monochromatic $MgK\alpha$ with $h\nu$ of 1253.6 eV was used as a X-ray source.

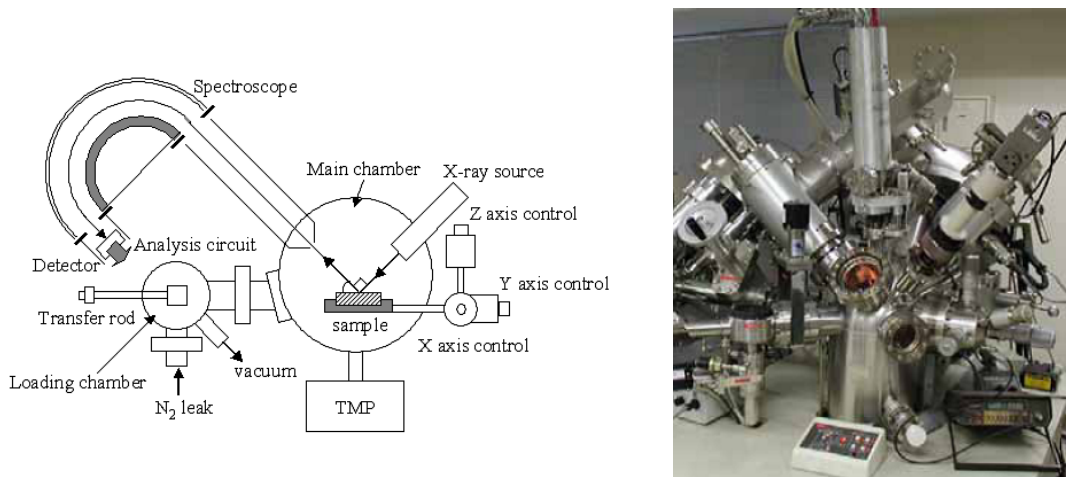


Figure 2.15: Schema and photo of XPS equipment

Figure 2.16 explains the principle of XPS. The binding energy is the minimum energy needs for breaking the chemical bond of molecule and is inherent in each bond of molecule. Thus, the binding states can be identified by the positions of the binding energy which the peak appears. In the case that the peak position was different from the expected position, the chemical bond states were discussed considering the amount of shift to higher or lower energy side.

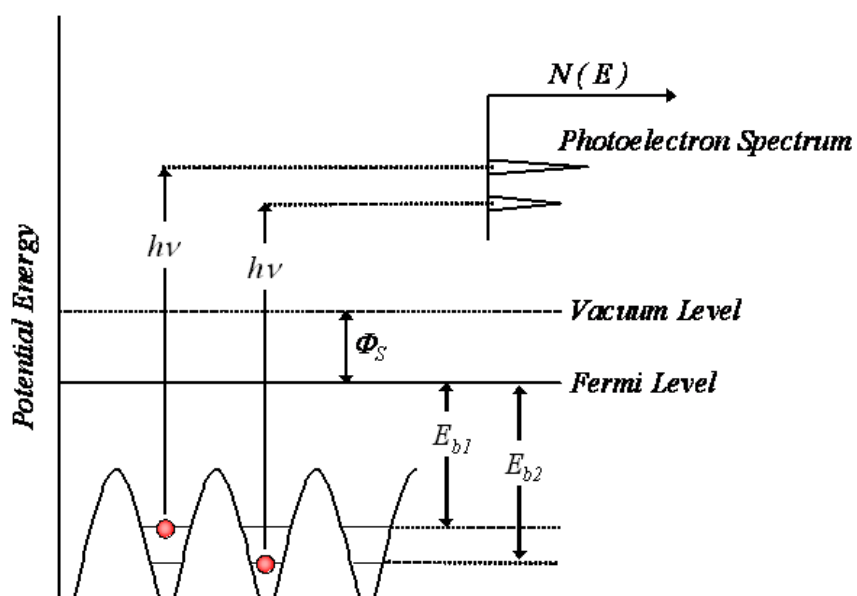


Figure 2.16: Principle of XPS measurement.

2.2.6 **Advanced XPS Analyses by Super Photon ring- 8 GeV (SPring-8)**

SPring-8 is the one of the world's largest radiation facilities. The advantages of SPring-8 over average XPS equipments are the high-brightness of radiation which is about a hundred thousand times as high as normal X-ray and the high radiation energy of 30keV \sim 40keV.

The schematic view of SPring-8 facilities are depicted in figure 2.17. The electrons generated by E-gun are accelerated by linear-accelerator up to 1 GeV. Additionally, the ellipsoid-shaped synchrotron accelerates the electron and delivers them to the strage ring. The strage ring with diameter of 500 m can preserve the electrons keeping the energy at 8 GeV for more than 100 hours. The principle of radiation emission is shown in figure 2.18. As the electron with a speed close to light passes through the magnetic field, the track of electron is bent and radiate electromagnetic wave in the tangential direction of track. The radiation has the wide range spectrum from micro wave to x-ray, additionally, good directivity and polarization. For such qualities, the radiation has been utilized in many scientific technology fields as the best light source in the wavelength ranging from vacuum ultraviolet ray to x-ray.

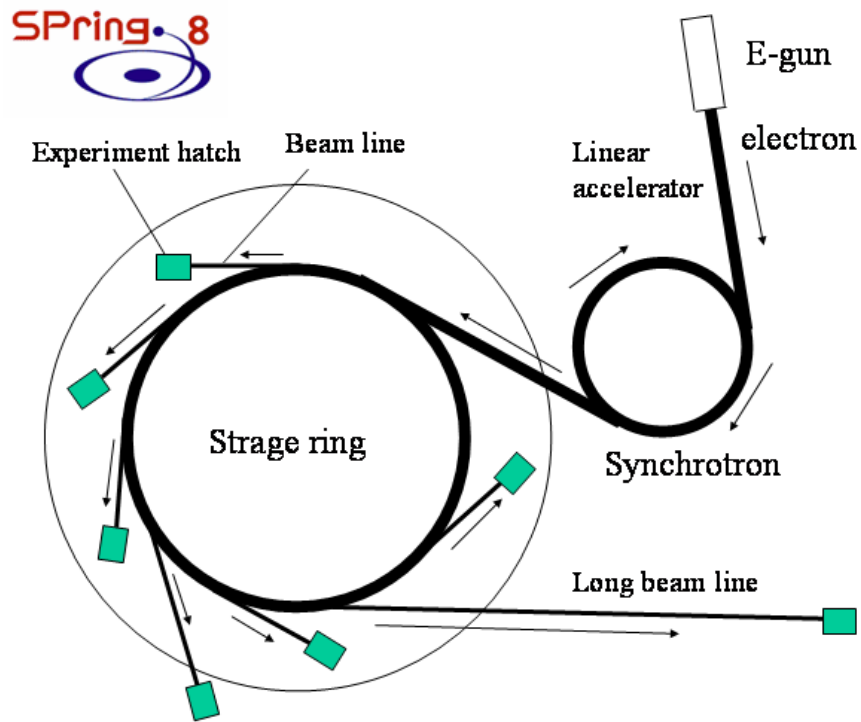


Figure 2.17: The schematic view of SPring-8 facilities.

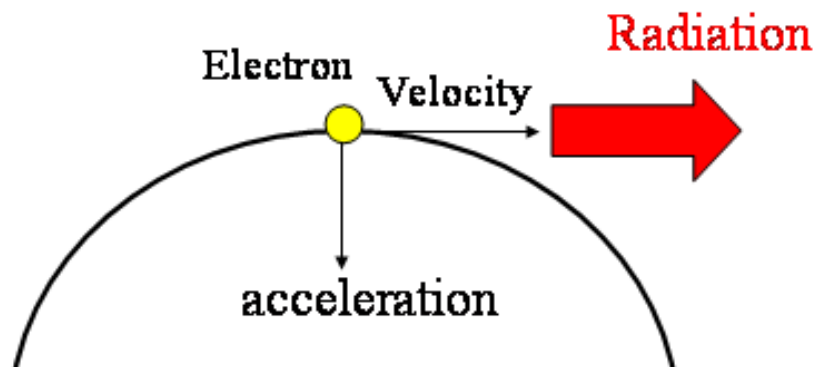


Figure 2.18: The principle of radiation emission.

2.2.7 Split C-V Method for Effective Mobility Measurements

In general, high-k dielectrics degrade channel carrier mobility, so the measurements and analyses of mobility are necessary. The mobility measurements were performed by conventional split C-V method. The schematic flow of split C-V method is shown in figure 2.19. In the split C-V method, the gate to channel capacitance C_{gc} and the gate to bulk capacitance C_{gb} are measured independently (a). C_{gc} was measured by connecting the high lead of the LCR meter to the gate electrode and the low lead to source and drain terminals, the substrate being grounded while C_{gb} was by connecting the low lead to the bulk, high lead to the gate, and the source and drain being grounded.

The inversion layer charges Q_{inv} and the bulk depletion charges Q_{bd} (shown in figure 2.19(b)) were extracted from C_{gc} and C_{gb} by following equations.

$$Q_{inv} = \int_{V_{ga}}^{V_g} C_{gc} dV_g \quad (2.17)$$

$$Q_{bd} = \int_{V_{fb}}^{V_g} C_{gb} dV_g \quad (2.18)$$

where V_{ga} is a voltage in accumulation region and V_{fb} the flatband voltage.

The effective mobility μ_{eff} is calculated as follow.

$$\mu_{eff} = \frac{g_D L}{W Q_{inv}} \quad (2.19)$$

where L is the gate length, W the gate width and the drain conductance g_D (shown in figure 2.19(C)) is defined as

$$g_D = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}=\text{constant}} \quad (2.20)$$

Experimental effective mobility data follow a universal curve reference independent of the substrate impurity concentration and back-biasing of the device, if plotted as a function of the transverse effective electric field E_{eff} :

$$E_{eff} = \frac{Q_{bd} + \eta Q_{inv}}{\epsilon_{si}} \quad (2.21)$$

2.2 Characterization Methods

where η accounts for averaging of the electric field over the electron distribution in the inversion layer. The parameter η is usually taken as $\eta=1/2$ for the electron mobility and $1/3$ for the hole mobility. ϵ_{si} denotes the dielectric constant of silicon. The representative effective mobility versus effective electric field is demonstrated in figure 2.19(d).

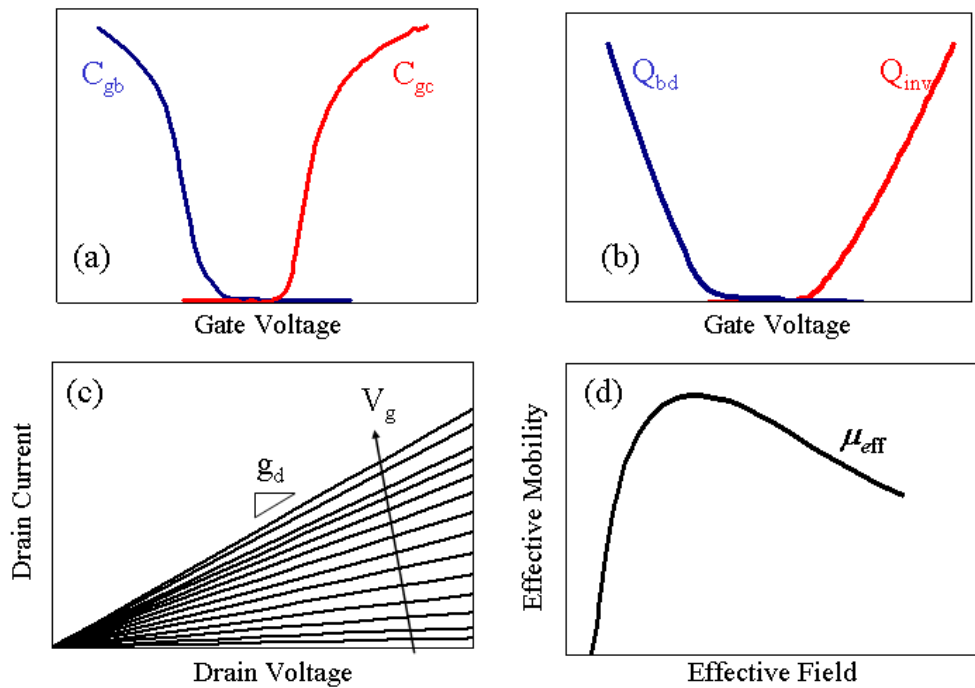


Figure 2.19: Schematic flow of Split-CV method

2.2.8 Charge Pumping Methods

Charge Pumping (CP) is a very sensitive method for the characterization of interface traps which are located at the gate dielectric-silicon interface of MOSFET. Circuit diagram for the CP measurements are shown in figure 2.20. The MOSFET gate is connected to a pulse generator. MOSFET source and drain are tied together and slightly reverse biased with voltage V_R . The time varying gate voltage is of sufficient amplitude for the surface under the gate to be driven into inversion and accumulation. The charge pumping current I_{CP} is measured at the substrate. I_{CP} is caused by the repetitive recombination of minority carriers with majority carriers at the interface traps when the gate pulses the channel between inversion and accumulation.

The pulse train can be square, triangular, trapezoidal, sinusoidal, or trilevel. Among them, square, triangular and trapezoidal pulse waveforms were used for charge pumping measurements. These methods are described below.

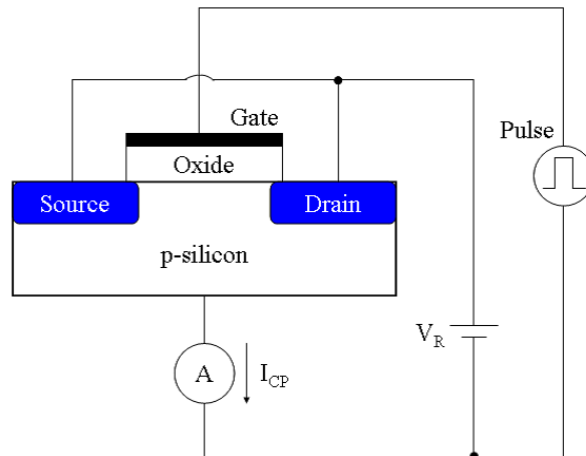


Figure 2.20: The measurement circuit for charge pumping method.

Square Pulse Method Timing chart of square pulse method and the parameter definitions in the waveform are shown in figure 2.21 schematically.

The waveforms can be constant base voltage in accumulation and pulsing with varying the base voltage from inversion to accumulation keeping ΔV constant. The square pulse method extracts the interface-state density from the I_{CP} versus the pulse base voltage curve. The interface-state density D_{it} is given by

$$\overline{D_{it}} = \frac{I_{cp}}{f \cdot q \cdot A_g} \quad (2.22)$$

where f is pulse frequency, q the electron charge, A_g the channel area of the transistor and $\overline{D_{it}}$ the mean interface-state density, averaged over the energy levels swept through by the Fermi level.

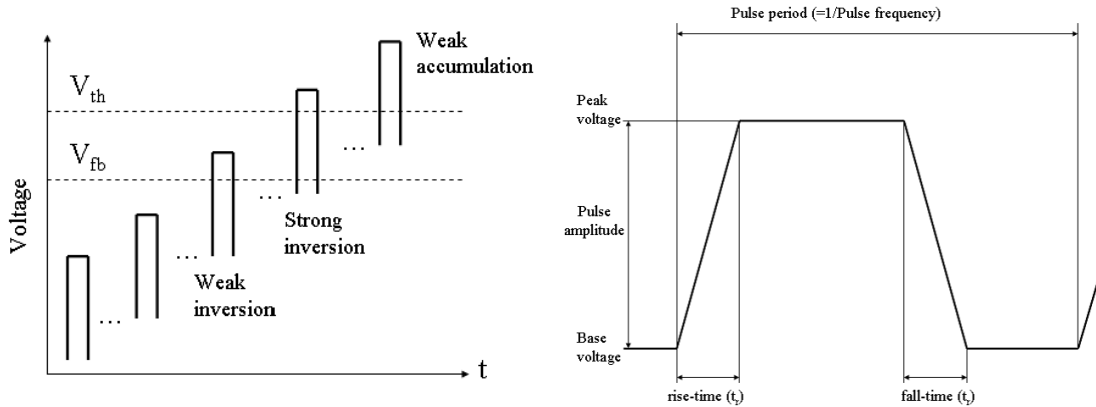


Figure 2.21: Timing chart of square pulse method and the parameter definitions in the waveform

Triangular Pulse Method The triangular pulse method extracts the mean interface-state density $\overline{D_{it}}$ and capture cross section σ from the recombined charge versus the pulse frequency curve.

Timing chart of triangular pulse method and the parameter definitions in the waveform are shown in figure 2.22 schematically. The curve is obtained by applying a constant height triangle wave to the gate, measuring the charge pumping current, stepping up the pulse frequency, repeating the measurement, and extracting the recombined charge. The mean interface-state density ($\overline{D_{it}}$) is extracted using the following equation, where, *Slope* is the slope of the regression line for the recombined charge Q_{ss} versus pulse frequency f curve on a linear-log graph.

$$Slope = \frac{dQ_{ss}}{d \log f} = \frac{2qkT\overline{D_{it}}}{\log e} A_g \quad (2.23)$$

$$\overline{D_{it}} = \frac{\log e \cdot Slope}{2qkT A_g} \quad (2.24)$$

where Q_{ss} is the recombined charge per pulse period, k the boltzmann's constant, T the temperature.

The mean capture cross section $\sigma = \sqrt{\sigma_n \sigma_p}$ was calculated using following equation.

$$\sigma = \frac{1}{v_{th} \cdot n_i} \frac{|V_{GH} - V_{GL}|}{|V_{fb} - V_{th}|} \frac{f_0}{\sqrt{\alpha \cdot (1 - \alpha)}} \quad (2.25)$$

where σ_n is the capture cross section of electrons, σ_p the capture cross section of holes, v_{th} the thermal velocity of the carriers, n_i the intrinsic carrier concentration, V_{GH} the pulse peak voltage, V_{GL} the pulse base voltage and $\alpha = t_r / (t_r + t_f)$ is the gate pulse duty cycle, where t_r is the pulse rise time and t_f the pulse fall time.

2.2 Characterization Methods

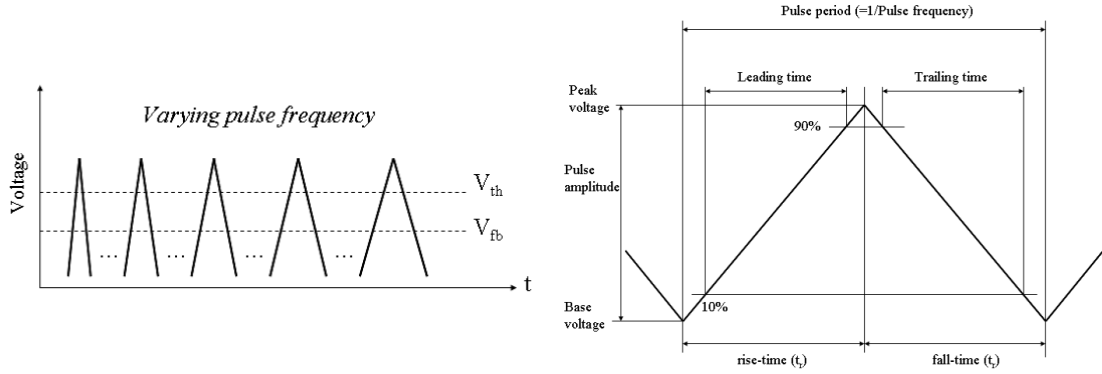


Figure 2.22: Timing chart of triangular pulse method and the parameter definition in the waveform

Trapezoidal Pulse Method The basic charge pumping technique gives an average value of D_{it} over the energy interval ΔE , however, it does not give an energy distribution of the interface trap densities. Trapezoidal pulse method gives an energy distribution of the interface traps.

Timing chart of trapezoidal pulse method and the parameter definitions in the waveform are shown in figure 2.23 schematically. For a trapezoidal waveform, the amplitude of the pulse is held constant while the rise-time t_r and the fall-time t_f of the pulse are varied. The substrate leakage current is measured for each change of the pulse transient time (rise-time or fall-time). For each sampling measurement, the averaged substrate current is defined as the charge pumping current I_{CP} . First, I_{CP} is measured while varying the fall-time of the pulse constant and keeping the rise-time of the pulse constant. Next, I_{CP} is measured while varying the rise-time of the pulse constant and keeping the fall-time of the pulse constant. The energy distribution of interface-states is obtained by following

2.2 Characterization Methods

equation.

$$E_1 = E_i + kT \ln \left(v_{th} \sigma_p n_i t_r \frac{|V_{fb} - V_{th}|}{|V_{GH} - V_{GL}|} \right) \quad (2.26)$$

$$\overline{D_{it1}} = -\frac{t_r}{q A_g k T f} \frac{dI_{CP}}{dt_r} \quad (2.27)$$

$$E_2 = E_i - kT \ln \left(v_{th} \sigma_n n_i t_f \frac{|V_{fb} - V_{th}|}{|V_{GH} - V_{GL}|} \right) \quad (2.28)$$

$$\overline{D_{it2}} = -\frac{t_f}{q A_g k T f} \frac{dI_{CP}}{dt_f} \quad (2.29)$$

where E_1 is the energy below the intrinsic level, E_2 the energy over the intrinsic level, E_i the center level of the forbidden band, D_{it1} the interface-state density for E_1 and D_{it2} the interface-state density for E_2 .

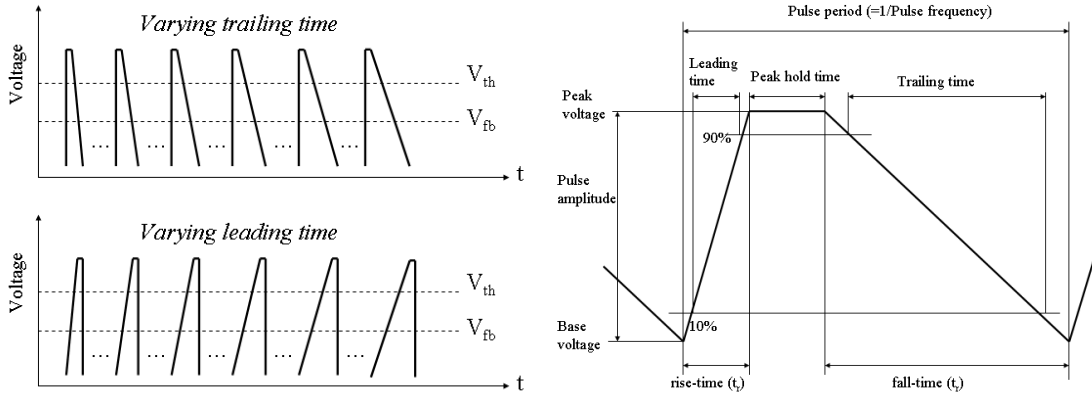


Figure 2.23: Timing chart of trapezoidal pulse method and the parameter definition in the waveform

Chapter 3

THE ELECTRICAL CHARACTERISTICS OF N-MOS CAPACITORS

3.1 Al gated n-MOS Capacitors

3.1.1 Introduction

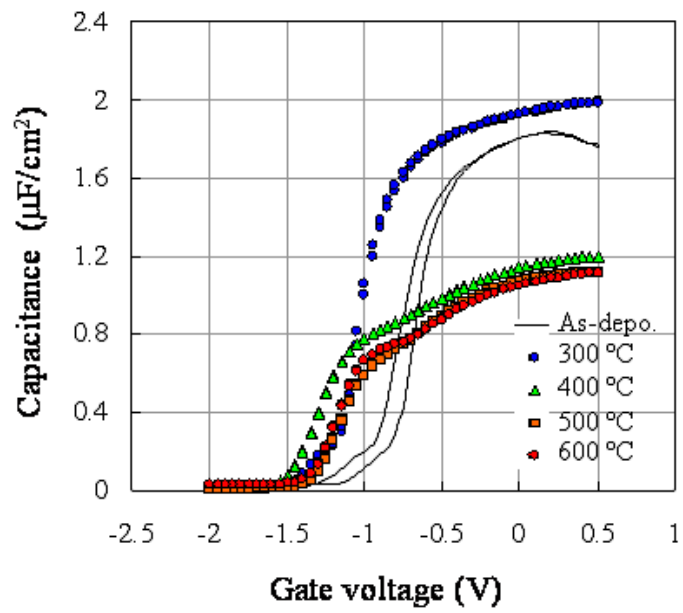
The n-MOS capacitors with $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack dielectric were fabricated, besides La_2O_3 and Y_2O_3 monolayer samples. The detail fabrication process was mentioned in section 2.1. The substrate temperature during deposition was kept at a constant temperature of 250 °C. Al was deposited on dielectrics as gate electrodes. RTAs were performed under O_2 and N_2 ambient.

3.1.2 La_2O_3 Monolayer

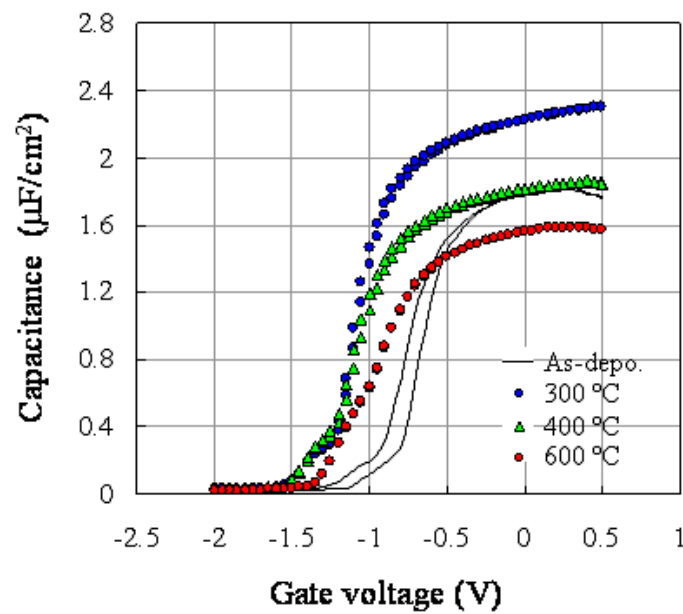
Figure 3.1 shows the CV characteristics (measurement frequency was 100kHz) that are for the samples with PDAs in (a) O_2 or (b) N_2 at 300 °C - 600 °C for 5 minutes. Both of the results (a) and (b), the capacitance decreased with increase of annealing temperature, indicating the growth of the interfacial layer. Taking note of more increase of capacitance for the sample annealed at 300 °C rather than as-deposited sample, this might be caused by moisture absorbent of La_2O_3 film and a thickness distended. The distended film was improved by heat treatment.

Figure 3.2 shows the CV characteristics with measurement frequencies.

In the case that the samples with PDAs in O_2 , the frequency dispersions in a transverse direction were observed except for 300 °C annealing and the slight bumps in the center of the curve were observed. These might be caused by the growth of interfacial layer, such as SiO_x and La-silicate and SiO_x would behave as the positive charge so that the electrons were trapped in the interface states. However, in the case of N_2 PDAs, less frequency dispersions than O_2 annealing were observed because the growth of the interfacial layer was limited compared to O_2 annealing.



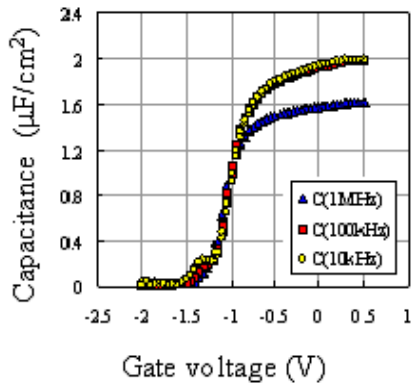
(a) Annealed in O_2



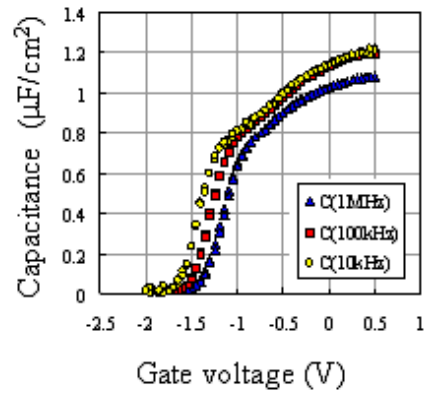
(b) Annealed in N_2

Figure 3.1: Comparison of C-V measured at 100 kHz with each annealing temperatures in (a) O_2 ambient and (b) N_2 ambient.

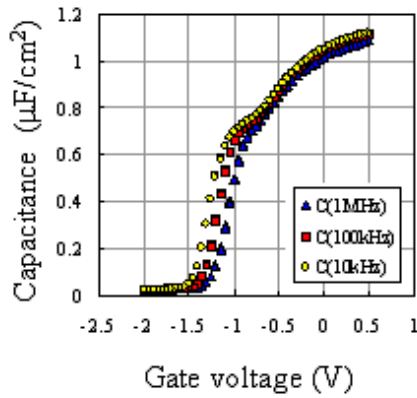
3.1 Al gated n-MOS Capacitors



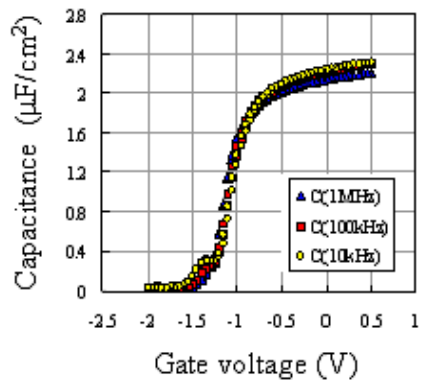
(a) 300 °C in O₂



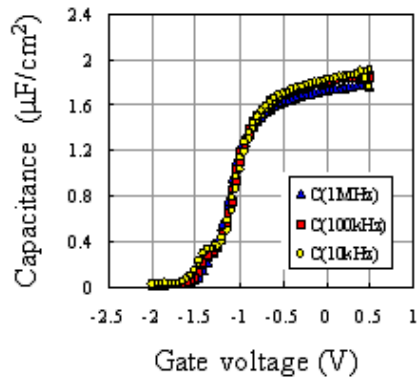
(b) 400 °C in O₂



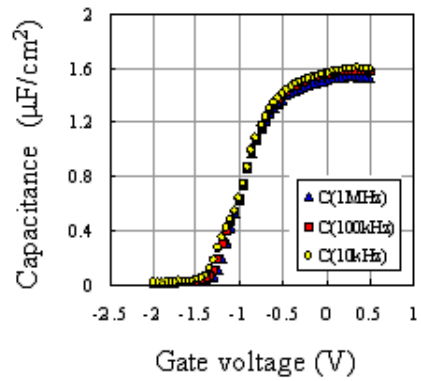
(c) 600 °C in O₂



(d) 300 °C in N₂



(e) 400 °C in N₂



(f) 600 °C in N₂

Figure 3.2: CV characteristics of La₂O₃ monolayer samples annealed in O₂ and N₂.

3.1 Al gated n-MOS Capacitors

The thickness of as-deposited sample was 4.6 nm and the relationships of EOT to annealing conditions are shown in figure 3.3.

For the samples with PDAs in O₂, although EOT was maintained small value up to 300 °C, both EOT and t_{phy} increased precipitously from 400 °C. This indicates that the growth of the interfacial layer proceeded from the temperature 400 °C. However, the increasing amount of EOT from 400 °C to 600 °C was not so much. The interfacial layer growth might be gradually saturated.

For the samples with PDAs in N₂, EOT and t_{phy} seem to increase lineary, however, the increasing amount of them was not as much as that of in O₂ annealing case, indicating the growth of the interfacial layer was hard to proceed in N₂ ambient compared to O₂ ambient.

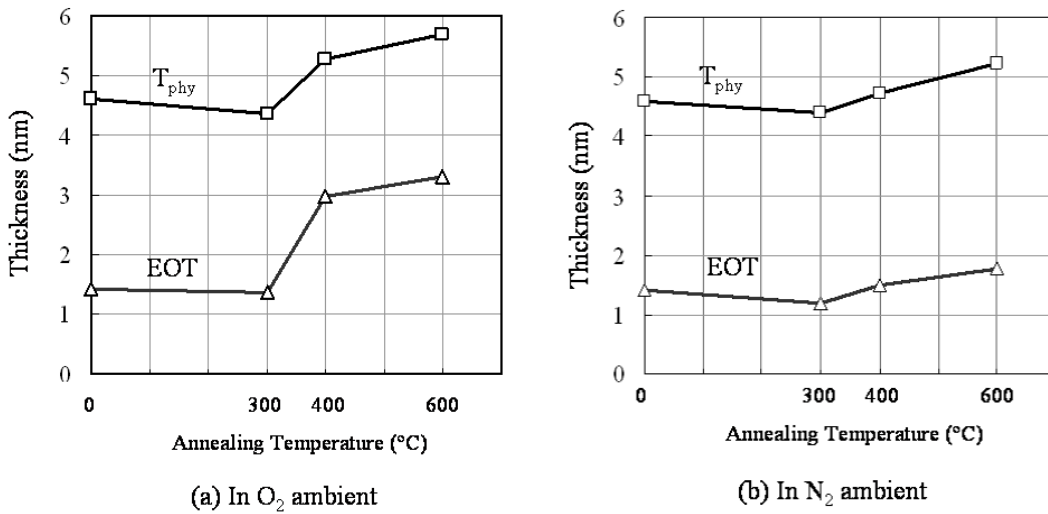


Figure 3.3: The relation of EOT and t_{phy} to annealing temperature for the samples with La₂O₃.

3.1 Al gated n-MOS Capacitors

Figure 3.4 shows the J-V characteristics compared between annealing temperatures for (a) O₂ (b) N₂ annealing.

For the samples with O₂ PDA at 300 °C, leakage current density level was subequal to that of as-deposited. The magnitude of leakage current density became smaller with increase of the annealing temperature because of the increase of the EOT value from 300 °C to 400 °C as shown in figure 3.3 (a). The leakage current density for the 400 °C PDA sample was three orders magnitude less than that of 300 °C. And it was reduced another two orders by 600 °C annealing.

In the case of N₂ PDA, 600 °C annealed sample showed the slight reduction of leakage current. However, the leakage current level of 400 °C PDA sample was almost the same as 300 °C sample.

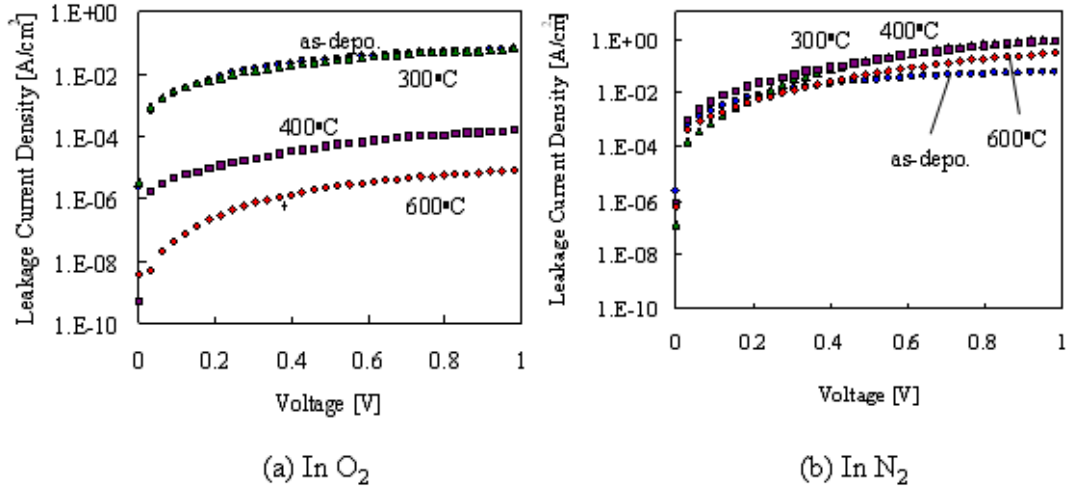


Figure 3.4: The J-V characteristics of La₂O₃ film.

3.1.3 Y₂O₃ Monolayer

Figure 3.1 shows the CV characteristics (measurement frequency was 100kHz) that are for the samples with PDAs in (a) O₂ or (b) N₂ at 300 °C - 600 °C for 5 minutes.

For the samples with O₂ PDA, the accumulation capacitance decreased with increase of annealing temperature, indicating the growth of the interfacial layer. However, the decreasing amount of capacitance from 500 °C to 600 °C was very slight. The pace of the interfacial layer growth might become slowly around 500 °C. The point different from La₂O₃ monolayer is that as-deposited sample had the highest accumulation capacitance. This is the evidence of having the resistance to moisture.

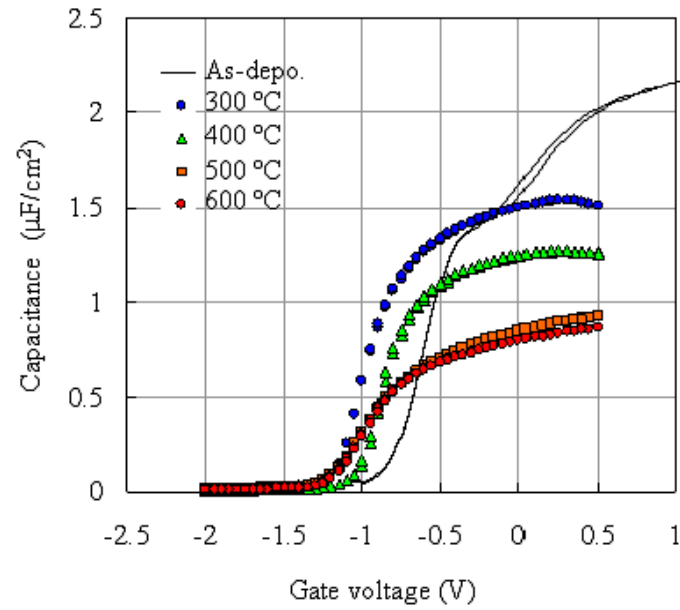
For the samples with N₂ PDA at 300 °C or 400 °C, they had the almost same capacitance value. Increasing the annealing temperature up to 600 °C, capacitance decreased. In the case of N₂ annealing, the growth of interfacial layer proceeded rapidly between 400 °C and 600 °C.

The CV characteristics compared between the measurement frequencies of 1MHz, 100kHz and 10kHz are shown in figure 3.6.

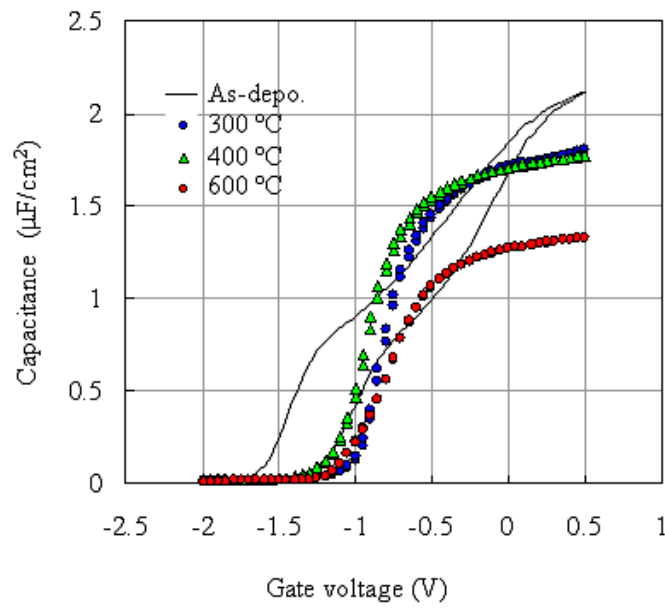
For the samples with O₂ PDA at 300 °C and 400 °C, there were almost no frequency dispersions and hysteresis. And the slight bump which was observed in CV curve for La₂O₃ monolayer was not observed. For the 600 °C PDA sample, frequency dispersions were observed.

In the case that the samples with N₂ PDA, although there were no hysteresis, the accumulation capacitance dropped at 1MHz. There might be the capacitance component which was not able to follow high frequency.

3.1 Al gated n-MOS Capacitors



(a) In O_2



(b) In N_2

Figure 3.5: Comparison of C-V measured at 100 kHz with each annealing temperatures in (a) O_2 ambient and (b) N_2 ambient.

3.1 Al gated n-MOS Capacitors

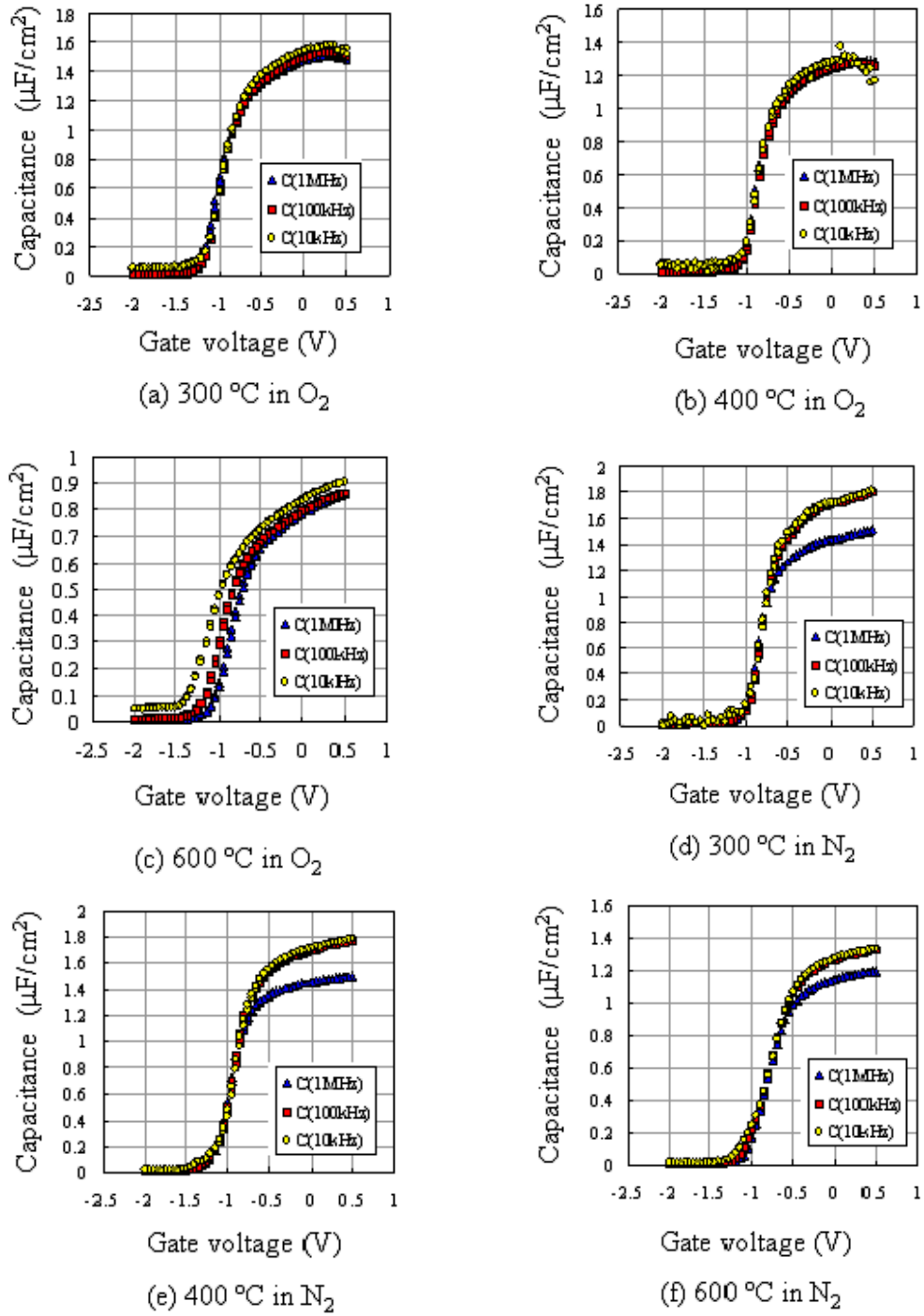


Figure 3.6: CV characteristics of Y_2O_3 monolayer samples annealed in O_2 and N_2 .

3.1 Al gated n-MOS Capacitors

Relationships of EOT and t_{phy} to annealing conditions are shown in figure 3.7.

In the both of the cases O_2 PDA and N_2 PDA, marked increase of t_{phy} were not observed and it increased in propotion as annealing temperature. EOT increased with increase of annealing temperature for O_2 annealed samples, especially slope of a line between 400 °C and 600 °C became steeper indicating the growth of the interfacial layer which had lower dielectric constant.

For N_2 annealed samples, the increasing amount of EOT was not so much up to 400 °C. However, EOT value of 600 °C PDA sample increased a little as well as in O_2 ambient. The growth of the interfacial layer was suppressed by annealing in N_2 .

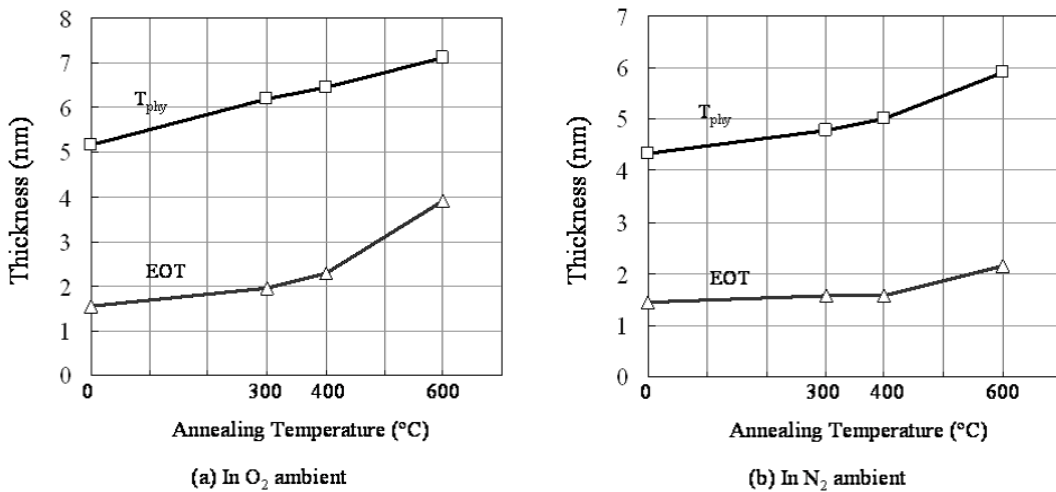


Figure 3.7: The relation of EOT and t_{phy} to annealing temperature for the samples with Y_2O_3 .

3.1 Al gated n-MOS Capacitors

Figure 3.8 shows the JV characteristics of the samples with Y_2O_3 annealed in (a) O_2 or (b) N_2 .

There were hardly any differences in the leakage current density measured at 1 V between each annealing conditions for the samples with O_2 PDAs. The leakage current density level at 1 V was about $10^{-3}(A/cm^2)$ order.

In the case of N_2 PDA, the leakage current was reduced with increase of annealing temperature. Comparing the samples annealed at 300 °C and 400 °C, the leakage current density level at 1 V was almost the same ($10^{-1}(A/cm^2)$) and reduced to $10^{-3}(A/cm^2)$ order by annealing at 600 °C.

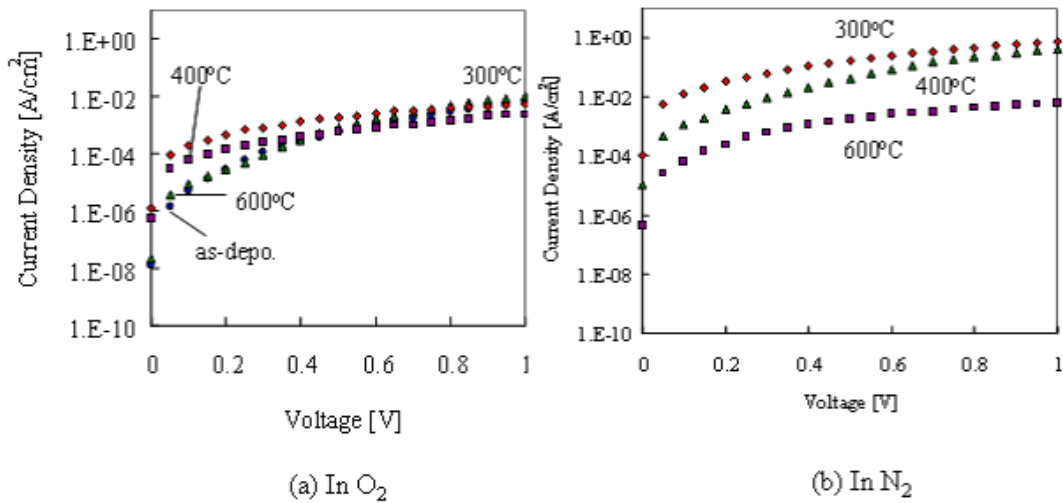


Figure 3.8: The J-V characteristics of Y_2O_3 film.

3.1.4 $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ Stack

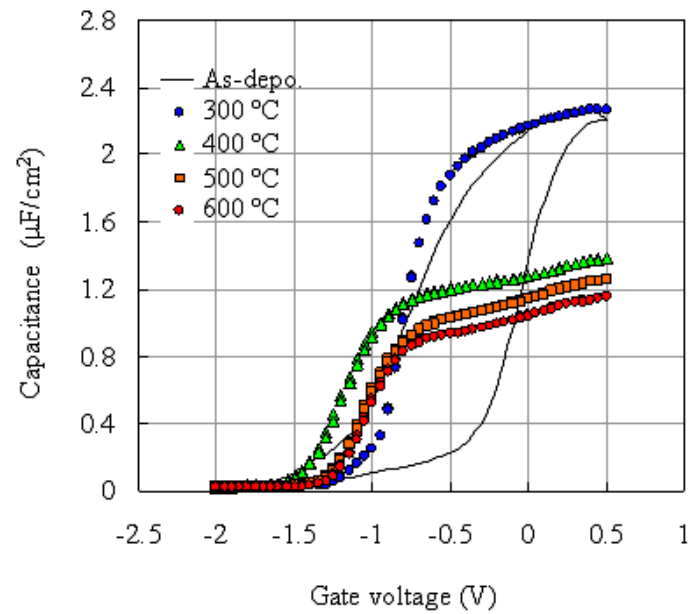
Figure 3.9 shows the CV characteristics measured at 100 kHz. Samples with $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack dielectric were annealed in (a) O_2 or (b) N_2 ambient at 300 °C - 600 °C for 5 minutes. Both La_2O_3 and Y_2O_3 were deposited about 1.7 nm and 1.7 nm, respectively.

For the as-deposited sample, large hysteresis was observed and the capacitance value equal to that of 300 °C sample. The accumulation capacitance decreased considerably as the samples were annealed in O_2 at more than 400 °C and decreasing amount of capacitance became smaller with annealing temperature.

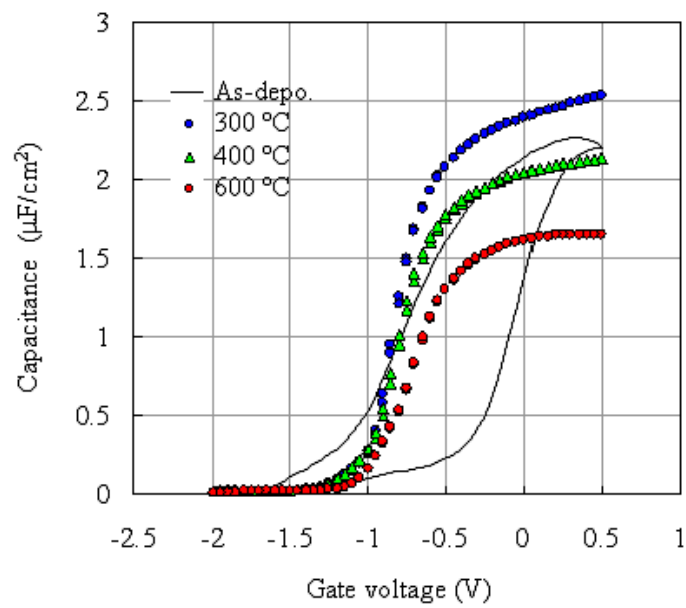
In the case that the samples were annealed in N_2 , capacitance for 300 °C sample was the highest of all and higher than that of as-deposited. The decreasing amount of capacitance with high temperature annealing was not so large. As was expected, the growth of the interfacial layer seemed not to proceed as annealed in N_2 .

The CV characteristics compared between measurement frequencies of 1MHz, 100kHz and 10kHz are shown in figure ???. The frequency dispersions were observed for the samples with O_2 PDA at more than 400 °C while in the case of N_2 annealing, dispersions were not observed. The slight bump around the weak inversion region which was observed in results of La_2O_3 was eliminated. The effect of Y_2O_3 buffer layer on the interface states between dielectric and Si was confirmed.

3.1 Al gated n-MOS Capacitors



(a) In O_2



(b) In N_2

Figure 3.9: Comparison of C-V measured at 100 kHz with each annealing temperatures in (a) O_2 ambient and (b) N_2 ambient.

3.1 Al gated n-MOS Capacitors

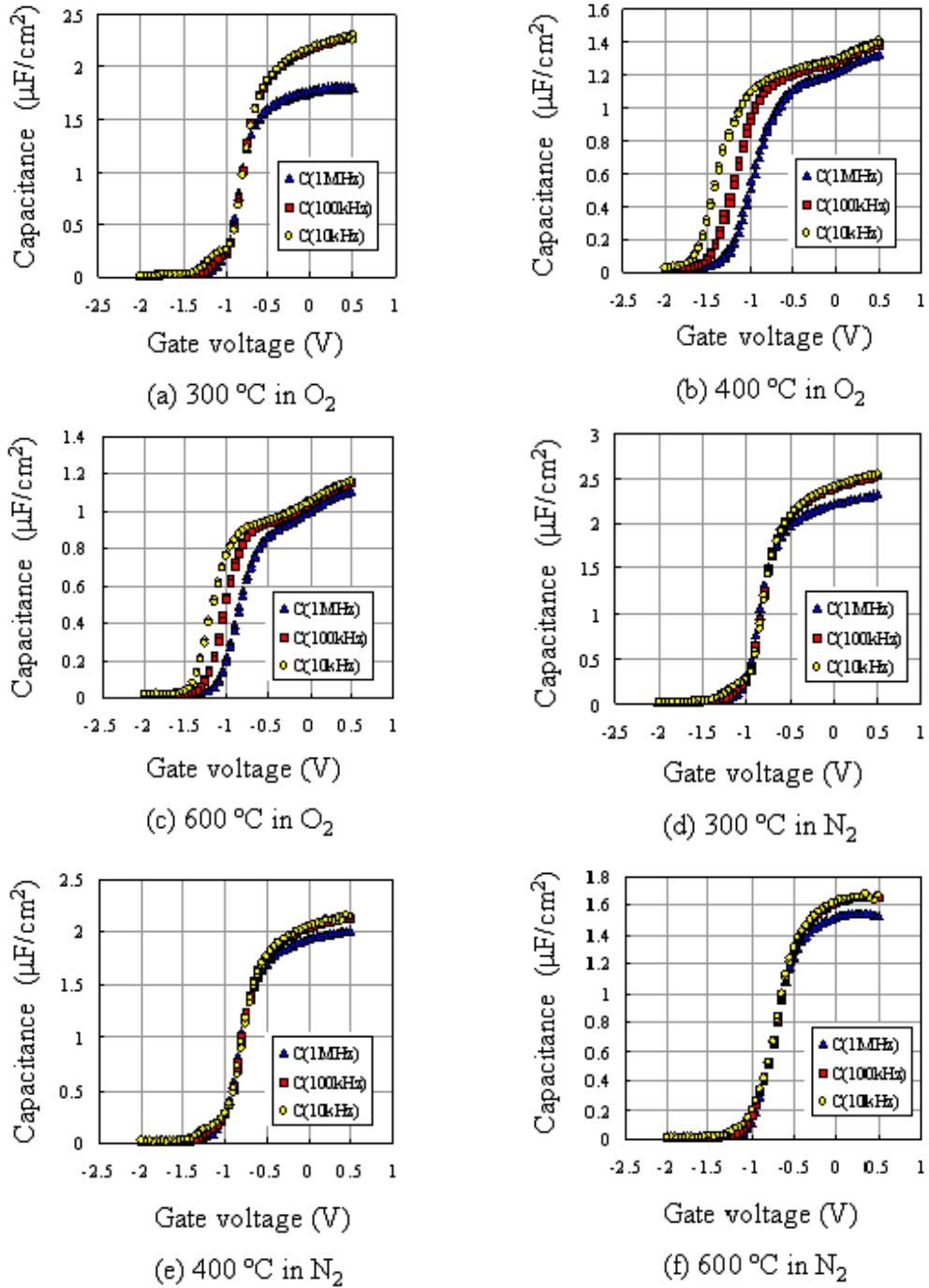


Figure 3.10: CV characteristics of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack samples annealed in O_2 and N_2 .

3.1 Al gated n-MOS Capacitors

Relationships of EOT and t_{phy} to annealing conditions are shown in figure 3.11 (a) O_2 PDA and (b) N_2 PDA.

For the samples with 300 °C PDA in O_2 and N_2 , small EOT of 1.1 nm and 1.0 nm respectively were obtained. However, EOT increased as annealed at 400 °C in O_2 . The growth of the interfacial layer proceeded by annealing at more than 400 °C while the growth rate of interfacial layer became slowly for 600 °C PDA sample.

For the samples with N_2 PDA, EOT and t_{phy} increased lineary with annealing temperature. The slope of EOT line was slightly steeper than the slope of t_{phy} . This indicates that a dielectric constant of the interfacial layer grown at the interface was a little bit lower. EOT of 600 °C PDA sample was 1.6 nm.

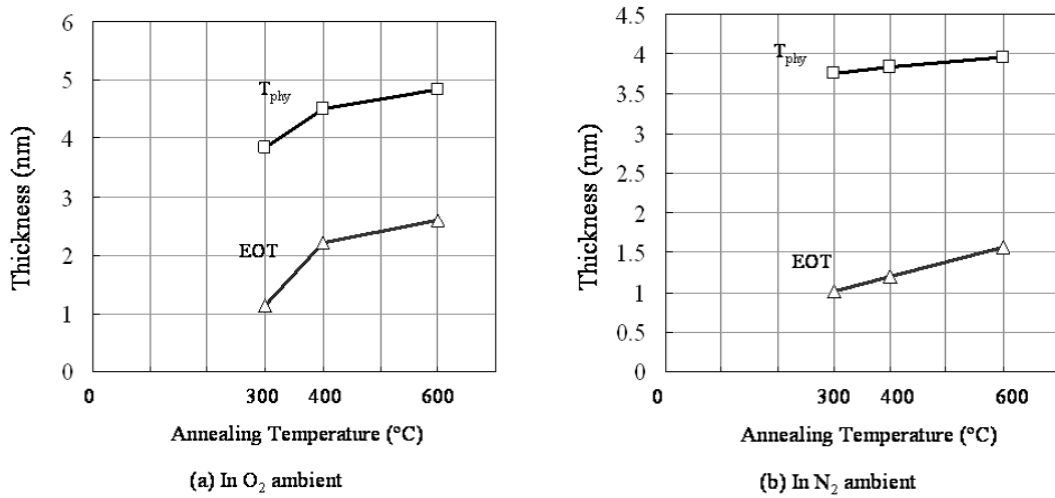


Figure 3.11: The relation of EOT and t_{phy} to annealing temperature for the samples with $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$.

3.1 Al gated n-MOS Capacitors

Figure 3.12 shows the JV characteristics of the samples with $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ annealed in (a) O_2 or (b) N_2 .

Since a thickness of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film was so thin, the leakage current density was totally large.

In the case of O_2 PDA, there were hardly any differences in leakage current density between as-deposited, 300 °C and 400 °C. For the 600 °C sample, the leakage current was reduced significantly at the expense of EOT.

In the results of N_2 annealing, the leakage current density was large for low temperature annealed (300 °C or 400 °C) samples because the growth of the interfacial layer was suppressed in addition to thin thickness of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ dielectric. The leakage current density was reduced to approximately $10^{-4}(\text{A}/\text{cm}^2)$ by 600 °C anneal.

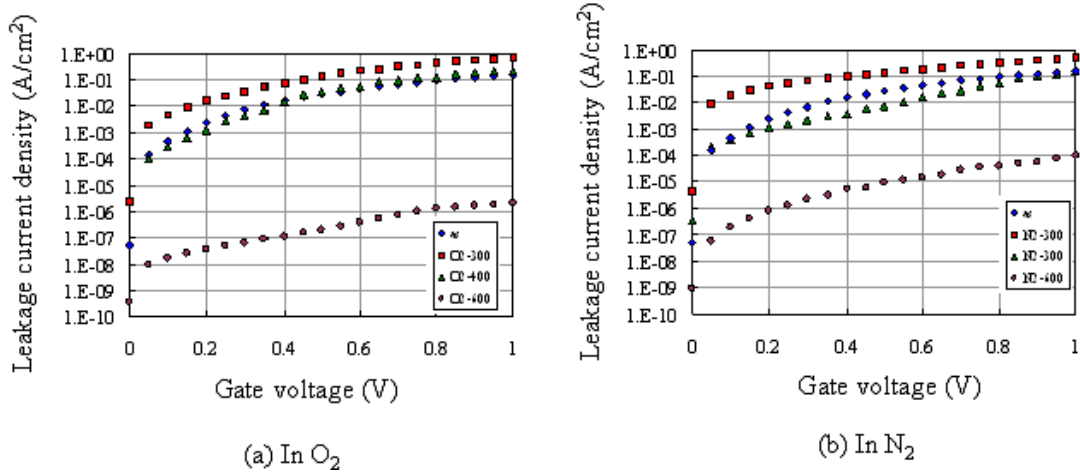


Figure 3.12: The J-V characteristics of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film.

3.1.5 The Comparison Between Three Dielectrics

Al gated n-MOS capacitors with each dielectric films, La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ will be discussed with an emphasis on their comparison. To minimize the EOT, thin films were deposited as far as possible: If a dielectric thickness was too thin, the appropriate evaluation could not be done due to a significant gate leakage.

Heat treatments were performed in only N_2 ambient because the growth of the interfacial layer clearly proceeds with O_2 annealing. High temperature heat treatments up to $1000\text{ }^\circ\text{C}$ were attempted to investigate the heat-stability. Treatment time for high temperature annealing was shortened because it was obvious that the growth of the interfacial layer was proceeded if the higher annealing temperature it became.

Figure 3.13, 3.14 and 3.15 show the CV characteristics of La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ samples respectively, measured at 100 kHz compared between annealing temperatures.

Annealing temperatures of $300\text{ }^\circ\text{C}$, $600\text{ }^\circ\text{C}$ for 5 minutes, $800\text{ }^\circ\text{C}$ 1 minute, $900\text{ }^\circ\text{C}$ 30 seconds and $1000\text{ }^\circ\text{C}$ spike were attempted for La_2O_3 samples and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack samples. $300\text{ }^\circ\text{C}$, $600\text{ }^\circ\text{C}$ for 5 minutes, $900\text{ }^\circ\text{C}$ 30 seconds and $1000\text{ }^\circ\text{C}$ spike were attempted for Y_2O_3 .

The small bumps in the CV curve which might be caused by interface states around inversion region were observed for the La_2O_3 samples. In the CV curve of the Y_2O_3 samples, they were suppressed completely. For $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ samples, although they were not quite eliminated due to thinner thickness, the CV characteristics were close to Y_2O_3 .

The accumulation capacitance of the samples with La_2O_3 and Y_2O_3 films annealed at high temperature $900\text{ }^\circ\text{C}$ and $1000\text{ }^\circ\text{C}$ was at between that of $300\text{ }^\circ\text{C}$ and $600\text{ }^\circ\text{C}$. However, capacitance of $900\text{ }^\circ\text{C}$ sample was the highest for the $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ sample while $300\text{ }^\circ\text{C}$ sample has the highest capacitance for other

3.1 Al gated n-MOS Capacitors

samples. Presumed cause for that is that the growth of the interfacial layer was suppressed or it was consumed by Y_2O_3 buffer layer with high temperature and short time heat treatment.

The differences in the La_2O_3/Si and Y_2O_3/Si interface could be observed in the slope of CV curve from inversion region to accumulation region. If the shallower curve it is, the interface trap density is large. The slope of CV curve for Y_2O_3 and La_2O_3/Y_2O_3 samples were steeper than that of La_2O_3 , indicating that the La_2O_3/Si interface has much interface states.

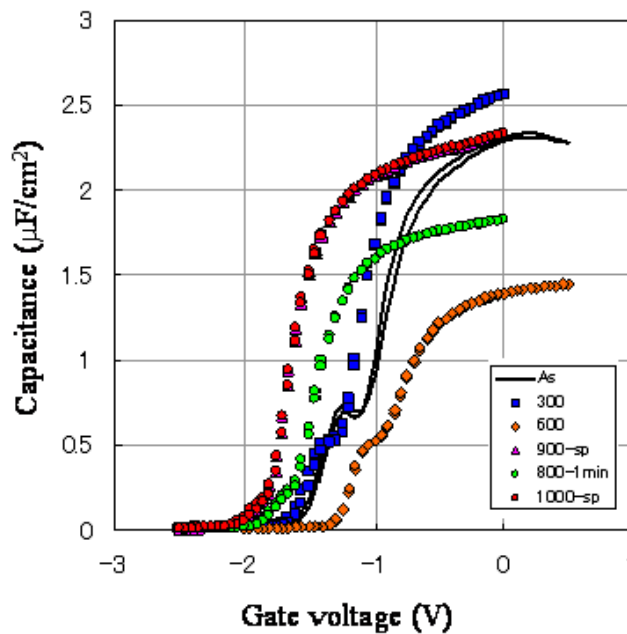


Figure 3.13: CV characteristics of La_2O_3 monolayer measured at 100 kHz.

3.1 Al gated n-MOS Capacitors

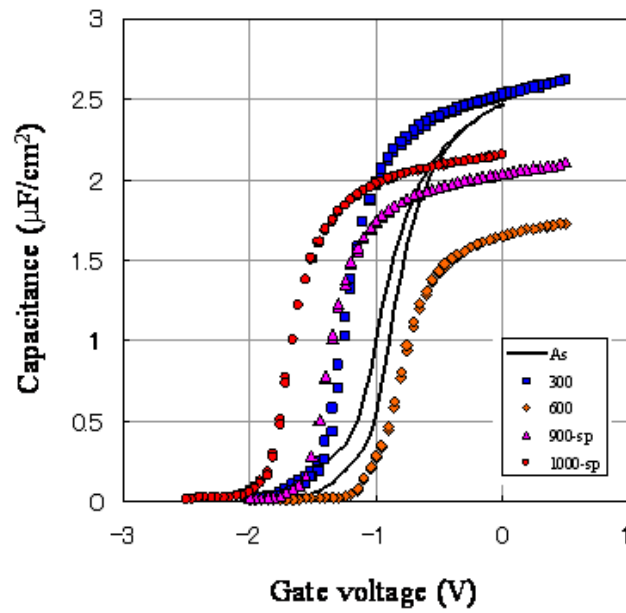


Figure 3.14: CV characteristics of Y_2O_3 monolayer measured at 100 kHz.

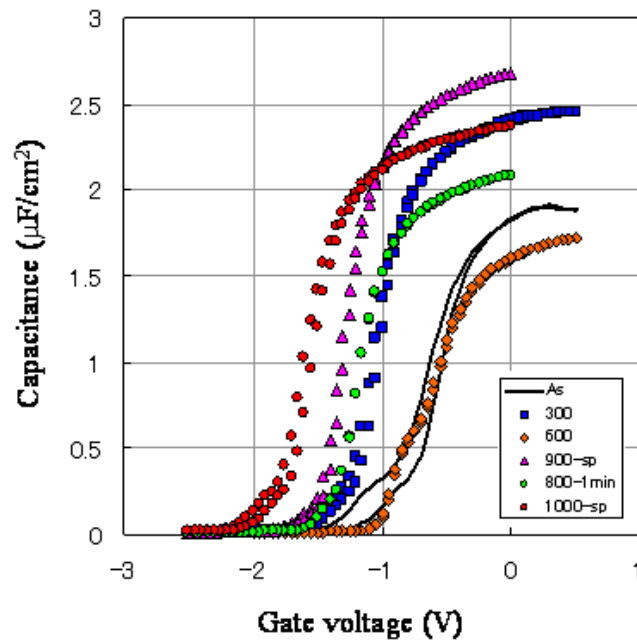


Figure 3.15: CV characteristics of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack measured at 100 kHz.

In the figure 3.13 - 3.15, large flatband voltage shift was observed for all the samples annealed at high temperature 800 °C to 1000 °C. Figure 3.16 shows the flatband voltage of each samples as a function of annealing conditions. The flatband voltage shift was the smallest as annealed at 600 °C for all the samples. However, it was enlarged as the samples were annealed at high temperature. The conceivable cause is the short-time annealing because the flatband voltage became smaller with increase of annealing temperature with the same PDA times of 5 minutes while flatband voltage for the samples with 300 °C PDA were shifted on a large scale in spite of the same annealing time. Hence, the shorter annealing time and the lower annealing temperature become, the larger the flatband voltage shift becomes.

Comparing between La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ samples, the largest flatband voltage shift was observed for the La_2O_3 samples especially in the case of high temperature annealing, indicating the oxygen deficiency in La_2O_3 film. Thus, the positive charge in La_2O_3 film or at the interface might induce larger flatband voltage shift. For Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack samples, the flatband voltages denote the same tendency with each other. Since Y_2O_3 has stronger affinity for oxygen than La_2O_3 , the oxygen deficiency was limited by using Y_2O_3 buffer layer.

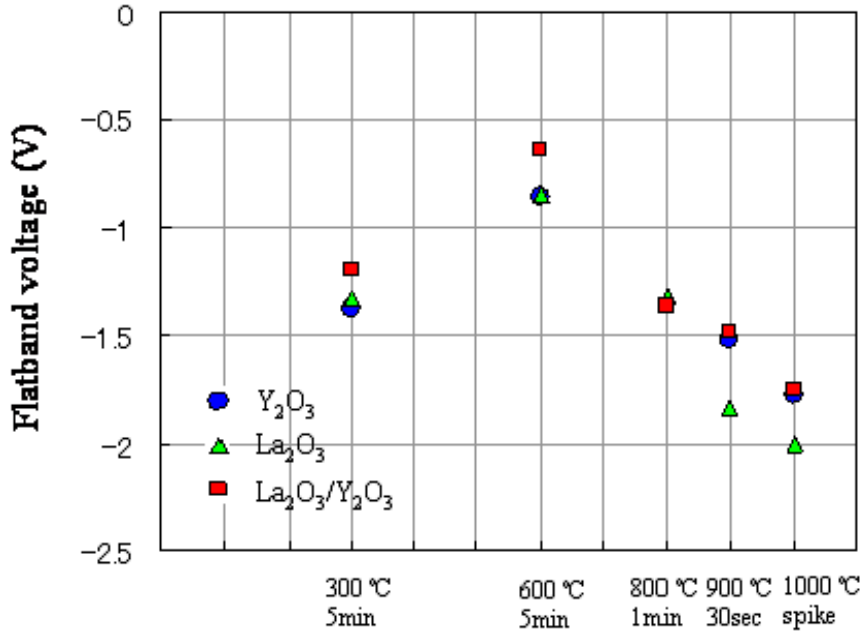


Figure 3.16: The comparison of flatband voltage between three samples.

Figure 3.17 shows the gate leakage current density at 1 V for each dielectrics as a function of EOT calculated from CV characteristics compared between La₂O₃, Y₂O₃ and La₂O₃/Y₂O₃ samples. The plots were fitted by exponential approximated line.

Comparing La₂O₃ and Y₂O₃ dielectric film, obvious difference in the leakage current density was observed. The leakage currents for La₂O₃ samples were relative large even with large EOT values. A large charge trap density at the interface or in the oxide might contribute to the increase of gate leakage current.

For the samples with Y₂O₃ film, the leakage current density was reduced dramatically compared with La₂O₃ film. In the case of Y₂O₃ dielectric, the charge trap density would not increase with increase of annealing temperature. In fact,

3.1 Al gated n-MOS Capacitors

the significant reduction of leakage current for Y_2O_3 has been reported [15].

The effect of Y_2O_3 buffer layer was confirmed in the result of La_2O_3/Y_2O_3 stack. The relation of leakage current to EOT was the same tendency of that of Y_2O_3 . The reduction of leakage current is very essential as reducing the thickness of a dielectric to reduce the EOT because the device would not operate due to a large amount of gate leakage current. The reduction of leakage current without increasing EOT indicates the possibility for more reduction of EOT with reducing a physical thickness of dielectric film.

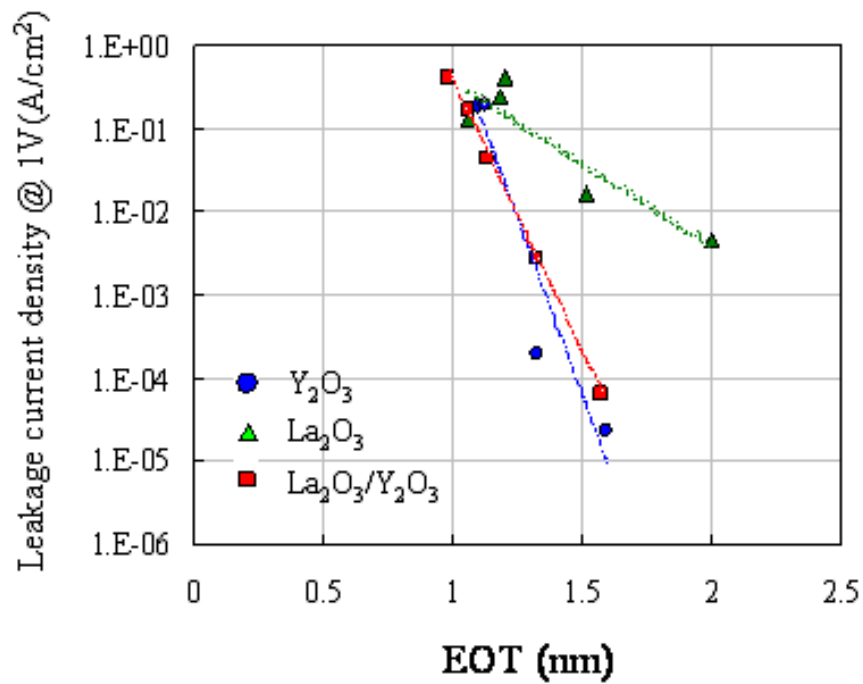


Figure 3.17: The relationship of the gate leakage current density at 1V to EOT.

3.2 Pt gated n-MOS Capacitors

As discussed the EOT and dielectric constant ϵ in comparison between La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ dielectrics, it is inadequate to use Al as a gate electrode because the interfacial layer grows between dielectric and gate electrode. Since the interfacial layer is expected to be the alumina (Al_2O_3) which has lower dielectric constant than La_2O_3 and Y_2O_3 , the accurate evaluations of dielectric constant are impossible.

Pt was used for gate electrodes to solve this problem. Pt has a property not to produce the interfacial layer at the interface between dielectric film and gate electrode. The accurate evaluations for each dielectrics were performed by Pt gated n-MOS capacitors.

After dielectric deposition, samples were annealed in N_2 at 300 °C, 600 °C, 800 °C and 1000 °C for 5 minute. Annealings up to high temperature with the same annealing time were performed. In addition, 1000 °C for 1 minutes and spike were performed as the high-temperature with short-time annealing.

Figure 3.18 - 3.20 show the CV curve measured at 100 kHz with Pt gate electrodes on La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ dielectric films.

In the case that the Pt was used as gate electrodes, a hysteresis were observed, especially in the lower the annealing temperature and the shorter annealing time cases. Fixed charge in the oxide might contribute to the hysteresis and it was prone to be visible as the Pt gate was used.

For La_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack samples, accumulation capacitance increased compared with Al gate. This indicates that the interfacial reaction between La_2O_3 and gate electrode was suppressed. For Y_2O_3 samples, however, capacitance did not increase even with the same physical thickness. As far as Y_2O_3 concerned, it would not react with gate electrode even though Al was used. This is well explained from strong affinity for oxygen Y_2O_3 has.

3.2 Pt gated n-MOS Capacitors

Although 1000 °C spike annealing yields an increase of capacitance, flatband voltage was shifted to negative voltage side. In the CV curve of 1000 °C 5 min, 1 min and spike, the shorter annealing time became, flatband voltage was shifted to negative side. And capacitance of La_2O_3 samples decreased with increase of annealing temperature. Detail discussions about EOT will be continued.

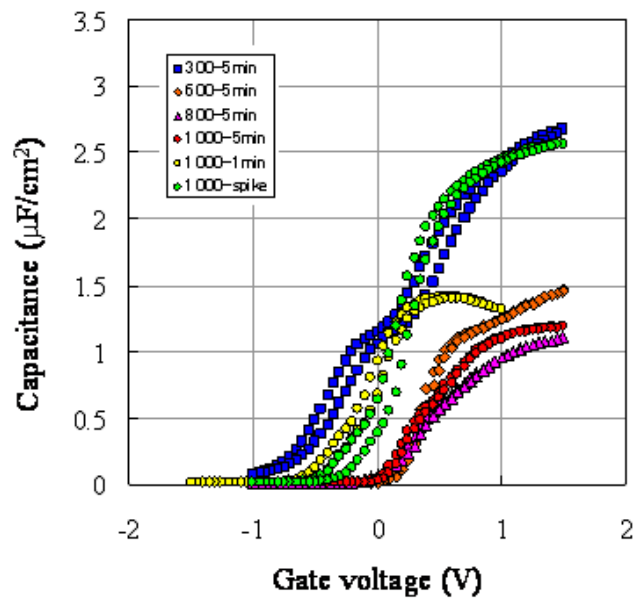


Figure 3.18: CV with Pt gate for La_2O_3 samples measured at 100 kHz.

3.2 Pt gated n-MOS Capacitors

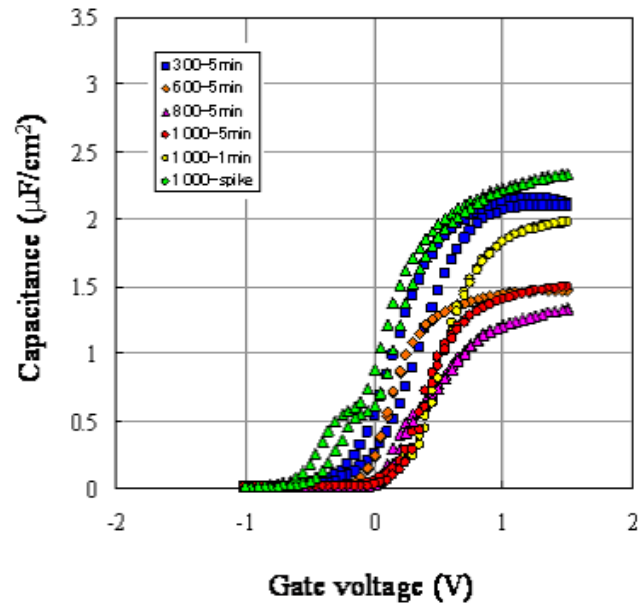


Figure 3.19: CV with Pt gate for Y_2O_3 samples measured at 100 kHz.

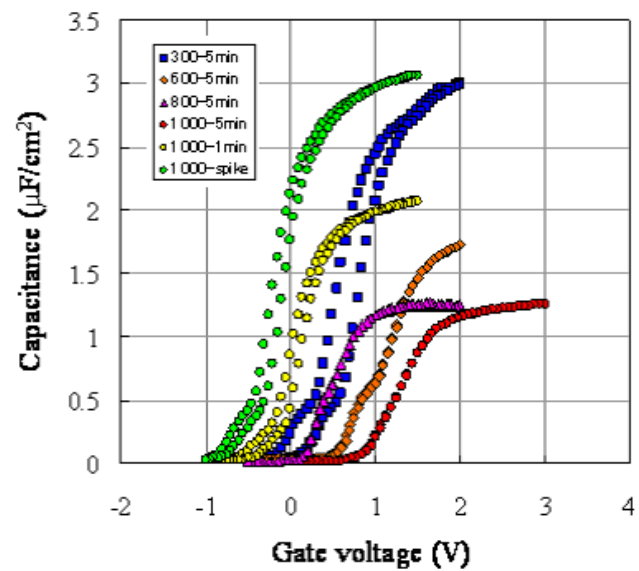


Figure 3.20: CV with Pt gate for La_2O_3/Y_2O_3 samples measured at 100 kHz.

Figure 3.21(a) shows the relation of EOT to physical thickness. The annealing conditions for each samples were 300 °C 5 min., 600 °C 5 min., 800 °C 5 min., 1000 °C 5 min., 1000 °C 1 min. and 1000 °C spike. For Y₂O₃ monolayer samples, approximated line positioned on the upper side, indicating that Y₂O₃ has lower dielectric constant than that of La₂O₃ and La₂O₃/Y₂O₃ stack. Comparing La₂O₃ monolayer and La₂O₃/Y₂O₃ stack, the approximated line for La₂O₃/Y₂O₃ samples is positioned upper side than La₂O₃ samples and a slope of the line for stack samples is steeper. Therefore, the thicker T_{phy} became, the more increase of EOT was limited for La₂O₃/Y₂O₃ stack samples.

For understandability, only of (b) 5 minutes annealing time and (c) 1000 °C annealed samples were extracted from figure 3.21(a). In the case that the samples were annealed for 5 minutes, both T_{phy} and EOT increased with increase of annealing temperature for each dielectrics. However, the slopes of approximated line were different. The slopes of a line for Y₂O₃ monolayer and La₂O₃/Y₂O₃ roughly conformed. For La₂O₃ samples, a slope became steeper, indicating the growth of the interfacial layer with increase of annealing temperature. If the annealing time was the same, the distinctive difference between the La₂O₃/Si and the Y₂O₃/Si interface was observed.

The results of constant annealing temperature of 1000 °C with varying the annealing time are shown in figure 3.21(b). Also the difference in a slope between La₂O₃/Si and Y₂O₃/Si interface was observed. A line for La₂O₃ monolayer samples shifted upward. The reason for that is expected to be the high temperature annealing. In the case of high temperature annealing, La₂O₃/Si interface readily forms the interface layer resulting in an increase of EOT.

La₂O₃/Y₂O₃ thick film of approximately 7.6 nm was deposited to examine the dependence on film thickness. The results of these samples were added to figure 3.21(a) as shown in (d). Although the data dispersions were observed, a slope of

3.2 *Pt gated n-MOS Capacitors*

approximated line was almost the same as the $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ thin film and the line positioned on the lower side. In the case of thick film, the silicate of the upper part of film is expected to be limited i.e. silicon penetrations into La_2O_3 film were suppressed by making the film thicker. Hence, permittivity of dielectric film was higher compared with thin film.

3.2 Pt gated n-MOS Capacitors

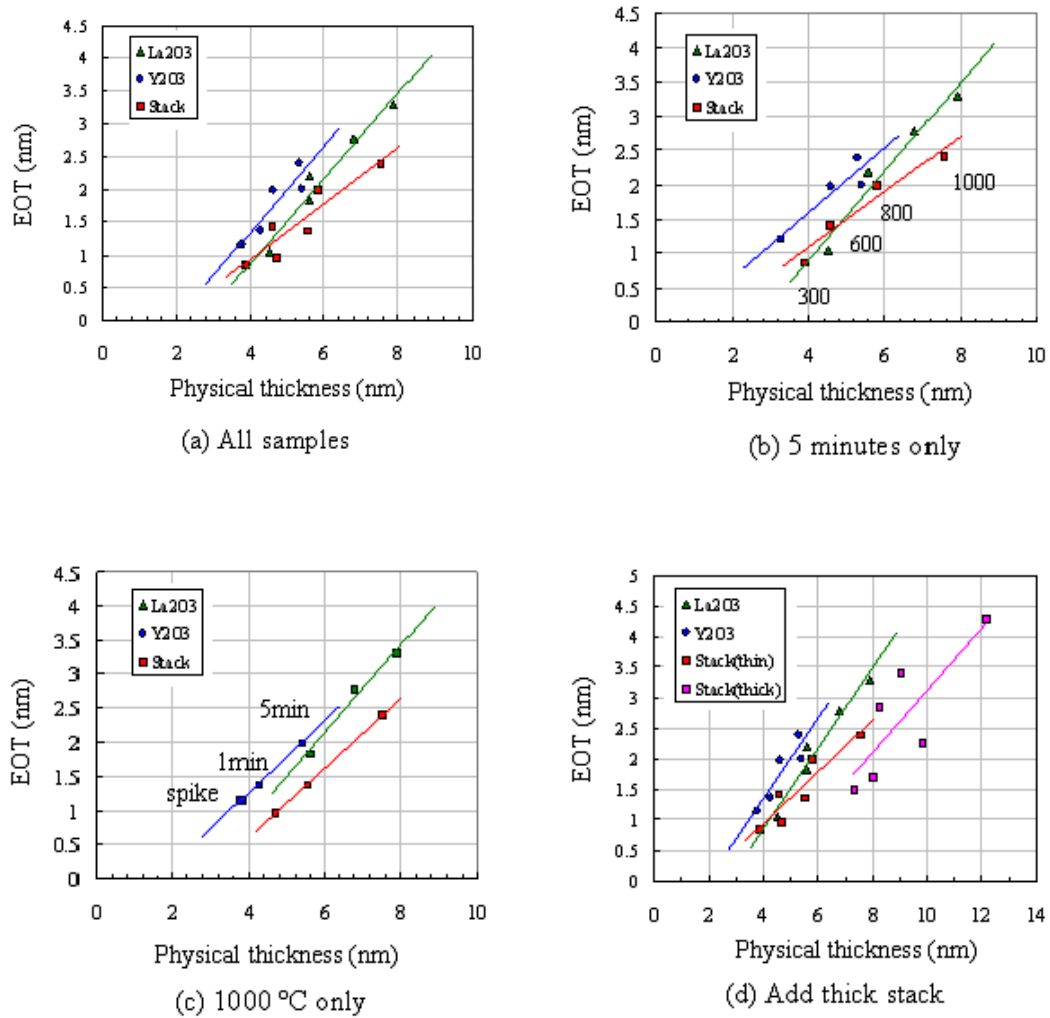


Figure 3.21: The relationships of EOT to T_{phy} . (a) All the samples, (b) Extracted 5 minutes annealing only, (c) Extracted 1000 °C annealing only and (d) Thick stack dielectric added.

3.2 Pt gated n-MOS Capacitors

Variation of dielectric constants of La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ films as a function of annealing conditions are shown in figure 3.22.

For La_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack samples annealed at 300 °C, dielectric constant were relatively high. As annealed at high temperature for 5 minutes, the dielectric constant decreased due to the growth of the interfacial layer. Especially, the decreasing amount of dielectric constant for La_2O_3 was significant. The highest dielectric constants were obtained for all the dielectrics in 1000 °C spike PDA case.

As was expected, dielectric constant of Y_2O_3 film was the lowest. However, dielectric constant of stack samples became higher than La_2O_3 monolayer by using Y_2O_3 as a buffer layer. That might be because the formation of La-silicate and the growth of the interfacial layer were suppressed.

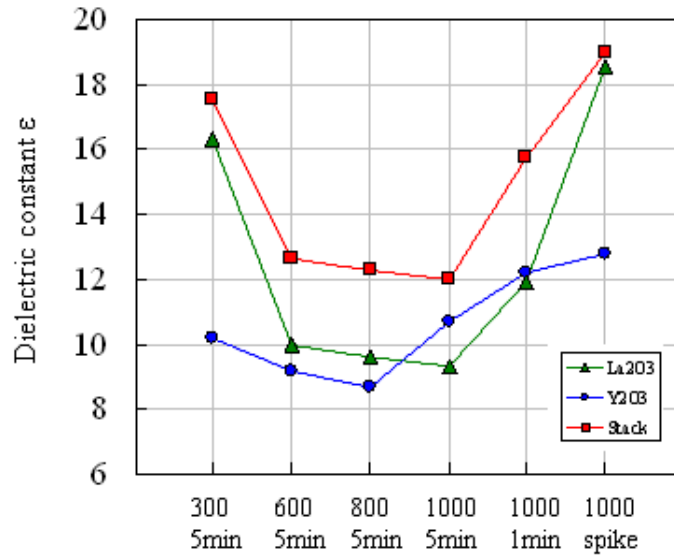


Figure 3.22: Comparison of dielectric constant between La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film.

3.2 Pt gated n-MOS Capacitors

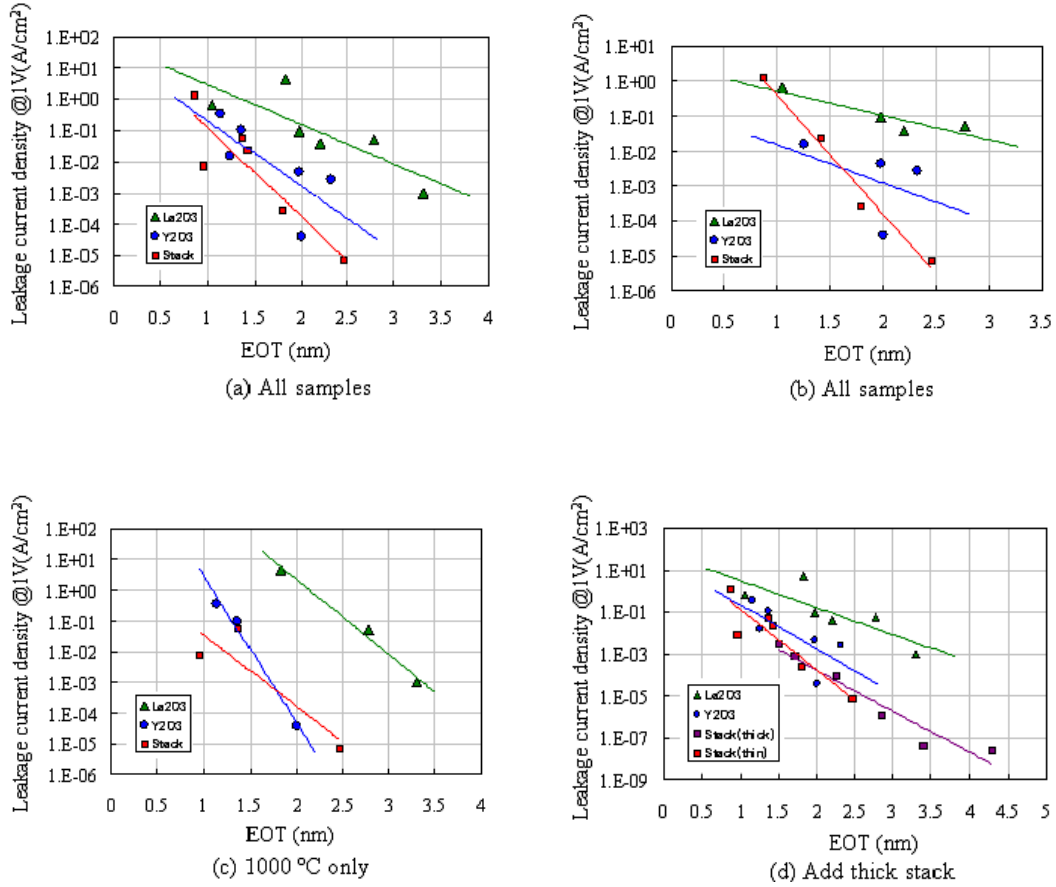


Figure 3.23: The relationships of the leakage current density at 1V to EOT for (a) All the samples, (b) Extracted only of 5 minutes annealed samples, (c) Extracted only of 1000 °C annealed samples and (d) Thick stack dielectric added.

The gate leakage current density at 1V as a function of EOT are shown in figure 3.23(a). The leakage for La₂O₃ samples was relatively large. However, for Y₂O₃ and La₂O₃/Y₂O₃ samples, the leakage current was at lower level. The Y₂O₃/Si interface might have the effects on minimizing the leakage current. Although the results are in agreement with the results of Al gated MOS-capacitors. The approximated line for Y₂O₃ positioned between La₂O₃ and stack while overlapped with the line for stack samples in Al-gated case. This difference resulted from the

interfacial reaction between La_2O_3 layer and gate electrodes.

For further consideration, only of (b) 5 minutes PDA samples and (c) 1000 °C PDA samples were extracted from figure 3.23(a). As the samples were annealed for constant time 5 minutes, the leakage current was significantly reduced by using Y_2O_3 as a buffer layer.

In the case that the samples were annealed at 1000 °C with varying the annealing time, the leakage current of La_2O_3 samples were so large. The difference between La_2O_3 and Y_2O_3 was observed notably in high temperature PDA case.

$\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ thick film of approximately 7.6 nm was deposited to examine the dependence on film thickness. The results of thick stack film were added to figure 3.23(a) and shown in figure 3.23(d). Although the slight differences were observed in EOT vs. T_{phy} , the results of thick stack samples were on a extension of the approximated line for thin stack samples. As far as the leakage current density vs. EOT plot concerned, the dependence on film thickness was not observe.

3.3 Control Experiment of Other Stack Structures

3.3.1 Introduction

$\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack structure was mainly used in this study. It is necessary to examine whether $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack is better structure or not, or to confirm the superiority of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack. In this section, the electrical characteristics of n-MOS capacitors with various structural stacks are compared.

The electric characteristics of $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3$ and $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ dielectric structures, as depicted in figure 3.24 and 3.25, were examined. The samples were annealed in N_2 ambient with various temperatures and Al gate was used.

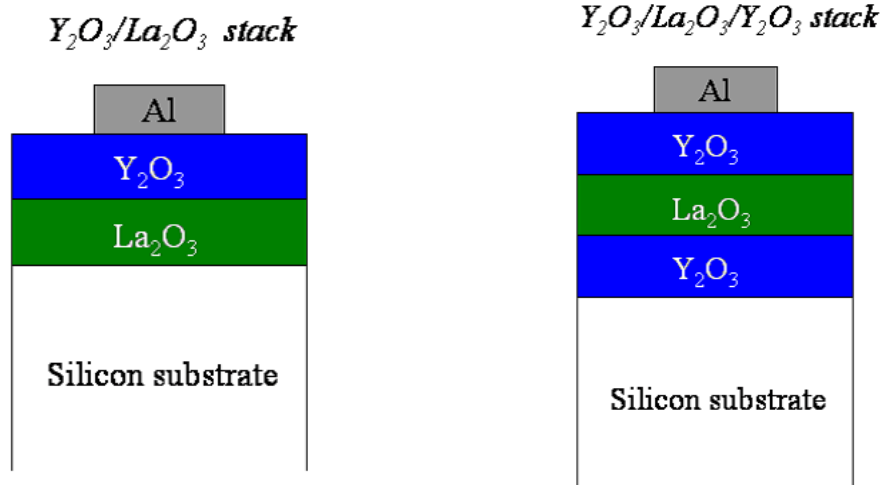


Figure 3.24: Schematic illustration of $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3$ structure. Figure 3.25: Schematic illustration of $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ structure.

3.3.2 $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3$ structure

After deposition of $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3$ film, samples were annealed in N_2 with temperatures of 300 °C, 600 °C for 5min and 800 °C for 1 min and 1000 °C spike.

Figure 3.26 shows the C-V characteristics measured at 100 kHz and compared between PDA temperatures. As was expected, the slight bump resulting from the interface traps was observed in the weak inversion region. This slight bump was also observed in La_2O_3 monolayer case, indicating that it is inherent in the $\text{La}_2\text{O}_3/\text{Si}$ interface. The capacitance for as-deposited sample was the highest denoting the same tendency of Y_2O_3 monolayer. The increase of physical thickness due to moisture absorption was suppressed covering La_2O_3 with Y_2O_3 .

Figure 3.27 shows the relationships of gate leakage current density at 1V to EOT calculated from CV. The results of La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ were inserted for comparison. It is obvious that the gate leakage current was significant large as compared to other dielectrics. The slope of a line was similar to that of La_2O_3 samples indicating the $\text{La}_2\text{O}_3/\text{Si}$ interface largely contributed to the gate leakage. In addition, the amount of gate leakage was larger than La_2O_3 sample. It is contemplated that the replaced upper half of La_2O_3 layer by Y_2O_3 (with lower dielectric constant) had the EOT increased.

The significant gate leakage current was critical issue for MOSFET. Hence, $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3$ should not be applied to gate dielectric film. Although acceptable results were not obtained, it was refound that difference in the gate leakage current between $\text{La}_2\text{O}_3/\text{Si}$ and $\text{Y}_2\text{O}_3/\text{Si}$.

3.3 Control Experiment of Other Stack Structures

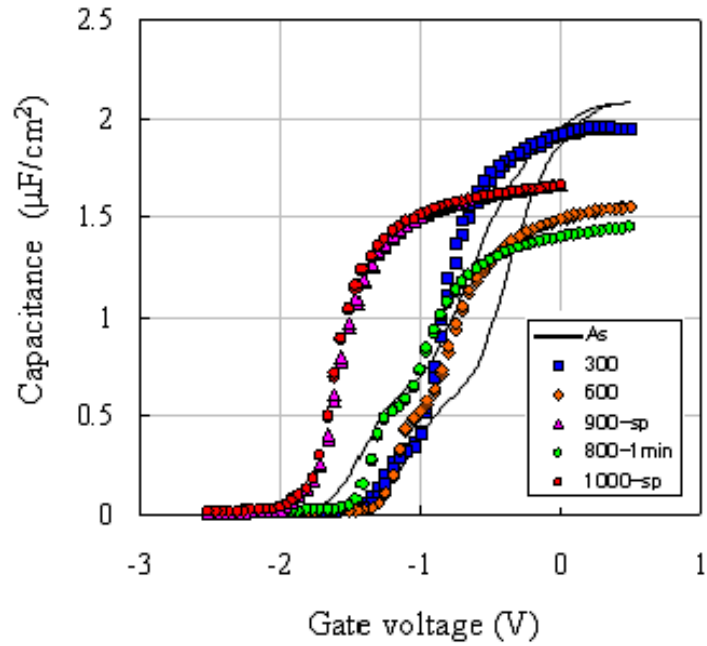


Figure 3.26: CV characteristics measured at 100 kHz for $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3$ samples.

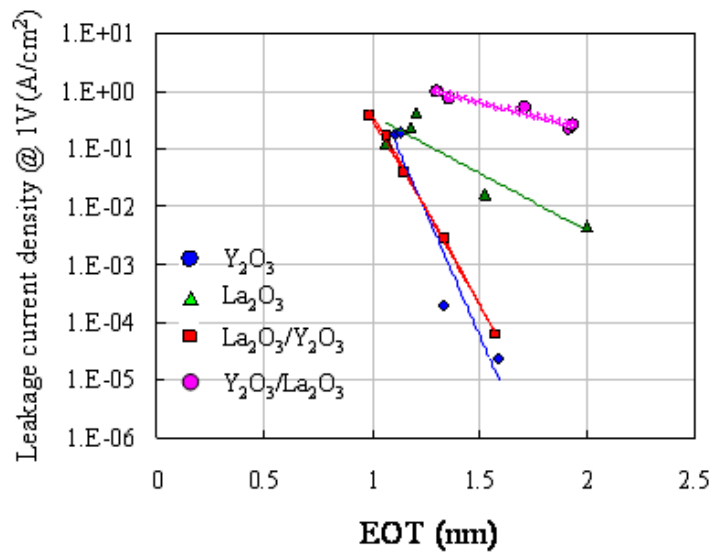


Figure 3.27: $J @ 1\text{V}$ vs. EOT for $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3$ samples compared with other dielectric structures.

3.3.3 $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ structure

After deposition of $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film, samples were annealed in N_2 with temperatures of 300 °C and 400 °C for 5 minutes.

Figure 3.28 shows the C-V characteristics measured at 100 kHz. The slight bump in the weak inversion region was not observed indicating the $\text{Y}_2\text{O}_3/\text{Si}$ interface is the effective. More noteworthy are the small flatband voltage shift compared with other dielectrics. Figure 3.29 shows the flatband voltage compared between each dielectric structures. The flatband voltage shifts of each dielectric films except for $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film were extremely large. This is because that the generation of positive fixed charges was limited by $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ structure: The contributing factors of generating positive charges, such as oxygen deficiency and water absorption, were suppressed. $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ structure is expected to be effective in improving channel mobility of MOSFET.

Figure 3.30 shows the gate leakage current density at 1V as a function of EOT calculated from CV. The results of other dielectric structures were inserted for comparison. The gate leakage current for $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film was the lowest compared to other dielectric films with the same EOT value. The $\text{Y}_2\text{O}_3/\text{Si}$ interface would contribute to the reduction of the gate leakage and the Gate/ Y_2O_3 interface be also effective in the leakage reduction.

Better results were obtained in $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ samples. However, in the case that thinner EOT is required, $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ might not be able to achieve it because the physical thickness becomes thinner, the thickness assigned to Y_2O_3 becomes quite thin. Therefore the effects of Y_2O_3 would not be exerted in the case of thin film. It is worth further consideration as for $\text{Y}_2\text{O}_3/\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$.

3.3 Control Experiment of Other Stack Structures

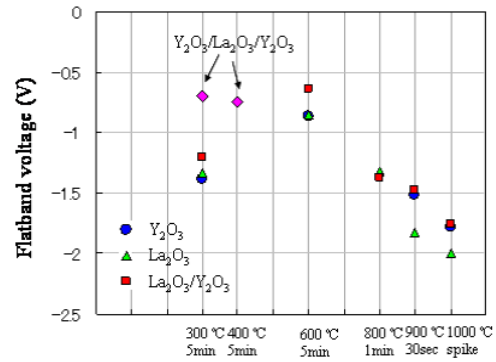
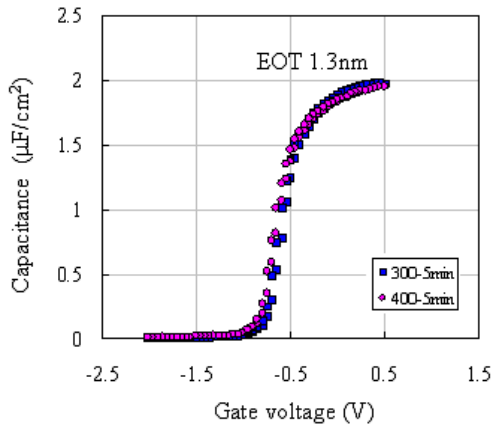


Figure 3.28: CV characteristics measured at 100 kHz for $Y_2O_3/La_2O_3/Y_2O_3$ samples. Figure 3.29: Comparison of flatband voltage between each dielectrics.

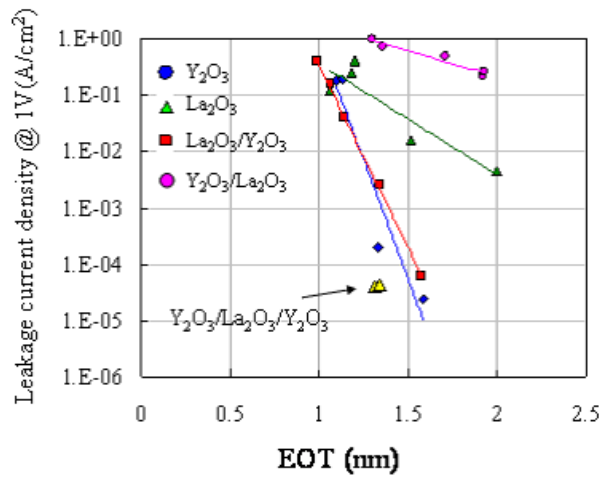


Figure 3.30: $J @ 1V$ vs. EOT for $Y_2O_3/La_2O_3/Y_2O_3$ samples compared with other dielectric structures.

3.4 PMA effect on the Al-gate/ Y_2O_3 interface

3.4.1 Introduction

One of the critical issue for MOSFET is the normally-on property resulting from the flatband voltage shift. Post Metallization Annealing (PMA) is the method to recover the flatband voltage shift. The effect of PMA on La_2O_3 film has been reported [29]. The application of PMA treatment into La_2O_3 solves the flatband voltage shift. However, the EOT increases significantly due to the growth of Al_2O_3 . Figure 3.31 shows the CV characteristics of Al-gated La_2O_3/Y_2O_3 stack film with 300 °C PMA in (a) O_2 and (b) N_2 ambient. Although the flatband voltage shift was improved, the EOT increased significantly. Furthermore, a large hysteresis was observed in O_2 PMA case and the hysteresis could not be quite suppressed either in N_2 PMA case.

In this section, the effect of PMA on Al-gate/ Y_2O_3 interface will be discussed.

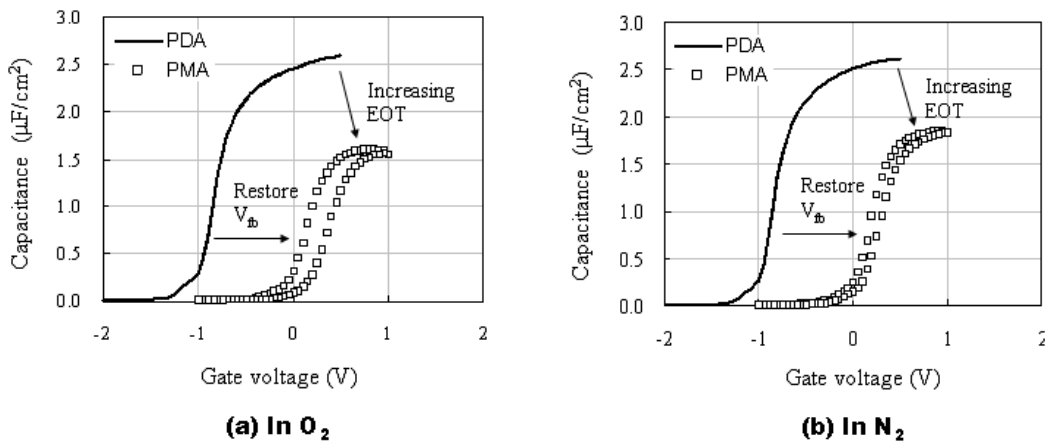


Figure 3.31: CV characteristics of La_2O_3/Y_2O_3 stack with 300 °C PMA. (a) PMA in O_2 (b) PMA in N_2 .

3.4.2 Results and Discussion

Figure 3.32 shows the CV characteristics of Al/Y₂O₃/Si with 300 °C PMA (also PDA and PDA+PMA for comparison) in (a) O₂ and (b) N₂ ambient. EOT of O₂ PDA sample was 1.76 nm. However, capacitance value increased incredibly for the PMA sample. This is the exact opposite of La₂O₃ film. In the case that both PDA and PMA treatments were applied to the sample, capacitance showed the lowest. The growth of Y₂O₃/Si interfacial layer by two times heat-treatment had an influence on increasing EOT in PDA+PMA case. The slight decrease of EOT compared to PDA sample was observed in N₂ PMA case. Although N₂ PMA case is understandable as the suppression of Al/Y₂O₃ interfacial layer, it is incomprehensible that the extreme reduction in EOT was observed only in O₂ case. The interfacial layer with higher dielectric constant, such as YAl_xO_y, might grow as annealed in O₂ ambient. The large hysteresis of PMA samples resulting from the charges in oxides was not suppressed. The large hysteresis would degrade channel mobility.

In addition, PMA treatment was applied to Al/Y₂O₃/La₂O₃/Y₂O₃ stack samples. PMA temperature was 300 °C and ambience was N₂. EOT was 1.32 nm for 300 °C PDA and 1.26 nm for 300 °C PMA. It is obvious that Y₂O₃ limited the growth of the interfacial layer between dielectric and gate electrode.

As Al was evaporated, Al with a heat would produce Al₂O₃ between Gate and La₂O₃. This is because that the electrical property of Y₂O₃ capacitor with Al gate was more excellent than with Pt gate. The suppression of Gate/Y₂O₃ interfacial layer would be associated with the limitation of Y₂O₃/Si interfacial layer.

3.4 PMA effect on the Al-gate/ Y_2O_3 interface

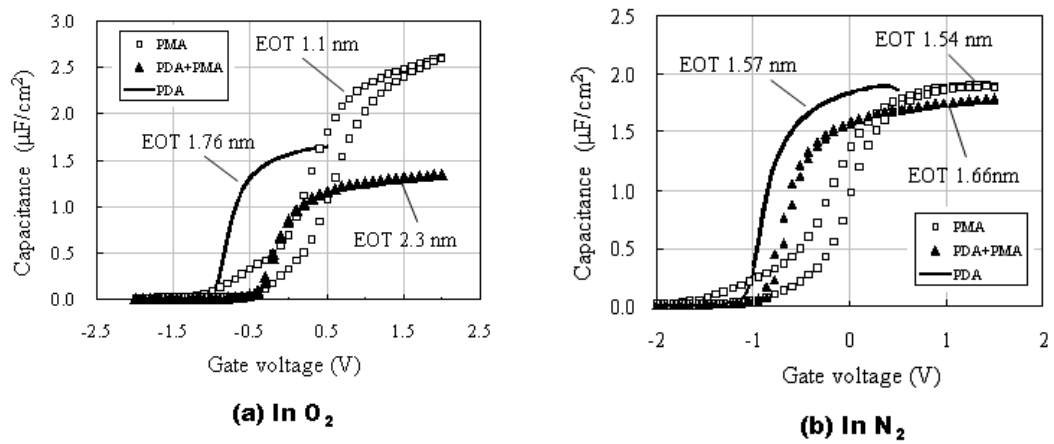


Figure 3.32: CV characteristics of Y_2O_3 with 300 °C PMA. (a) PMA in O_2 (b) PMA in N_2 .

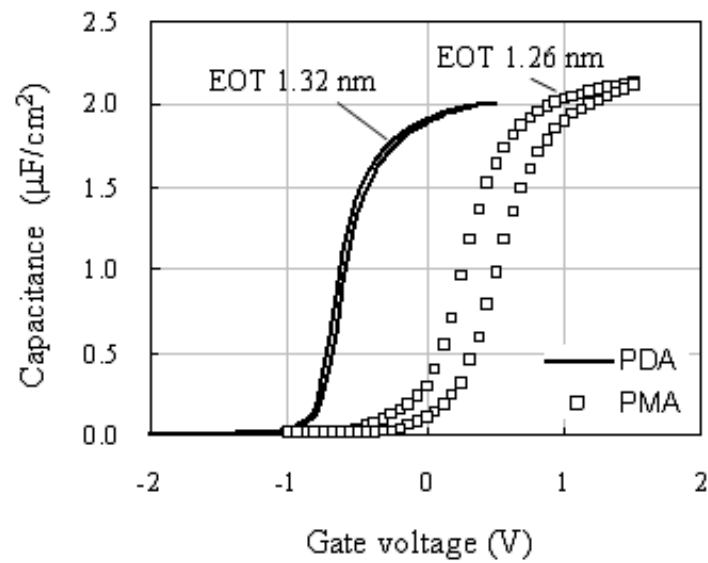


Figure 3.33: CV characteristics of $Y_2O_3/La_2O_3/Y_2O_3$ samples with 300 °C PMA in N_2 .

3.5 Optimum Conditions for Dielectric Deposition

3.5.1 Introduction

The stack structure of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ would allow us to devise the deposition condition of dielectric film for EOT reduction. Dielectric films were deposited mainly at substrates temperature of 250 °C through the study. In this section, two deposition processes will be discussed, besides 250 °C deposition. One is Y_2O_3 deposition at 250 °C and then La_2O_3 deposition at Room Temperature (RT). The other is that Y_2O_3 is deposited at 250 °C and then in-situ vacuum annealing (IVA) at 400 °C for 90 minutes prior to RT deposition of La_2O_3 . In addition, some of the samples were ex-situ annealed in N_2 . Pt was used as a gate electrodes. These deposition processes were depicted in figure 3.34 and 3.35.

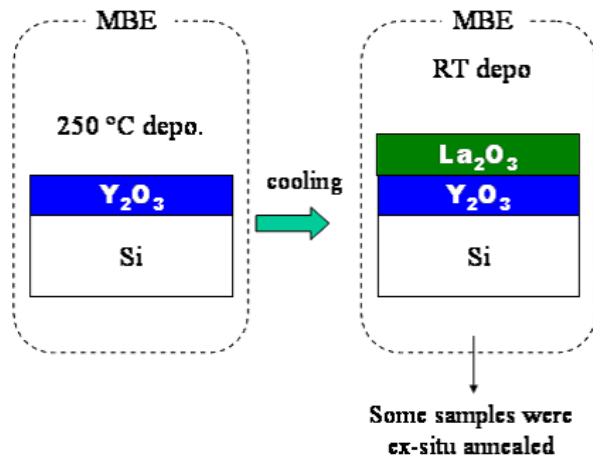


Figure 3.34: Deposition process flow for 250 °C deposition of Y_2O_3 and RT deposition of La_2O_3 .

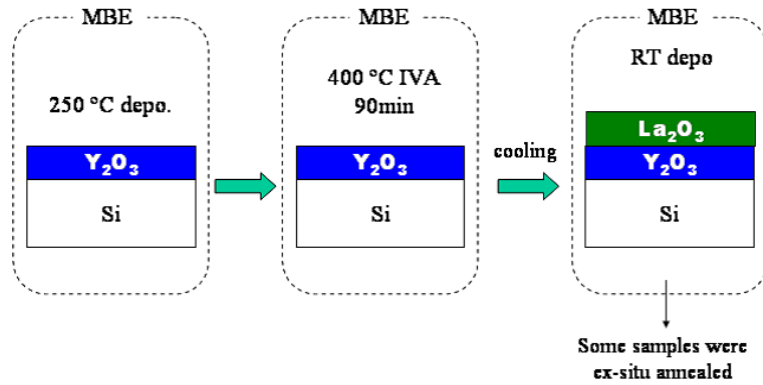


Figure 3.35: Deposition process flow. 250 °C deposition of Y_2O_3 , in-situ vacuum anneal for Y_2O_3 film and then RT deposition of La_2O_3 .

3.5.2 Results and Discussion

Figure 3.36 shows the CV characteristics measured at 100kHz for stack film of 250 °C depo. Y_2O_3 and RT depo. La_2O_3 compared between various annealing temperatures. The samples were annealed in N_2 at 300 °C, 400 °C, 600 °C for 5 minutes and 800 °C, 1000 °C for 30 seconds.

Although hysteresis was observed in 300 °C sample, the lowest EOT of 0.9 nm was obtained. 400 °C sample exhibited no hysteresis and the second lowest EOT value. In the case of high temperature annealing of 800 °C and 1000 °C for 30 seconds, flatband voltage shift was not as large as spike annealing. The 30 seconds treatments are expected to be enough long to remove defects in the oxides. The short time annealing might contribute to a large flatband shift voltage. La_2O_3/Y_2O_3 was found to be thermally stable. Although 600 °C PDA for 5 minutes showed the largest EOT value, increasing fraction of EOT was minimized compared to 250 °C depo stack film.

3.5 Optimum Conditions for Dielectric Deposition

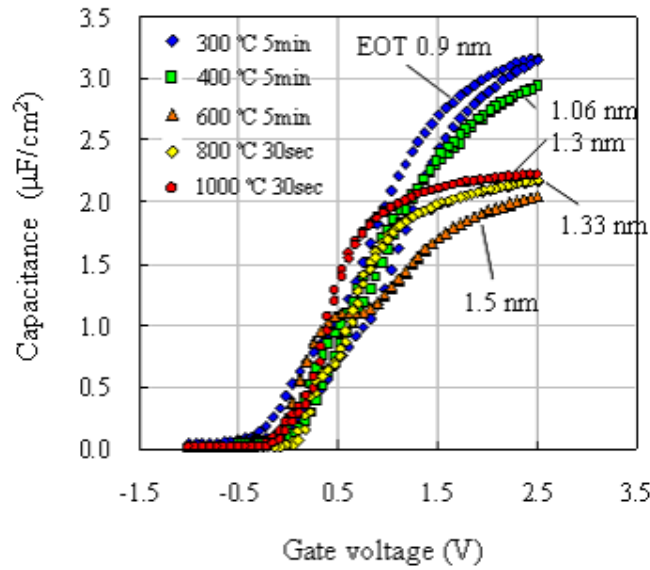


Figure 3.36: CVs at 100kHz for 250 °C depo. Y_2O_3 and RT depo. La_2O_3 stack film.

Figure 3.37 shows the CV characteristics with measurement frequencies of 1 MHz, 100 kHz and 10 kHz for the stack film of 250 °C depo. Y_2O_3 annealed in-situ at 400 °C for 90 min and RT depo. La_2O_3 . There were no frequency dispersions. However, the large bump in weak inversion region was observed indicating the increase of the interface-states. The lower measurement frequency became, the bump became larger. IVA tends to proceed oxygen deficiency and Y_2O_3 could not prevent it.

In sequence, some of the samples were ex-situ annealed in N_2 at 300 °C, 400 °C and 600 °C for 5 minutes and their CV characteristics at 100 kHz are shown in figure 3.38. The impact of interface states observed as a bump was eliminated by ex-situ RTA without increasing EOT value.

3.5 Optimum Conditions for Dielectric Deposition

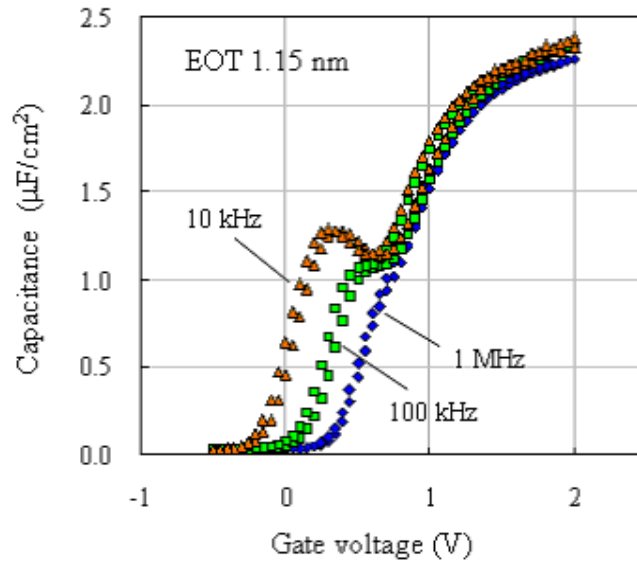


Figure 3.37: CVs with 1MHz, 100 kHz and 10 kHz for stack film with 250 °C depo. Y_2O_3 annealed in-situ at 400 °C for 90 min and RT depo. La_2O_3 .

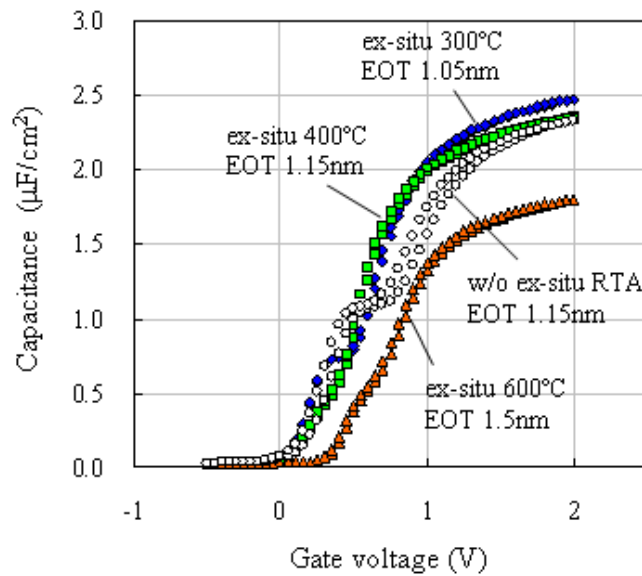


Figure 3.38: CVs at 100 kHz for stack film with 250 °C depo. Y_2O_3 annealed in-situ at 400 °C for 90 min and RT depo. La_2O_3 .

3.5 Optimum Conditions for Dielectric Deposition

Figure 3.39 exhibits EOT versus physical thickness compared to 250 °C depo. $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack film.

Stack film of 250 °C depo. Y_2O_3 and RT depo. La_2O_3 is defined as the "250+RT" and of in-situ vacuum annealed 250 °C depo. Y_2O_3 and RT depo. La_2O_3 is as the "IVA+RT" afterward.

For 250+RT samples, EOTs tend to be slightly larger than those of 250 °C depo. stack. For IVA+RT samples, tendencies of EOT vs. T_{phy} were similar to 250 °C depo. stack. As far as the reduction of EOT, 250 °C depo. stack film seems to be better.

Figure 3.40 shows the relationships of the gate leakage current density at 1 V to EOT compared to 250 °C depo. stack film. The IVA+RT samples showed similar property to 250 °C depo. stack in the lower EOT region and the gate leakage was reduced with decreasing EOT in the larger EOT region; the gate leakage of IVA+RT samples with high temperature PDA was lower. The 250+RT samples showed the significant reduction of the gate leakage currents especially in high temperature region. The formation of La-silicate might be suppressed in 250+RT stack case. The reduction of charges in the oxides contributed to the lowering of gate leakage currents. 250+RT stack must be useful for thin physical thickness of stack dielectric.

3.5 Optimum Conditions for Dielectric Deposition

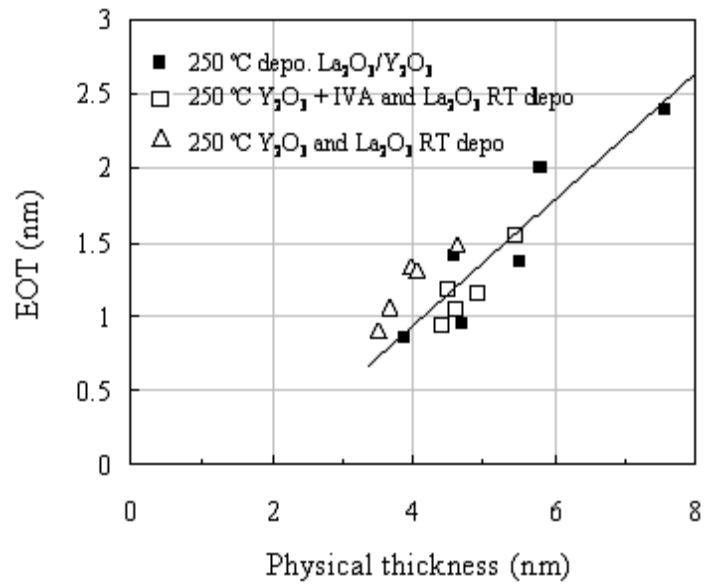


Figure 3.39: The relationships of EOT to T_{phy} compared with 250 °C depo. stack film.

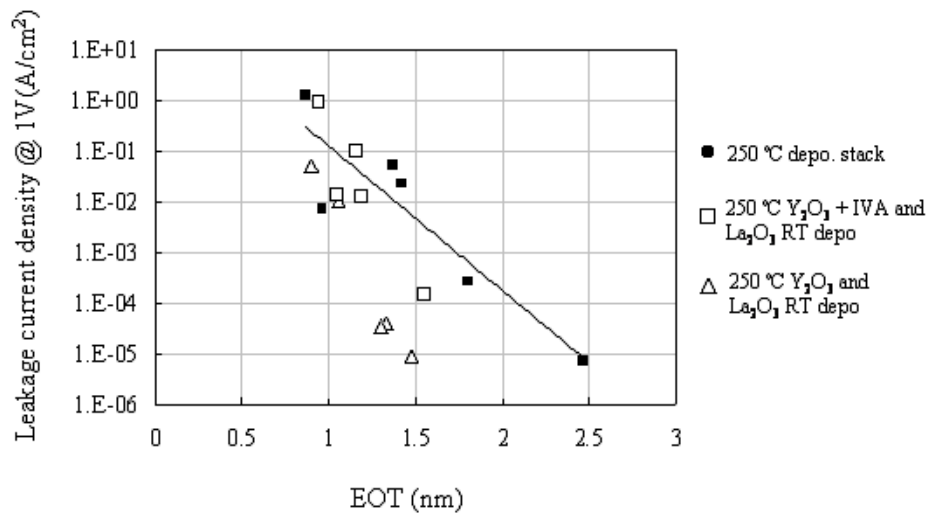


Figure 3.40: J vs. EOT plots compared with 250 °C depo. stack film.

3.6 Conclusion

Al- and Pt-gated n-MOS capacitors with La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ dielectrics were fabricated and the electrical characteristics of CV and JV were evaluated.

For La_2O_3 film, a dielectric constant was high as annealed at low temperature. However, the EOT increased substantially as annealed at high temperature.

Although a dielectric constant of Y_2O_3 was lower than La_2O_3 film, Y_2O_3 capacitors showed outstanding reduction of gate leakage currents especially as treated at high temperature and elimination of a bump in CV curve attributed to the reduction of interface-states density.

The electrical properties of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ capacitors showed an effect of Y_2O_3 buffer layer. The gate leakage was reduced without increasing EOT. A dielectric constant of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film was totally higher than La_2O_3 film and the EOT values of stack film with high temperature annealing was much more smaller. It was found that Y_2O_3 buffer layer is useful for high temperature processed La_2O_3 devices in terms of the reduction of EOT and the gate leakage currents.

Chapter 4

STRUCTURAL ANALYSES

4.1 Morphological Analyses

4.1.1 Introduction

AFM method is useful for observation on dielectric film. The surface roughness and crystallization contribute to the gate leakage currents or the mobility degradation. Especially, surface roughness of thin film has a significant impact on the electric field mobility. It is important to examine the surface morphology.

La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack films were deposited on silicon at 250 °C substrate temperature and annealed in O_2 at 300 °C-600 °C. AFM images and RMS (root-mean-square surface roughness) were obtained.

4.1.2 Results and Discussion

Figure 4.1 shows the AFM images of La_2O_3 film. The scanned area of the surface was 500×500 nm. The image of as-deposited film showed acanth-like shape. It was never flat. The roughness which was observed in as-deposited stage is expected to be caused by the moisture absorption. This roughness was improved in 300 °C PDA case. However, the asperity began to appear in 400 °C and island-like shape was observed in 600 °C PDA case. High-temperature PDA tends to induce the increase of surface roughness.

Figure 4.2 shows the AFM images of Y_2O_3 film. The scanned area of the surface was 500×500 nm. For the Y_2O_3 film, the difference of physical appearance was not observed up to 500 °C PDA. For 600 °C PDA film, acanth-like shape was observed. It seems to be uneven rough and flat.

Figure 4.3 shows the AFM images of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film. The scanned area of the surface was 500×500 nm. It seems to be totally flat for all the samples except for as-deposited film. Since the La_2O_3 surface absorbs moisture in the air, the roughness increased in as-deposited case.

4.1 Morphological Analyses

Figure 4.4 shows the RMS value as a function of annealing temperature compared between La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack. RMS tendencies are quite contrast; RMS of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film increased with annealing temperature and on a decreasing trend on reaching 400 °C PDA temperature. In La_2O_3 and Y_2O_3 monolayer case, the RMS was on the increasing on reaching 400 °C PDA temperature. Since both the Y_2O_3 and La_2O_3 surface did not show especial better morphology, one would speculate $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack structure contribute to the improvement of surface roughness or Y atoms make the interatomic bond stronger.

4.1 Morphological Analyses

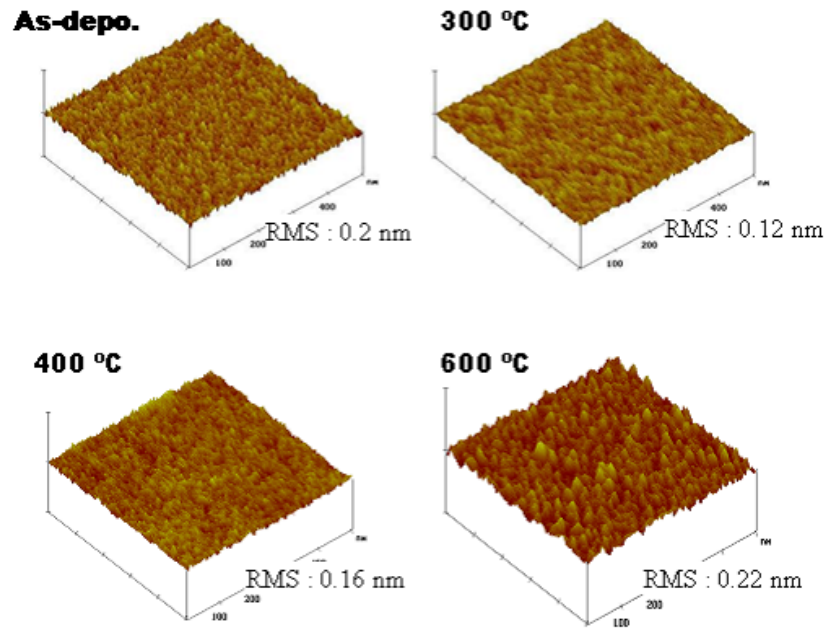


Figure 4.1: AFM images of La_2O_3 films

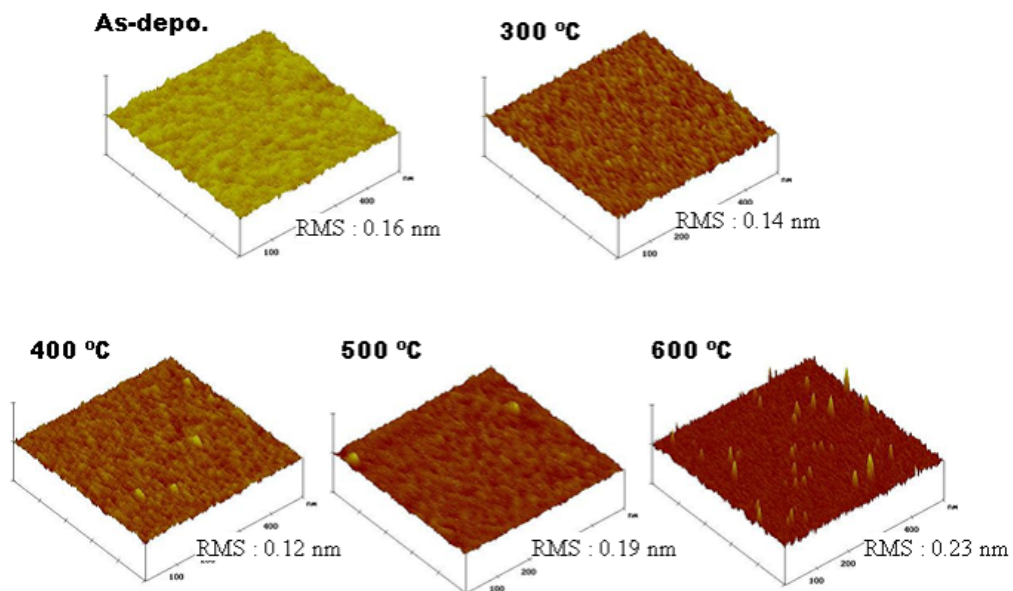


Figure 4.2: AFM images of Y_2O_3 films

4.1 Morphological Analyses

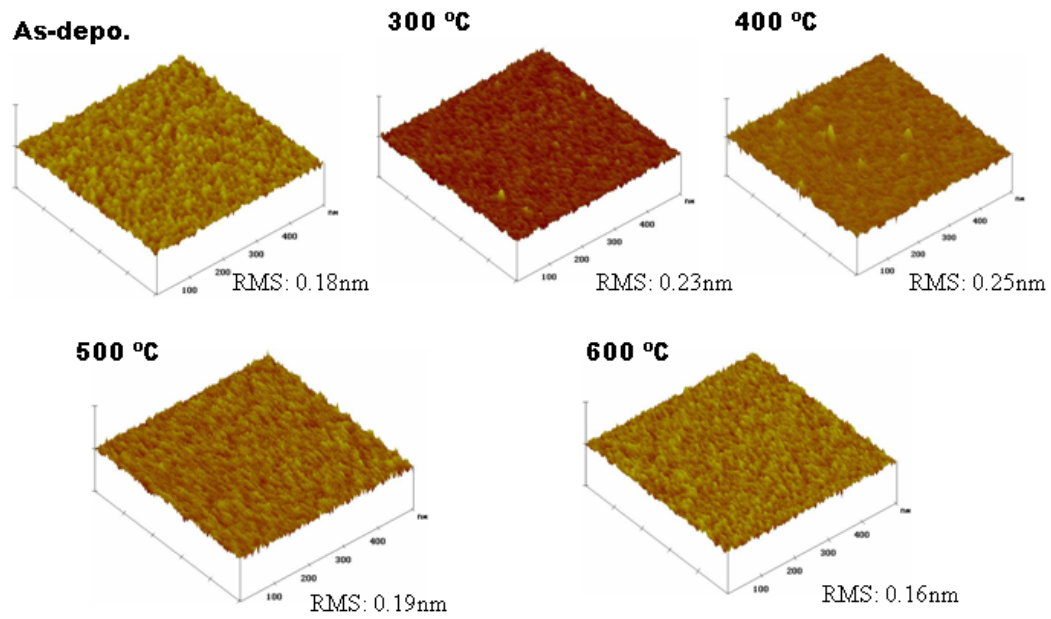


Figure 4.3: AFM images of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ films

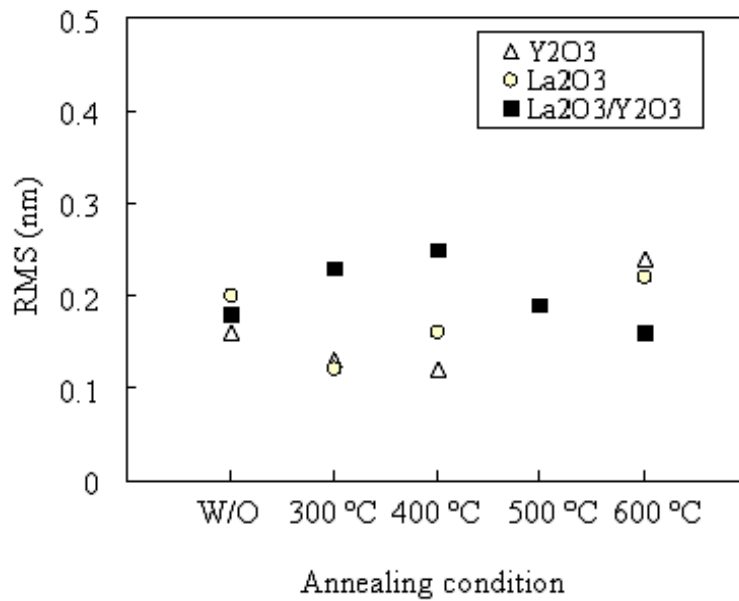


Figure 4.4: RMS value as a function of annealing temperatures compared between the films.

4.2 XPS analyses

4.2.1 Introduction

The improvement of dielectric constant by Y_2O_3 buffer layer was revealed from the viewpoint of the electrical characteristics in the previous section. One would expect the reason for improving the dielectric constant was the reduction of interfacial layer growth and limitation of La-Silicate by Y_2O_3 buffer layer. In this section, consideration of the evidence of improving permittivity from the viewpoint of structural analyses by X-ray will be made. Analyses were made by Angle-Resolved X-ray Photoelectron Spectroscopy (AR-XPS). ESCA and BL47XU in the SPring-8 facilities were used as a XPS equipment.

4.2.2 Results and Discussions

Figure 4.5, 4.6 and 4.7 show the Si-2p, La-3d and Si-2s spectra for La_2O_3 monolayer samples of (a) As-deposited and (b) 600 °C PDA in O_2 . $\text{La}_2\text{O}_3/\text{Si}$ interface was able to be probed and detected the substrate Si peak at 99.3 eV in the Si2p spectra[21]. The absence of silicide peaks is consistent with the selected oxidation conditions. The spectral region of Si2p peak also contains contributions from the La4d peaks at 101.9 eV and 105.5 eV that overlap with SiO_2 peak expected at 103.3 eV[30]. Thus, attempts to deconvolve the peak could not be made. The La3d spectra in figure 4.6 (a) and (b) exhibit a doublet resulting from the spin-orbit splitting of the $\text{La}3d_{3/2}$ and $\text{La}3d_{1/2}$ peaks. Both (a) and (b) show the significant amount of La-silicate because there is a little La_2O_3 components. Si2s spectra in figure 4.7 (b) showed high intensity of the interfacial layer which was not observed for as-deposited sample.

Figure 4.8, 4.9 and 4.10 show the Si-2p, Y-3d and Si-2s spectra for Y_2O_3 monolayer samples of (a) As-deposited and (b) 600 °C PDA in O_2 . Peak assigned

to silicon substrate is observed in both figure 4.8 (a) and (b), and strong peak at 102.7 eV for 600 °C PDA sample is consistent with Si-O bonding. The measured Si-O peak maximum is at lower binding energy than expected for SiO₂ (103.3 eV), and within the expected range (102-103 eV) for Si-O bonding in metal silicates[21]. The Y3d spectra in figure 4.9 (a) and (b) exhibit a doublet resulting from the spin-orbit splitting of the Y3d_{3/2} and Y3d_{5/2} peaks at 160.8 eV and 159.0 eV, respectively, whereas the reference peak positions for Y3d_{3/2} and Y3d_{5/2} for Y₂O₃ are 158.8 and 156.8 eV[21]. Most Y₂O₃ were silicated as well as La₂O₃ monolayer case. No peaks for Y-Si at ~0.2 and ~0.6 eV lower than the metallic yttrium and silicon peaks, respectively, are observed in the Y3d or Si2p spectra. The SiO₂ components in Si2s spectra of figure 4.10 seem not to be as much as those of La₂O₃ monolayer.

Figure 4.11, 4.12 and 4.13 show the Si-1s and La-3d spectra measured by BL47XU for La₂O₃/Y₂O₃ stack samples with (a) 300 °C and (b) 500 °C PDA in O₂. The excited photoelectrons with take off angle of 8°, 15°, 20°, 30°, 52° and 80° were detected. Since the Si2p spectra overlap with La4d spectra, Si1s spectra were detected to analysis fraction of silicate and silicon oxides. Peaks at 1838.8 eV attribute to silicon substrate and small peaks within the range from 1840 eV and 1843 eV to the interfacial layer. The La3d spectra in figure 4.12 showed that the peak position was at close to the La₂O₃ peak compared with figure 4.6, indicating the suppression of La-silicate.

4.2 XPS analyses

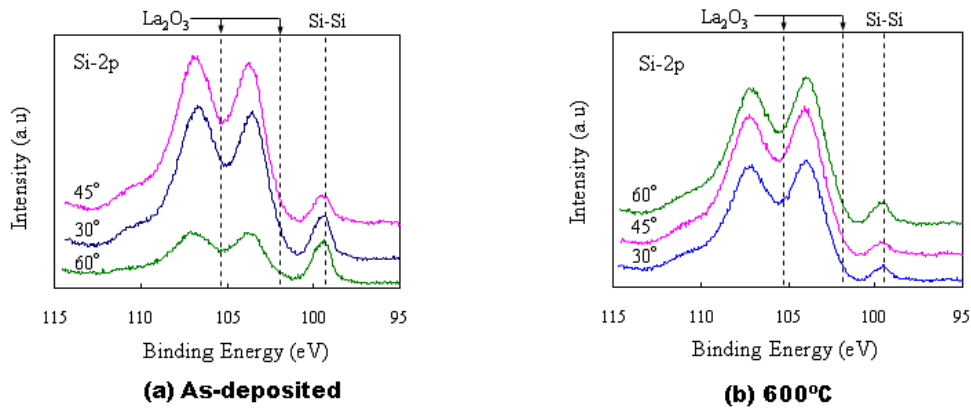


Figure 4.5: Si2p spectra of (a) As-deposited and (b) 600 °C PDA La_2O_3 samples.

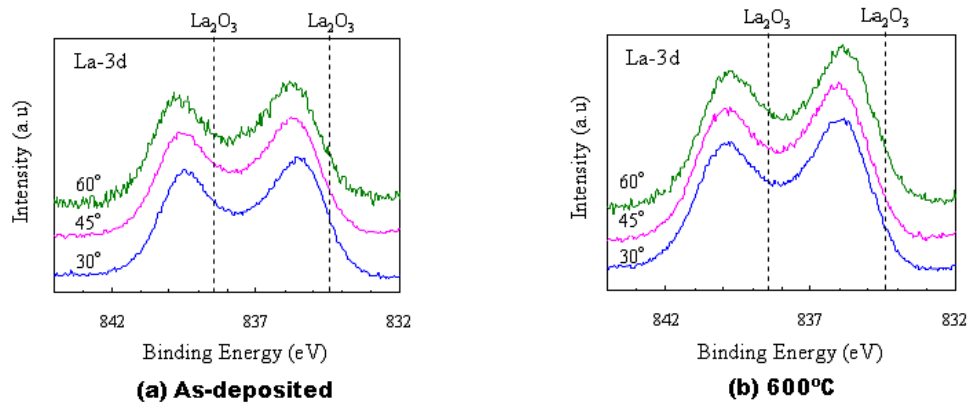


Figure 4.6: La3d spectra of (a) As-deposited and (b) 600 °C PDA La_2O_3 samples.

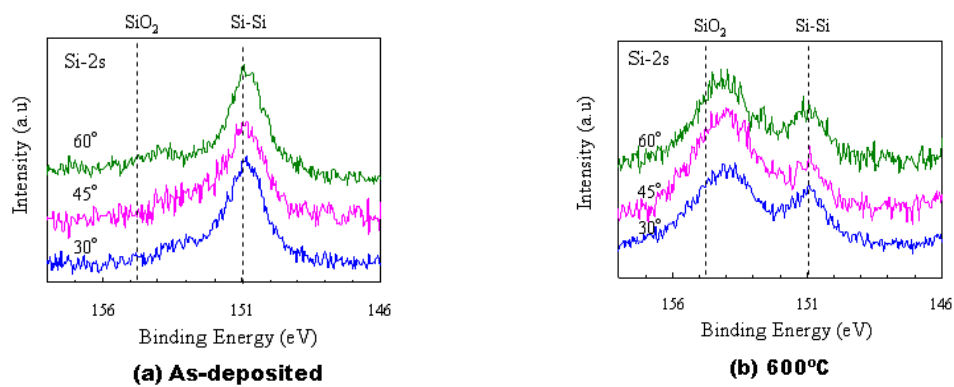


Figure 4.7: Si2s spectra of (a) As-deposited and (b) 600 °C PDA La_2O_3 samples.

4.2 XPS analyses

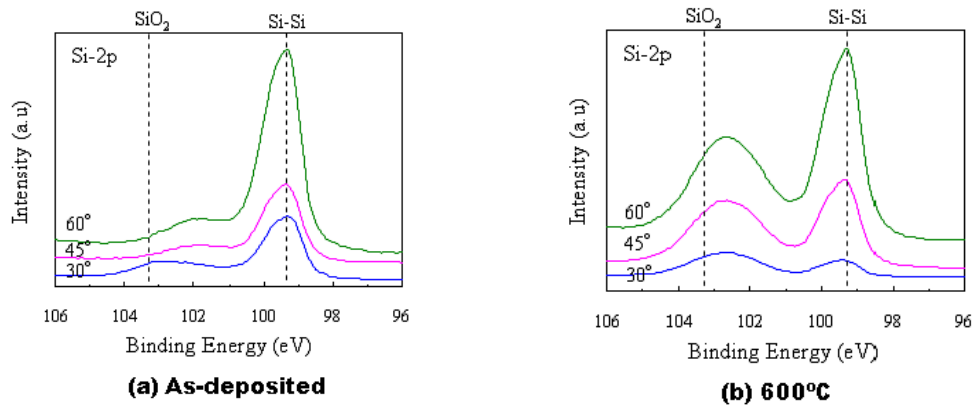


Figure 4.8: Si2p spectra of (a) As-deposited and (b) 600 °C PDA Y₂O₃ samples.

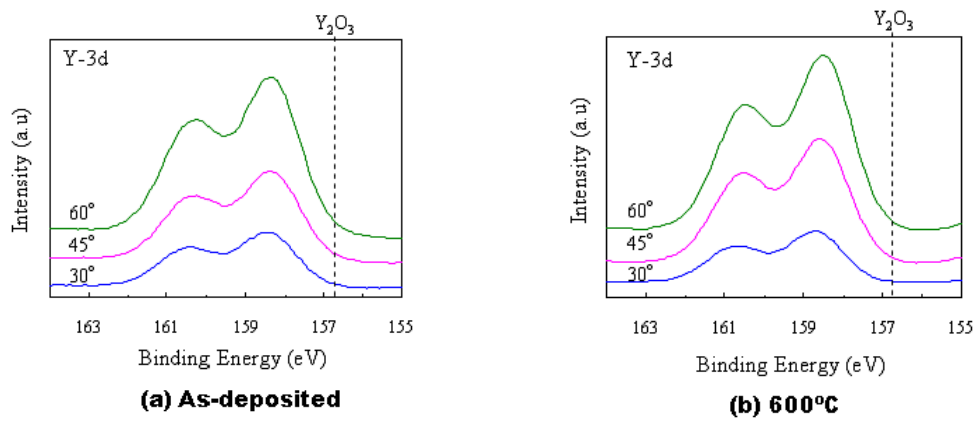


Figure 4.9: Y3d spectra of (a) As-deposited and (b) 600 °C PDA Y₂O₃ samples.

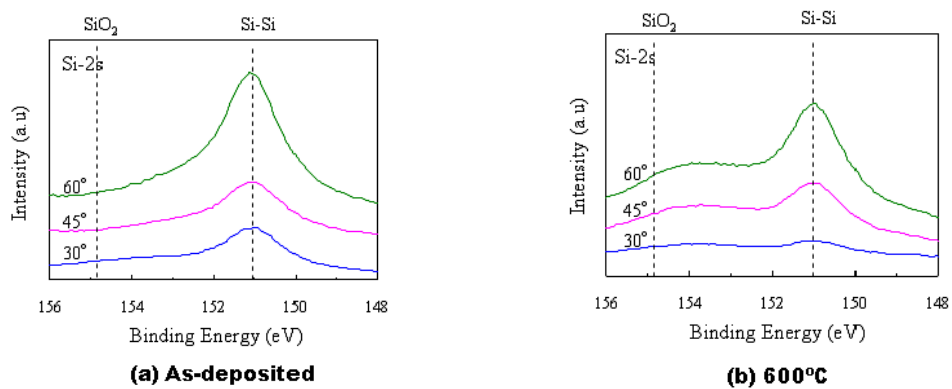


Figure 4.10: Si2s spectra of (a) As-deposited and (b) 600 °C PDA Y₂O₃ samples.

4.2 XPS analyses

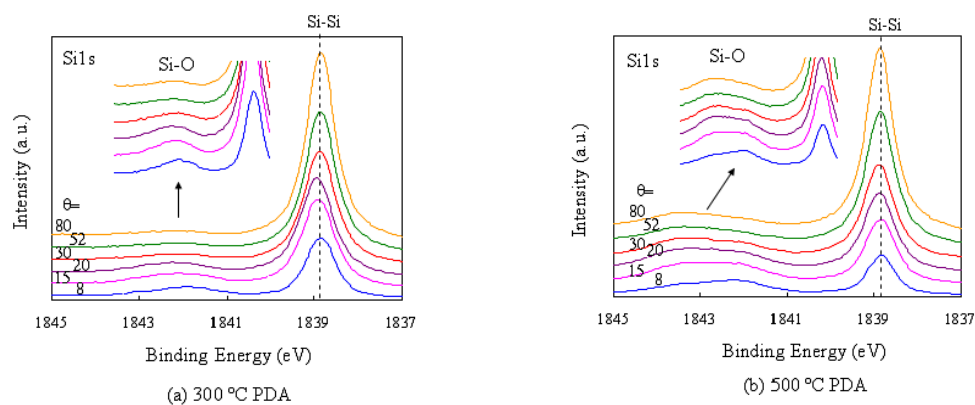


Figure 4.11: Si1s spectra of stack samples with (a) 300 °C and (b) 500 °C PDA.

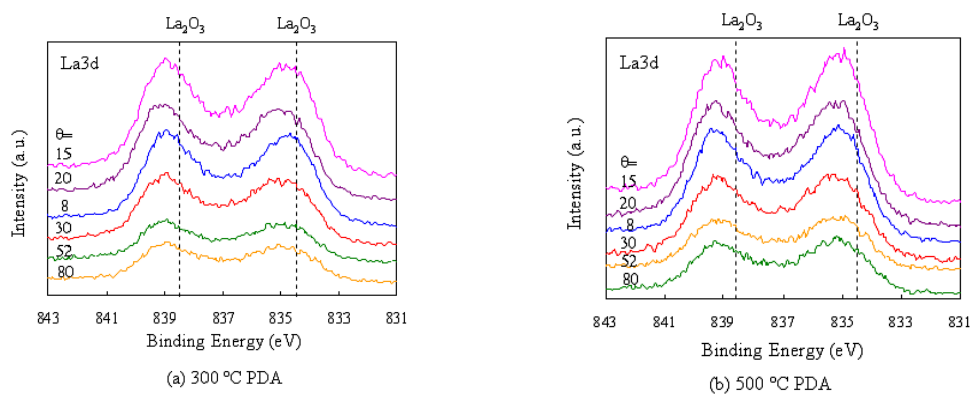


Figure 4.12: La3d spectra of stack samples with (a) 300 °C and (b) 500 °C PDA.

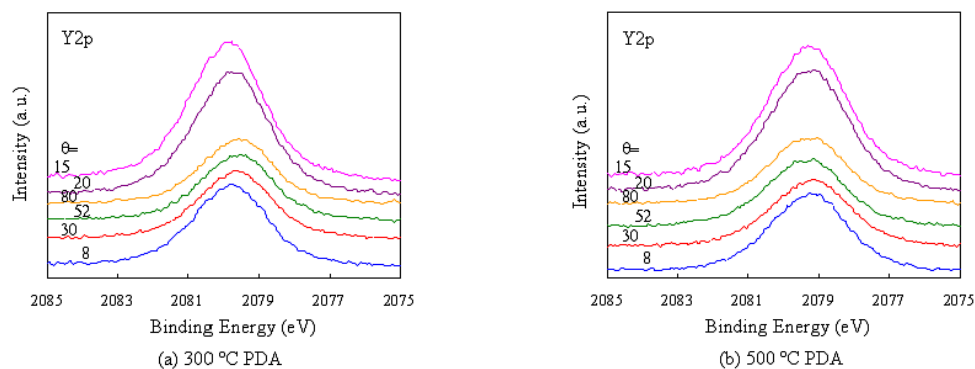


Figure 4.13: Y2p spectra of stack samples with (a) 300 °C and (b) 500 °C PDA.

The comparisons of La3d spectra between La₂O₃ monolayer and La₂O₃/Y₂O₃ stack samples are demonstrated in figure 4.14. (a) and (b) show the sample with 300 °C PDA and 500 °C PDA, respectively. Binding energy of x-axis was corrected by the peak position of Si-Si bond. The take-off angle of photoelectron was 15 °.

The obvious difference in the peak position between two samples in both PDA temperature cases was observed. The reported peak position of La₂O₃ was 834.5 eV and 838.5 eV [12]. The spectrum of La₂O₃ monolayer sample was marginally shifted to a higher-binding energy indicating the presence of a more Si-rich lanthanum silicate. Furthermore, larger shift of spectrum for La₂O₃ sample with 500 °C PDA was observed compared with 300 °C PDA indicating the proceeding of La-silicate as annealing temperature became higher. These sights are in good agreement with the results of High-resolution Rutherford Backscattering Spectrometry (HRBS). Figure 4.15 shows the compositional depth profile of 3 nm La₂O₃ film with (a) 300 °C PDA and (b) 500 °C PDA determined by an HRBS spectrum. The Si component began to be detected mere 1 nm depth from dielectric surface for 300 °C PDA sample, indicating Si diffusion into the oxide film and the presence of La-silicate. It is obvious that Si diffusion into oxide film was accentuated in the case of 500 °C PDA.

In figure 4.14, the peaks lie close to the peak position of La₂O₃ for La₂O₃/Y₂O₃ stack samples indicating that the amount of La-silicate was reduced by Y₂O₃ buffer layer. Since the limitation of La-silicate has an effect on improving dielectric constant, the EOT calculated from MOS capacitor with La₂O₃/Y₂O₃ film could be reduced.

4.2 XPS analyses

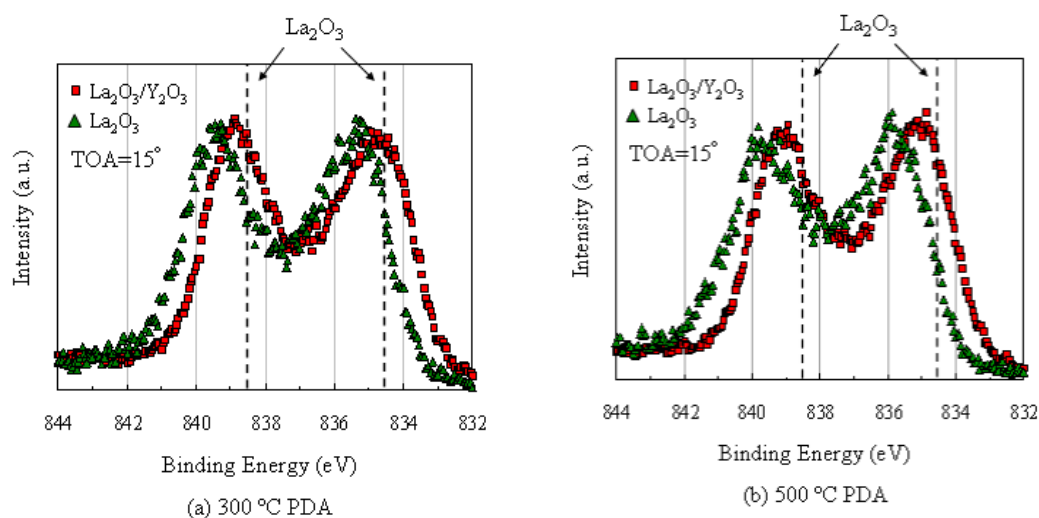


Figure 4.14: Comparison of La_{3d} spectra between La₂O₃ sample and La₂O₃/Y₂O₃ sample. (a) 300 °C PDA and (b) 500 °C PDA.

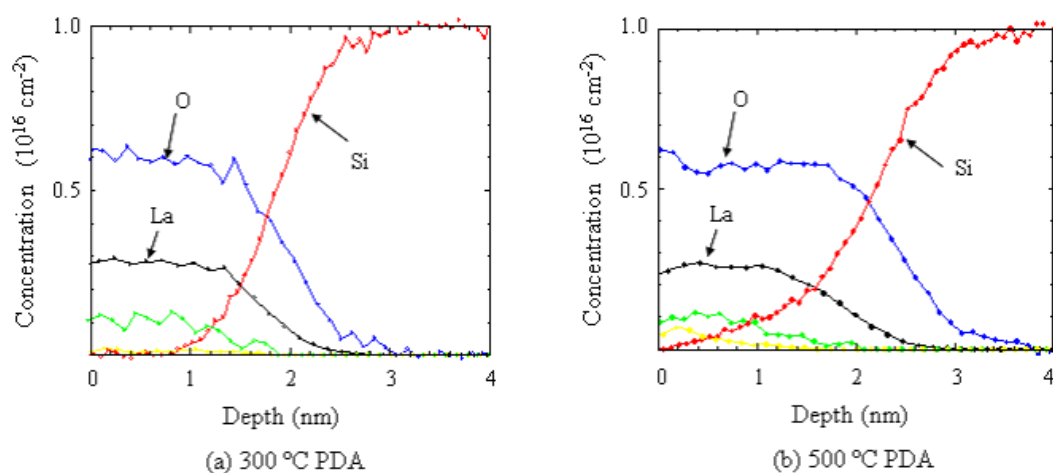


Figure 4.15: The compositional depth profile of La₂O₃ film with (a) 300 °C PDA and (b) 500 °C PDA determined by an HRBS spectra.

Figure 4.16 shows the O1s spectra in comparison between the annealing temperatures for each dielectrics of (a) La_2O_3 , (b) Y_2O_3 and (c) $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack. Photoelectrons with take off angle of 60° were detected and the peak height was normalized. For the as-deposited La_2O_3 sample, the spectra exhibits a peak at ~ 532 eV with FWHM (full width half maximum) of 2.6 eV. This peak lies between the SiO_2 and La_2O_3 peaks at 533.3 eV and 529.9 eV respectively, consistent with the formation of La-O-Si silicate bonding units. For the 600 °C PDA sample, a broader peak with FWHM of 3.0 eV than as-deposited was observed. This indicates the increase of SiO_2 peak at 533.3 eV.

For the Y_2O_3 samples, a broadness of spectra for each PDA temperatures was almost constant of 2.7eV. It is obvious that the increasing amount of SiO_2 peak was not as much as that of La_2O_3 sample even with high temperature annealing. However, Y_2O_3 peak at 529.5 eV decreased with PDA temperature, indicating the formation of Y-O-Si silicate.

For the $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack samples, SiO_2 composition seem to increase with PDA temperature. La_2O_3 or Y_2O_3 composition was observed between 529.5 eV and 529.9 eV for the as-deposited and 300 °C samples. However, their composition decreased as annealed at 600 °C.

Figure 4.17 shows the Si2s spectra compared between each dielectrics with 600 °C PDA. Take-off angle of photoelectron was 60° . Two peaks at approximately 151 eV and 154 eV were mainly observed for each dielectrics. One is corresponding to Si-Si peak and the other is products of a reaction with silicon such as silicate and silicon oxides (SiO_x). All the peak intensities were normalized by Si-Si peak intensity.

Si2s spectra for Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack film were similar indicating these dielectrics have the same interface of $\text{Y}_2\text{O}_3/\text{Si}$. The strong peak around 154 eV was observed for La_2O_3 sample compared with Y_2O_3 monolayer and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$

4.2 XPS analyses

stack suggesting the growth of significant amount of interfacial layer. The composition of SiO_2 and the silicate in the interfacial layer should be separated to obtain the SiO_2/Si and Silicate/Si area ratio.

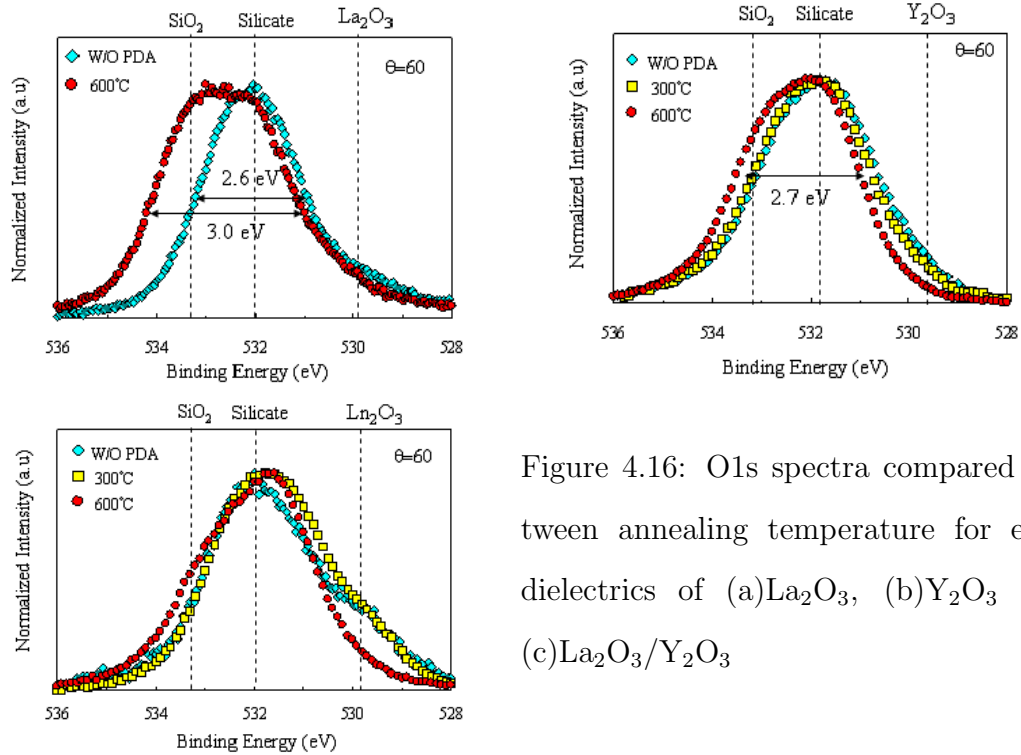


Figure 4.16: O1s spectra compared between annealing temperature for each dielectrics of (a) La_2O_3 , (b) Y_2O_3 and (c) $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$

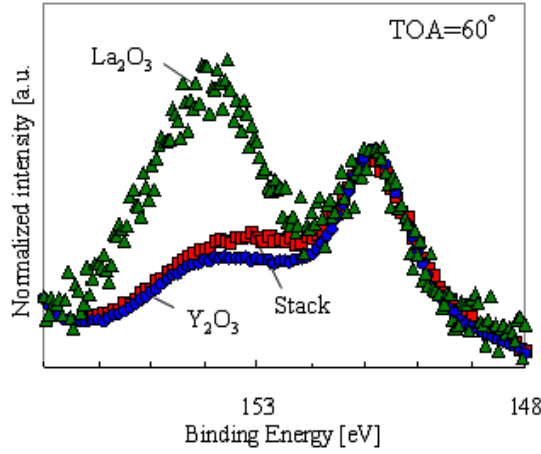


Figure 4.17: Comparison of Si2s Spectra between each dielectrics. Samples were annealed at 600 °C. Take-off angle of photoelectron was 60°.

The component part of the interfacial layer in Si2s spectra was separated into SiO₂ and silicate using following equation.

$$Y = H \left(PG \cdot \exp \left(-(\ln 2) \cdot \left(\frac{2(x - pp)}{FWHM} \right)^2 \right) + \frac{1 - PG}{1 + \left(\frac{2(x - pp)}{FWHM} \right)^2} \right) \quad (4.1)$$

where,

Y : Intensity of the spectrum H : peak height PG : Percent of Gaussian
 pp : peak position $FWHM$: Full Width Half Maximum

The peak separations of Si2s spectra were demonstrated in figure 4.18 for each dielectrics of (a) La₂O₃, (b) Y₂O₃ and (c) La₂O₃/Y₂O₃ stack films. The take off angle of photoelectrons was 60 ° and intensities of spectra were normalized by bulk-Si peak. For La₂O₃ samples, the significant increases of SiO₂ and the silicate were observed in 600 °C PDA case. For Y₂O₃ monolayer and La₂O₃/Y₂O₃ stack films, changes in SiO₂ composition with increase of PDA temperature were nearly

similar to each other. As for the silicate composition, large silicate peak in the spectra for 600 °C PDA $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film was observed. La-silicate might be formed with 600 °C PDA.

The silicate/bulk-Si and SiO_2 /bulk-Si area ratio were calculated for accurate comparisons as shown in figure 4.19 and 4.20. The silicate/bulk-Si area ratio in figure 4.19 exhibits increasing fraction of silicate for 600 °C PDA La_2O_3 film while the gradual increase for $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ and Y_2O_3 films. The La_2O_3 film was more likely to form a silicate than Y_2O_3 . In fact, an IR study of the interfacial reactions between rare-earth-metal oxides and Si substrates found that the fraction of silicate bonding increases with the ionic radius of the rare-earth element. Larger atoms, in general, leave more free space for Si diffusion[31]. Since La has a larger ionic radius than that of Y ($r_{\text{La}}=1.17$ and $r_{\text{Y}}=1.08$ [32]), La-silicate was formed more readily.

SiO_2 /bulk-Si area ratio increased for 600 °C PDA La_2O_3 film as well as silicate/bulk-Si while gradual increase of it was observed in Y_2O_3 and stack cases. $\text{Y}_2\text{O}_3/\text{Si}$ was found not to readily react with silicon substrates resulting in the growth of interfacial layer.

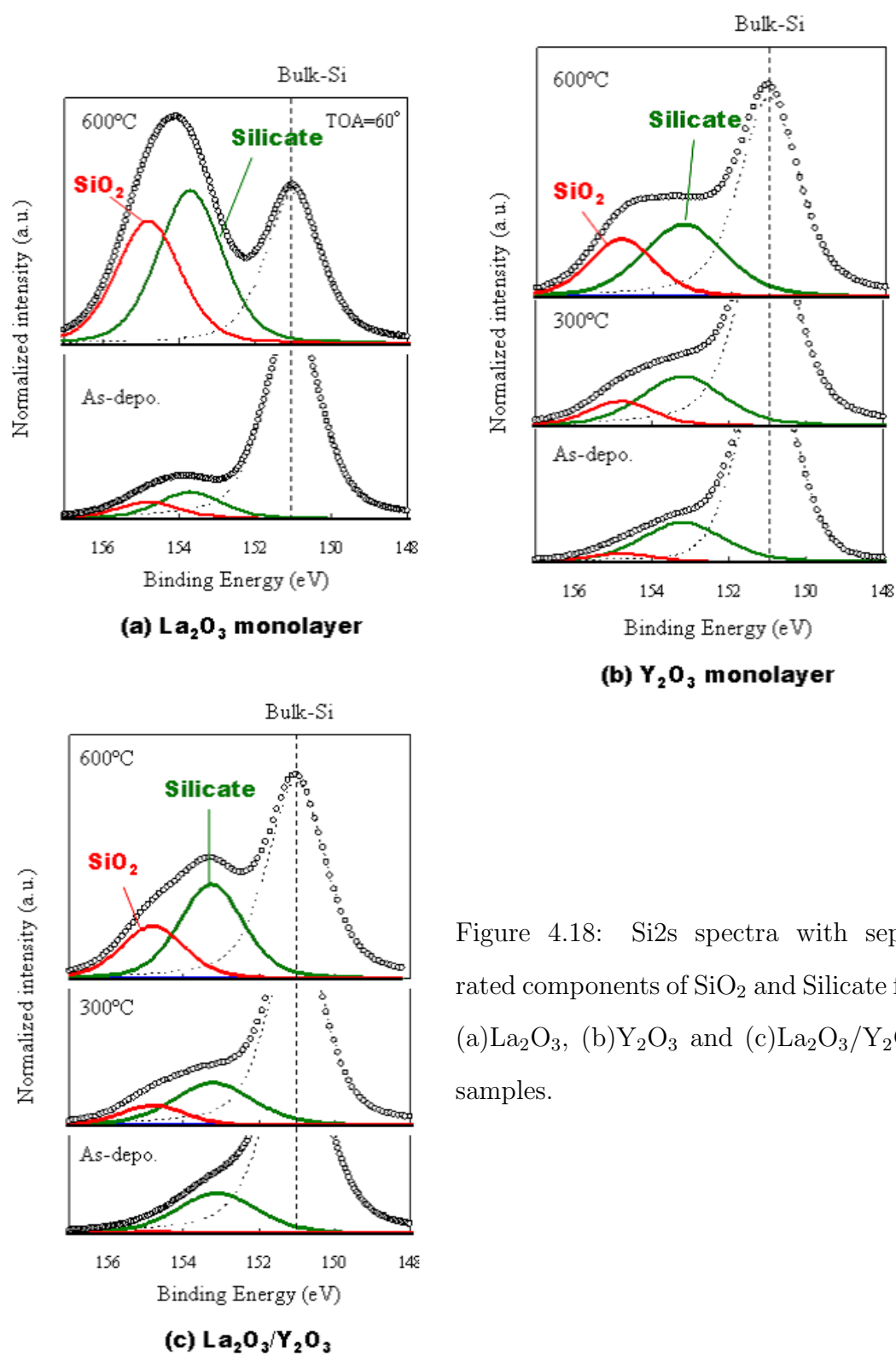


Figure 4.18: Si_{2s} spectra with separated components of SiO₂ and Silicate for (a)La₂O₃, (b)Y₂O₃ and (c)La₂O₃/Y₂O₃ samples.

4.2 XPS analyses

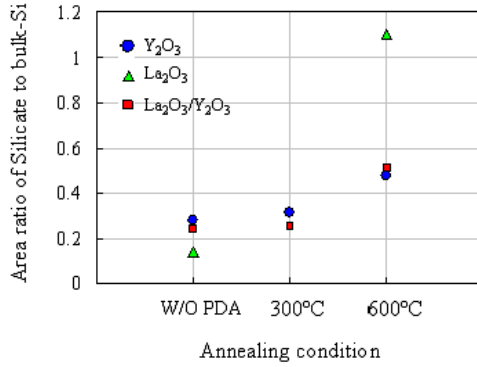


Figure 4.19: Silicate/Si area ratio.

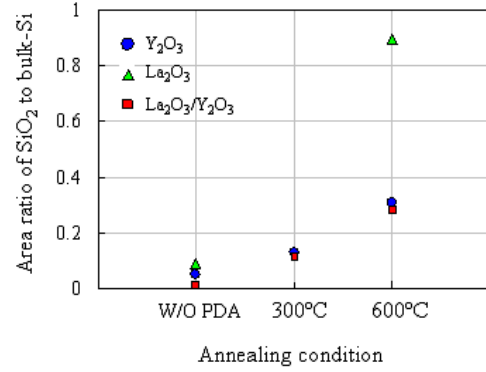


Figure 4.20: SiO₂/Si area ratio.

Only of Si2p spectra for Y₂O₃ monolayer samples were allowed to be separated because Si2p spectra for La₂O₃ and La₂O₃/Y₂O₃ overlap with the La4d spectra. The interfacial layer compositions in Si2p spectra for Y₂O₃ sample were separated into silicon oxides (SiO_x) and the silicates to test the credibility of the results of separation of Si2s spectra. Si1s spectra for La₂O₃/Y₂O₃ samples measured by BL47XU in the SPring-8 facilities are also capable to be separated into Si-O bonding compositions.

It is necessary to introduce the silicate model prior to peak separation. Figure 4.21 shows the model for the structure of silicon oxides and the silicate. Assuming that the silicon combined with four oxygen atoms was as a Si⁴⁺ and one oxygen atom combined with La or Y was as a silicate, silicate peak will lie between Si⁴⁺ and Si³⁺ peak because of the difference in electronegativity between silicon and rare earth metals ($\chi_{Si}=1.8$, $\chi_{La} = \chi_{Y}=1.2$). Hence, the peak of Si⁴⁺ with La or Y must be shifted to a negative side.

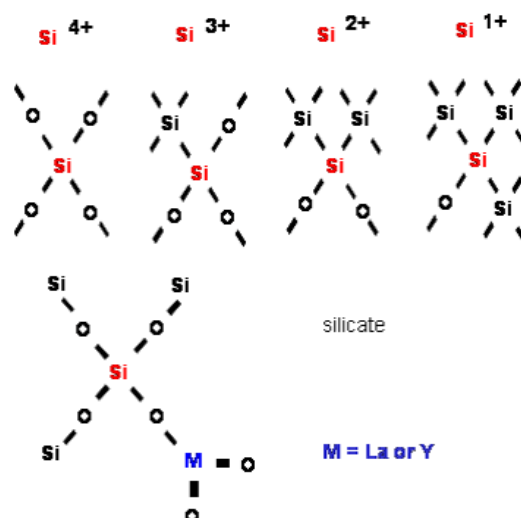


Figure 4.21: Assumed silicate model for peak separation of Si1s spectra.

The peaks separated Si2p spectra and Si1s spectra for Y_2O_3 monolayer and La_2O_3/Y_2O_3 respectively were demonstrated in figure 4.22 and 4.23.

For as-deposited Y_2O_3 sample, the peaks of silicon sub-oxides were dominant and the silicate peak increased with 300 °C annealing. For 600 °C PDA Y_2O_3 film, the silicate was more likely to increase and SiO_2 peaks also increased. Y_2O_3 monolayer was found to be the silicate dominant. These results are clearly in good agreement with the results of Si2s spectra.

For La_2O_3/Y_2O_3 stack film, the amount of SiO_2 were considerably small and the silicate and silicon sub-oxides peaks were relatively large for as-deposited sample. With 300 °C PDA, the silicate and the silicon sub-oxides peaks slightly increased. This silicate peak will be contributed to yttrium silicate because the amount of lanthanum silicate must be reduced by Y_2O_3 buffer layer as shown in figure 4.14. SiO_2 was found not to grow at 300 °C PDA. The increase of Si^{4+} peak in the spectrum for 400 °C PDA sample was observed. It was found that the SiO_2 began to proceed at around 400 °C PDA temperature. Although the increase of

4.2 XPS analyses

the silicate peak was observed in 500 °C PDA spectrum, the increasing amount of SiO₂ was a little. The growth of SiO₂ is expected to be saturated at around 500 °C PDA temperature. Yet utilized XPS equipments and analyzed spectra were different, compositions in the interfacial layer for Y₂O₃ and La₂O₃/Y₂O₃ films were found to be similar.

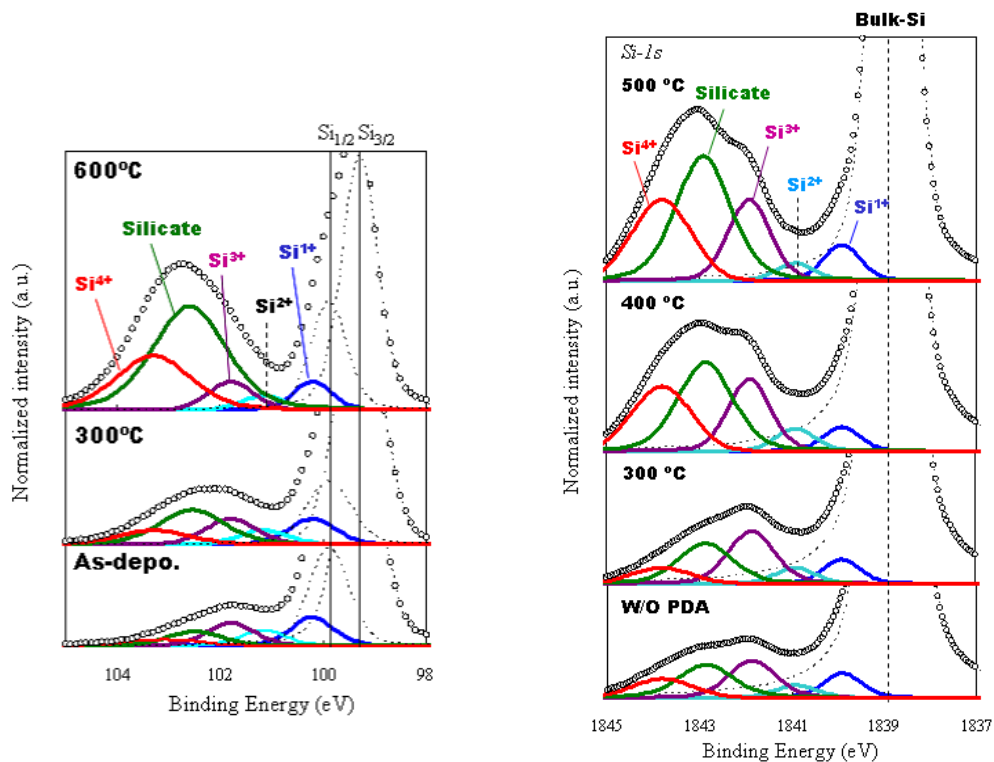


Figure 4.22: Si2p spectra for Y₂O₃ samples with separated components.

Figure 4.23: Si1s spectra for La₂O₃/Y₂O₃ samples with separated components.

4.3 Conclusion

Morphological analyses on La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ films with O_2 PDA were examined. $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ films were found to decrease the surface roughness with increase of annealing temperature while it increased with annealing temperature in La_2O_3 and Y_2O_3 monolayer case.

Chemical compositions in La_2O_3 , Y_2O_3 , $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ and the interfacial layer between silicon and dielectrics were analyzed using X-ray.

The $\text{La}_2\text{O}_3/\text{Si}$ interface was found to readily react with silicon substrate during high temperature treatment and grow SiO_2 interfacial layer. HRBS and XPS analyses revealed the La-silicate formation even for as-deposited La_2O_3 film and it proceeded with increase of annealing temperature.

It was shown that La-silicate formation in the $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack film was limited by Y_2O_3 buffer layer. Furthermore, The $\text{Y}_2\text{O}_3/\text{Si}$ interface showed less growth of SiO_2 interfacial layer than the $\text{La}_2\text{O}_3/\text{Si}$ interface especially in high temperature PDA case.

Chapter 5

THE ELECTRICAL CHARACTERISTICS OF N-MOSFETS

5.1 Introduction

In this section, the electrical characteristics of n-MOSFETs will be discussed. n-MOSFETs listed as below were fabricated. All the films were annealed after dielectric deposition in N₂ ambient at 300 °C, 400 °C and 600 °C for 5 minutes. Al was used as gate electrodes.

- With a thickness of 4.2 nm La₂O₃ monolayer film.
- With a thickness of 3.5 nm Y₂O₃ monolayer film.
- With 5.5 nm thick La₂O₃/Y₂O₃ stack film.
- With 3.3 nm thin La₂O₃/Y₂O₃ stack film.

In general, MOSFET with thin La₂O₃ film was not operated due to the significant gate leakage. 4 nm thick La₂O₃ film might be outer limit for operating the MOSFET.

However, n-MOSFET with 1 nm EOT ($T_{\text{phy}}=3.5$ nm) of La₂O₃/Y₂O₃ was successfully fabricated and evaluated. Since Y₂O₃ buffer layer has an effect reducing the gate leakage currents without increasing EOT as shown in the section 3, physical thickness of Y₂O₃ or La₂O₃/Y₂O₃ could be minimized as far as possible.

5.2 Current - Voltage (I-V) Characteristics

The operation of n-MOSFETs with dielectrics of La₂O₃, Y₂O₃ and stack was confirmed as demonstrated in figure 5.1-5.4. Annealing conditions were (a) 400 °C as a low temperature annealing and (b) 600 °C as a high temperature annealing in N₂. Drain current ($\mu\text{A}/\mu\text{m}$) was normalized by multiplying EOT value of the sample.

5.2 Current - Voltage (I - V) Characteristics

The noteworthy is the heat treatment dependence on the amount of drain currents between La_2O_3 and Y_2O_3 dielectrics. EOT should increase with increase of annealing temperature for both La_2O_3 and Y_2O_3 dielectrics. However, the normalized drain currents increased by high temperature annealing for Y_2O_3 MOSFETs, in stark contrast, it decreased for La_2O_3 MOSFETs. In the $I_d - V_d$ characteristics of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stacks, the normalized drain current increased with increase of annealing temperature. These difference might be associated with the interface charge trap density. The interface charge trap will be discussed in detail in the section of Charge pumping.

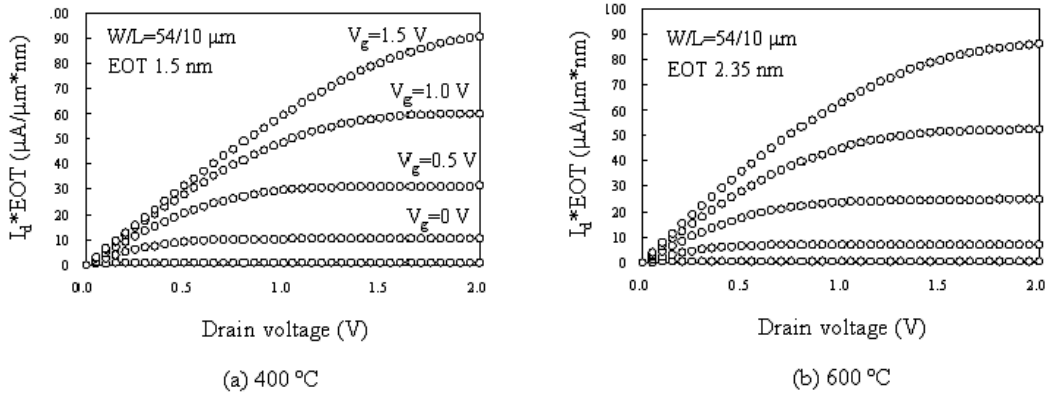


Figure 5.1: $I_d - V_d$ characteristics of La_2O_3 n-MOSFETs.

5.2 Current - Voltage (I - V) Characteristics

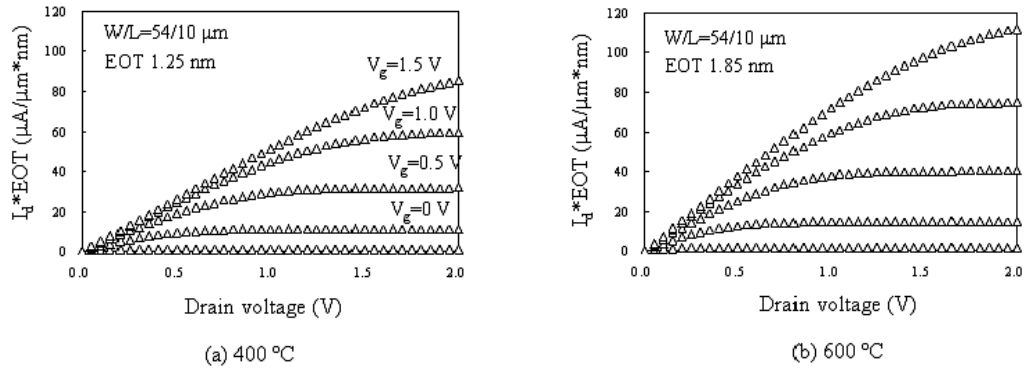


Figure 5.2: $I_d - V_d$ characteristics of Y_2O_3 n-MOSFETs.

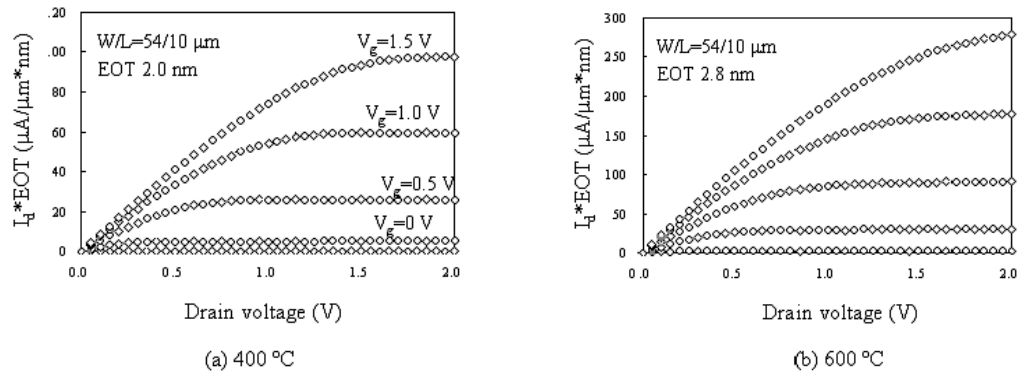


Figure 5.3: $I_d - V_d$ characteristics of thick stack n-MOSFETs.

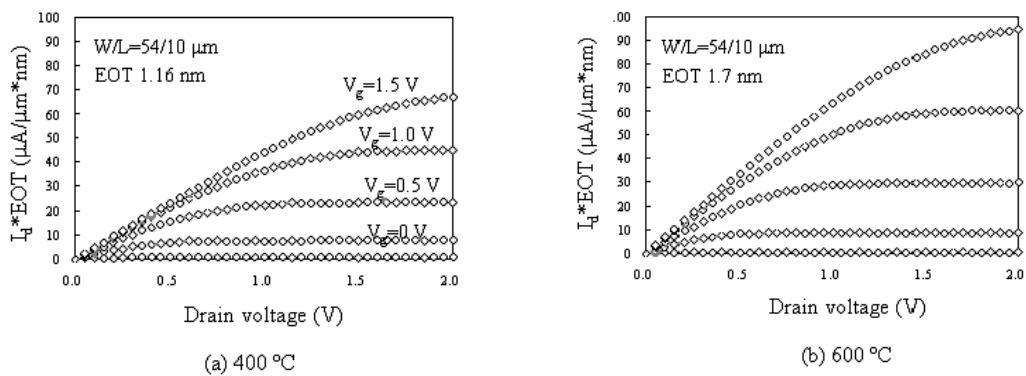


Figure 5.4: $I_d - V_d$ characteristics of thin stack n-MOSFETs.

5.2 Current - Voltage (*I-V*) Characteristics

$I_d - V_g$ and $J_g - V_g$ characteristics of La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ films annealed at 600 °C were shown in figure 5.5(a)-(d). Drain voltage was constant of 0.1 V.

Gate leakage current density was approximately 10^{-5} to 10^{-4} level for each samples. However, the difference in the amount of gate leakage between each samples was hardly observed.

Threshold voltage V_{th} was obtained from $I_d - V_g$ characteristics. Figure 5.6 shows V_{th} as a function of annealing temperature. For La_2O_3 and Y_2O_3 monolayer samples, absolute V_{th} are relative large. However, in the case of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack samples, absolute value of V_{th} was smaller. Al_2O_3 has a negative fixed charge while La_2O_3 and Y_2O_3 have a positive fixed charge. Hence, it is reasonable to consider that negative charge in Al_2O_3 which was grown at $\text{La}_2\text{O}_3/\text{Gate}$ interface cancelled positive charge in La_2O_3 and/or Y_2O_3 out. Furthermore, in the case of stack films, since Y_2O_3 buffer layer was expected to prevent oxygen deficiency, the generations of positive fixed charge were limited.

Subthreshold slope (S.S.) was calculated from $I_d - V_g$ slope in the subthreshold region. For the Y_2O_3 and stack MOSFETs annealed at 600 °C, excellent S.S. values were obtained while S.S. value of 600 °C annealed La_2O_3 became worse. S.S. as a function of annealing temperature is shown in figure 5.7. For Y_2O_3 monolayer samples, excellent S.S. values were obtained in each annealing conditions. For La_2O_3 MOSFETs, S.S. values were relatively large and it became larger by 600 °C annealing. For $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$, S.S. for 300 °C annealed MOSFETs were significantly worse. However they were improved by 600 °C annealing. A tendency of S.S. with annealing temperature was in contrast to that of La_2O_3 film.

5.2 Current - Voltage (I - V) Characteristics

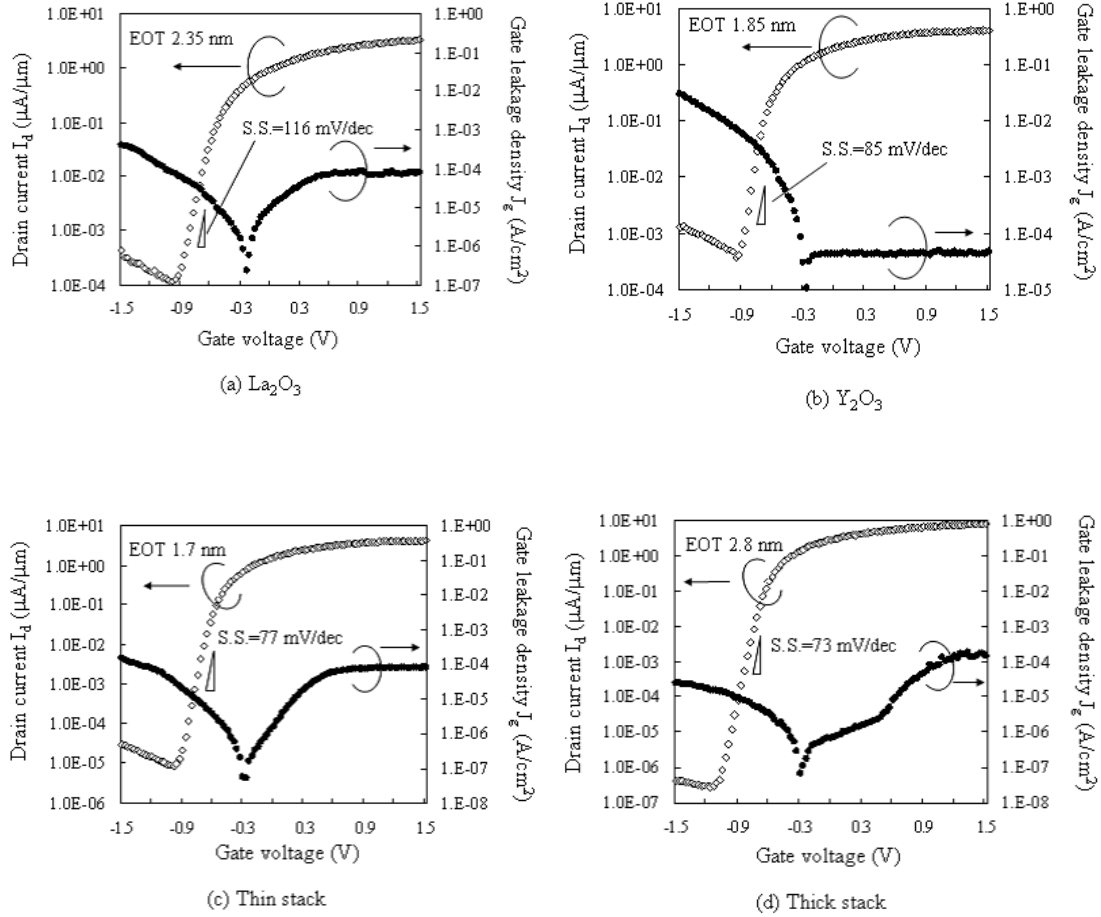


Figure 5.5: Drain current vs. Gate voltage ($I_d - V_g$) and Gate leakage vs. Gate voltage ($J_g - V_g$) characteristics of (a) La_2O_3 , (b) Y_2O_3 , (c)thin $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack and (d)thick $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack dielectrics annealed at 600°C . V_d was a constant of 0.1 V.

5.2 Current - Voltage (I - V) Characteristics

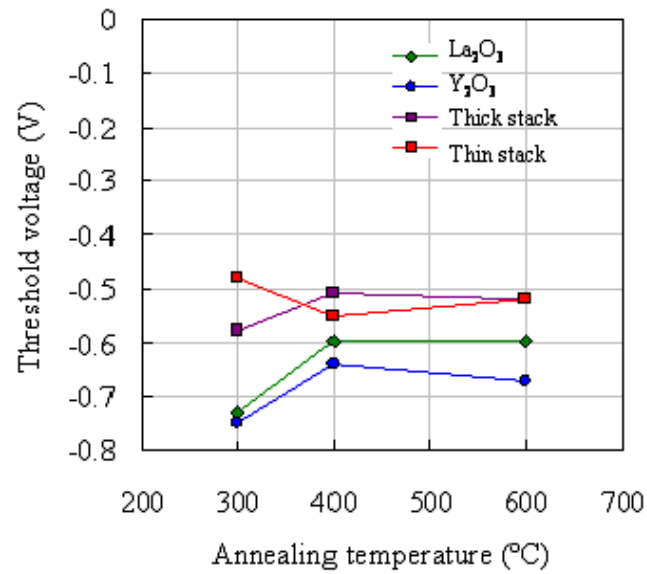


Figure 5.6: Threshold voltage (V_{th}) as a function of annealing temperature.

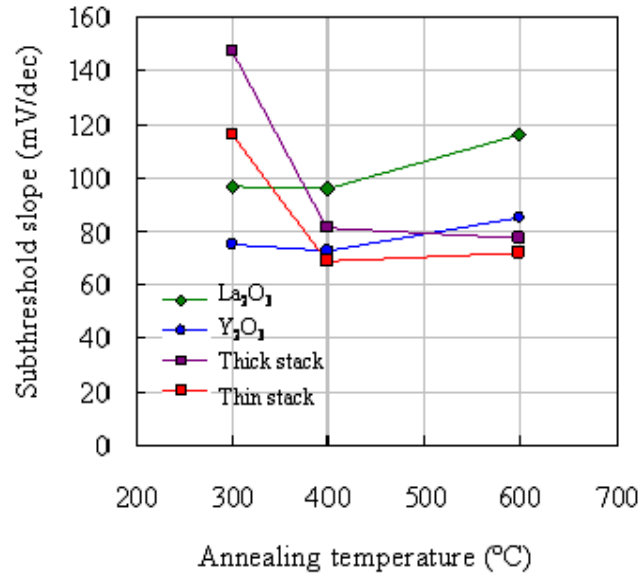


Figure 5.7: Subthreshold slope (S.S.) as a function of annealing temperature.

5.3 The Effective Mobility

The effective mobility (μ_{eff}) was calculated by split CV method and μ_{eff} was plotted as a function of effective electric field (E_{eff}).

Figure 5.8 shows μ_{eff} vs. E_{eff} characteristics for La_2O_3 samples with parameterized annealing temperature. The highest effective mobility was obtained for 400 °C PDA MOSFET. For both 300 °C and 600 °C cases, lower mobility than 400 °C PDA were obtained. The effective mobility for the MOSFET with a high-temperature PDA La_2O_3 film was degraded by the interface states or oxide traps.

Figure 5.9 shows μ_{eff} vs. E_{eff} characteristics for Y_2O_3 samples with parameterized annealing temperature. The results of Y_2O_3 samples exhibited the contrastive tendency compared to La_2O_3 case. Maximum mobility of 300 °C sample was 150 cm^2/Vs at EOT of 1.2 nm and 236 cm^2/Vs for 600 °C sample at EOT of 1.85 nm. The higher annealing temperature became, the higher maximum mobility became. The mobility was not degraded even with high temperature PDA for Y_2O_3 MOSFET.

The effect of Y_2O_3 on effective mobility was observed in the results of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack samples. Figure 5.10 and 5.11 show effective mobility characteristics of thin stack film and thick stack film, respectively. The mobility was not degraded with high temperature annealing as well as Y_2O_3 MOSFET. However, the mobility degradation due to difference in film thickness was observed. Thinner thickness of stack film exhibited more degradation of the effective mobility. Comparing 600 °C samples, maximum mobility was 181 cm^2/Vs for thinner film while 221 cm^2/Vs for thicker film. In general, thinner EOT and/or higher dielectric constant tend to degrade carrier mobility.

5.3 The Effective Mobility

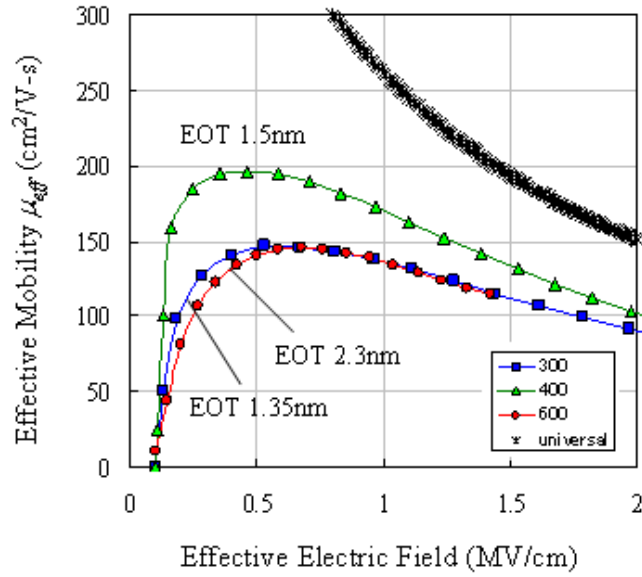


Figure 5.8: μ_{eff} vs. E_{eff} for La_2O_3 samples with various annealing temperature.

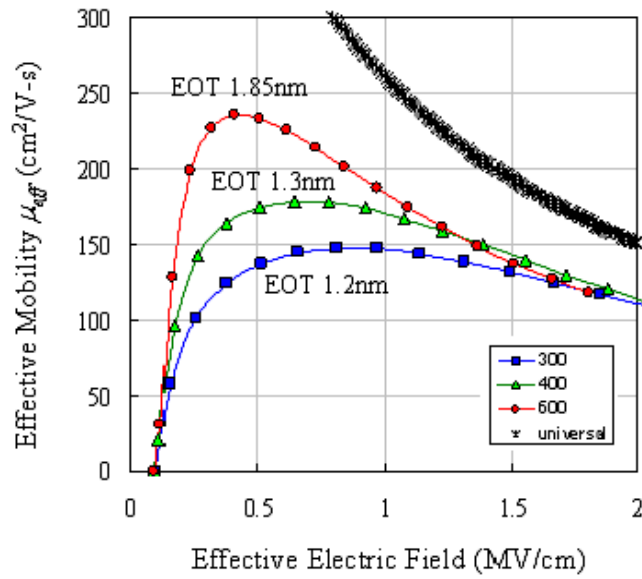


Figure 5.9: μ_{eff} vs. E_{eff} for Y_2O_3 samples with various annealing temperature.

5.3 The Effective Mobility

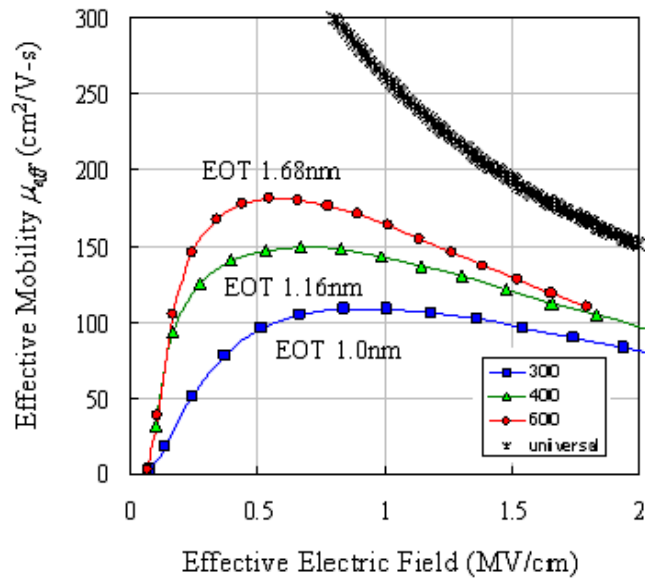


Figure 5.10: μ_{eff} vs. E_{eff} for thin stack samples with various annealing temperature.

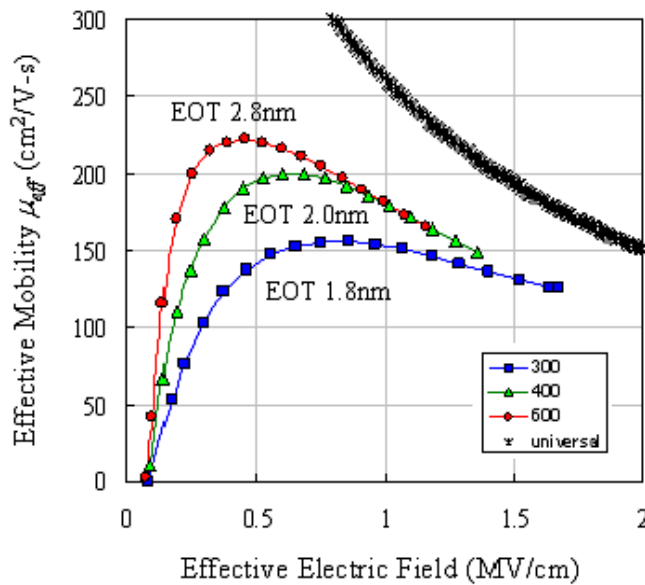


Figure 5.11: μ_{eff} vs. E_{eff} for thick stack samples with various annealing temperature.

5.3 The Effective Mobility

Figure 5.12 show effective mobility at 0.8 MV/cm as a function of EOT.

Y_2O_3 MOSFETs exhibited an excellent characteristics with thinner EOT and higher effective mobility.

For La_2O_3 MOSFETs, appropriate annealing condition must be low temperature because the higher annealing temperature became, EOT increased and mobility degraded.

For stack MOSFETs, EOT could be reduced compared to La_2O_3 and Y_2O_3 monolayer sample. However, the mobility with the same EOT was lower value than Y_2O_3 . As compared to La_2O_3 sample, significant difference in high temperature annealing was observed.

In summary, Y_2O_3/Si and La_2O_3/Si interface was different property especially in high temperature states. Following section will reveal the difference in the interface states between Y_2O_3/Si and La_2O_3/Si .

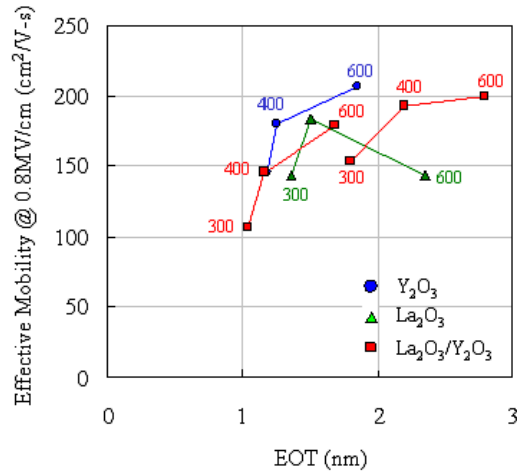


Figure 5.12: μ_{eff} at 0.8 MV/cm vs. EOT.

5.4 Characterization of Interface States by Charge Pumping Method

The interface states density was characterized by charge pumping method. Three kinds of waveforms of square, triangular and trapezoidal pulse were applied to gate electrode.

Figure 5.13 shows the charge pumping current (I_{cp}) applying the square waveform pulse as a function of pulse base voltage. Pulse frequency was 100 kHz, pulse amplitude 2.0 V and reverse bias to drain and source electrodes was 0.5 V. Some of the samples annealed at 300 °C could not be measured due to significant leakage current.

For La_2O_3 MOSFETs, I_{cp} was large at 300 °C and 600 °C PDA samples, indicating larger interface states density. The lowest I_{cp} was observed in 400 °C PDA case.

Y_2O_3 MOSFETs showed large I_{cp} in 400 °C PDA case while I_{cp} was smaller in 600 °C PDA case, indicating the reduction of interface states density by high temperature annealing.

The MOSFETs with thin or thick $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ film were fabricated and the I_{cp} tend to decrease with increase of annealing temperature for both thin and thick film. This tendency was the same as Y_2O_3 monolayer MOSFET.

These charge pumping profiles revealed a difference in the interface states between $\text{La}_2\text{O}_3/\text{Si}$ and $\text{Y}_2\text{O}_3/\text{Si}$ interface i.e. the interface states density is reduced with increase of PDA temperature in the $\text{Y}_2\text{O}_3/\text{Si}$ interface while it increased with PDA temperature in the $\text{La}_2\text{O}_3/\text{Si}$ interface. The detail analyses on the difference between high-temperature treated $\text{La}_2\text{O}_3/\text{Si}$ $\text{Y}_2\text{O}_3/\text{Si}$ were performed as follow.

5.4 Characterization of Interface States by Charge Pumping Method

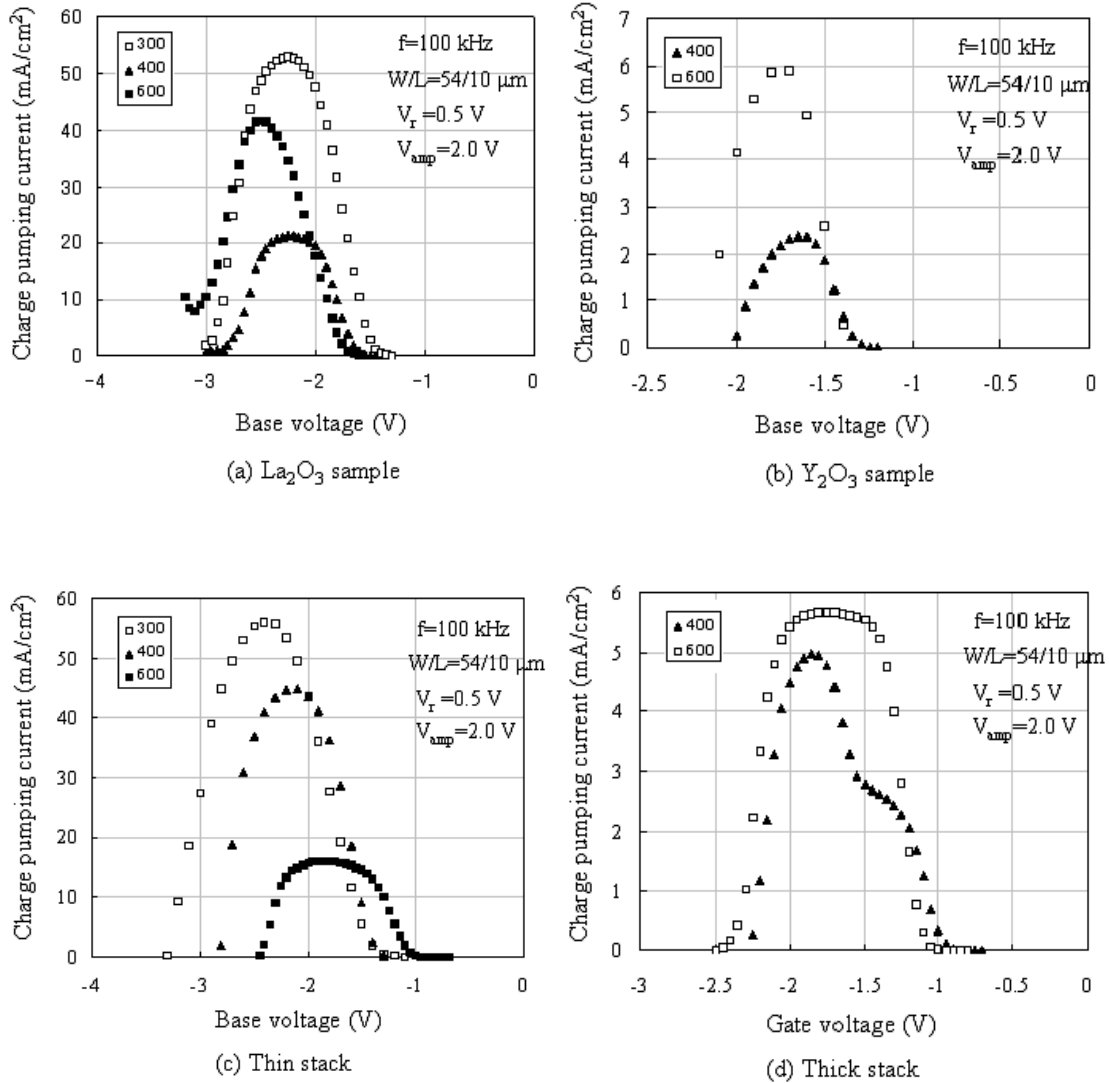


Figure 5.13: Charge pumping currents I_{cp} vs. pulse base voltage for (a) La_2O_3 , (b) Y_2O_3 , (c) thin $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack and (d) thick stack film. Pulse waveform was square, the frequency 100 kHz, the pulse amplitude 2.0 V and the reverse bias to source and drain electrode was 0.5 V.

5.4 Characterization of Interface States by Charge Pumping Method

Figure 5.14 shows a recombined charge per pulse I_{cp}/f as a function of frequency for La_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFETs with 600 °C PDA. Triangular pulses with frequencies of 1kHz \sim 500kHz and amplitude of 3.5 V were applied to gate electrode.

Mean capture cross-section σ was extracted using equation (32). σ was $4.7 \times 10^{-15} \text{cm}^2$ for the La_2O_3 MOSFET while $1.6 \times 10^{-15} \text{cm}^2$ for the $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFET. La_2O_3 showed higher capture cross-section indicating that high-temperature treated $\text{La}_2\text{O}_3/\text{Si}$ more likely to capture the carrier than $\text{Y}_2\text{O}_3/\text{Si}$. In terms of recombined charge per pulse, La_2O_3 showed higher value. This indicates the higher interface trap density. However, σ is the mean value multiplied capture cross-section of electrons (σ_n) by that of holes (σ_p). σ_n and σ_p should be extracted so that a consideration to the impact of the interface states on n-channel carrier can be made.

For this purpose, the trapezoidal waveform pulse CP measurement was performed. The trapezoidal pulse as shown in figure 2.23 was used, varying rise-time (t_r) with fixed fall-time (t_f) or varying fall-time (t_f) with fixed rise-time (t_r). The sweep range of t_r and t_f was from 125 ns to 1250 ns, fix trasient time was a constant 125 ns and pulse frequency was 100 kHz.

Figure 5.15 shows the charge pumping current I_{cp} as a function of rise-time or fall-time for (a) La_2O_3 (b) $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFETs with 600 °C PDA. For La_2O_3 MOSFET, more fall-time dependence of the charge pumping current was observed. This indicates that the density of the interface traps for electron carriers than hole carriers. Fall/rise time dependence of I_{cp} was very weak for $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFETs. There might be almost no differences in the interface trap density between electrons and holes in $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFET case. In addition, the charge pumping current was totally higher for La_2O_3 MOSFET indicating the higher trap density.

5.4 Characterization of Interface States by Charge Pumping Method

The capture cross-sections of electrons (σ_n) were extracted by the linear fitting of I_{CP}/f vs. $\ln(t_r * t_f)^{1/2}$ with fixed rise-time, which was demonstrated in figure 5.16 for $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFET. Following equation was used for σ_n extraction[33].

$$I_{CP}/f = 2qD_{it}A_gkT \left(\ln\sqrt{t_r t_f} + \ln \left(\frac{|V_{fb} - V_{th}|}{|V_{amp}|} \nu_{th} n_i \sqrt{\sigma_n \sigma_p} \right) \right) \quad (5.1)$$

where,

q : electron charge, A_g : channel area, k : boltzmann's constant, T : temperature

ν_{th} : thermal velocity of the carriers, V_{amp} : pulse amplitude

n_i : intrinsic carrier concentration, V_{fb} : flatband voltage, V_{th} : threshold voltage.

The σ_p was calculated as $\sigma_p = \sigma^2/\sigma_n$. The results are shown in table 5.1. The σ_p and σ_n for $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFET showed the subequality while the large difference was observed for La_2O_3 MOSFET. This indicates the electrons are more likely to be captured in the interface traps.

Equations 2.26-2.29 would give the energy distributions of the interface trap density. Figure 5.17 and cpdiststack shows the density of interface traps as a function of energy in the Si bandgap. Room-temperature charge pumping measurement do not allow to extract D_{it} closer to the band edges because of thermal emission.

It is obvious that the interface trap densities D_{it} of La_2O_3 MOSFET are totally higher than $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFET. Furthermore, focussing on the difference between the trap densities in negative side and that in positive side, the trap densities in positive side are slightly high. This indicates that interface traps above midgap are more effective in capturing electrons than interface traps below midgap in capturing holes. Therefore, the electron mobility was degraded

5.4 Characterization of Interface States by Charge Pumping Method

by interface trap density above midgap for high temperature treated La_2O_3 n-MOSFET.

As for $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack, energy distributions of the interface traps were almost the symmetric on either side. And figure 5.18 showed the lower interface states than La_2O_3 MOSFET. Y_2O_3 buffer layer covers the increase of the interface trap density in high-temperature treated La_2O_3 MOSFET.

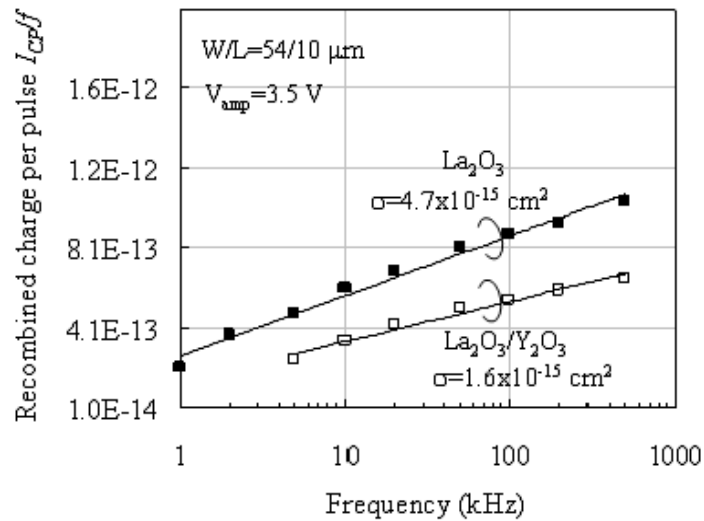
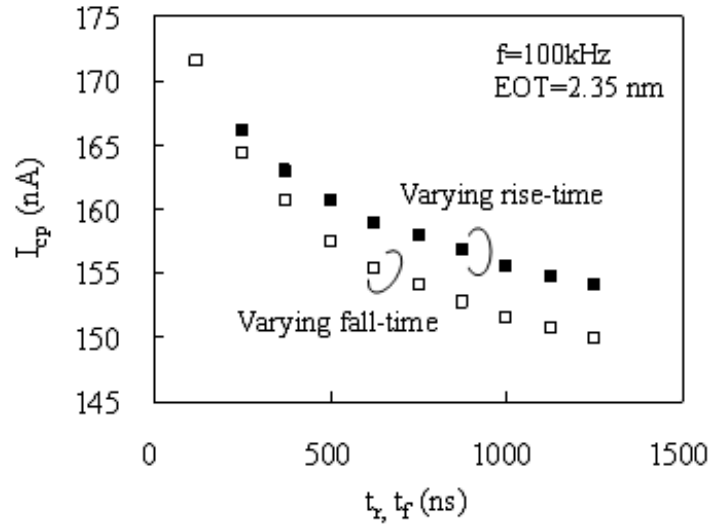
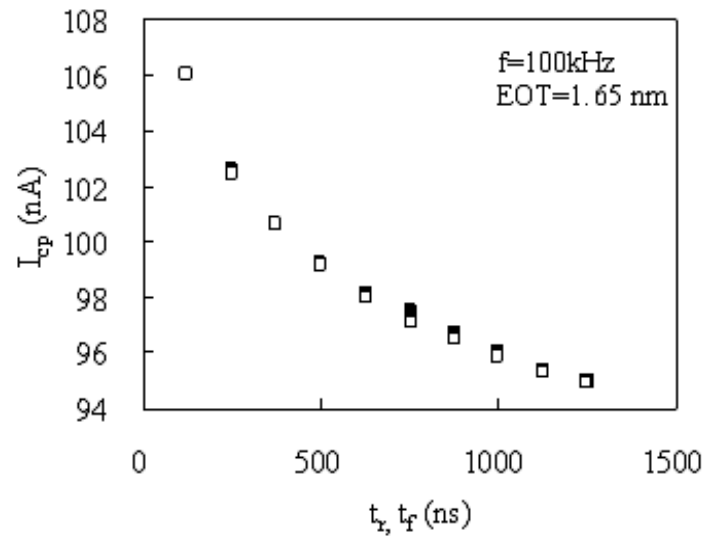


Figure 5.14: Recombined charge per pulse I_{cp}/f vs. pulse frequencies for La_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFETs with $600 \text{ } ^\circ\text{C}$ PDA. Triangular pulse ($t_r=t_f$) was used.

5.4 Characterization of Interface States by Charge Pumping Method



(a) La_2O_3



(b) $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$

Figure 5.15: The charge pumping current I_{cp} as a function of rise-time or fall-time for (a) La_2O_3 (b) $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFETs with $600\text{ }^\circ\text{C}$ PDA.

5.4 Characterization of Interface States by Charge Pumping Method

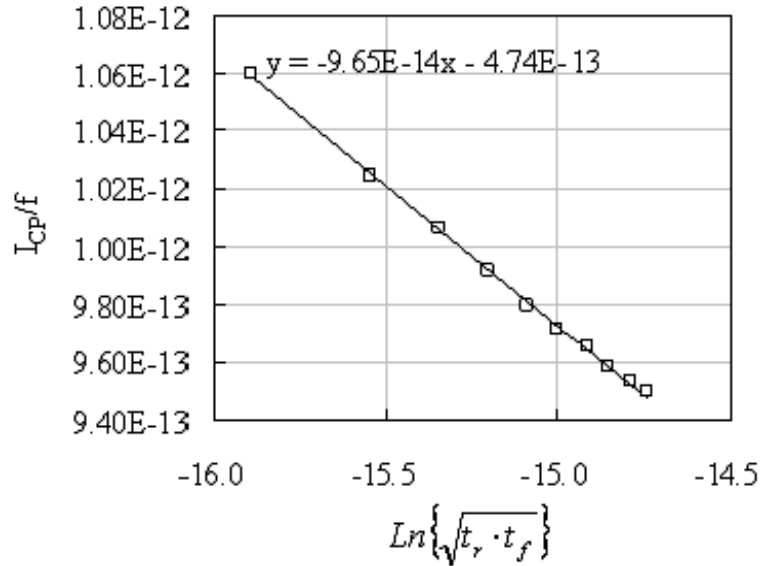


Figure 5.16: I_{cp}/f vs. $\text{Ln}(t_r * t_f)^{1/2}$ which provides the capture cross-section of electrons and holes. Trapezoidal pulse was used.

Table 5.1: Mean capture cross-section σ , extracted capture cross-section of electrons and holes, σ_n and σ_p .

	La_2O_3	$\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$
Mean capture cross-section σ	$4.7 \times 10^{-15} \text{cm}^2$	$1.6 \times 10^{-15} \text{cm}^2$
σ_n	$6.7 \times 10^{-15} \text{cm}^2$	$1.52 \times 10^{-15} \text{cm}^2$
σ_p	$3.3 \times 10^{-15} \text{cm}^2$	$1.7 \times 10^{-15} \text{cm}^2$

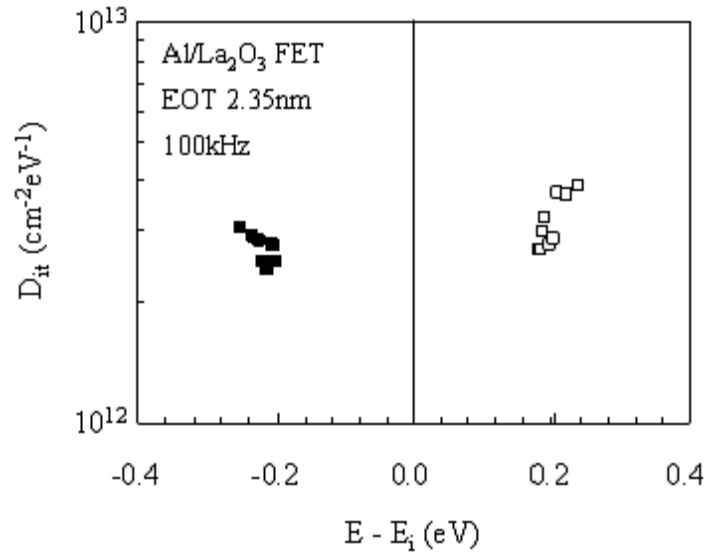


Figure 5.17: Energy distribution of interface traps as determined by rise/fall time dependence of charge pumping currents for La₂O₃ MOSFET with 600 °C PDA.

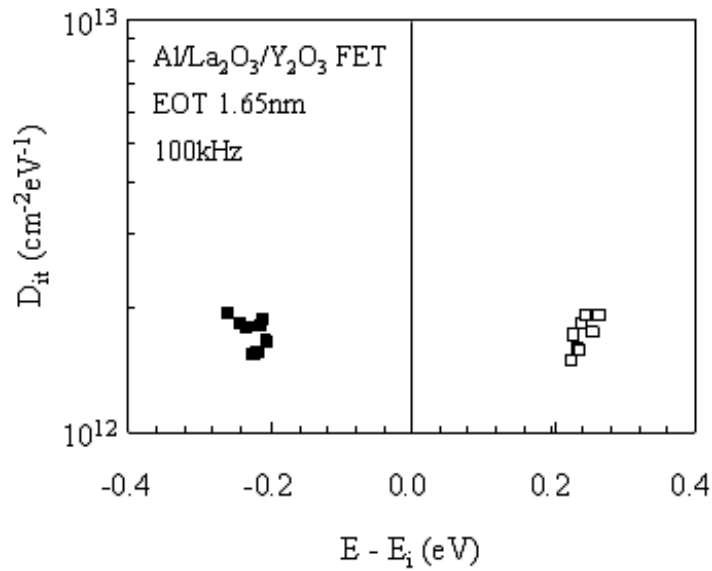


Figure 5.18: Energy distribution of interface traps as determined by rise/fall time dependence of charge pumping currents for La₂O₃/Y₂O₃ MOSFET with 600 °C PDA.

5.5 Conclusion

The n-MOSFETs with La_2O_3 , Y_2O_3 and $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ dielectrics were fabricated and evaluated. The operation of $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFET with the thinnest EOT of 1.0 nm was confirmed.

The MOSFET with high-temperature treated La_2O_3 film was found to be degraded the effective mobility. The charge pumping method revealed the increase of the interface states at high-temperature treated $\text{La}_2\text{O}_3/\text{Si}$.

Y_2O_3 MOSFETs showed better electrical properties with thinner EOT and high mobility. It was found that the high-temperature treated $\text{Y}_2\text{O}_3/\text{Si}$ interface improved the effective mobility in contrast to $\text{La}_2\text{O}_3/\text{Si}$. The charge pumping method proved the reduction of interface states with increase of PDA temperature. The effects of Y_2O_3 buffer layer was observed in $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ MOSFET. La_2O_3 MOSFET with Y_2O_3 buffer layer is capable of meeting the high-temperature process.

Chapter 6

GENERAL CONCLUSIONS

6.1 Conclusions

$\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ stack dielectric were deposited at 250 °C by electron-beam evaporation method and the electrical characteristics of n-MOS capacitors and n-MOSFETs were evaluated with emphasis on the difference between La_2O_3 monolayer devices. And chemical compositions in the dielectric films were analyzed by X-ray photoelectron spectroscopy.

From the spectroscopic ellipsometry and CV characteristics, it is found that Y_2O_3 buffer layer has the profound effects on lowering EOT values. In terms of the chemical compositions of the interfacial layer, XPS analyses revealed that the Y_2O_3 bufferlayer limits a growth of SiO_2 interfacial layer and La-silicate formations which lead to decreasing dielectric constant. Furthermore, from the JV characteristics, Y_2O_3 buffer layer is found to reduce the gate leakage currents without increasing EOT, especially for high-temperature treated films.

The results of CVs and JVs for $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ films suggest the capability of meeting a minimization of the physical thickness of a film as far as possible. n-MOSFETs with physical thickness of 3.3 nm $\text{La}_2\text{O}_3/\text{Y}_2\text{O}_3$ (EOT=1.0 nm) were fabricated and evaluated successfully. High-temperature treated $\text{Y}_2\text{O}_3/\text{Si}$ interface was found to improve the effective mobility while high-temperature treated $\text{La}_2\text{O}_3/\text{Si}$ interface degrade the mobility. The interface-states density were measured by charge pumping methods to confirm the dependence of the effective mobility on the interface-states density. Lower interface-states density at high-temperature treated $\text{Y}_2\text{O}_3/\text{Si}$ interface bears out the improvement of the effective mobility.

6.2 For Future Works

La_2O_3 must be one of the most promising dielectric for the next generation of HfO_2 gate insulator due to its high dielectric constant.

Many attempts to reduce the EOT have been made for La_2O_3 film. However, the thinner physical thickness it became, the more significant the gate leakage became. That was not so simple. The buffer layer for La_2O_3 film is essential to minimizing the EOT. Although Y_2O_3 has been investigated as a buffer layer for La_2O_3 in this study, there may be another material for buffer layer. Sc_2O_3 can be promising as well as Y_2O_3 because of its excellent features, such as a high thermal stability, large absolute lattice constant and water-resistance etc..

Study on alternative Al-gate is also essential because Al-gate induces the large flatband shift and the Al_2O_3 growth at Gate/Dielectric interface. Metal gate (except for Al) is required to achieve the further refinement of devices.

Finally, although n-channel MOSFETs were fabricated throughout the study, the evaluations for p-channel MOSFETs should be also required in terms of CMOS applications.

Acknowledgements

Firstly, I would like to acknowledge my parents who allowed me to study at graduated college and have warmly watched over me.

I would like to appreciate my principal advisor Professor Hiroshi IWAI who gave me an exact directions of the study and precious experience.

I would like to appreciate Professor Takeo HATTORI who gave me useful advices on XPS and recommended the experiment in SPring-8.

I would like to appreciate Associate Professor Kazuo TSUTSUI. His incisive question made me deeply think about the study.

I would like to appreciate reserach assistant Parhat Ahmet for his support on the experiment.

I would like to appreciate reserach assistant Kuniyuki KAKUSHIMA who fuelled my motivation to study. And his advices for my study always provided a big hint.

I would like to appreciate secretaries who cared for my surroundings.

I would like to appreciate my mentor Kunihiro MIYAUCHI who taught me how to perform experiments and gave me a lot of useful advices on the study.

I would like to appreciate Toru MATSUDA, Musashi Institute of Technology, who gave me useful advices on XPS and taught me how to analyze the data.

Finally, I would like to appreciate my colleagues Jin-Aun NG, Molina Reyes Joel, Atsushi KURIYAMA, Hendriansyah SAUDDIN, Issui AIBA, Xiang, Yusuke KUROKI, Akira FUKUYAMA, Satoshi YOSHIZAKI, TaeWan Kim, Koji NAGAIRO, Yasuhiro SHIINO, Kiichi Tachi, Masayuki Nakagawa, Song JaeYeol and Takashi SHIOZAWA. Communications and discussions with them always relaxed and motivated me. I would never forget the days I shared with you.

This work was partially supported by Semiconductor Technology Academic Research Center (STARC), and Special Coordination Funds for Promoting Sci-

ACKNOWLEDGEMENTS

ence and Technology by Ministry of Education, Culture, Sports, Science, and Technology, Japan.

Kentaro NAKAGAWA

March 2006

References

- [1] International Technology Roadmap for Semiconductors (ITRS) update 2004.
- [2] R. Chau, S. Datta, M. Doczy, J. Kavalieros and M. Metz, "Gate Dielectric Scaling for High-Performance CMOS: from SiO₂ to High-k".
- [3] L.Kang et al., "MOSFET devices with polysilicon on single-layer HfO₂ high-k dielectrics", IEDM Tech.Dig., pp.35-38(2000).
- [4] S. Ohmi et al., "High Quality Ultrathin La₂O₃ Films for High-k Gate Insulator", Proc. ESSDERC'01., pp.235-238 (2001).
- [5] A.Chin et al., "High quality La₂O₃ and Al₂O₃ gate dielectrics with equivalent oxide thickness 5-10Å", symp. on VLSI Tech., pp.16-17 (2000).
- [6] H. J. Osten et al., "Epitaxial Praseodymium Oxide: A New High-K Dielectric", IWGI Ext. Abst., pp.100-106 (2001).
- [7] J.-P. Maria et al., "High-temperature stability in lanthanum and zirconia-based gate dielectrics", J. Appl. Phys. 90, 7 (2001).
- [8] S. Jeon et al., "Excellent Electrical Characteristics of Lanthanide (Pr, Nd, Sm, Gd and Dy) Oxide and Lanthanide-doped Oxide for MOS Gate Dielectric Applications", IEDM Tech. Dig., pp. 471-474 (2001).
- [9] J. A. Ng et al., "Effects of low temperature annealing on the ultrathin La₂O₃ gate dielectric; comparison of post deposition annealing and post metallization annealing", Microelec. Eng., 80, 206-209, (2005).
- [10] S.Ohmi et al., "Characterization of La₂O₃ and Yb₂O₃ Thin Films for High-k Gate Insulator Application", J. Electronchem. Soc., 150, F13. 4240 (2003).

REFERENCES

- [11] H. Nohira et al., "Chemical and electronic structure of $\text{Lu}_2\text{O}_3/\text{Si}$ interfacial transition layer", *J. Appl. Surf. Sci.*, 216 (2003).
- [12] T. Gougousi et al., "Properties of La-silicate high-k dielectric films formed by oxidation of La on silicon", *J. Appl. Phys.*, 1691 (2003).
- [13] T. Gougousi et al., "Postdeposition reactivity of sputter-deposited high-dielectric-constant films with ambient H_2O and carbon-containing species", *J. Appl. Phys.*, 95, 3(2004).
- [14] S. Ohmi et al., "Electrical Characteristics for Lu_2O_3 Thin Films Fabricated by E-Beam Deposition Method", *J. Electrochem. Soc.*, 151 (4) 1-0 (2004).
- [15] S. Guha et al., "Atomic beam deposition of lanthanum- and yttrium-based oxide thin films for gate dielectrics", *J. Appl. Phys.*, 77, 2710 (2000).
- [16] Hand book on the Physics and Chemistry of Rare Earths edited by L. Eyring, K. A. Gschneider and L. Eyring (North-Holland, Amsterdam, 1979), Vol. 3, Chap. 27.
- [17] K. J. Hubbard and D. G. Schlom, "Thermodynamic stability of binary oxides in contact with silicon", *J. Mater. Res.*, Vol. 11, No. 11, 2757 (1996).
- [18] F. Paumier et al., "Effects of SiO_2 overlayer at initial growth stage of epitaxial Y_2O_3 film growth", *J. Crys. Growth*, 220 (2000).
- [19] J. J. Chambers et al., "Yttrium silicate formation on silicon: Effect of silicon preoxidation and nitridation of interface reaction kinetics", *Appl. Phys. Lett.* 77, 15, 2385 (2000).
- [20] G.V. Samsonov, *The Oxide Handbook*, IFI/Plenum Data Company, New York, 1982.

REFERENCES

- [21] J. F. Moulder, W.F. Stickle, P.E. Sobol and K. D. Bomben, Handbook of X-ray Photoelectron Spectroscopy (Perkin-Elmer Corporation, Eden Prairie, MN, 1992).
- [22] D. Niu et al., "Water absorption and interface reactivity of yttrium oxide gate dielectrics on silicon", Appl. Phys. Lett, 80, 19, 3575 (2002).
- [23] M. Copel et al., "Characterization of silicate/Si(001) interfaces", Appl.Phys.Lett., 81, 22, 4227 (2002).
- [24] Y. Kim et al., "Space-charge-limited currents in La_2O_3 thin films deposited by e-beam evaporation after low temperature dry-nitrogen annealing", J. Appl. Phys., in press.
- [25] Y. Kim et al., "Electrical properties of vacuum annealed La_2O_3 thin films grown by e-beam evaporation", Microelectron J. 2005; 36(1):41-9.
- [26] E. Miranda et al., "Modeling of the tunneling current in sub-5nm La_2O_3 gate oxides", IEEE Electron Dev. Lett., in press.
- [27] E. Miranda et al., "Effects of high-field electrical stress on the conduction properties of ultra-thin La_2O_3 film", Appl. Phys. Lett., in press.
- [28] J. J. Chambers et al., "Effects of surface pretreatments on interface structure during formation of ultra-thin yttrium silicate dielectric films on silicon".
- [29] A. Kuriyama, "Effect of Post Metallization Annealing for La_2O_3 Gate Thin Film", Master thesis.
- [30] Y. Uwamino, T. Ishizuka, and H. Yamatera, J. Electron Spectrosc. Relat. Phenom. 34, 67 (1984).
- [31] H. Ono and T. Katsumata, Appl. Phys. Lett. 78, 1832 (2001).

REFERENCES

- [32] R. D. Shannon, R.D. Shannon, *Acta Crystallogr.* , A32, 751 (1976).
- [33] G. Groeseneken et al. *Trans. Electr. Dev.* 31, 42 (1984).