Master Thesis

Novel Gate Stack and Process Optimization for La_2O_3-MOSFET

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Chapter 1

Introduction

1.1 Background of This study

In recent years, our lives are becoming affluent with the global promotion of Information Technology (IT) as represented by computers, internets and cell-phones. As it is now, these are fundamental part of everyday life. These information equipments are realized by astonishing progress in silicon LSI (Large-Scale Integration) technology. The performance of silicon LSI depends on the capability of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) which is core part of LSI systems. In order to obtain high performance devises, it is necessary to miniaturize the MOSFET with the scaling method. The scaling method is based on reducing the device dimension in both lateral and vertical. The consensus scenario of how the device parameters are scaled for the next technology is provided in the International Technology Roadmap for Semiconductor (ITRS). A simple description of miniaturization with scaling factor of κ is shown in Figure 1.1 and Table 1.1. To gain κ times of the device performance, the physical device dimensions are reduced by κ times, while the electrical parameters are increased by κ times.

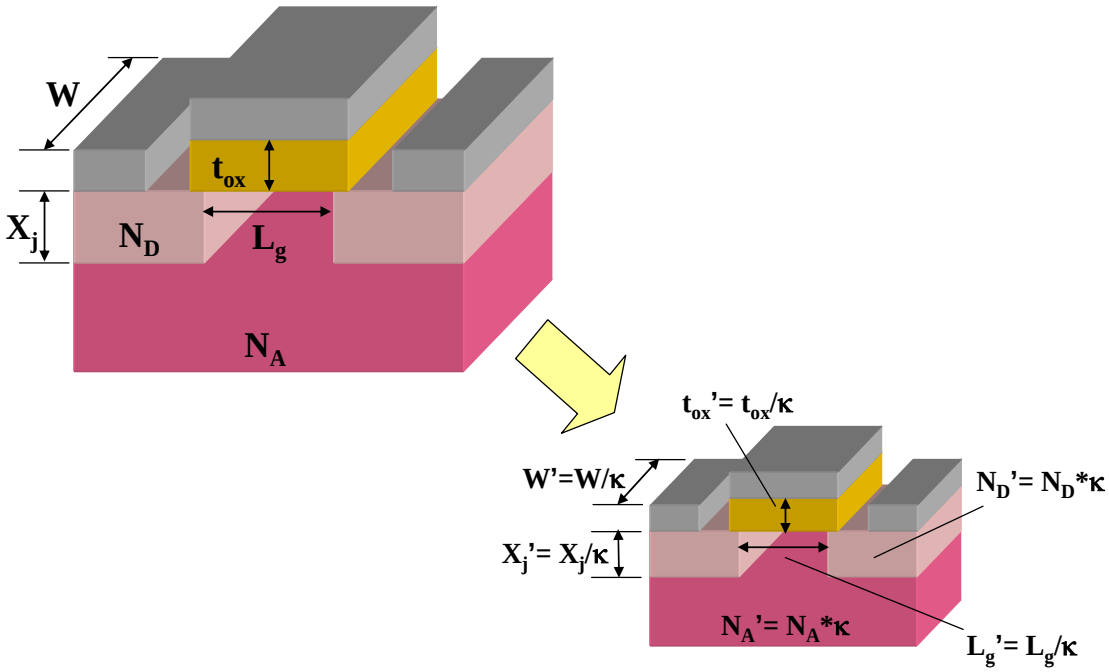


Figure 1.1 : Scaling Method.

Parameter	Inisial	Scaled
Channel Length	L	L/κ
Channel Width	W	W/κ
Total Device Area	A	A/κ^2
Gate Oxide Thickness	t_{ox}	t_{ox}/κ
Gate Capacitance	C_{ox}	$C_{ox}*\kappa$
Junction Depth	X_j	X_j/κ
Power Supply Voltage	V_{dd}	V_{dd}/κ
Threshold Voltage	V_{th}	V_{th}/κ
Doping Concentration	N_A	$N_A*\kappa$
	N_D	$N_D*\kappa$

Table 1.1 : Scaling of MOSFET by the scaling factor κ.

1.2 Limits of SiO_2

As is well known, Silicon dioxide film (SiO_2) is the most common materials as gate insulator film. However, a big hurdle is confronted to miniaturize the element size as in the past with keeping high performance and high integration.

From ITRS 2004 up date (Table 1.2), Equivalent Oxide Thickness (EOT) will rise to the below 1nm level in near future. On the other hand, the direct-tunneling leakage current is too increasing to be neglected as shown in Figure 1.2. Therefore, SiO_2 gate insulator film is to be replaced with an alternative material, which can be suppressed leakage current.

Year of Production	2005	2007	2010	2014	2018
Physical Gate Length (nm)	32	25	18	11	7
EOT (nm)	1.1	0.9	0.7	0.6	0.5
Gate Leakage Current Density (A/cm^2)	$5.20*10^2$	$9.30*10^2$	$1.90*10^3$	$9.09*10^3$	$2.40*10^4$
Power Supply Voltage (V)	1.1	1.1	1.0	0.9	0.7

Table 1.2 : ITRS 2004 up date.

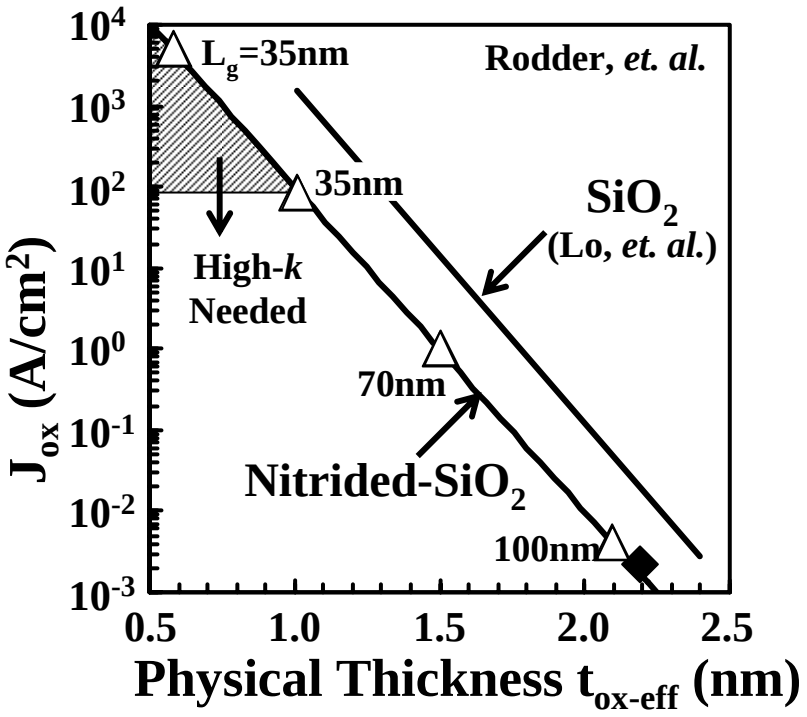


Figure 1.2 : Relations between gate leakage current and physical thickness of SiO_2 film.

1.3 Requirements of high-k materials

To overcome this problem, high-k (high dielectric constant) materials have been attracted much attention. The key guidelines for selecting an alternative gate dielectric material are high dielectric constant, large band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability. Among them, high dielectric constant and large band gap are the minimum required characteristics to suppress the gate leakage current. The direct-tunneling leakage current (J_{DT}) flow through a gate insulator film is determined by the tunneling probability of carrier. The tunneling probability of carrier (D_{DT}) is shown in below equation where physical thickness of insulator (d), electron effective mass in the gate insulator film (m^*) and barrier height of insulator (ϕ_b).

$$J_{DT} \propto D_{DT} \propto \exp\left\{-\frac{4\pi d\left(2m^{*}\phi_{b}\right)^{\frac{1}{2}}}{h}\right\}$$

Relationship between physical thickness of SiO_2 (d_{EOT}) and physical thickness of high-k gate insulator (d) obtained by the same gate capacitance value (C) is shown in below equation where dielectric constant of SiO_2 (ε_{ox}) and high-k gate insulator ($\varepsilon_{high\text{-}k}$).

$$C = \frac{\varepsilon_{high-k}}{d} = \frac{\varepsilon_{ox}}{d_{EOT}}$$

$$d = \frac{\varepsilon_{ox}}{\varepsilon_{high-k}} d_{EOT}$$

Therefore, the gate leakage current can be suppressed by using high-k materials, which means that the physical thickness of high-k films can be thicken without changing EOT. In addition, the gate leakage current can also be suppressed by using large band gap materials.

The possible candidate of several metal oxides system for the use of gate dielectric materials is shown in white spaces of Table 1.3.

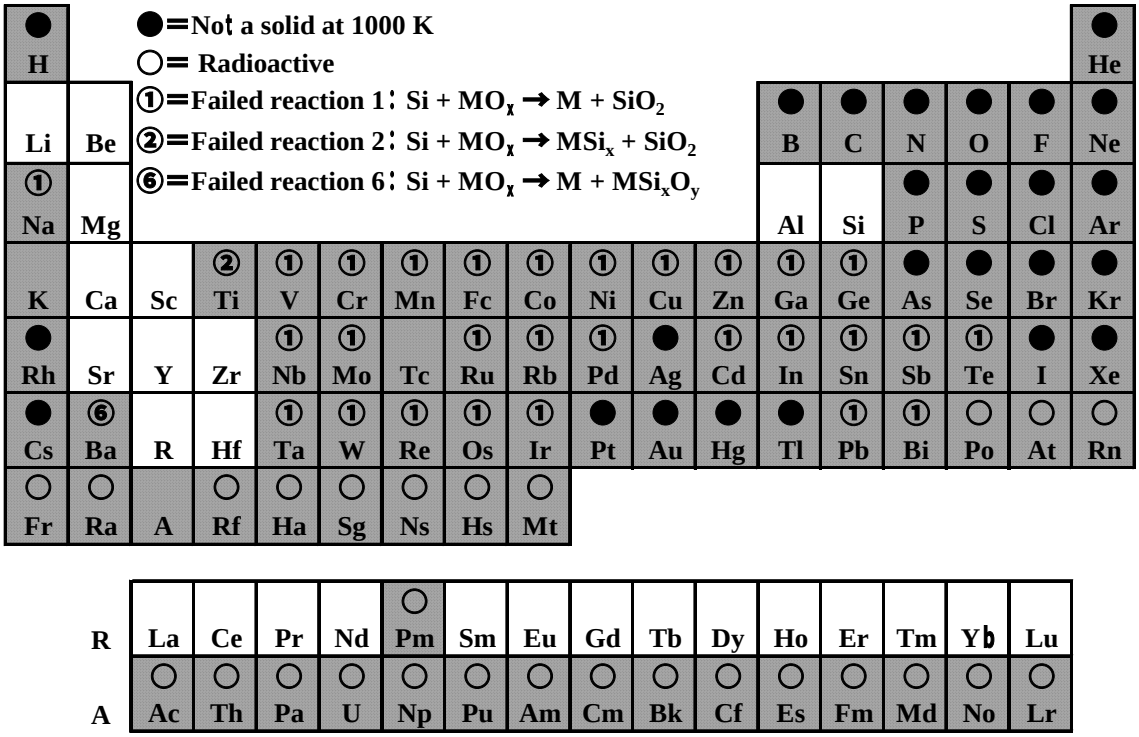


Table 1.3 : Candidate of metal oxides that has possibility to be used as high-k gate insulator.

Among the candidate of high-k materials, Hf-based materials are the most promising candidate of them. As shown in Figure 1.3, many papers on high-k materials are submitted in the primary conferences up to 2002. However, from 2003 to now, the candidate of high-k materials have narrowed down to Hf-based materials. Therefore, Hf oxides (HfO_2) and Hf-based silicates or nitrides (HfSiON), with dielectric constants of 25 and 10 to 15 respectively, are among the promising materials for the 65 or 45-nm-technology nodes.

Usually, when the EOT becomes small, the effective carrier mobility tends to decrease due to scattering in the high-k layer or at the interface between the high-k layer and the substrate. It has reported that Hf-based films have reduced scattering when a SiO_2-based interfacial layer of 0.5 to 0.7 nm is inserted, however, this attempt increases

the EOT.

Consequently, in this work, Lanthanum Oxide (La_2O_3), one of the rare earth oxides, has been tried as a gate insulator, because it has a relatively high dielectric constant of 27, which is slightly higher than that of HfO_2 and a high band offset of 2.3 eV from the conduction band of silicon to La_2O_3 has the advantage of further reducing the leakage current.

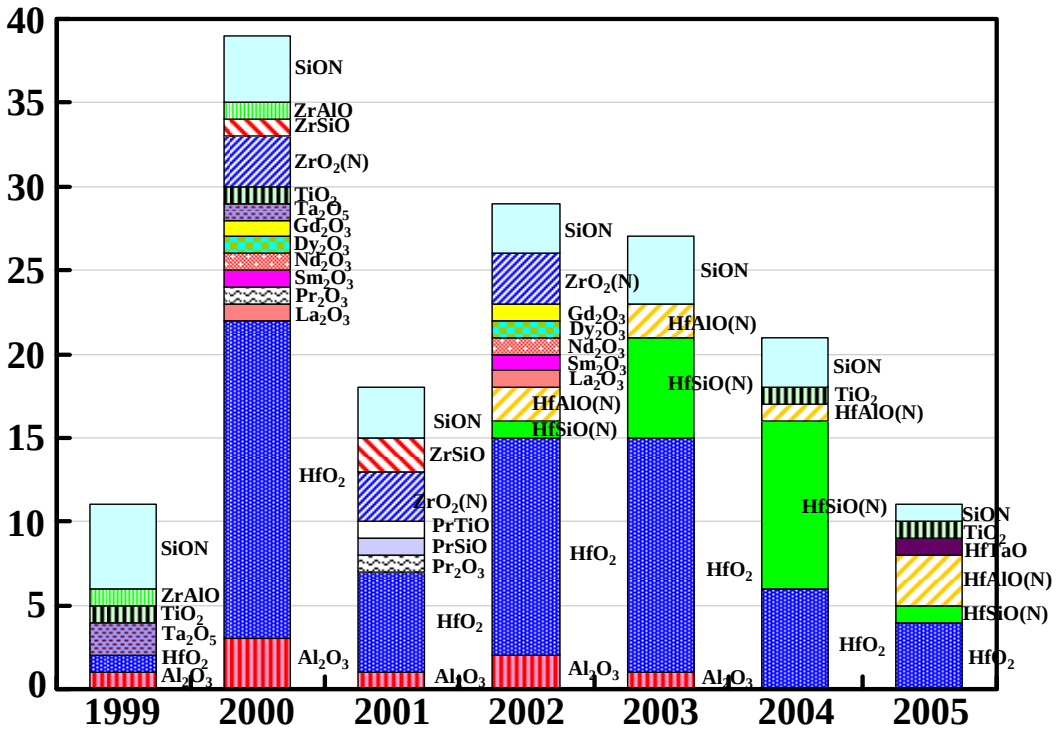


Figure 1.3 : Reported High-k materials.

1.4 Properties of La_2O_3

To perform a low EOT, high-k gate dielectrics materials must have high enough dielectric constant. However, material with very high dielectric constant tends to have narrower band gap that allows higher Schottky conduction currents and tunneling currents. Figure 1.4 shows band gap energy of several metal oxide and silicate materials as a function of dielectric constants. La_2O_3 gives high dielectric constant of 27 and wide band gap of 5.6 eV that is suitable for the use of gate dielectrics.

To inhibit a low leakage current due to Schottky emission conduction mechanism, the high-κ gate dielectric materials must have wide band gap and high barrier of more than 1 eV for both electrons and holes. Figure 1.5 predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy. La_2O_3 has a good symmetrical band barrier of more than 2 eV for both electrons and holes that is compatible for CMOS devices.

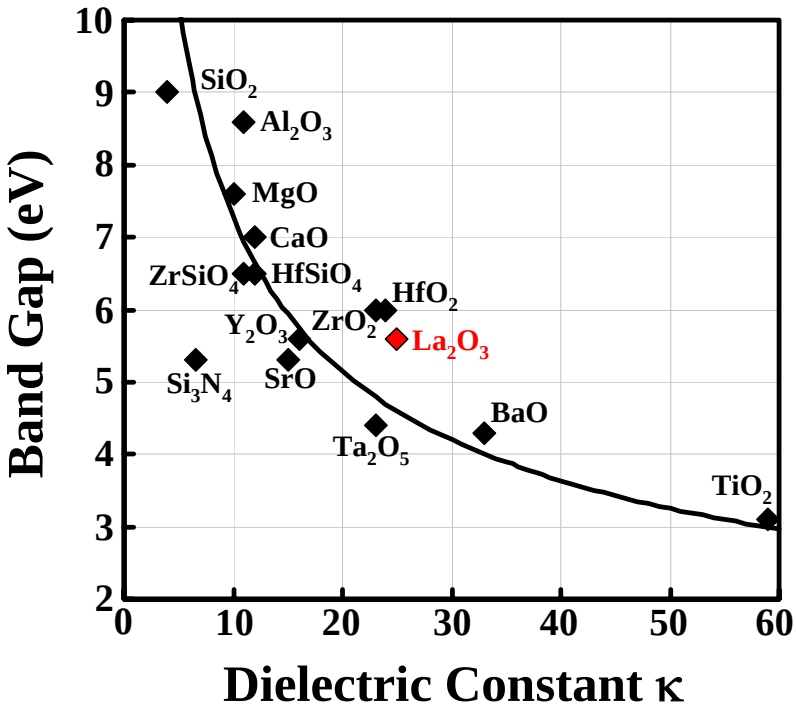


Figure 1.4 : Band gap energy of several metal oxide and silicate materials as a function of dielectric constant.

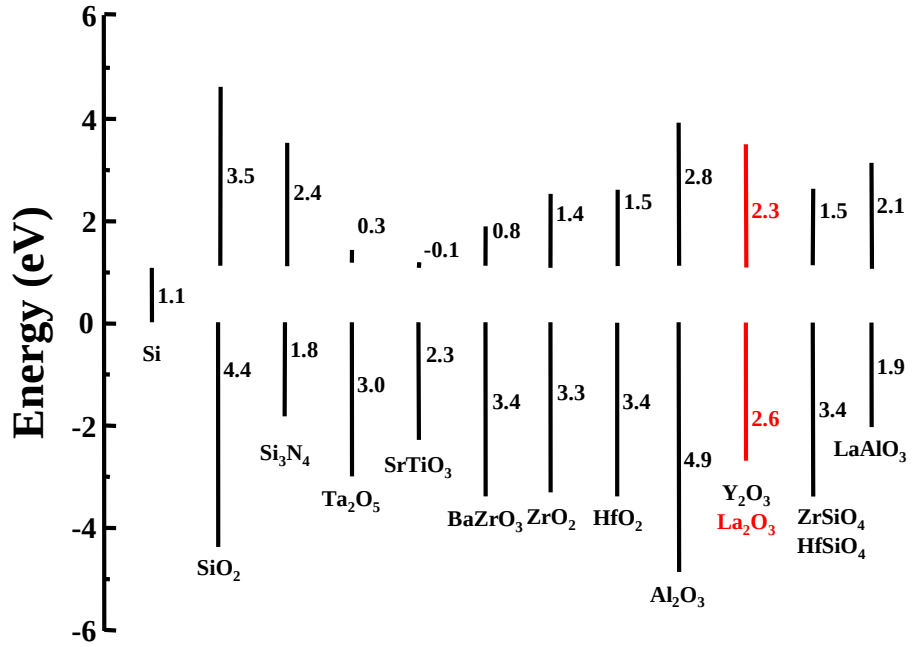


Figure 1.5 : Predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy.

Previously, excellent results on several high-k gate dielectrics materials have been reported. Figure 1.6 shows reported leakage current density of various high-k gate materials as a function of EOT. From Figure 1.6, the superiority of La_2O_3 is obvious, low EOT with low leakage current can be achieved with La_2O_3.

Finally, La_2O_3 is considered to be the most promising gate dielectric material for the next generation gate dielectric technology. La_2O_3 material shows good physical properties, high dielectric constant of 27, wide band gap of 5.6 eV, symmetrical band offset for electrons and holes of more than 2 eV, and good thermal stability in contact with silicon. In this study, the electrical properties of MOSFET with La_2O_3 gate dielectrics will be evaluated.

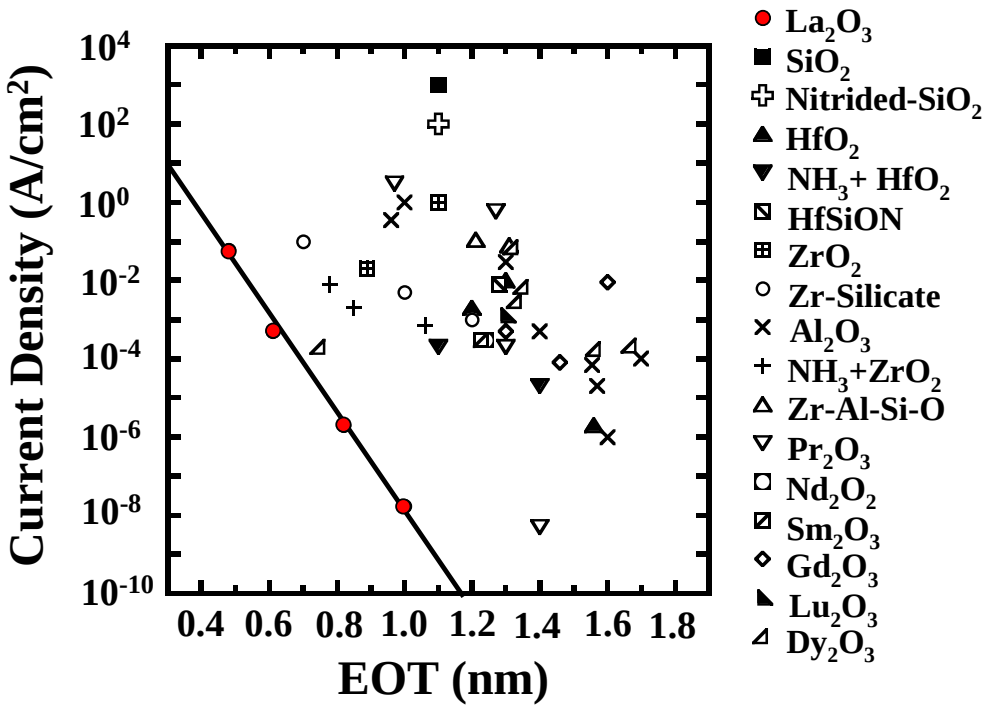


Figure 1.6 : Reported leakage current density of various high-k gate materials as a function of EOT.

1.5 Purpose of This Study

One of the serious problems for the high-k gate insulator is mobility degradation. The mobility is the most important factor to achieve the high performance MOSFET. However, using high-k materials as gate insulator, mobility degradation become more and more prominent as compared to the SiO_2 film, which is due to the high amount of fixed charge, interface trapped charge and so on (Figure1.7). As shown in Figure 1.8, these defects become center of the Coulomb Scattering to degrade mobility.

Thus, in this work, we mainly discuss the mobility and study on process optimization for La_2O_3 nMOSFETs to improve the mobility.

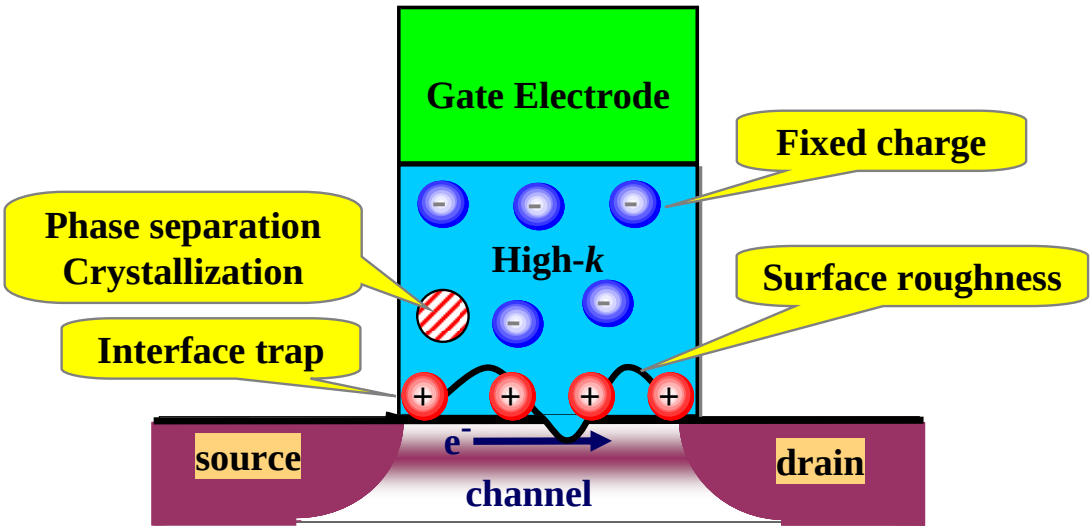


Figure 1.7 : The factor of mobility degradation.

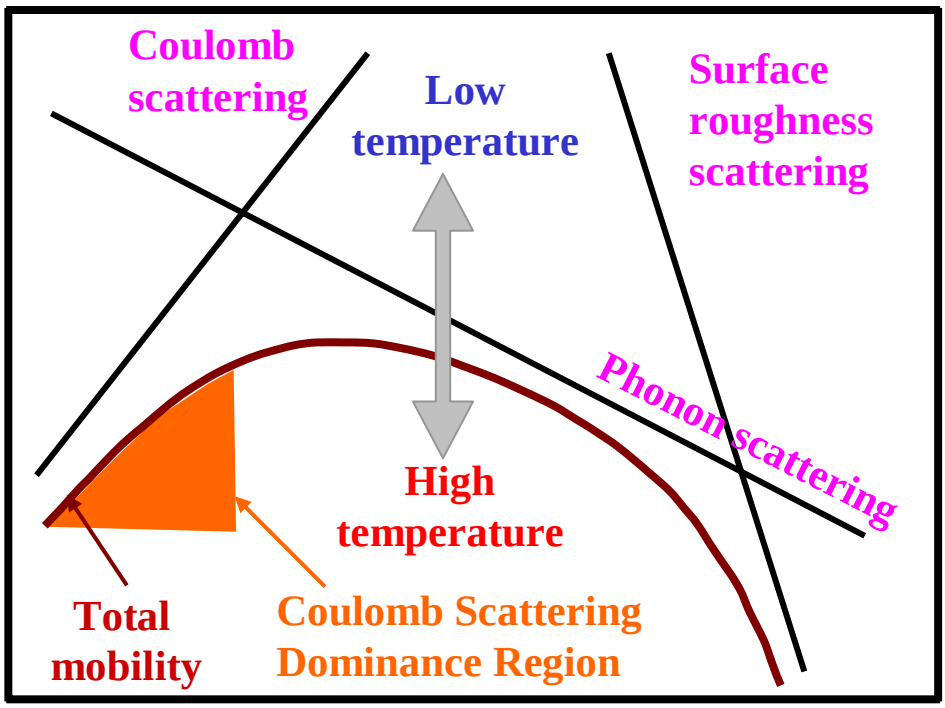


Figure 1.8 : Metric for Mobility Progress.

Chapter 2

Fabrication and Characterization Methods

In this chapter, we describe the details of procedures, instrumentations, appliances, and tools for fabrications and characterizations of La_2O_3 Metal-Oxide-Substrate Capacitor (MOS Capacitor) and n-channel Metal-Oxide-Semiconductor Field Effect Transistor (nMOSFET).

2.1 Experimental Procedure

2.1.1 Fabrication Procedure for MOS Capacitor

The fabrication procedure for MOS Capacitor is shown in Figure 2.1. La_2O_3 thin films were deposited on n-type silicon (100) substrate by Electron-Beam Evaporation. at substrate temperature 250^oC followed by H_2SO_4/H_2O_2 mixture (SPM) cleaning and HF-dip processes. Then, upper electrode and back side electrode were formed by Vacuum Evaporation Method or RF Magnetron Sputtering Method. In this experiment, we performed two type of the annealing method using Rapid Thermal Annealing (RTA) method. One is the Post Deposition Annealing (PDA) and the other is the Post Metallization Annealing (PMA). Detailed explanation of each process and experimental equipment will be described in next section.

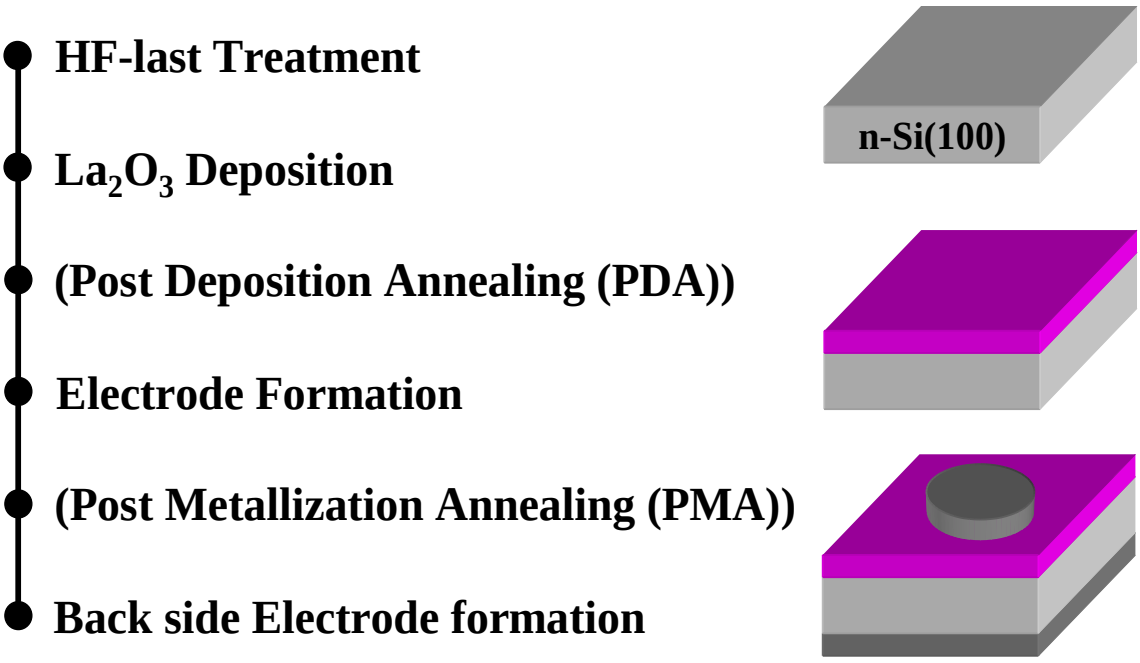


Figure 2.1 : The fabrication procedure for MOSCAP.

2.1.2 Fabrication Procedure for nMOSFET

The fabrication procedure for nMOSFET is shown in Figure 2.2 and the cross-sectional description in La_2O_3 nMOSFET fabrication is shown in Figure 2.3. nMOSFET fabrication was started from S/D implanted Si(100) substrate. La_2O_3 thin film was deposited by Electron-Beam Evaporation followed by substrate cleaning. After metal gate formation, the gate area was defined with photolithography followed by metal gate etching. The Al-Pad area was formed with lift-off process under acetone solution and Al back side electrode were formed afterwards.

- HF-last Treatment
- La_2O_3 Deposition
- (PDA)
- Gate Electrode Formation
- (PMA)
- Gate Patterning
- Gate Etching
- S/D Pad Patterning
- Al Pad Deposition
- Pad Formation with Lift-off
- Back side Electrode formation

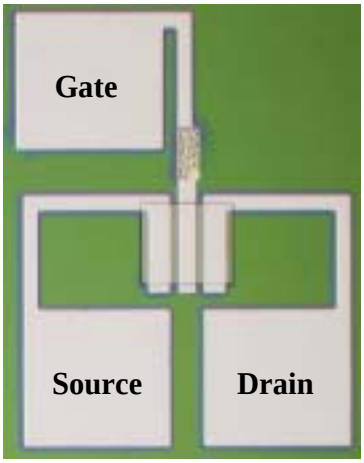


Figure 2.2 : The fabrication procedure for nMOSFET.

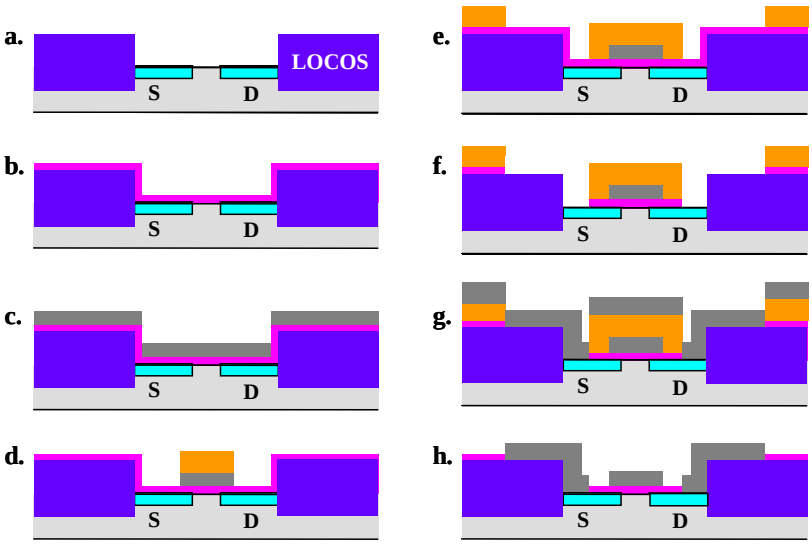


Figure 2.3 : Cross section description in La_2O_3 nMOSFET fabrication procedure.

2.2 Fabrication Methods

2.2.1 Wet Cleaning Method of Silicon Substrate

Prior to deposit of high-k gate thin films for LSI fabrication process, the ultra-pure surface of a bare Si-substrate should be chemically cleaned to remove particles contamination, such as metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. It is considered that this substrate cleaning process is very important to realize desirable device operation and its reproducibility.

In full fabrication processes as well as substrate cleaning, DI (de-ionized) water is one of the most important because DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. Theoretical resistively of pure water at 25ºC is 18.3 MΩ·cm. The resistively value of ultra-pure water (UPW) used in this study achieve more than 18.2 MΩ·cm and have fewer than 1.2 colony of bacteria per milliliter and no particle larger than 0.25 um.

In this study, the method of substrate cleaning process was used a typical processing using hydrofluoric acid, which is usually called RCA cleaning method, was proposed by W. Kern et al. But some steps were reduced. The steps were shown in Fig.2.4. Firstly, a cleaning steps in solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2 = 1:4, called by SPM) performed to remove any organic material and metallic impurities after UPW cleaning. Secondly, the step in a solution of dilated hydrofluoric acid (HF:H_2O=1:100) was performed to remove chemically and native oxides which might have been formed on Si surface. Final step was dipped in UPW

because hydrogen-terminated surface.

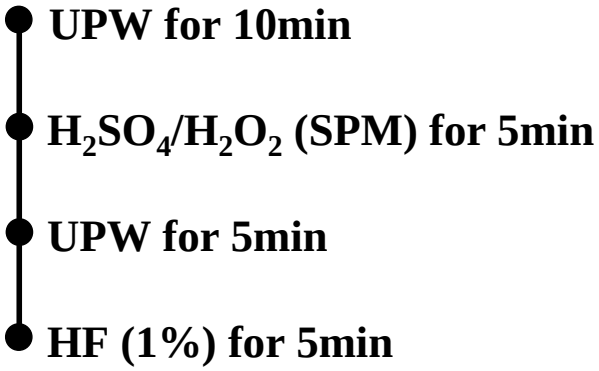


Figure 2.4 : Si Surface cleaning process.

2.2.2 Electron-Beam Evaporation Method

Electron-Beam Evaporation method using MBD equipment is employed for depositing La_2O_3 in this study.

Figure 2.5 shows the schematic drawings of the equipment and inside of its growth chamber. Air in the loading chamber is removed to degree of a vacuum of 10^{-8} Torr by a turbo molecular pump connected to a rotary pump. Vacuum in the growth chamber reaches as high as 10^{-10} Torr by the removal of air with an ion pump and the introduction of liquid N_2 trap.

In the growth chamber, sintered La_2O_3 target, which is evaporation source, is irradiated with electron beam accelerated by -5 kV. The target is heated up and La_2O_3 molecules are evaporated. Then ultra thin La_2O_3 film is deposited on the Si-substrate. The degree of a vacuum is from 10^{-7} to 10^{-8} Torr while deposition. The substrate rotates 10 times per 1 minute horizontally to uniform the film thickness. Physical thickness of the film is monitored with a film thickness counter using crystal oscillator. The temperature of the substrate is controlled by a substrate heater and is measured by a thermocouple.

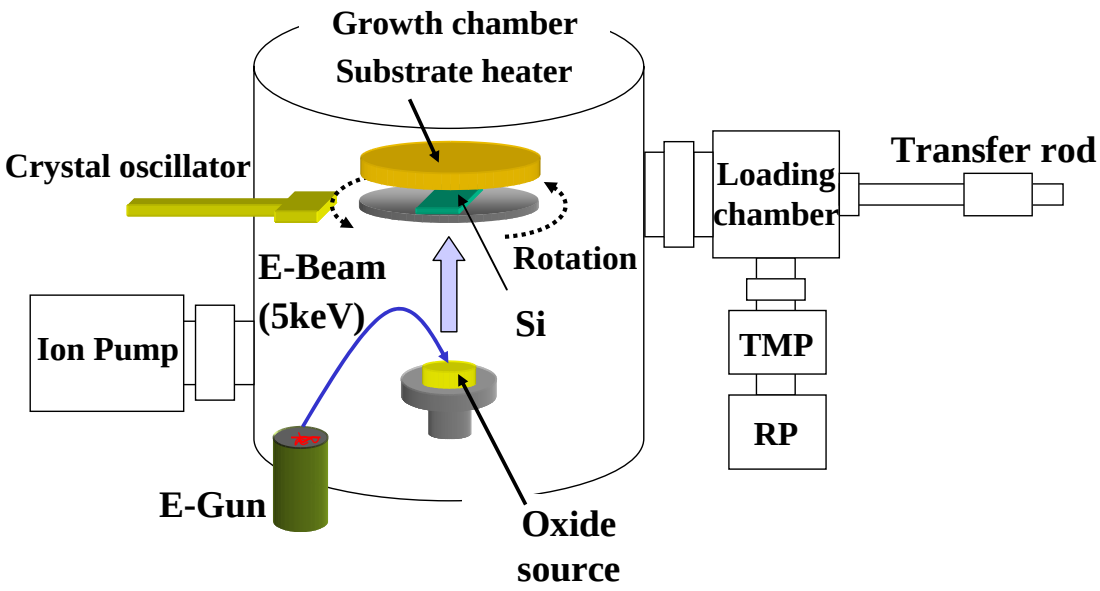


Figure 2.5 : Schematic drawing of e-beam evaporation system.

2.2.3 Rapid Thermal Annealing (RTA) Method

Thermal processes are often used for defects recovery or molecular introduction to dielectric thin films, for lattice recovery or impurity electrical activation of doped or ion implanted wafers. In this experiment, Rapid Thermal Processing MILA-3000 from ULVAC is used for annealing deposited La_2O_3 thin films. Figure 2.6 illustrated the schematic drawing for MILA-3000. High purity gas ambience can be obtained by pumping out and purging with the in use ambient gas. This RTP system is heated-up by infrared lamp heating furnace and cooled-down by flowing water radiator. The furnace temperature is of the range from room temperature to around 1200^{o}C with ramp-up of less than 50^{o}C/sec and much slower on cooling-down. The available of ambient gases are N_2 and O_2 at atmospheric pressure by keeping the flowing gas at the rate of 1 lt./min.

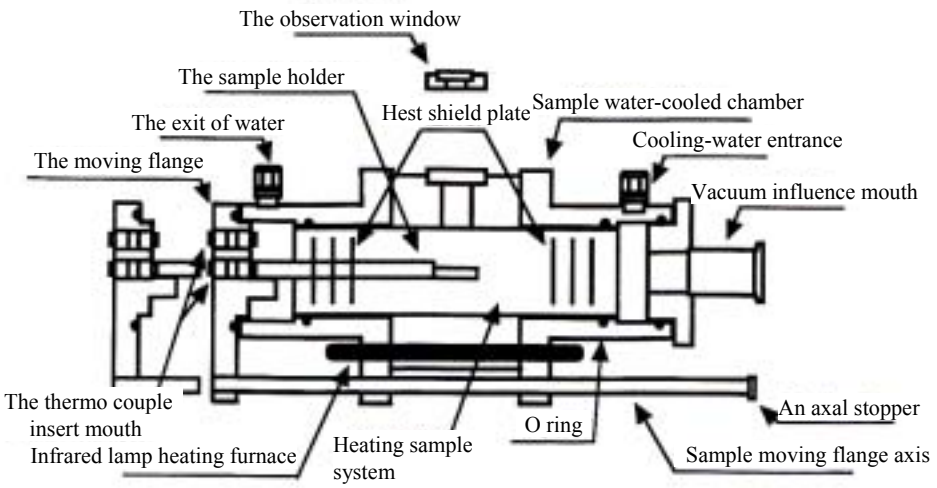


Figure 2.6 : Schematic drawing for Rapid Thermal Annealing (RTA) MILA-3000.

2.2.4 Vacuum Evaporation Method

All of Al metals in this work were obtained from deposition with bell jar vacuum thermal evaporation. Figure 2.7 illustrates a schematic drawing for vacuum thermal evaporation system. The system is utilized with Turbo Molecular Pump (TMP) to pump down to several 10^{-5} Torr. In case of MOS capacitor fabrication, metal shadow mask with circle opening of 200 μm diameters was used. Filament is made of tungsten, was used for heating the Al source up to its vapor temperature. Both filaments and Al sources are made of Nilaco, inc. with material purity of 99.999%.

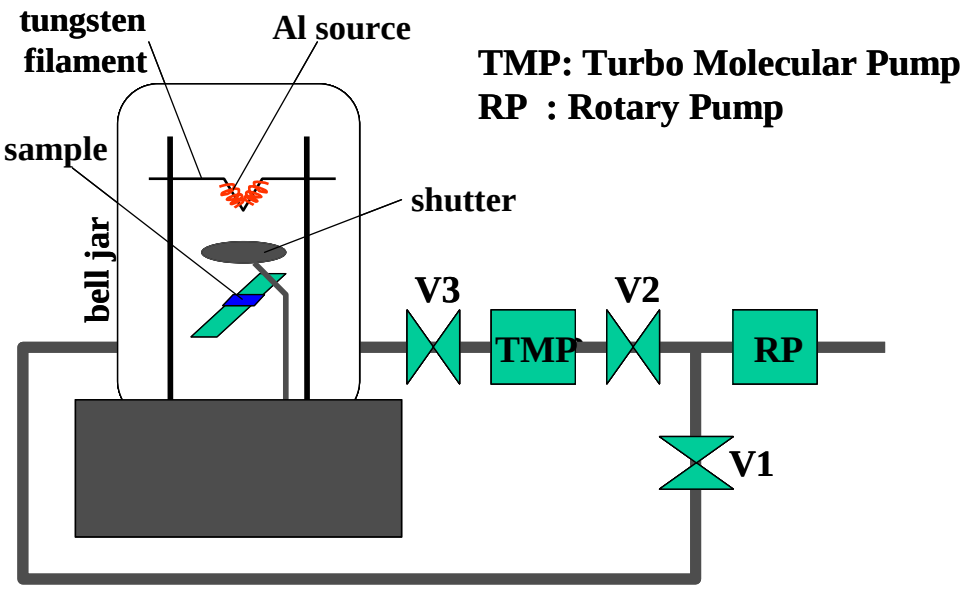


Figure 2.7 : Schematic drawing for vacuum thermal evaporation system.

2.2.5 RF Magnetron Sputtering Method

Some of a gate electrode material was deposited by RF magnetron sputtering method. Figure 2.8 illustrates a schematic drawing for RF magnetron sputtering system. This equipment deposits metal film by means of physical sputtering that occurs in a magnetically-confined RF plasma discharge of an inert Ar gas. Before the introduction of gases (Ar, Kr, N_2 or O_2), the process chamber was evacuated to degree of 10^{-5} Pa by a turbo molecular pump connected to a rotary pump and a liquid N_2 trap. The flow rate of gases is (7sccm) controlled by mass flow. The RF power supply system has auto impedance matching equipment and its capability of power supply is ~ 500W.

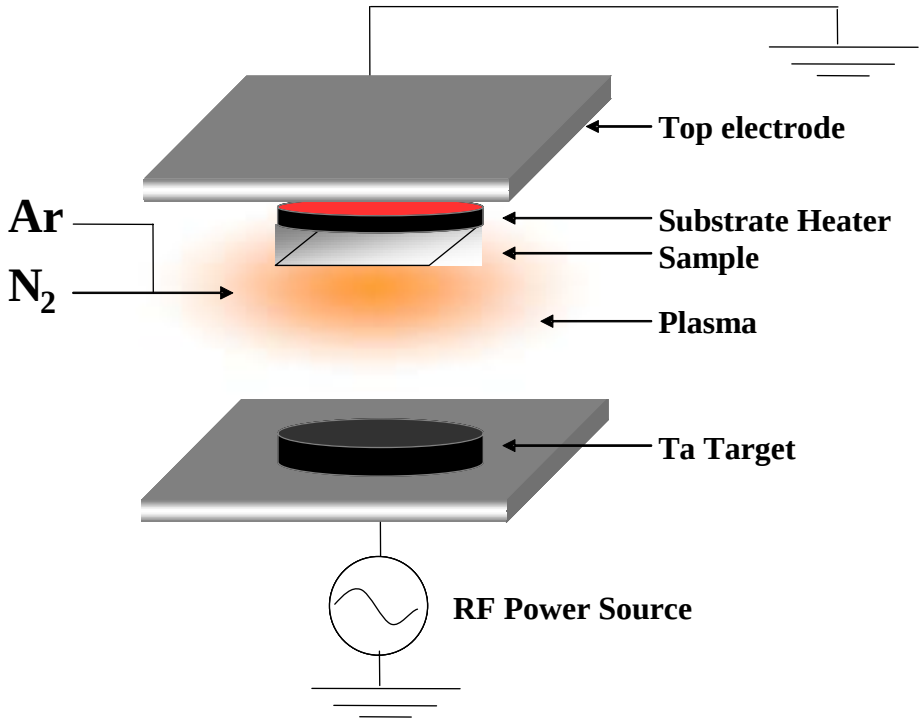


Figure 2.8 : Schematic drawing for RF magnetron sputtering system.

2.2.6 Mask Aligner

The spin-coated photoresist was exposed through the mask with high-intensity ultraviolet light (405 nm). In this study, the exposure process was performed by contact-type mask aligner, MJB3 (Karl Suss Co. Ltd.). The exposure time was set to 12 sec. The photo-resist was developed using the specified developer (NMD-3, Tokyo Ohka Co. Ltd.).

2.3 Measurement Methods

2.3.1 Spectroscopic Ellipsometry

Spectroscopic Ellipsometry is used predominantly to measure the thickness of thin dielectric films on highly absorbing substrates but can also be used to determine the optical constants of films or substrates. Figure 2.9 shows the plane-polarized light incident on a plane surface. The incident polarized light can be resolved into a component p, parallel to the plane of incidence and a component s perpendicular to the plane of incidence. The light propagates as a fluctuation in electric and magnetic fields at right angles to the direction of propagation. The reflection coefficients

$$R_p = \frac{E_p(reflected)}{E_p(incident)}$$

$$R_s = \frac{E_s(reflected)}{E_s(incident)}$$

are not separately measurable. However, the complex reflection ratio ρ defined in terms of the reflection coefficients R_p and R_s or ellipsometric angles ψ and Δ

$$\rho = \frac{R_p}{R_s} = \tan(\psi)e^{j\Delta}$$

is measurable. Then, ψ and Δ are called ellipso parameter.

For the air(n_0)-thin film(n_1)-substrate(n_2-jk_2) substrate system, where n_x is the index of refraction and k_x the extinction coefficient. In case of Si substrate, n_2 and k_2 are known, then n_1 and film thickness may be calculated from the result of ψ and Δ measurement.

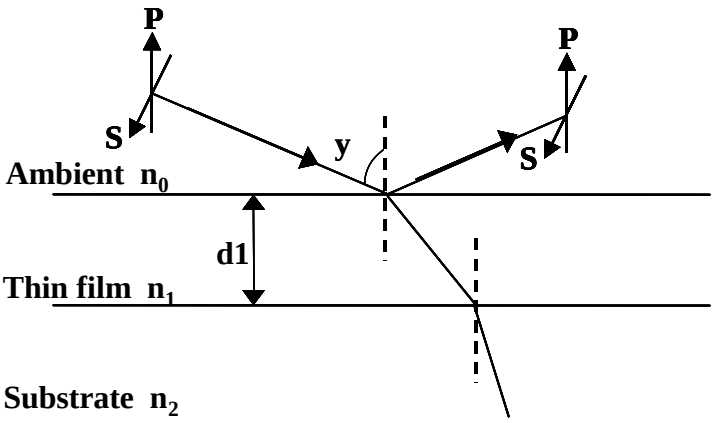


Figure 2.9 : Principle of Ellipsometry.

2.3.2 X-ray Photoelectron Spectroscopy (XPS)

Chemical state of a few nm surface layers is analyzed by X-ray Photoelectron Spectroscopy (XPS) as shown in Fig.2.10. An electron is emitted by the photoelectric effect when homogeneous light is applied material. The measuring method of electron energy and intensity distribution is called XPS method.

$$E_{kin}{}^{v} = h\nu - E_b - \phi$$

where $E_{kin}{}^{v}$, $h\nu$, E_b and ϕ are kinetic energy of liberated photoelectron, incident X-ray energy, binding energy of emitted electron for sample and work function for sample. If hν is constant, binding energy can be obtained by measuring the kinetic energy of emitted electron. Identification of element is easily possible by measuring $E_{kin}{}^{v}$ because binding energy of each electron orbit is different. On the other hand, binding energy of same orbit of same element is changed a little by an atomic surrounding state and environment. State analysis of element is possible by measuring this change variation called chemical shift.

Additionally, mean free path of electron is not so long because of scattering and absorption process of electron in solid. Therefore, since XPS method can observe only the surface of nm order, it is suitable for thin film evaluation.

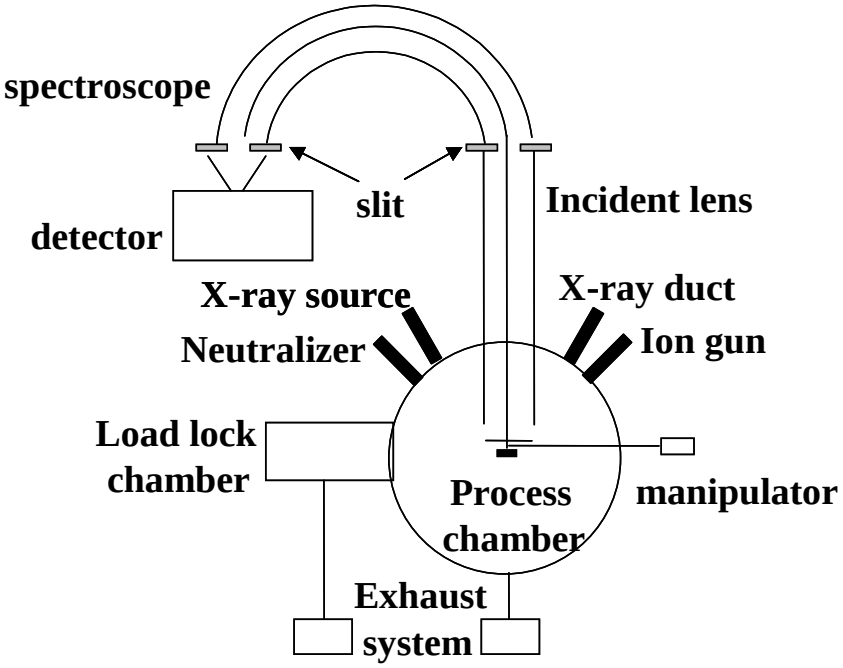


Figure 2.10 : Schematic diagram of XPS system.

2.3.3 Transmission Electron Microscopy (TEM)

Cross section of the sample is observed by Transmission Electron Microscope (TEM). TEM is microscopic equipment for observing internal structure of a thin sample by radiating electron beam to it. Figure 2.11 shows schematic cross section of a TEM. The principle of TEM is similar to that of optical microscope. In case of TEM, observation is made in a high vacuum, and an electron gun and electromagnetic lenses are used in place of a light source and optical lenses, respectively. Because wavelength of electron beam is less than that of visible ray, resolution of TEM is higher than that of optical microscope. The thickness of sample must be not greater than 0.1 μm so as to transmit electron beam. In some case, Focused Ion Beam (FIB) equipment is used for the lamination of the sample.

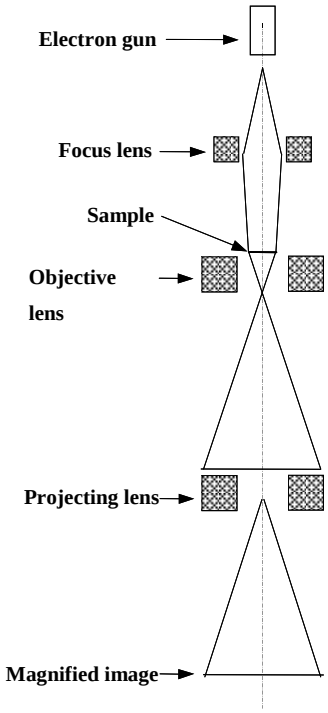


Figure 2.11 : Schematic cross section of TEM.

2.4 Characterization Method

2.4.1 Characterization of MOS Capacitor

2.4.1.1 C-V (Capacitance-Voltage) Measurement

Figure 2.12 shows the ideal of C-V characteristic of p-type MOS diode. Here, "ideal" MOS diode means that there is no interface-trapped charge (Q_{it}), fixed charge (Q_f), oxide trap charge (Q_{ot}) and mobile ion charge (Q_m). The total capacitance (C) of MOS diode equals the oxide capacitance (C_0) which is accumulated and the silicon capacitance (C_{Si}) connected in series as follows,

$$C = \frac{C_0 C_{Si}}{C_0 + C_{Si}} \quad \text{F/cm}^2.$$

And we obtain

$$\frac{C}{C_0} = \frac{1}{\sqrt{1 + \frac{2\varepsilon_{ox}{}^2 V}{qNA\varepsilon_{si}d^2}}},$$

where we have written out C_{Si} explicitly. This equation indicates that the capacitance decreases with increase of the gate voltage.

If applied voltage is negative, depletion layer is not generated but hole is accumulated in surface of silicon. As a result, the total capacitance equals approximately the oxide capacitance (ε_{ox}/d). Beyond strong inversion, even if the voltage increases more than that, the thickness of depletion layer doesn't increase any longer. The gate voltage is called threshold voltage (V_T) in this condition as follows.

$$V_T = \frac{\sqrt{2\varepsilon_{Si} q N_A (2\psi_B)}}{C_0} + 2\psi_B$$

Moreover, capacitance is as follows

$$C_{\min} = \frac{\varepsilon_{ox}}{d + (\varepsilon_{ox} / \varepsilon_{Si}) W_m}.$$

In conventional MOS diode, however, the difference of work function between metal and oxide (ϕ_{ms}) is not zero and there are varies space charges, such as Q_{it}, Q_f, Q_{ot} and Q_m, in oxide and interface of oxide-semiconductor, therefore those affect characteristics of ideal MOS diode. As a result, flat band voltage (V_{FB}) is shifted from ideal that as follows,

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_0}.$$

And C-V carve is parallel shifted as shown in Figure 2.12 (b) because ϕ_s, Q_m, Q_{ot} is not zero. And in addition to that, when there are much Q_{it}, that is changed by surface potential. Therefore, curve (c) as shown in Figure 2.12 is shifted and bended by Q_{it} value.

CET (Capacitance-equivalent-thickness) in other words, T_{ox} electrical equivalent means the thickness of equivalent SiO_2, can be calculated from accumulated capacitance of C-V characteristic as follows,

$$CET = \varepsilon_0 \varepsilon_{Si} \frac{S}{C_0}$$

where ε_0, ε_{Si} and S are permittivity of vacuum, dielectric constant of SiO_2 and area of a capacitor.

In this study, HP4284A (Hewlett-Packard Co. Ltd.) is used for measurement C-V characteristics. The range of measurement frequency is from 10k to 1MHz.

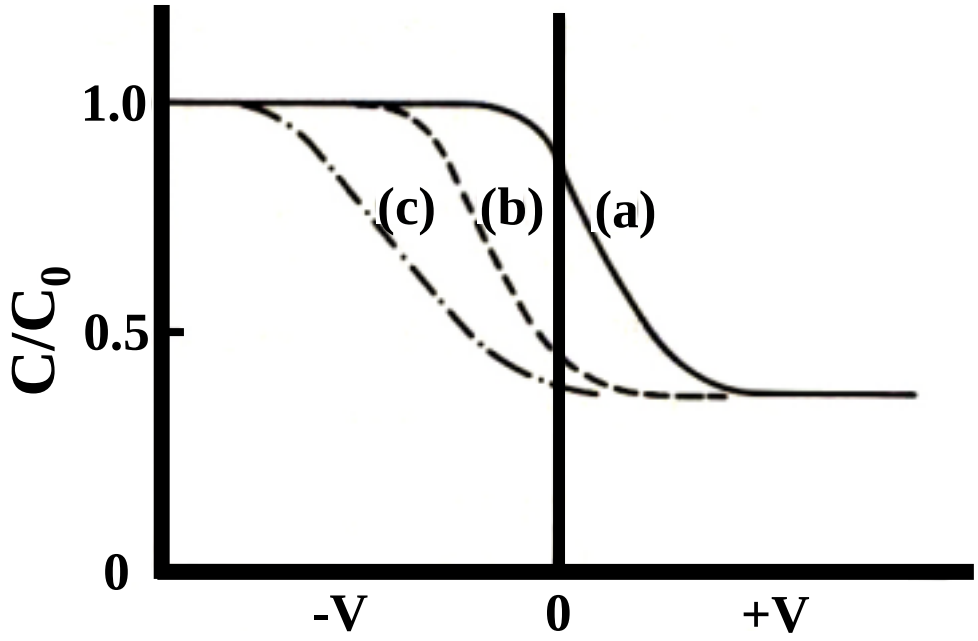


Figure 2.12 : The ideal of C-V characteristics of p-type MOS diode.

2.4.1.2 J-V (Leakage Current Density-Voltage) Measurement

It is important to suppress the leakage current of the gate dielectric film as small as possible in order to lower the power consumption of LSI. To estimate the leakage current density, J-V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.).

2.4.2 Characterization of nMOSFET

2.4.2.1 Threshold Voltage (V_{th}) Measurement

One of the common threshold voltage **(V_{th})** measurements is the linear extrapolation method with the drain voltage of typically 50-100 (mV) to ensure operation in the linear MOSFET region.

The threshold voltage is determined from the extrapolated or intercepts gate voltage V_{GSi} by

$$V_T = V_{GSi} - \frac{V_{DS}}{2},$$

where

$$V_{GSi} = V_{GS,\max} - \frac{I_{D,\max}}{g_{m,\max}}.$$

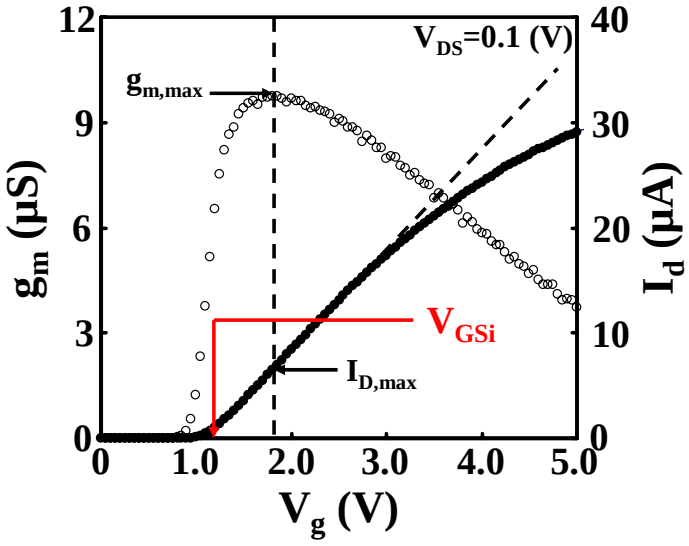


Figure 2.13 : The linear extrapolation method.

2.4.2.2 Subthreshold Slope (*S.S.*) Measurement

The subthreshold slope (*S.S.*) is calculated from below equation.

$$S.S. = \left(\frac{d\left(\log_{10} I_{ds}\right)}{dV_g} \right)^{-1}$$

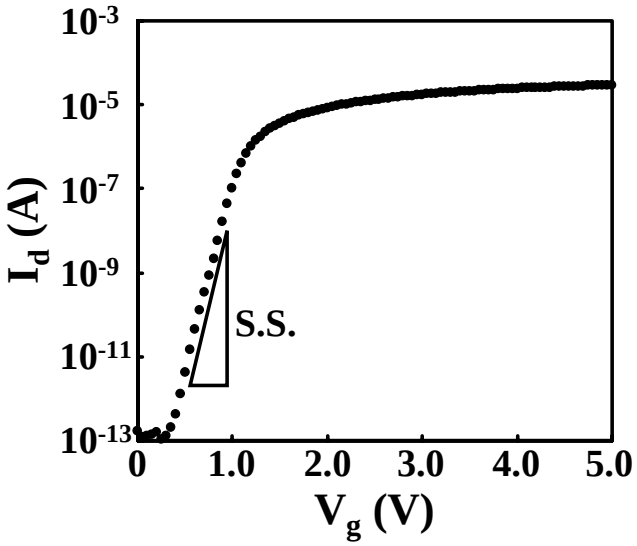


Figure 2.14 : The subthreshold slope calculated from I_d-V_g characteristic.

2.4.2.3 Split C-V Method

One of the most common measurements to obtain the effective mobility (μ_{eff}) is the split C-V method, which combines gate-to-channel capacitance (C_{gc}) and gate-to-bulk capacitance (C_{gb}).

μ_{eff} is obtained from below equation,

$$\mu_{eff} = \frac{g_d L}{W Q_n}$$

where the drain conductance g_d and the inversion charge density Q_n are defined as

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=constant}$$

$$Q_n = \int_{V_{FB}}^{V_{GS}} C_{gc} dV_{GS} .$$

E_{eff} is obtained from below equation,

$$E_{eff} = \frac{1}{\varepsilon_{Si}}\left(|Q_d| + |Q_n|\right)$$

where ε_{Si}=11.9 and the depletion charge density Q_d are defined as

$$Q_d = \int_{V_{FB}}^{V_{th}} C_{gb} dV_{GS}$$

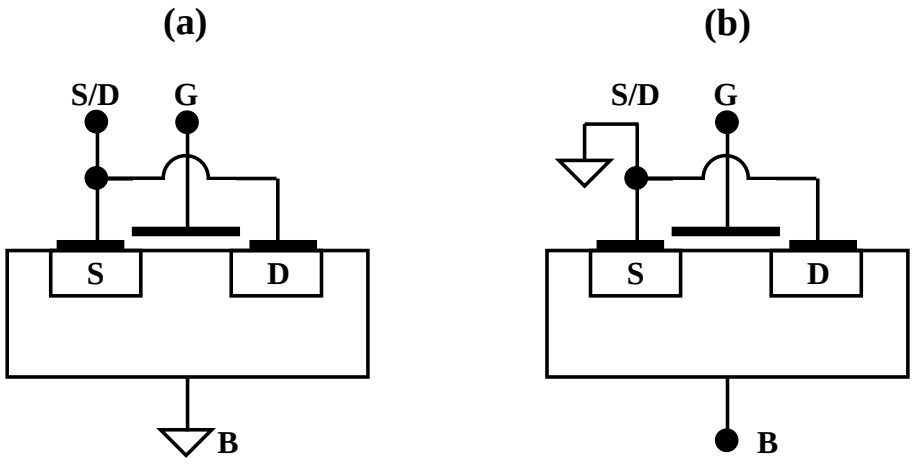


Figure 2.15 : Configuration for (a) gate-to-channel, (b) gate-to-substrate capacitance measurements.

2.4.2.4 Charge Pumping Method

Charge pumping is one of the measurement methods that extract the interface trapped density (D_{it}). Figure 2.16 shows the measurement circuit diagram of charge pumping. The gate of a MOSFET is connected to a pulse generator, a reverse bias (Vr) is applied to the source and the drain, while the substrate current is measured. This current is caused by the repetitive gate pulses the channel between inversion and accumulation.

In this work, we used the square pulse method that extracts the D_{it} from the charge pumping current (I_{cp}) vs. the pulse base voltage (V_{base}) curve.

D_{it} is obtained from below equation.

$$D_{it} = \frac{I_{cp}}{f * q * Ag}$$

where,

I_{cp} : Maximum charge pumping current

f : Pulse frequency

Ag : Channel area of MOSFET

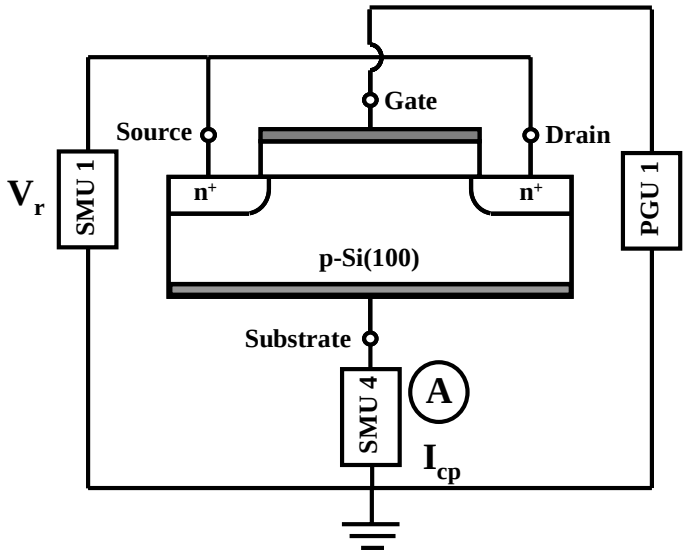


Figure 2.16 : Measurement circuit diagram of charge pumping method.

Chapter 3

Evaluation of Al Gate La_2O_3 nMOSFETs

In this chapter, we discuss electrical characteristics and chemical characteristics at the interface of La_2O_3/Si and gate electrode/La_2O_3. Firstly, we investigated the effect of PDA on several heat treatments to select appropriate annealing condition. Then, we performed PMA with this annealing condition and compared with PDA.

3.1 The effect of PDA on Al Gate La_2O_3 nMOSFETs

3.1.1 Experimental Procedure

La_2O_3 thin films with physical thickness of 4.5 nm were deposited by MBE systems. These films were subsequently annealed by RTA at 300°C for 5min. Ambient of PDA were N_2, O_2, F.G. (Forming Gas) (N_2:H_2=97:3). Then, Al electrode was evaporated by bell jar. In nMOSFETs fabrication process, Al metal etched on H_3PO_4 solution at 45^{o}C.

3.1.2 C-V characteristics of MOS Capacitors

Figure 3.1 shows the C-V characteristics of La_2O_3 MOS Capacitors with PDA performed in N_2 ambient for 5min. As compared to the without PDA sample (AsDepo.), the flat band voltage (V_{FB}) of the PDA sample shifted in a negative direction and the capacitance value increased. Increment of the capacitance value is considered that La_2O_3 films are densified by PDA treatment. The shifted in a negative direction of V_{FB} is due to the increment of positive fixed charges (La^{3+}) induced during the PDA treatment.

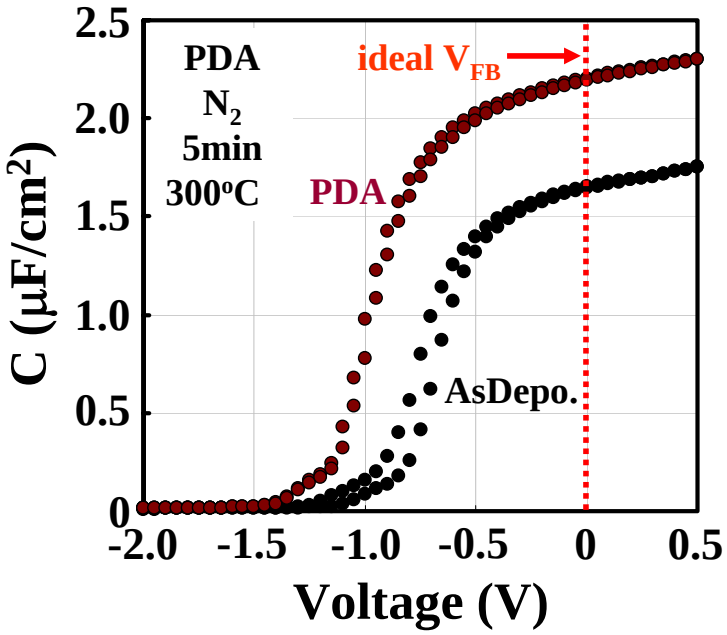


Figure 3.1 : High frequency (100MHz) C-V characteristics of La_2O_3 MOS Capscitors after PDA treatment.

3.1.3 Electrical Characteristics of nMOSFETs

3.1.3.1 I_d - V_d and I_d - V_g Characteristics

Figure 3.2 and 3.3 show the I_d-V_d and I_d-V_g characteristics of Al gate La_2O_3 nMOSFETs with PDA performed in N_2 ambient for 5 min. From Figure 3.2, we confirmed normal operating as a transistor by well behaved I_d-V_d characteristic. From Figure 3.3, we confirmed *Normally-ON* characteristic with V_{th}=-1.09 V and the S.S. of 95 mV/Dec. was obtained.

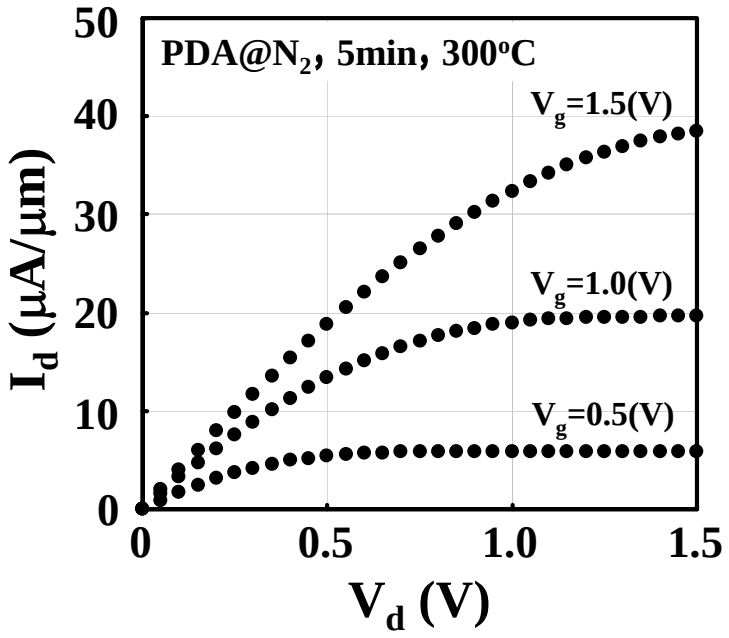


Figure 3.2 : I_d-V_d characteristics of Al gate La_2O_3 nMOSFETs after PDA treatment.

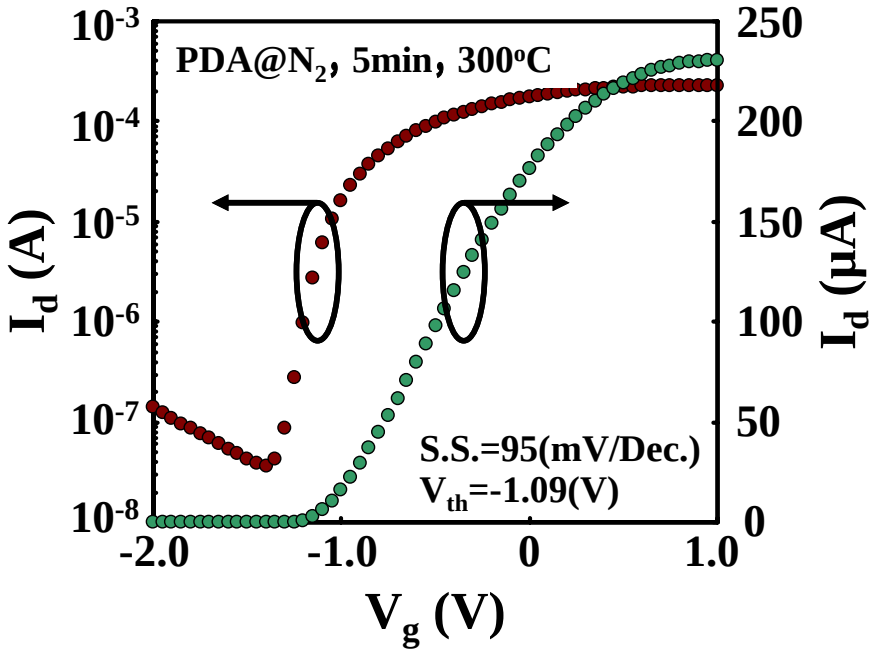


Figure 3.3 : I_d-V_g characteristics of Al gate La_2O_3 nMOSFETs after PDA treatment.

3.1.3.2 Dependence of Annealing Ambient on V_{th} and *S.S.*

Figure 3.4 shows the dependence of annealing ambient on V_{th} and *S.S.*. As compared to the AsDepo., the significant V_{th} shift towards a negative direction was confirmed in all PDA samples. On the other hand, good property on the value of S.S. was obtained by PDA treatment. From this behavior, PDA has effect on the formation of fairly good quality at the La_2O_3/Si interface.

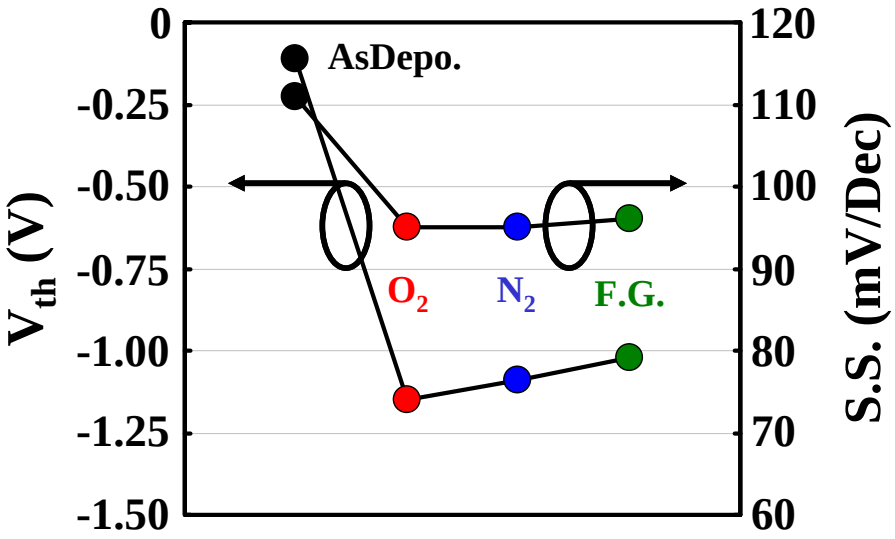


Figure 3.4 : The dependence of annealing ambient on V_{th} and S.S..

3.1.3.3 Effective Electron Mobility (μ_{eff})

Figure 3.5 shows the relationship of effective electron mobility (μ_{eff}) and effective electric field (E_{eff}). As compared to the AsDepo., mobility improvement was confirmed in PDA samples. Among them, PDA sample with N_2 ambient shows higher mobility than other ambient. In AsDepo., mobility degradation can be seen in low E_{eff} side. This is due to the Coulomb Scattering caused by fixed charge (Q_f) or interface trap density (D_{it}).

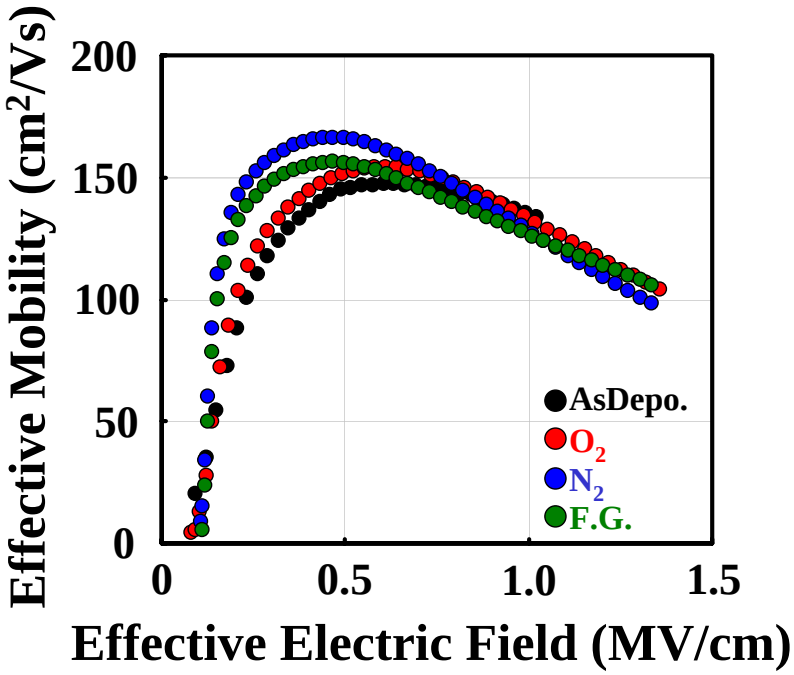


Figure 3.5 : The relationship of effective electron mobility (μ_{eff}) and effective electric field (E_{eff}).

From above mentioned results, it is understood that PDA has the effect on the formation of fairly good quality at the La_2O_3/Si interfaces. Therefore, we researched chemical characteristics at the La_2O_3/Si interfaces to investigate how the composition of interfaces changes after PDA treatment.

3.1.4 Investigation at the La_2O_3/Si interfaces by XPS

Figure 3.6 shows the XPS Analysis of (a) La-*3d* and (b) O-*1s* spectrums measured in take-off angle at 45°. From La-*3d* spectrum, in the PDA samples, the peak of La shifted the low energy side about 0.5 eV as compared to the AsDepo., which suggests that the uncombined atoms of La and O in the AsDepo. are binding after PDA treatment. From O-*1s* spectrum, it can be seen that the peak of La_2O_3 was appeared by 530 eV. This is considered that the uncombined atoms of La and O_2 in the AsDepo. are binding

after PDA treatment in the same result of La-*3d* spectrum. For this reason, in the PDA samples, as compared to the AsDepo., the formation of fairly good quality at the La_2O_3/Si interfaces was obtained thanks to the suppression of defects in La_2O_3 films.

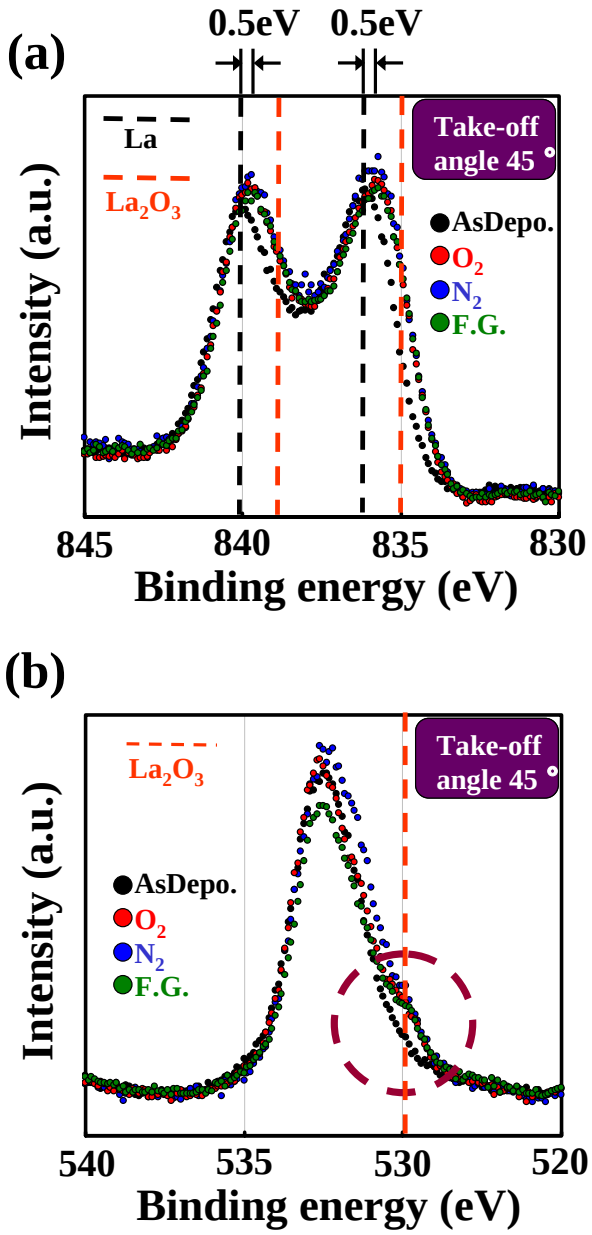


Figure 3.6 : The XPS Analysis of (a) La-*3d* and (b) O-*1s* spectrums measured in take-off angle at 45°.

Figure 3.7 shows the XPS Analysis of O-*1s* spectrum measured in take-off angle at 30° and 60° respectively. Whereas the peak of La_2O_3 is not appeared in take-off angle at 30°, it is appeared in take-off angle at 60°. As a result, it is considered that the amount of La-O bond increased as near La_2O_3/Si interface.

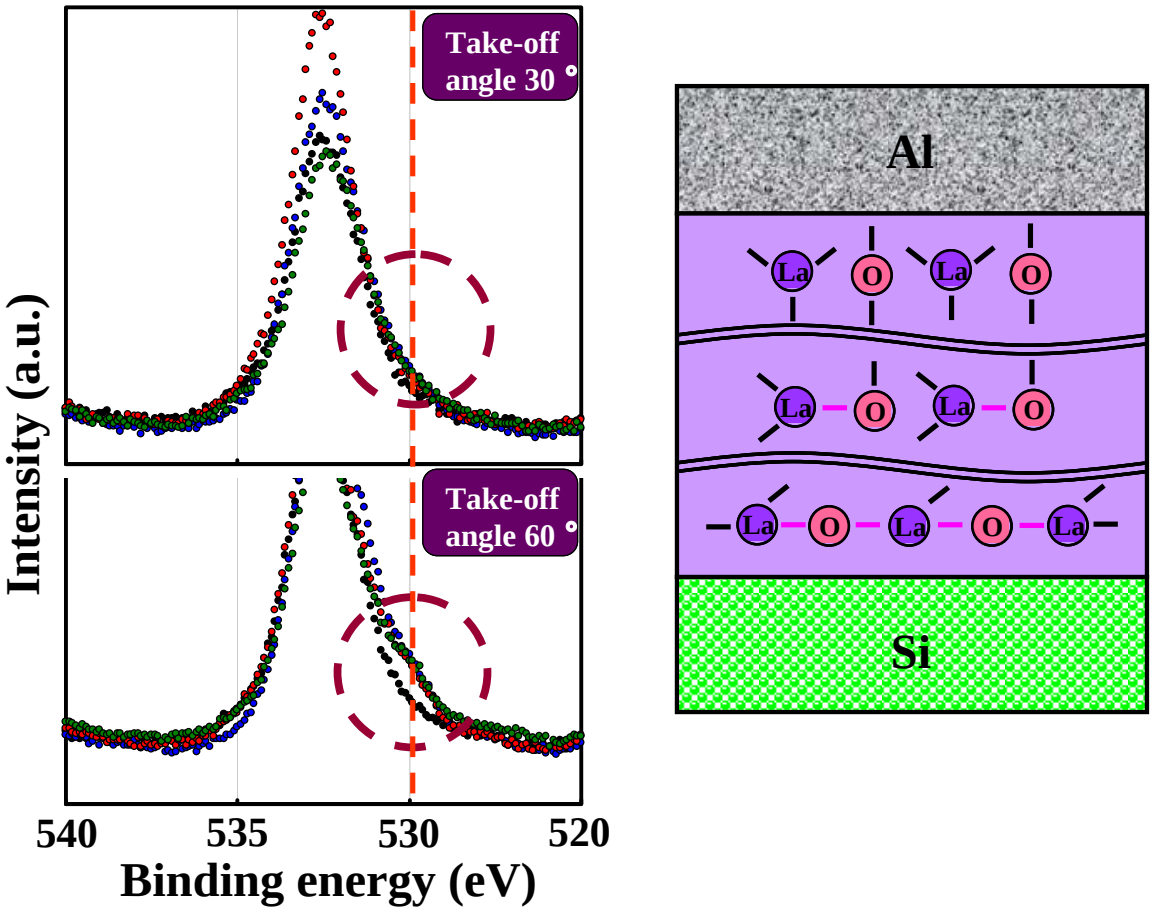


Figure 3.7 : The dependence of take-off angle at 30° and 60° in O-*1s* spectrum.

3.1.5 Summery

In this section, we investigated the effect of PDA on Al gate La_2O_3 nMOSFETs. As a result, we could improve the mobility by PDA in N_2 ambient, which is thanks to the increment of La-O bond near the interface of La_2O_3 and Si. However, the obtained mobility is very low and *Normally-ON* characteristic was confirmed in the case of PDA. Thus, we investigated the effect of PMA on Al gate La_2O_3 nMOSFETs to solve these issues.

3.2 The effect of PMA on Al Gate La_2O_3 nMOSFETs

3.2.1 C-V Characteristics of MOS Capacitors

Figure 3.8 shows the C-V characteristics of La_2O_3 MOS Capacitors after PDA and PMA. As compared to the PDA sample, V_{FB} of the PMA sample shifted in a positive direction and the capacitance value decreased. This behavior can be explained by the formation of an interfacial layer at the Al/La_2O_3 interface.

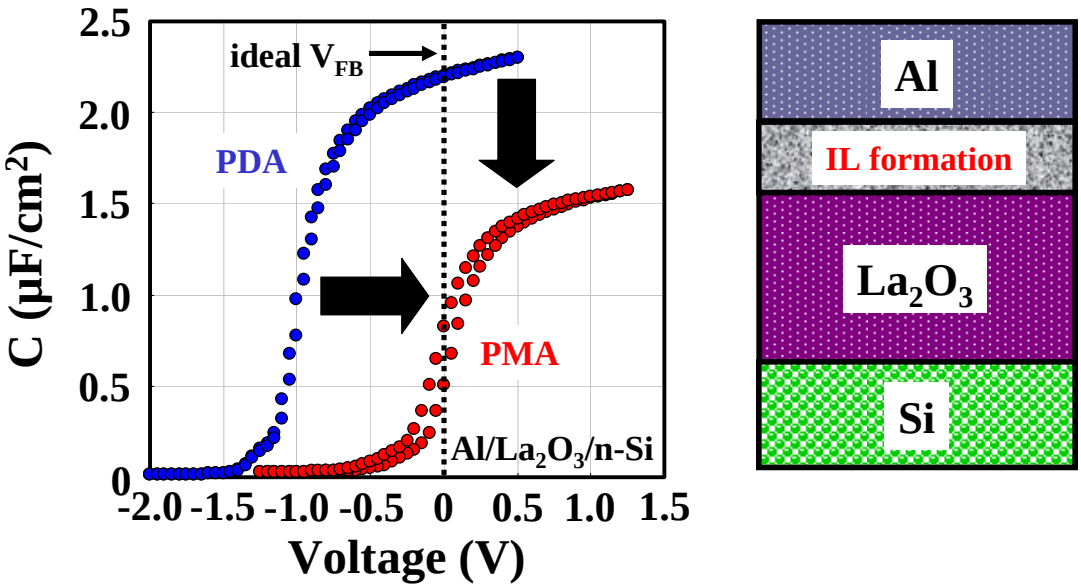


Figure 3.8 : High frequency (100MHz) C-V characteristics of La_2O_3 MOSCAP after PDA and PMA.

3.2.2 Electrical Characteristics of nMOSFETs

3.2.2.1 I_d - V_d and I_d - V_g Characteristics

Figure 3.9 shows I_d-V_d characteristics of Al gate La_2O_3 nMOSFETs with PMA treatment in N_2 ambient for 5 min compared with PDA. Higher drive current was

obtained for the PMA sample as compared to the PDA sample. Figure 3.10 shows the I_d-V_g characteristics. Extracted V_{th} of 0.36 V confirm that *Normally-ON* characteristic was completely suppressed after PMA treatment and good S.S. of 83 mV/Dec. was obtained.

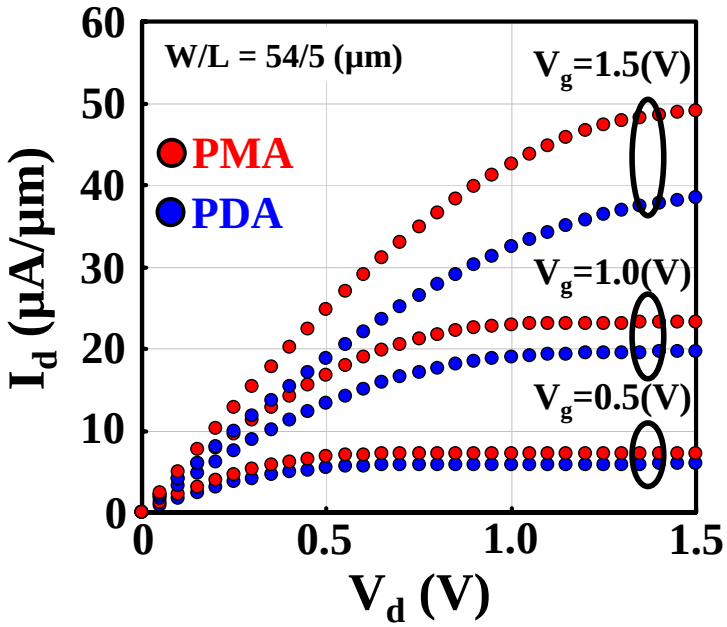


Figure 3.9 : I_d-V_d characteristics of Al gate La_2O_3 nMOSFETs with PMA treatment in N_2 ambient for 5 min compared with PDA.

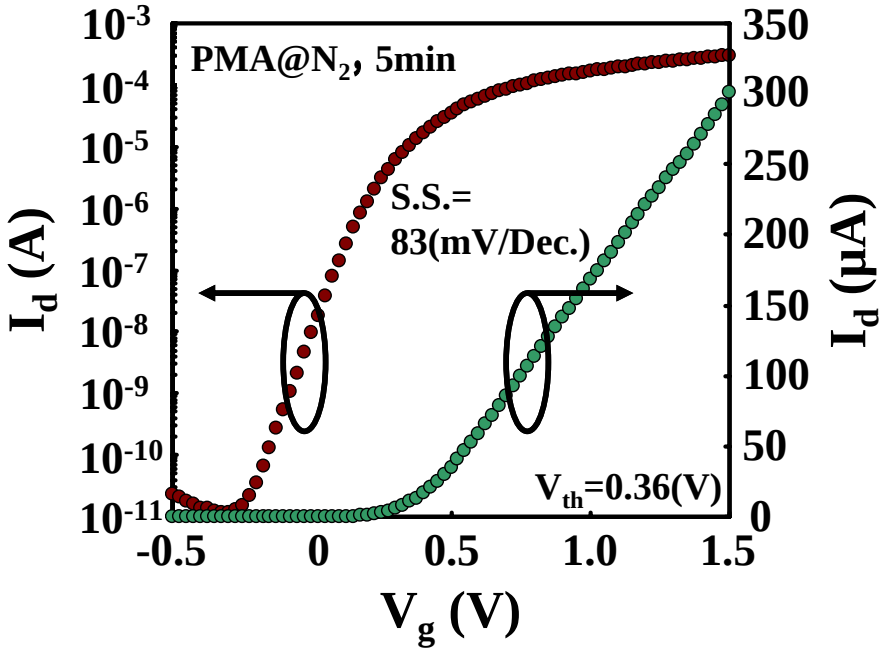


Figure 3.10 : I_d-V_g characteristics after PMA treatment.

3.2.2.2 J_g-V_g characteristics

Figure 3.11 shows J_g-V_g characteristics with comparison of PDA and PMA. The leakage current of the PMA sample decreased by about two orders of magnitude compared to that of the PDA sample.

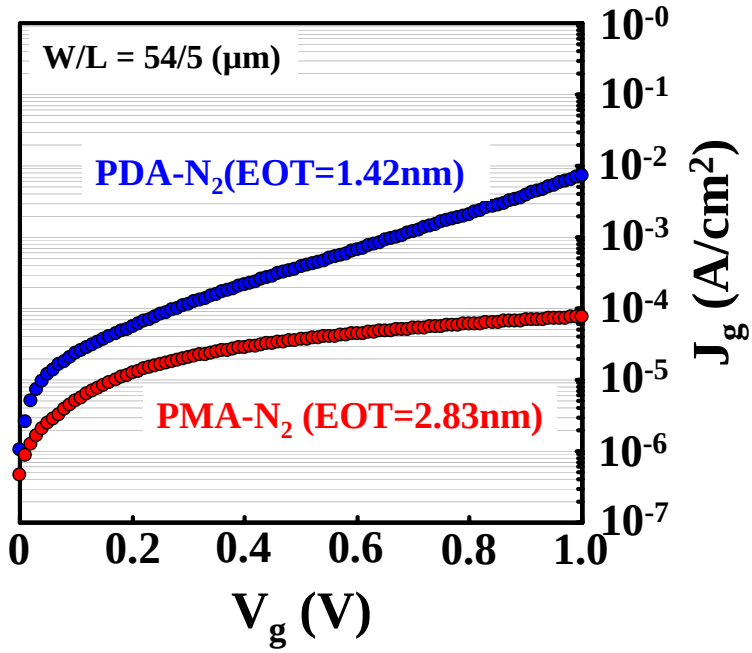


Figure 3.11 : The J_g-V_g characteristics comparison with PDA and PMA.

3.2.2.3 Effective Electron Mobility (μ_{eff})

Figure 3.12 shows the comparison of effective electron mobility (μ_{eff}) of Al and Pt gate La_2O_3 nMOSFETs. In the case of the Al electrode, the effective mobility was improved after PMA treatment as compared to PDA treatment. However, Al gate nMOSFETs gave better mobility than those with Pt gates after the same PMA treatment. Although the physical thickness of La_2O_3 was the same, an EOT increment was observed in the case of an Al gate. In order to explain the mobility improvement and EOT increment of PMA samples, XPS was used to analyze the metal/La_2O_3 interface.

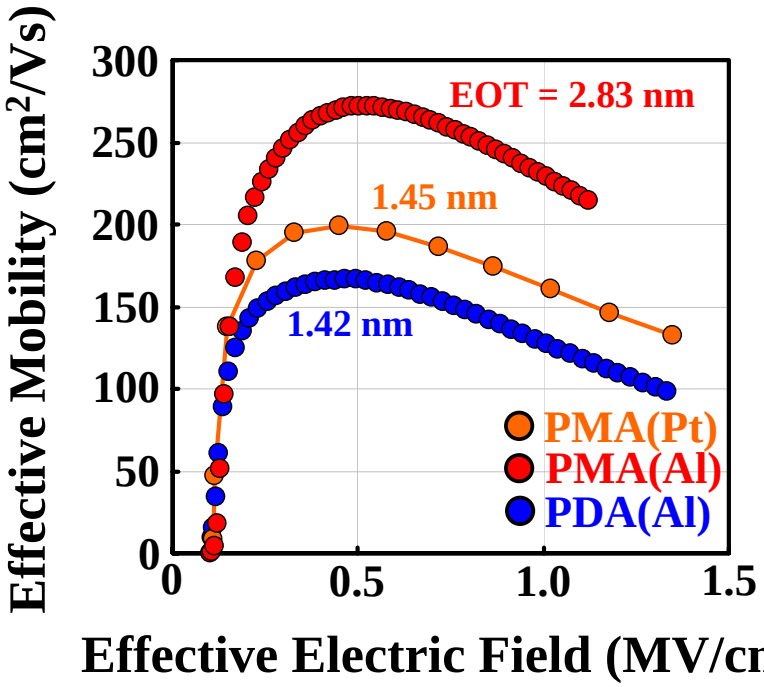


Figure 3.12 : Effective electron mobility (μ_{eff}) of Al and Pt gate La_2O_3 nMOSFETs.

3.2.3 Investigation at the Metal/La_2O_3 interfaces by XPS

Figure 3.13 shows the XPS Analysis of (a) Pt/La_2O_3 and (b) Al/La_2O_3 structures after PMA. From Pt-*4f* and La-*3d* spectra, no chemical shift was observed for the Pt and La_2O_3 peaks, thus there is no formation of an interfacial layer between Pt and La_2O_3. From Al-*2p* and O-*1s* spectra, chemical shifts were clearly observed, which suggests the formation of Al_2O_3 at the Al/La_2O_3 interface.

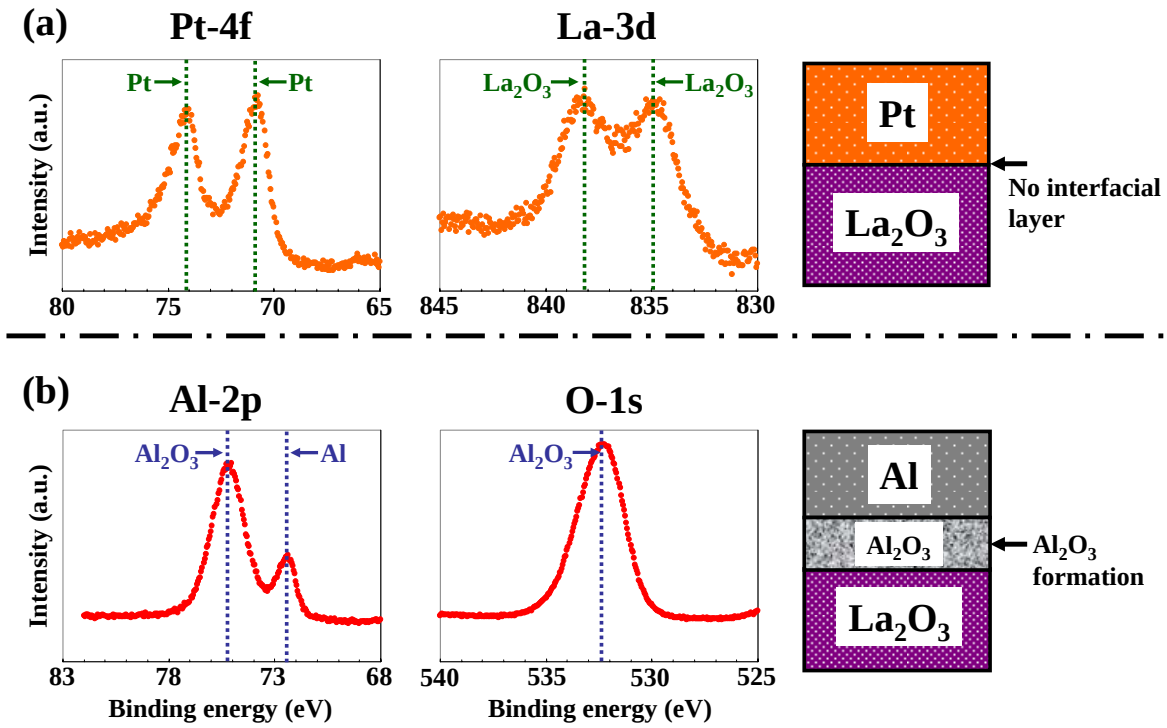


Figure 3.13 : XPS Analysis of (a) Pt/La_2O_3 and (b) Al/La_2O_3 structures after PMA.

3.2.4 Estimation of the Al_2O_3 thickness after PMA treatment

Estimation of the Al_2O_3 thickness after PMA treatment was carried out by CV measurements for various annealing durations (Figure 3.14). Longer annealing decreases the capacitance value, and also induces hysteresis in the CV measurements. The reduction in capacitance can be attributed to the formation of Al_2O_3, which has a relatively lower dielectric constant of 8 used for the thickness calculation. Figure 3.15 shows the relationship between flatband voltage shift (ΔV_{FB}) and annealing duration. As the annealing duration increased, V_{FB} shifted further in a positive direction. This might be due to the formation of the Al-O- dangling bonds in the Al_2O_3, which may be ascribed to negative fixed charge. Thus, we were motivated to investigate the precise

thickness control of the Al_2O_3 layer to offset ΔV_{FB}. In order to obtain ΔV_{FB}=0, we estimated the Al_2O_3 thickness from EOT calculations and observations by TEM. For the PMA sample with 10 minutes of annealing, the Al_2O_3 thickness can be estimated to be 2.2nm from the EOT, which is in good agreement with the TEM observation of 2.0 nm. Figure 3.16 shows the relationship between Al_2O_3 thickness and ΔV_{FB}. From this figure, the Al_2O_3 thickness was nearly proportional to ΔV_{FB}. From the figure, we can estimate that 1.3 nm Al_2O_3 is necessary to offset ΔV_{FB} to zero.

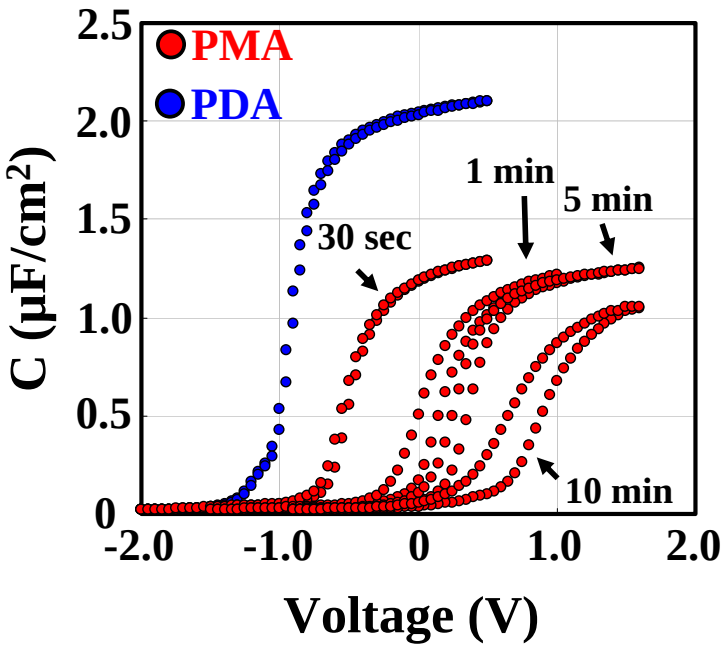


Figure 3.14 : C-V characteristics of Al gated La_2O_3 MOS Capacitors. Longer PMA shifts the flatband voltage in a positive direction.

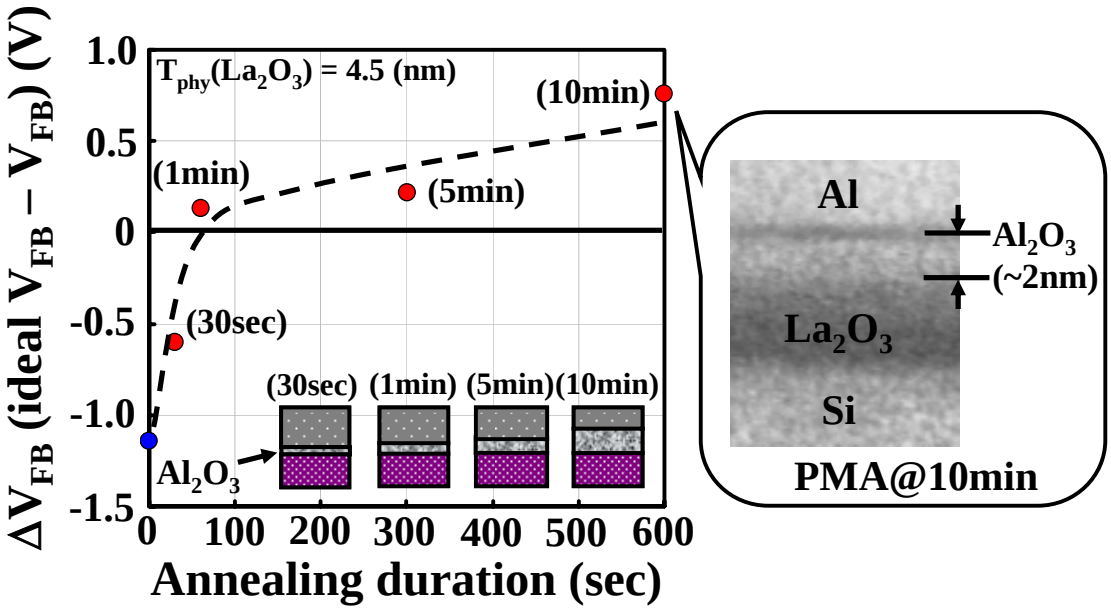


Figure 3.15 : The dependence of ΔV_{FB} on annealing duration. A 1 minute annealing can cancel the shift.

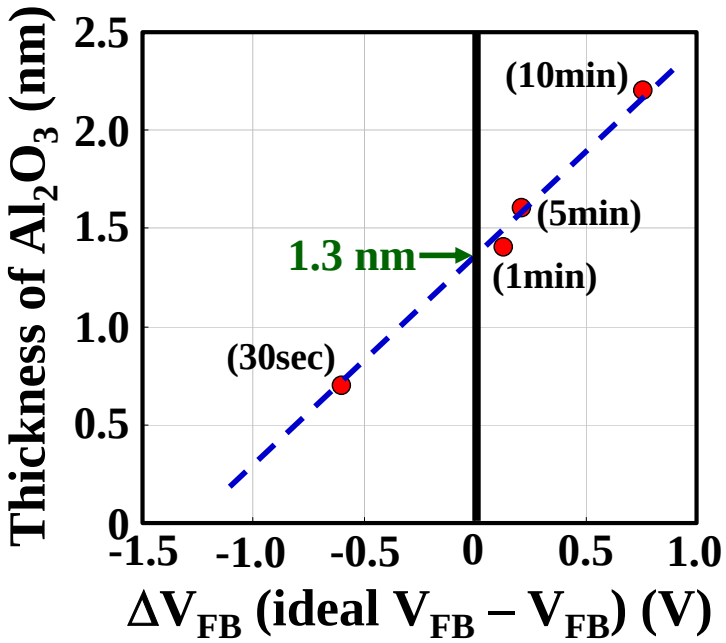


Figure 3.16 : The dependence of Al_2O_3 thickness on ΔV_{FB}. Ideal flatband voltage can be obtained with 1.3 nm of Al_2O_3.

3.2.5 The proposed model for mobility improvement

Figure 3.17 shows the proposed model for mobility improvement in PMA MOSFETs. After PDA, V_{FB} shifted in the negative direction. We speculate that the fixed charge density (Q_f) and the interface trapped density (Q_{it}) increased due to oxygen vacancies inside the La_2O_3 formed during PDA. On the other hand, after PMA, The negative charge of Al_2O_3 compensates the positive charge of La_2O_3. It was not confirmed that Al diffuses into La_2O_3 film to annihilate the positive charge of La_2O_3, which might be the main reason behind mobility improvement.

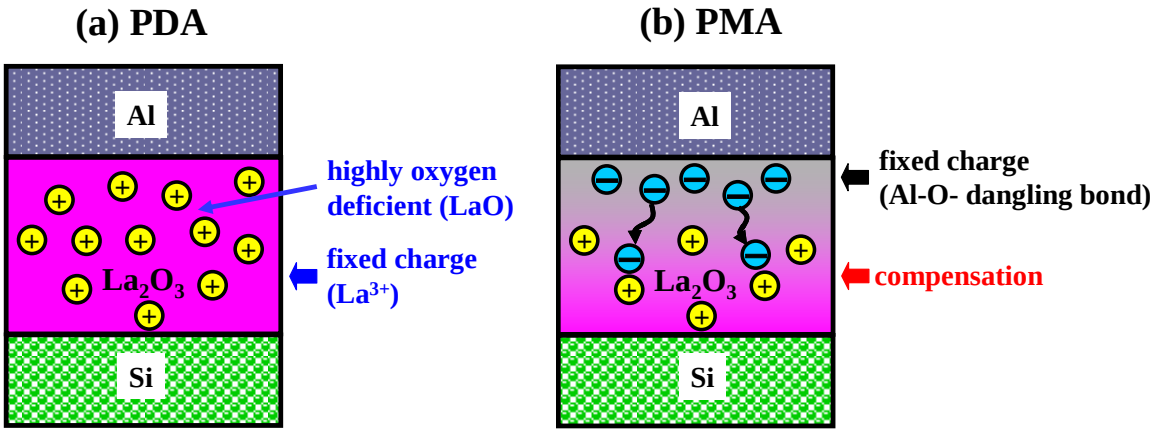


Figure 3.17 : Proposed model for mobility improvement by (a) PDA, (b) PMA. The number of oxygen vacancies seems to be suppressed by the Al gate electrode.

3.2.6 Summary

In this section, we investigated the effect of PMA on Al gate La_2O_3 nMOSFETs. As a result, we could improve the mobility by PMA treatment as compared to the PDA, which is thanks to that the negative charge of Al_2O_3 compensates the positive charge of La_2O_3. However, there is a critical issue of EOT increment in the case of Al gate electrode with PMA treatment. Thus, we search for a new gate electrode material to suppress the EOT increment.

Chapter 4

Evaluation of W Gate La_2O_3 nMOSFETs

In this chapter, first of all, we explored several gate electrode materials to select the best one out of them. Next, we fabricated nMOSFETs using selected gate electrode in an effort to realize the device of below EOT = 1 nm. Lastly, we proposed the structure that Al adds to the interface of gate electrode and La_2O_3 and discussed the mobility improvement.

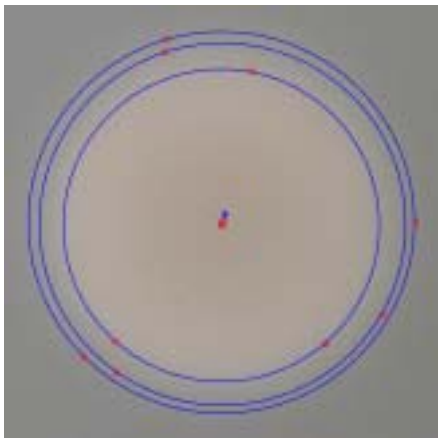
4.1 Investigation of Gate Electrode Materials

4.1.1 Experimental Procedure

Ti, Ru, W and TaN were formed on the same physical thickness of La_2O_3. PDA and PMA were performed to each electrode in N_2 ambient for 5min at 300°C. All electrodes were formed by RF sputtering method.

4.1.2 C-V Characteristics of Each Electrode

Figure 4.1 shows the C-V characteristics of each electrode. In this experiment, the accumulation capacitance values of each metal have large amount of uncertainties due to the overcoating of metal through shadow mask. However, even taking these facts into account, it is clear that the capacitance values of metals used in this experiment are higher than that of Al. Among them, considering the C-V curve and high capacitance value, W was chosen for the following experiments.



*overcoating by sputter

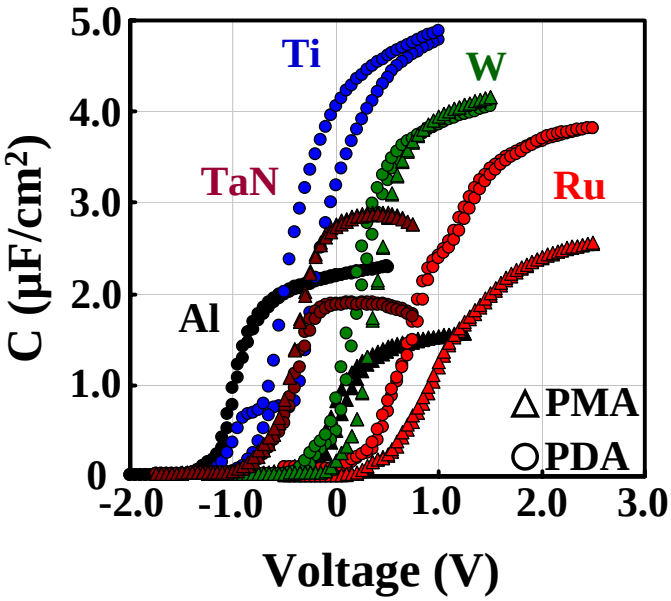


Figure 4.1 : The C-V characteristics of each electrode.

4.2 Evaluation of W Gate La_2O_3 nMOSFETs

4.2.1 Comparison with Evaporation and Sputter

4.2.1.1 Experimental Procedure

There is fear that the formation of electrode using sputter causes a lot of physical damage in gate insulator film. Thus, we formed gate electrode by evaporation and compared with sputter. Additionally, in order to realize a device of below EOT = 1 nm, comparatively thin La_2O_3 film with physical thickness of 4.0 to 4.5 nm was used. Both of PDA and PMA were performed in N_2 ambient for 5 min at 300°C. W was etched by H_2O_2 solution.

4.2.1.2 J_g-EOT characteristics

Figure 4.2 shows the J_g-EOT characteristics. In the case of evaporation, nearly the same value of J_g was obtained in no dependence of annealing condition. The smallest EOT of 1.10 nm was obtained in PMA sample. On the other hand, in the case of sputter, EOT was reduced about 2 nm as compared to the evaporation in spite of the J_g levels are just about the same. The smallest EOT of 0.92 nm could be realized in both of PDA and PMA sample. The increment of EOT by evaporation was considered that the high amount of silicate layer was formed. This is because evaporation camber becomes high temperature which is due to the high melting point of W.

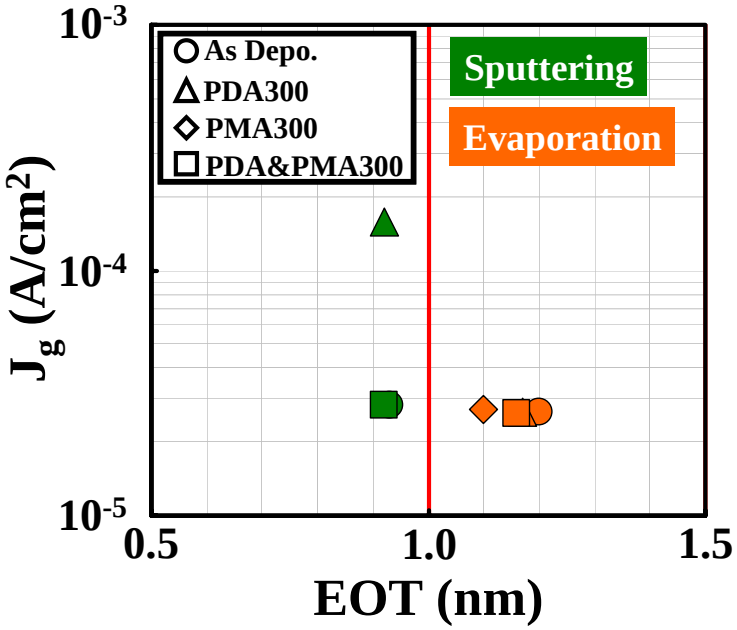


Figure 4.2 : J_g-EOT plot with comparison of evaporation and sputter

4.2.1.3 Electrical Characteristics of W Gate La_2O_3 nMOSFEs

We compared the sample with EOT=0.92 nm obtained from sputter and EOT=1.10 nm obtained from evaporation. Figure 4.3 shows the I_d-V_d characteristics. From these figure, we conformed normal operating as a transistor both of them. Figure 4.4 shows the I_d-V_g characteristics. From these figures, good subthreshold slope was obtained by sputter as compared to the evaporation. Figure 4.5 shows the relationship of μ_{eff} and E_{eff}. Maximum μ_{eff} of 138 and 150 cm^2/Vs was obtained from sputter and evaporation.

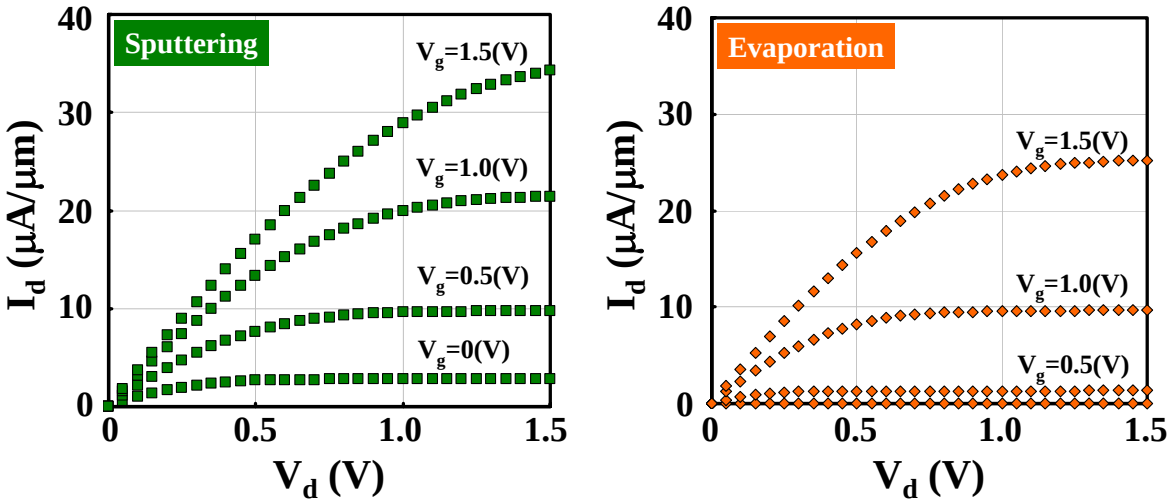


Figure 4.3 : I_d-V_d characteristics in the sample of 0.92 and 1.10 nm.

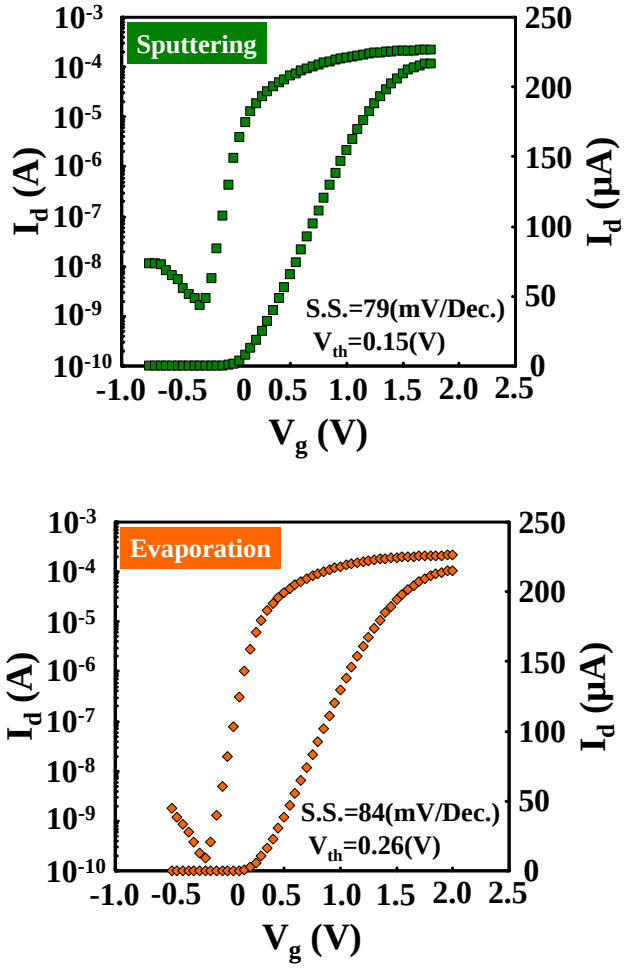


Figure 4.4 : I_d-V_g nMOSFET characteristics with EOT of 0.92 and 1.10 nm.

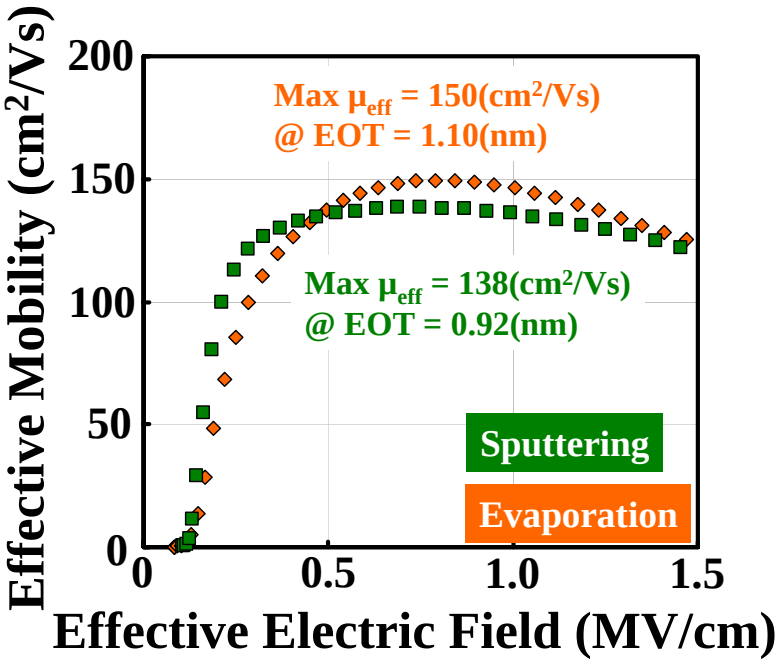


Figure 4.4 : The relationship of μ_{eff} and E_{eff} with EOT of 0.92 and 1.10 nm.

4.2.1.4 Summery

In this subsection, we fabricated W gate La_2O_3 nMOSFETs using sputter and evaporation and then evaluated these samples. As a result, minimum EOT of 0.92 nm can be obtained by sputter and confirmed normal operation as a transistor. However, the value of μ_{eff} obtained from this experiment was too small. Thus, there is a definite limit to improve the mobility with reducing EOT. Therefore, we proposed the structure that Al adds to the interface of W and La_2O_3 and evaluated weather mobility increment was obtained or not with minimizing increment of EOT.

4.3.2 Investigation of W/Al/La_2O_3 Structure

4.3.2.1 Experimental Procedure

W and Al were formed by sputter on the La_2O_3 with physical thickness of 6.0 nm. The amounts of added Al were 0, 0.5, 1.0 and 2.0 nm respectively. PMA was performed at 300°C, 400°C, 500°C and 600°C in N_2 ambient for 5min respectively.

4.3.2.2 J_g-EOT Characteristics

Figure 4.5 shows the dependence of annealing temperature and the amount of added Al on J_g-EOT characteristics. In the case that PMA was performed at 300°C, 400°C and 500°C, the tendency to increase EOT and to decrease J_g could be confirmed as the amount of added Al increased, and then the best characteristic was obtained at 300°C. However, in the case of PMA at 600°C, both of EOT and J_g increased as the amount of added Al increased. The reasons for these behaviors were that the silicate layer increased due to the high temperature annealing treatment and the defect was formed in La_2O_3 film due to the Al diffusion into the La_2O_3 film.

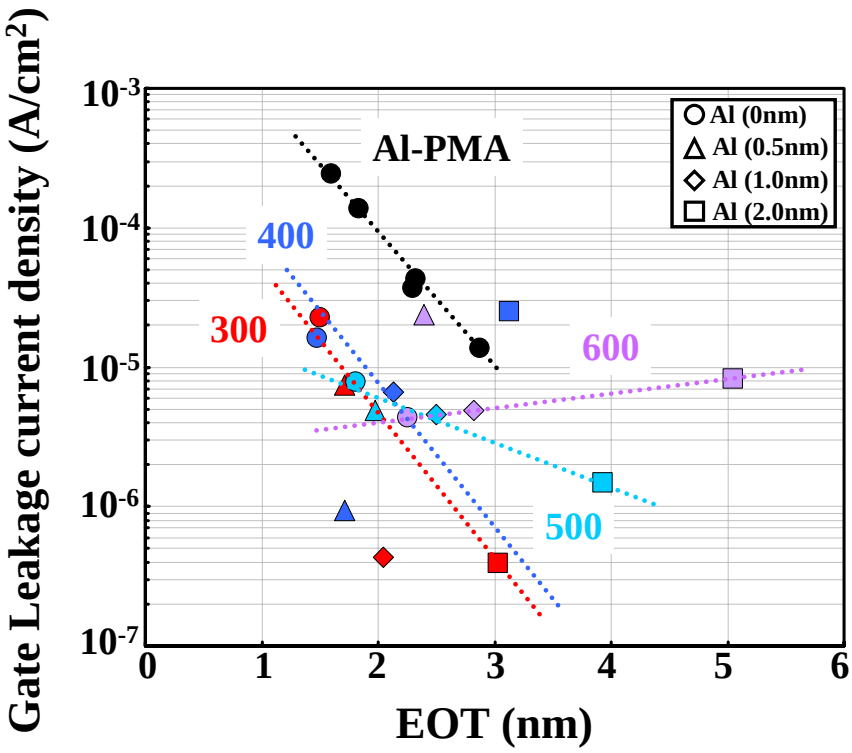


Figure 4.5 : The dependence of annealing temperature and the amount of added Al in J_g-EOT characteristics.

4.3.2.3 *S.S.* and V_{th}

Figure 4.6 shows the dependence of annealing temperature and the amount of added Al on *S.S.*. In the case that PMA was performed at 300°C, very good *S.S.* of 66 mV/Dec., which is nearly the same as SiO_2 reference, was obtained. The tendency that *S.S.* deteriorates as annealing temperature rises was confirmed. As concerns the dependence of the amount of added Al, *S.S.* deteriorates drastically in the case with added Al of 2.0 nm on each annealing temperature, which is due to the interface trap caused by the Al diffusion into the La_2O_3 film.

Figure 4.7 shows the dependence of annealing temperature and the amount of added Al on V_{th}. There is the abrupt deterioration of V_{th} in the case with added Al of 2.0

nm just as in the case of *S.S.*. This is due to the high amount of positive fixed charge, which is arise from the factor that the high amount of Al absorb O atoms in La_2O_3 film, in consequence it is considered that V_{th} shifted negative side drastically.

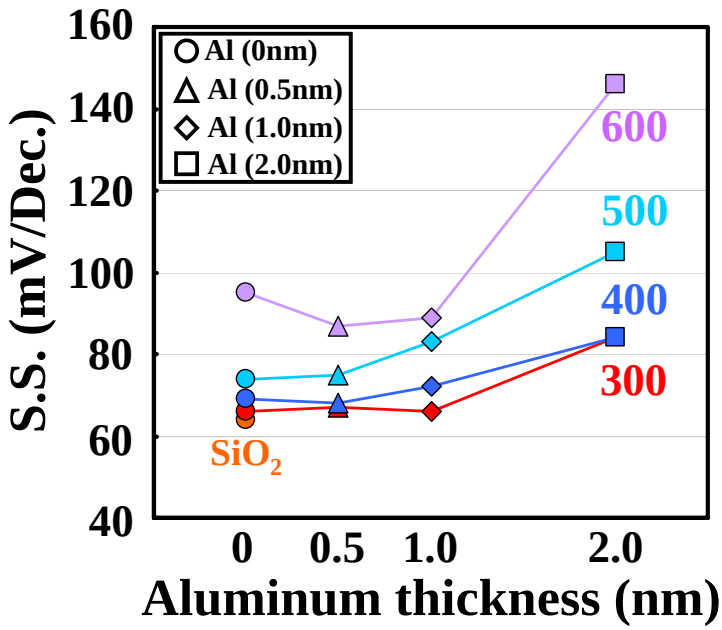


Figure 4.6 : The dependence of annealing temperature and the amount of added Al on *S.S.*.

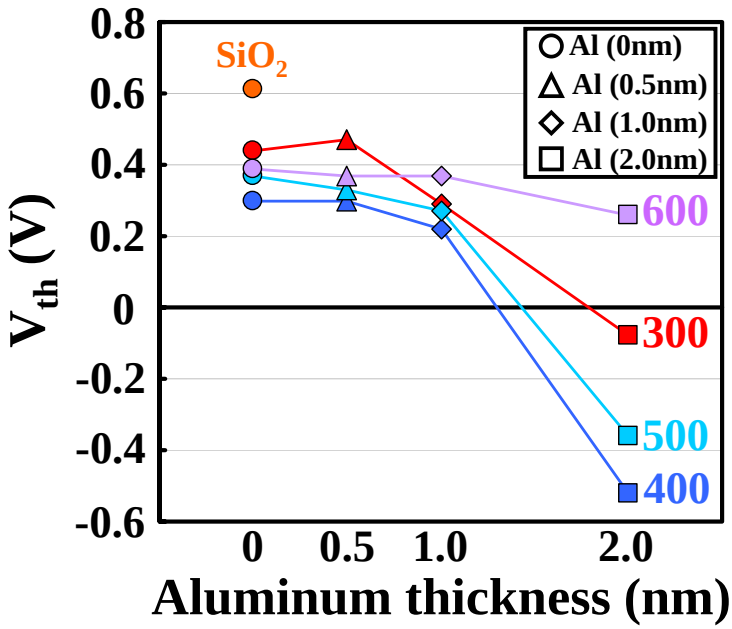


Figure 4.7 : The dependence of annealing temperature and the amount of added Al on V_{th}.

4.3.2.4 Effective Electron Mobility (μ_{eff})

Figure 4.8 shows the dependence of the amount of added Al on each annealing temperature. In the samples with added Al of 0.5 and 1.0 nm at 300°C, 400°C and 500°C PMA treatment, mobility was improved as compared to the sample without added Al. However, significant mobility degradation could be seen the sample with added Al of 2.0 nm. This is due to the coulomb scattering which is ascribed to the fixed charge and interface trapped density. On the contrary, in the case of 600°C, mobility was nearly the same value in no dependence on the amount of added Al.

Figure 4.9 shows the dependence of the annealing temperature on each the amount of added Al. In the samples without added Al and with added Al of 0.5, 1.0 nm, mobility degradation was confirmed as annealing temperature rise. At the same time, mobility was improved in the sample with added Al of 2.0 nm as annealing temperature rises.

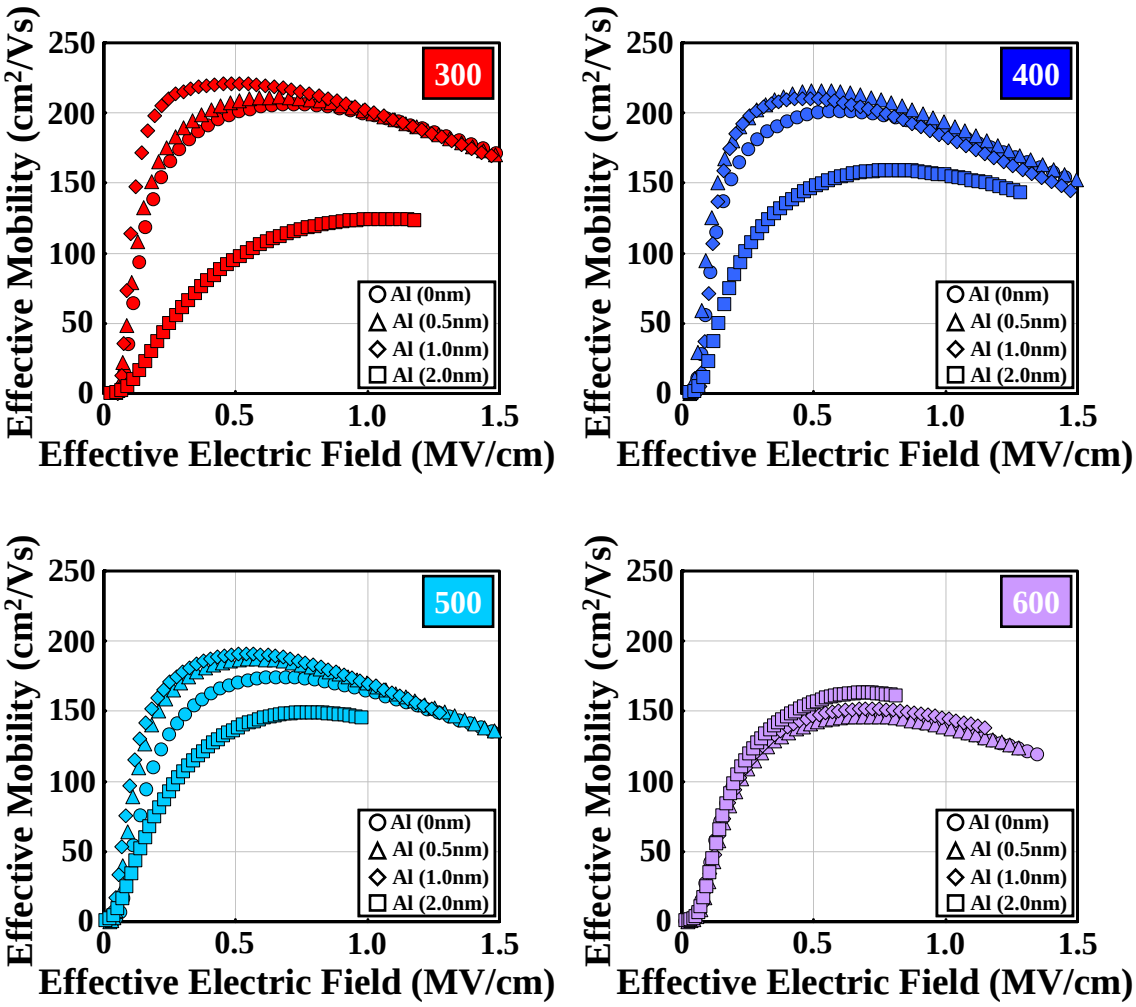


Figure 4.8 : The dependence on the amount of added Al on each annealing temperature in μ_{eff}.

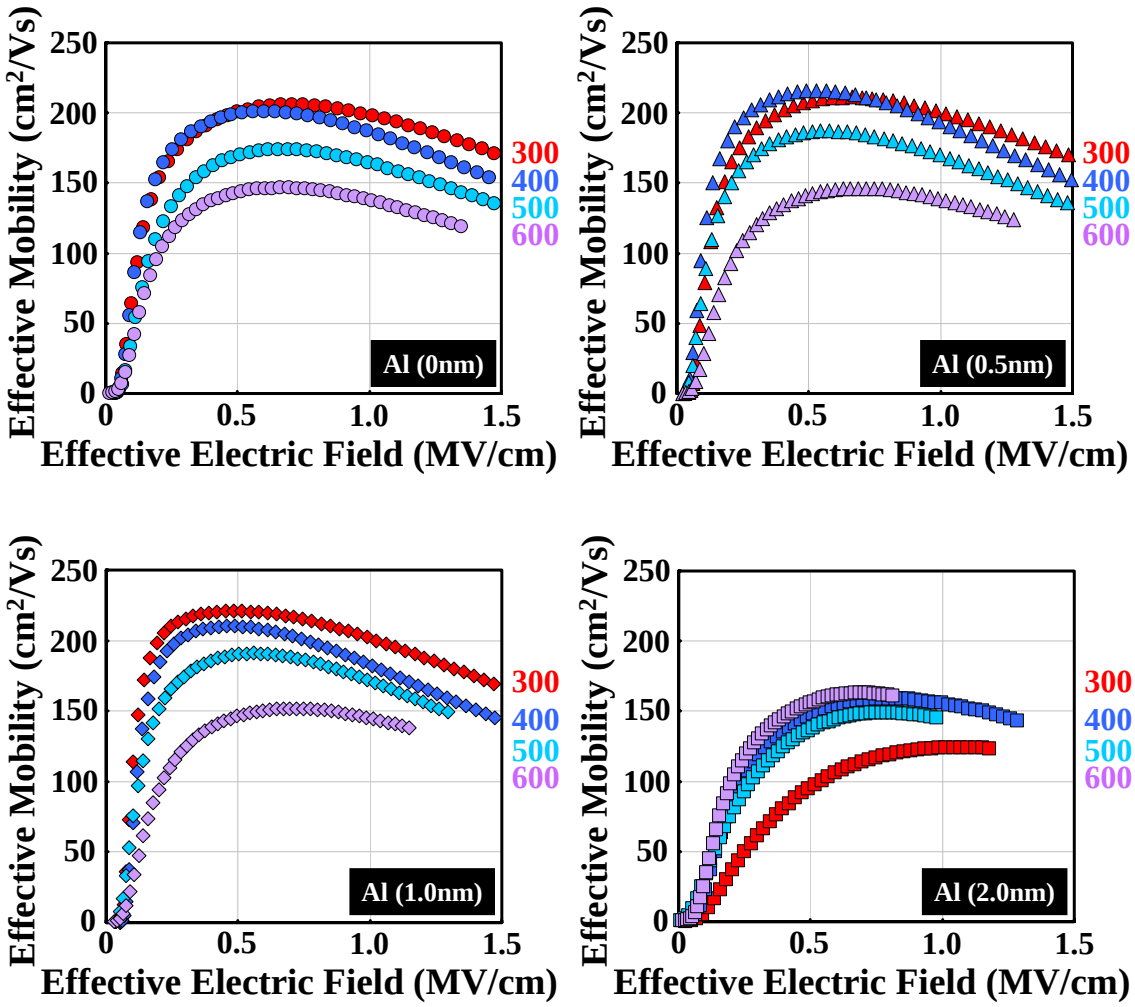


Figure 4.9 : The dependence of the annealing temperature on each the amount of added Al in μ_{eff}.

4.3.2.4 Interface Trap Density (D_{it})

Figure 4.10 shows the dependence of the amount of added Al on each annealing temperature. In case of all annealing temperature, the tendency that D_{it} increases as the amount of added Al increase was confirmed. This is due to the diffusion and O_2 absorption of Al.

Figure 4.11 shows the dependence of the annealing temperature on each the amount of added Al. In all case of the amount of added Al, nearly the same D_{it} obtained at PMA with 300°C and 400°C, while D_{it} increment was confirmed as annealing temperature rise at PMA with 500°C and 600°C.

Figure 4.12 shows the relationship of peak μ_{eff} and D_{it}. From this figure, the tendency to degrade μ_{eff} as D_{it} increase was confirmed, which suggests that μ_{eff} depends on D_{it} considerably. But then, the samples which has nearly the same value of D_{it} were compared, high μ_{eff} can be obtained from Al added samples as compared to the without Al added samples. As results, it is considered that the cause of mobility degradation was not only D_{it} but also another factor. Therefore, we attempted the low temperature measurement to explore the cause of mobility degradation.

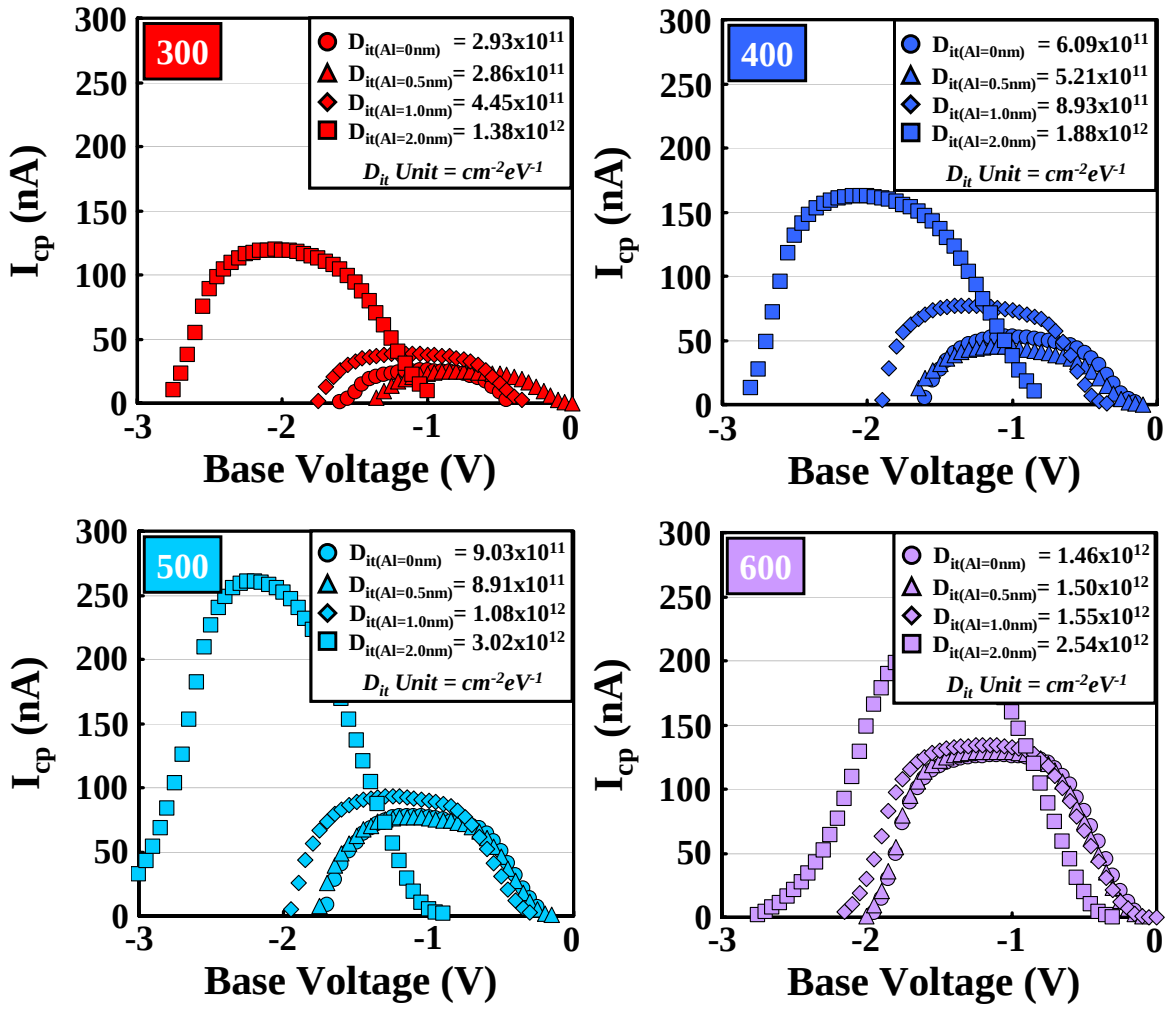


Figure 4.10 : The dependence on the amount of added Al on each annealing temperature in D_{it}.

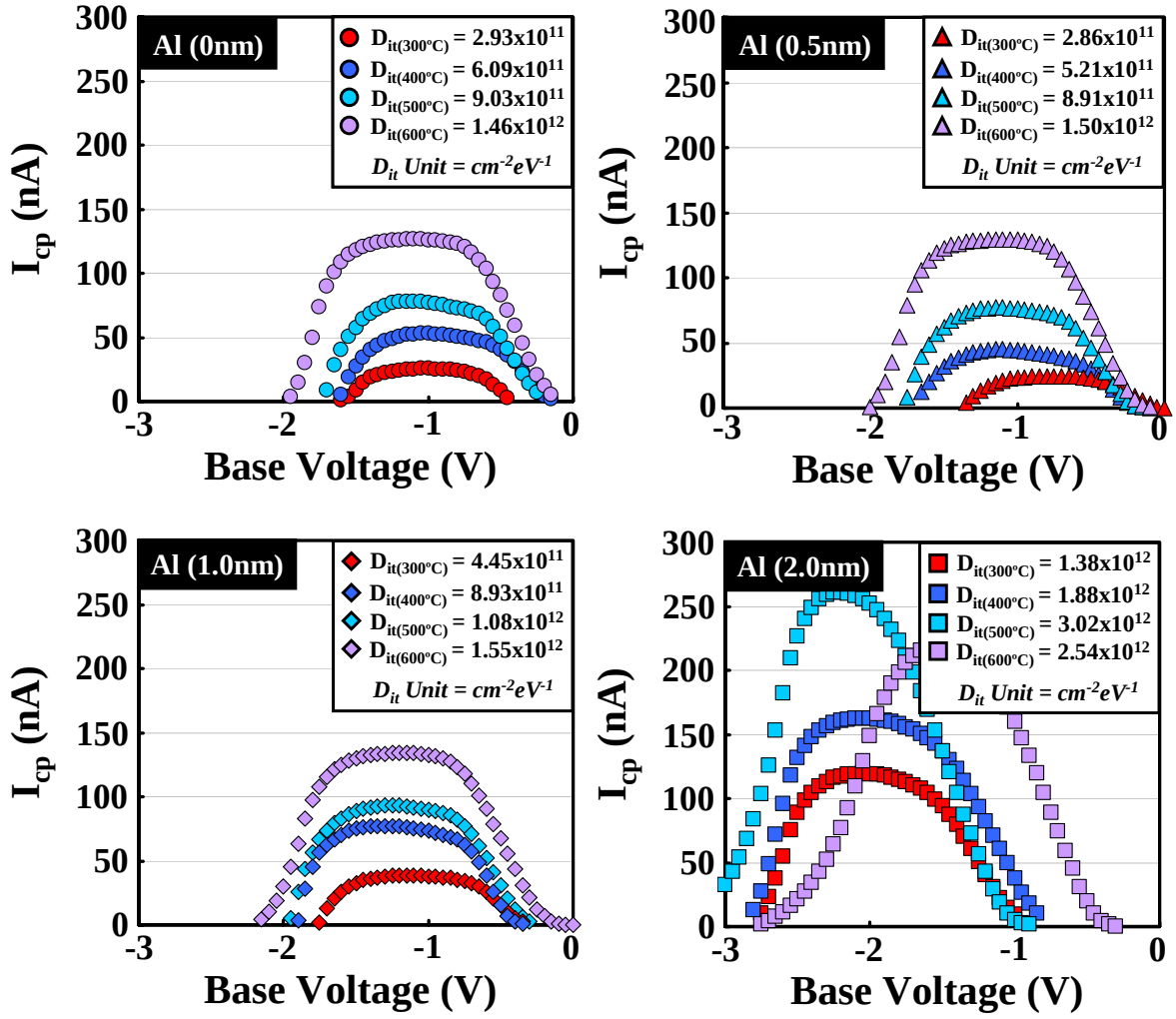


Figure 4.11 : The dependence of the annealing temperature on each the amount of added Al in D_{it}.

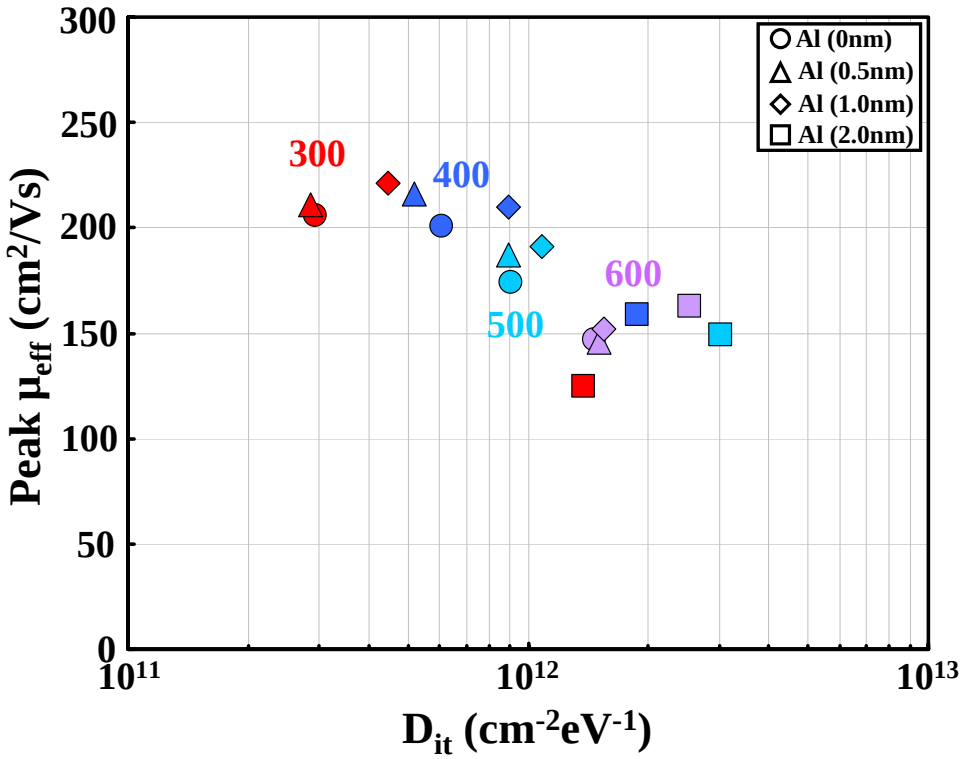


Figure 4.12 : The relationship of peak μ_{eff} and D_{it}.

4.3.2.5 Low Temperature Measurement

We used the two sample of without Al and with added Al of 1.0 nm in the case of PMA at 300°C, and then we measured these two samples in 40K, 80K, 150K, 300K respectively. Figure 4.13 shows the relationship of μ_{eff} and E_{eff}. From this figure, as measurement temperature lower, mobility improvement can be seen in the sample with added Al of 1.0 nm. On the other hand, mobility improvement can not be seen in the sample without Al. Especially, this behavior become prominent in low E_{eff} side which suggests that the sample without Al come under the strong influence of coulomb scattering due to the fixed charge. As a result, it is considered that the influence of fixed charge in the La_2O_3 films can be suppressed in the sample with added Al of 1.0 nm as compared to the sample without Al.

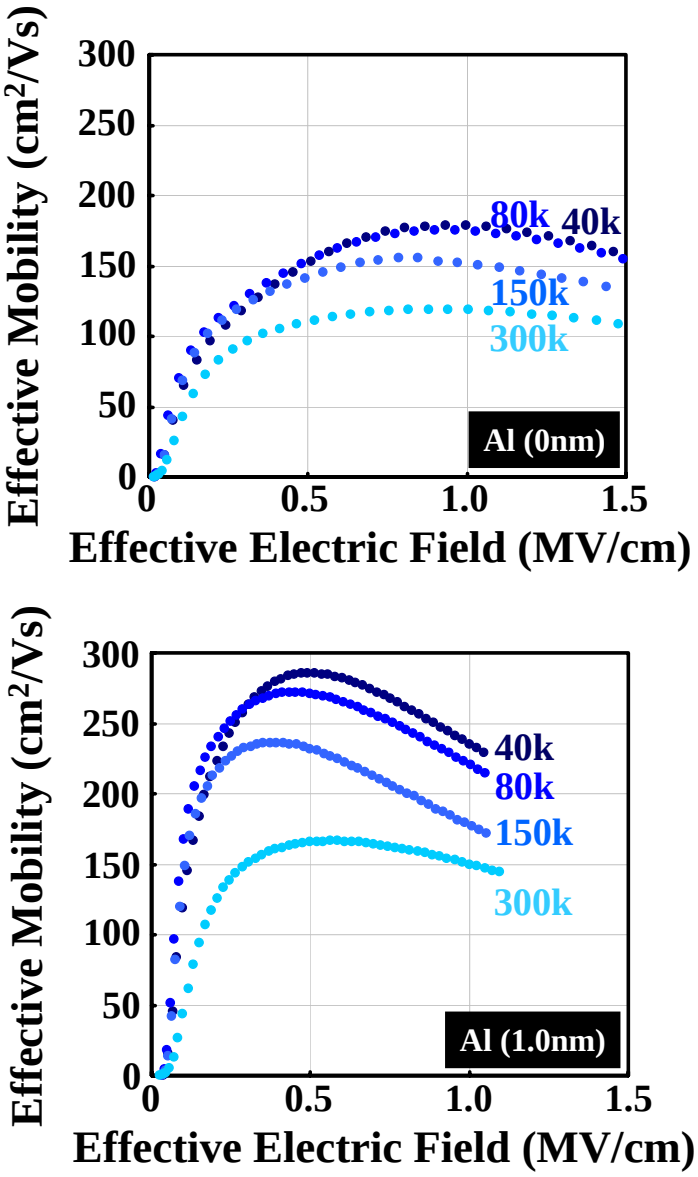


Figure 4.13 : The comparison on μ_{eff} of the sample of without Al and with added Al of 1.0 nm.

4.3.2.6 Summery

In this subsection, we proposed the structure that Al adds to the interface of W and La_2O_3 and then the effect of Al addition evaluated. As a result, in low temperature annealing from 300 to 500°C, mobility improvement can be obtained from the samples with added Al of 0.5 and 1.0 nm as compared to the sample without added Al, which is thanks to the suppression of influence of fixed charge.

Chapter 5

Conclusions

5.1 Results of This Study

In this work, several annealing condition and metal gate electrode were evaluated to optimize the fabrication process for La_2O_3 nMOSFET and improve the mobility.

5.1.1 Al Gate La_2O_3 nMOSFETs

We investigated the effect of PDA and PMA on Al gate La_2O_3 nMOSFETs. The results obtained from this experiment are as follows.

- We could improve the mobility by PDA in N_2 ambient, which is thanks to the increment of La-O bond near the interface of La_2O_3 and Si. However, the obtained mobility is very low and *Normally-ON* characteristic was confirmed.

- We could improve *Normally-ON* characteristic and the mobility by PMA treatment as compared to the PDA, which is thanks to that the negative charge of Al_2O_3 compensates the positive charge in La_2O_3 films. However, EOT increment was confirmed in the case of Al gate electrode with PMA treatment.

5.1.2 W Gate La_2O_3 nMOSFETs

We explored several gate electrode materials and then selected W as the best gate electrode materials. The results of W Gate La_2O_3 nMOSFETs are as follows.

- Minimum EOT of 0.92 nm can be obtained and then confirmed normal operation as a transistor.

- In low temperature annealing from 300 to 500°C, mobility improvement can be obtained from the samples with added Al of 0.5 and 1.0 nm as compared to the sample without added Al, which is thanks to the suppression of influence of fixed charge.

5.2 Future Prospects for La_2O_3

Figure 5.1 and 5.2 show the J_g-EOT and Peak μ_{eff}-EOT plots obtained from in this work. From these figures, La_2O_3 exhibits excellent results than Hf-based materials on J_g. On the other hand, μ_{eff} was too small as compared with the Hf-based materials. Therefore, How to maximize the dielectric constant to gain thick physical thickness becomes more and more important because μ_{eff} decreases with EOT.

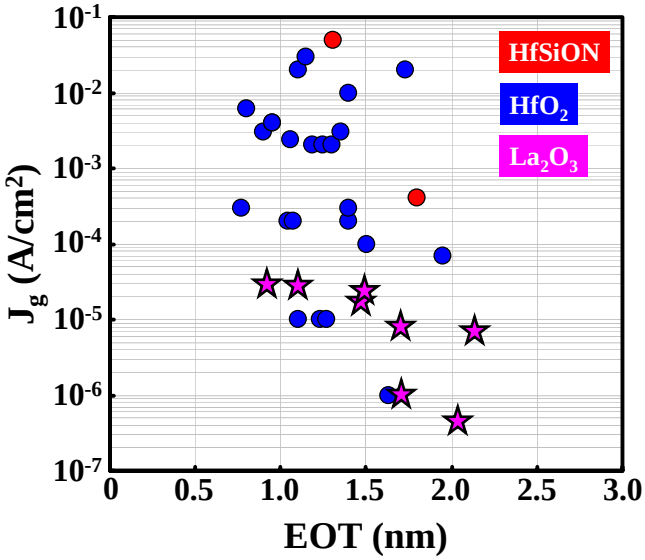


Figure 5.1 : J_g-EOT plot of La_2O_3 and Hf-based materials.

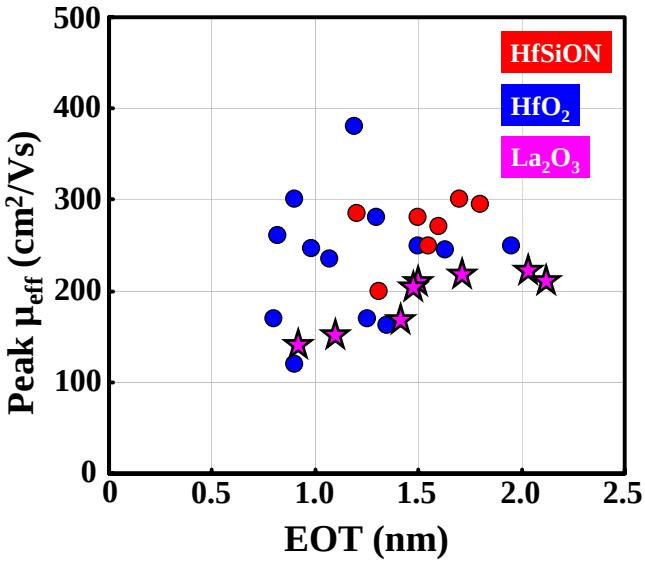


Figure 5.2 : Peak μ_{eff}-EOT plot of La_2O_3 and Hf-based materials.

Acknowledgments

The author would like to thank his supervisor at Tokyo Institute of Technology, Professor Hiroshi Iwai for his excellent guidance and continuous encouragement.

The author would like to thank Professor Nobuyuki Sugii very much for his polite instruction, useful advice, and continuous support.

The author would like to thank Professor Hiroshi Ishiwara for his valuable advice.

The author would like to thank Professor Takeo Hattori for his valuable advice on XPS.

The author would like to thank Associate Professor Kazuo Tsutsui for his valuable discussions.

The author would like to thank Associate Professor Shun-ichiro Ohmi for his useful advice and discussions.

The author would like to thank Dr. Kuniyuki Kakushima and Dr. Perlhat Ahmet for his useful discussions and appropriate advice for this study.

The author would like to thank Mr. Jin Aun NG for his kind instruction for the

experiment.

The author would like to thank all members of Professor Iwai's Laboratory, Mr. Atsushi Kuriyama, Mr. Mollina Reyes Joel, Mr. Yuichiro Sasaki, Mr. Hendriansyah Sauddin, Mr. Issui Aiba, Mr. Ruifei Xiang, Mr. Kentaro Nakagawa, Mr. Akira Fukuyama, Mr. Satoshi Yoshizaki, Mr. Koji Nagahiro, Mr. Jaeyeol Song, Mr. Takashi shiozawa, Mr. Yasuhiro shiino, Mr. Masayuki Nakagawa, Mr. Kiichi Tachi and Woei Yuan Chong for their kind friendship and discussions.

The author would like to express sincere gratitude to laboratory secretaries, Ms. N. Iizuka, Ms. Y. Hashizume, Ms. T. Fukuyama and Ms. A. Matsumoto.

This study was partially supported by Semiconductor Technology Academic Research Center (STARC).

This study was partially supported by Grant-in-Aid for Scientific Research Priority Areas (A): Highly Functionalized Global Interface Integration.

Finally the author would like to thank his parents for their everlasting supports and understanding.

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Yokohama, JAPAN

January 2006

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