Master Thesis

Electrical Characteristics of La_2O_3 MIM Capacitor with Different Process Condition

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Contents

CONTENTS I

CHAPTER 1 1
1.1 Background of this study 2
1.2 High-k Gate Dielectric and La_2O_3 4
1.3 Conduction Mechanism 10
1.3.1 Schottky (SK) Conduction 10
1.3.2 Poole-Frenkel (P-F) Conduction 12
1.3.3 Space-charge-limited current (SCLC) 15
1.3.4 Fowler-Nordheim (F-N) Conduction 16
1.3.5 Image-force Effect 17
1.4 Purpose of This Study 18

CHAPTER 2 20
2.1 Si Substrate Wet Cleaning 21
2.2 E-Beam Evaporation by Molecular Beam Epitaxy (MBE) Method 22
2.3 Rapid Thermal Annealing (RTA) 23
2.4 Atomic Force Microscopy (AFM) 24
2.5 Transmission Electron Microscopy (TEM) 25
2.6 Spectroscopic Ellipsometry 26
2.7 Voltage Coefficient of Capacitance (VCC) 27

CHAPTER 3 29
3.1 Fabrication Process of Pt/La_2O_3/Pt MIM Capacitor 30
3.2 Characteristics of Pt/La_2O_3/Pt MIM Capacitor 31
3.2.1 Deposition Temperature 31
3.2.2 Characteristics of MIM Capacitor 33
3.2.3 Conduction Mechanism 40
3.2.4 Roughness of Bottom Pt Surface 47
3.2.5 Summary 50
3.3 Fabrication Process of Pt/La_2O_3/Pt/W MIM Capacitor 51
3.4 Characteristics of Pt/La_2O_3/Pt/W MIM Capacitor 52
3.4.1 Characteristics of MIM Capacitor 52
3.4.2 Conduction Mechanism 62

3.4.3 Pt/La_2O_3/Si MIS Capacitor 69
3.4.4 Summary 72

CHAPTER 4 73
4.1 Conclusion of this study 74
4.2 Future Issues 76

ACKNOWLEDGEMENTS 77

REFERENCES 78

Chapter 1

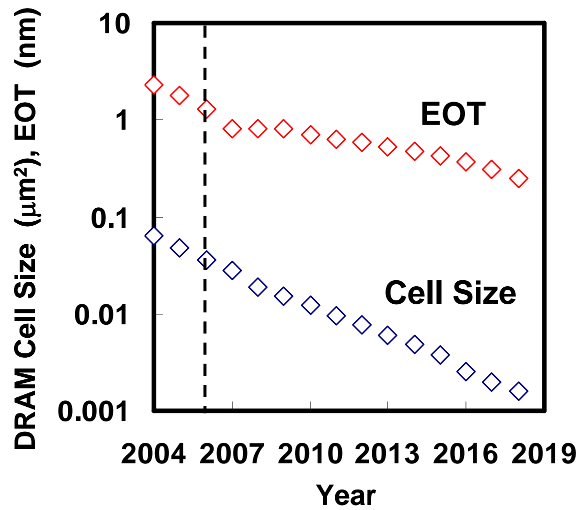
Introduction

1.1 Background of this study

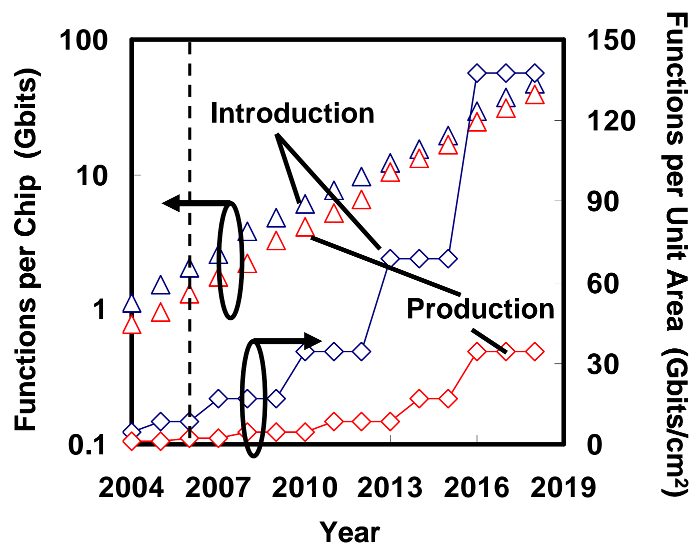
Recently, LSI used various products such as personal computer, cellular phone and mobile devices etc. It is required more and more high speed and low power consumption. These products and requirements are realized by the progresses of silicon LSI technology that are high density, high integration and so on. The performance of LSI technology depends on the characteristics of metal-insulator-semiconductor field effect transistor (MISFET), MIS capacitor and metal-insulator-metal (MIM) capacitor. As the minimizing physical size of the devices, more and more possible to integrate transistors and capacitors and integration of various functions were attained and developed. As possible to attain various functions, it is expected that the importance for RF and DRAM (Dynamic Random Access Memory) devices will increase in the future, more and more. So, not only transistors but also MIM capacitors are important devices. But SiO_2-based transistor used LSI devices has serious problem such as increasing of the power consumption by increasing leakage current of devices caused tunneling current for thin film. In capacitors, the needed capacitance do not keep for more and more integration. More and more integrated, improved increasing leakage current is important factor for LSI devices and products. High-k material is one of the improved this problem – High-k materials have a high relative dielectric constant. So, film thickness will be possible to thick to reduce direct tunneling current.

Famous devices to use MIM capacitor is DRAM. High capacitance density with good electrical and physical characteristics MIM capacitor is importance for the future MIM application. Since MIM capacitor have high capacitance density, cell area of DRAM capacitor will be reduced and easily integration more and more. Recently, many mobile devices used DRAM capacitor and increase DRAM capacitor amount and using

devices more and more. RF device is also important device and will increase to use more and more for the future. So, MIM capacitors that used to DRAM and RF are very important devices and need to develop devices for our useful and happy life.



(a) DRAM cell size and EOT



(b) Functions (Gbits) per chip and Area

Fig.1-1 ITRS roadmap for DRAM

1.2 High-k Gate Dielectric and La_2O_3

The metal-insulator-semiconductor (MIS) transistor which constitutes the main building block of large scale integration (LSI) systems and metal-insulator-metal (MIM) capacitors must be shrunk in size to improve its performance. For that purpose, the thicknesses of gate and capacitor insulator have been thinner. Up to the present, SiO_2, SiON and Si_3N_4 have been used gate insulator and capacitor. Because SiO_2, SiON and Si_3N_4 have a good property such as very low fixed charge density and high thermal stability on Si substrate, especially. According to International Technology Roadmap for Semiconductor (ITRS), in the future, the gate dielectric oxide will become a few atoms in thickness because of this continuous shrinking for MIS transistor and a higher capacitance density and lower leakage current will be required for capacitor [1]. However, if the dielectric oxide is too thin, then the gate tunneling leakage current exponentially increase and this effect brings about serious problems to operate the devices.

In the case of thick insulator, that works as barrier for tunneling carriers. However, in the case of thin insulator less than about 1 nm, the carriers directly pass through the insulator owing to quantum effect. Consequently, the leakage current increase exponentially. This phenomenon will cause increasing of power consumption and degradation of LSI reliability.

As one of the solutions for overcoming the limits of SiO_2 dielectric as described in before, high-k materials have been attached much attention. High-k material has high relative dielectric constant. The capacitance C_i is expressed as following.

$$C_i = \varepsilon_0 \varepsilon_i \frac{S}{t} \quad \text{(Eq.1-1)}$$

Here, ε_0 and ε_i are vacuum dielectric constant (8.855×10^{-14} F/cm) and relative dielectric constant (ex. SiO_2 is 3.9), S is electrode area, t is thickness of film. As a method of maintaining enough capacitance value with shrinking of gate area, the physical thickness of insulator has been thinned conventionally. However, the phenomenon of direct tunneling leakage current effect by the limit of thinning physical thickness will be serious problem. Therefore, any other new schemes have been required to maintain capacitance density with the shrinking device. As one of the breakthrough ways, there is the way using high-k material instead of conventional SiO_2, SiON and Si_3N_4. This way make possible to increase insulator thickness with maintaining capacitance density. The band diagrams of high-k material case and SiO_2 are shown in Figure 1-2. The arrows represent flow of carrier. As this figure, direct tunneling leakage current can be suppressed by increasing insulator thickness owing to using high-k material.

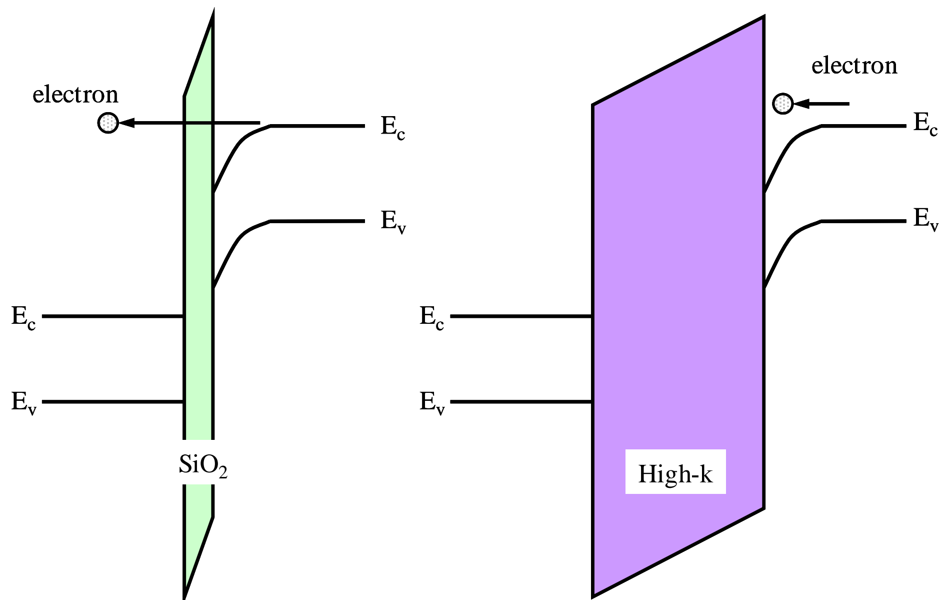


Fig.1-2 Band diagrams of high-k material and SiO_2

ITRS requires the replacement of SiO_2 gate dielectric and MIM capacitor films with high-k materials immediately. The requirement for high-k materials are high relative dielectric constant, low leakage current density, chemical thermodynamic stability on Si, heat stability, small interface state density and fixed charge, high mobility and high reliability.

Recently, in order to overcome the limits of SiO_2, SiON and Si_3N_4, several promising materials have been investigated by a large number of researchers. Under these restricted conditions, metal oxides like Al_2O_3, ZrO_2, HfO_2 and rare earth oxides have been studied eagerly for the next generation gate dielectric materials because they have high relative dielectric constants and wide bandgap [29-31].

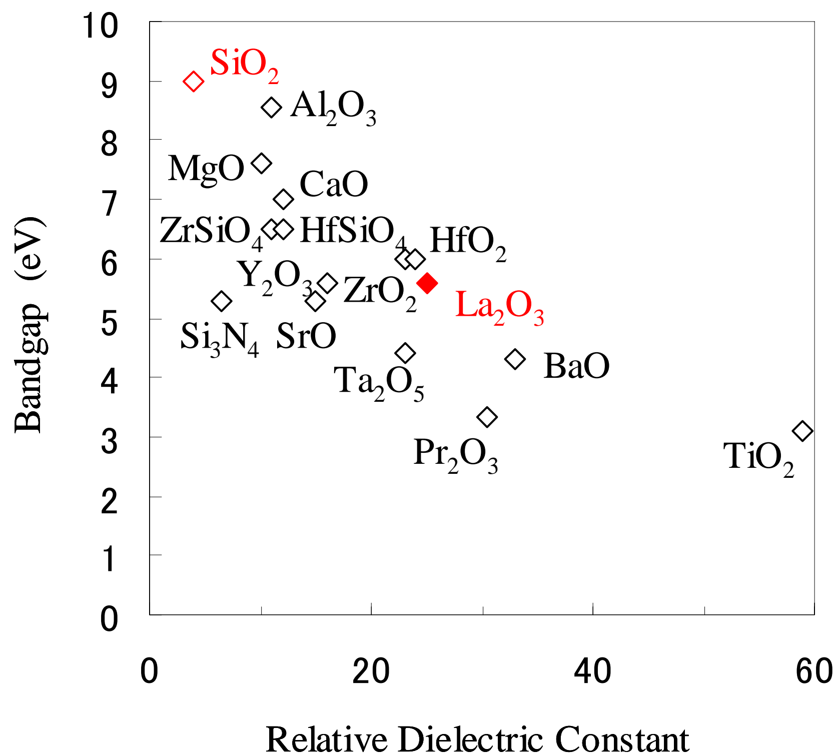


Fig.1-3 Bandgap vs. relative dielectric constant of SiO_2, La_2O_3 and other materials

Figure 1-4 shows the band offsets for high-k dielectrics on Si [11]. Recently, excellent results of rare earth oxides, such as La_2O_3, Ce_2O_3, Pr_2O_3, Gd_2O_3, Dy_2O_3 and their silicate have been reported [32-37]. However, high-k materials including rare earth oxides have many problems such as formation of interfacial layer, interface state, thermal stability and growth micro crystal and moisture absorption.

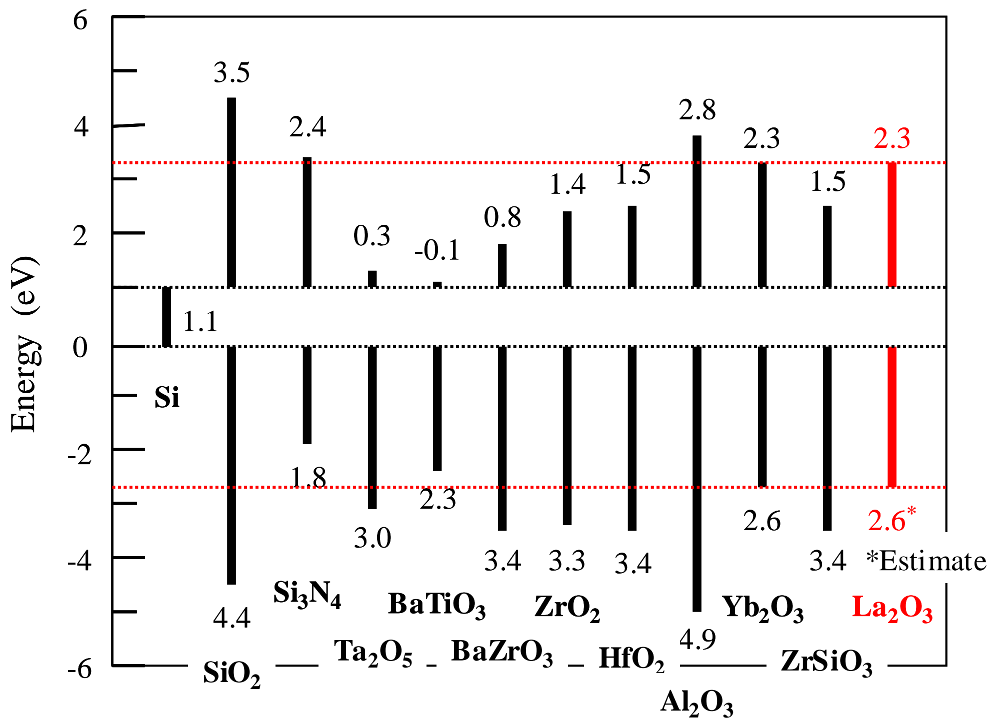


Fig.1-4 Band offsets of SiO_2, high-k materials and La_2O_3 on silicon

Figure 1-5 shows a part of the lanthanides elements. There are 15 elements of atomic numbers are 57 to 71. Here, Pm is an unstable radioactive artificial element and should be removed from the candidates. Lanthanoids are called "*rare earth*" elements, but it should be noted that they are actually no rare in the earth-shell and even their contents are longer than that of Hg, In, Ag, etc.

H He
N O
Al Si
Sc Ti
Sr Y Zr Nb
Hf Ta
Ac

Lanthanoids La Ce Pr Nd Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

Fig.1-5 Periodic table of lanthanide

Although, the outer shell electron configurations are the same for all the lanthanide elements, it was found that the properties of lanthanide oxides are quite different. The bandgap for the lanthanide oxides are shown in Figure 1-6. The reported relative dielectric constants of rare earth oxides are about 10 to 30 and the energy bandgap is about 2.4 to 5.5 eV. Rare earth oxides have good properties and are expected for next generation insulator.

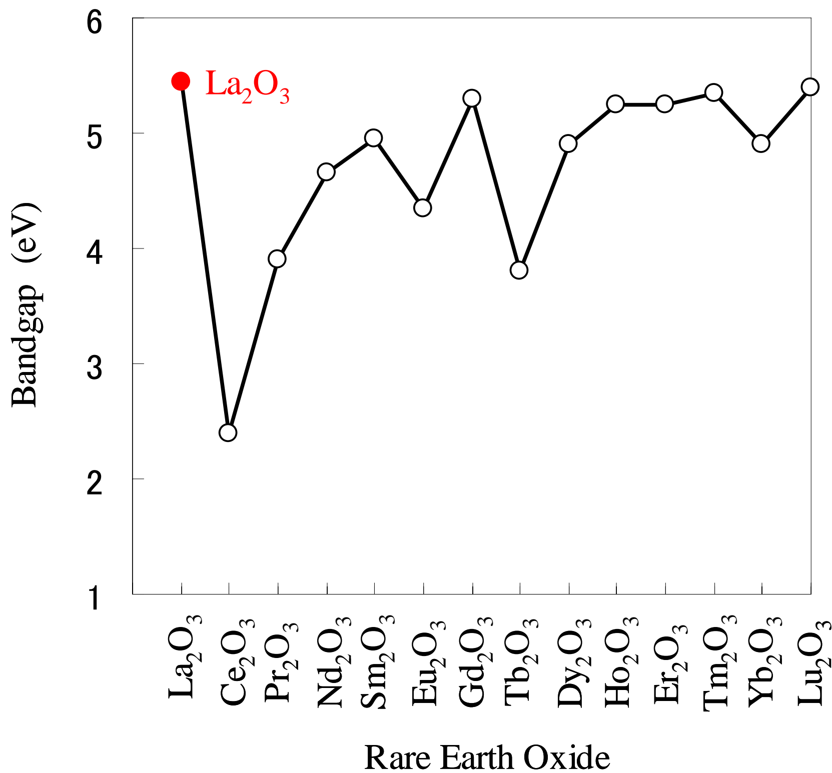


Fig.1-6 Bandgap of rare earth oxides

1.3 Conduction Mechanism

1.3.1 Schottky (SK) Conduction

The Schottky effect is the image-force-induced barrier for charge carrier emission with an applied field [3]. Figure 1-7 shows potential barrier at the metal-vacuum interface. Maximum barrier height is reduced to image-force effect when an electric field is applied. This can help the emission of thermally activated carriers from the metal electrode, which is called Schottky emission. This type of carrier emission is completely analogous to thermionic emission expect that the applied field lowers the barrier height. Metal-vacuum system seen in Figure 1-7 is also equivalent to metal-insulator system as well as semiconductor-insulator system, expect for the dielectric constant of vacuum part.

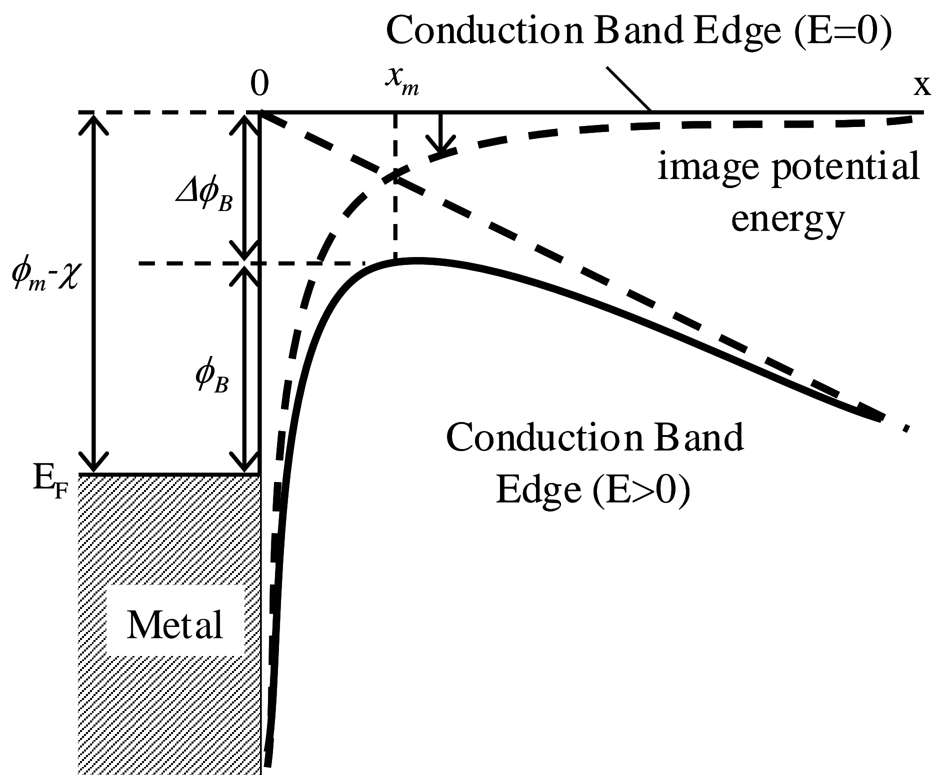


Fig.1-7 Band-Energy diagram between a metal surface and a vacuum

The main feature of Schottky emission is Schottky barrier lowering (or image-force lowering) [3];

$$\Delta\phi_B = q\sqrt{\frac{qE}{4\pi\varepsilon}} \quad \text{(Eq.1-2)}$$

Permittivity ε should be replaced by an appropriate permittivity characterizing the medium. Since carrier emission occurs at much higher energy levels than Fermi level oh the injecting electrode, tunneling probability can be regard as 1. So Tunneling current is

$$J = \frac{4\pi m^* q}{h^3} k_B{}^2 T^2 \exp\left(-\frac{E_m - E_F}{k_B T}\right)\left[1 - \exp\left(-\frac{V}{k_B T}\right)\right] \quad \text{(Eq.1-3)}$$

$$E_m - E_F = \phi_0 - \left(\frac{qE}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2} \quad \text{(Eq.1-4)}$$

Here, h is Plank constant, k_B is Boltzmann constant, E_m is barrier height (ϕ_0=ϕ_m-χ), V is applied voltage. On condition is V>>k_BT, Eq. 1-3 becomes

$$J = \frac{4\pi m^* q}{h^3} k_B{}^2 T^2 \exp\left(-\frac{\phi_0}{k_B T}\right)\exp\left(\frac{\beta_s}{k_B T}E^{1/2}\right) \quad \text{(Eq.1-5)}$$

$$\beta_s = \left(\frac{q}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2} \quad \text{(Eq.1-6)}$$

This J is also called Richardson-Schottky equation.

As expected, the Schottky current is thermally activated process and the activation energy is characterized by Eq.1-4. The activation energy is modulated by applied bias with Schottky barrier height lowering effect. One notice that the barrier deformation decrease as the dielectric constant increase, indicating that, in high-k oxide films, Schottky emission seems to be less probable than in conventional SiO_2 film.

1.3.2 Poole-Frenkel (P-F) Conduction

In MIS (Metal-Insulator-Semiconductor) structure, the P-F and Schottky emission results from the lowering of a Coulomb potential barrier by an applied field. The Schottky is associated with the insulator barrier near to the injecting electrode, whereas the P-F effect is associated with the barrier at the trap well in the bulk of insulator film. Thus, neutral donor traps that is neutral when filled and positive when empty don't experience the P-F effect owing to the absence of the Coulomb potential.

Figure 1-8 shows thermionic emission of trapped carrier in the bulk of the film, which occurs at the trap site. Internal thermionic emission is called P-F emission, while external one is Schottky emission. Another way for emission of electron is hopping process, which is a kind of tunneling process in a short range.

It should be notified here that P-F conduction by P-F emission is closely related to the oxide film thickness while Schottky conduction by Schottky emission isn't related to that, as far as the equal oxide field is concerned.

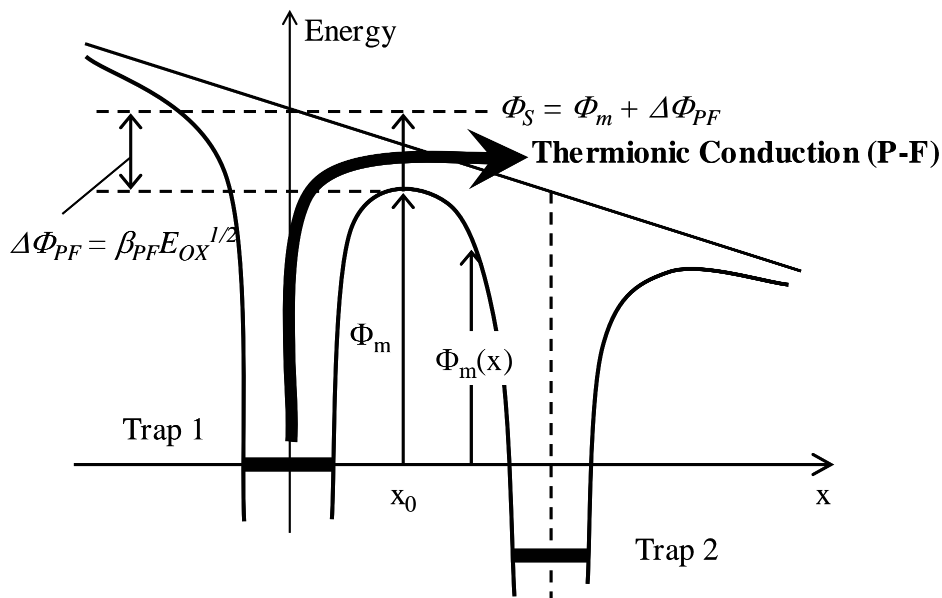


Fig.1-8 Thermionic Condition (Poole-Frenkel Condition)

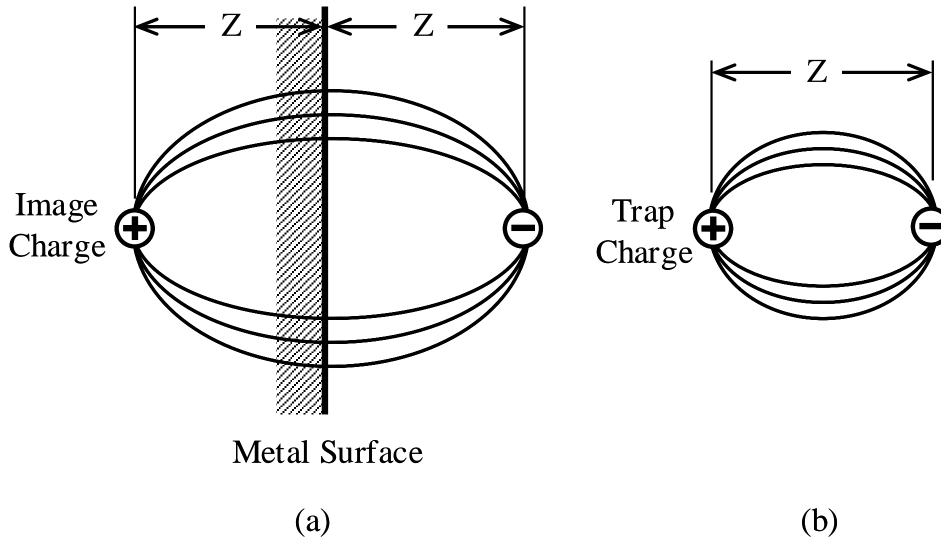


Fig.1-9 Restoring force on escaping electron [6]

(a) The Schottky effect. (b) The Poole-Frenkel effect.

Figure 1-9 shows the restoring force in both Schottky and P-F effect, which comes from Coulomb interaction between escaping electron and a positive charge. The restoring force is due to electrostatic potential that make electron move back to its equilibrium position. Although the restoring force is same of the both, they differ in tha the positive image charge is fixed for the P-F barriers but mobile with Schottky emission. This results in a barrier lowering twice as great for the P-F effect.

$$\Delta\phi_{PF} = \left(\frac{q^3 E}{\pi\varepsilon_0\varepsilon_i}\right)^{1/2} = \beta_{PF} E^{1/2} \qquad \text{(Eq.1-7)}$$

$$\Delta\phi_{SK} = \left(\frac{q^3 E}{4\pi\varepsilon_0\varepsilon_i}\right)^{1/2} = \beta_{SK} E^{1/2} \qquad \text{(Eq.1-8)}$$

In that the electrons have enough energy to go over the energy barrier and travel in the conduction band with a mobility μ which is dependent on the scattering with the lattice, the general expression of the bulk current is expressed by

$$J = qn(x)\mu E \qquad \text{(Eq.1-9)}$$

The concentration of free carrier in the insulator is following.

$$n = N_c \exp\left(-\frac{q(E_c - E_F)}{kT} \right) \quad \text{(Eq.1-10)}$$

Since E_c-E_F is equal to effective trap barrier height including barrier lowering effect described by Eq. 1-7, the effective barrier height and governed by the P-F emission is written by following.

$$E_c - E_F = \phi_{SK} - \Delta\phi_{PF} = \phi_{SK} - \beta_{PF} E^{1/2} \quad \text{(Eq.1-11)}$$

$$J = qN_c \exp\left(-\frac{\phi_{SK}}{kT} \right) \exp\left(\frac{q}{kT} \beta_{PF} E^{1/2} \right) \mu E \quad \text{(Eq.1-12)}$$

1.3.3 Space-charge-limited current (SCLC)

SCLC with localized trap levels in the oxide band is given by following.

$$J = \frac{9}{8}\varepsilon_0 \varepsilon_i \mu \frac{V^2}{L^3} \qquad \text{(Eq.1-13)}$$

Here, ε_0 is dielectric constant of vacuum, ε_i is dielectric constant, μ is carrier mobility, V is applied voltage, L is film thickness. The mobility μ is often found to be strongly field dependence, particularly at high field. SCLC with exponential trap levels is given by following.

$$J = N_c \mu q^{(1-l)} \left[\frac{\varepsilon l}{N_t (1+l)} \right]^l \left(\frac{2l+1}{l+1} \right)^{1+l} \frac{V^{l+1}}{L^{2l+1}} \qquad \text{(Eq.1-14)}$$

Here, N_c is density of states of conduction band, q is electron charge, N_t is total trap density.

1.3.4 Fowler-Nordheim (F-N) Conduction

F-N tunneling occurs when electrons tunnel into the conduction band of the oxide layer. Figure 1-10 (a) shows F-N tunneling of electrons from the silicon surface inversion layer. The complete theory of F-N tunneling is rather than completed. For the simple case where the effects of finite temperature and image-force barrier lowering are ignored the tunneling current density is given by [4]

$$J = \frac{q^3 E}{8\pi h \phi_{OX}} \exp\left(- \frac{4\sqrt{2m^*}\phi_{OX}{}^{3/2}}{3\hbar q E} \right) \qquad \text{(Eq.1-15)}$$

Here, h is Plank constant, q is electric charge, E is electric field in the oxide, ϕ_{OX} is barrier height of the oxide.

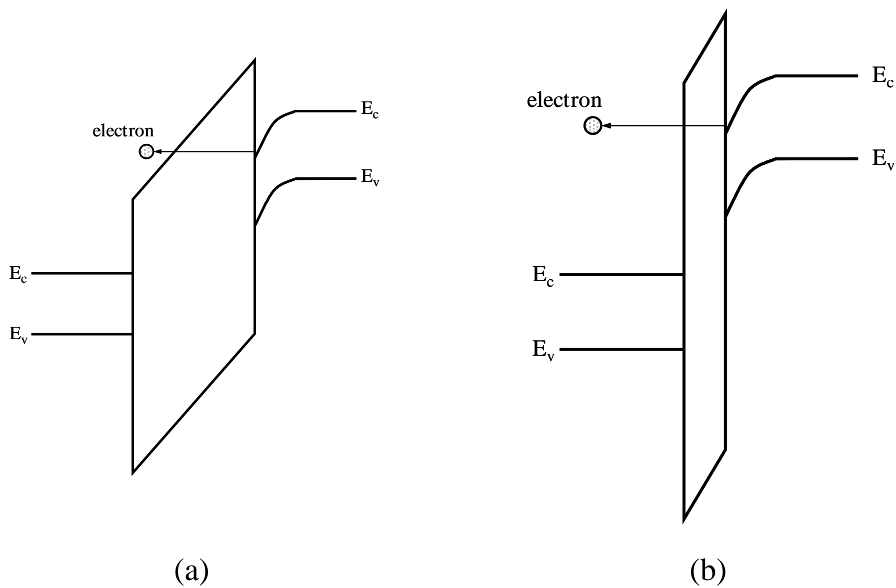


Fig.1-10 (a) F-N tunneling and (b) direct tunneling [2]

1.3.5 Image-force Effect

The abrupt changes in potential at the metal-insulator or insulator-semiconductor interface are physically unrealistic, since abrupt changes in potential imply infinite electric field. The potential changes gradually as a result of the image-force. When electron is at a distance x from the metal, a positive charge will be induced on the metal surface, which is called image charge. The force of emission between the electron and the image charge is equivalent to the force that would exist between the electron and an equal positive charge located at –x. This attractive force is called the image-force given by [3].

$$F = \frac{-q^2}{16\pi\varepsilon x^2} \quad \text{(Eq.1-16)}$$

Here, q is electron charge and ε is the permittivity of the insulator. From the (Eq.1-16), one can realize that attractive force is inversely proportional to the dielectric constant of the film, so that in the high-k film, the effect of image-force will be small. It is worth commenting that the dielectric constant in the image-force equation is the high frequency constant for the electrode-limited conduction case, since electron spend only an extremely short time in the immediate vicinity of the surface in the course of carrier emission.

1.4 Purpose of This Study

In this study, Pt used upper and bottom electrodes. Pt has high work function and high work function is important factor for MIM capacitor because of leakage current of MIM capacitor causes for electron current. Pt is also stability metal-insulator interface for thermal fabrication processes. So, I think that expected interface effect condition characteristics will obtain easily.

La_2O_3 is thought of next generation dielectric for Hf-based materials. La_2O_3 film has similar bandgap of HfO_2, the value is 6eV. But, La_2O_3 has higher band offset for electron, that value is 2.3eV for Si, than other high-k materials such as HfO_2, that value is 1.5eV. La_2O_3 has also high relative dielectric constant value (>27). So, high capacitance density is obtained easily to use La_2O_3 film. So, I think that La_2O_3 is good material for MIM capacitor from following reasons; 1) La_2O_3 has high band offset for electron. Mainly leakage current of MIM capacitor is electron current. 2) High capacitance density is obtained easily to have high relative dielectric constant.

La_2O_3 MIM capacitor is not studied prosperous and good fabrication process is unknown. Therefore, purpose of this study is base study for La_2O_3 MIM capacitor fabrication process. In this study, I study to optimize annealing temperature and annealing condition, mainly.

In this study, upper and bottom electrode is Pt. Pt has a high work function about 5.5eV. Pt is well known that it is hard to form interfacial layer. As use Pt electrode, I thought that characteristics of La_2O_3 film can study well, because La_2O_3 MIS capacitor and transistor has interfacial layer between insulator and silicon interface.

Table1-1 shows requirements in ITRS roadmap for RF MIM capacitor.

Table1 Requirement for MIM capacitor in ITRS Roadmap for RF devices

	2007	2010	2013	2016
Capacitance Density	4 (fF/μm^2)	5 (fF/μm^2)	7 (fF/μm^2)	10 (fF/μm^2)
J/(CV) (fA/(pFV))	7			
VCC α (ppm/V^2) β (ppm/V)	<100			

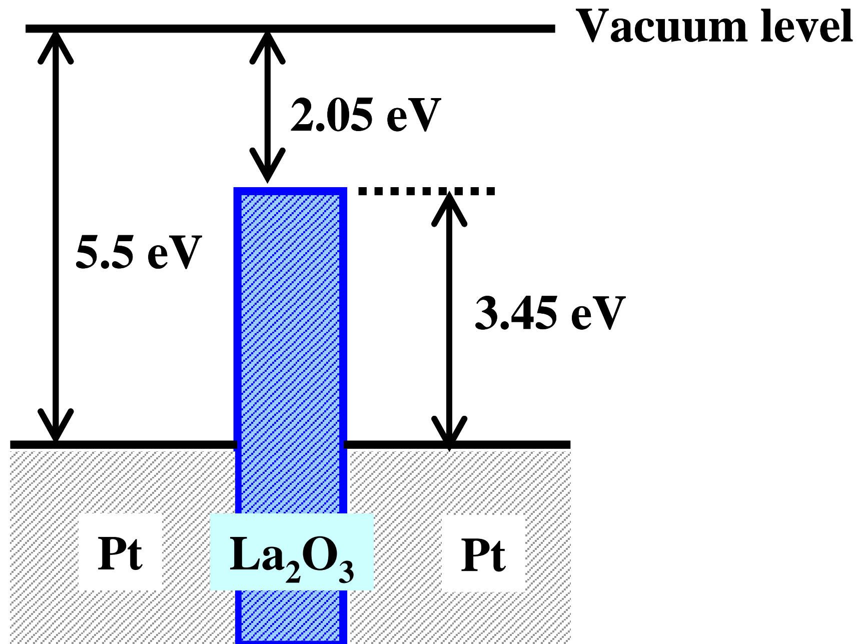


Fig.1-11 Band diagram of Pt/La_2O_3/Pt MIM capacitor in this study

Chapter 2

Fabrication and Characterization Methods

2.1 Si Substrate Wet Cleaning

For deposition of high quality thin film, ultra clean Si surface is required, without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in substrate cleaning is de-ionized (DI) water. DI water is highly purified and filtered to remove all traces of ionic, particle and bacterial contamination. The theoretical resistivity of pure water at $25^{o}C$ is 18.25 MΩcm. Ultra-pure water (UPW) systems used in this study provided UPW with more than 18.2 MΩcm, this is fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the substrate cleaning process was based on RCA cleaning process, was proposed by W. kern et al. But some steps were reduced. First, a cleaning steps in a solution of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2 = 4:1) was performed to remove any organic material and metallic impurities. And then, the native oxide was removed by diluted hydrofluoric acid (HF: H_2O = 1: 99). Finally, the cleaned wafer was dipped in DI water and loaded to chamber immediately.

2.2 E-Beam Evaporation by Molecular Beam Epitaxy (MBE) Method

Figure 2-1 shows E-beam evaporation using MBE method, which was used in this study. There are two chamber, loading chamber and growth chamber, and three type pumps, rotary pump (RP), turbo molecular pump (TMP) and ion pump (IP). In the growth chamber, there are four types of oxide sources in the bottom side. This system can heat substrate holder at the deposition. La_2O_3 film is deposited by the E-beam evaporation in ultra high vacuum growth chamber. Then, since the chamber is maintained at the ultra high vacuum state, the La_2O_3 molecule begins to be evaporated when the temperature of the source is greater than the evaporation temperature. Evaporation temperature is reported as 3620 ^{o}C. And there are crystal meter for measurements thickness.

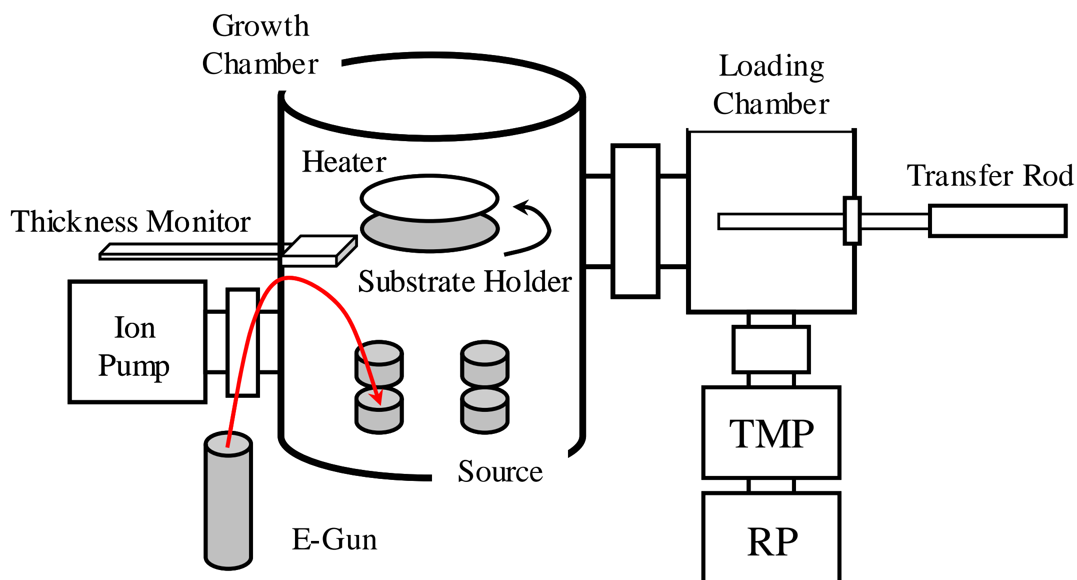


Fig.2-1 E-beam evaporation equipment by MBE method

2.3 Rapid Thermal Annealing (RTA)

In this study, rapid thermal annealing (RTA) is used for thermal treatment after deposition process, post deposition and post metallization. The silica tube is filled with N_2, O_2 and forming gas (3% H_2) in atmospheric pressure after to vacuum in the tube. O_2 annealing system is MILA3000 made in SHINKU-RIKO and N_2 and forming gas annealing system is ULVAC QHC-P610CP made in ULVAC-RIKO. Heat-up rate is 10 ^{o}C per second each systems.

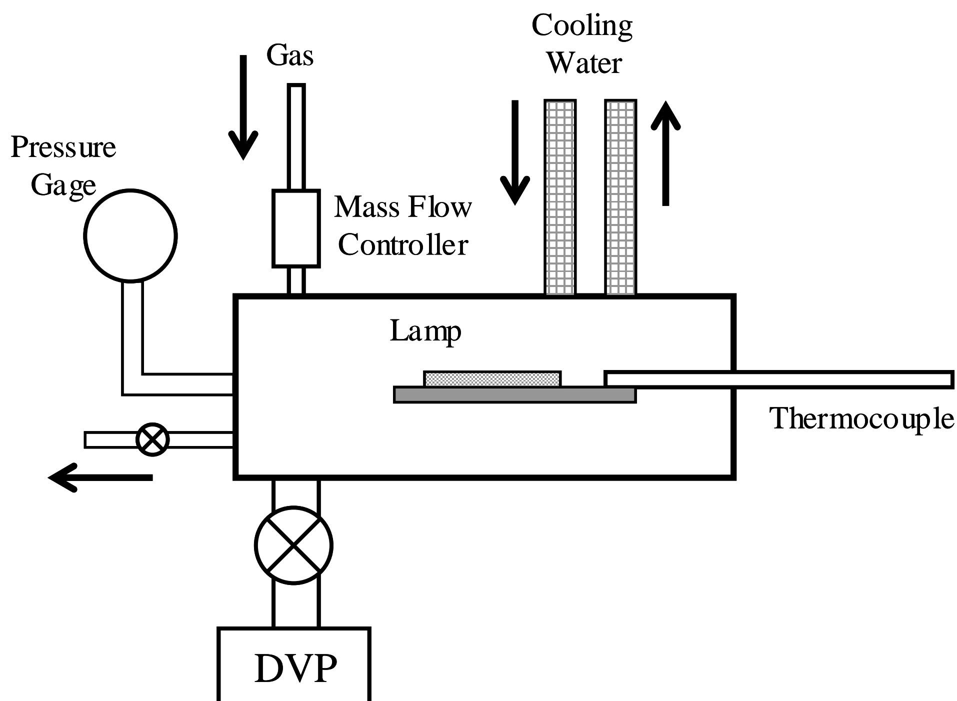


Fig.2-2 RTA system

2.4 Atomic Force Microscopy (AFM)

AFM enables to measure surface morphology by utilizing force between atoms and approached tip. The roughness of sample surface is observed precisely by measurement of x-y plane and z. Figure 2-3 shows the principle of AFM.

Tip is vibrated during measurement, and displacement of z direction is detected. This method is called trapping mode AFM (TM-AFM). Resolution limit for normal AFM is 5 ~ 10 nm depending on distance between sample surface and tip. On the other hand, resolution limit for TM-AFM is depending on size of tip edge. Thus, resolution limit for TM-AFM is about 1 nm.

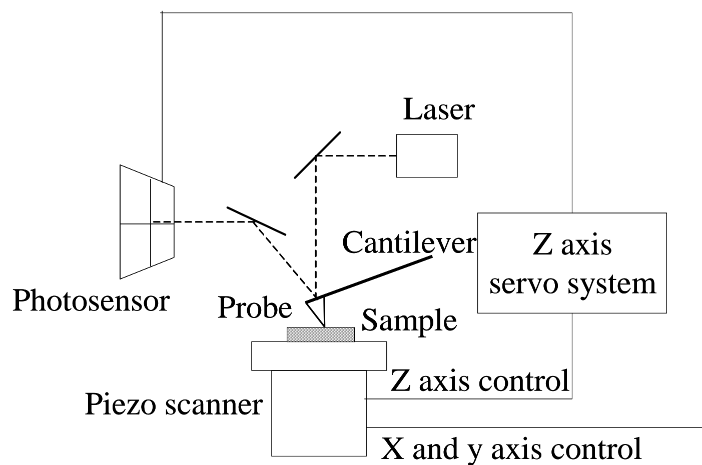


Fig.2-3 Principle of AFM

2.5 Transmission Electron Microscopy (TEM)

Cross-section TEM image is the most important analysis method to characterize physical thickness, film quality and interface condition.

Figure 2-4 Shows TEM system. First, focus lenses change convergent angle and beam size. The electron beam transmitted through the thin fragment sample passes objective lens and projective lens, and finally projected on fluorescent screen. Recording oh the image is performed by direct exposure on exclusive film for electron microscope set lower part of the fluorescent screen.

Electron interacts strongly with lattice by scattering. Thus, sample has to be very thin fragment. Required thickness of the sample is 5 to 500 nm at 100 kV. TEM images are obtained in very high resolution such as 0.2 to 0.3 nm at 200 kV.

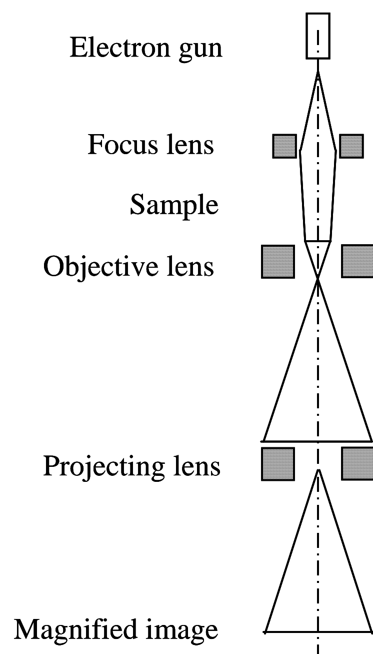


Fig.2-4 TEM system

2.6 Spectroscopic Ellipsometry

Figure 2-5 is principle of ellipsometry. The physical film thickness was optically extracted by Otsuka FE-5000 ellipsometer using a Cauchy model and a single layer approximation. Incident angle was fixed 70°. Photon energy varied from 1.55 to 4.14 eV for data fitting. Energy of 1.55 and 4.14 eV correspond to wavelength 800 and 300 nm, respectively. Film thickness without PDA corresponds to the as deposition film thickness.

Cauchy's distributed type is well applied to the thin left distantly from the absorption domain of a thin film layer, k=0, as an approximation type of wavelength distribution of a typical reflective index. Cauchy's distributed equation is following;

$$n = \frac{A}{\lambda^4} + \frac{B}{\lambda^2} + C \qquad \text{(Eq.2-1)}$$

$$k = 0 \qquad \text{(Eq.2-2)}$$

Here, n is reflective index, λ is wavelength, A, B and C are fitting constant.

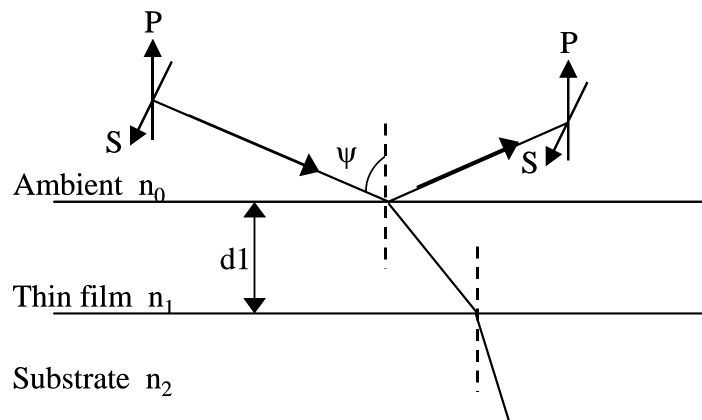


Fig.2-5 principle of Ellipsometry

2.7 Voltage Coefficient of Capacitance (VCC)

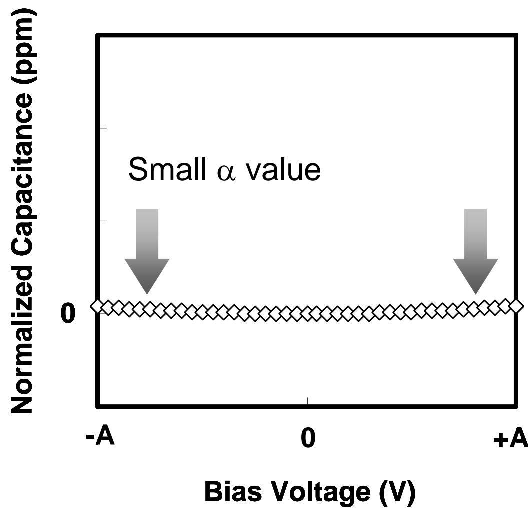
Capacitance-voltage (C-V) characteristics of MIM capacitors' equation is following

$$Q = CV \qquad \text{(Eq.2-3)}$$

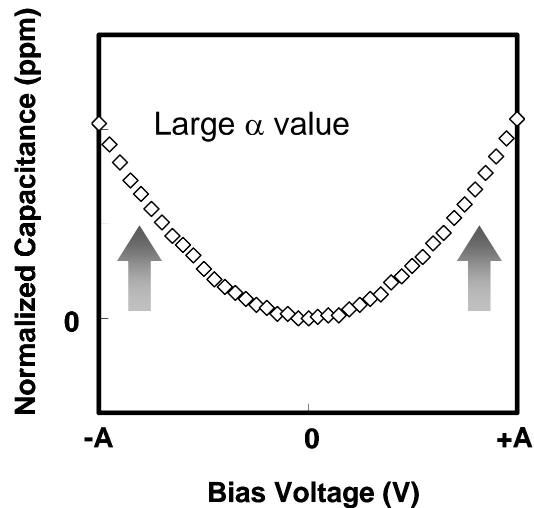
But, in fact, C-V characteristics of MIM capacitors are parabolic characteristics of following [28]. And it is called voltage coefficient of capacitance (VCC).

$$C = C_0(\alpha V^2 + \beta V + 1) \qquad \text{(Eq.2-4)}$$

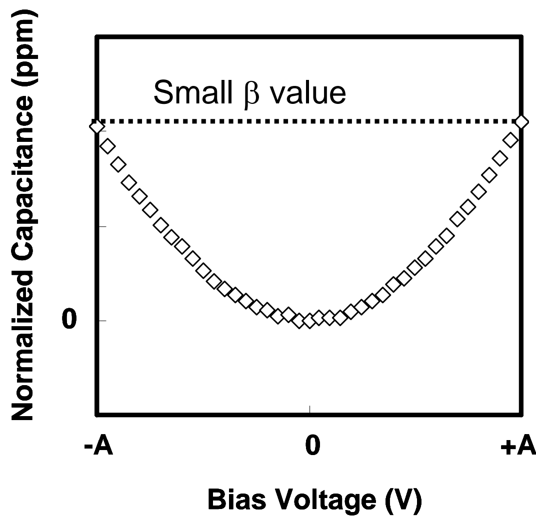
Here, α is quadratic VCC (ppm/V^2), β is linear VCC (ppm/V) and C_0 is capacitance of zero bias voltage. This is important parameter of mixed-analog and RF capacitor and required ITRS roadmap less than 100 ppm/V^2 and ppm/V [1]. SiO_2 has a negative α [14] and HfO_2, Al_2O_3, Ta_2O_5, La_2O_3 etc have a positive α [12-38]. Laminated negative and positive α materials reduced to α value [14]. Figure 2-6 shows typical C-V characteristics of different α and β values. In small α value C-V characteristic, C-V curve becomes close to linear curve. In large α value C-V characteristic, C-V curve becomes the parabolic curve. In small β value C-V characteristic, C-V curve becomes the symmetry curve for zero bias, large β do not.



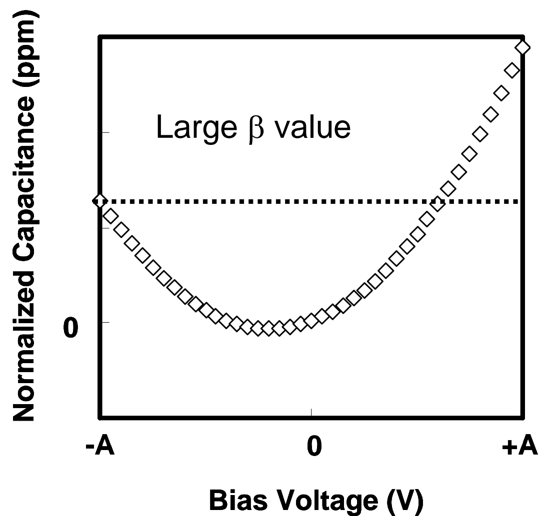
(a) small α value C-V characteristic
At low capacitance density



(b) large α value C-V characteristic
At high capacitance density



(c) small β value C-V characteristic
With PDA and PMA



(d) large β value C-V characteristic
With PDA or PMA

Fig.2-6 typical C-V characteristics of different α and β condition

Chapter 3

Experiment and Characterization of MIM Capacitor

3.1 Fabrication Process of Pt/La_2O_3/Pt MIM Capacitor

The fabrication process of MIM Capacitor shows following figure 3-1. A Pt/Ta_2O_5/SiO_2/Si substrate was contributed from Semiconductor Technology Academic Research Center (STARC). Cleaning process is UPW cleaning at 5min, SPM cleaning at 10 min and UPW cleaning at 10 min. La_2O_3 film was deposited by e-beam evaporation at room temperature. Post deposition annealing (PDA) time was 10 min and gases were O_2 and N_2. Pt upper electrode was deposited by e-beam evaporation at 30 nm. Finally, post metallization annealing (PMA) was same condition of PDA.

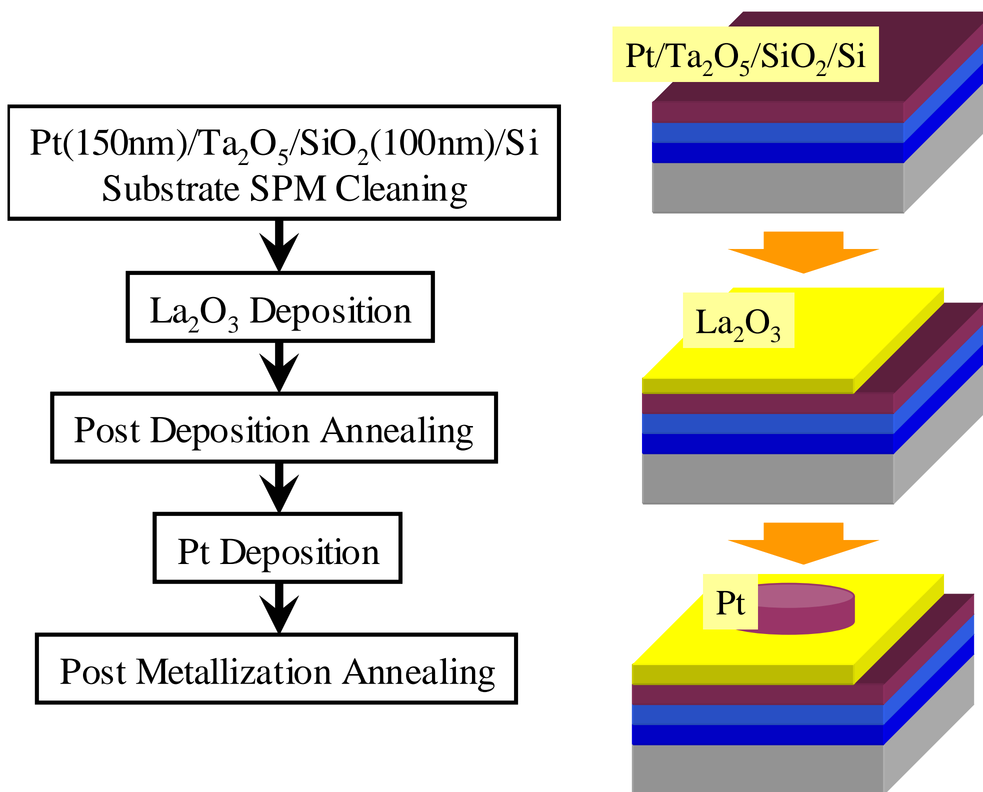


Fig.3-1 Fabrication flow of Pt/La_2O_3/Pt MIM capacitor

3.2 Characteristics of Pt/La_2O_3/Pt MIM Capacitor

3.2.1 Deposition Temperature

First, La_2O_3 film was deposited at 250 ^oC on heating substrate condition and externals looked normal. This condition is the best deposition temperature of La_2O_3 metal-insulator-semiconductor (MIS) capacitor from our study. Since PDA treatment, La_2O_3 deposited area was discolored in from clear to white. Sometimes, this phenomenon was happened in as-deposition samples that have passed long time.

Later fabrication process, deposited Pt upper electrode, have done and measured capacitance-voltage (C-V) and current-voltage (J-V) characteristics. Then, blowing air to remove surface particles, deposited area with Pt upper electrode was flaked out, but Pt upper electrode deposited on without La_2O_3 film didn't. Figure 3-2 shows this phenomenon. This samples La_2O_3 thickness was 50nm, thus heating substrate time at 250 ^oC was two hours.

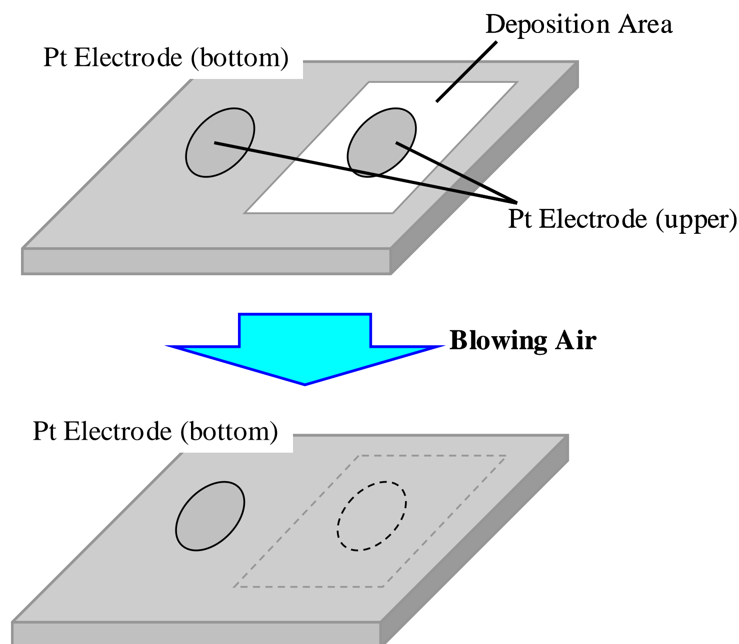


Fig.3-2 Flaked out phenomenon of heating substrate condition

Two reasons were thought of this phenomenon.

First, I thought that heating time was too long. But La_2O_3 thicknesses were 40nm, 30nm, 20nm and 15nm conditions also have happened same phenomenon, colored in from clear to white. In MIS capacitor, this phenomenon wasn't seen in thickness of 15nm condition.

Second, I thought that heating temperature was too higher. Thus, deposition temperature was changed from 250 ^{o}C to 150 ^{o}C. As this condition, same phenomenon was happened. Next, heating temperature have changed from 150 ^{o}C to room temperature, a phenomenon of colored in from clear to white didn't happen. As a result, I thought that heating substrate in deposition process was a bad for the Pt substrate had been exerted.

Therefore, in my following study, deposition temperature was room temperature. This deposition condition is different from MIS capacitor and transistor fabrication processes in our work.

3.2.2 Characteristics of MIM Capacitor

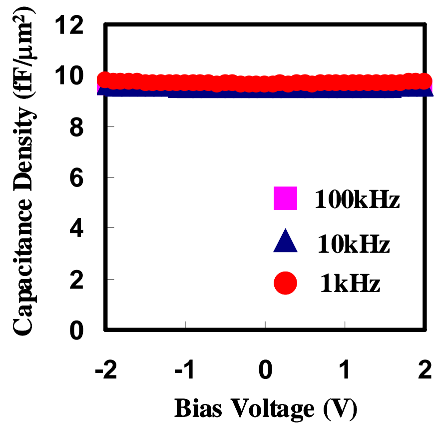
Figure3-3 shows capacitance-voltage characteristics of Pt/La_2O_3/Pt MIM capacitors. These are same thickness of as deposition condition. Capacitance density with annealed is different thickness, respectively. This phenomenon is same as MIS capacitor. This is a densification of La_2O_3 for annealing [42]. PDA (post deposition annealing) and PDA+PMA (post metallization annealing) condition is obtained high capacitance density and a little lower capacitance density for PMA condition. It is thought that only and PDA+PMA conditions are thinner than only PMA condition. On Si substrate, as deposition La_2O_3 thickness is 24.6 nm, N_2 PDA condition is 19.1 nm and O_2 PDA condition is 18.8 nm. But interfacial layers grew on the Si La_2O_3. So, La_2O_3 on the Pt thickness is less than thickness of on the Si La_2O_3. Further, thickness of PDA+PMA condition is changed from PDA condition. For MIM capacitor, O_2 annealing is obtained higher capacitance density than N_2 annealed condition. It is thought that O_2 annealing on the Si is caused of interfacial layer, but O_2 annealing on the Pt don't grow interfacial layer. So, O_2 annealing is improved La_2O_3 film defect, O_2 deficit.

Figure3-4 shows normalized capacitance for zero bias voltage. Here, α and β is following; $C = C_0 (\alpha V^2 + \beta V + 1)$. Quadratic VCC value α is correlation for capacitance density. But linear VCC value β is no correlation for capacitance density. β is correlation for annealing condition. PDA+PMA condition is obtained smaller β value than only PDA or PMA condition.

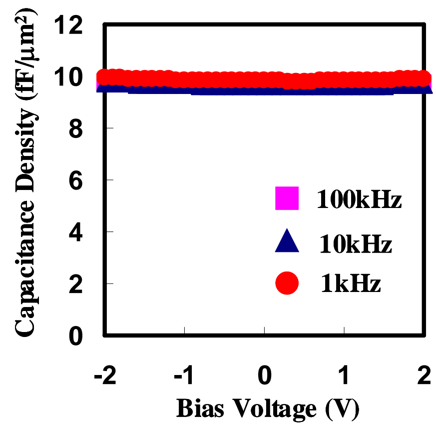
Figure3-5 shows capacitance density-voltage coefficient of capacitance (VCC) characteristics. Both of PDA and PDA+PMA condition were similar capacitance density, but VCC weren't similar. PDA+PMA condition was better value of VCC. This result is thought that upper electrode has a defect and upper Pt-La_2O_3 interface has interfacial

state. This consideration was obtained from Figure3-6, shows capacitance density-leakage current characteristics, and figure3-6, shows leakage current-voltage characteristics. PDA condition is larger leakage current than PDA+PMA condition. PMA condition is considered upper metal-insulator interface improved. But PDA+PMA condition is lower leakage current and higher capacitance density than PMA only condition. I considered this result that only PMA condition is improved upper and bottom interface and arose distortion, at the same time. La_2O_3 film is changed for annealing. PMA that is after PDA condition is smaller physical changes of La_2O_3 film than PMA only condition. So, I considered that best annealing condition is PDA+PMA, first, it was improved that bottom Pt-La_2O_3 interface and changed physical property for PDA. Second, upper Pt-La_2O_3 interface was improved for PMA, this condition is less physical change than PMA only condition so that different characteristics was arose from PMA only condition and PDA+PMA condition.

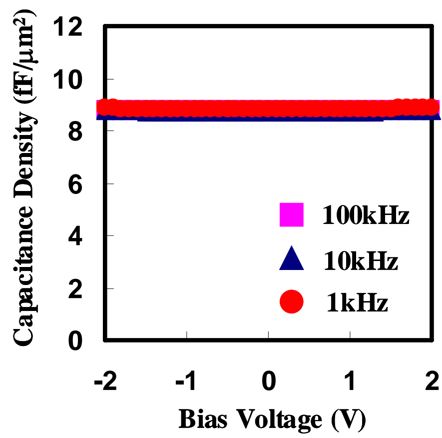
Figure3-7 and 3-8 show temperature characteristics of PDA+PMA condition. Increasing temperature, leakage current increased. Schottky conduction is temperature dependence conduction mechanism. Leakage current increasing is from one to two orders of magnitude 80°C. F-N conduction mechanism has temperature dependence [4]. This is shown in Figure3-7 and 3-8.



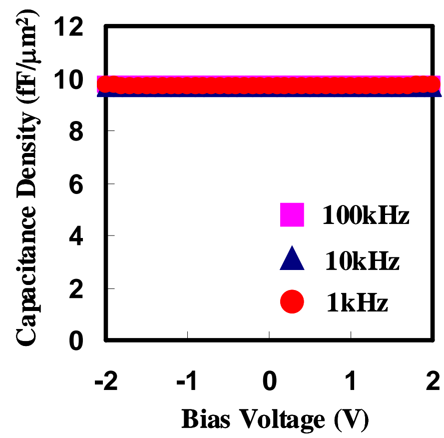
(a) N_2 300°C PDA



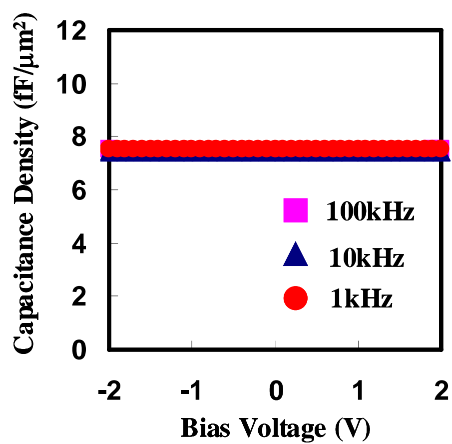
(b) O_2 300°C PDA



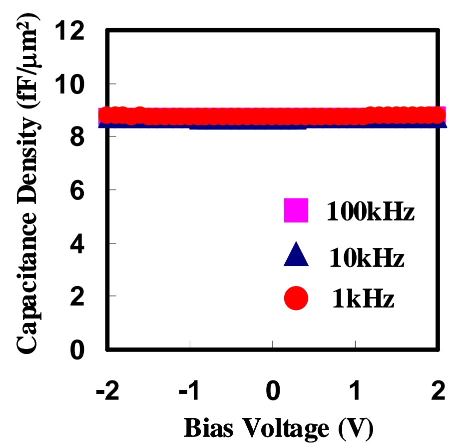
(c) N_2 300°C PDA+PMA



(d) O_2 300°C PDA+PMA

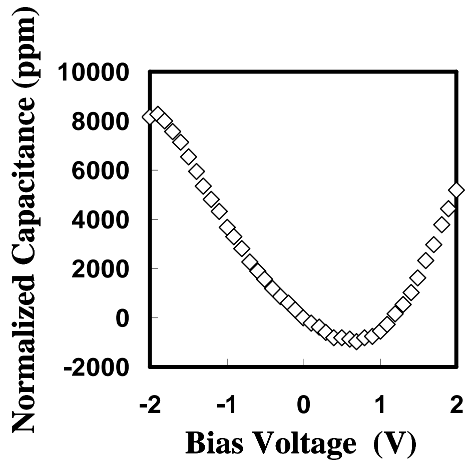


(e) N_2 300°C PMA

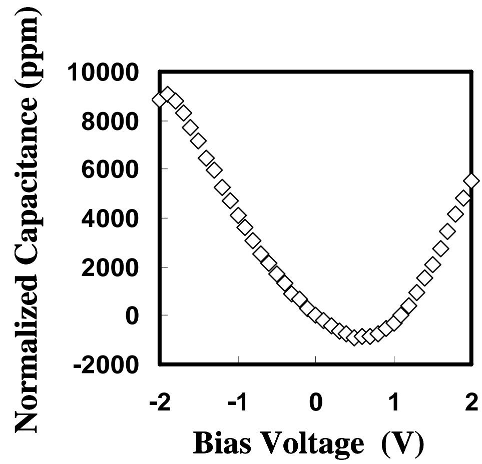


(f) O_2 300°C PMA

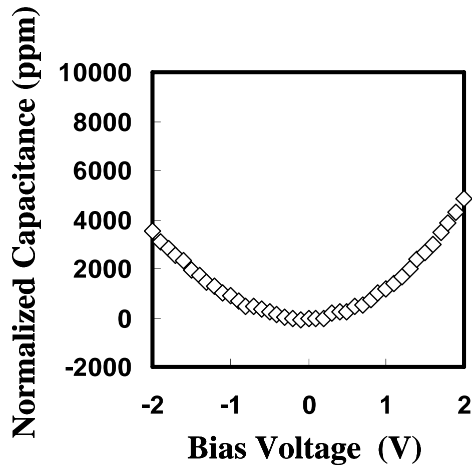
Fig.3-3 C-V characteristics of different annealing gas and condition



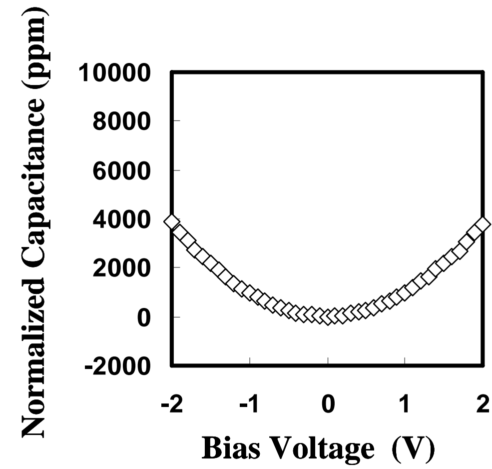
(a) N_2 300°C PDA (C = 9.47 fF/μm²)
α = 1782, β = -1478



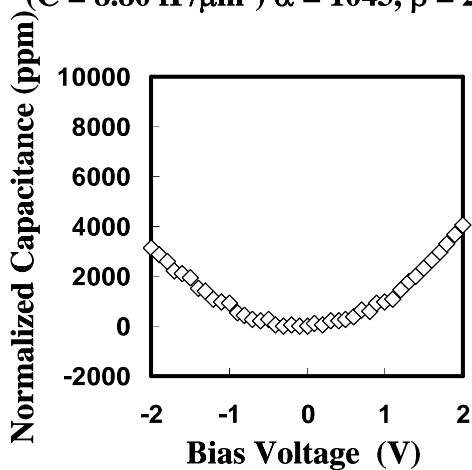
(b) O_2 300°C PDA (C = 9.65 fF/μm²)
α = 1944, β = -1556



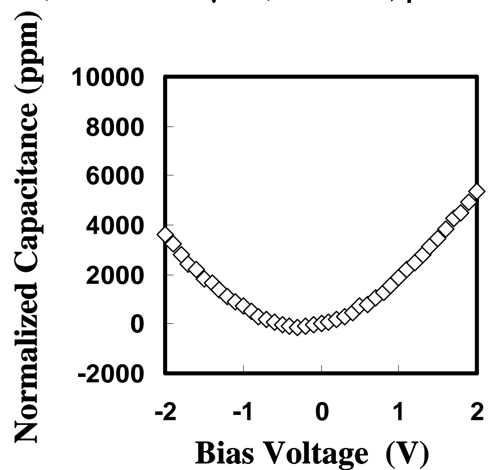
(c) N_2 300°C PDA+PMA
(C = 8.80 fF/μm²) α = 1043, β = 242



(d) O_2 300°C PDA+PMA
(C = 9.73 fF/μm²) α = 946, β = -3.5



(e) N_2 300°C PMA (C = 7.47 fF/μm²)
α = 907, β = 175



(f) O_2 300°C PMA (C = 8.71 fF/μm²)
α = 1311, β = 517

Fig.3-4 Normalized capacitance with different annealing conditions

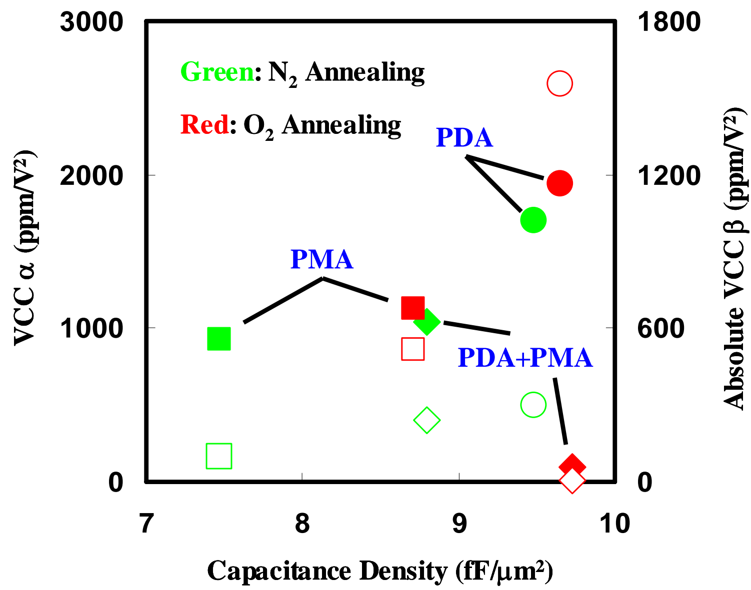


Fig.3-5 VCC vs. capacitance density

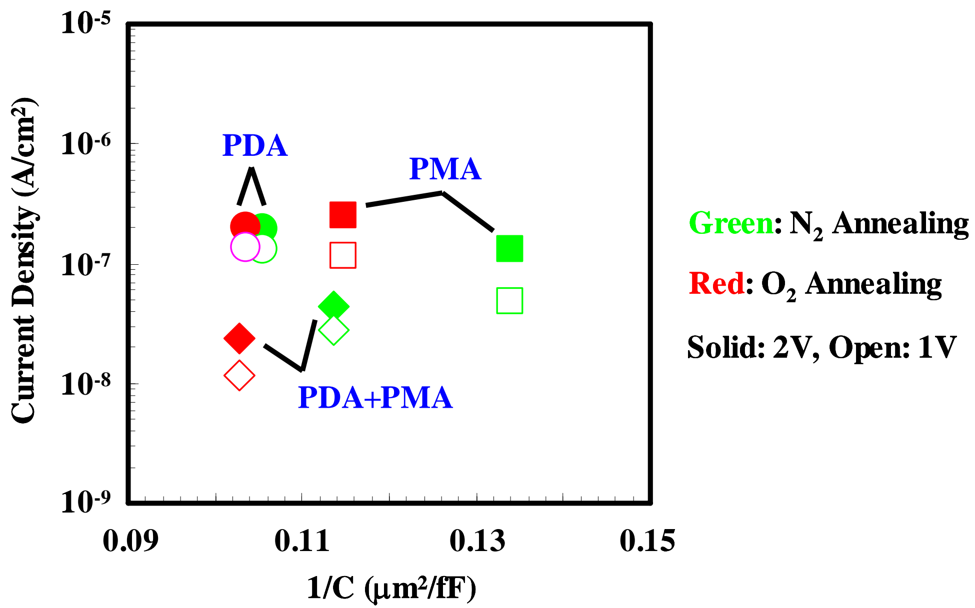


Fig.3-6 Current density vs. 1/C

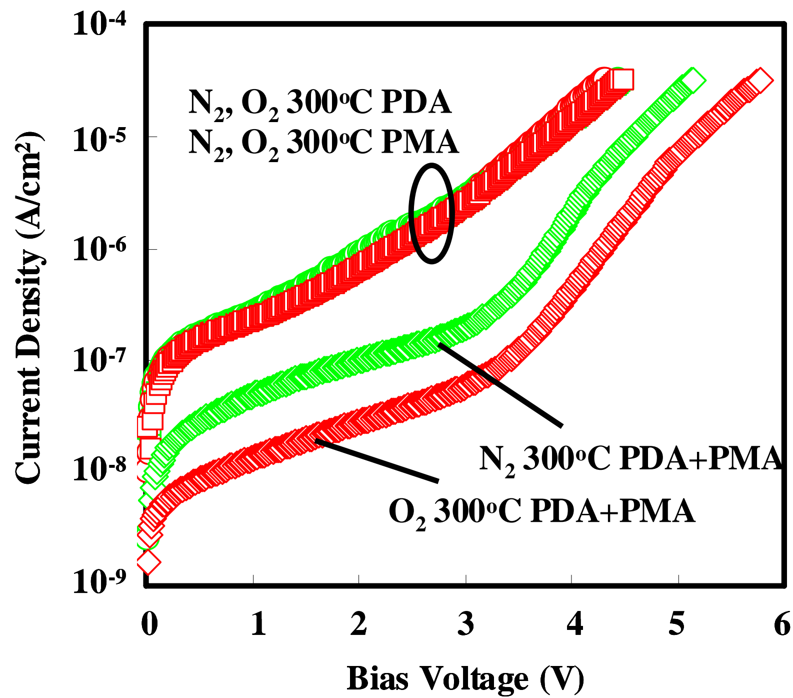


Fig.3-7 Current density vs. bias voltage with annealed condition

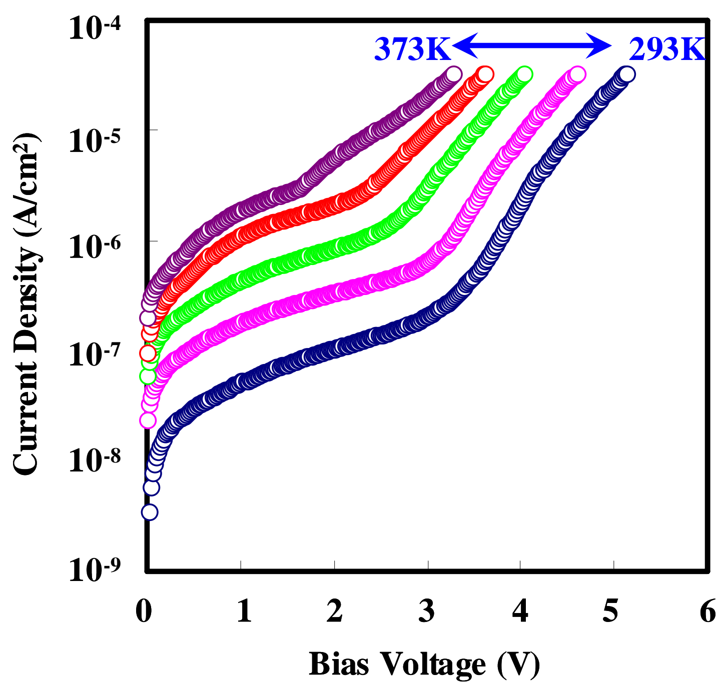


Fig.3-8 Temperature characteristic of N_2 PDA+PMA 300°C

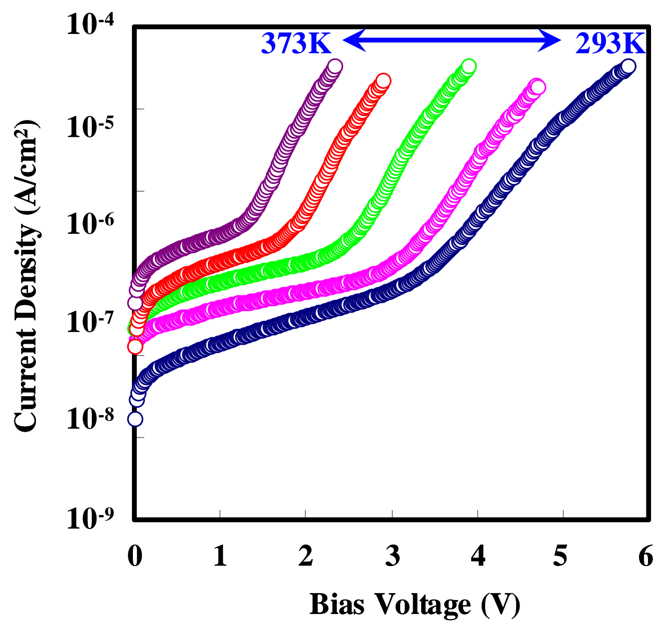


Fig.3-8 Temperature characteristic O_2 PDA+PMA 300°C

3.2.3 Conduction Mechanism

Figure3-9 - 3-14 show conduction mechanisms. La_2O_3 MIM capacitor conduction mechanism is Schottly conduction and Fowler-Nordheim (F-N) conduction mechanism. At low voltage, Schottky conduction mechanism was shown. Pt-La_2O_3 (or La_2O_3-Pt) has high barrier height and film thickness is thick, so mainly conduction mechanism is Schottky conduction mechanism. At high voltage, F-N conduction mechanism was shown. F-N conduction is one of tunneling current. This depends on electric field, in the other hand this depends on film thickness. So, F-N conduction is shown at high field region.

Conduction mechanism of PDA condition both N_2 and O_2 is from Schottky to Poole-Frenkel (P-F) to F-N conduction. P-F conduction mechanism is caused in a trap site of insulator and interface. This is considered that without PMA is remained interfacial state or trap site at La_2O_3 film or upper Pt-La_2O_3 interface. So, P-F conduction is shown for J-V characteristic.

Conduction mechanism of PMA and PDA+PMA condition both N_2 and O_2 are from Schottky to F-N conduction. From this result, treatment of PMA was reduced trap site and interfacial state in upper and bottom Pt-La_2O_3 interface. But only PMA condition, current density is one order larger than with PDA and PMA. Only PMA, it is considered that trap site and interface condition is not improved perfectly.

To obtain low leakage current, it is important that various defect have to be improved. So, with PDA+PMA condition is better annealing condition for Pt/La_2O_3/Pt MIM capacitor to obtain good electrical characteristics.

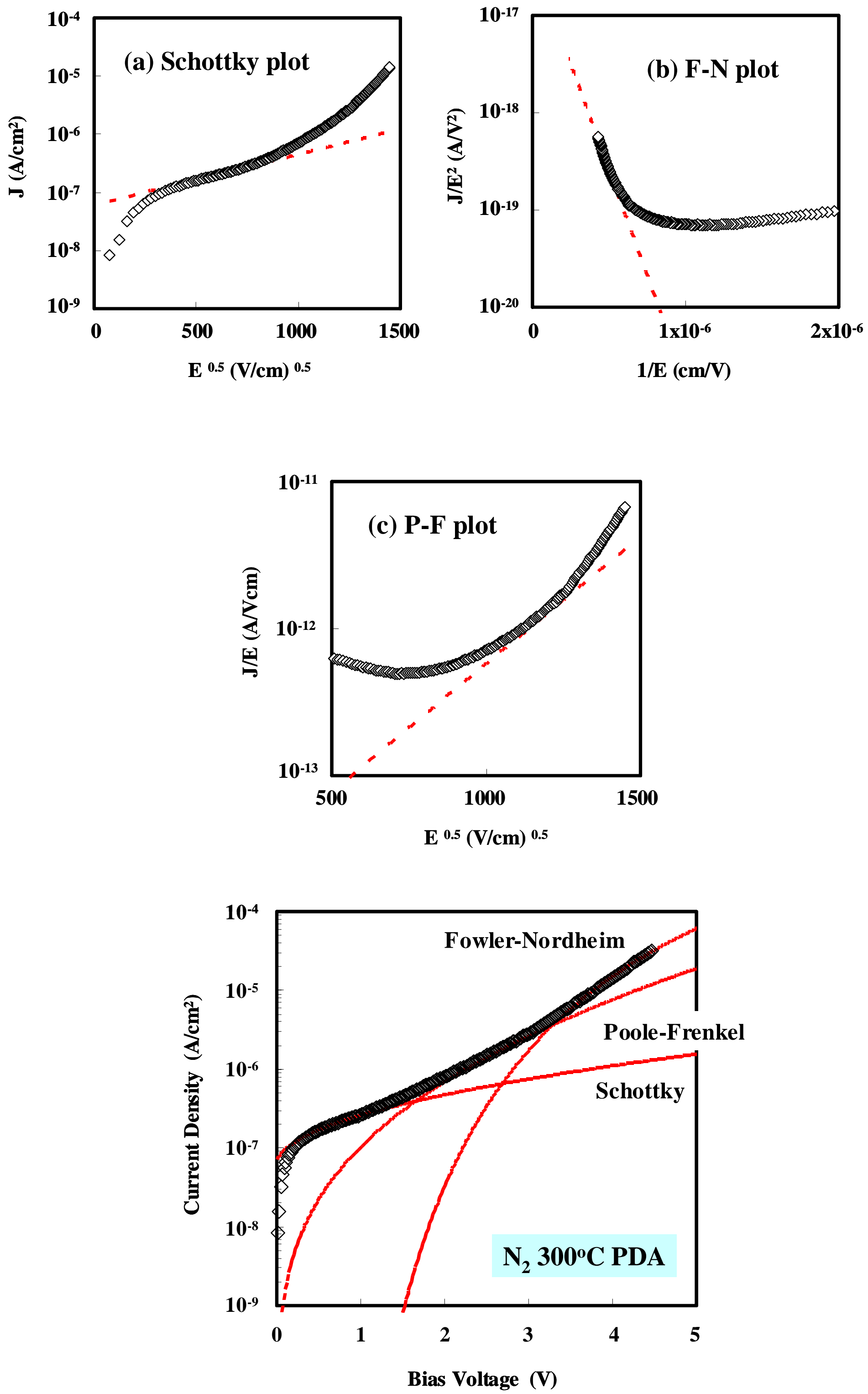


Fig.3-9 N_2 PDA 300°C Conduction

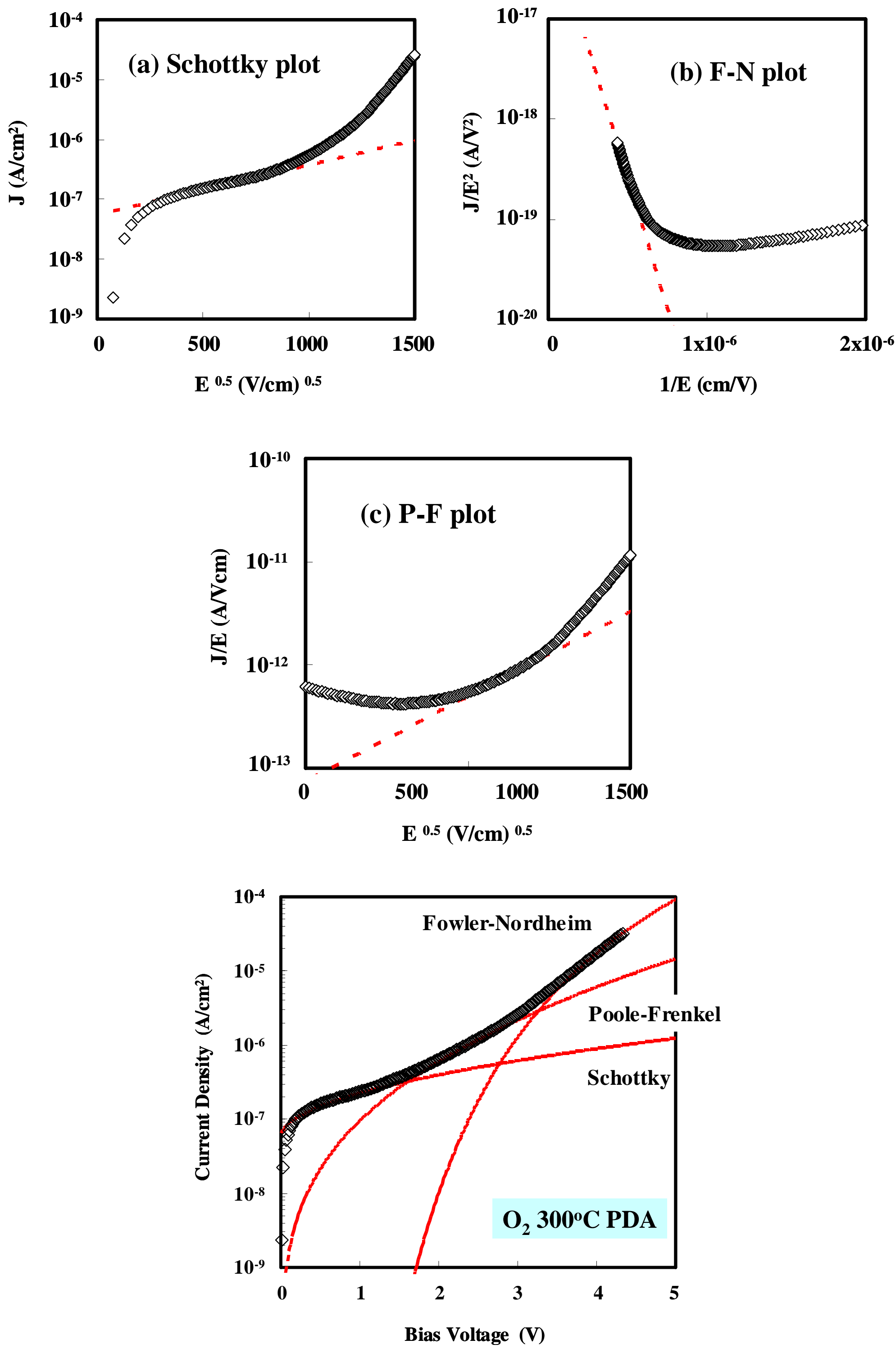
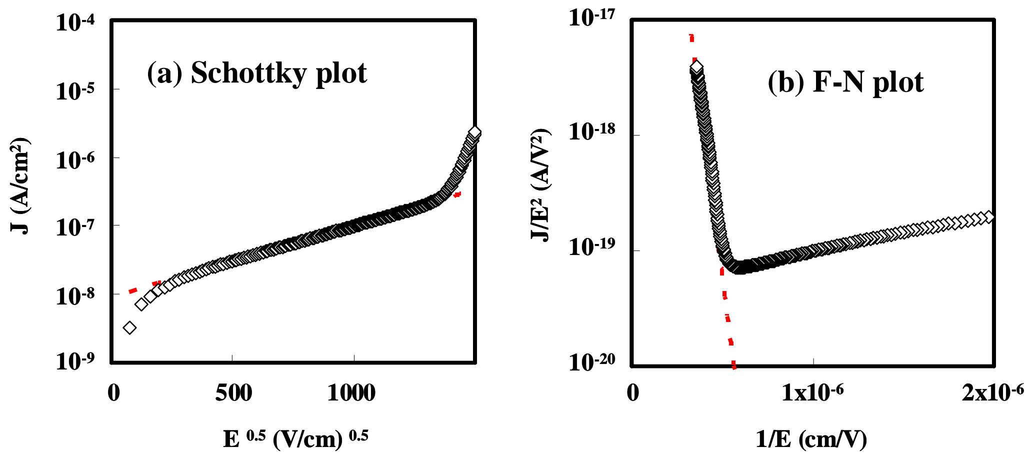


Fig.3-10 O_2 PDA 300°C Condition



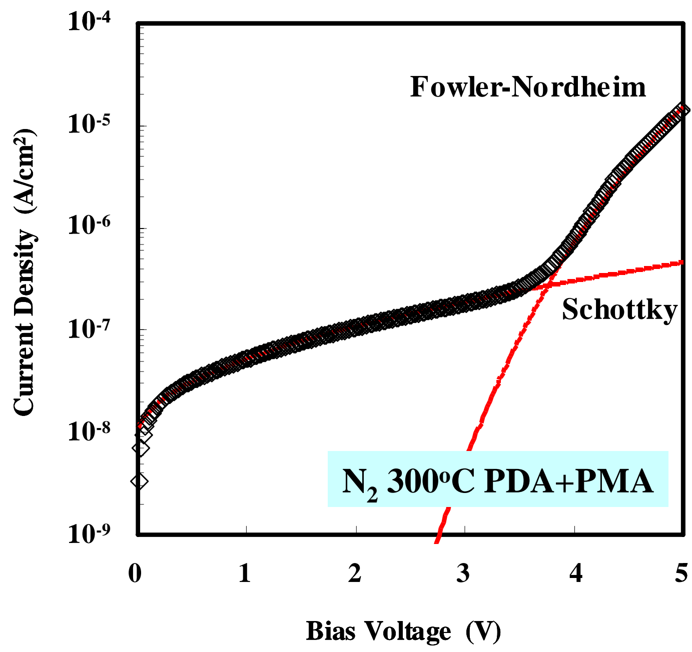
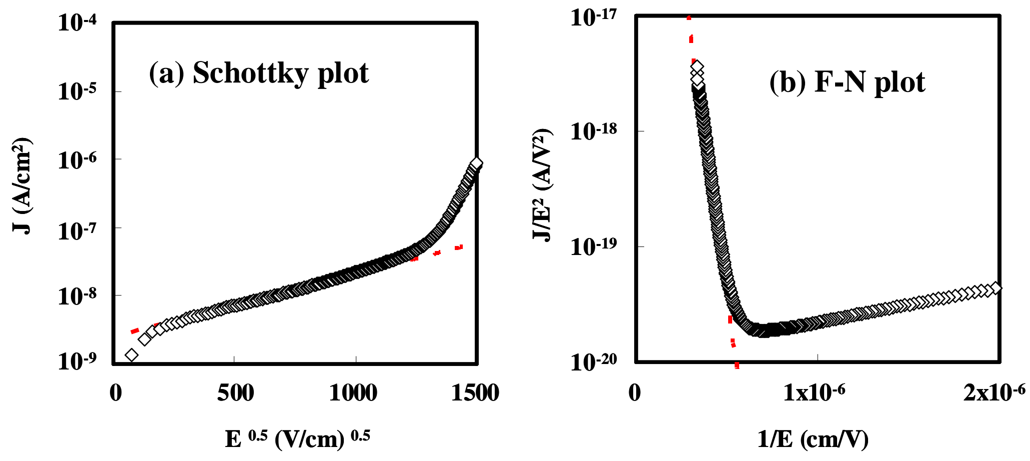


Fig.3-11 N_2 PDA+PMA 300°C Condition



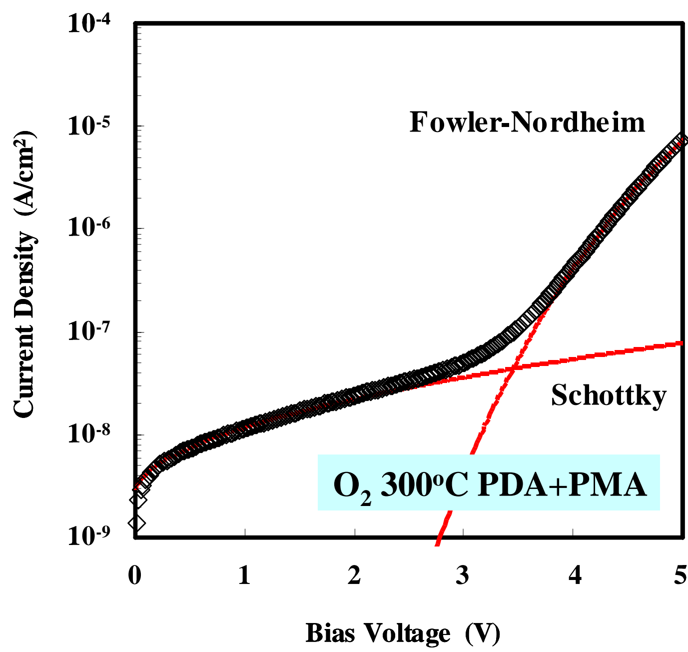


Fig.3-12 O_2 PDA+PMA 300°C Condition

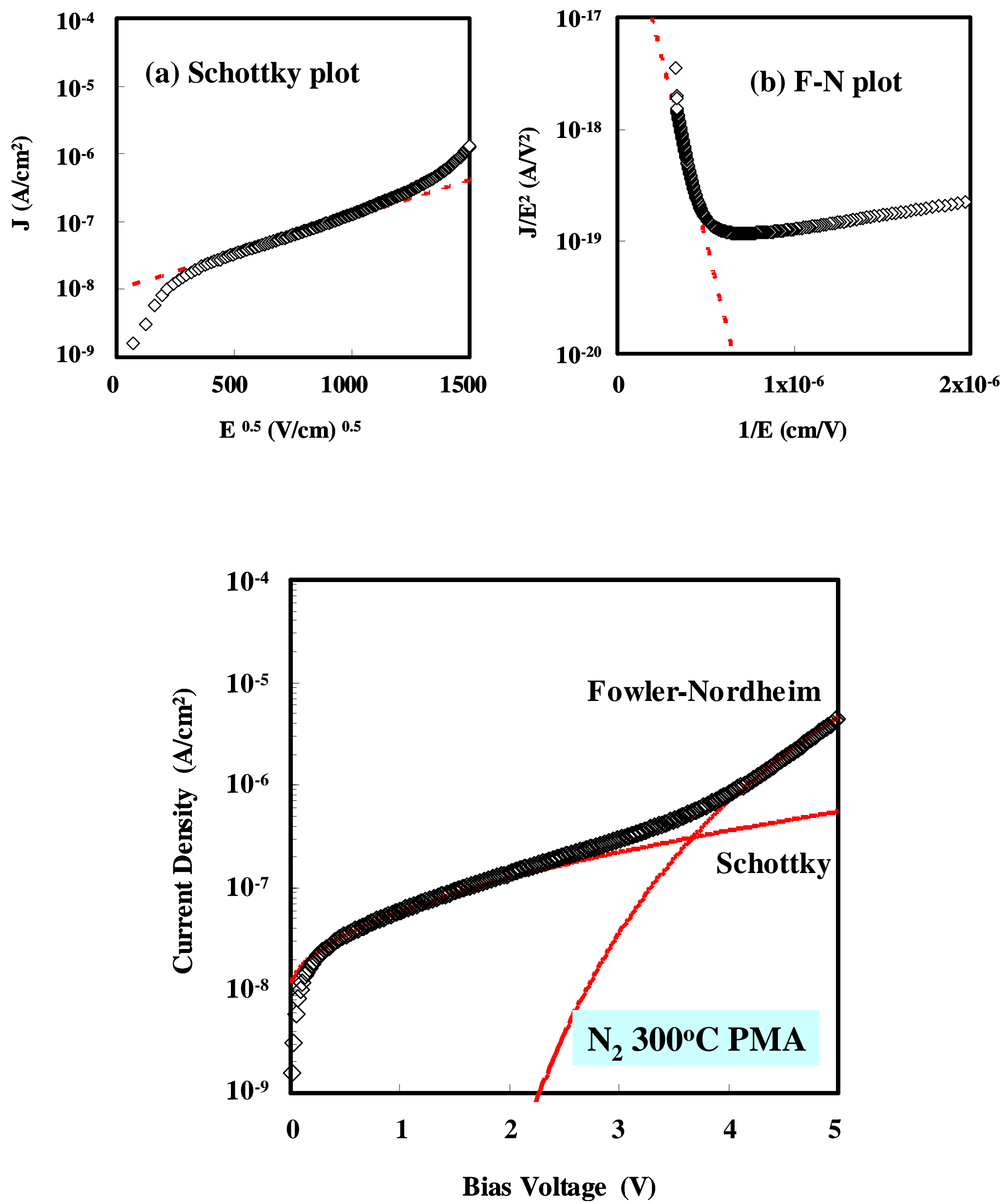
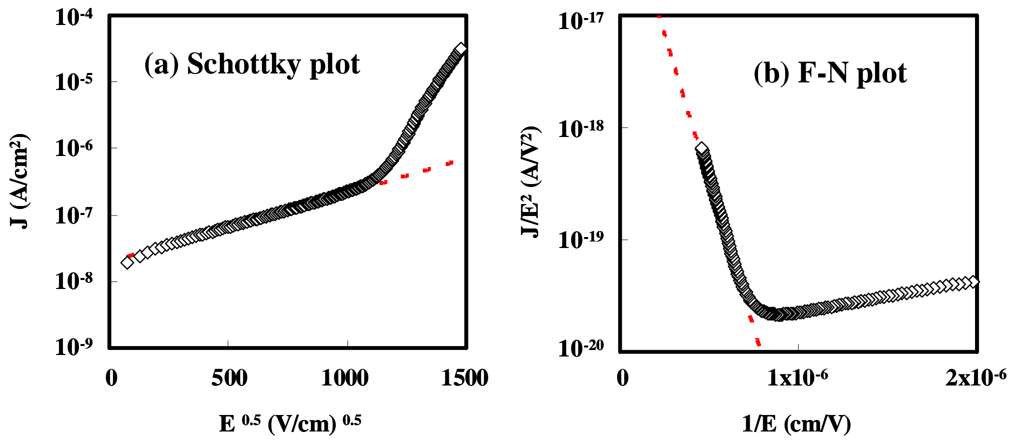


Fig.3-13 N_2 PMA 300°C Condition



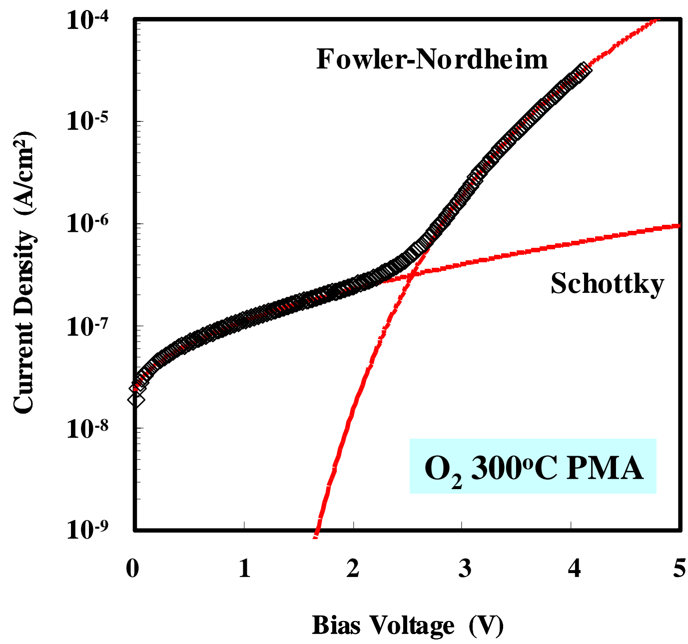


Fig.3-14 O_2 PMA 300°C Condition

3.2.4 Roughness of Bottom Pt Surface

Figure3-15 shows TEM image of 30 nm thickness of La_2O_3 film. Bottom Pt surface has a large roughness from this TEM image. Electrical characteristics were obtained, but value is bad other high-k materials MIM capacitors published previously. And thickness of Pt/La_2O_3/Pt capacitor less than 12 nm, electrical characteristics are not obtained all samples. Current-voltage characteristics are resistance characteristic (ohm conduction). This thickness La_2O_3 on Si, Characteristics of MIS capacitors obtain easily.

To be considered many reasons, the most different thing of Si and MIM substrate is surface roughness. Si surface is very flat, but metal surface is not flat. So, I thought that this is one of this characteristic reason, measured substrate roughness by AFM equipment. Figure 3-16 shows Pt/Ta_2O_5/SiO_2/Si substrate AFM image. Very large RMS value is obtained. In Si substrate, this value is less than 0.5 nm. I guessed that this characteristic reason is substrate roughness for this result. It is thought that roughness is important factor to obtain good electrical characteristics.

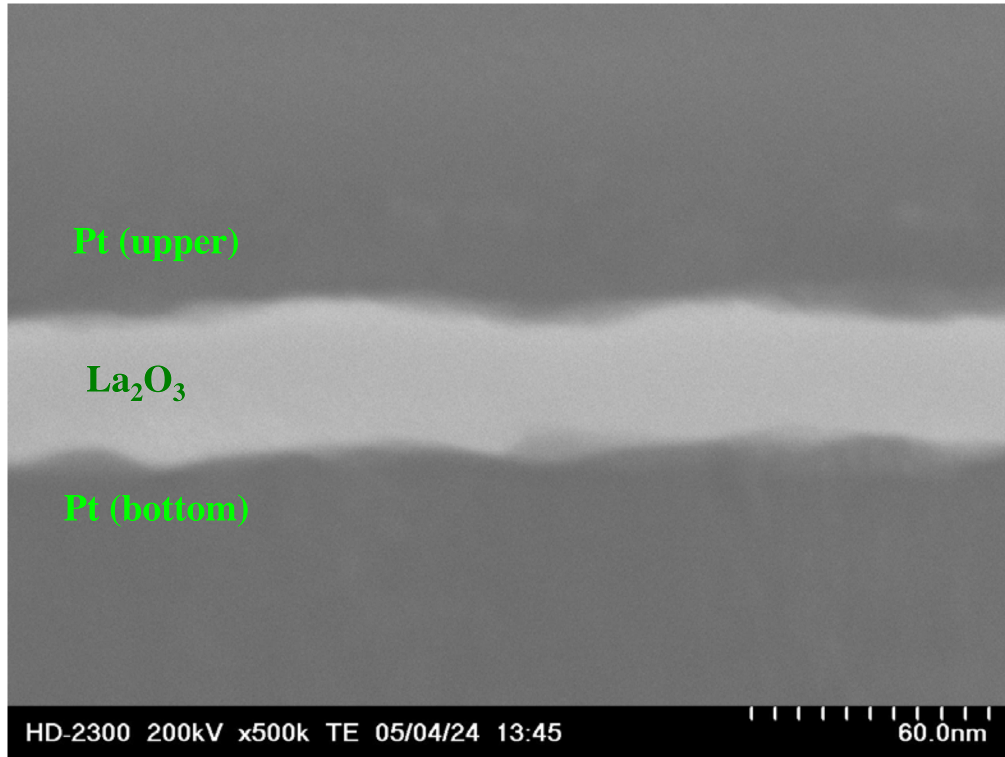


Fig.3-15 TEM image of La_2O_3 MIM capacitor

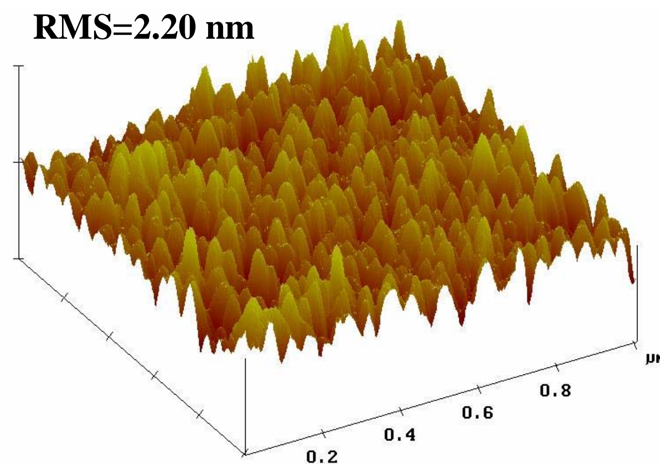


Fig.3-16 AFM image of Pt/Ta_2O_5/SiO_2/Si substrate

New Pt substrate has though to deposit on SiO_2/Si. But Pt-SiO_2 interface is bad accretion. Thus, one layer introduce between Pt layer and SiO_2 layer. I approached Al and W of sputter system. But Al is week for high temperature fabrication process above 500^oC. On the other hand, W is too strong for high temperature fabrication process because of melting point is about 3400^oC (Al is 659^oC). W layer thickness is only a few nm, because of to improve accretion only need a few layer between Pt and SiO_2 interface. In consideration of these, I determine thickness of W layer is 20 nm and Pt layer is 40 nm. This thickness is thick to the final target thickness. Because improve this thick thickness, thin layer is better surface condition. Figure 3-17 shows this condition thickness AFM image. Substrate roughness is improved this condition. Next chapter, thickness of W and Pt are 2 nm and 20 nm, respectively. A thinner La_2O_3 thickness high capacitance density MIM capacitor will fabricate this substrate condition.

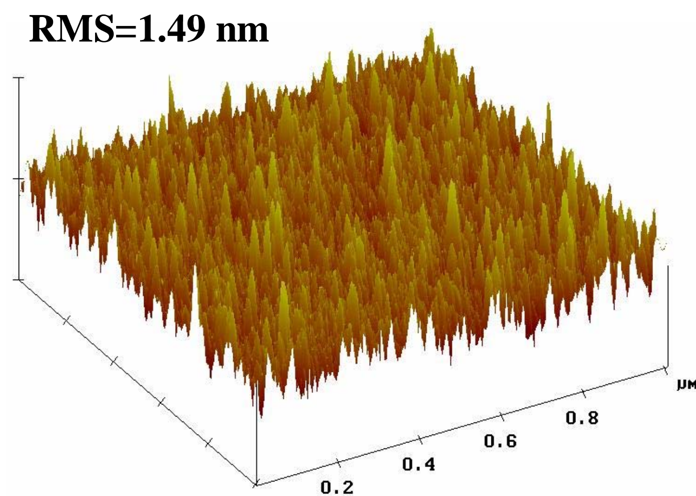


Fig.3-17 Improved substrate AFM image

3.2.5 Summary

In this section, Pt/La_2O_3/Pt MIM capacitor fabricated and demonstrated with Pt/Ta_2O_5/SiO_2/Si substrate. The best deposition temperature for La_2O_3 MIM capacitor is room temperature compared with 300°C deposited. Since same thickness of as deposition, different thickness was obtained for annealing. This phenomenon is same as MIS capacitor [42]. High capacitance density and small VCC values were obtained with PDA+PMA condition. Only PDA or PMA condition is large VCC value, especially β value.

From leakage current-voltage characteristics, with PDA+PMA condition is lower leakage current than PDA only and PMA only condition. I considered only PDA or PMA condition is smaller defects improvement than with PDA+PMA condition. So, with PDA+PMA condition is obtained high capacitance density and low leakage current. Here, only PMA and PDA+PMA seem to be same conditions electrical characteristics is different. But Only PMA condition is not enough to improve various defects.

Substrate roughness is important factor for electrical characteristics. Because thickness that was obtained good characteristics at Si substrate is thick, but electrical characteristics wasn't obtained at MIM capacitor.

3.3 Fabrication Process of Pt/La_2O_3/Pt/W MIM Capacitor

The fabrication process of MIM Capacitor shows following Figure 3-18. SiO_2 film was grown on p-type Si substrate by thermal oxidation at 100 nm. Cleaning process is UPW cleaning at 5 minutes, SPM cleaning at 10 minutes, UPW cleaning at 10 minutes and HF (1%) at 30 seconds. W layer was deposited by sputter system at 2 nm for adhesion layer. Then, Pt bottom electrode was deposited by e-beam evaporation at 20 nm. La_2O_3 film was deposited by e-beam evaporation at room temperature. PDA time was 10 min and gases were forming gas (3%-H_2), O_2 and N_2. Pt upper electrode was deposited by e-beam evaporation at 30 nm. Finally, PMA was same condition of PDA.

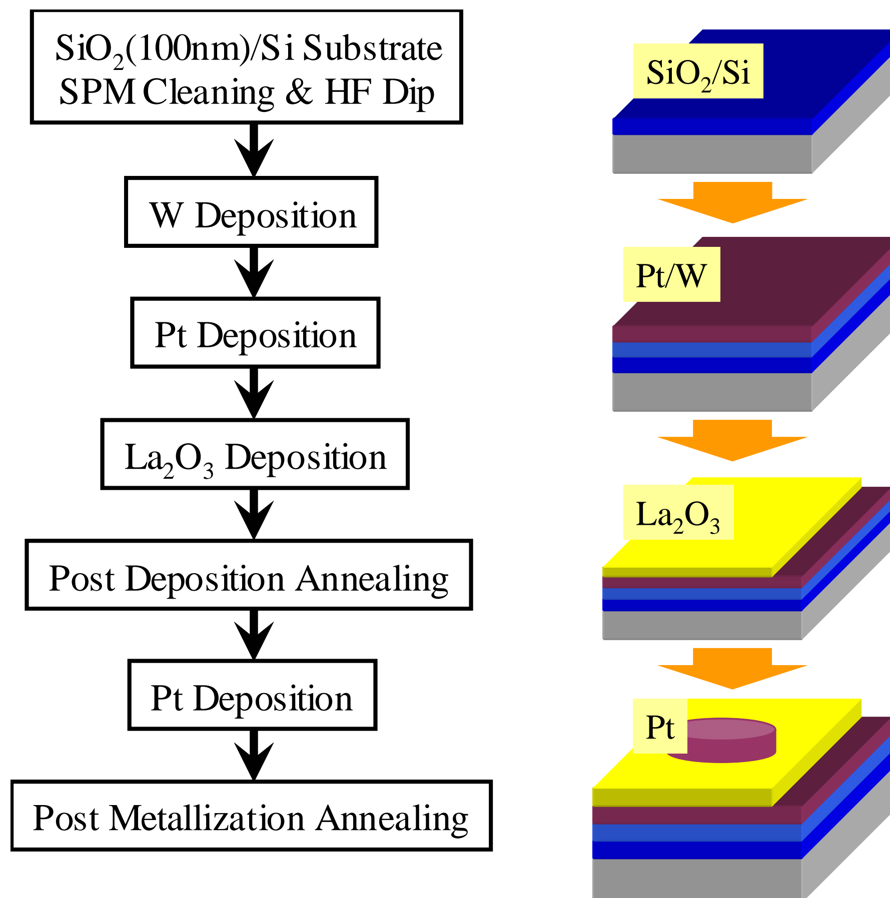


Fig.3-18 Fabrication flow Pt/La_2O_3/Pt/W MIM capacitor

3.4 Characteristics of $Pt/La_2O_3/Pt/W$ MIM Capacitor

3.4.1 Characteristics of MIM Capacitor

At first, substrate roughness is important factor. Because of thinner than last section condition, better characteristics were obtained than last section. Figure 3-19 and 3-20 show TEM image of 300°C and 500°C forming gas annealed sample. Surface roughness is smaller than last section sample in Fig.3-15. In this image, no interfacial layer between Pt and La_2O_3. Thicknesses of these MIM capacitors were 8.7 nm in Figure 3-19 and 7.9 nm in Figure 3-20, respectively. For MIS capacitor, 500°C annealing sample is thicker than 300°C annealing because of interfacial layer is grown at 500°C annealed.

Figure3-21 shows capacitance density-voltage characteristics of different annealing condition. Thickness of as deposition is 12.4 nm. In this section, annealing condition is only with PDA+PMA. In addition to forming gas (FG), annealing gases are N_2, O_2 and FG. Annealing temperature is 300°C and 500°C. Linear C-V curves were obtained all conditions. From Figure3-20, FG annealing condition is obtained highest capacitance density. FG 500°C condition is the highest capacitance density 22.45 fF/μm^2.

Figure3-22 shows bias voltage vs. normalized capacitance characteristics. Symmetry curves were obtained for all condition. With PDA and PMA is good annealing condition for new substrate, $Pt/W/SiO_2/Si$. So, with PDA and PMA annealing needs to reduce various interfacial defects and trap sites in the insulator. 500°C annealing condition characteristics were shown smaller voltage coefficients than 300°C annealing for all annealing condition.

Figure3-23 shows that to be obtained characteristics of the highest capacitance density condition. This condition was in forming gas annealing at 300°C for 10 minutes with PDA and PMA. This capacitance density is the 25.54 fF/μm^2. Leakage current of

this condition is $2.7x10^{-7}$ A/cm^2 at 1V and $6.5x10^{-7}$ A/cm^2 at 2V. This is the smallest leakage current ever published higher than 20 fF/μm^2 MIM capacitor in Figure3-28. In this capacitor, Schottky and F-N conduction mechanism were shown from J-V characteristics. In next section this detail was discussed.

Figure3-24 shows capacitance density-VCC characteristics. FG annealing condition is high capacitance density, but VCC is as same as other annealing condition. Especially, 500°C annealing condition was very low VCC β, less than 100 ppm/V that is required ITRS roadmap, was obtained.

Figure3-25 shows current density-1/C (CET) characteristics. Low 1/C is high capacitance density. Capacitance density is different, but leakage current @1V is as same as different annealing gas. Low leakage current and high capacitance density was obtained with FG annealing condition. N_2 condition is similar leakage current, but capacitance density is smaller than FG annealing condition. One of this reason, I considered difference of La_2O_3 thickness.

Figure3-26 shows current density-voltage characteristics. 300°C annealing condition was larger leakage current than 500°C at low voltage. At high voltage region, 300°C annealing condition was lower than 500°C. Annealing gases were not correlation and temperatures were correlation. This result was different conduction mechanism was shown. Detail of this shows next section.

Figure3-28 shows 1/C vs. current density characteristics of this study data and reference data ever published. These data of dielectric film and top/bottom electrode were different respectively. This study data is obtained very low leakage current for same 1/C. In this study, I used Pt for top/bottom electrode. And other published MIM capacitors used TiN, TaN etc for top/bottom electrode. Pt has the largest work function for these metals. Pt electrode is one of the reason that to obtained low leakage current.

But La_2O_3 film is also the reason to obtained good characteristics. If good characteristics were obtained to change electrode from Pt to others, it is determined that La_2O_3 film is good material for MIM capacitor.

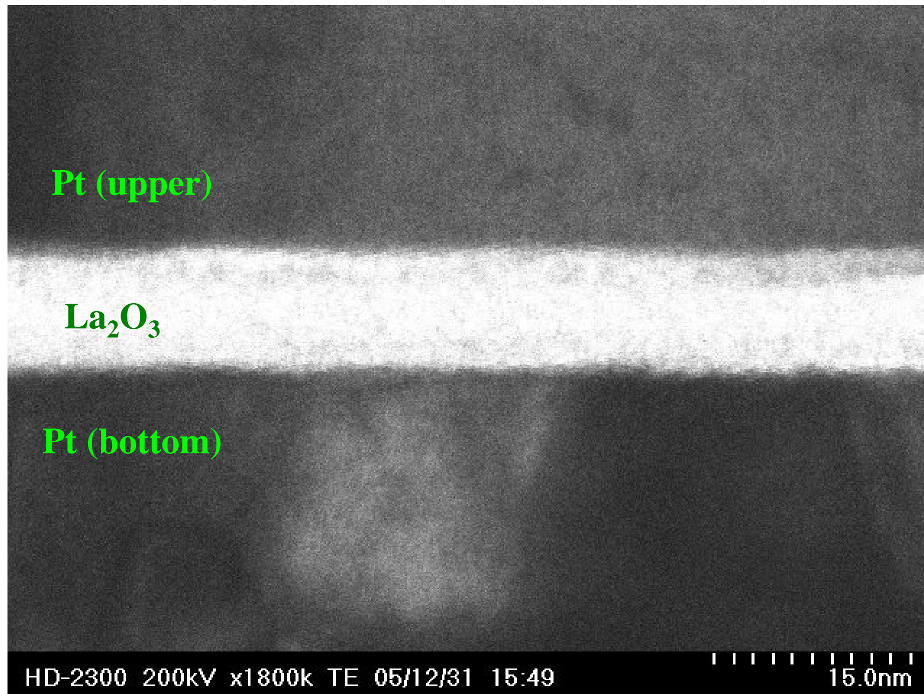


Fig.3-19 TEM image of 300°C annealing sample

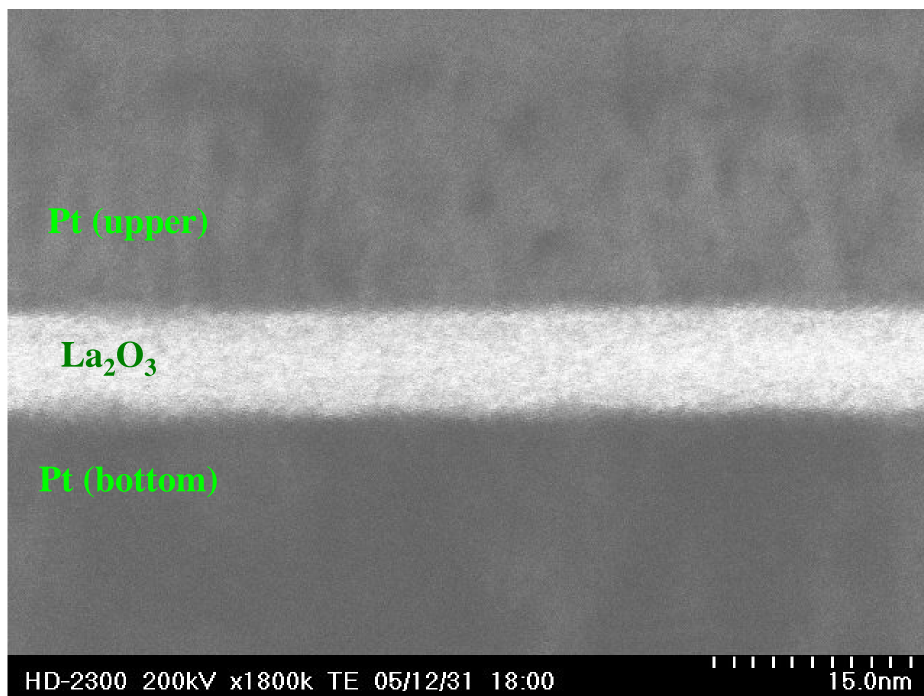
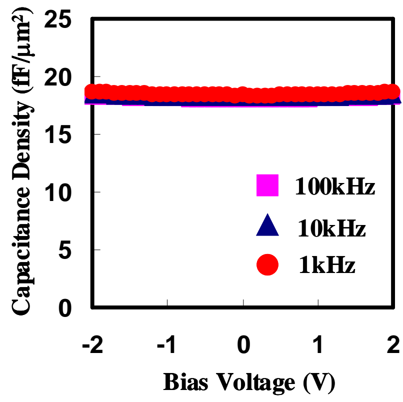
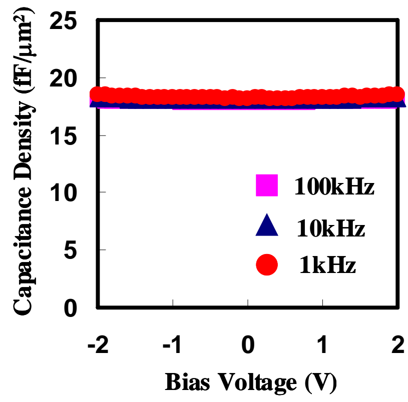


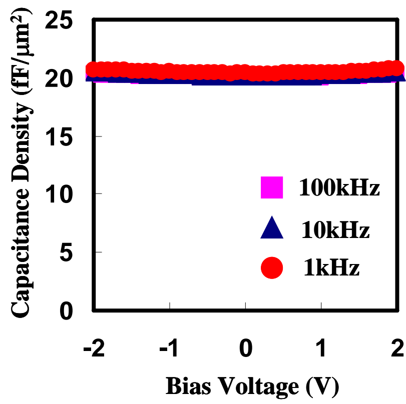
Fig.3-20 TEM image of 500°C annealing sample



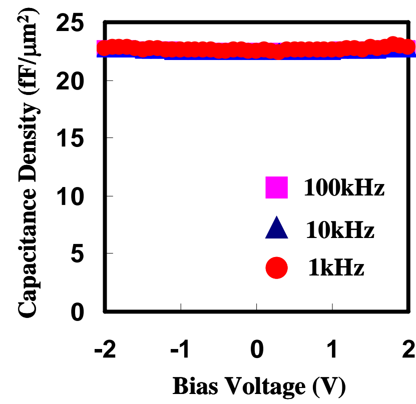
(a) N_2 300°C PDA+PMA



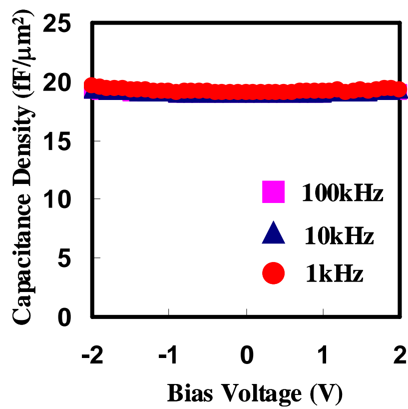
(b) N_2 500°C PDA+PMA



(c) FG 300°C PDA+PMA

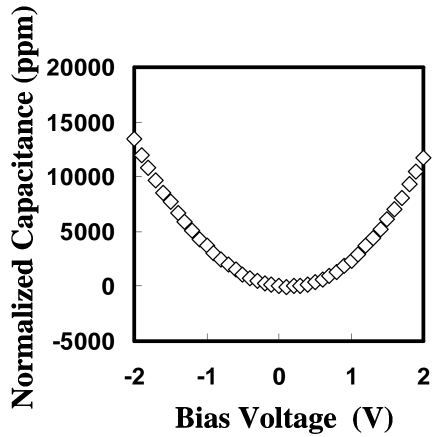


(d) FG 500°C PDA+PMA

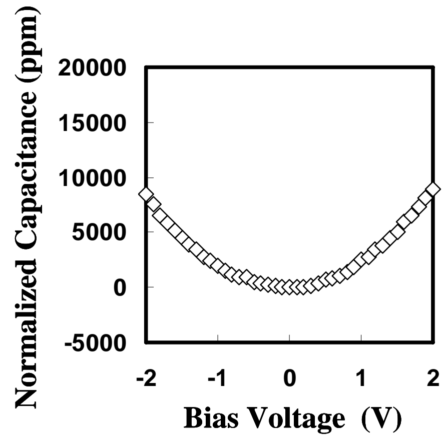


(e) O_2 300°C PDA+PMA

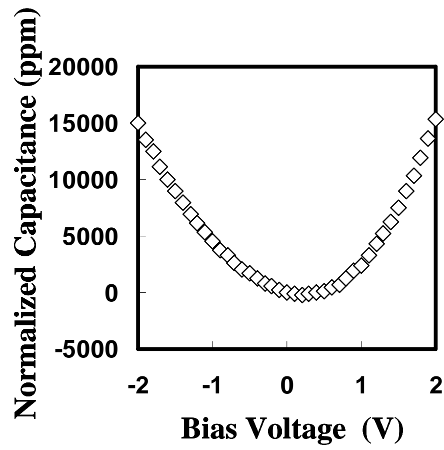
Fig.3-21 C-V characteristics with different annealing condition



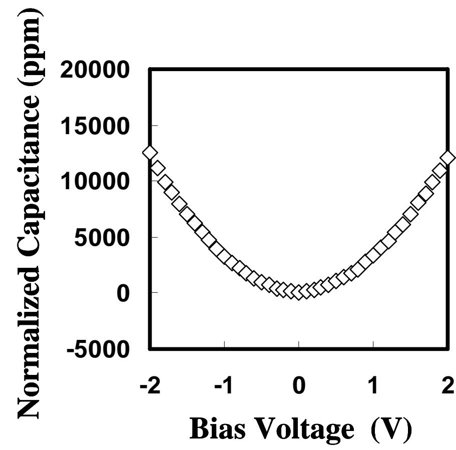
(a) N_2 300°C PDA+PMA
C = 17.98 fF/μm², α = 3118, β = -499



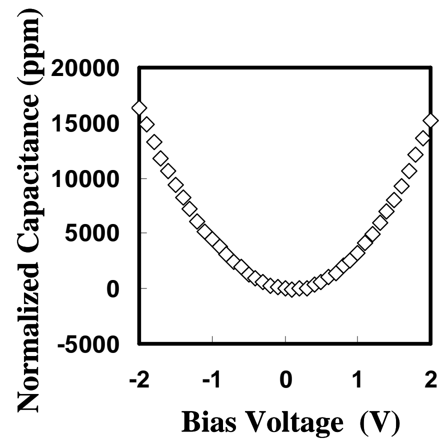
(b) N_2 500°C PDA+PMA
C = 17.83 fF/μm², α = 2159, β = 181



(c) FG 300°C PDA+PMA
C = 19.98 fF/μm², α = 3764, β = -418

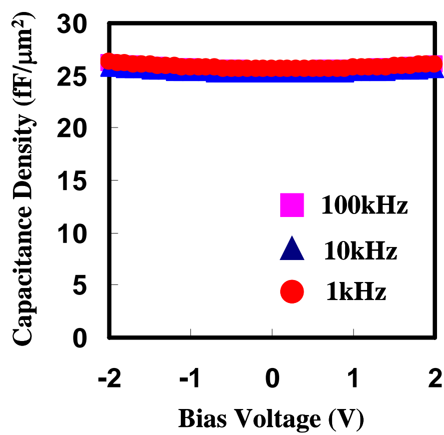


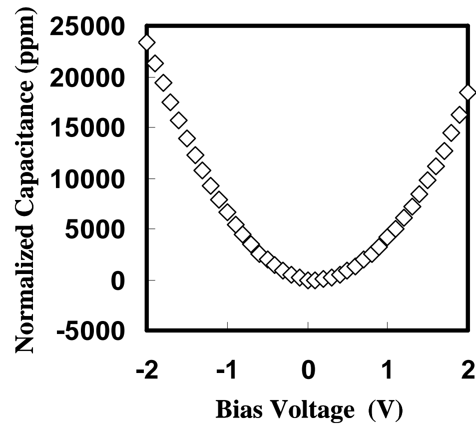
(d) FG 500°C PDA+PMA
C = 22.45 fF/μm², α = 3023, β = -20.9



(e) O_2 300°C PDA+PMA
C = 18.91 fF/μm², α = 3920, β = -421

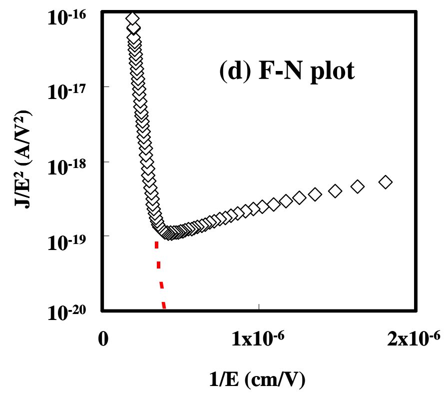
Fig.2-22 Normalized capacitance with different annealing conditions

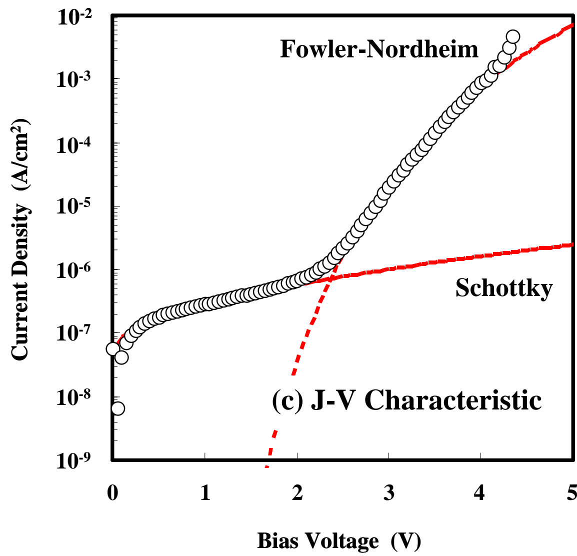




(b) Normalized Capacitance

(a) C-V Characteristic **C = 25.54 fF/μm², α = 5182, β = -1324**





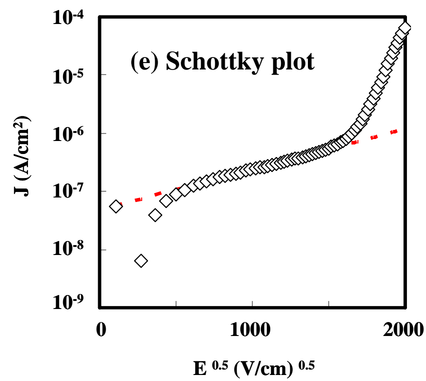


Fig.3-23 electrical characteristics of highest capacitance density MIM capacitor

In forming gas at 300°C for 10 minutes with PDA and PMA

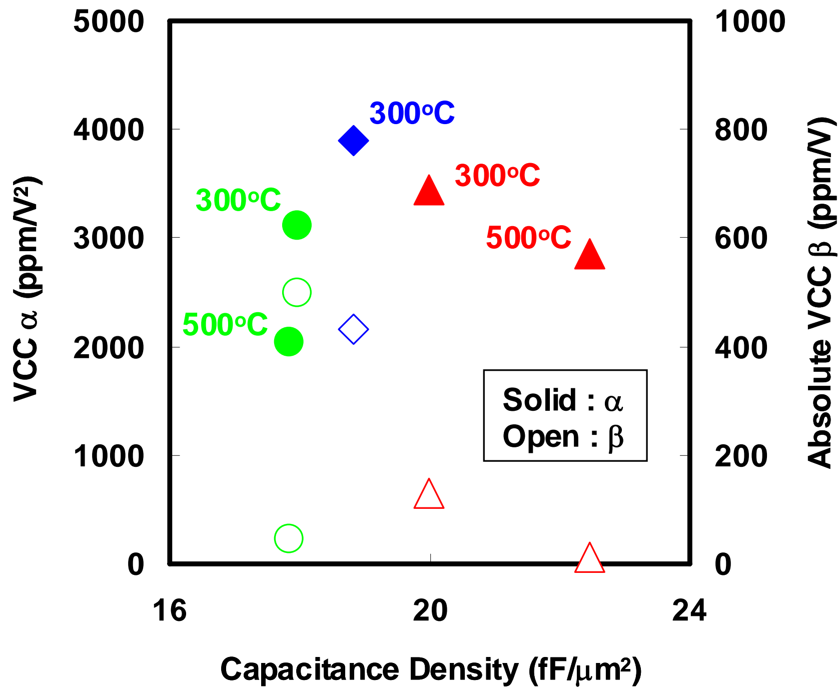


Fig.3-24 VCC vs. capacitance density

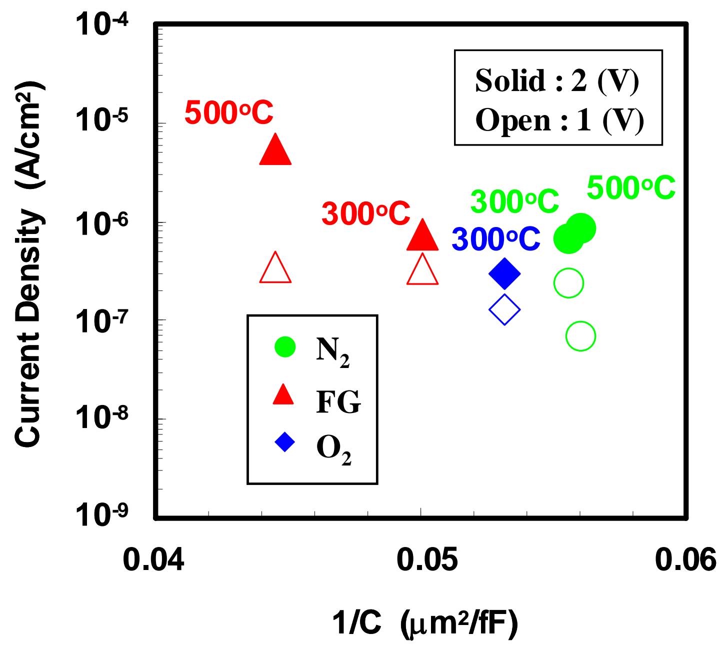


Fig.3-25 Current density vs. 1/C characteristics with 1V and 2V

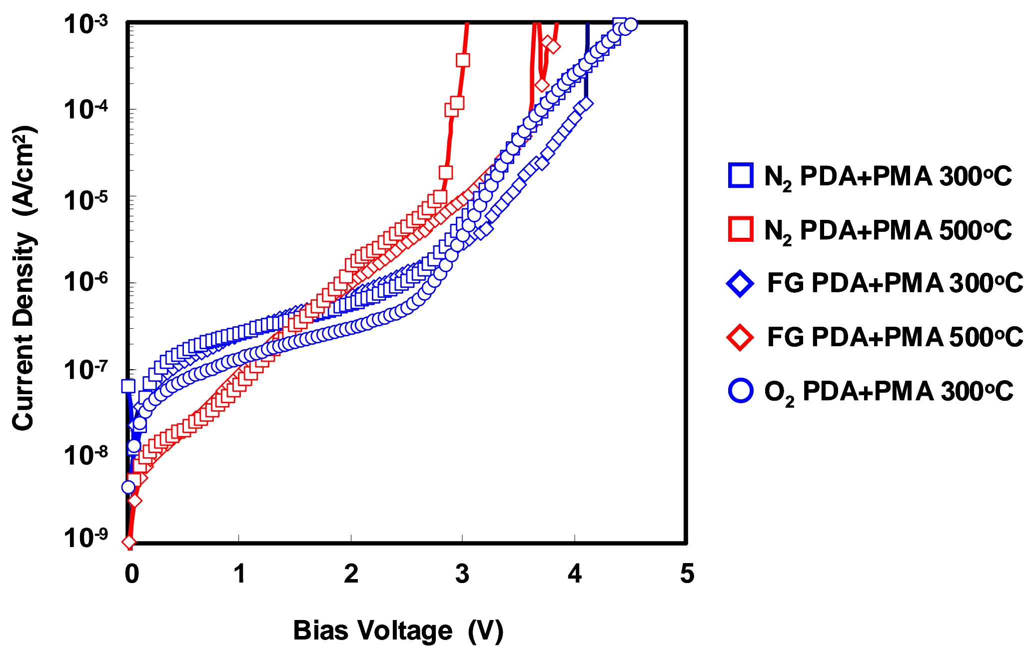


Fig.3-26 Current density vs. voltage characteristics with different annealing condition

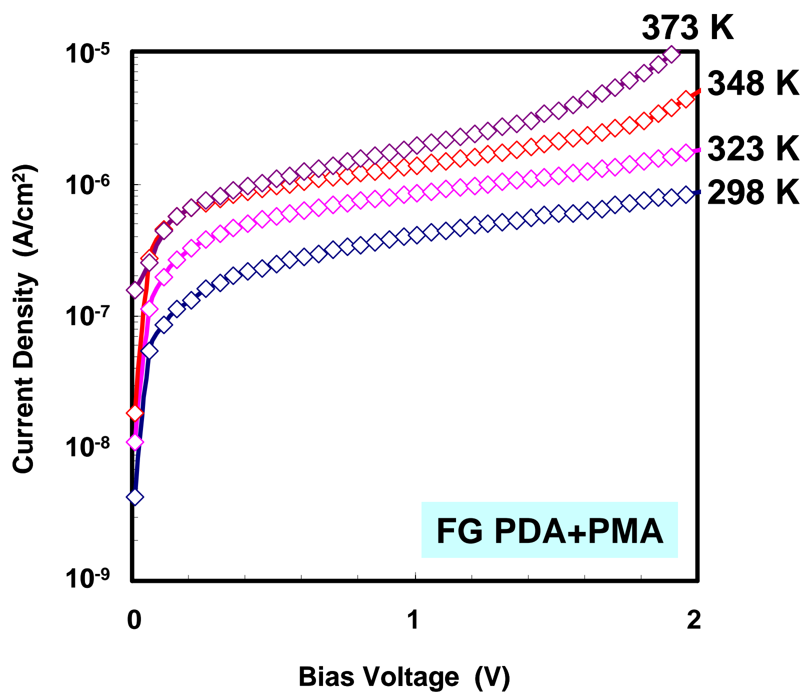
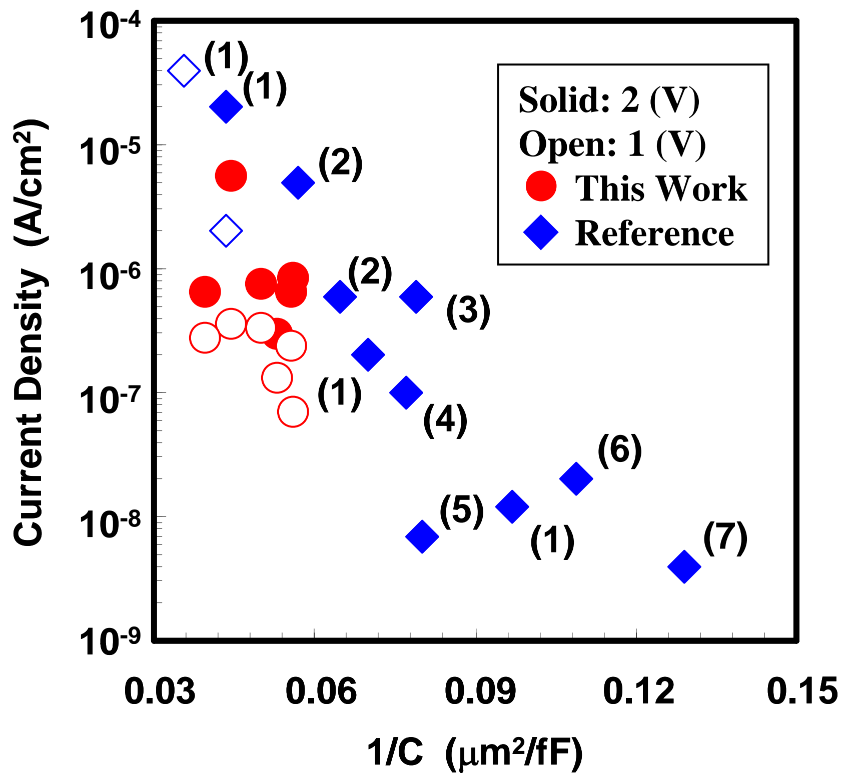


Fig.3-27 Temperature dependence with FG PDA and PMA at 300°C condition



(1): TiTaO (K.C. Chiang, VLSI'05)[40]
(2): Al/Hf/Nb/Hf/Al (S. J. kim, VLSI'05)[39]
(3): HfO_2 (X. Yu, EDL'03)[18]
(4): HfTbO (S. J. Kim, VLSI'03)[41]
(5): Al/Hf/Al/Hf/Al (H, Hu, IEDM'03)[38]
(6): Al/Ta/Al (T. Ishikawa, IEDM'02)[21]
(7): HfO_2/SiO_2 (S. J. Kim, VLSI'04)[14]

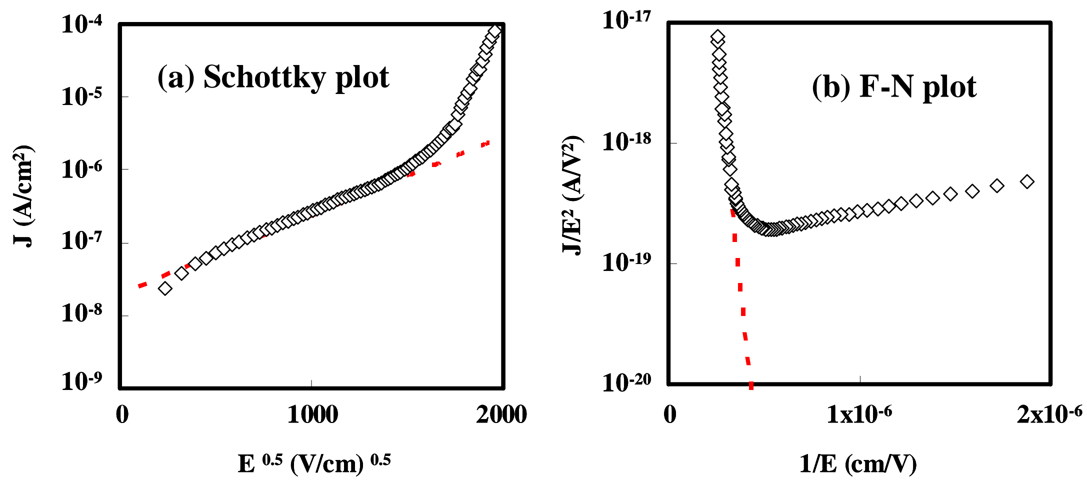
Fig.3-28 J-1/C with our study and reference data

Here, Al is Al_2O_3, Hf is HfO_2, Nb is Nb_2O_5, and Ta is Ta_2O_5.

3.4.2 Conduction Mechanism

Figure3-29 - 3-33 show conduction mechanism with different annealing condition. At 300°C annealing condition, Schottky and F-N conduction mechanism was shown as same as last section. Under low bias voltage, Schottky conduction was shown. Under high bias voltage, F-N conduction was shown in Fig.3-29, 3-31 and 3-33. At 500°C annealing condition, P-F conduction was shown between Schottky and F-N conduction region in Fig. 3-30 and 3-32. This difference is annealing temperature, annealing time and gas correlation is not. I considered that 500°C annealing is introduced trap site in La_2O_3. P-F conduction is caused trap site in insulator. But leakage current of 500°C annealed sample under low voltage is lower than 300°C annealed sample.

In 300°C annealed condition, appeared conduction mechanisms are Schottky and F-N conductions. These conduction mechanisms are not caused trap sites, mainly. Schottky conduction is caused a band offset and F-N conduction is caused a high electric field. So, 300°C annealing is good annealing temperature that is expected very low trap sites. 500°C annealing is expected that increasing trap sites, but as leakage current was very low under low bias voltage region and high capacitance density was obtained, it is thought that La_2O_3 film is stability at 500°C heating process with stability interface condition between La_2O_3 and metal (or Si).



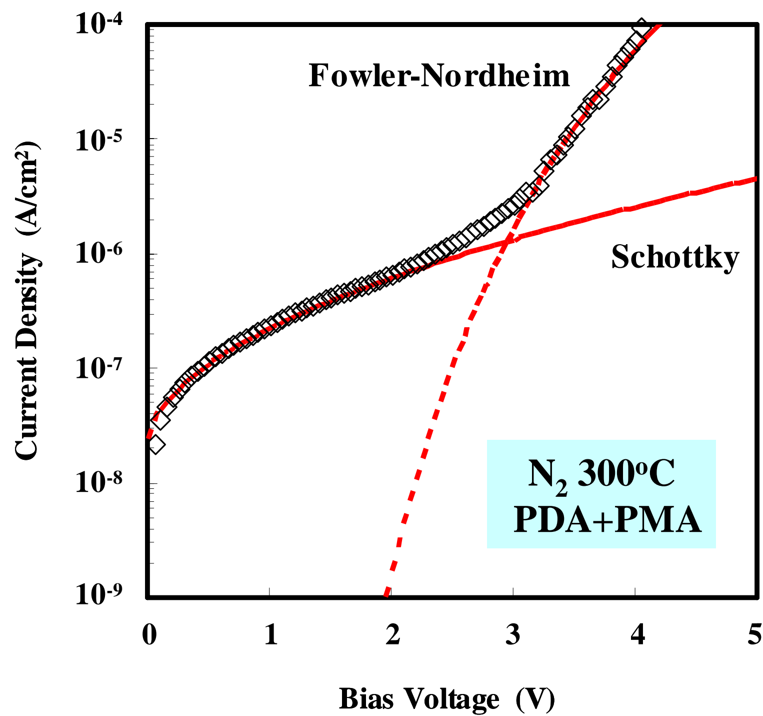


Fig.3-29 N_2 PDA+PMA 300°C conduction

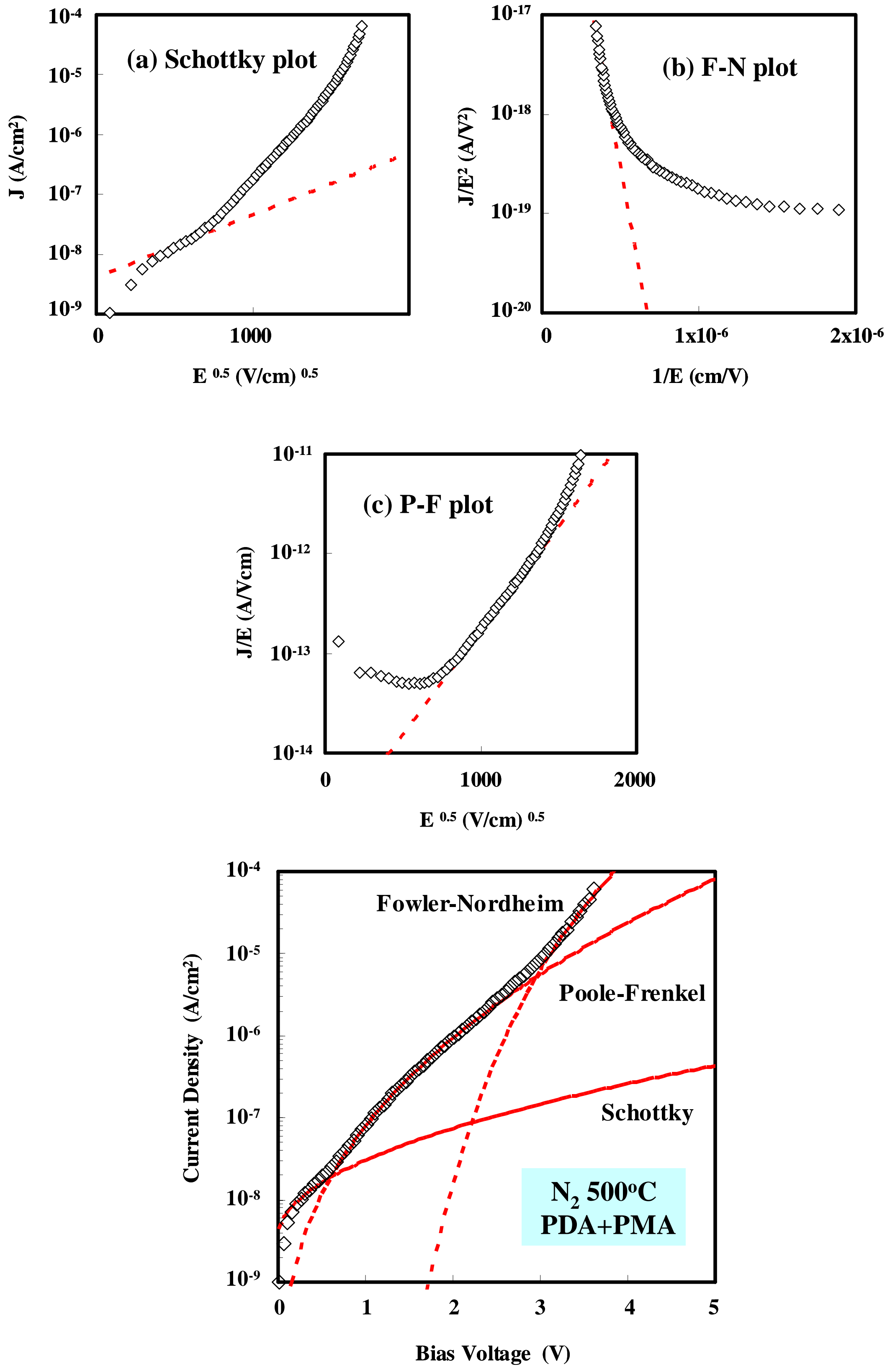
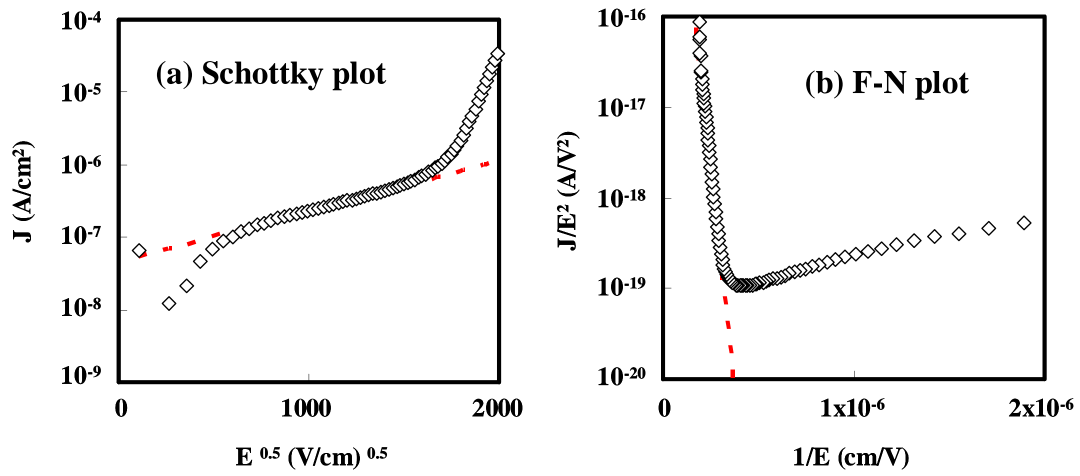


Fig.3-30 N_2 PDA+PMA 500°C conduction



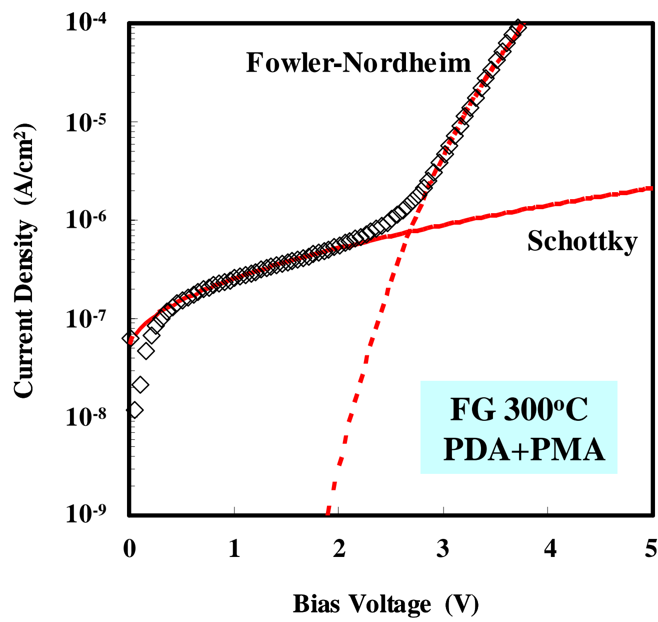


Fig.3-31 FG PDA+PMA 300°C conduction

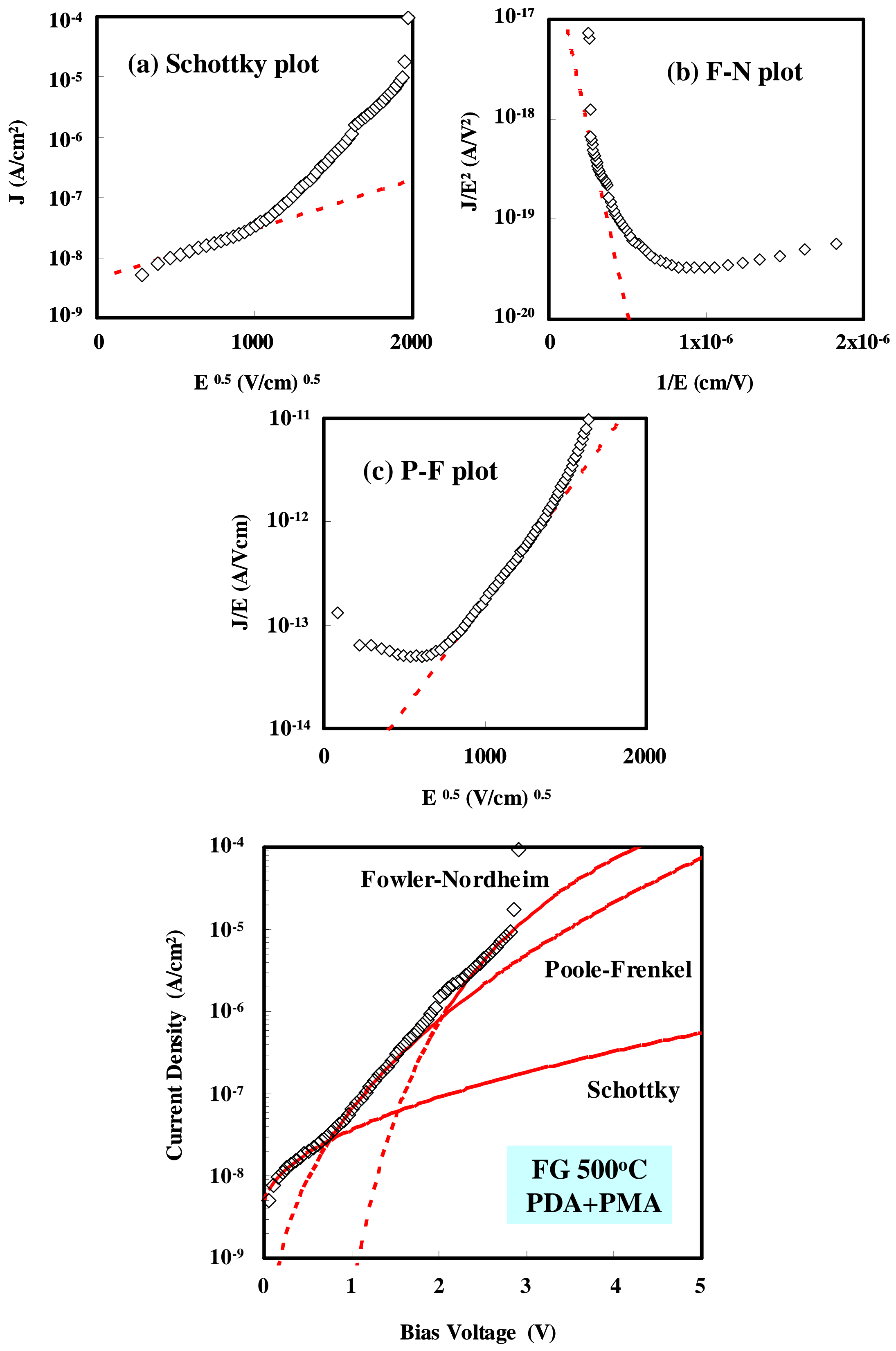


Fig.3-32 FG PDA+PMA 500°C conduction

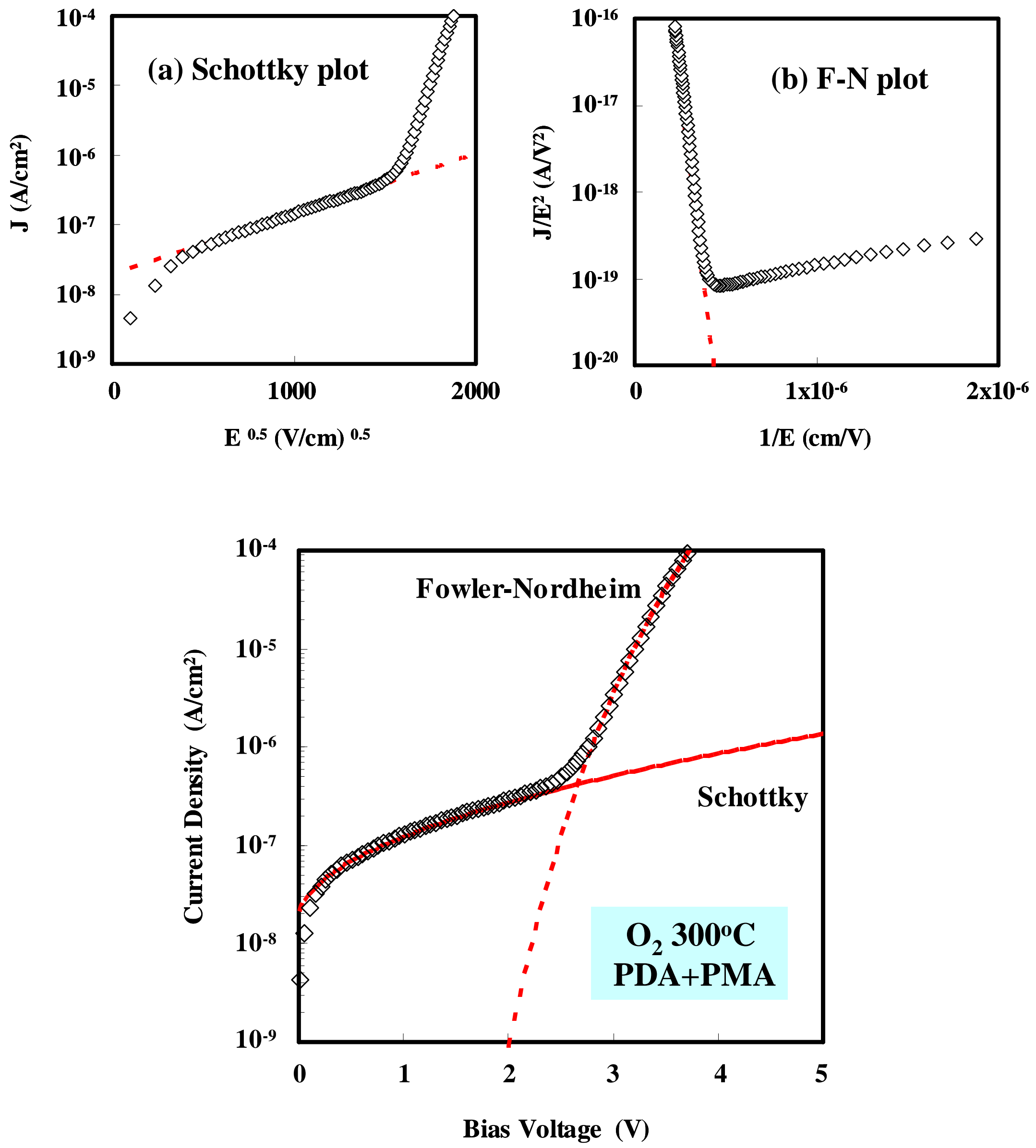


Fig.3-33 O_2 PDA+PMA 300°C conduction

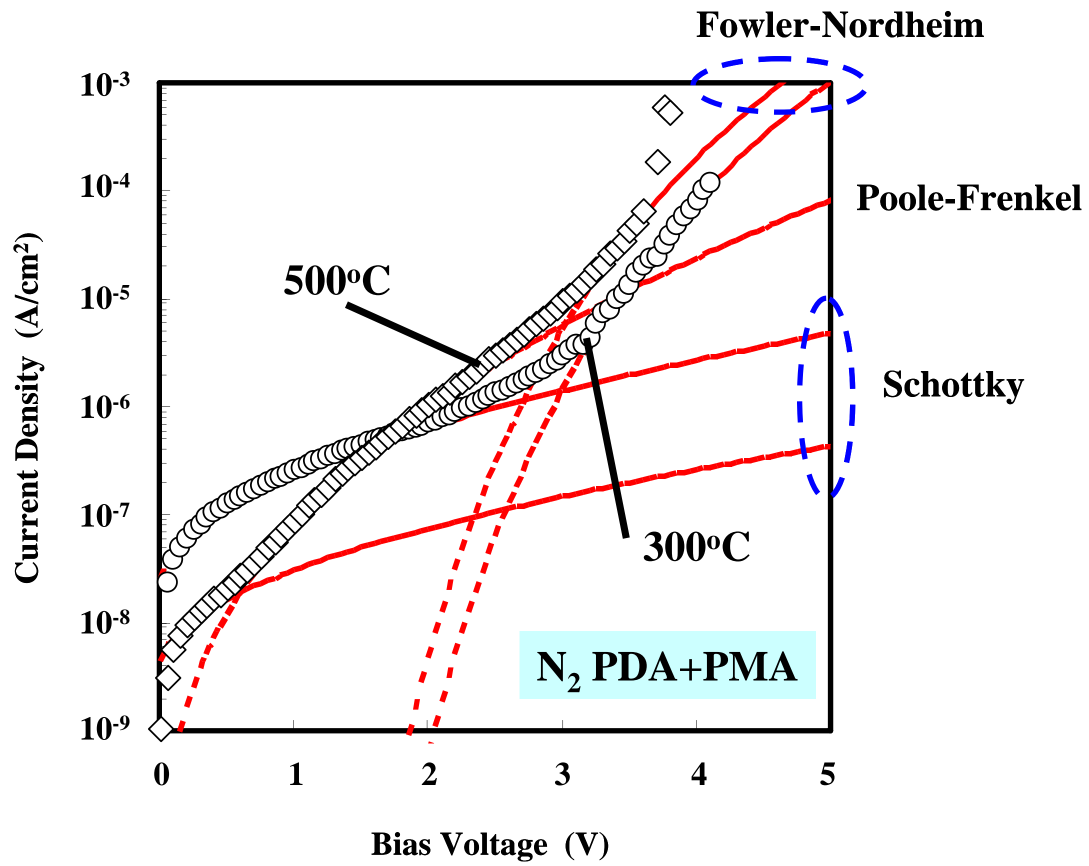


Fig.3-34 J-V characteristic with conduction mechanism 300°C and 500°C

3.4.3 Pt/La_2O_3/Si MIS Capacitor

In this study, effect of interface thought to use MIS and MIM structure. Upper electrode is Pt. Deposition condition and annealing condition is same as MIM and MIS. So, difference of MIS and MIS is structure, Pt/La_2O_3/Si and Pt/La_2O_3/Pt. Figure 3-35 shows MIS and MIM structures. Thickness of La_2O_3 is 10.7 nm for as deposition. Annealing treatment is PDA and PMA in forming gas 300°C. After PDA, La_2O_3 thickness becomes 8.3 nm on Si.

Figure 3-36 shows C-V characteristics of MIS and MIM capacitors with FG PDA and PMA annealing, 300°C, 10 minutes. In accumulation, capacitance of MIS capacitor is lower than MIM capacitor. Figure 3-37 shows J-V characteristics and conduction mechanism. Under low voltage, Schottky conduction was mainly both MIS and MIM capacitors. Under high voltage, F-N conduction is mainly, but appeared region were difference. MIM capacitor changed from Schottky to F-N faster. F-N conduction is strongly depended on electric field. This is thought that La_2O_3 thickness of MIM capacitor is thinner than MIS capacitor.

So, La_2O_3 film with interfacial layer is controlled is good material for next generation MIS devices.

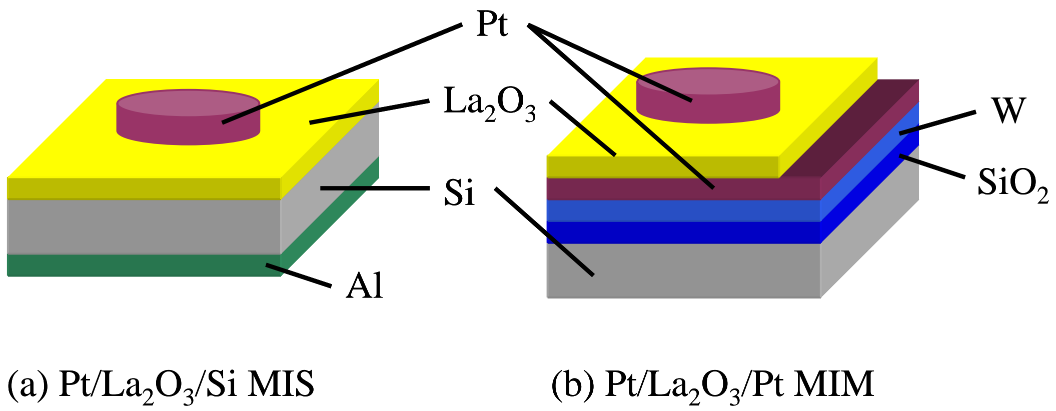


Fig.3-35 MIS and MIM structure

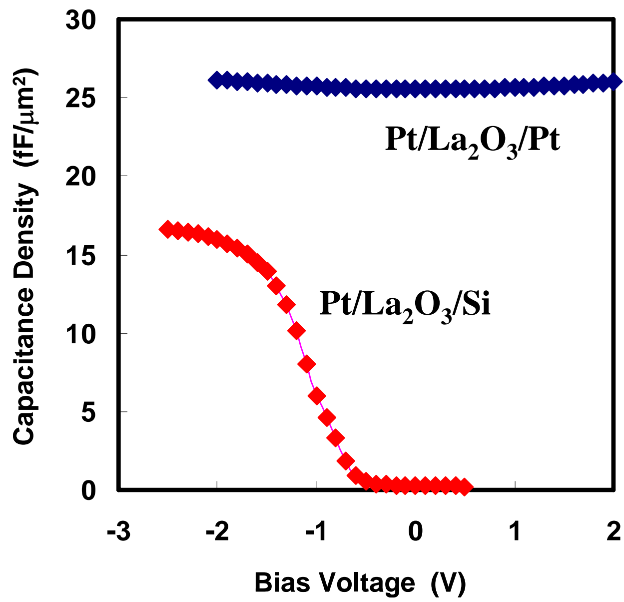


Fig.3-36 C-V characteristics of MIS and MIM capacitors

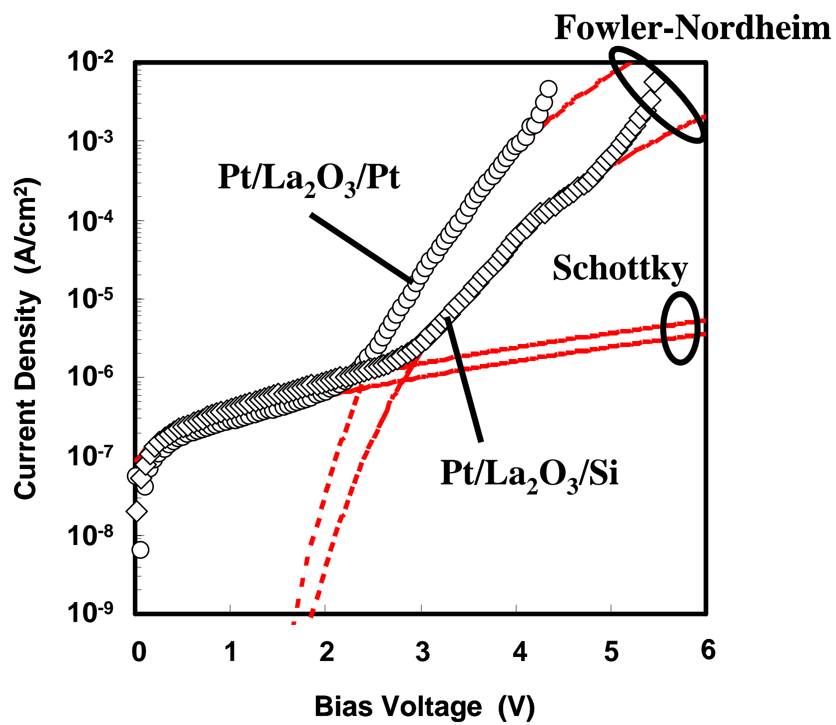


Fig.3-37 J-V characteristics with conduction mechanism

3.4.4 Summary

In this section, to obtain characteristics high capacitance density, I improved Pt substrate roughness. Thinner thickness Pt/La_2O_3/Pt MIM capacitor can fabricated to improve substrate roughness. Therefore, substrate roughness is one of important factor for MIM capacitor. The highest capacitance density and low leakage current were obtained at FG annealing condition. Annealing temperature dependence is obtained between 300^oC and 500^oC. At 300^oC annealing condition, Schottky conduction and F-N conduction was obtained N_2, O_2 and FG annealing, respectively. At 500^oC annealing condition, Schottly conduction, P-F conduction and F-N conduction were obtained N_2 and FG annealing condition. Thus, annealing temperature increasing, trap site of insulator was increased.

Chapter 4

Conclusion

4.1 Conclusion of this study

Pt/La_2O_3/Pt MIM capacitor was deposited by e-beam evaporation. Deposition temperature is room temperature. Heating at 250^oC in deposition process, electrical characteristics were not obtained. Annealing gases are N_2, O_2 and forming gas. Annealing temperature and time are 300^oC and 500^oC at 10 minutes. As same thickness of as deposition condition, La_2O_3 film thickness was changed different thickness for annealing gas and temperature. Three annealing conditions used, only PDA, only PMA and PDA and PMA. With only PDA, high capacitance density was obtained higher than with only PMA condition. It is thought that thickness of with only PDA condition is thinner than only PMA condition. With PDA and PMA, capacitance density is as same as or less than PDA. With PDA and PMA is the best annealing condition to obtain good characteristics such as low leakage current, high capacitance density and small linear VCC β. With PDA and PMA condition, leakage current is one order lower than with only PDA or PMA condition. It is thought that interface between Pt electrode and La_2O_3 film is more stability than with only PDA or PMA condition. This is also thought from linear VCC value β. The β value with only PDA or PMA conditions are very large and with PDA and PMA condition is very small. Small β value means to obtain near the same capacitance density in the same positive and negative bias voltages were applied. But it is expected that characteristics of only PMA condition is obtained same characteristics with PDA and PMA condition. However, characteristics between with only PMA and with PDA and PMA were different. Since La_2O_3 film became densification with annealing, I considered that only PMA condition not only made stability but also formed defect in La_2O_3 film or Pt-La_2O_3 interface at the same time. In the results, PDA and PMA needed to obtain stability interface and good characteristics

for Pt/La_2O_3/Pt MIM capacitor. However, Pt is known as stability metal in general, so difficult to form interfacial layer with many annealing condition. In other metal such as formed interfacial layer with annealing, with PDA and PMA may be not the best annealing condition.

Annealing temperature is increased from 300^oC to 500^oC, trap site increased from conduction mechanism characteristics. But in Pt/La_2O_3/Pt MIM capacitor, it is enough stability with 500^oC heating process if interface between La_2O_3 and metal (or Si) is stability.

To improve substrate surface roughness, good characteristics were obtained. So, substrate roughness is important factor to obtain good characteristics of MIM capacitor.

For Pt/La_2O_3/Pt MIM capacitor, process conditions were depended on electrical characteristics strongly. Flat substrate surface and with PDA and PMA need to obtain good stability and electrical characteristics. At low annealing temperature condition is more stability than at high annealing temperature. However, at high annealing temperature condition is obtained high capacitance density and low leakage current under low bias voltage region. Annealing temperature condition is decided to target characteristics such as needed high capacitance density, low leakage current etc.

4.2 Future Issues

In this study, we obtained high capacitance density, low leakage current and small linear VCC β. On the other hand, quadratic VCC α value is as same as other high-k material. Many high-k materials have positive α value. But there is negative a value material such as SiO_2. And to laminate positive α and negative α materials, small α is obtained [14]. Thus, to laminate SiO_2 and La_2O_3, advantage of high relative dielectric constant is lost. Therefore, in the future, we need to research high relative dielectric constant and negative α value material.

Substrate roughness effect is important factor to obtain good characteristics. Good surface substrate and high work function value metals also need to the future MIM capacitors.

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Akira Fukuyama,

Yokohama,

February, 2006

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