Master Thesis

Study on La_2O_3/Y_2O_3 Stacked Gate Dielectrics

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Chapter 1

Introduction

1.1 Background of this Study

In recent years, electric products such as personal computer and cell phone are rapidly improved to high speed processing, miniaturization and low power consumption, and now these are indispensable in our life. These products and improvements are realized by progresses of silicon LSI technology that are high density, high integration and so on. The performance of silicon LSI system extremely depends on the characteristics of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). The performance of FET has improved by miniaturizing the physical size of the devices according to scaling law. By the shrinking of devices with the same scaling coefficient S, it becomes possible to operate at higher speed switching operation, and the lower power consumption due to the shrinking the channel length as shown in Fig. 1.1 and Table 1.1. As these results, whole performance of LSI system can be also improved. Therefore, the research in the devices for downsizing is very important to continue improvement of products and this research has continued throughout the world universities and company currently.

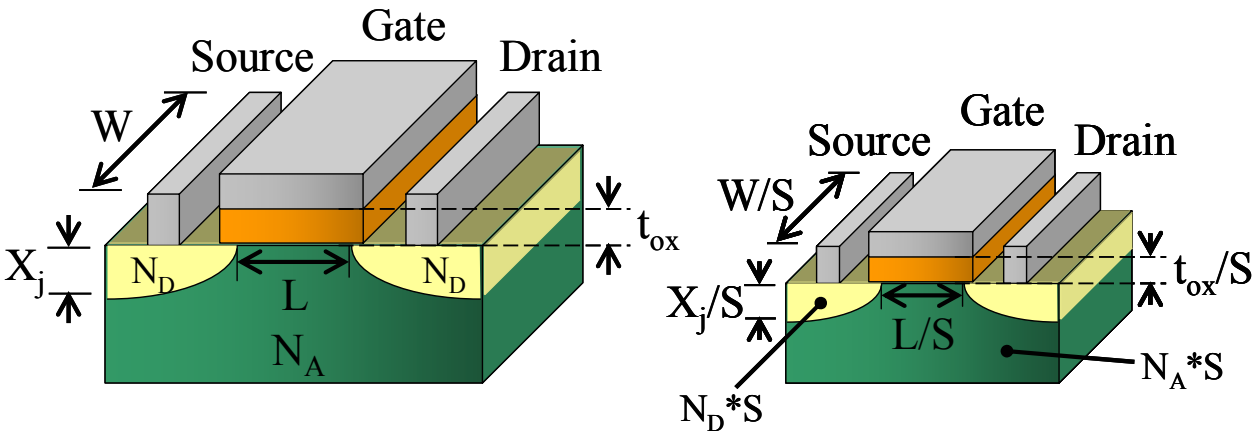


Fig. 1.1 Scaling method on MOSFET

Table 1.1 Scaling on MOSFET by a scaling factor S

Quantity	Before Scaling	After Scaling
Channel Length	L	L' = L/S
Channel Width	W	W' = W/S
Device Area	A	$A' = A/S^2$
Gate Oxide Thickness	t_{ox}	$t_{ox}' = t_{ox}'/S$
Gate Capacitance per Unit Area	C_{ox}	$C_{ox}' = S*C_{ox}$
Junction Depth	X_j	$X_j' = X_j*S$
Power Supply Voltage	V_{DD}	$V_{DD}' = V_{DD}/S$
Threshold Voltage	V_{th}	$V_{th}' = V_{th}/S$
Doping Densities	N_A	$N_A' = N_A*S$
	N_D	$N_D' = N_D*S$

1.2 Limits of SiO_2 as Gate Insulator

The MOS transistor which constitutes the main building block of LSI systems must be shrunk in size to improve its performance. For that purpose, the thickness of the gate insulator has been thinner. Up to the present, SiO_2 has been used gate insulator. Because SiO_2 has good property such as very low fixed charge density and high thermal stability on Si substrate. According to International Technology Roadmap for Semiconductor (ITRS), In the future, the gate dielectric oxide will become a few atoms in thickness because of this continuous shrinking[1]. However, if the dielectric oxide is too thin, then the gate tunneling leakage current exponentially increases and this effect brings about serious problems to operate the devices. Fig. 1.2 shows the schematic band diagram explaining direct tunneling mechanism. The direct tunneling equation is as follows.

$$I \propto \exp\left[-(m\phi)^{1/2} \cdot D\right] \quad \cdots\cdots\cdots\cdots\cdots\cdots (1)$$

m: electron effective mass ϕ: barrier height of Si

D: physical thickness of insulator

In the case of thick insulator, that works as barrier for carriers. However, in the case of thin insulator less than about 1nm, the carriers directly pass through the insulator owing to quantum effect. Consequently, the leakage current exponentially increases. This phenomenon will cause increasing of power consumption and degradation of LSI reliability. Table 1.2 shows the electrical property of 1nm SiO_2 gate insulator MOSFET. This table says gate leakage current density will be 600 [A/cm^2] when SiO_2 thickness

will be 1nm. And in the case of the thickness of insulator is 0.8nm, the leakage current density will become 1kA/cm^2 over by direct tunneling effect. However, in 2006, EOT (Equivalent Oxide Thickness) in high performance logic technology becomes 1nm, and in 2008, becomes 0.8nm according to ITRS as shown in Table 1.3. Therefore, the new scheme for overcoming aforementioned problem is required to realize EOT value conformed to the ITRS roadmap.

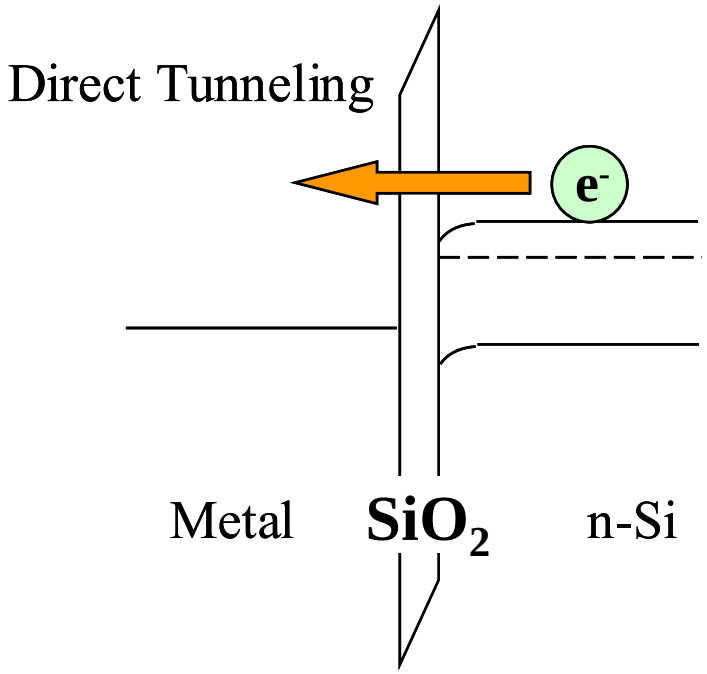


Fig. 1.2 Band diagram for thin SiO_2 MOS capacitor

Table 1.2 Electrical property of 1nm SiO_2 gate insulator MOSFET

EOT [nm]	1.0
Leakage Current Density (at 25°C) [A/cm^2]	100
Gate Length [nm]	0.1
Gate Width [nm]	5
Gate Area [cm^2]	5×10^{-9}
Functions per Chip (Transistors/Chip)	5×10^{-1}
Total Gate Area [cm^2]	5×10^{-1}
Total Leakage Current per Chip [A/chip]	50

Table 1.3 ITRS 2004 edition

(High Performance Logic Technology Requirements)

	2005	2008	2011	2014	2017
EOT [nm]	1.1	0.8	0.7	0.6	0.5
Leakage Current Density Limit (at 25°C) [A/cm2]	5.2×10^2	1.1×10^3	2.08×10^3	9.09×10^3	2.08×10^4
Physical Gate Length [nm]	32	22	16	11	8
Power Supply Voltage [V]	1.1	1.0	1.0	0.9	0.8

1.3 Requirements and Problems for High-k Gate Dielectrics

As one of the solutions for overcoming the limits of SiO_2 dielectric as described in section 1.2, high-k materials have been attracted much attention. High-k material is a material which has high relative dielectric constant. The capacitance C_i of gate dielectric is expressed as follows.

$$C_i = \frac{\varepsilon_0 kS}{t} \cdots\cdots\cdots\cdots (1)$$

ε_0: vacuum dielectric constant k: relative dielectric constant

S: gate dielectric area t: physical thickness of gate dielectric

Where, the value of vacuum dielectric constant is about 8.855×10^{-14} [F/cm] and SiO_2 relative dielectric constant is 3.9. As a method of maintaining enough capacitance value with shrinking of gate area, the physical thickness of insulator has been thinned conventionally. However, the phenomenon which is direct tunneling leakage current effect by the limit of thinning physical thickness will be serious problem. Therefore, any other new schemes have been required to maintain capacitance value with the shrinking device. As one of the breakthrough ways, there is the way using high-k material instead of conventional SiO_2. This way make possible to increase insulator thickness with maintaining capacitance. The band diagrams of high-k material case and SiO_2 case are shown in Fig. 1.3. The arrows represent flow of carrier. As this figure, direct tunneling leakage current can be suppressed by increasing insulator thickness owing to using high-k material.

ITRS requires the replacement of SiO2 gate dielectric films with high-k materials immediately. The requirements for high-k materials are as follows.

(1) Large dielectric constant (k=10~30)

(2) Small leakage current density

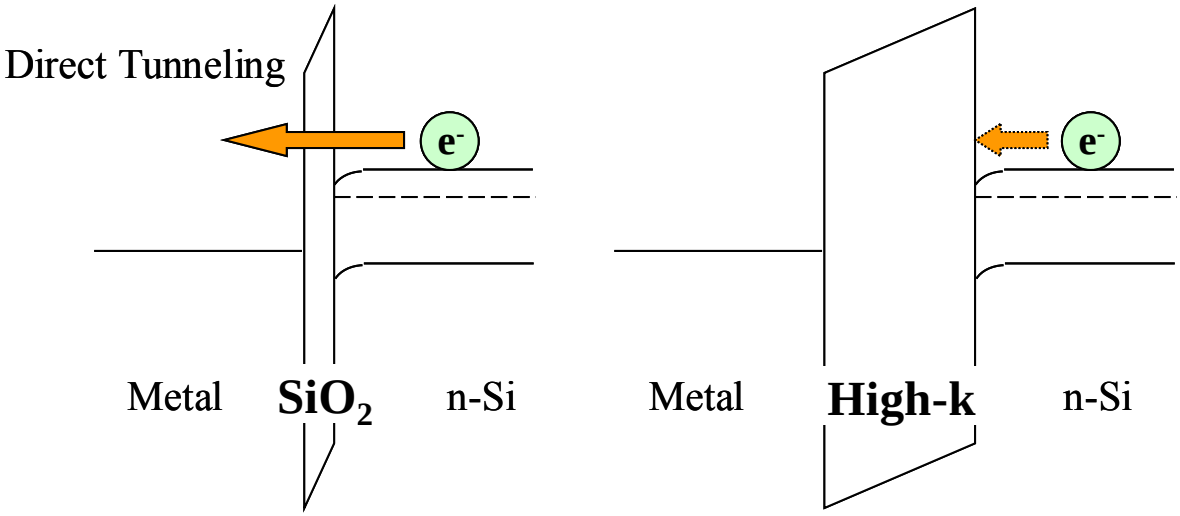
(3) Chemical thermodynamic stability on the Si (1000 K)

(4) Small density of interface state and fixed charge

(5) High mobility and high reliability

In order to overcome the limits of SiO_2, several promising materials have been investigated in recent years by a large number of researchers. The elements which can be the candidates of the alternative insulator are quite limited because of the thermodynamic instability on Si or radioactivity as shown in Fig. 1.4. Under these restricted conditions, metal oxides like Al2O3, ZrO 2 , HfO2 and rare earth oxides have been studied eagerly for the next generation gate dielectric materials because they have high dielectric constants and wide band gap[2-4]. Fig. 1.5 shows the band offsets for high-k dielectrics on Si[27]. Recently, excellent results of rare earth oxides, such as La_2O_3, CeO_2, Pr_2O_3, Gd_2O_3, Dy_2O_3 and their silicate have been reported[5-12]. However, high-k materials including rare earth oxides have unsolved problems such as formation of interfacial layer and growth micro crystal and moisture absorption. And the problems of high-k materials Al_2O_3, ZrO_2 and HfO_2 are as follows. Al_2O_3 has high relative dielectric constant about 10, this value is about 2.5 times as large as SiO_2. However Al_2O_3 has the biggest problem that is strong dependence of the flat-band shift on the film thickness due to the fixed charge. The control of this flat-band shift is very

difficult. ZrO_2 and HfO_2 are popular materials because of their very high dielectric constants and thermodynamic stability on the Si. However, their materials have the problems that are growth of silicate or SiO_2 at interfacial layer and changing into micro-crystal during the thermal process. Above all problems, most serious problem is formation of silicide during the thermal process.



(a) SiO_2 (b) High-k material

Fig. 1.3 The band diagrams of MIS capacitor

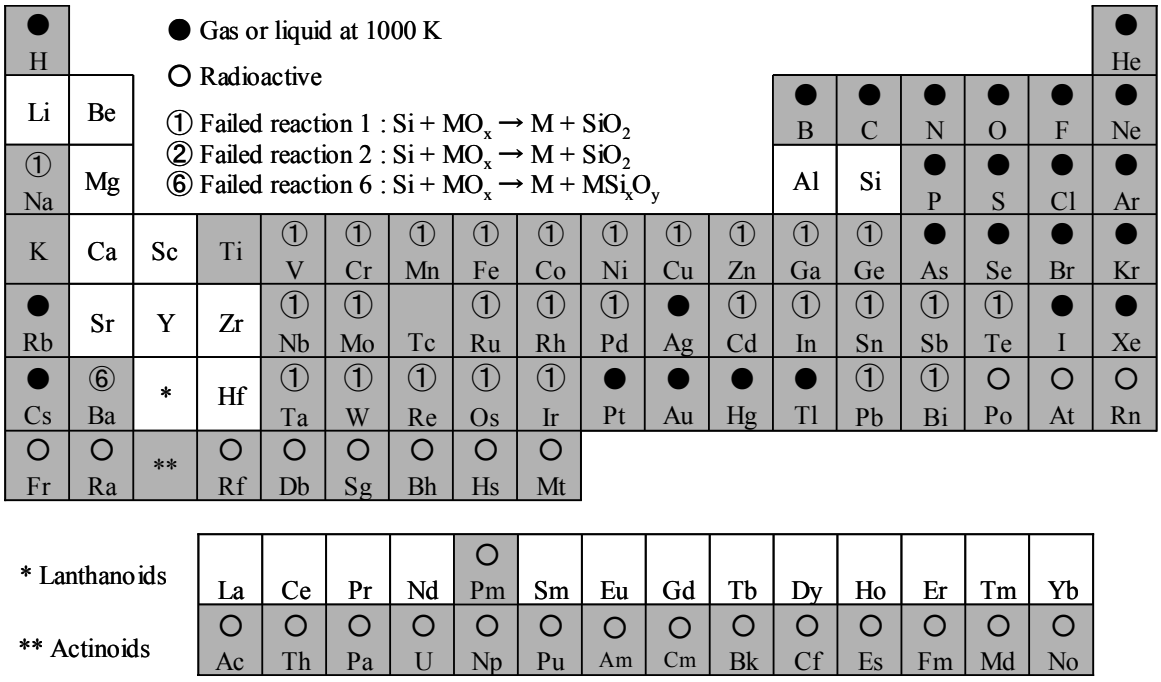


Fig. 1.4 Candidates of the elements
which have possibility to be utilized as high-k gate insulators

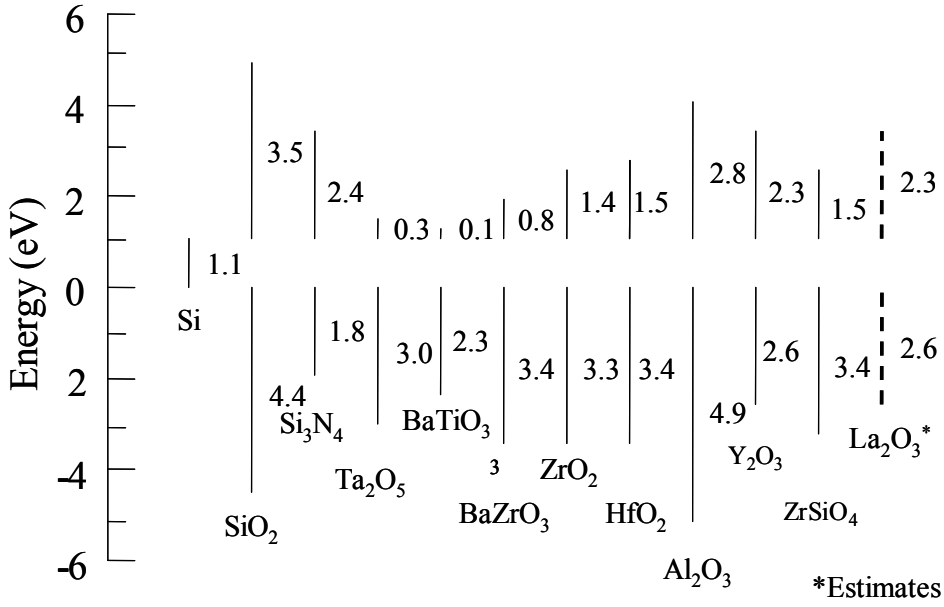


Fig. 1.5 Band offsets for high-k dielectrics on Si

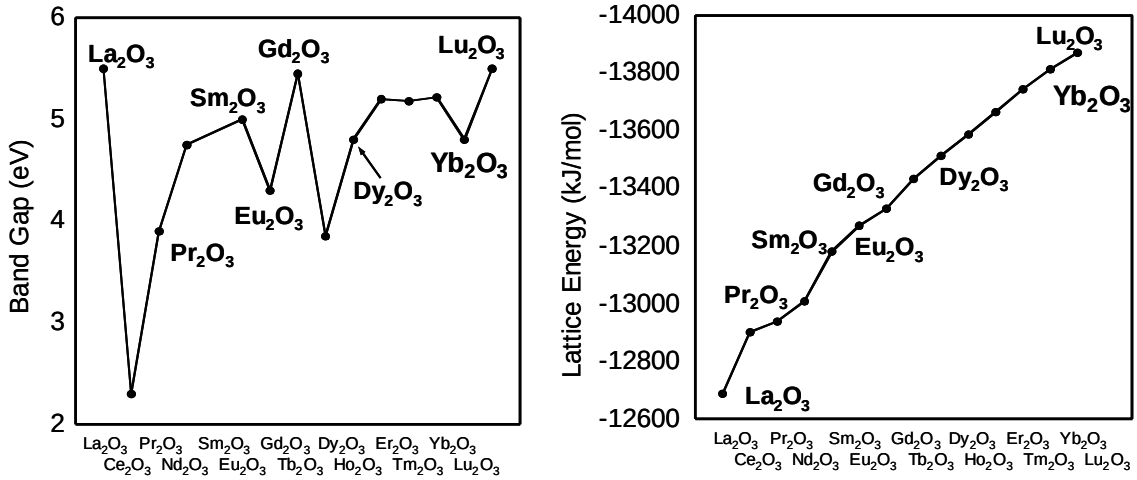
1.4 Physical Properties of Rare Earth Oxide

Fig. 1.6 shows a part of the periodic table, for lanthanide elements. There are 15 elements, but Pm is an unstable radioactive artificial element and should be removed from the candidates. Lanthanides are called as "*rare earth*" elements, but it should be noted that they are actually no rare in the earth-shell and even their contents are larger than that of Hg, In, Ag, etc.

Although, the outer shell electron configurations are the same for all the lanthanide elements, it was found that the properties of lanthanide oxides are quite different. The band gap and lattice energy for the lanthanide oxides are shown in Fig. 1.7 (a) and (b) respectively. The reported dielectric constants of rare earth oxides are about 10-30, and the energy band gap is about 2.4-5.5eV. The properties of some major rare earth oxides are shown in Table 1.4 As this table, rare earth oxides which have good properties are expected as next generation insulator.

La^{57}	Ce^{58}	Pr^{59}	Nd^{60}	Sm^{62}	Eu^{63}	Gd^{64}	Tb^{65}	Dy^{66}	Ho^{67}	Er^{68}	Tm^{69}	Yb^{70}	Lu^{71}

Fig. 1.6 Lanthanide elements



(a) Band gap (c) Lattice energy

Fig. 1.7 Band gap and lattice energy for lanthanide elements

Table 1.4 The reported high-k materials for gate insulators

Materials	SiO_2	Al_2O_3	La_2O_3	Pr_2O_3	Gd_2O_3	HfO_2	ZrO_2
EOT [nm]	0.8	1.5	0.48	1.4	1.5	0.8	0.8
Contact stability with Si [kJ/mol] $Si+MO_x->M+SiO_2$	Stable	+63.4	+98.5	+105.8	+101.5	+47.6	+42.3
Lattice energy [kJ/mol]	13125	15916	12687	12938	13330	a b c	11188
Bandgap [eV]	9	6-8	5.4	3.9	5.4	5.7	5.2-7.8
Structure	Amorphous	Amorphous	Amorphous	Crystal T>700°C	Crystal T>400°C	Crystal T>700°C	Crystal T>400-800°C
k	3.9	8.5-10	27	13	17	24	11-18.5

1.5 Purpose of This Study

One of the serious problems for the high-k gate dielectric is thermal stability on Si substrate. As shown in Table 1.4, there are several candidates that are thought to be theoretically stable on Si. However, it cannot be said necessarily that they are stable because the thermodynamic property of thin film is different from the bulk case by the influences of the difference from the stoichiometric composition, interfacial stress and so on. In general, most high-k materials react with Si easily during the annealing process after deposition, and low dielectric interfacial layer consisting of SiO_2 or silicate is formed.

La_2O_3 is one of the promising materials with high dielectric constant (reported value is 27) in the rare earth oxides. However, La_2O_3 also has problem that EOT increases owing to the silication of La_2O_3 and growth of SiO_2 layer[14] as shown in Fig. 1.6. Therefore the solution of this problem is indispensable to improve characteristics of insulator.

Y_2O_3 is also one of the rare earth oxides and has the following features[15].

(1) Strong affinity for oxygen ($2.4x10^{-22}$ kcal/O atom)

(2) Strong thermodynamic stability (up to 2300oC)

(3) High dielectric constant (18)

(4) Large band gap (5.5eV)

And, it is reported that Y_2O_3 thin film is also very stable on Si substrate[17]. Fig. 1.7 shows Gibbs free energy values of the rare earth materials and the other famous

high-k materials for the following reaction[13].

$$Si + MO_x \rightarrow M + SiO_x$$

This value means ease of growth of interfacial layer. Y_2O_3 has very large value. In other words, Y_2O_3 is a material which easily suppresses growth of interfacial layer compared with the other high-k materials.

In order to maintain EOT and suppress a leakage current after annealing, we used stack gate dielectrics structure. As shown in Fig. 1.8, thermodynamic stable Y_2O_3 is deposited on Si substrate as buffer layer, and high dielectric constant La_2O_3 is deposited on Y_2O_3. The purpose of this study is suppression of La-silicate layer growth by La_2O_3 / Y_2O_3 structure for improvement performance of the gate insulator.

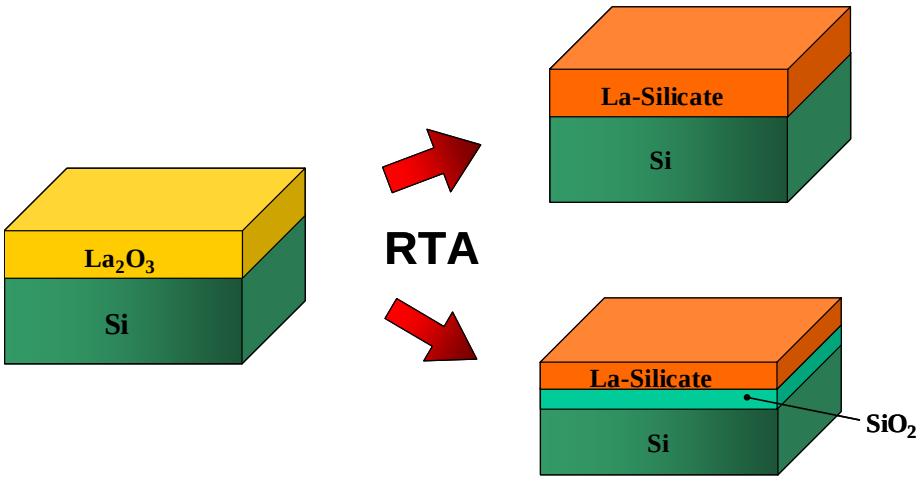


Fig. 1.6 Problem of La_2O_3 films

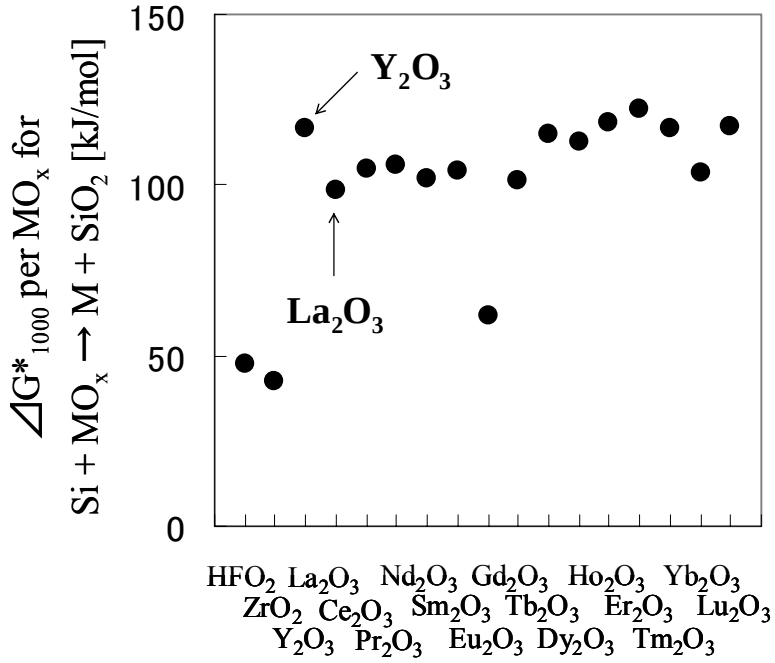


Fig. 1.7 Gibbs free energy per MO_x for $Si + MO_x \rightarrow M + SiO_2$

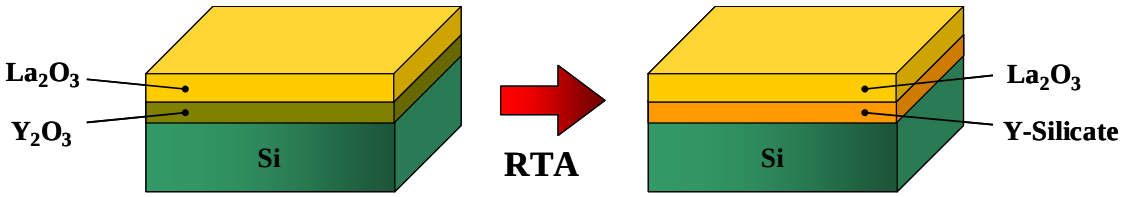


Fig. 1.8 Schematic of La_2O_3/Y_2O_3 structure before and after annealing

Table 1.4 thermodynamic properties

Metal	$-\triangle G_f$ (10^{-22} kcal/O atom of metal oxide)	Expected oxidation product of metal silicide on silicon
Si	1.70	
Ta	1.52	$SiO_2/TaSi_2/Si$
Mo	0.88	$SiO_2/MoSi_2/Si$
W	1.01	$SiW_2/WSi_2/Si$
Y	2.40	$Y_2O_3 \cdot SiO_2/Si$
La	2.26	$La_2O_3 \cdot SiO_2/Si$
Zr	2.06	$ZrO_2 \cdot SiO_2/Si$
Hf	2.16	$HfO_2 \cdot SiO_2/Si$

Chapter 2

Fabrication and Characterization Methods

2.1 Fabrication Methods

2.1.1 Si Substrate Wet Cleaning

For deposition of high quality thin films, ultra clean Si surface is required, without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination, The theoretical resistivity of pure water at 25^{o}C is 18.25 M Ωcm. Ultra-pure water (UPW) systems used in this study provided UPW with more than 18.2 MΩcm resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle (fΦ0.1 μm) per milliliter.

In this study, the substrate cleaning process was based on RCA cleaning process, was proposed by W.kern et al. But some steps were reduced. The steps were shown in Fig.2.1. First, a cleaning steps in a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2=4:1) was performed to remove any organic material and metallic impurities. And then, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:100). Finally, the cleaned wafer was dipped in DI water and loaded to chamber immediately.

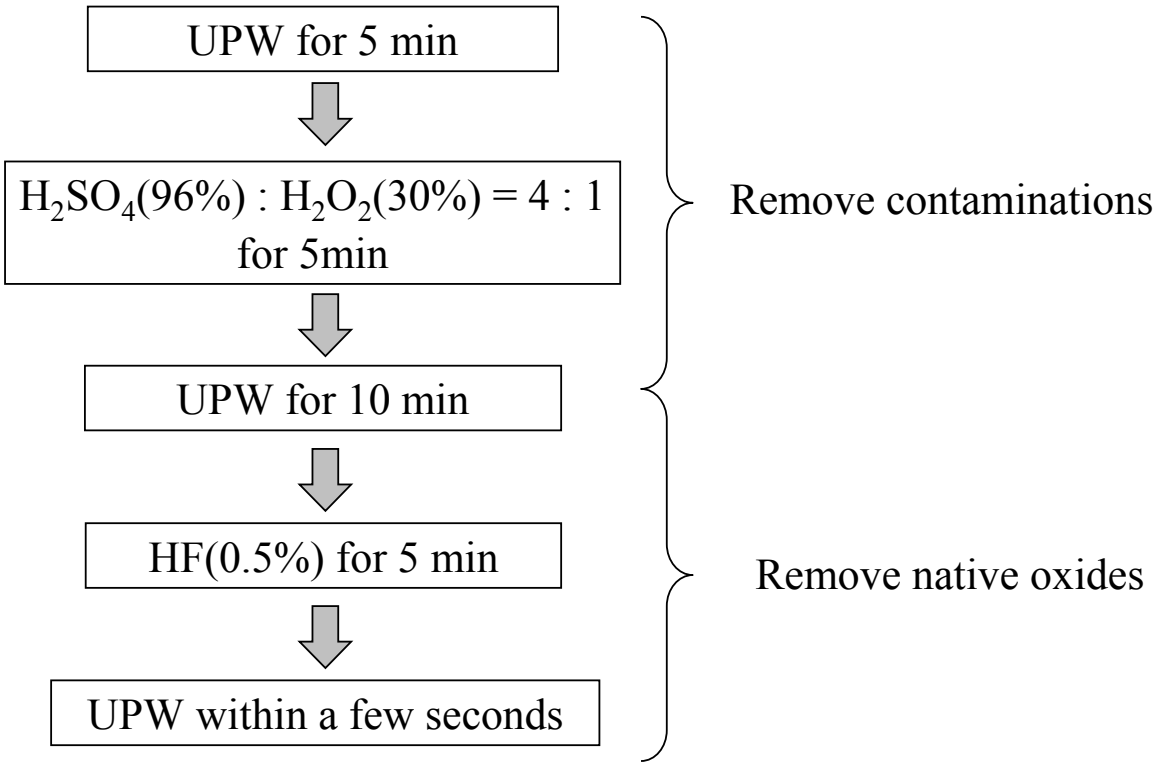


Fig 2.1 Cleaning process of Si substrate

2.1.2 Si Substrate Wet Cleaning

In order to reduce leakage current and interfacial layer, chemical oxidation on Si surface is attempted. In this study, Oxidation method is used by dipping 30% H_2O_2 that seem to make suitable oxide layer and oxidation rate is 0.7nm by 30min at room temperature.

After cleaning process, Si substrate was dipped in H_2O_2 and then substrate was dipped in DI water and load to chamber immediately. The steps were shown in Fig.2.2.

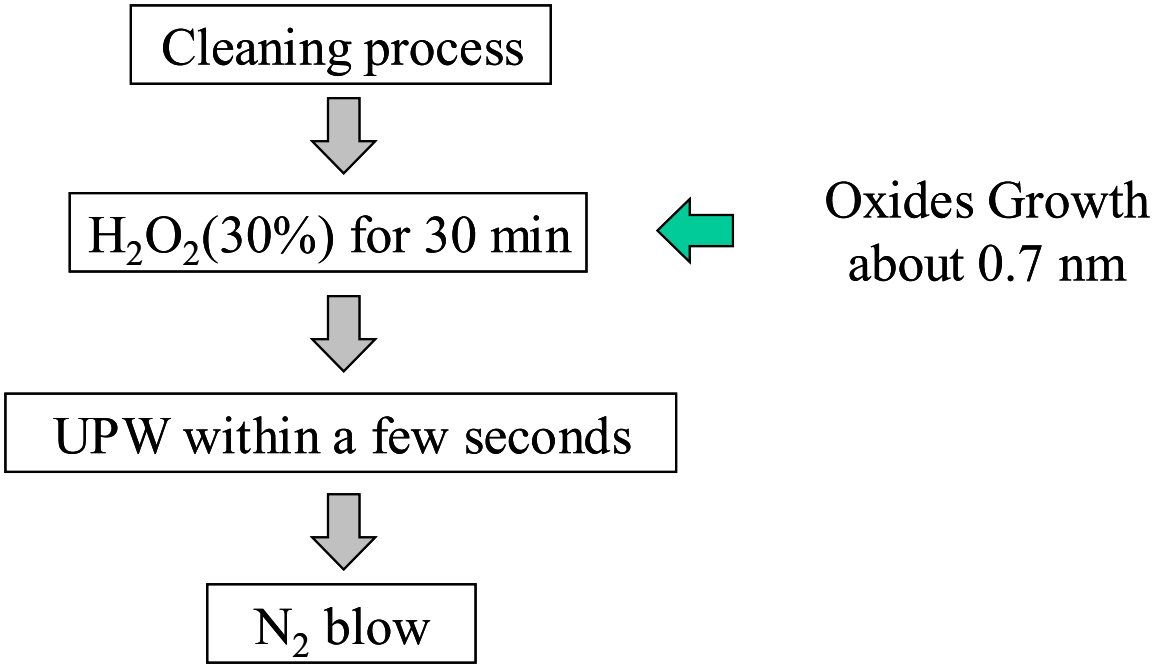


Fig 2.2 Cleaning process of Si substrate

2.1.3 Molecular Beam Deposition (MBE) Process

MBD method is one of the PVD (physical vapor Deposition) methods using molecular beam epitaxy (MBE) system. The material is evaporated by using E-beam and deposited on Si substrate. Only molecular beam is used for depositing in ultra high vacuum (~10^{10} Torr). This method prevents contaminants in film that C-VD method has and provides controllable nanometer order thin films. This method is suitable for research basic characteristics of high-k thin films.

Figure 2.3 and Fig.2.4 shows MBE system, which was used in this study. There are two chambers and four pumps to make ultra high vacuum, four E-guns in deposition chamber and two power supplies that are capable to evaporate two materials in the same time. (Not use plural E-guns in this study.) And there are crystal meter for measurements thickness and RHEED for Analysis.

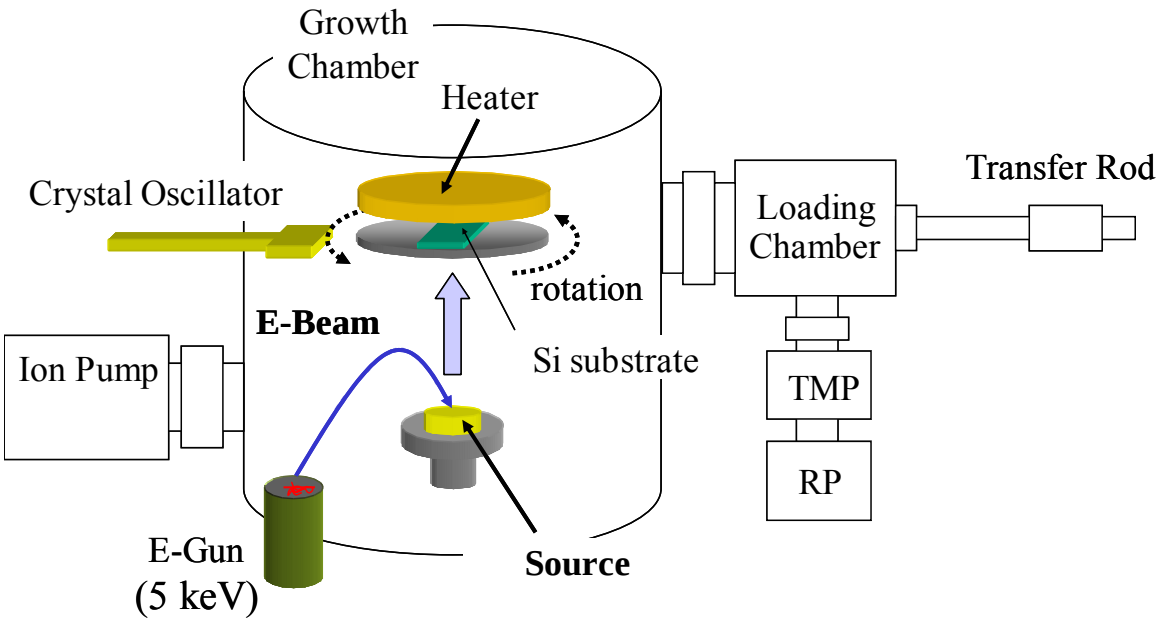


Fig. 2.3 Schematic of the MBE System

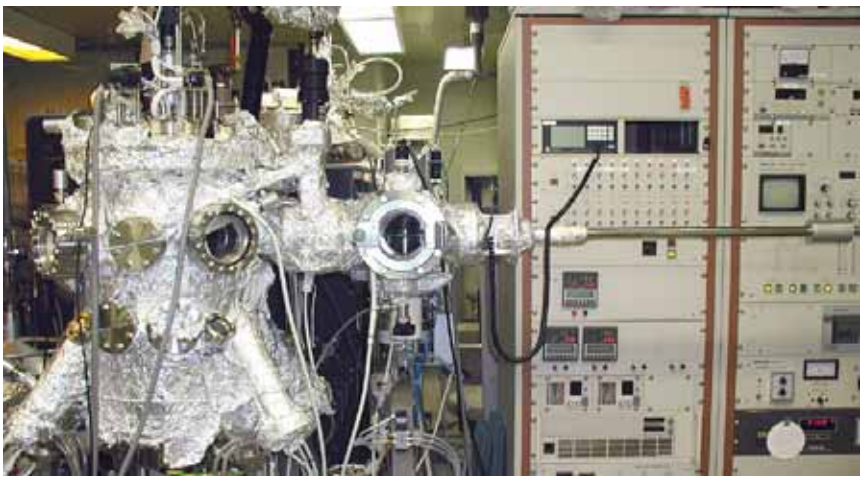


Fig. 2.4 Photo of the MBE system

2.1.4 Rapid Thermal Annealing (RTA)

In this study, RTA (rapid thermal annealing) is used for thermal process after depositing process. The silica tube filled O_2 or N_2 (flow rate are 1.2 L/min) in atmospheric pressure. Therefore it is impossible to remove contaminant gas perfectly in tube. Equipment image was show in Fig.2.5.

Fig2.5 RTA (MILA3000 made in SNKU-RIKO company)

2.1.5 Vacuum Evaporation Method

High-vacuum evaporation was simple method for forming metal electrode like Pt, Al and Ag. In high vacuum chamber, metal source is evaporated by thermal heating with high voltage and is deposited on substrate covered metal mask. In this study, tungsten electrical resister is used for heating Al source that has low melting point (660.37°C) in case by n type substrate and Ag source (961.93°C). This method is possible to contaminate films. Equipment image was show in Fig.2.6 and Fig 2.7(Photo).

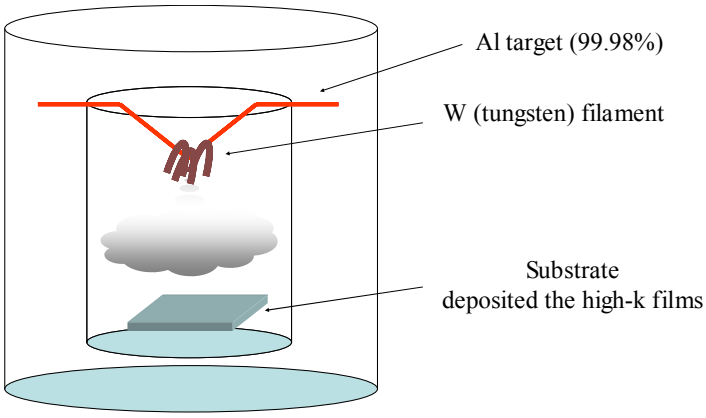


Fig2.6 Metal electrode deposition

Fig2.7 High-vacuum bell jar for metal deposition

2.1.6 Transistor (n-MISFET) process

In this study, the transistor is using n-channel Metal-Insulator-Silicon Field Effect Transistor (n-MISFET). The fabrication process is the identical to n-MIS Capacitor until Al electrode deposition. After photo process is carried out, the gate or source and drain are generated through wet processes as etching. Finally, Al is left from Si substrate as lift-off with Supersonic wave (SSW). Figure 2.8 shows n-MISFET process flow. The photo process flow is shown Figure 2.9.

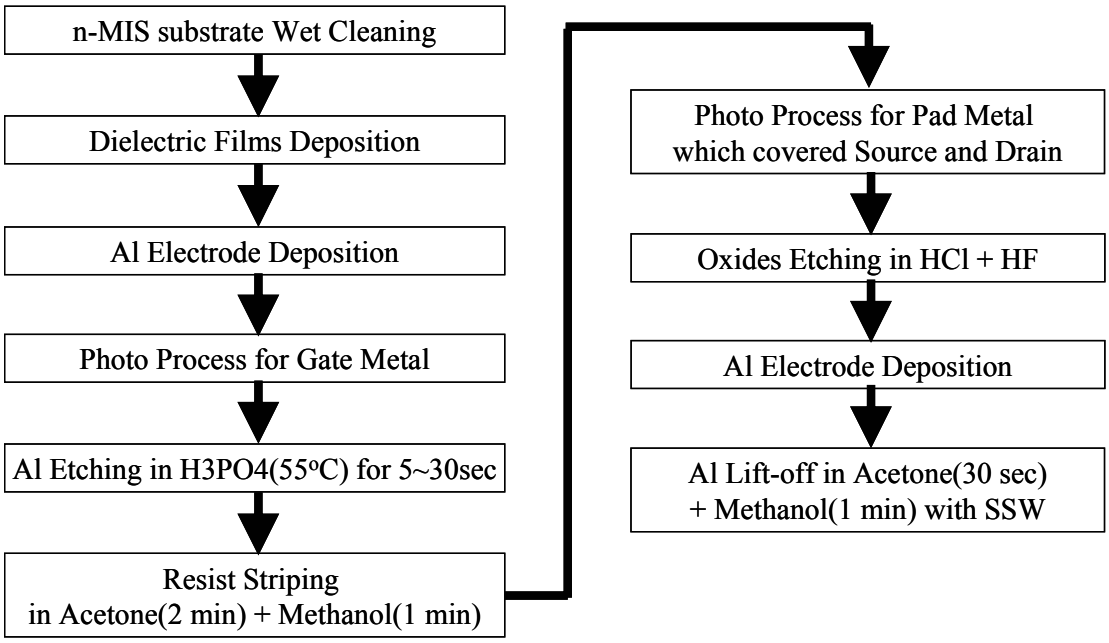


Fig2.8 n-MISFET process flow

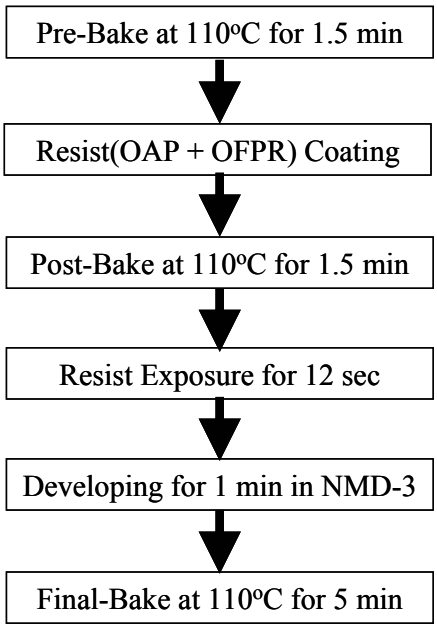


Fig2.9 Photo process flow

2.2 Measurement Equipments

2.2.1 C-V Measurement

In this study, 4284A precision LCR meter made by HP measured C-V characteristics. Measurement frequency was 1 kHz~1MHz. Figure 2.10 shows the photo in front of LCR meter equipment.

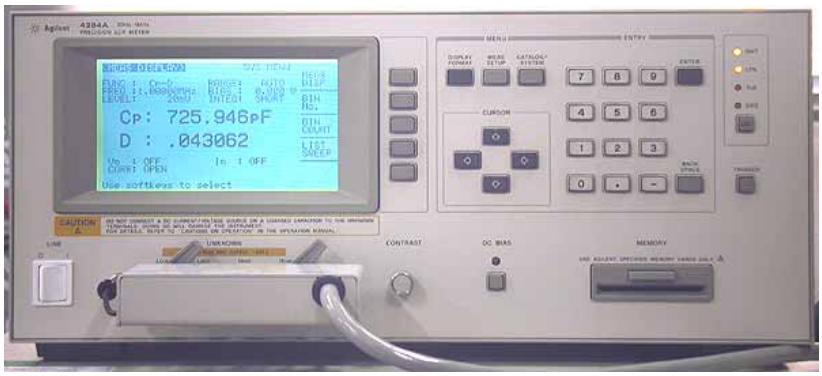


Fig 2.10 LCR meter HP 4284A.

2.2.2 J-V measurement

The one of important electrical properties to estimate high-k films is I-V characteristics. I-V characteristics were measured to evaluate leakage current characteristics. Measurement range were 10^{-14} A ~ 0.4 A. 4156C type precision semiconductor parameter analyzer made by HP measured them.

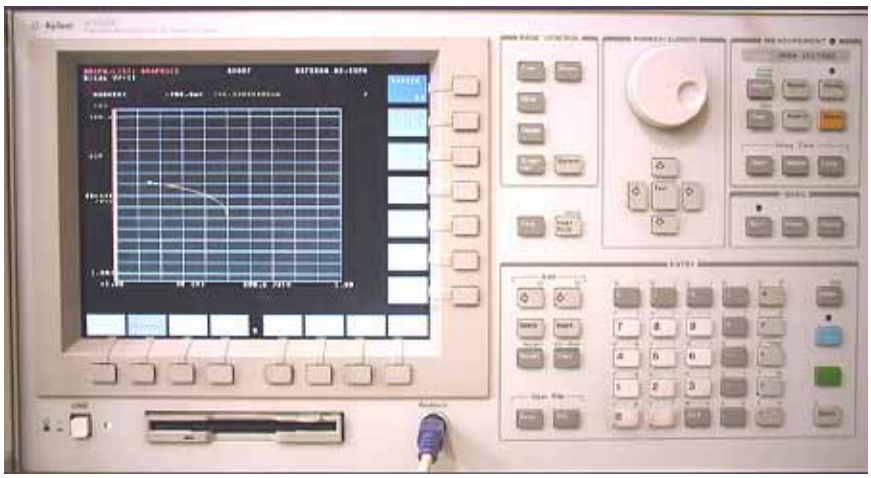


Fig 2.11 Semiconductor parameter analyzer HP 4156C

2.2.3 Atomic Force Microscopy (AFM)

AFM enables to measure surface morphology by utilizing force between atoms and approached tip. The roughness of sample surface is observed precisely by measurement of x-y plane and z. Fig.2.12 shows the principle of AFM.

Tip is vibrated during measurement, and displacement of z direction is detected. This method is called tapping mode AFM (TM-AFM). Resolution limit for normal AFM is 5 ~ 10nm depending on distance between sample surface and tip. On the other hand, resolution limit for TM-AFM is depended on size of tip edge. Thus, resolution limit for TM-AFM is about 1nm.

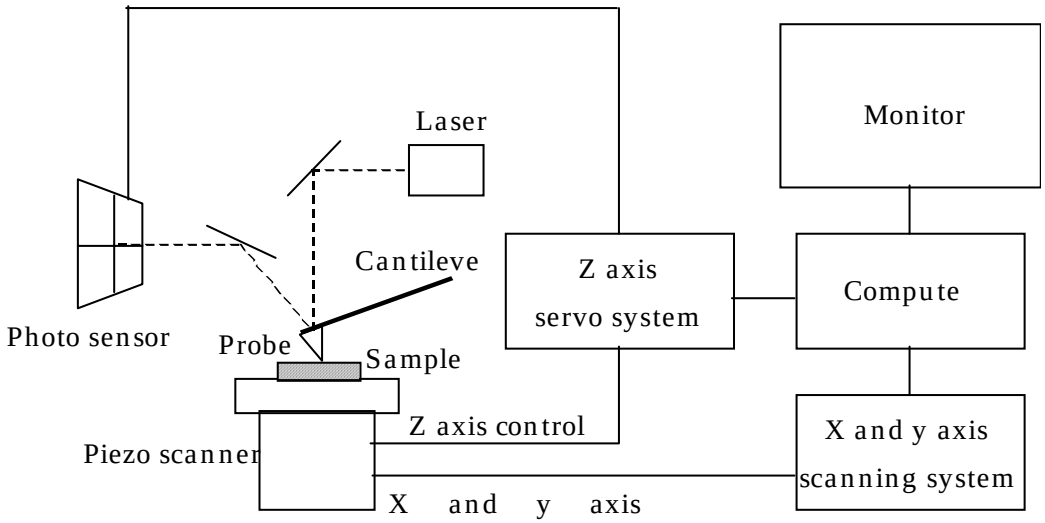


Fig.2.12 Principle of AFM

2.2.4 X-ray Photoelectron Spectroscopy (XPS)

XPS, also known as Electron spectroscopy for chemical analysis (ESCA) is one of the availability methods that estimate thin film and Si interface.

Fig.2.13 shows the schematic drawing of XPS equipment that was used in this study. During analysis, the pressures of main chamber were about 10^{-9} Torr vacuums with turbo pomp. Surface analysis by XPS is accomplished by irradiating a sample with monoenergetic soft X-ray and analyzing the energy of the detected electrons. Non-monochromatic MgKα (1253.6 eV) X-ray is used in this study. The method is illustrated with the energy band diagram in Fig.2.14. This photoelectron has limited penetrating power in a solid on the order of 1-10 μm. They interact with atoms in the surface region, causing electrons to be emitted by the photoelectric effect. The emitted electrons have measured kinetic energies given by

$$KE = h\nu - BE - \phi_s \qquad (2.1)$$

where hυ is the energy of the photoelectron, BE is the binding energy of the atomic orbital from which the electron originates and ϕs is the spectrometer work function (4.8 eV).

The binding energy may be regarded as the energy difference between the initial and final states of the ion from each type of atom, there is a corresponding variety of kinetic energies of the emitted electron. Because each element has a unique set of binding energies, XPS can be used to identify and determine the concentration of the elements

in the surface. Variation in the elemental binding energies (Chemical shift) arises from difference in the chemical potential and polarizability of compounds. These chemical shifts can be used to identify the chemical states of the materials being analyzed.

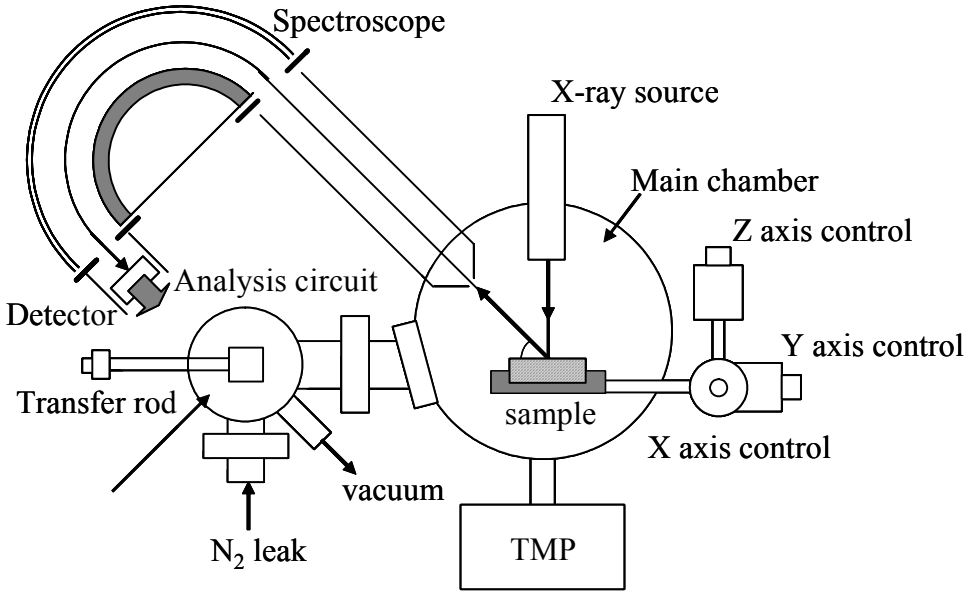


Fig. 2.13 XPS schematic, physical electronics PHI5600 ESCA spectrometer

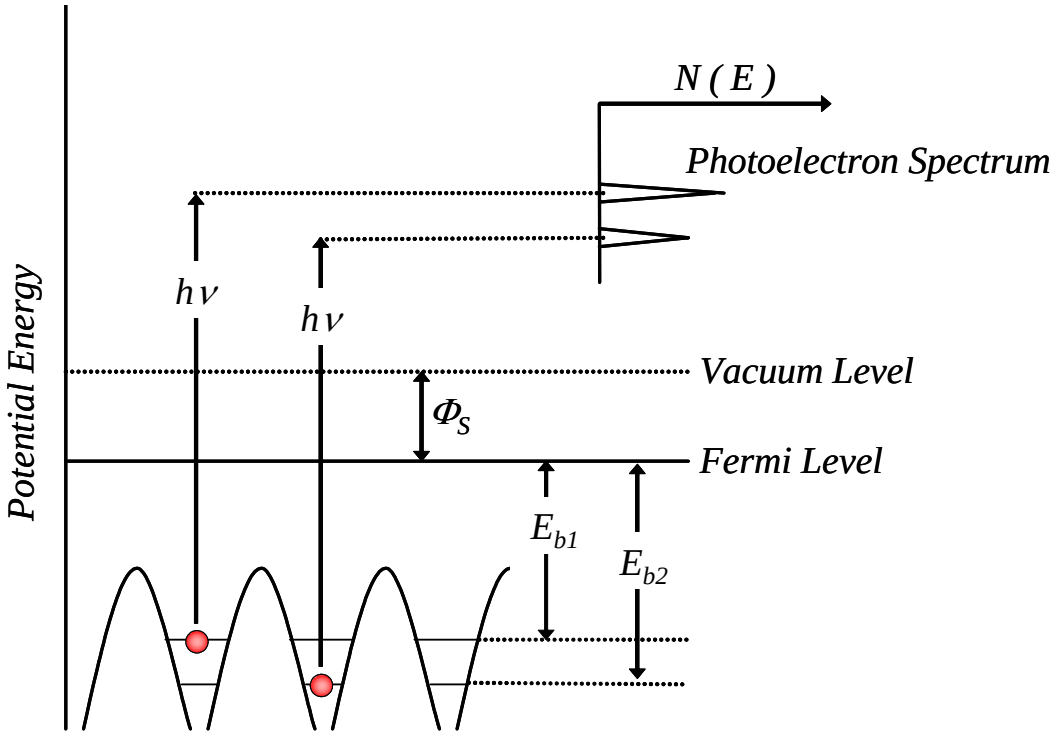


Fig. 2.14 Illustration of measurement method with the energy band diagram

2.2.5 Ellipsometer

Ellipsometory is the method to estimate the optical property of material or surface film thickness measuring the change of polarization condition caused by the reflection of light. Generally, when light is illuminated to a material, the polarization condition of incident light and reflected light are different. This method evaluates the surface condition from this difference. P component of polarized light is horizontal to the plane formed by incident and reflected light and vertical component is S. Ordinary non-polarized light becomes linear polarized light in which the phase and intensity are the same between P and S polarization component when it was passed through 45^{o}-declined polarizer. When the linear polarized light is illuminated to the material, phase different Δ arises between P and S component in the reflected light. Also, the reflection intensity is different between P and S component of polarized light because the reflectance of P and S component is different at the material surface (Fig. 2.15).

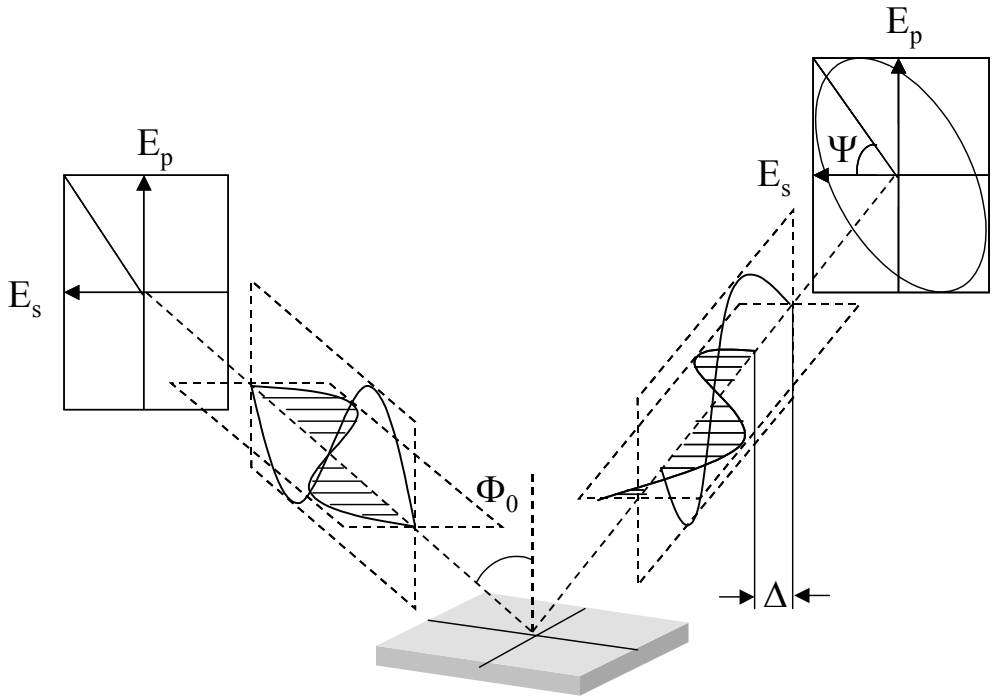


Fig. 2.15 Illustration of the measurement principle for ellipsometer

P and S component in electric field vector of the reflected light are given by

$$E_p = a_p \cos(\omega t - \delta_p)$$
$$E_s = a_s \cos(\omega t - \delta_s) \qquad (2.1)$$

Here, a_p, a_s, are amplitudes of P and S direction respectively. δ_p and δ_s express the phase deviations in the each component. Introducing the relation $\delta_p - \delta_s = \Delta$, the following equation is obtained.

$$\frac{{E_p}^2}{{a_p}^2} + \frac{{E_s}^2}{{a_s}^2} - 2\frac{E_p}{a_p}\frac{E_s}{a_s}\cos\Delta = \sin^2\Delta \qquad (2.2)$$

This equation expresses ellipse in general. The condition of elliptically polarized light is determined by the relative phase difference Δ and reflection amplitude ratio. Taking the tangent, reflection amplitude ration is expressed as reflection amplitude angle ψ. Ellipsometer measures and determines Δ and Ψ or cosΔ and tanΨ.

Following system is assumed for the typical measurement. The system consists of ambient, thin film, and substrate.

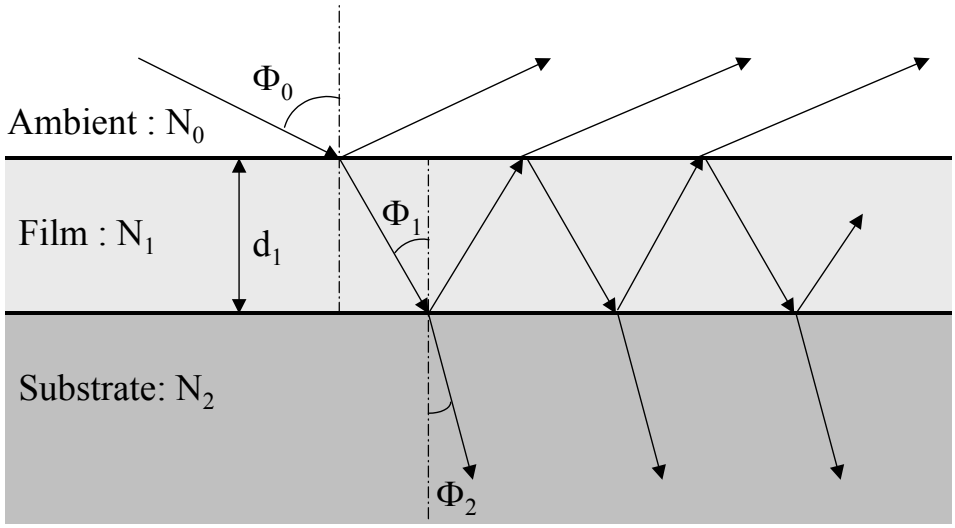


Fig. 2.16 System of three layers for typical measurement

The relation between reflectance ratio in P, S component of polarized light and ellipso parameter is expressed as

$$\tan \Psi e^{j\Delta} = \frac{R_p}{R_s} \tag{2.3}$$

Here, Rp and Rs are complex reflection constant (Fresnel constant). Giving complex refraction $N_i = n_i - jk_i$, Fresnel constant at the each interface is given by

$$r_{i,i+1p} = \frac{N_i \cos\Phi_{i-1} - N_{i-1} \cos\Phi_i}{N_i \cos\Phi_{i-1} + N_{i-1} \cos\Phi_i}$$
$$r_{i,i+1s} = \frac{N_{i-1} \cos\Phi_{i-1} - N_i \cos\Phi_i}{N_{i-1} \cos\Phi_{i-1} + N_i \cos\Phi_i} \tag{2.4}$$

The phase angle β_i in the i layer film is

$$\beta_i = 2\pi\left(\frac{d_i}{\lambda}\right) N_i \cos\Phi_i \tag{2.5}$$

Here, d_i is film thickness, λ is wavelength of incident light and φ_i is incident angle in the i layer. Using these parameter,

$$R_p = \frac{r_{o1p} + r_{12p} e^{-j2\beta_1}}{1 + r_{o1p} r_{12p} e^{-j2\beta_1}}$$
$$R_s = \frac{r_{o1s} + r_{12s} e^{-j2\beta_1}}{1 + r_{o1s} r_{12s} e^{-j2\beta_1}} \tag{2.6}$$

Therefore, if complex refraction in each layer, incident angle and wavelength of light at measurement are known, film thickness can be calculated by measuring ellipso parameter.

Chapter 3

Experimental Results

3.1 Fabrication Procedure

The fabrication flows of single layer and stacked layers structure MIS capacitors are shown in Fig 3.1. First, Si substrate was cleaned by wet process. Next, the rare earth oxides were deposited on the Si substrate by the MBE system. The Si substrate temperature is 250°C during the deposition. Then, these samples were annealed at 300-600°C for 5 minutes by RTA (Rapid Thermal Annealing) Finally, Al electrodes were deposited on the top and bottom of samples.

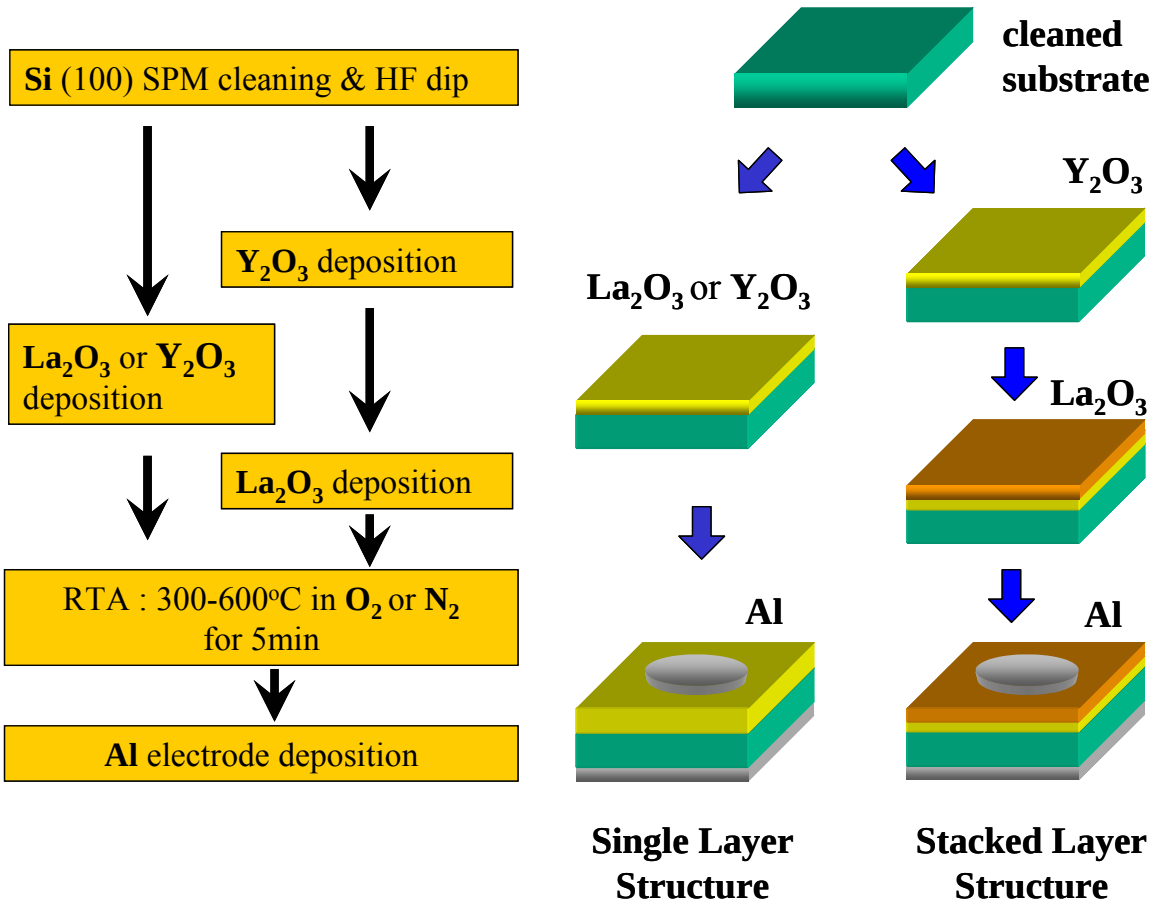


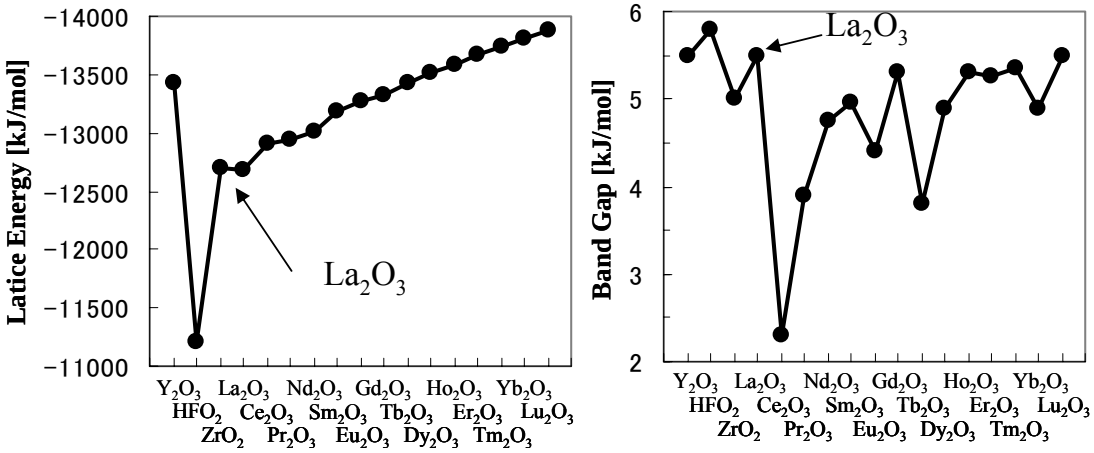
Fig. 3.1 The fabrication flow of single layer and stacked layers structure MIS capacitors

3.2 Characteristics of La_2O_3

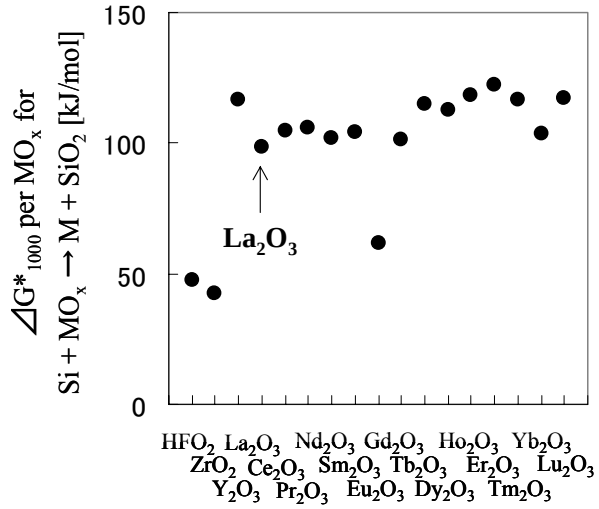
In this section, physical properties of La_2O_3 will be described and the measurement results of electrical characteristics (J-V, C-V), AFM and XPS and the calculated data from the results of electrical characteristics will be shown.

3.2.1 Physical Properties of La_2O_3

Lanthanum oxide (La_2O_3) is one of the rare earth oxides. Fig. 3.2 shows band gap, lattice energy and Gibbs free energy for $Si + MO_x \rightarrow M + SiO_x$ reaction of La_2O_3. La_2O_3 is the material that has the largest band gap and the lowest lattice energy in the rare earth materials. Therefore, in the case using La_2O_3 as the insulator, it is expected that the leakage current will be suppressed because of high barrier height in alignment with Si conduction band. And, it is also expected that increasing of leakage current owing to the crystallization will be also suppressed because of low lattice energy. The dielectric constant is very high value reported value is 27[8]. Table 3.1 shows physical properties of La_2O_3. Therefore La_2O_3 is one of the expected materials as alternative insulator material. However, La_2O_3 has the problem which is increasing of EOT owing to growth of interfacial layer by annealing process.



(a) Lattice energy (b) Band gap



(c) Gibbs free energy

Fig. 3.2 Physical properties of La_2O_3

Table 3.1 Physical properties of La_2O_3

Band gap [eV]	5.5
Lattice energy [kJ/mol]	-12687
Relative dielectric constant	27
Gibbs free energy [kJ/mol]	98.47

3.2.2 Characteristics of La_2O_3

In this section, the characteristics of La_2O_3 will be shown. Specially, the effect of annealing condition was investigated. La_2O_3 was deposited about 5nm on Si substrates by MBE. The temperature of substrate during the deposition was 250oC and the rate of deposition is ~0.1nm/1min. The C-V characteristics were measured at 10 kHz, 100 kHz and 1 MHz frequencies.

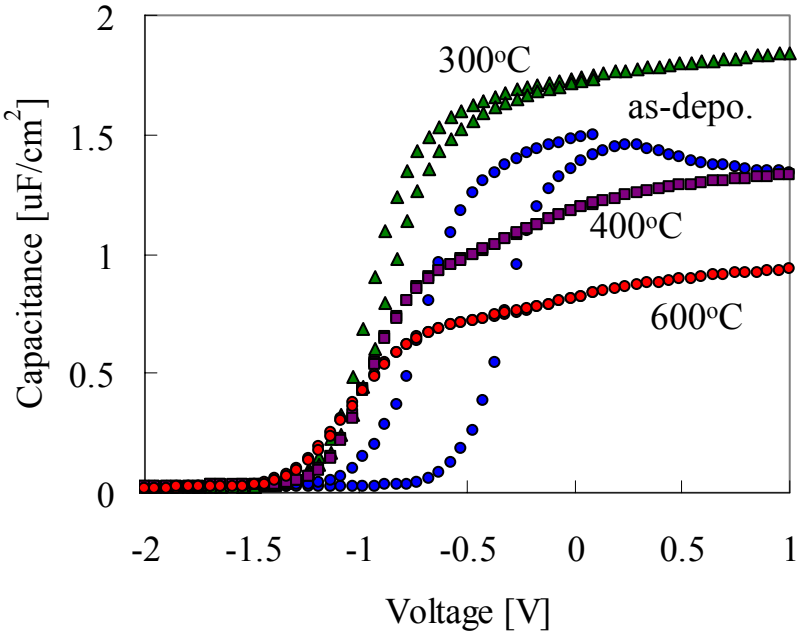
3.2.2.1 Electrical Characteristics

Fig. 3.3 shows the C-V characteristics of the samples with/without annealing measured at 1 MHz frequency. Annealing temperatures were 300°C-600°C and annealing ambient were O_2 and N_2. The annealing time of both O_2 and N_2 annealing was 5 minutes.

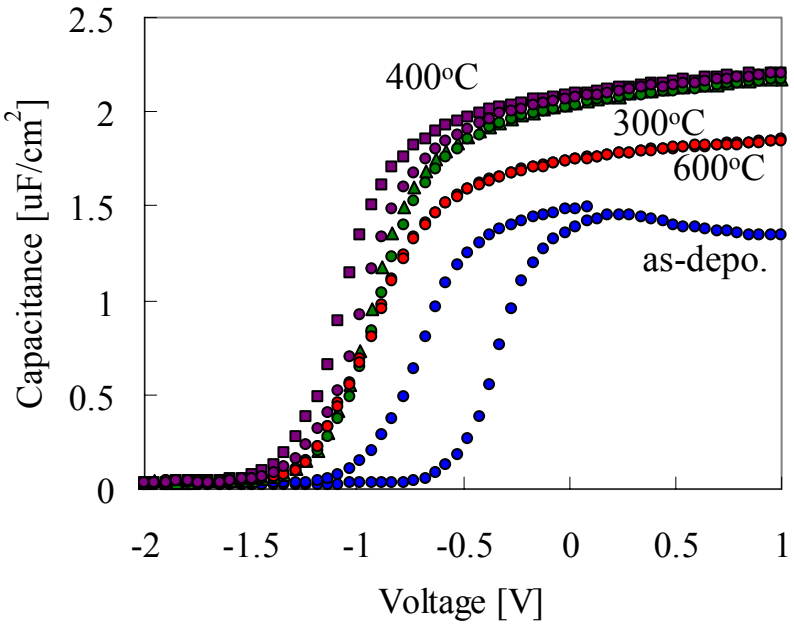
In the case of O_2 annealing, the large hysteresis was observed for the as-deposited film. The other annealing films suppressed the hysteresis compared with as-deposited film. In 400oC annealing, the hysteresis was especially suppressed. The accumulation capacitance value was the highest in 300oC annealing (EOT is 1.5nm). And in 400oC annealing or more temperature, the capacitance values were decreased and gradually increased at accumulation region without being saturation. This phenomenon is suggested that the low dielectric interfacial layer such as SiO_2 and/or La-Silicate was grown between the insulator and Si substrate by the annealing process. Fig. 3.4 shows the change of the flat band voltage calculated from C-V curve with annealing temperature. The ideal flat band voltage when using Al electrode for n-Si is

about +2.0 V. The flat band voltage is slightly decreased with increasing annealing temperature. In 300oC annealing, lowest flat band voltage was obtained, but in other conditions, hardly the change of the value was observed. It is suggested that these very large flat band voltages were due to many positive fixed charged exist in the films.

In the case of N_2 annealing, 400oC annealing sample was obtained the highest capacitance value (EOT is 1.3 nm), however, the largest hysteresis that is about 0.1 V was observed in annealing samples. The similar capacitance value was obtained in 300oC annealing sample. There is not big change in the characteristic observed compared with O_2 annealing. The change in flat band voltage is shown in Fig. 3.4. As these results, the good characteristics were obtained by the annealing process.



(a) O_2 annealing



(b) N_2 annealing

Fig. 3.3 C-V characteristics for 5nm thick La_2O_3 films

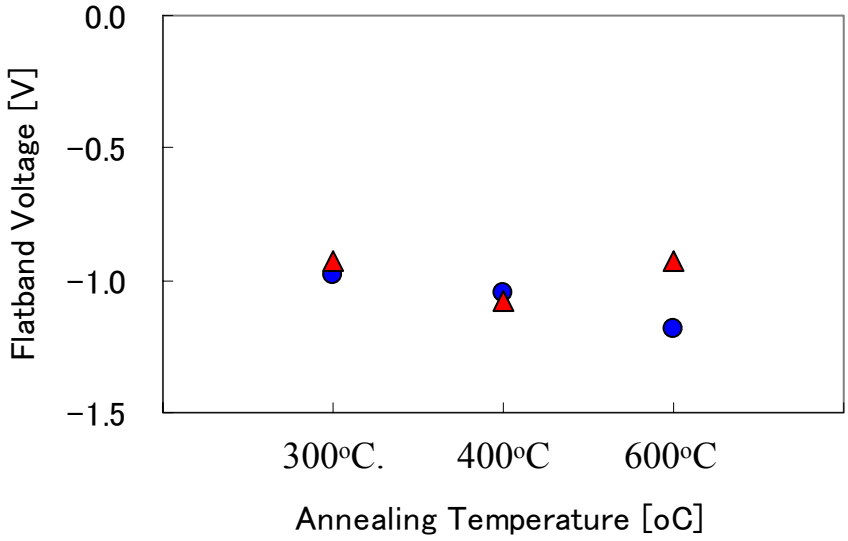


Fig. 3.4 Flat band voltage for O_2 or N_2 annealed 5nm thick La_2O_3 films

Fig. 3.5 and Fig. 3.6 show the dependences of C-V characteristic on the measurement frequency. These results are same samples as mentioned above which are as-deposited sample and annealed samples at 300-600oC in O_2 or N_2 ambient. The measurement frequencies were 1 MHz, 100 kHz and 10 kHz. In the case of O_2 annealing shown in Fig. 3.5, frequency dependencies were observed at depletion region. In 400oC and 600oC annealing, the strong dependencies were observed. In 300oC annealing case, frequency dependence was weak. However, small bump appeared at the weak inversion region. At the accumulation region, frequency dependence was hardly observed. In the case of N_2 annealing shown in Fig. 3.6, frequency dependencies were observed. Particularly, strong dependencies that are decreasing capacitance with decreasing frequency were observed in all annealing samples. And, similar to O_2 300oC annealing, small bumps were observed at the weak inversion region suggesting that the interfacial state was existed.

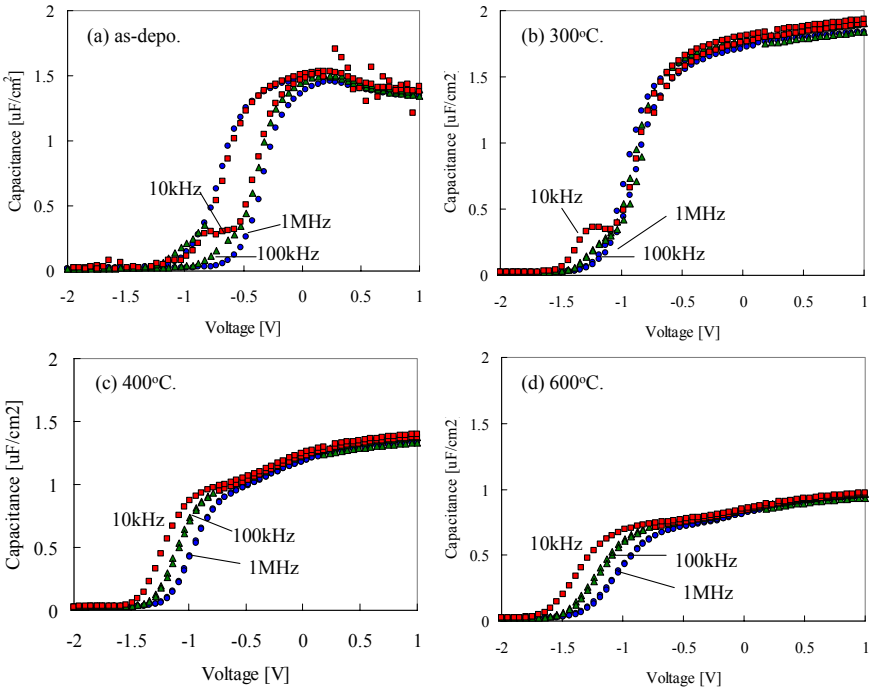


Fig. 3.5 Dependence of C-V characteristics on measurement frequency for O_2 annealed films

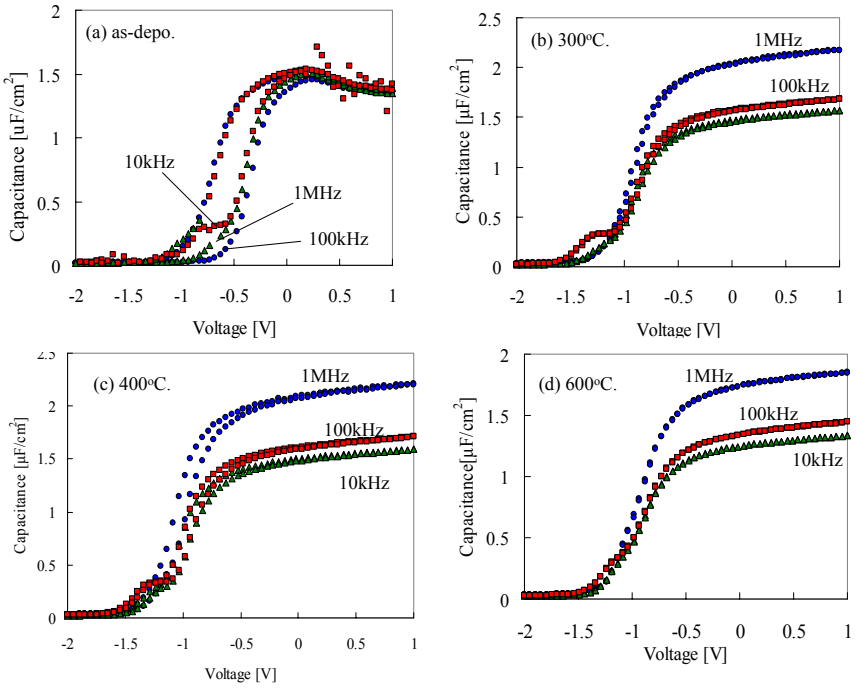
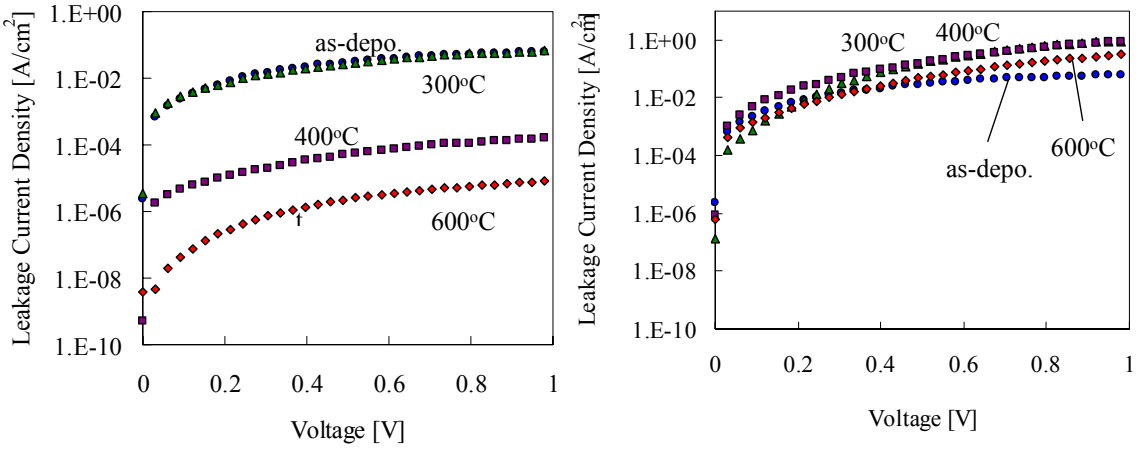


Fig. 3.6 Dependence of C-V characteristics on measurement frequency for N_2 annealed films

Fig. 3.7 shows the dependence of J-V characteristics on annealing temperature. In the case of O_2 annealing, the highest leakage current density was observed in as-deposited sample, and continuously decreased with increasing annealing temperature. The leakage current density was suppressed about three orders of magnitude between 300oC and 400oC annealing. And in the N_2 annealing case, the lowest leakage current was observed in as-deposited sample. In 300oC and 400oC annealing, the almost same leakage currents were observed, and in

600oC annealing, the middle value between as-deposited and 300oC (400oC) annealing was observed.



(a)O_2 annealed films (b)N_2 annealed films

Fig. 3.7 J-V characteristics for 5nm thick La_2O_3 films

Fig. 3.8 shows the J-EOT relationships for La_2O_3. The vertical line represents the leakage current density at Vg = 1V and horizontal line represents EOT (Equivalent Oxide Thickness). In the Both O_2 and N_2 annealing, leakage current was decreased and EOT was increased with increasing annealing temperature. In O_2 annealing, the obvious change was observed between 300oC annealing and higher temperature annealing than 300oC. These results suggested the sudden growth of low dielectric interfacial layer at over 300oC annealing as mentioned above. In the case of N_2 annealing, the change was hardly observed by change of annealing temperature compared with O_2 annealing.

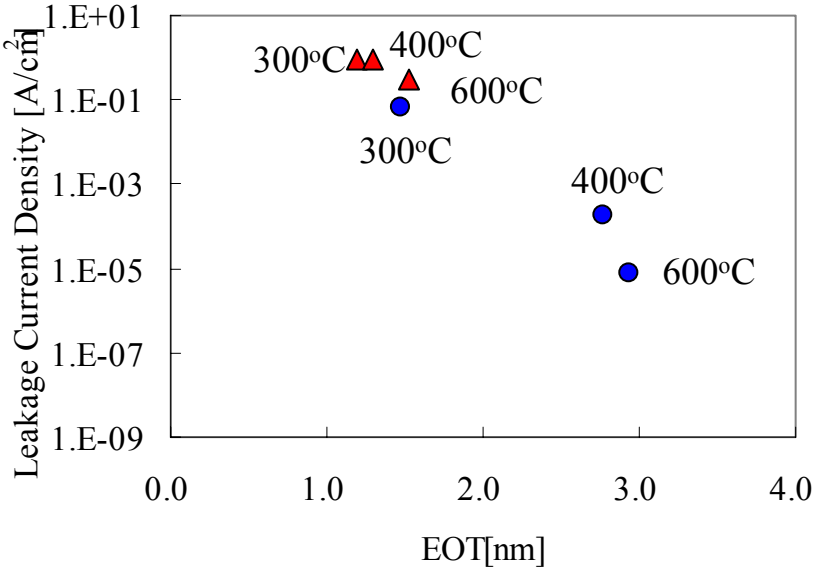
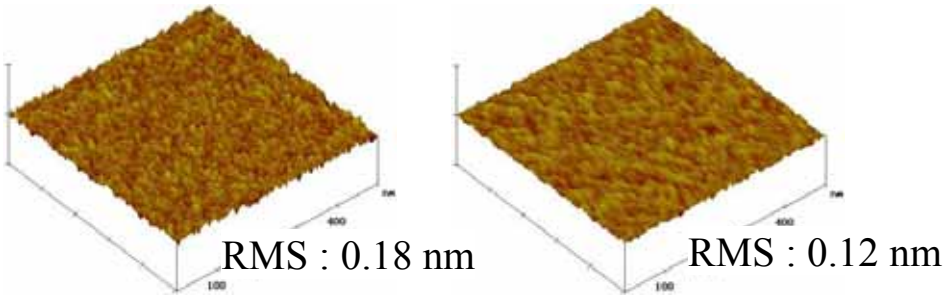


Fig. 3.8 J vs EOT plots for annealed La_2O_3 films

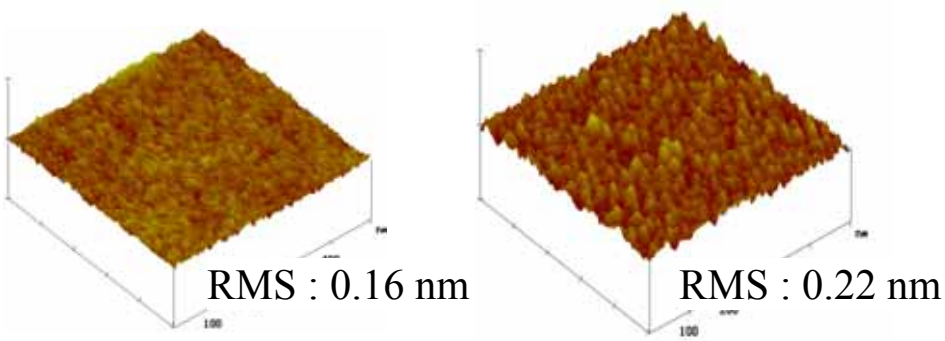
3.2.2.2 Surface Morphology

Fig. 3.9 and Fig. 3.10 show the surface morphologies and RMS (Root Mean Square) roughness values of the AFM (Atomic Force Microscope) images of the O_2 annealing films respectively. These results were measured before depositing electrode on the top of the samples. In other words, the surface of insulator film was measured. The scan size was 500 x 500 nm and the z direction was 5 nm/div.

The lowest value 0.12 nm was obtained in 300oC annealing. And the surface roughness was deteriorated with increasing annealing temperature. However, the distribution range of values was narrow that is 0.12-0.22 nm. These results are expected to have no crystallization for La_2O_3 film below 600oC annealing.



(a) as-deposition (b) 300 °C annealing



(c) 400 °C annealing (d) 600 °C annealing

Fig. 3.9 AFM images for O_2 annealed 5nm thick La_2O_3 films

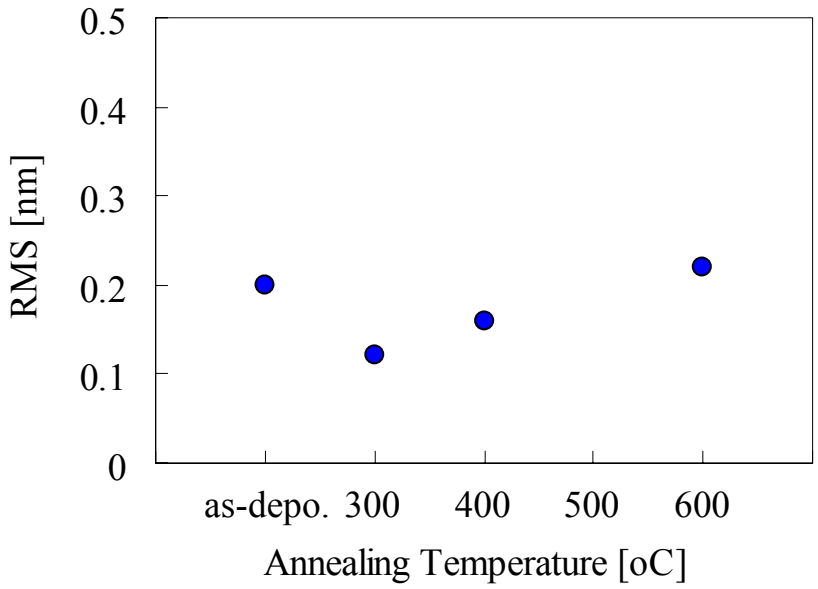


Fig. 3.10 RMS roughness values for O_2 annealed 5nm thick La_2O_3 films

3.2.2.3 XPS Analysis

In order to investigate the composition of the films before and after RTA, XPS analyses were carried out. The analyses were made at a take-off angle of 30o, 45° and 60oC for all samples. Fig. 3.11 shows the wide scan XPS spectra for the 4nm thick La_2O_3 film after RTA at 600oC in O_2 ambient. The spectrum peaks mainly appeared that are La3d, La4d, La4p, Si_2p, O1s, C1s and Si_2p. The narrow scan spectra are shown in Fig. 3.12 and Fig. 3.13. These figures show the spectra of before and after annealing, respectively and the spectral regions containing the Si2s, O1s and La3d peaks are displayed. For the Si2s spectra in Fig. 3.12 (a) we were able to probe the Si dielectric interface and detect the substrate Si peak at 151 eV[17] in the Si2s spectra. In before annealing, a SiO_2 peak at 153.3 eV was hardly observed shown in Fig. 3.12 (a), but after RTA, that peak clearly appeared shown in Fig. 3.13(a). This result indicates that a SiO_2 layer was grown. The Fig. 3.12 (b) and Fig. 3.13 (b) show the O1s spectra. The single peak was observed at ~532 eV in before RTA, this peak lies between the SiO_2 and La_2O_3 peaks at 533.3 and 529.9 eV[18] respectively. These spectrum peaks represents the formation of La-O-Si silicate bonding units. And in after annealing, the shoulder at ~ 533.0 eV is clearly visible and also indicates the presence of a SiO_2 interfacial layer. The La3d spectra in Figs. 3.12 (c) and 3.13 (c) were hardly changed between before and after annealing. These results were considered that La-Si-O composition was already formed at interfacial layer before annealing and the SiO_2 layer was grown by the annealing at 600oC in O_2.

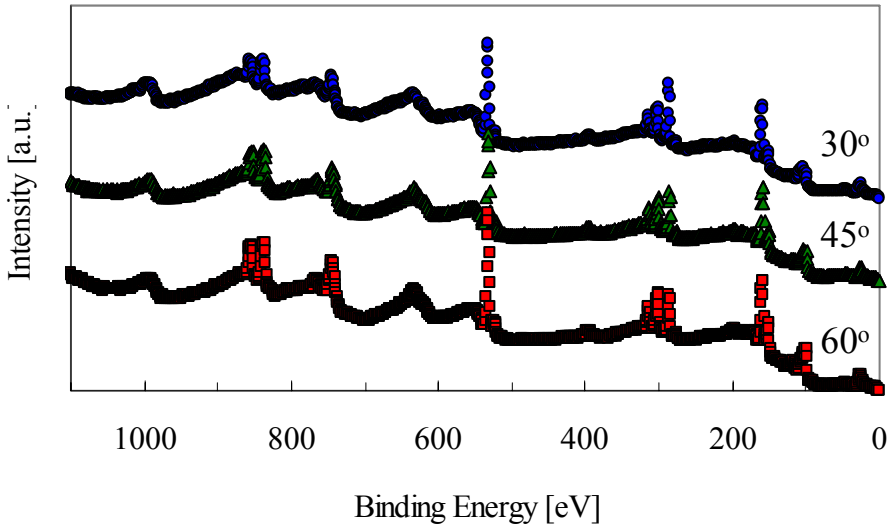
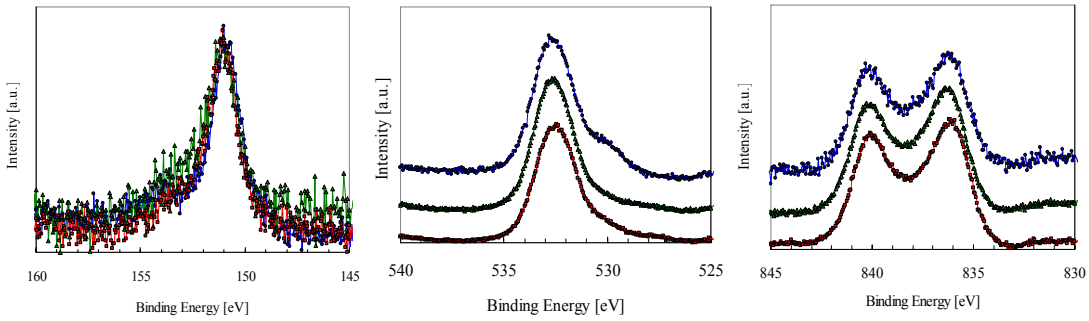
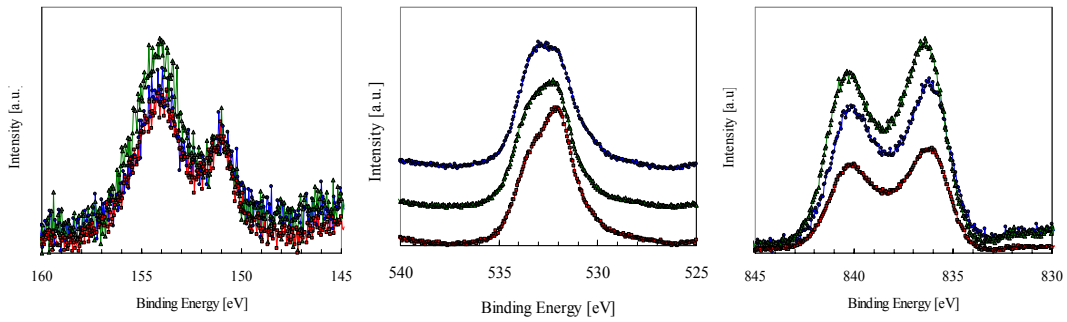


Fig. 3.11 Wide scan XPS spectra for O_2 600oC annealed 4 nm thick La_2O_3 film



(a) Si2s (b) O1s (c) La3d

Fig. 3.12 Narrow scan XPS spectra for 4 nm thick as-deposited La_2O_3 films

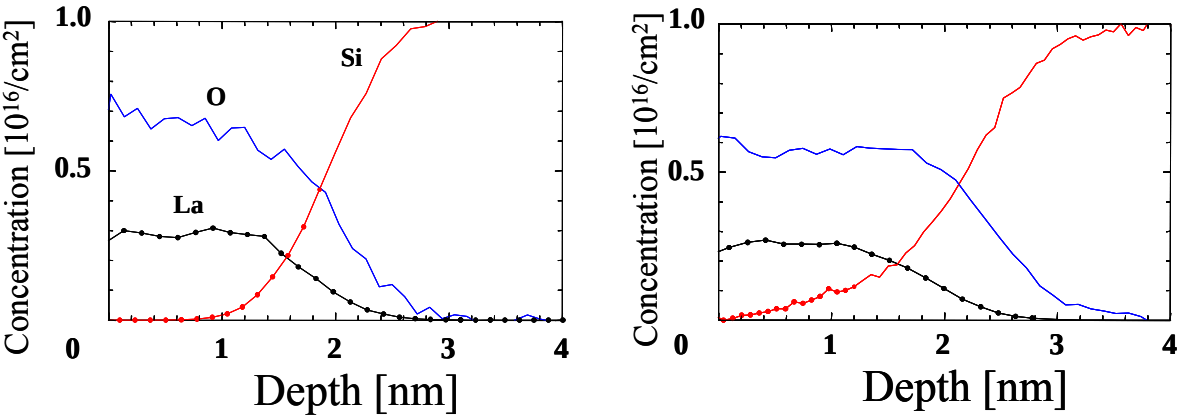


(a) Si2s (b) O1s (c) La3d

Fig. 3.13 Narrow scan XPS spectra for O_2 annealed La_2O_3 films

3.2.2.3 RBS Analysis

Fig. 3.14 (a) and (b) show RBS spectra for 4nm La_2O_3 deposited samples. The samples of (a) and (b) were as-deposition and 300°C annealing, respectively. In as-deposition, Si diffusion had been already observed by the deposition indicating the deposition with heating up Si substrate to 250°C makes Si diffusion to insulator. In 600°C annealing, the slope of Si line was gradual compared with as-deposition sample and the layer which constructs only Si and O was observed at interfacial layer. This result indicates SiO_2 layer was existed. These results were consistent with XPS results.



(a) as-deposition (b) 600°C annealing

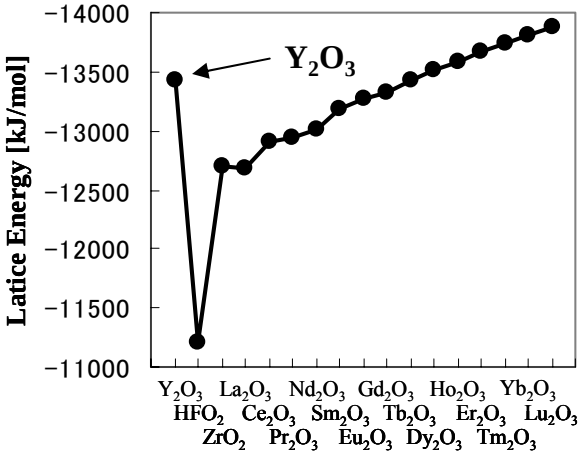
Fig. 3.14 RBS spectra for 4 nm thick La_2O_3 films

3.3 Characteristics of Y_2O_3

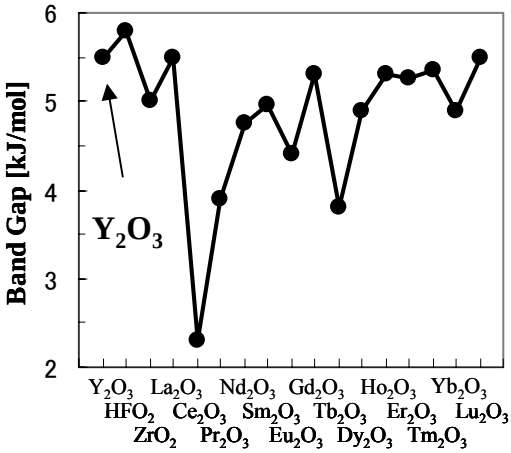
In this section, physical properties of Y_2O_3 will be described and the measurement results of electrical characteristics (J-V, C-V), AFM and XPS and the calculated data from the results of electrical characteristics will be shown.

3.3.1 Physical Properties of Y_2O_3

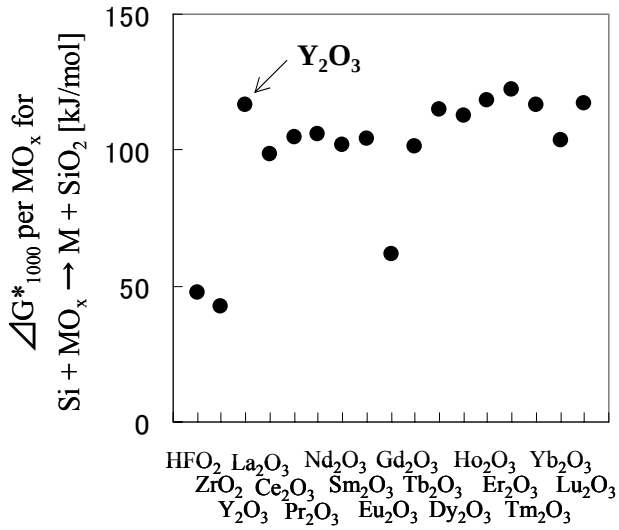
Yttrium oxide Y_2O_3 is also one of the rare earth oxides. This material exhibits attractive features for electronic applications as part of metal-oxide-semiconductors hetero structures used in the MOS transistor[20–23]. Y_2O_3 should be a suitable material for a metal oxide semiconductor because of several particularly relevant physical properties such as a wide band gap that is 5.5 eV same with La_2O_3 shown in Fig. 3.15, a high dielectric constant (~18), high thermal stability, chemical compatibility with silicon, and a low lattice mismatch between the Y_2O_3 and silicon lattice parameters [24–26]. And Y_2O_3 has a high moisture resistance compared with La_2O_3[21]. The Y-O bond is quite strong, since the free energy of formation per oxygen atom ($-\Delta G_f$)(at 25^oC) is $2.40x10^{-22}$ kcal for Y_2O_3 compared to $1.70x10^{-22}$ kcal for SiO_2[21].



(a) Band gap



(b) Lattice energy



(c) Gibbs free energy

Fig. 3.15 Physical properties of Y_2O_3

Table 3.2 Physical properties of Y_2O_3

Band gap [eV]	5.5
Lattice energy [kJ/mol]	-13.438
Relative dielectric constant	18
Gibbs free energy [kJ/mol]	2.40×10^{-22}

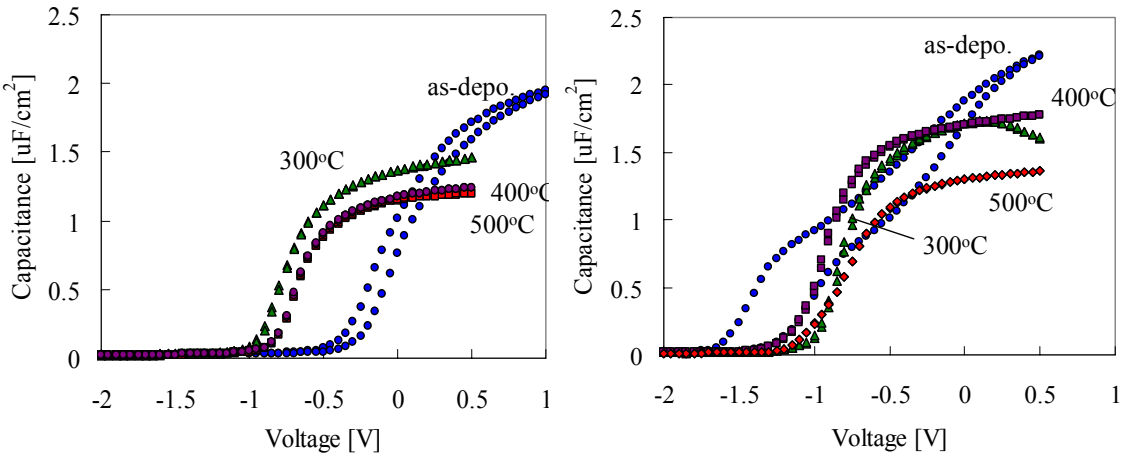
3.3.2 Characteristics of Y_2O_3

In this section, the characteristics of Y_2O_3 will be shown. Specially, the effect of annealing condition was investigated in in common with La_2O_3. Y_2O_3 was deposited about 4nm or 5nm on Si substrates for O_2 annealing and N_2 annealing by MBE and the rate of deposition is ~0.15nm/1min.

3.3.2.1 Electrical Characteristics

Fig. 3.1.5 (a) shows the C-V characteristics for about 5 nm deposited Y_2O_3 films with/without annealing in O_2. These samples were annealed at 300-600oC for 5minutes. And the measurement frequency was 1MHz. The property without annealing has the highest capacitance value and the lowest flat band voltage shift in all O_2 annealing samples. However, the hysteresis was also the largest. In other annealing cases, the hysteresis was suppressed and decreasing of capacitance value with increasing annealing temperature was slight with the largest changes occurring between 300oC and 400oC. There was almost no change of characteristic between 400oC and 600oC. Fig. 3.1.5 (b) shows C-V characteristics for 4nm deposited Y_2O_3 films with/without annealing in N_2 for 5 minutes and annealing temperatures were 300oC, 400oC, and 600oC. In the as-deposited films, although C-V characteristic was not observed, after annealing good characteristics without hysteresis were obtained. The variety was almost nothing between 300oC and 400oC annealing. But after 600oC annealing, capacitance value was decreased suggesting growth of interfacial layer. Fig. 3.1.6 shows the flat band voltage of all of O_2 and N_2 annealing samples. The smallest

flat band voltage was observed at O_2 300oC and 400oC annealing. This result suggested that positive fixed charge in films was deceased by O_2 annealing and almost all these flat band voltages were almost smaller than La_2O_3 films.



(a) O_2 annealing (b) N_2 annealing

Fig. 3.16 C-V characteristics for 4nm and 5nm thick Y_2O_3 films

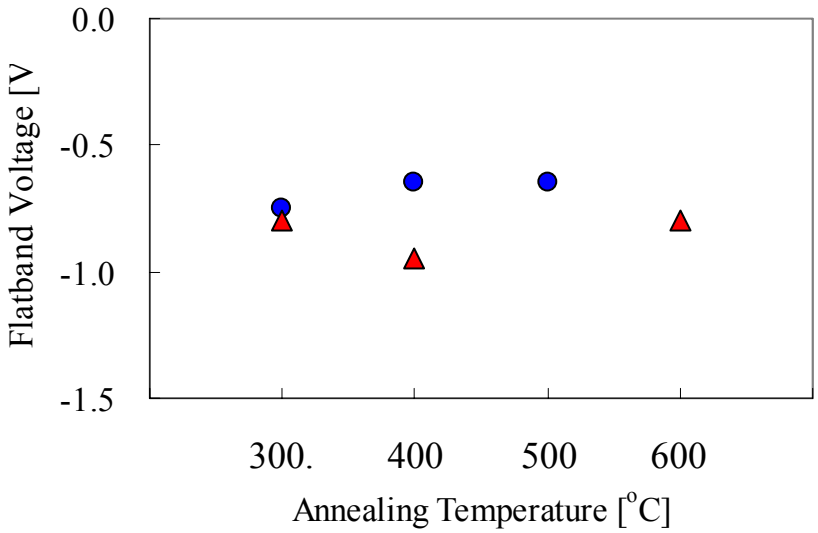


Fig. 3.17 Flat band voltage for O_2 or N_2 annealed 4nm and 5nm thick Y_2O_3 films

Fig. 3.18 and 3.19 show the C-V characteristics of O_2 and N_2 annealing samples with frequency as a parameter respectively. These results are same sample mentioned above that are annealed at 300-600 for 5 minutes. The measurement frequencies were 1 MHz, 100 kHz and 10 kHz.

In both O_2 and N_2 annealing, as-deposited films have strong frequency dependence, particularly that are observed at weak inversion region. However, after annealing these dependences were disappeared for all samples. This point is most different point from La_2O_3 films in C-V characteristics. And other different point from La_2O_3 films are no bump at weak inversion region suggesting no interfacial state.

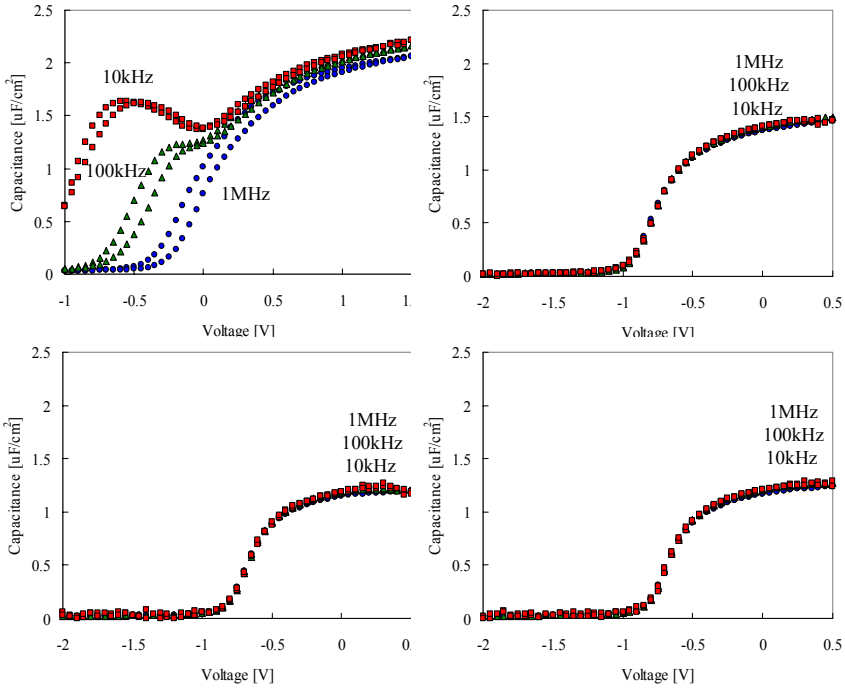


Fig. 3.18 Dependence of C-V characteristics on measurement frequency for O_2 annealed films

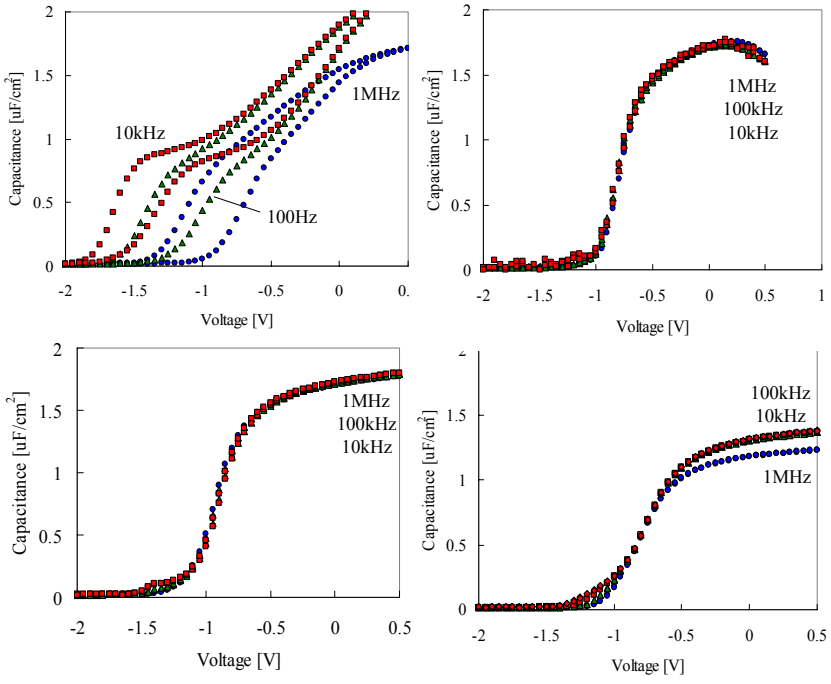
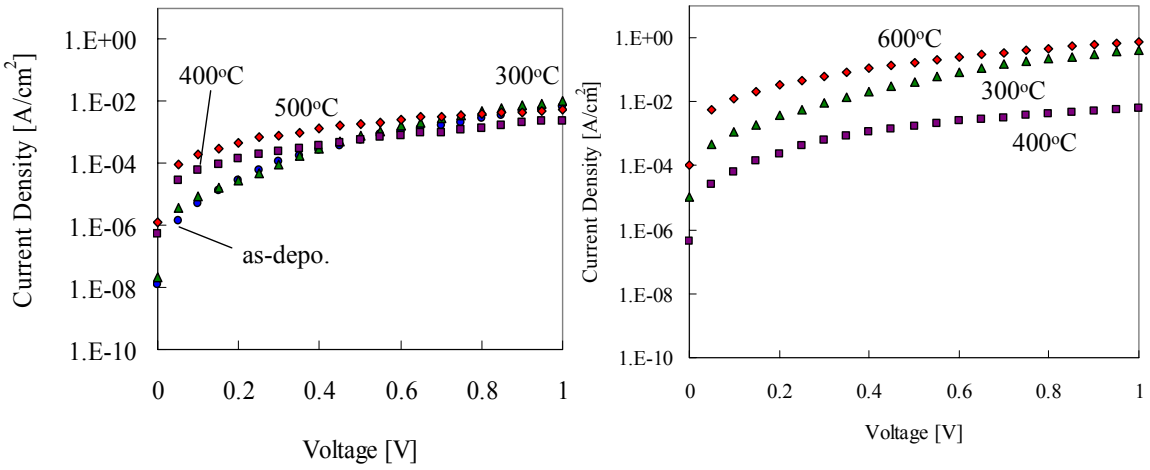


Fig 3.19 Dependence of C-V characteristics on measurement frequency for N_2 annealed films

Fig. 3.20 (a) and (b) show J-V characteristics for 4 nm deposited O_2 annealing sample and 5 nm deposited N_2 annealing sample respectively. In O_2 annealing sample, the leakage currents were hardly changed between all samples. In N_2 annealing sample, decreasing of leakage current densities with increasing annealing temperature was observed. The largest change that is two orders of magnitude was observed between 400oC and 600oC annealing. The leakage current of without annealing sample was not measured so as the C-V curve was unable to obtain.



(a) O_2 annealing (b)N_2 annealing

Fig. 3.20 J-V characteristics for 4nm and 5nm thick films

Fig. 3.21 shows J-EOT relationships for Y_2O_3 films. The change was hardly observed between 300-500oC annealing in O_2 ambient, but in 600oC annealing the increasing EOT was clearly observed with suppression of leakage current density about six orders of magnitude compared with 400oC annealing. In the case of N_2 annealing, 300oC annealing and 400oC annealing were almost same position, but in 600oC annealing, the EOT increasing about 0.5 nm with decreasing of leakage current about

two orders of magnitude. The slopes of O_2 and N_2 annealing were similar slope each other.

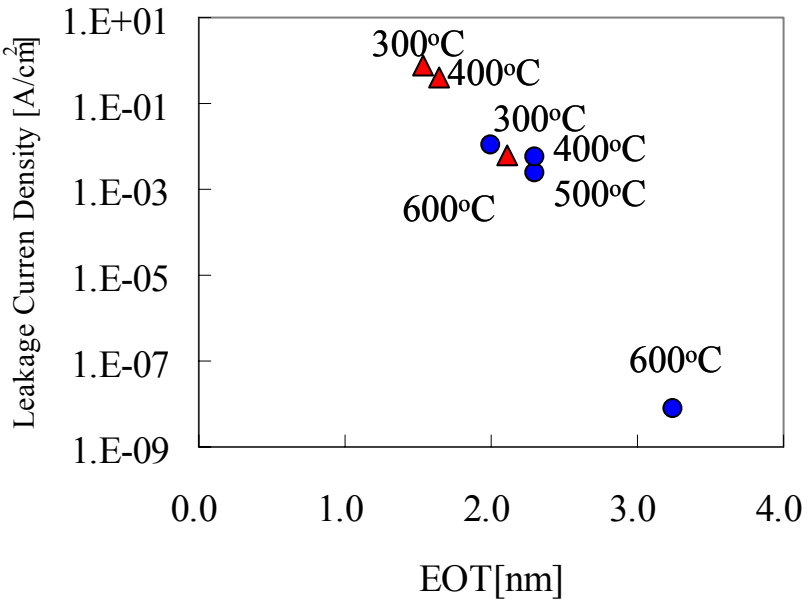
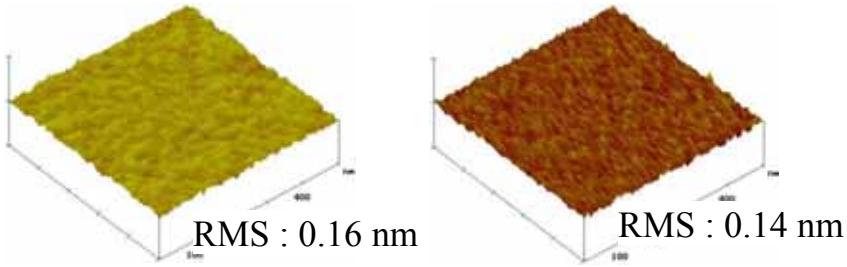


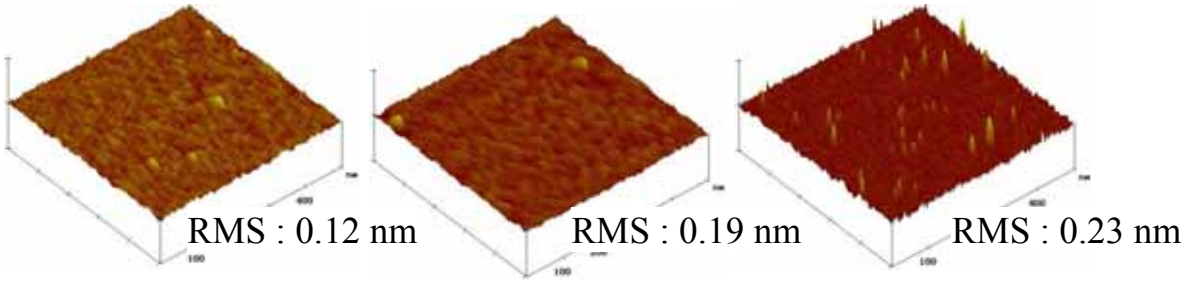
Fig. 3.21 J vs EOT plots for annealed Y_2O_3 films

3.3.2.2 Surface Morphology

Fig. 3.22 shows the surface morphologies and RMS roughness values of the AFM images in the O_2 annealing films respectively. The scan size was 500 x 500 nm and the z direction was 5 nm/div. The RMS value of as-deposited film was 0.16 nm, and the RMS value was improved to 0.12 nm which is smallest value in all samples by the 300oC annealing in O_2 ambient. In the other annealing case, the RMS value of 300oC annealing sample was similar to 400oC annealing sample that value is 0.14 nm. However, the RMS value was increased by higher temperature annealing. The largest value was 0.23 nm for 600oC annealing sample.



(a) as-deposition (b) 300°C annealing



(c) 400°C annealing (d) 500oC annealing (e) 600oC annealing

Fig. 3.22 AFM images for O_2 annealed 4nm thick Y_2O_3 films

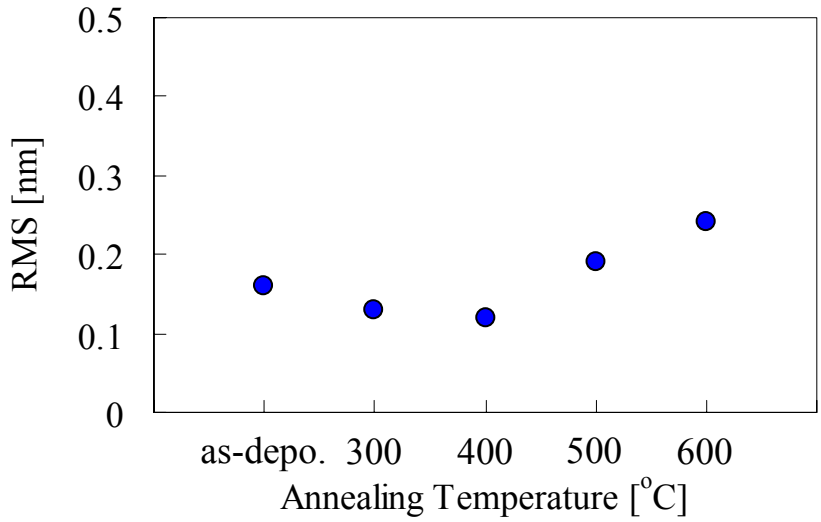


Fig. 3.23 RMS roughness values for O_2 annealed 4nm thick Y_2O_3 films

3.3.2.3 XPS Analysis

Fig. 3.24 shows the wide scan spectra for Y_2O_3 film containing mainly the spectrum regions of Si2p, Si2s, Y3d, C1s and O1s. In Fig. 3.25 (a), (b) and 3.26, XPS results contain the Y3d, Si2s, O1s and Si2p photoelectron spectrum regions for Y-O-Si, Y_2O_3, SiO_2 and Si-Si bonding. Fig. 3.25 (a) presents the Y3d and Si2s photoelectron spectra. The $Y3d_{3/2}$ and $Y3d_{5/2}$ compositions of the spin-orbit splitting are measured at 158.4 and 160.3 eV, respectively indicating that the Y-silicate was formed even before annealing and the absence of Y-silicide in Y-O-Si films, since a metallic Y3d peak at 156.0 eV is not observed. The transition of the peak was not observed after annealing suggesting that the yttrium composition was not changed. In other words, Y-Si-O composition was maintained after annealing. Fig. 3.25 (b) presents the O1s spectra for Y-O-Si, Y_2O_3 and SiO_2. The O1s peak at 531.8 eV is intermediate between O1s for SiO_2 (533.0 eV) and Y_2O_3 (529.5 eV). This peak similarly indicates that the Y-Si-O combination was existed. The measured FWHM of O1s in Y-O-Si is 3.0 eV, which is greater than expected for an elemental oxide (FWHM of SiO_2 is 1.8 eV [14]) indicating the presence of multiple oxygen bonding configuration in the Y-O-Si. Fig.3.26 (a) and (b) show Si2s and Si2p spectra regions, respectively. These figures represented change of peak intensities owing to the annealing. In Fig 3.26 (a), the single peak was observed at 531.8 eV but another peak was appeared at 103 eV by 600oC annealing. This result suggested that the Si-O bonding such as SiO_2 was formed by high temperature annealing. Fig. 3.26 (b) shows Si2p photoelectron peak. In 300oC and 400oC annealing, the peak intensity was weak at 103 eV. However, in 600oC annealing, this peak intensity became strong. This peak indicated similar phenomenon to Si2s which is

growth of interfacial layer. These results indicated that Si rich Y silicate layer was grown at the bottom of the film with increasing annealing temperature.

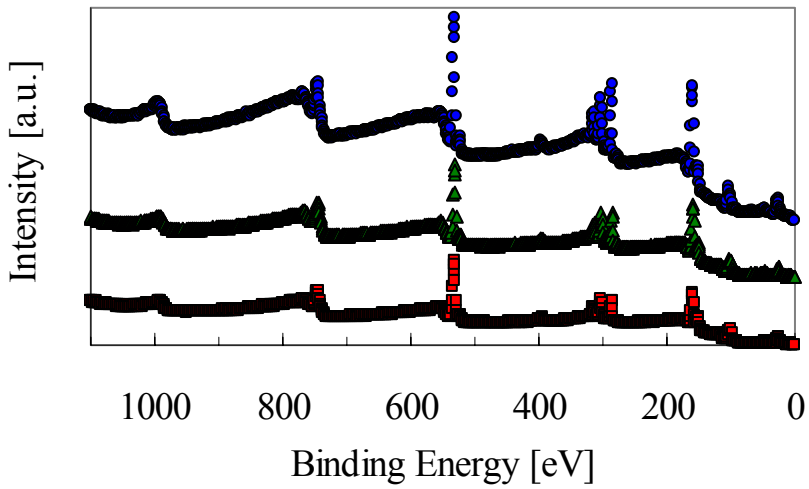
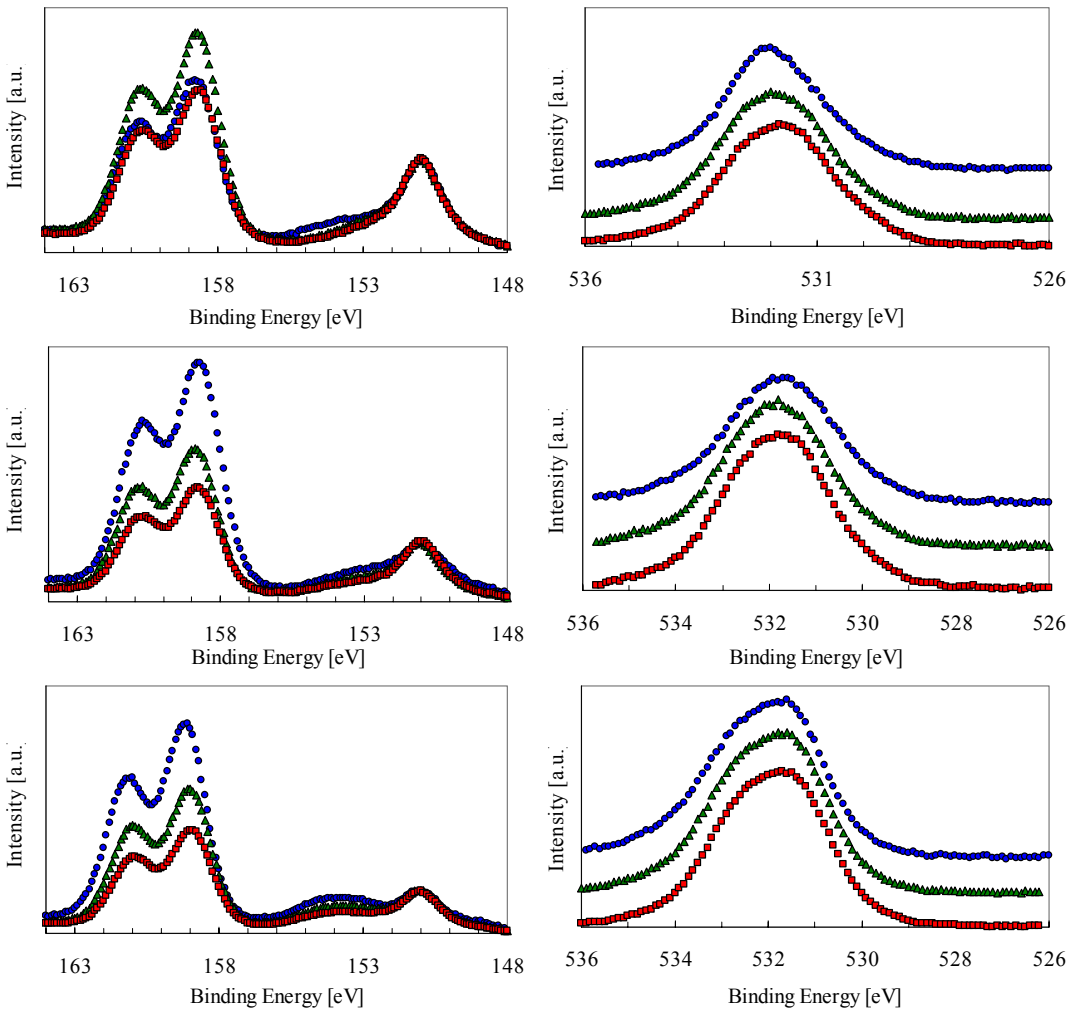
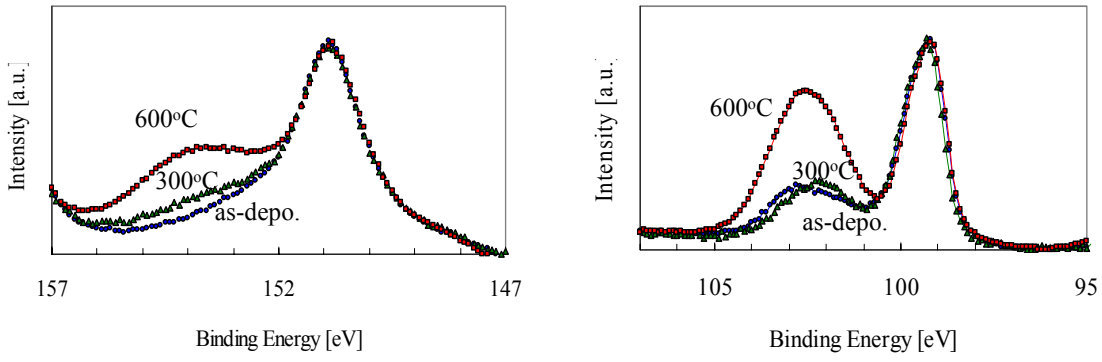


Fig. 3.24 Wide scan XPS spectra for O_2 600oC annealed 4nm thick Y_2O_3 film



(a) Y3d and Si2s (b) O1s

Fig. 3.25 narrow scan XPS spectra for Y_2O_3 films

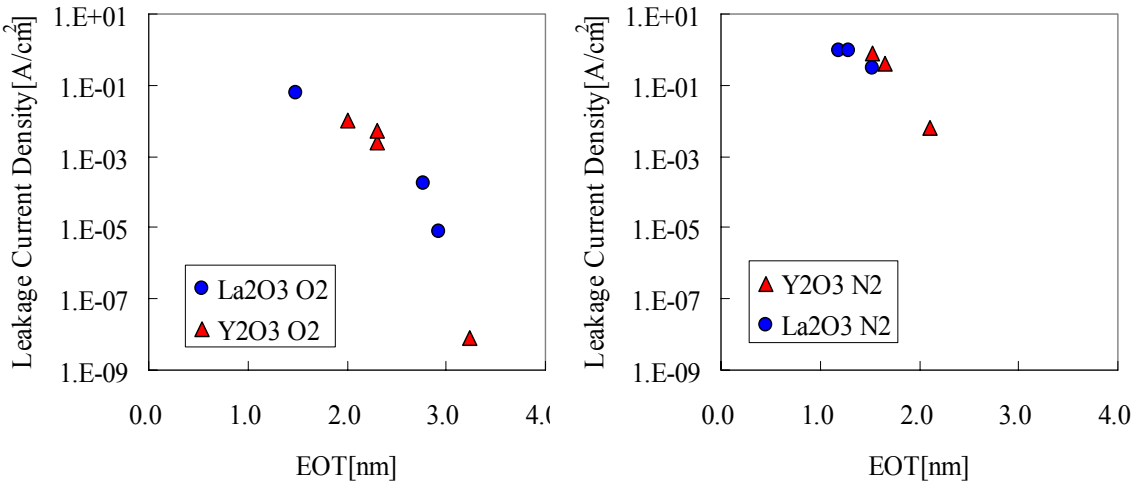


(a) Si2s (b) Si2p

Fig. 3.26 Change of spectrum for Y_2O_3 films by annealing

3.4 Comparison between La_2O_3 and Y_2O_3 films

We investigated properties that are electrical characteristic, surface roughness and composition of La_2O_3 and Y_2O_3 single layer structure. Although in both La_2O_3 and Y_2O_3 as-deposited thin films, good C-V characteristics were not observed, the excellent curve was observed by O_2 300oC annealing. In La_2O_3 films, C-V characteristic were clearly deteriorated by over 300oC annealing, however, the characteristics without frequency dependence were observed in Y_2O_3 films. The J-EOT relationships were shown in Fig. 3.27 (a) and (b). The transition of the RMS roughness values of the AFM images is shown in Fig. 3.28. The low RMS values were obtained by 300-400 annealing in Both La_2O_3 and Y_2O_3 films.



(a) O_2 annealed samples (b) N_2 annealed samples

Fig. 3.27 J vs EOT plots for annealed La_2O_3 and Y_2O_3 films

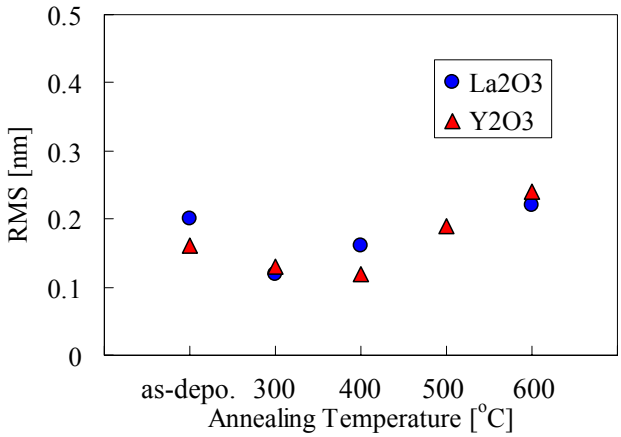


Fig. 3.28 transition of RMS roughness values for La_2O_3 and Y_2O_3 films

We found that as-deposited films also have interfacial layer. The XPS spectra indicating growth of interfacial layer was shown in Fig. 3.29. This figure shows the spectra of La_2O_3 and Y_2O_3 sample that were annealed at 600oC in O_2 ambient. It is observed that the peak of interfacial layer arising from La_2O_3 film was stronger than Y_2O_3 film. From these results, it can be suggested that interfacial layer was easily grown in La_2O_3 compared with Y_2O_3.

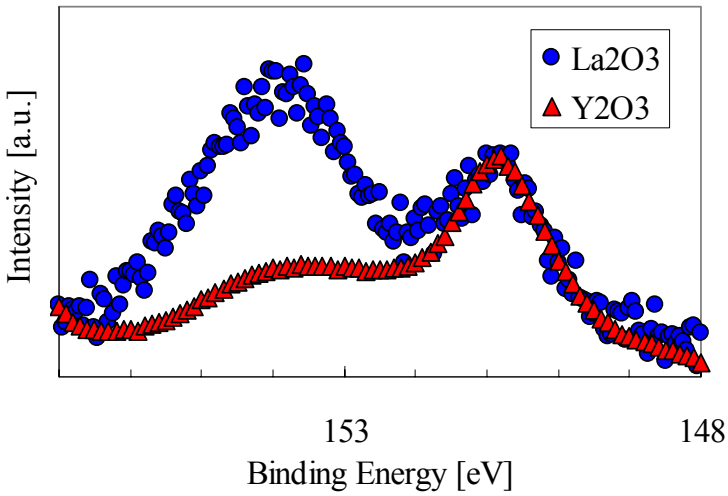


Fig. 3.29 Si2s spectra for O_2 600oC annealed La_2O_3 and Y_2O_3 film with take-off angle is 60°

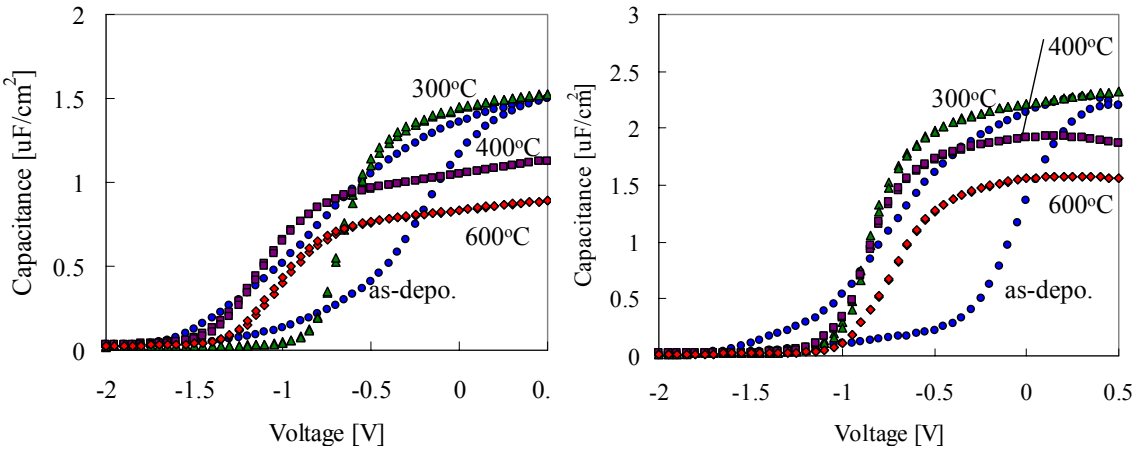
3.5 Characteristics of La_2O_3/Y_2O_3 Stack Structure

In this section, the characteristics of La_2O_3 and Y_2O_3 stack structure will be described and the measurement results of electrical characteristics (J-V, C-V), AFM, XPS and the calculated data from the results of electrical characteristics will be shown..

3.5.1 Electrical Characteristics

Fig. 3.30 (a) and (b) show the dependence of C-V characteristics for about 4nm La_2O_3/Y_2O_3 films with/without annealing. The annealing temperatures and time were 300-600^{o}C and 5 minutes, respectively and the annealing ambient was O_2 or N_2. The O_2 and N_2 annealing samples were deposited about 4 nm and 3 nm, respectively. The measurement frequency was 1MHz in these figures. In the case of O_2 annealing, strong dependence of capacitance value on annealing temperature was observed. In as-deposited film has large hysteresis, however, after annealing the hysteresis was disappeared. The highest capacitance value was observed in 300oC annealing. And the dependence which is decreasing capacitance value with increasing annealing temperature was observed considering that the interfacial layer was grown. The flat band voltages of all annealing samples were shown in Fig. 3.31. The increasing flat band voltage shift of 300^{o}C annealing sample was lowest, and higher temperatures annealing than 300^{o}C were same each other. In N_2 annealing, increasing capacitance values were observed by annealing. The capacitance value of 300oC annealing sample was highest in N_2 annealing samples, and the decreasing of capacitance value was observed in higher temperature annealing. These results indicate growth of interfacial

layer similar to O_2 annealing.



(a) O_2 annealing (b) N_2 annealing

Fig. 3.30 C-V characteristics for 4nm and 3nm thick La_2O_3/Y_2O_3 films

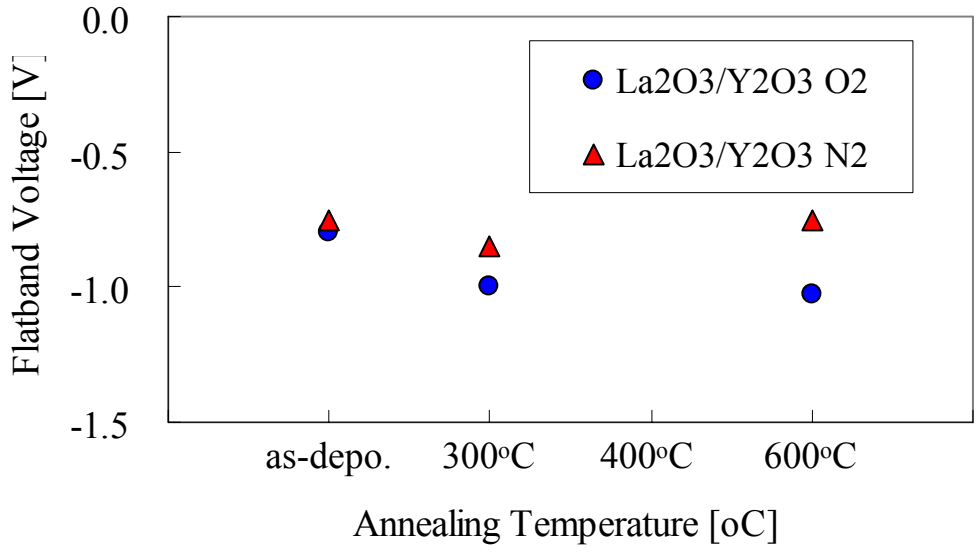


Fig. 3.31 Flat band voltage

for O_2 or N_2 annealed 4nm and 3nm thick La_2O_3/Y_2O_3 films

The dependencies of C-V characteristic of 300-600oC annealing samples on the frequency are shown in Fig. 3.32 and 3.33. The measurement frequencies were 1 MHz, 100 kHz, 10 kHz and 1 kHz. In the case of O_2 annealing, the hysteresis which was observed in as-deposited film was disappeared. In 300oC annealing sample, the excellent curves without frequency dependence and the bump at weak inversion region were obtained. In over 300oC annealing samples, strong frequency dependencies that are shift to lower voltage side with increasing annealing temperature were observed at weak inversion region. In the case of N_2 annealing, 300oC annealing sample presented the good curve compared with other samples. However, the frequency dependence which was decreasing accumulation capacitance at 1 MHz frequency was observed in all N_2 annealing samples. The dependence at a weak inversion region which was seemed in over 300oC O_2 annealing was not observed in N_2 annealing.

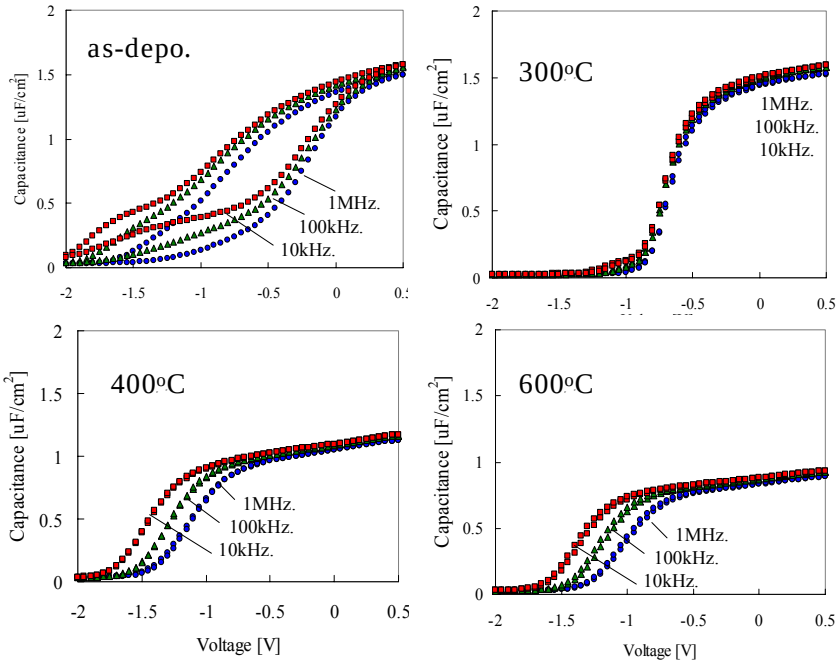


Fig. 3.32 Dependence of C-V characteristics on measurement frequency for O_2 annealed films

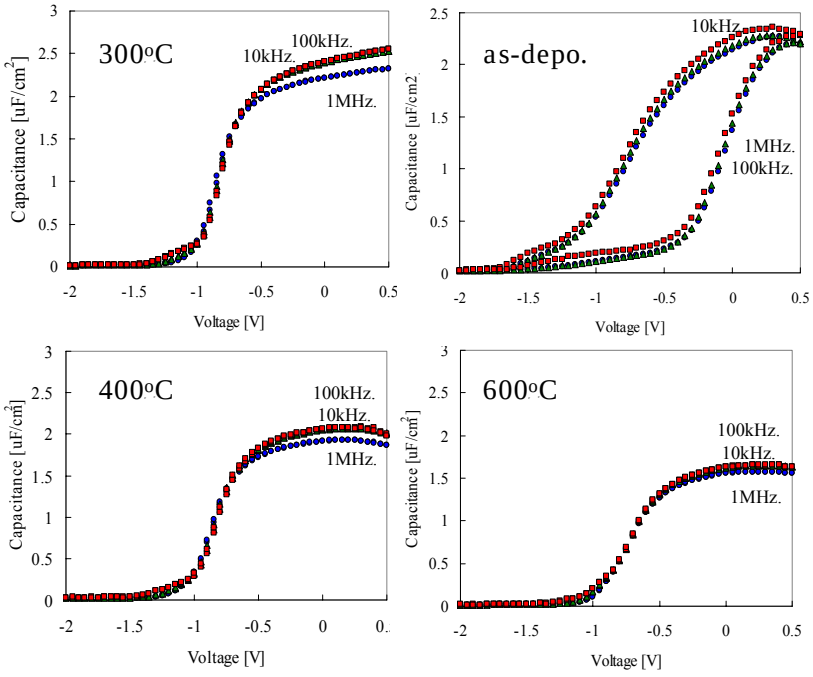
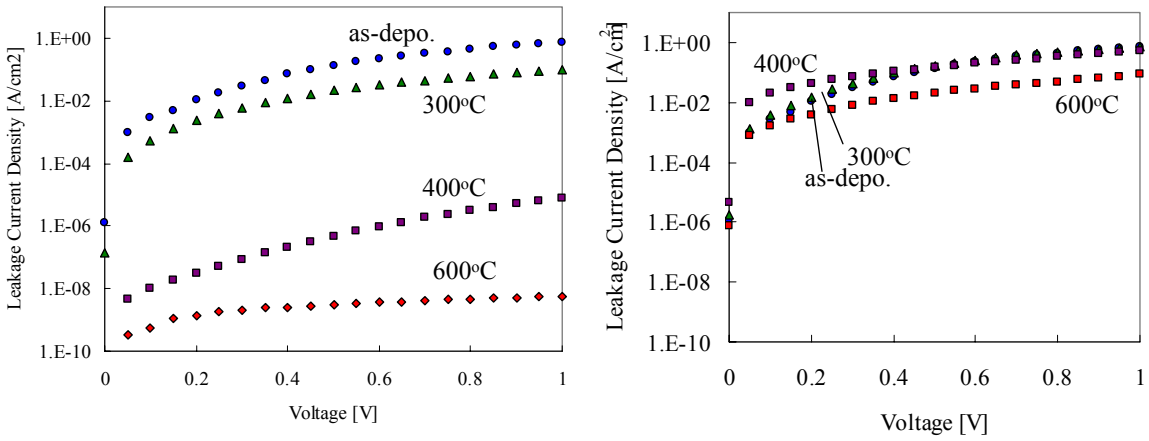


Fig. 3.33 Dependence of C-V characteristics on measurement frequency for N_2 annealed films

Fig. 3.34 (a) and (b) show the J-V characteristics for O_2 and N_2 annealing La_2O_3/Y_2O_3 samples. O_2 and N_2 annealing sample were deposited about 4nm and 3nm, respectively. In the case of O_2 annealing, the dependence which is decreasing of the leakage current with increasing temperature suggesting growth of interfacial layer was observed. In the case of N_2 annealing, the dependence was weak compared with O_2 annealing. However, the decreasing of leakage current with increasing annealing temperature was clearly observed.



(a) O_2 annealing (b) N_2 annealing

Fig. 3.34 J-V characteristics for 4nm and 3nm thick La_2O_3/Y_2O_3 films

The J-EOT plots for La_2O_3/Y_2O_3 structure samples were shown in Fig. 3.35. In case of N_2 annealing, the changes of the leakage current densities and EOT values were very small compared with O_2 annealing samples. In the case of O_2 annealing, the change of leakage current density and EOT between 300oC and 600oC annealing samples were about seven orders of magnitude and 1.8 nm.

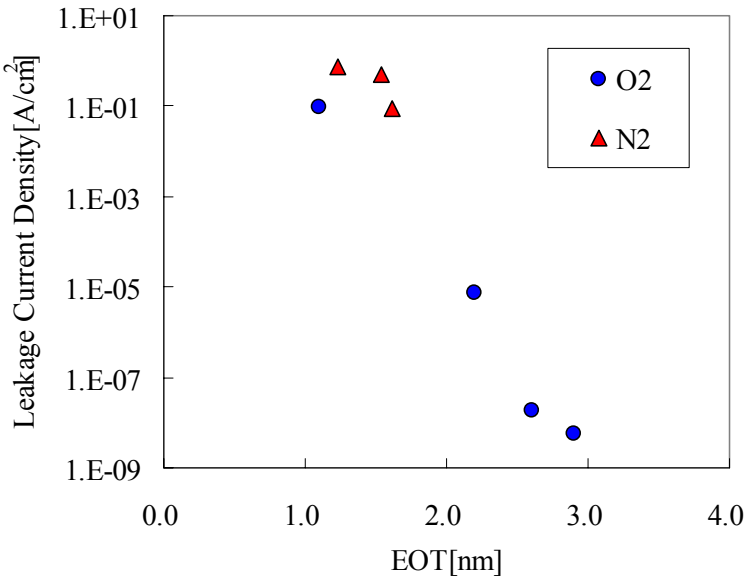
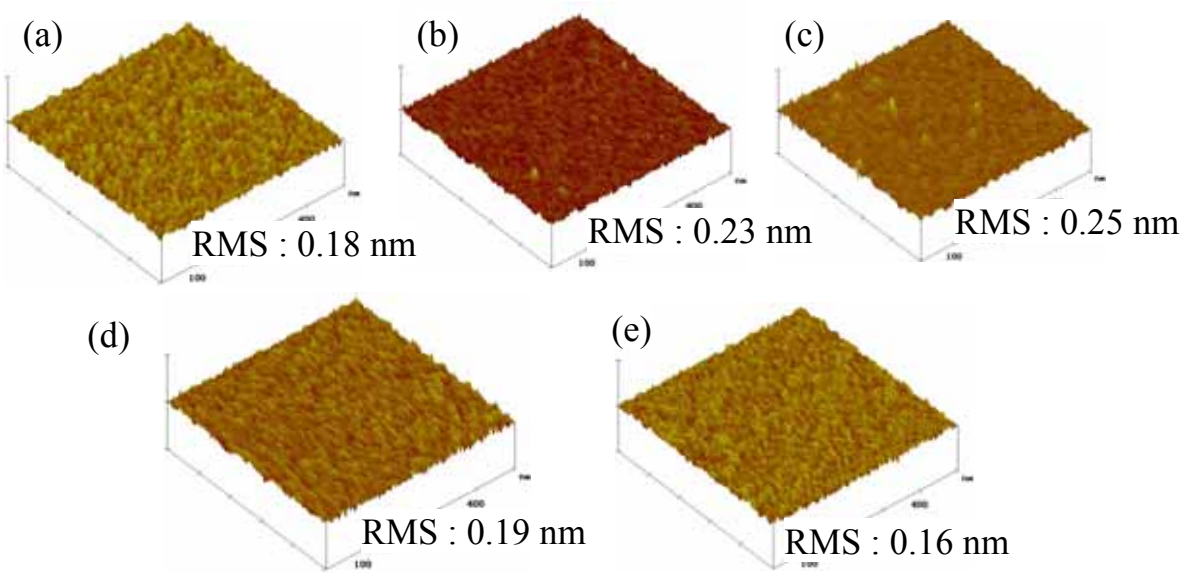


Fig. 3.35 J vs EOT plots for annealed La_2O_3/Y_2O_3 films

3.5.2 Surface roughness

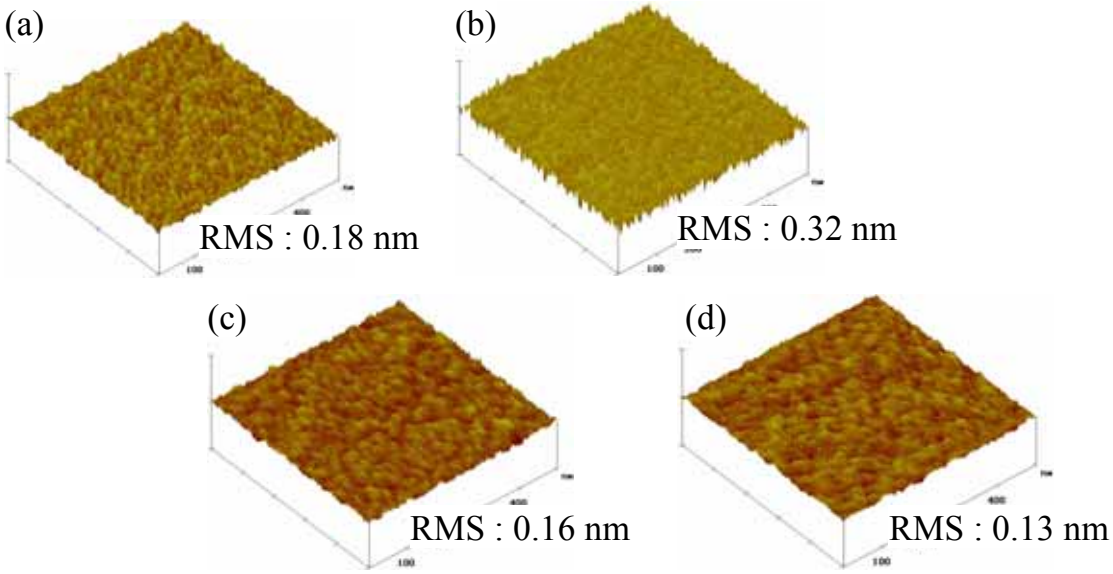
Fig. 3.36 (a) and (b) show the AFM images and RMS roughness values of the AFM images in the O_2 and N_2 annealing films, respectively. The scan size was 500 x 500 nm and the z direction was 5 nm/div. The largest value was observed at N_2 300oC annealing in all samples. In the case of O_2 annealing, the roughness of 400oC annealing sample was largest. And, it observed that the RMS values were decreased with increasing annealing temperature. However, particularly, the big change of the RMS was not observed.



(a) as-deposition (b) 300°C annealing (c) 400°C annealing

(d) 500°C annealing (e) 600°C annealing

Fig. 3.36 AFM images for O_2 annealed La_2O_3/Y_2O_3 films



(a) as-deposition (b) 300°C annealing

(c) 400°C annealing (d) 600°C annealing

Fig. 3.36 AFM images for N_2 annealed La_2O_3/Y_2O_3 films

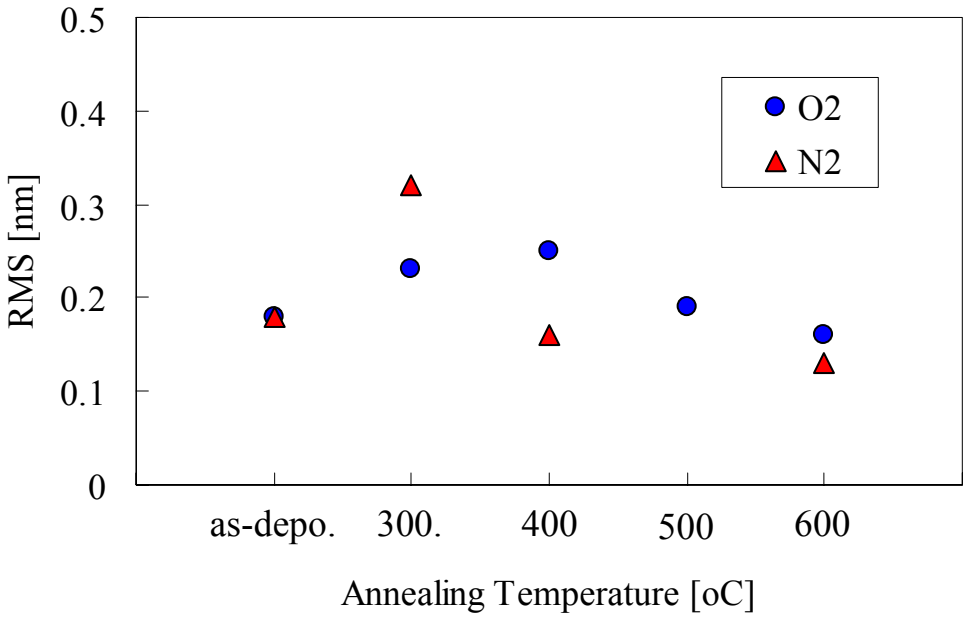


Fig. 3.37 RMS roughness values for O_2 and N_2 annealed La_2O_3/Y_2O_3 films

3.5.3 XPS Analysis

Fig. 3.38 shows the wide spectra for La_2O_3/Y_2O_3 film containing the photoelectron spectrum of O1s, Si2p, La4d, Si2s, Y3d, Y3p, O1s and La3d. The deposited oxide thicknesses of both Y_2O_3 and La_2O_3 were 1nm, therefore total physical thickness was 2nm. We measured the spectra of O1s, Si2p, Si2s, Y3d, O1s and La3d as shown in Fig. 3.39 (a) and (b) show the spectra of Y3d and Si2s that were normalized at 151 eV for Si substrate peak in Si2s. The peaks of Y3d were not shifted in 300oC annealing sample compared with as-deposited sample, however, the peak transition was observed by 600oC annealing suggesting formation of Si-rich layer such as Y-Si-O and SiO_2. Fig. 3.39 (b) presents expanded region of Si2s peak containing Si-Si bonding peak. The peaks except Si substrate peak at 151 eV were not observed in Si2s spectrum region, however, the peak expected interfacial silicate layer was appeared at higher side energy after annealing and the peak intensity was increased with increasing annealing temperature shown in Fig. 3.40. This appearance of the energy peak higher than 151 eV indicates the same phenomenon with Y3d peak that is growth of interfacial layer. The spectral region around the Si2p peaks shown in Fig. 3.41 (a) contains contributions from the La4d peaks[18] at 101.9 and 105.5 eV that overlap with the SiO_2 and Y-Si-O peak expected at 103.3 eV. No attempts were made to deconvolve the peaks. The transition of La3d peak was hardly observed shown in Fig. 3.41 (b).The O1s peak lies between the SiO_2 and $La_2O_3(Y_2O_3)$ peaks at 533.3 and 529.9 eV[18] respectively, was observed shown in Fig. 3.42 suggesting a formation of silicate layer.

Fig. 3.43 (a) and (b) show the O1s spectra arising from La_2O_3/Y_2O_3 4nm thin film. The physical thicknesses of both La_2O_3 and Y_2O_3 were 2nm. In this 4nm thickness

sample, the peak of 530 eV meaning O1s peak arising from La_2O_3 and Y_2O_3 bonding was clearly visible compared with the La_2O_3 and Y_2O_3 single layer sample and thinner stack structure sample. The FWHM of 600oC annealing sample at 532 eV peak is wider than 300oC annealing. This result suggested that Y_2O_3 and/or La_2O_3 were intermixed with Si by high temperature annealing.

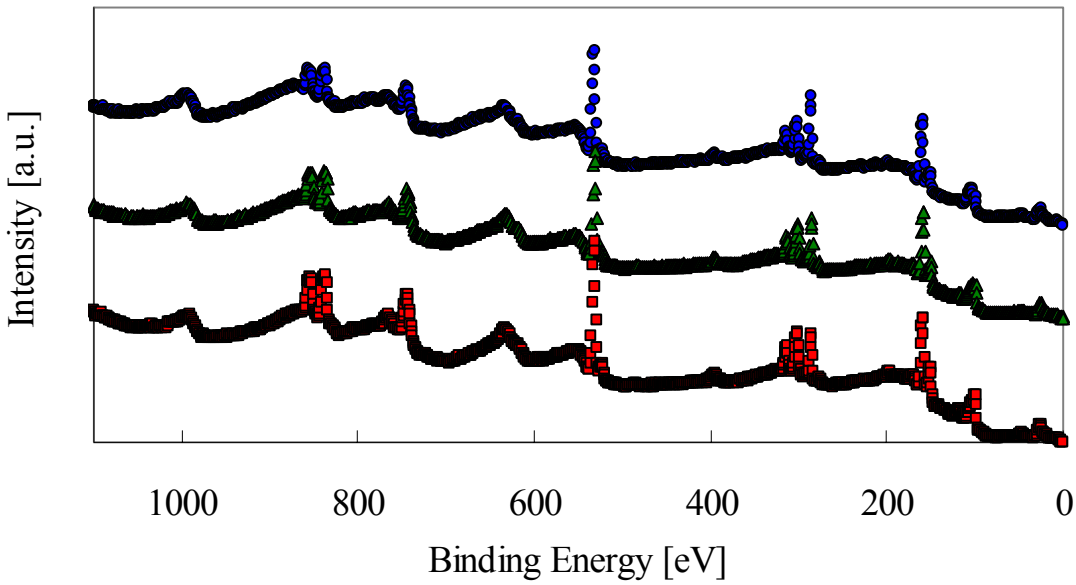
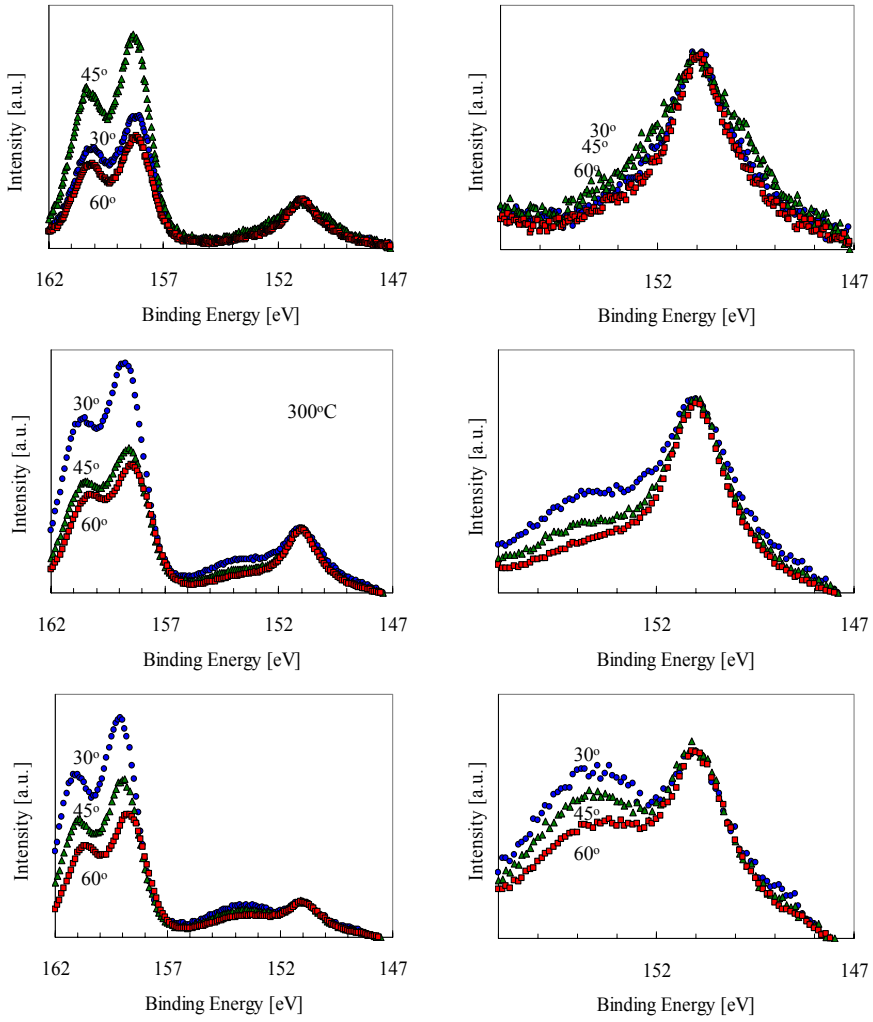


Fig. 3.38 Wide scan XPS spectra for O_2 600oC annealed 2nm thick La_2O_3/Y_2O_3 film



(a) Y3d and Si2s spectra (b) Si2s spectra

Fig. 3.39 Y3d and Si2s spectra for 2nm thick La_2O_3/Y_2O_3 films

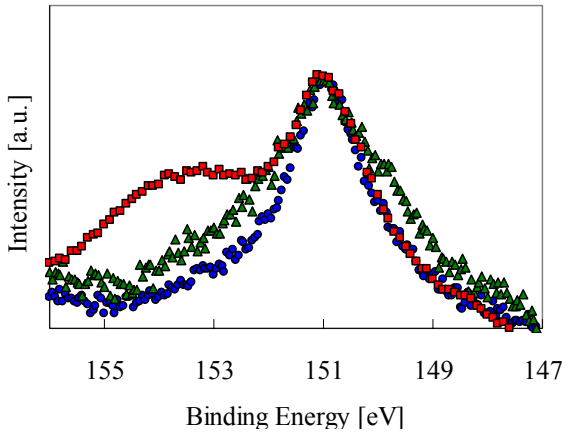
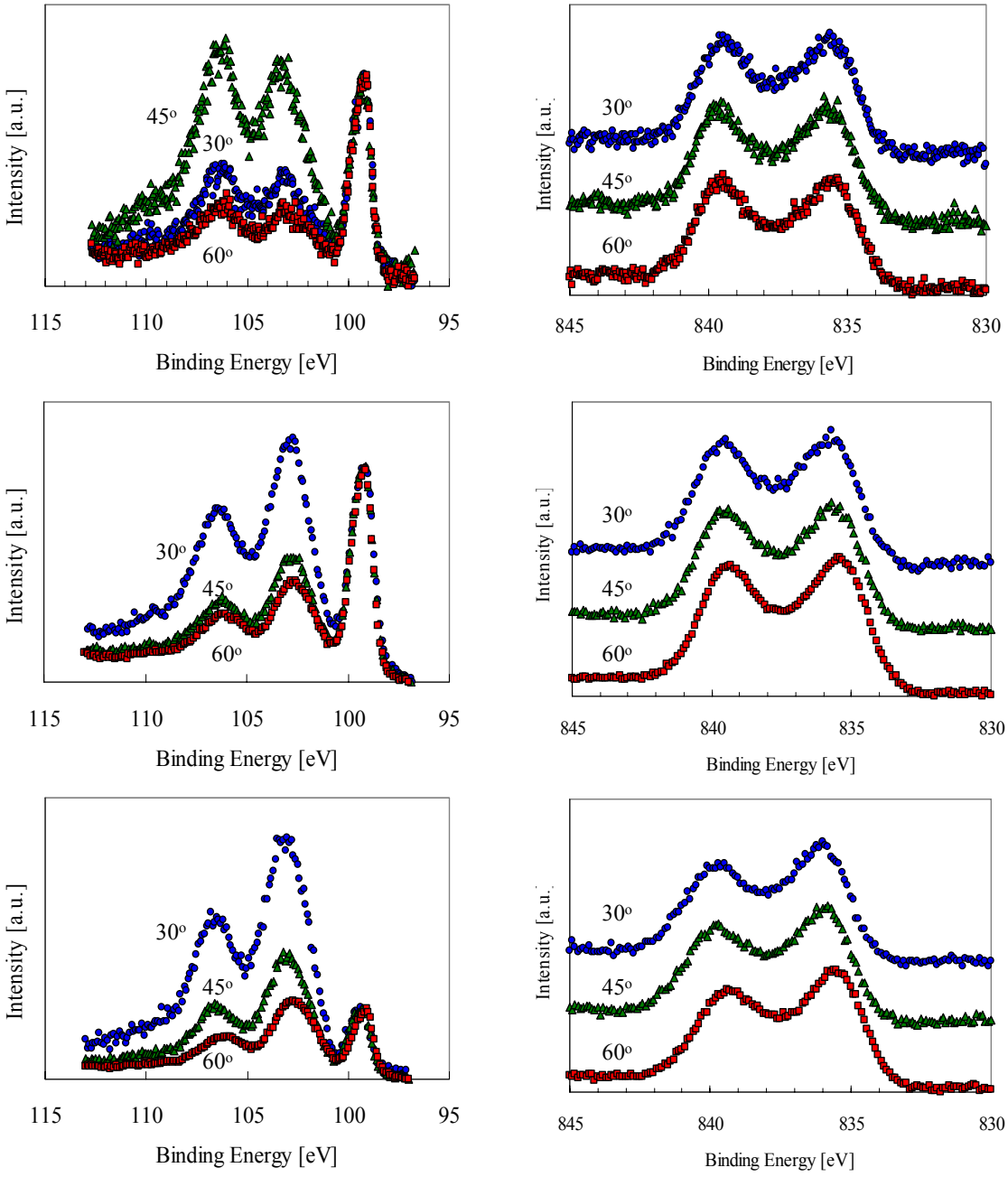


Fig. 3.40 change of Si2s spectrum for La_2O_3/Y_2O_3 by annealing



(a) Si2p spectra (b) La3d

Fig. 3.41 Si2p and La3d spectra for 2nm thick La_2O_3/Y_2O_3 film

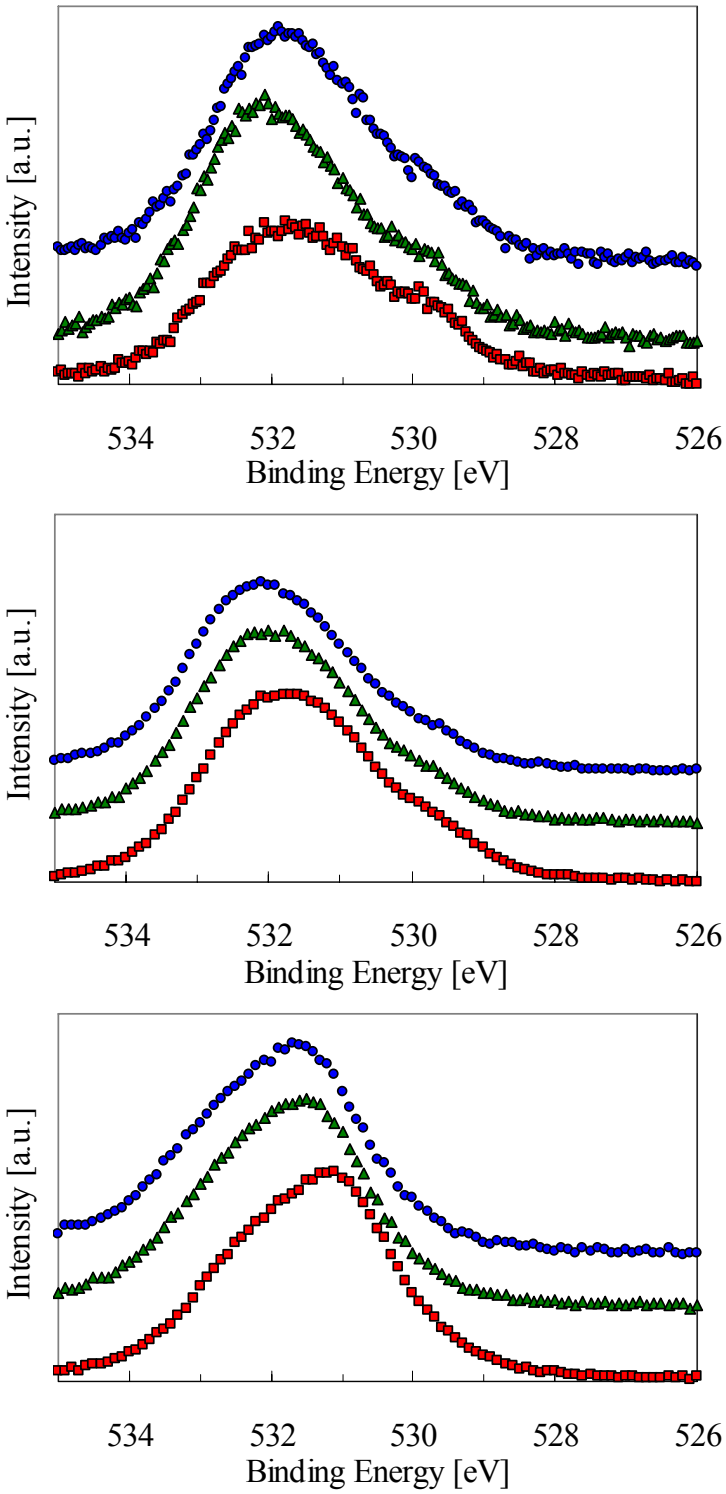


Fig. 3.42 O1s spectra for 2nm thick La_2O_3/Y_2O_3 film

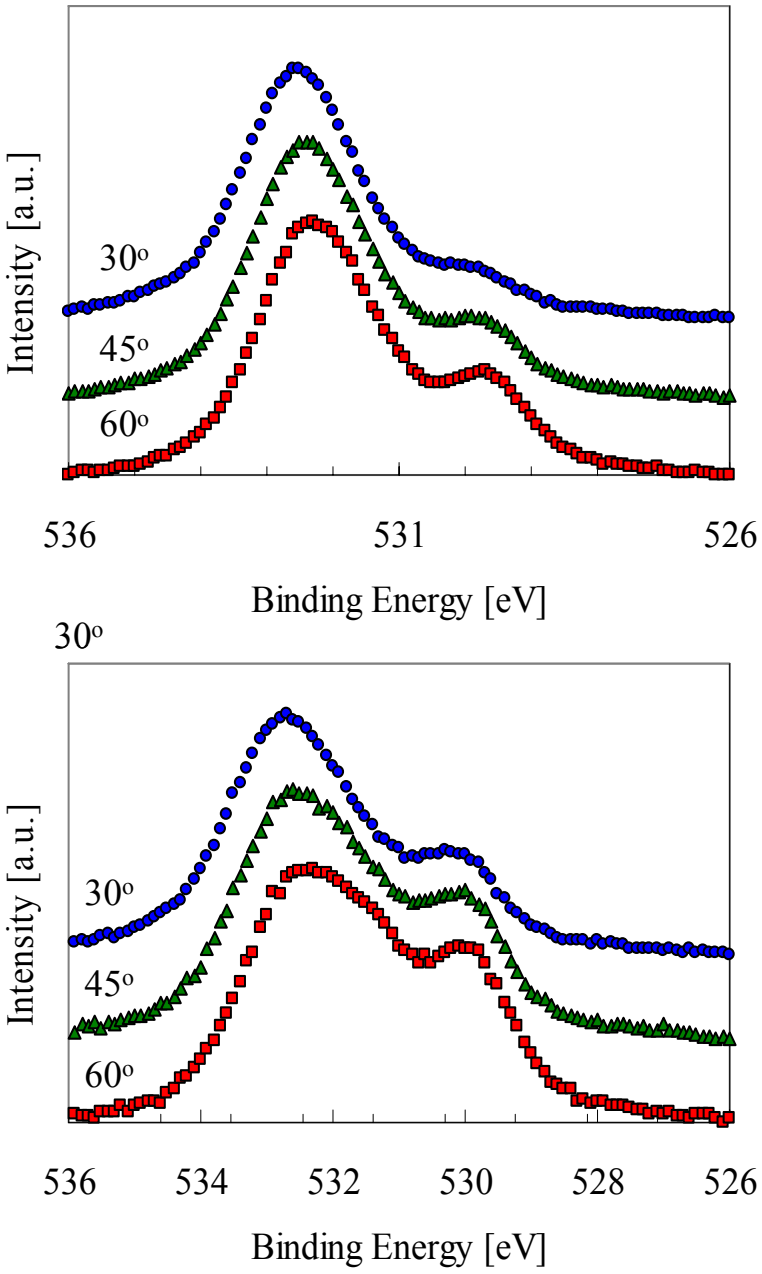
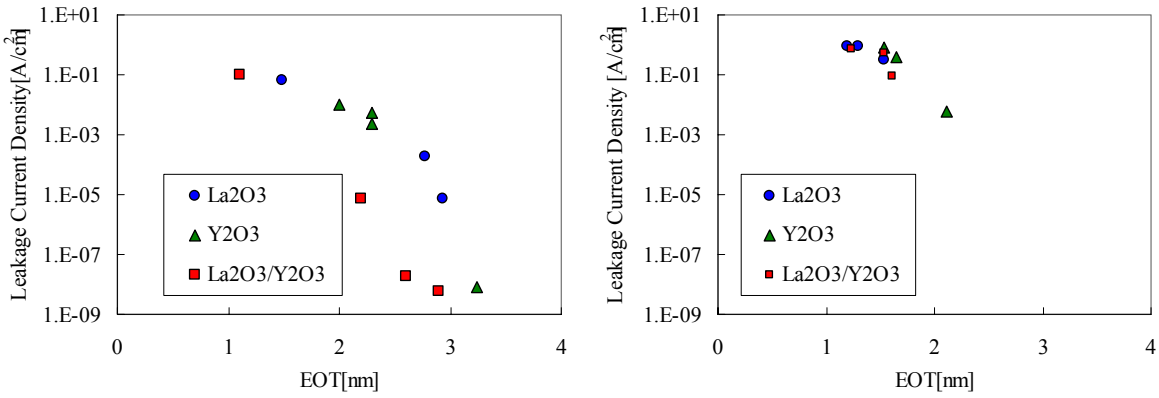


Fig. 3.43 O1s spectra for 4nm thick La_2O_3/Y_2O_3 film

3.6 Effect of Stack Structure

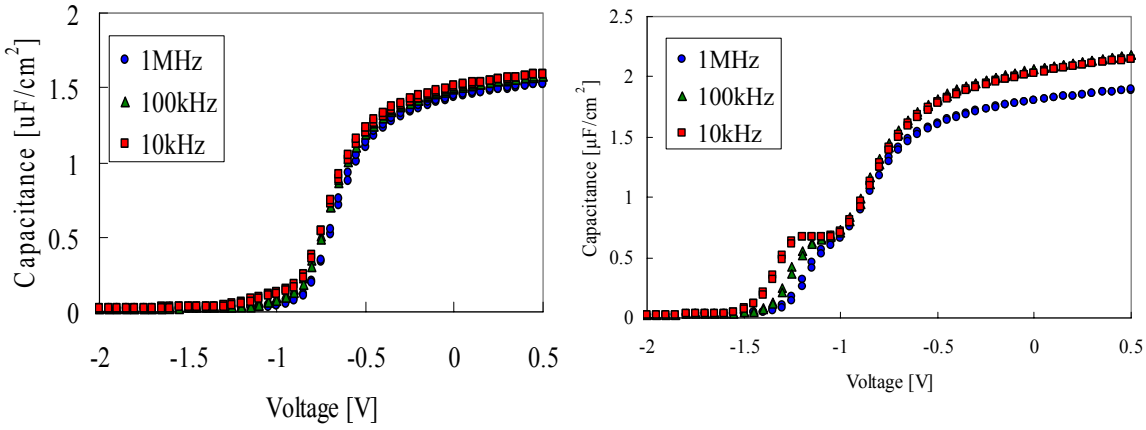
The excellent C-V curves without hysteresis and frequency dependence were observed by O_2 300oC annealed La_2O_3/Y_2O_3 structure. Fig. 3.44 (a) and (b) show the J-EOT plots for single layer samples and stacked layer samples. In the case of O_2 annealing, the evident improvement was observed by using stack structure. The accumulation capacitance values were decreased by higher temperature annealing suggesting formation of interfacial layer. These phenomena were similar in all O_2 annealing samples. In the case of N_2 annealing, the transition of plot point was smaller than O_2 annealing same with single layer samples.



(a) O_2 (b) N_2

Fig. 3.44 J vs EOT plots for O_2 and N_2 annealed La_2O_3/Y_2O_3 films

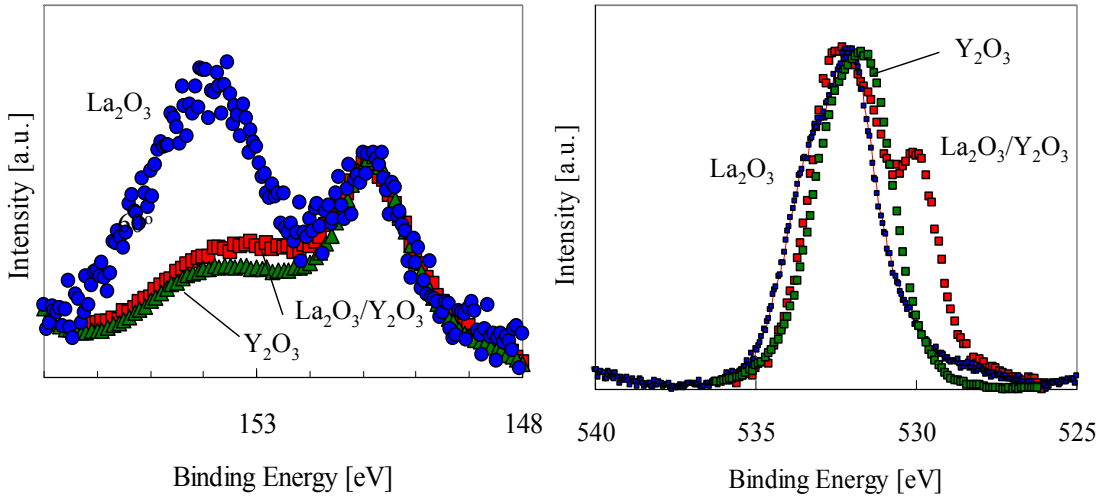
Fig. 3.45 (a) shows C-V characteristics for stacked layer sample annealed at 300°C in O_2 ambient. Fig. 3.45 (b) shows the C-V characteristics for chemical oxidized La_2O_3 single layer sample. Annealing temperature was 300°C and ambient was O_2. In stacked layer sample, excellent characteristics were observed as mentioned previous section. In using chemical oxide sample, large frequency dependence was observed compared with stack layer sample and flat-band shift was large.



(a) stacked structure (b) chemical oxide

Fig. 3.45 C-V characteristics

The Fig. 3.46 (a) and (b) show the Si2s and O1s spectra arising from O_2 annealed La_2O_3, Y_2O_3 and La_2O_3/Y_2O_3 samples, respectively. This figure represents the peaks which were measured at take-off angle of 60^o. In the case of O_2 annealing, the two peaks were observed at 151 eV and 154 eV meaning Si-Si bonding and Si-rich interfacial layer, respectively. The peak of La_2O_3 sample was stronger than peaks of Y_2O_3 and La_2O_3/Y_2O_3 suggesting strong reaction was caused between Si substrate and La_2O_3 film in La_2O_3 sample. The similar characteristic was observed between Y_2O_3 and La_2O_3/Y_2O_3. This results indicated that the same interfacial reaction was caused between Y_2O_3 and La_2O_3/Y_2O_3. Fig. 3.46 (b) shows the O1s peak. In La_2O_3/Y_2O_3 sample, strong peak at 530 eV was observed compared with other samples. This results was suggested that the silication was observed by using stack structure.



(a) Si2s spectra (b) O1s spectra

Fig. 3.46 Si2s and O1s spectra for

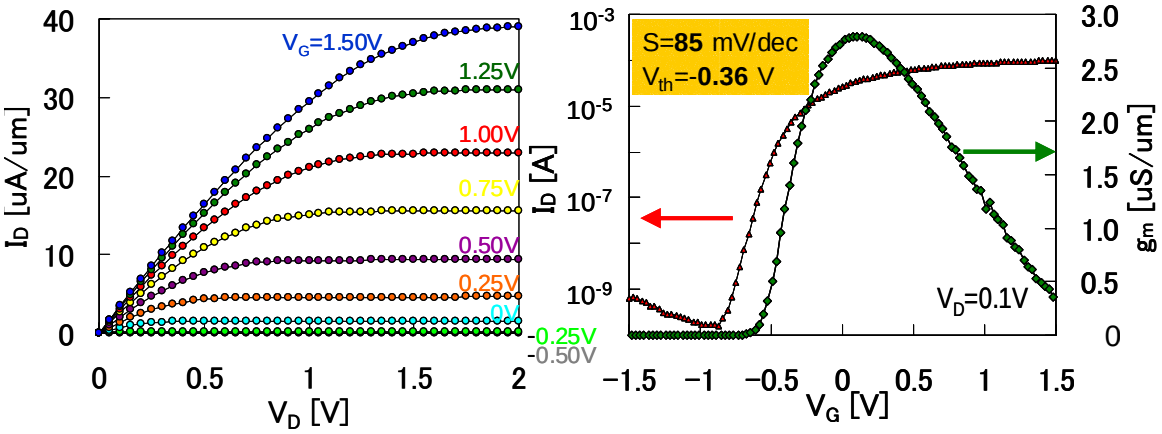
O_2 600oC annealed La_2O_3, Y_2O_3 and La_2O_3/Y_2O_3 films

Chapter 4

Confirmation of Stacked Dielectrics Transistor Operation

4.1 Characteristics of Stacked Dielectrics Transistor

In this section, we will report characteristics of stacked dielectrics transistor. Fig. 4.1 (a) and (b) show I_D-V_D and I_D-V_G characteristics of stack structure transistor respectively. The gate length and the gate width of this transistor were 10um and 27um, respectively. In I_D-V_D characteristics, the applied gate voltage were from -0.50V to 1.5V with 0.25 V step. As this figure, we found that operation of stack structure transistor. Fig. 4.1 (b) shows I_D-V_G characteristics at V_D=0.1V. S-factor and threshold voltage of this device were 85 mV/dec and -0.36 V.



(a)ID-VD (b) ID-VG

Fig. 4.1 the electrical characteristics of La_2O_3/Y_2O_3/Si nMISFET

Fig. 4.2 and 4.3 show dependences of I_D-V_D and I_D-V_G characteristics on annealing temperature respectively. Annealing conditions were without annealing and 300, 400, 600 ^oC annealing in O_2 ambient for 5 minutes. In 300^oC annealing, lowest subthreshold slope factor was obtained.

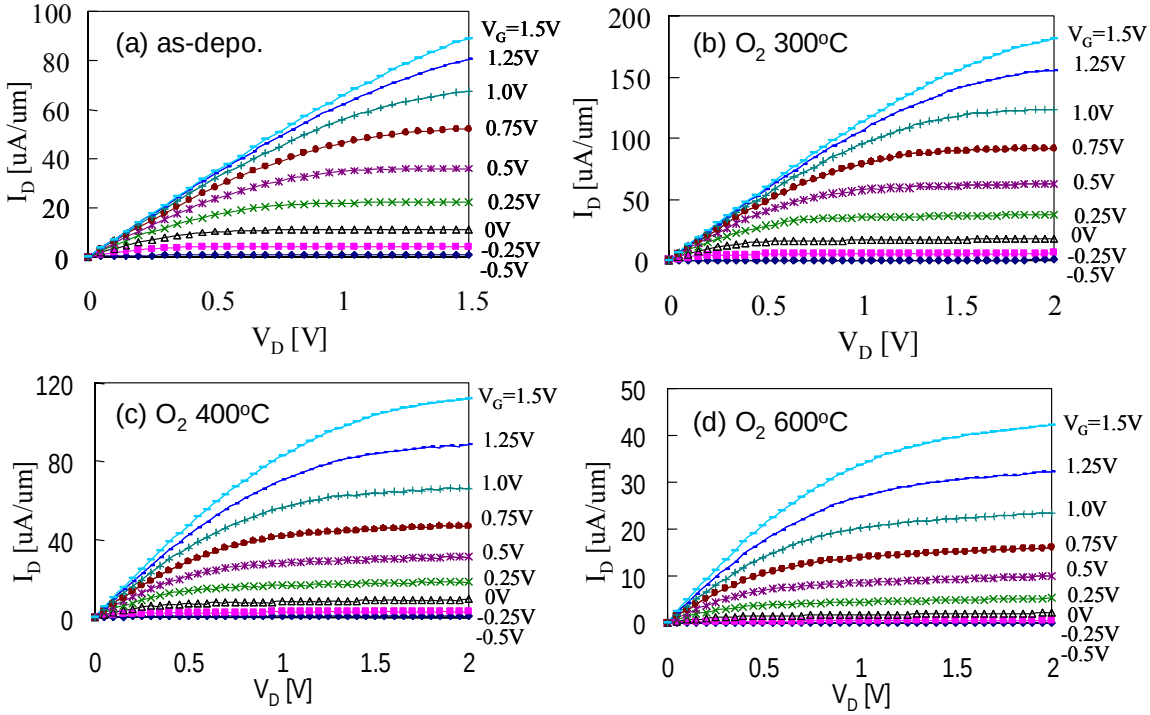


Fig. 4.2 I_D-V_D characteristics

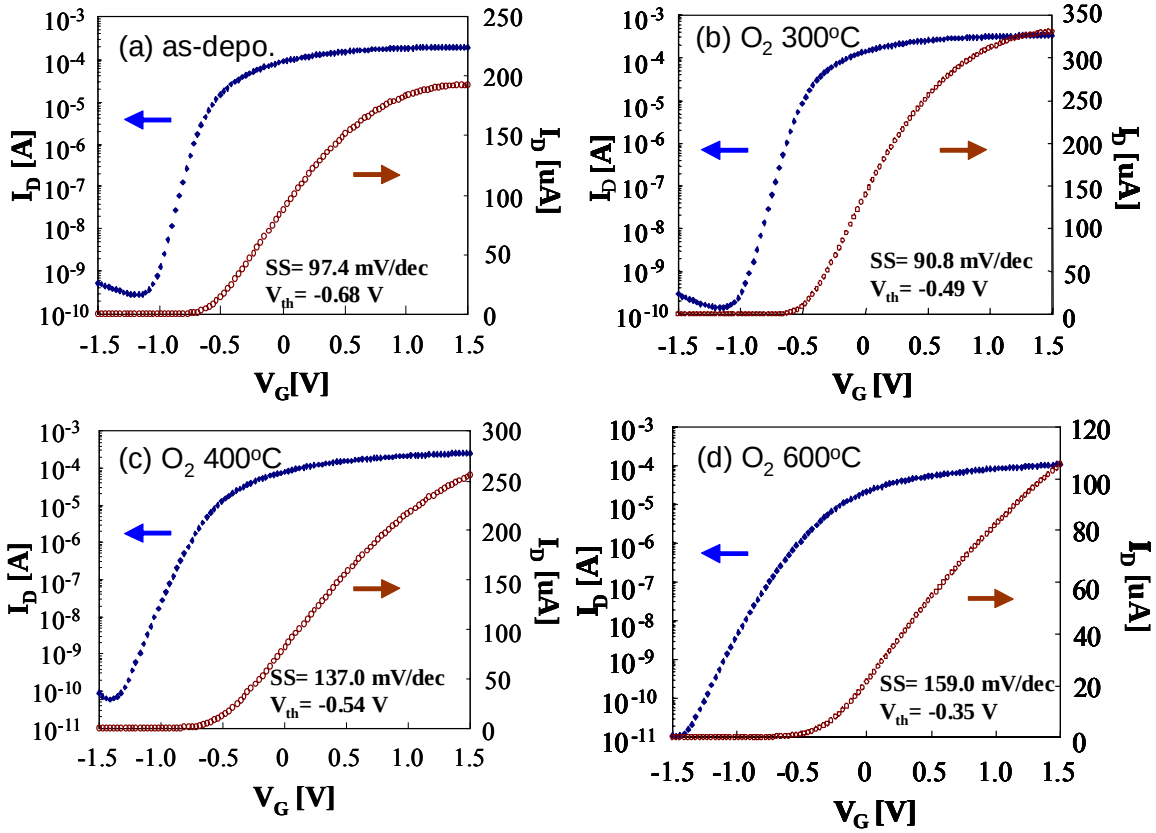


Fig. 4.3 I_D-V_G characteristics

Chapter 5

Conclusion

5.1 Results of This Study

La_2O_3/Y_2O_3 thin films deposited at 250°C by MBE. They were annealed at 300-600oC in O_2 or N_2 ambient. Excellent C-V characteristics without hysteresis and frequency dependence were obtained with suppression of the accumulation capacitance decrease by using stacked dielectrics structure. It is found that best annealing condition is 300oC annealing in both O_2 and N_2 ambient. Comparison with the La_2O_3 and Y_2O_3 single layer structure, the electrical characteristics were improved by stack structure. It was found that interfacial layer was more grown by high temperature annealing and in as-deposited films; interfacial layer was already grown. In 600oC annealing case, it is considered that both silicate and SiO_2 layer were grown. In La_2O_3 films, C-V characteristic were clearly deteriorated by over 300oC annealing, however, the C-V characteristics without frequency dependence were obtained in Y_2O_3 films. As the results of XPS, It was suggested that Y_2O_3 film is a smaller reaction with Si substrate which is growth of interfacial layer than La_2O_3 film. In stacked structure as Y_2O_3 was buffer layer, similar XPS results were observed with Y_2O_3 single layer films. These results suggested that growth of interfacial layer was suppressed by stack structure. In La_2O_3/Y_2O_3 structure, the cause of leakage current decreasing was thought by the suppression of interfacial layer growth.

5.2 Future Issues

In this study, we obtained excellent results which are suppression of leakage current for gate dielectric thin films and investigated effect of anneal condition on films by XPS. However, we still have some unresolved problems. One of the problems is flat band voltage shift. The cause of this problem for rare earth oxides is still not clarified completely. It is necessary to study about the relation between flatband voltage shift and the distribution of the oxide charges. For the purpose of clarifying the mechanism of oxide charge generation during the fabrication process, more detail analyses should be carried out from both the sides of electrical characteristics and physical or chemical measurements. And, for the application to the gate insulator of transistor, the characteristics of single layer and stacked layers MOSFET should be more investigated.

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Yokohama,

March 2005

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