Low-Frequency (1/*f*) Noise of NMISFET with La_2O_3 High-k Gate Dielectrics and Analysis of Electrical Properties of Ultra-Shallow p^+/n Junctions Formed by Plasma Doping Method

- A THESIS -

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To my father, mother, brothers and sister.

Abstract

Electronics markets are driving Large Scale Integration (LSI) technology to have high performance and high functionality or even low stand-by power. Si-based microelectronic devices have accomplished these requirements by miniaturization of the active devices called Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). This rapid shrinking of the feature size of MOSFET devices has forced the gate dielectric thickness and Source-Drain Extension (SDE), which is the main subjects in this study, to decrease rapidly to a critical point. In gate dielectric, the search of a new material for replacement of ultra-thin silicon dioxide has been addressed due very high leakage current caused by direct tunneling. Key guidelines for selecting an alternative gate dielectric material are dielectric constant, band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability. Lanthanum oxide (La_2O_3) is considered to be promising gate dielectric in the next 10 years. It has dielectric constant of 27, band gap of 5.6 eV, band alignment with silicon of more than 2 eV, good thermal stability in contact with silicon, and in a form of amorphous below temperature 1800^{o}C. However, investigation on formation of La_2O_3 thin films over silicon with good interface quality, good compatibility with current processing, and good reliability must be carried out. In SDE formations, critical requirements on Ultra-Shallow Junctions (USJ) with low sheet resistance are difficult to obtain by conventional ion implantation, which is limited to high energy doping, and conventional activation annealing, which can cause deeper impurity diffusion. Plasma doping method shows the most promising method for USJ in respect with low energy

doping. New annealing methods like Flash Lamp Annealing (FLA) and Laser Annealing (LA) should be introduced to suppress impurity diffusion. Combination of plasma doping and these new instantaneous annealing may leave defects or interstitial impurity atoms, which may act as generation-recombination centers. In this study, we investigate two major subjects. The first, we evaluate the low-frequency noise of La_2O_3 gate insulated NMISFETs, which is related to the interface quality. And the second, we examine the leakage current of ultra-shallow p^+/n junctions caused by traps leaving in space charge regions (SCR). In the end, based on the above investigations, we discuss an expected formation processes to form high device quality.

Chapter 1. General Introduction

So far, we have been taking the benefits and conveniences of many electronic appliances to our life. The needs on automation and portability have forced these technological devices to have high-performance, high functionality and even low power consumption. In the last three decades, the progresses of electronics advances have been accomplished with the growth of Si-based microelectronic devices in Very-Large-Scale Integration (VLSI) technology. The rapid growth in VLSI technology has been enabled with miniaturization of the active devices, called Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), to even smaller sizes. This miniaturization was technically termed by "scaling rule." An obvious benefits from device miniaturization – higher packing densities, higher circuit speeds, more functions, and lower power consumptions – have been a prime key in the evolution of today's computer and communication system that offer superior performance, reduced cost, and reduced physical size, in comparison with their predecessors.

1.1 Perspective on CMOS Technology

The scaling rule is based on reducing the device dimension in both lateral (i.e. lithographic feature size) and vertical (e.g. gate dielectrics, junction depth, etc.). The consensus scenario of how the device parameters are scaled for the next technology is provided in the International Technology Roadmap for Semiconductor [1]. A simple

description of miniaturization with scaling factor of S is shown in Fig. 1.1 and Table 1.1. To gain S times of the device performance, the physical device dimensions are reduced by S times, while the electrical parameters are increased by S times.

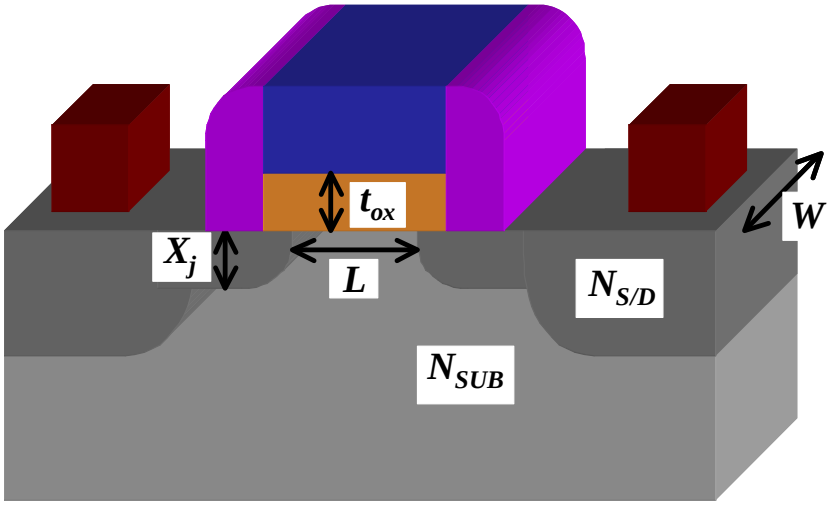

Fig. 1.1 An overview on scaling of MOSFET device structure.

Table 1-1 Miniaturization with scaling factor of S.

Parameter	Initial	Scaled
channel length	L	L/S
channel width	W	W/S
total device area	A	A/S^2
gate oxide thickness	t_{ox}	t_{ox}/S
gate capacitance	C_{ox}	$C_{ox} \times S$
junction depth	X_j	X_j/S
power supply voltage	V_{dd}	V_{dd}/S
threshold voltage	V_{th}	V_{th}/S
substrate doping concentration	N_{SUB}	$N_{SUB} \times S$
S/D doping concentration	$N_{S/D}$	$N_{S/D} \times S$

1.1.1 Requirements in Gate Dielectrics

The silicon gate oxide with physical thickness of about 1.5 nm has been used for the most recent advanced LSI products. To improve the channel drive current and transconductance, physical thickness of silicon gate oxide must be scaled down to less than 1.5 nm. Nitrided-SiO_2 materials are extensively used for near-1-nm gate oxides technology.

Currently, a technical term equivalent oxide thickness (EOT) is used for non-SiO_2 gate dielectrics. EOT is defined as the physical thickness of SiO_2 to have an electrical inversion charge value equivalent with the respective gate dielectric if SiO_2 gate oxide is used. Fig. 1.2 shows the projection of the gate oxide technology defined in International Roadmap for Semiconductors (ITRS) 2004. The lower level corresponds to High Performance (HP) Main Processing Unit (MPU), the middle is for Low Operating Power (LOP), and the upper is for Low Standby Power (LSTP). Requirements showed in Fig. 1.2 indicate an EOT progressing to less than 1 nm.

The gate dielectric has emerged to be one of the most difficult challenges for the future device scaling due to high direct tunneling currents. Fig. 1.3 shows the leakage current density of the-state-of-the-art silicon gate oxide as a function of effective physical thickness. In HP MPU applications that have high allowable leakage currents, nitrided-SiO_2 might be scaled as thin as 1 nm. However, leakage current, thickness control and reliability may limit the use of nitrided-SiO_2 bellow 1 nm. Significantly, high-κ gate materials are needed for sub-1-nm gate oxide technology and for LOP and LSTP applications that have strictly low allowable leakage currents.

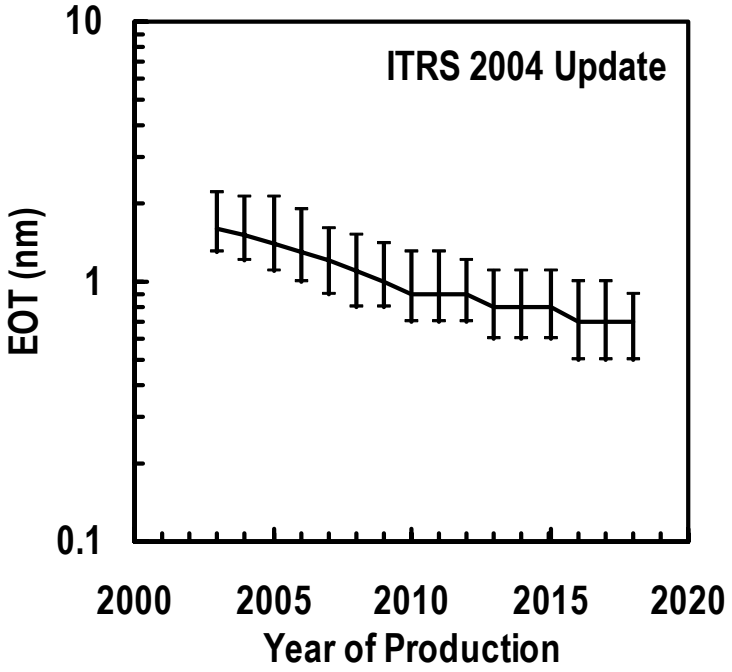

Fig. 1.2 Trend in gate dielectrics: Low EOT values are needed to improve the drive current (and transconductance) of MOSFET.

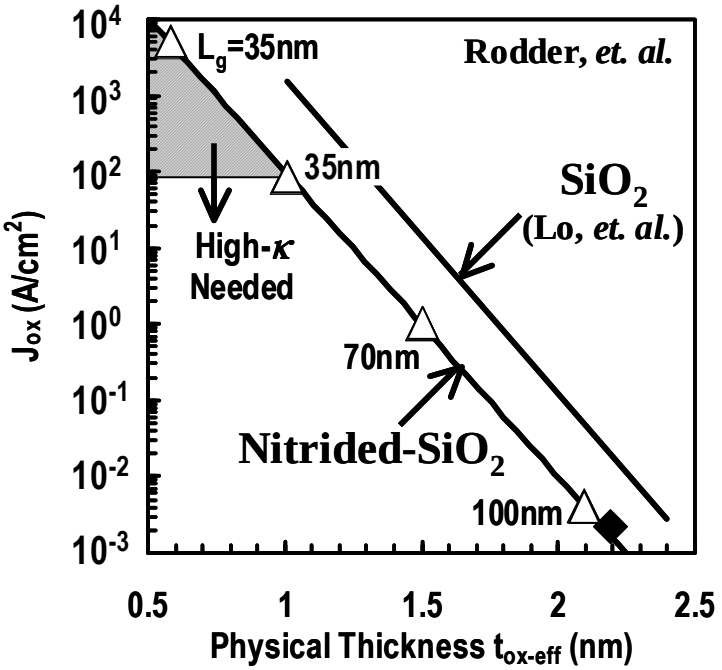

Fig. 1.3 The leakage current density of the-state-of-the-art silicon gate oxide as a function of effective physical thickness. For sub-1-nm gate oxide technology, high-κ gate materials are needed due to high leakage currents.

1.1.2 High-κ Gate Materials

There are many materials that are considered to be potential as replacements for SiO_2 as the gate oxide technology are scaled beyond 1 nm. The key guidelines for selecting an alternative gate dielectric material are dielectric constant, band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability.

In silicon semiconductor processes, thermal processing as high as 1000 K is very common to reduce defect formations. Thermal stability in contact with silicon up to 1000 K is required for high-κ gate dielectric materials. The possible candidate of several metal oxides system for the use of gate dielectric materials is shown in white spaces of Fig 1.4.

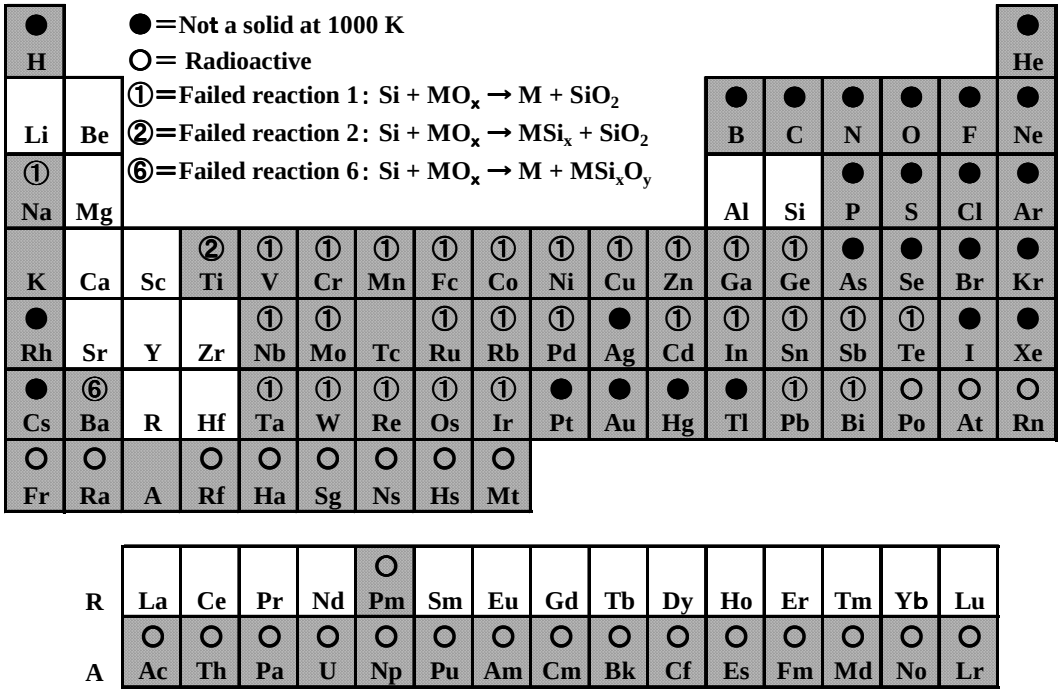

Fig. 1.4 Candidate of metal oxides that are thermodynamically considered to have good stability in contact with silicon up to 1000 K.

Thermal stability in contact with silicon is shown by the standard Gibbs free energy of the system (ΔG^o) of the possible reactions between the metal oxides and silicon that is usually metal, silicide, or silicate formations. Lowering of Gibbs free energy of the system ($\Delta G^o < 0$) means the formation reactions are in straight forward. The following is the available data of ΔG^o at 1000K on metal and silicide formation for lanthanum oxide (La_2O_3) material.

$$Si + LaO_x \rightarrow La + SiO_2 \qquad \Delta G^o_{1000K} = +98.470 \text{ kcal/mol}$$
$$Si + LaO_x \rightarrow LaSi_z + SiO_2 \qquad \Delta G^o_{1000K} = +66.372 \text{ kcal/mol}$$

As ΔG^o of metal and silicide formation for La_2O_3 material is remained positive, it is considered that La_2O_3 does not react with silicon to form metal or silicide in silicon interface.

To perform a low EOT, high-κ gate dielectrics materials must have high enough dielectric constant. However, material with very high dielectric constant tends to have narrower band gap that allows higher Schottky conduction currents and tunneling currents. Fig. 1.5 shows band gap energy of several metal oxide and silicate materials as a function of dielectric constants. La_2O_3 gives high dielectric constant of 25 and wide band gap of 5.6 eV that is suitable for the use of gate dielectrics

To inhibit a low leakage current due to Schottky emission conduction mechanism, the high-κ gate dielectric materials must have wide band gap and high barrier of more than 1 eV for both electrons and holes. Fig. 1.6 Predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy. La_2O_3 has a good symmetrical band barrier of more than 2 eV for both electrons and holes that is compatible for CMOS devices.

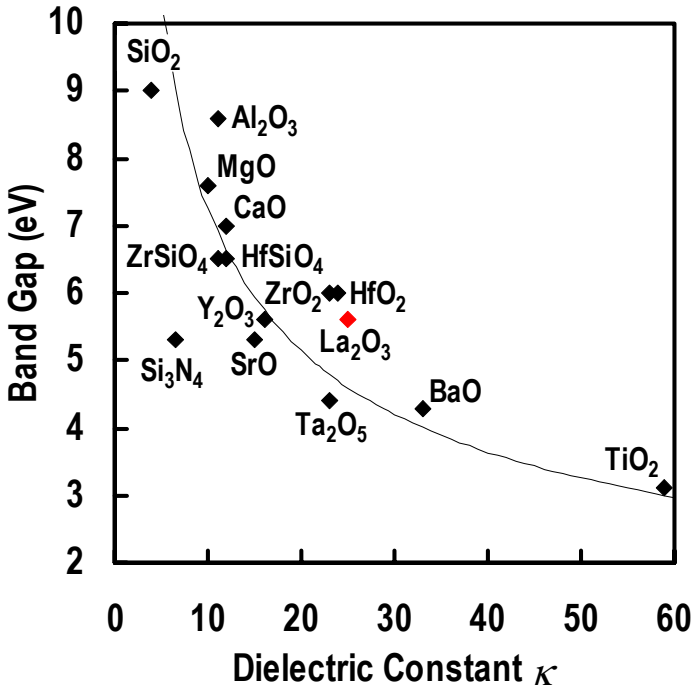

Fig. 1.5 Band gap energy of several metal oxide and silicate materials as a function of dielectric constant. Material with very high dielectric constant has narrower band gap that is not suitable for the use of gate dielectrics.

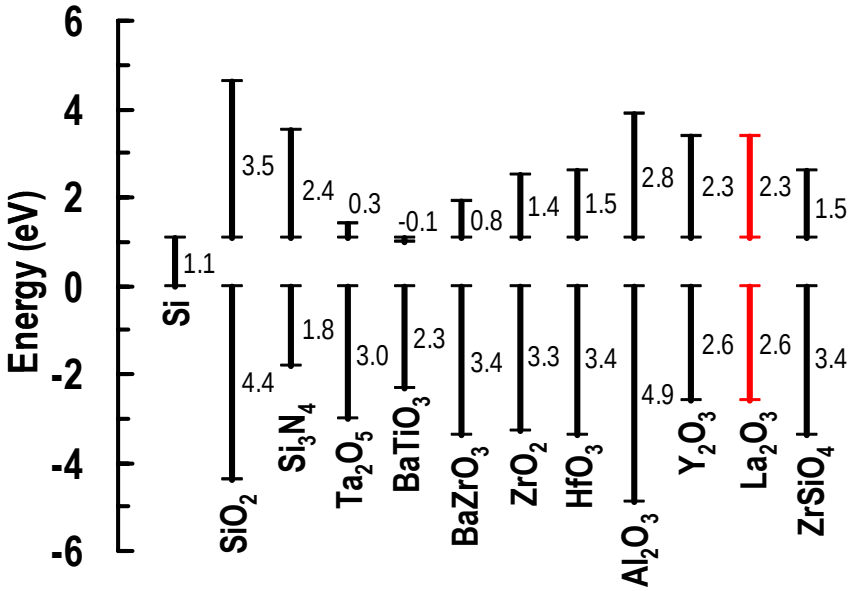

Fig. 1.6 Predicted band offset of several binary and ternary metal oxides in alignment with silicon band energy.

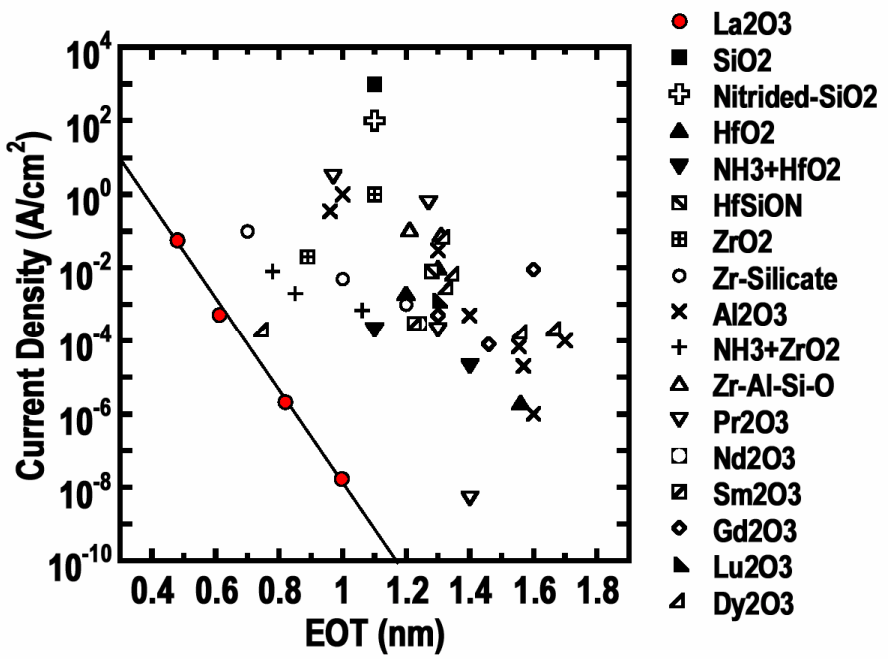

Fig. 1.7 Reported leakage current density of various high-κ gate materials as a function of EOT. La_2O_3 shows superiority over other materials due to very low leakage current.

Previously, excellent results on several high-κ gate dielectrics materials have been reported. Fig. 1.7 shows reported leakage current density of various high-κ gate materials as a function of EOT. From Fig. 1.7, the superiority of La_2O_3 is obvious, low EOT with low leakage current can be achieved with La_2O_3.

Finally, La_2O_3 is considered to be the most promising gate dielectric material for the next generation gate dielectric technology. La_2O_3 material shows good physical properties, *e.g.* high dielectric constant of 27, wide band gap of 5.6 eV, symmetrical band offset for electrons and holes of more than 2 eV, and good thermal stability in contact with silicon. In this thesis, the electrical properties of MISFET with La_2O_3 gate dielectrics will be evaluated.

1.1.3 Requirements for High Frequency and Analog/Mixed-Signal Applications

Recently, the needs of communication and information technology are increased with the development of a highly-information-oriented society. Various communication systems are coming out in various areas, services, and bandwidths so called ubiquitous electronics. These have been realized by the progress of wireless communication systems. A wide range of frequency bandwidths from 0.8-10 GHz are attracting our attention for the use of Global Standard for Mobile (GSM), Wide Code Division Multiple Access (WCDMA), Global Positioning System (GPS), 802.11 protocol for Local Area Network (LAN), etc. Fig. 1.8 shows application spectra of several semiconductor materials for High Frequency (HF) and Analog/Mixed-Signal (AMS) Technologies. Gigahertz applications of silicon devices will be the driving forced of wireless communication systems due to cost, power consumption, functionality, and available frequency bands.

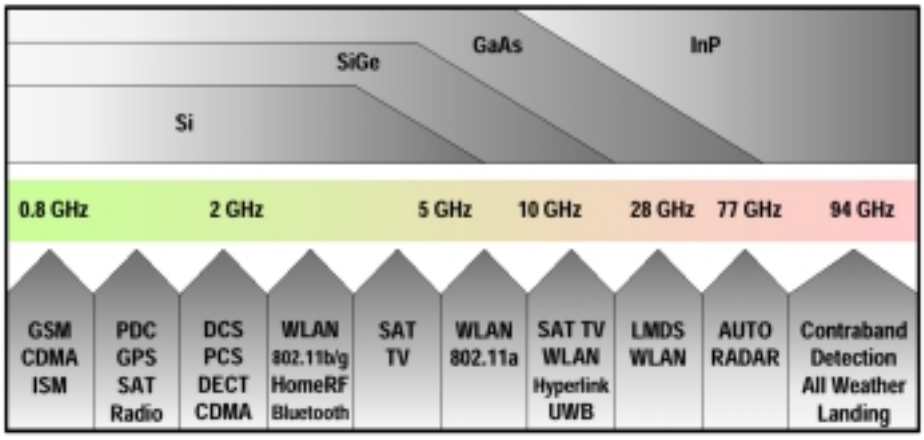

Fig. 1.8 Application spectra of several semiconductor materials for High Frequency and Analog/Mixed-Signal Technologies.

The bases of wireless communication devices are realized by semiconductor integrated circuits. Mostly, current wireless communication devices are contents of Radio Frequency/Intermediate Frequency (RF/IF) and Base Band (BB) sections as shown in Fig 1.9. The functional of receiver circuits in RF/IF block are to extract the signal components of the high frequency by demodulating them to digital signals. While the transmitter are to modulate the digital signals with frequency components and amplifying them in order to be ready to transmit to the outside medium. Devices used in HF and AMS require having sufficiently low Noise Figure (NF).

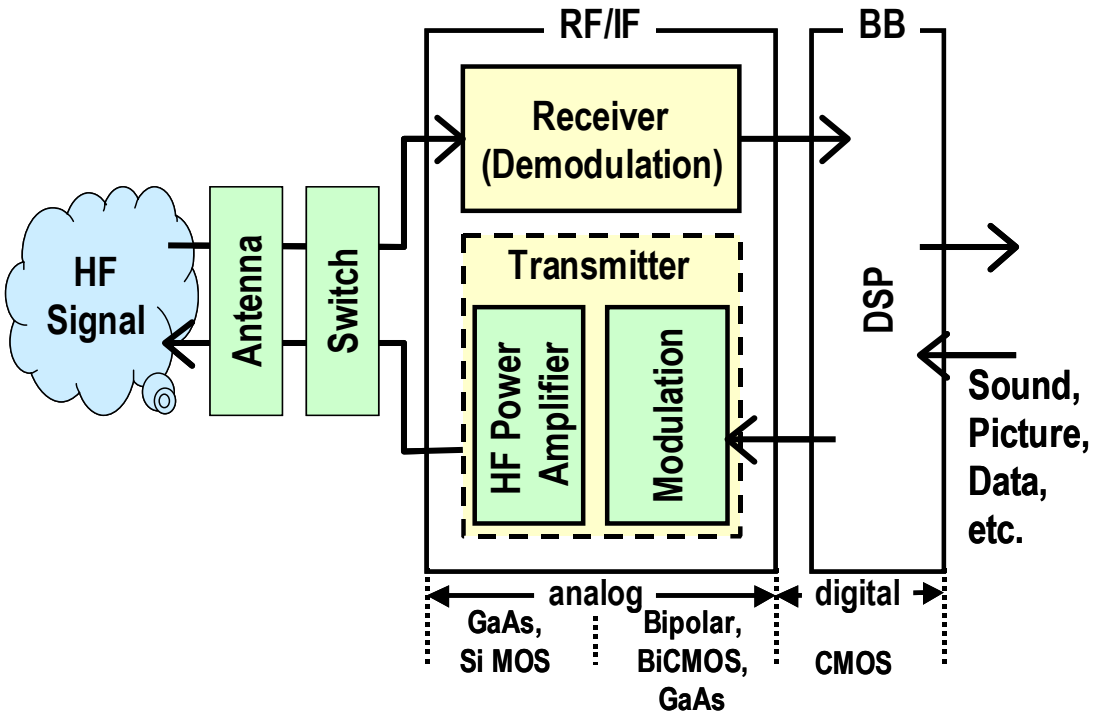

Fig. 1.9 Typical schematic block for wireless communication devices.

Low Frequency Noise (LFN) which is dominated by 1/*f* noise is becoming a major concern in analog applications, because excessive of this kind of noise can lead to a serious limitation of their performances and functionalities. In high frequency circuit applications, 1/*f* noise spectrum is up-converted to give rise to phase noise in oscillators, mixers or modulators. Fig. 1.10 shows the requirements of NMOS analog speed devices as defined in ITRS 2004 update version. To preserve a high signal-to-noise ratio, device with 1/*f* noise as low as $WLS_{vg}/EOT^2 < 10^{-4}$ V^2/Hz is required.

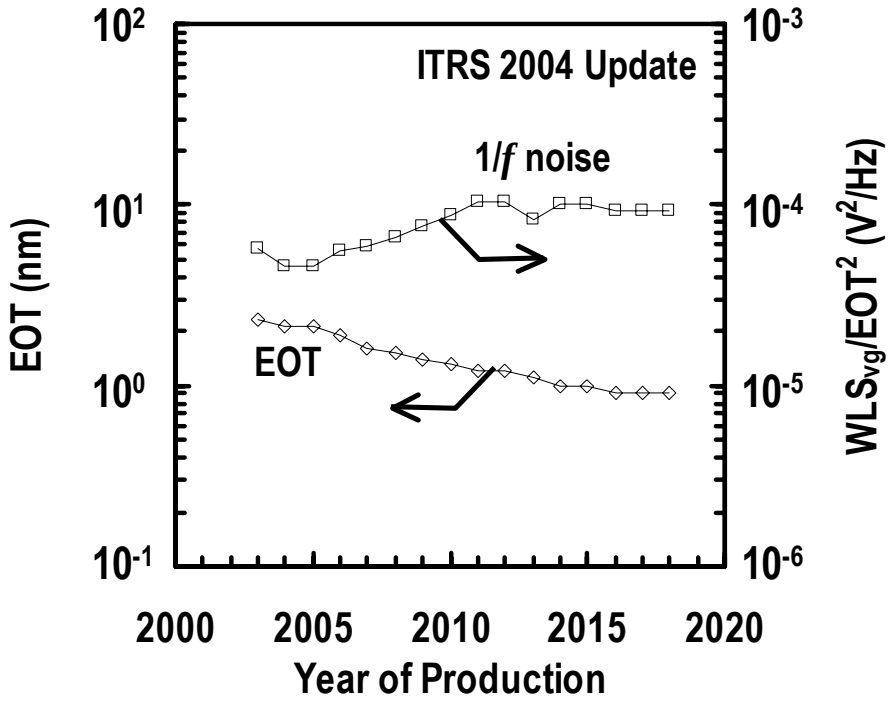

Fig. 1.10 Requirements of NMOS analog speed devices as defined in ITRS 2004 update version.

1.1.4 Requirements in Source/Drain Extension (SDE)

Miniaturization of MOSFET reduces the Source/Drain Extension (SDE) junction depths to minimize the device short-channel effects. While having an ultra-shallow junction, SDE must have a low sheet resistance to preserve low parasitic resistance that enables high drive currents. Fig. 1.11 shows the requirements of junction depth X_j and sheet resistance R_s for PMOS SDE. Junction depths of less than 20 nm with sheet resistance of about 1000 Ω/sq. will be needed for PMOS devices. In the next 5 years, severe requirements of sub-10-nm junctions with sheet resistance as low as 800 Ω/sq. will be required. Formation of this Ultra-Shallow Junction (USJ) for SDE with conventional low energy ion implantation will be high cost and difficult on controlling low energy. Therefore, a new doping method for USJ formation technology like Plasma Doping (PD) method will be highly demanded.

Typically, USJ are formed by high dose ultra-shallow doping method followed by nearly diffusion less annealing method. Fig. 1.12 shows potential solutions for USJ formation. Plasma doping combined with millisecond annealing like Flash Lamp Annealing (FLA) or non-melt Laser Annealing (LA) appears to be the most likely alternatives for sub-10-nm USJ formations. Plasma doping method is expected to have the following merits: (1) Easiness on controlling low energy doping, (2) High throughput, fast formation and compatibility for large wafer size, and (3) low cost.

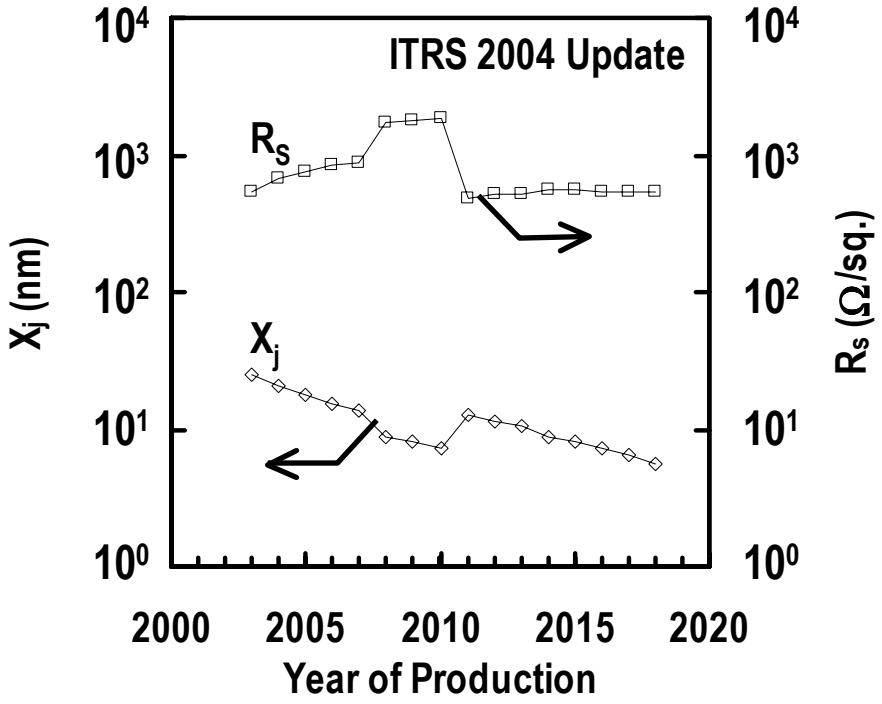

Fig. 1.11 Requirements of junction depth X_j and sheet resistance R_s for source/drain extension of PMOS devices.

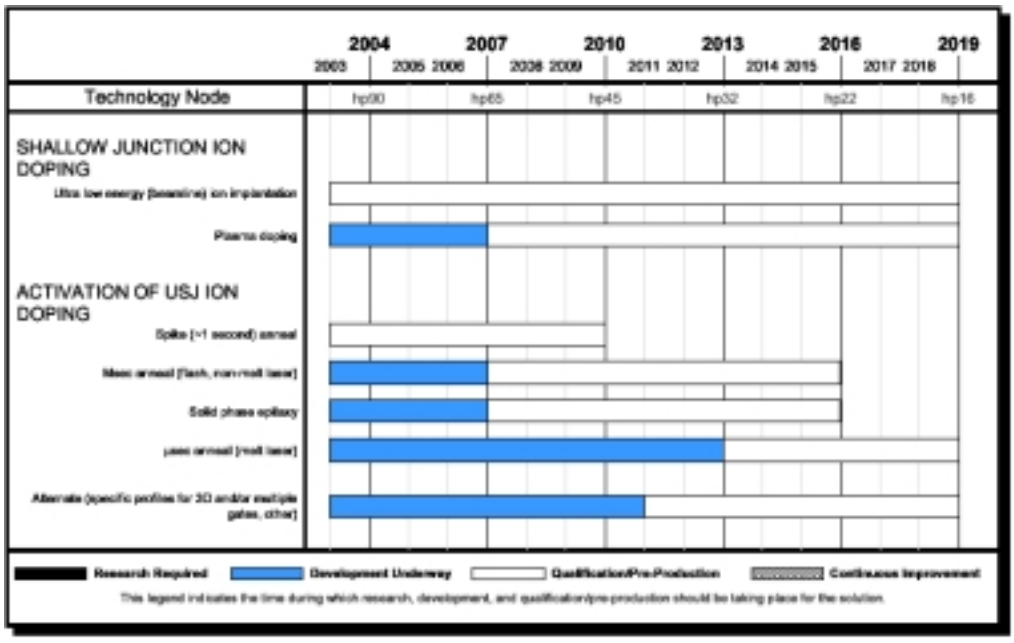

Fig. 1.12 Potential solutions for source/drain extension formations.

1.2 Motivations of This Study

In this thesis, a detail study of two major parts related to the electrical quality of vertically scaled to an extreme region of two MOSFET parameters will be evaluated. The first part is related to the channel quality of NMISFET with high-κ gate dielectrics. Low-frequency noise that is very important parameter in mixed or analog design will be carried out. The second part is related to the junction quality of ultra-shallow junction formed by plasma doping method.

1.2.1 Low-Frequency (1/*f*) Noise of NMISFET with La_2O_3 High-κ Gate Dielectrics

There have several reports on the superiority of electrical properties of La_2O_3. Low current densities at EOT of less than 1 nm, high drive current and high mobility of NMISFET can be achieved with La_2O_3 gate dielectrics. Good quality La_2O_3 thin films can be achieved by deposition over pre-treated chemical oxide substrate instead of HF-last substrate due to La-riched film formations. In this study, evaluations of the low-frequency noise of La_2O_3 gate insulated NMISFETs will be addressed. A unified model approach based on combined number fluctuation, correlated number - mobility fluctuation and mobility fluctuation models will be used. The possibility of the use La_2O_3 as gate dielectrics for analog applications will be evaluated. Lastly, considerations to obtain a better quality of La_2O_3 thin films will be discussed.

1.2.2 Analysis of Electrical Properties of Ultra-Shallow p^+/n Junctions Formed by Plasma Doping Method

Plasma doping method is an attractive method on ultra-shallow junction formations due to low energy doping. This new doping method that may result an amorphous doping layer must be recovered by annealing method. In sequence to impurity doping, new annealing methods like Flash Lamp Annealing (FLA) and Laser Annealing (LA) should be introduced to suppress deeper impurity diffusion. However, combination of plasma doping and these new instantaneous annealing may leave defects or interstitial impurity atoms that may act as generation-recombination centers. In this study, we examine the leakage current of ultra-shallow p^+/n junctions caused by traps leaving in space charge regions. At last, based on the above investigations, we will discuss an expected formation processes to form high device quality.

1.3 Outline of the Thesis

This thesis is composed of six chapters. In this chapter, we describe the background of this study, the perspective on CMOS technology, future requirements of gate dielectrics technology and source/drain extension formation, and our motivations on working on this study.

In chapter 2, we illustrate theoretical reviews to understand behaviors and mechanisms of the experimental results. MIS capacitor and p/n junction are the simplest device structure forming MISFET, having good satisfaction on evaluation the device quality. A universal theory on low-frequency noise of MISFET device is still a difficult

discussion until now. An approach on unified physical and empirical theory will be reviewed in this chapter.

Details of device fabrication procedures, appliances and instruments, and measurement techniques will be showed in chapter 3. Basic operations and principles of appliances, instruments, and measurement systems are necessary to interpret a raw process and the measured data.

In chapter 4, we will discuss the experimental results on low-frequency noise of La_2O_3 gate insulated NMISFET. We will use a comparison approach with standard thermal growth SiO_2 for benchmarking the channel quality.

Electrical characteristics of ultra-shallow p^+/n junctions formed by flash lamp and spike rapid thermal activation annealing in sequence to plasma doping method will be discussed in chapter 5. A standard p^+/n junctions formed by ion implantation followed by spike rapid thermal annealing will be used as a reference. Trap levels, numbers, life times will be showed in parallel to the absolute value of reverse-biased current density.

In the last chapter, we will summarize our works and the conclusions will be stated with further issues and expectation for the future works.

Chapter 2. Theoretical Review

Several experiment results provide us an intuitive understanding while most of them are difficult to understand. Basic theoretical and concepts are sometimes needed for comprehensive understanding of the origins, mechanism, and behaviors of the results. In this chapter, we discuss the principle MIS capacitor, basic origins of low-frequency noise and electrical characteristics of p/n junctions.

2.1 Metal-Insulator-Semiconductor (MIS) Capacitor

In order to analyze the experimental *C-V* characteristics, the comparison between ideal and experimental *C-V* is necessary. *C-V* curve is divided into three regime, inversion, depletion and accumulation. Capacitance of Si depends on the surface potential while the insulator capacitance is constant. So, in order to reach the ideal curves, the capacitance of Si should be calculated, which is expressed by following equation:

1) $U_S \geq 0$

$$C_S = C_D \hat{U}_S \frac{\sinh(U_S + U_F) + \sinh(-U_F)}{\left[e^{-U_F}(e^{-U_S} + U_S - 1) + e^{U_F}(e^{U_S} - U_S - 1)\right]^{\frac{1}{2}}} \qquad \textbf{Eq. 2.1}$$

2) $0 \geq U_S \geq 2U_F$

$$C_S = \mathrm{sgn}\{U_S\} C_D \frac{e^{\frac{U_F}{2}} \cdot \left\{e^{U_S} - 1\right\}}{2\left\{e^{-U_S} - U_S - 1\right\}^{\frac{1}{2}}} \qquad \textbf{Eq. 2.2}$$

3) $2U_F \geq U_S$

$$C_S = \frac{\varepsilon_S}{W_m} = \frac{C_D}{\int_0^{U_S} (e^{U(x)} - 1) \frac{dU(x)}{F\{U(x), U_F\}}} \quad \textbf{Eq. 2.3}$$

$$F\{U_S, U_F\} \equiv \{\exp(-U_F)[\exp(-U_S) + U_S - 1] + \exp(U_F)[\exp(U_S) - U_S - 1]\}^{\frac{1}{2}} \quad \textbf{Eq. 2.4}$$

where *U(x)* and *Us* in above equation is defined as the following.

$$U_S \equiv \frac{q\phi_S}{kT} \quad \textbf{Eq. 2.5}$$

$$U(x) \equiv \frac{q\phi(x)}{kT} \quad \textbf{Eq. 2.6}$$

Hence, the capacitance of MIS diode can be calculated with the following equation.

$$C = \frac{C_i C_s}{C_i + C_s} \quad \textbf{Eq. 2.7}$$

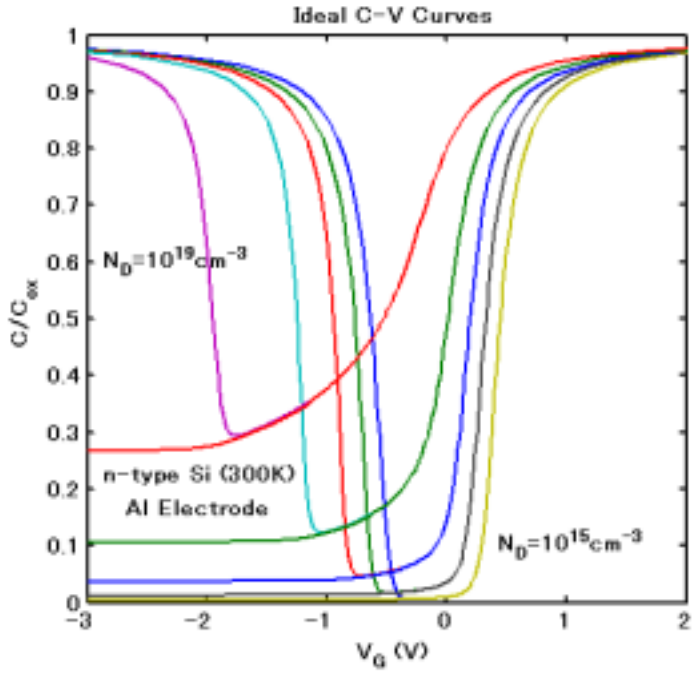

Fig. 2.1 Calculated ideal *C-V* curves of Al/insulator/n-Si with doping concentrations increased in every decade.

2.2 Low-Frequency Noise

A various models have been used to explain the 1/*f* noise in MOSFET devices. It has been generally accepted that the 1/*f* noise in the conduction channel of the device is associated with capture and emission of charge carriers from the traps in the oxide, very near to the Si/SiO_2 interface. In this subsection, we discuss some general properties of low-frequency noise.

2.2.1 Basic Mathematic in Noise Analysis

For a continuous value random variable *X*, the Probability Density Function (PDF) can be specified by the following expression.

$$f_x(x) \geq 0\,; \qquad \int_{-\infty}^{+\infty} f_x(x)dx = 1 \qquad \textbf{Eq. 2.8}$$

From the Probability Density Function, we can calculate all the moments of the random variable. The most important expressions for noise analysis are the mean and the mean square as respectively shown as below.

$$\overline{X} = \int_{-\infty}^{+\infty} f_x(x)dx \qquad \textbf{Eq. 2.9}$$

$$\overline{X^2} = \int_{-\infty}^{+\infty} x^2 f_x(x)dx \qquad \textbf{Eq. 2.10}$$

The mean square is often interpreted as the average power of a signal *X*. The square root of this power (denoted as RMS) represents as equivalent constant signal with power equal to the average power of *X*. From the mean and the mean square, we can calculate the variance of *X* as the following.

$$\sigma_x^2 = \overline{X^2} - \left(\overline{X}\right)^2 \qquad \textbf{Eq. 2.11}$$

This is interpreted as the square distance of X from its mean. When X has zero mean, its variance is equal to the mean square. The variance is often used to estimate the noise power.

For modeling a noise waveform, we may take a random process $X(t)$, where $-\infty \leq t \leq +\infty$. It is an infinite collection of random variables (noise samples) indexed by times t. For times t_1, t_2, t_3, …, t_n, the samples $X(t_1)$, $X(t_2)$, $X(t_3)$, …, $X(t_n)$ are random variables. In noise analysis, it is important to know the process mean and the autocorrelation function. The autocorrelation is expressed as below.

$$R_x(t+\tau) = \overline{X(t+\tau)X(t)} \qquad \textbf{Eq. 2.12}$$

Many important noise processes are modeled as stationary random processes, *i.e.*, processes with time invariant statistics. If both mean and autocorrelation function are time invariants, which is satisfying

$$\overline{X(t+\tau)} = \overline{X(\tau)} \qquad \textbf{Eq. 2.13}$$

$$R_x(t+\tau) = R_x(\tau) \qquad \textbf{Eq. 2.14}$$

then $X(t)$ is a Wide-Sense Stationary (WSS) process and its autocorrelation function has the following properties

a. The average process power is $R_x(0) = \overline{X^2(t)}$.

b. $R_x(\tau)$ is an even function, which is $R_x(\tau)=R_x(-\tau)$.

In the time range $0 \leq t \leq T$, the Fourier Transform of $X(t)$ is

$$X(t) = \sum_{-\infty}^{+\infty} \alpha_n \exp(j\omega_n t) \qquad \textbf{Eq. 2.15}$$

where,

$$\alpha_n = \frac{1}{T}\int_0^T X(t)\exp(-j\omega_n t)dt \qquad \textbf{Eq. 2.16}$$

The spectral power density of $X(t)$ is defined as the following.

$$S_x(f) = \lim_{T\to\infty} \overline{2T\alpha_n\alpha_n^*} \qquad \textbf{Eq. 2.17}$$

According to the Wiener-Khintchine theorem, the autocorrelation function and power spectral density function of a random variable $X(t)$ has the following relationship.

$$S_x(f) = 2\int_{-\infty}^{+\infty} R_x(\tau)\exp(-j2\pi f\tau)d\tau \qquad \textbf{Eq. 2.18}$$

$$R_x(\tau) = \int_0^{+\infty} S_x(f)\cos(2\pi f\tau)df \qquad \textbf{Eq. 2.19}$$

From the autocorrelation properties of a stationary process, when $\tau = 0$ in Eq. 2.19, we can obtain

$$R_x(0) = \overline{X^2(t)} = \int_0^{+\infty} S_x(f)df \qquad \textbf{Eq. 2.20}$$

This shows the physical meaning of the power spectral density that is mean square of random variable in the unit frequency bandwidth.

In noise analysis, it is necessary to estimate the mean and the autocorrelation function of a stationary noise process. There are two approaches to estimate them: the ensemble average and the time average. In the ensemble average, a large number of identical systems are constructed and measured simultaneously to extract the statistics in which we are interested. As a large number of identical systems are not available in practical experiments, this approach is not well suited for noise measurements. Instead of this, the time average is often used to analyze experimental noise data, as long as the noise process is stationary.

2.2.2 Generation and Recombination Noise

In semiconductor materials and devices, generation-recombination (GR) noise is

caused by fluctuation in the number of free carriers inside of two terminals semiconductor device sample, associated with random transitions of charge carriers between states in different energy bands. Typical examples of transitions are between conduction band and localized levels in the energy band gap, conduction and valence band, etc. Therefore, generation-recombination noise is inherently due to fluctuations of carrier number by keeping the total charge to neutrality.

As a simple model, we assume that there are N carriers in the device, with a generation rate $g(N)$ and recombination rate $r(N)$. The fluctuation in the number of carriers is described by a differential equation of the following form.

$$\frac{dN}{dt} = g(N) - r(N) + \Delta g(t) - \Delta r(t) \qquad \textbf{Eq. 2.21}$$

In here, $N = N_0 + \Delta N$, where N_0 is the equilibrium number of carriers. We may expand $g(N)$ and $r(N)$ in Taylor series and neglect the higher order terms:

$$g(N) = g(N + N_0) = g(N_0) + \left.\frac{\partial g}{\partial N}\right|_{N_0} \Delta N \qquad \textbf{Eq. 2.22}$$

$$r(N) = r(N + N_0) = r(N_0) + \left.\frac{\partial r}{\partial N}\right|_{N_0} \Delta N \qquad \textbf{Eq. 2.23}$$

By substituting these two equations into Eq. 2.21, we obtain

$$\frac{dN}{dt} = g(N_0) - r(N_0) + \left.\left(\frac{\partial g}{\partial N} - \frac{\partial r}{\partial N}\right)\right|_{N_0} \Delta N + \Delta g(t) - \Delta r(t) \qquad \textbf{Eq. 2.24}$$

Here we define $H(t)=\Delta g(t) - \Delta r(t)$ as a random noise term, and τ as the lifetime of the carriers that gives

$$\frac{1}{\tau} = \left(\frac{\partial r}{\partial N} - \frac{\partial g}{\partial N} \right)\Bigg|_{N_0} \qquad \textbf{Eq. 2.25}$$

By giving $g(N_0) = r(N_0)$, we may simplify Eq. 2.24 into the following form.

$$\frac{d\Delta N(t)}{dt} = -\frac{\Delta N(t)}{\tau} + H(t) \qquad \textbf{Eq. 2.26}$$

For $0 \leq t \leq T$, we can expand $H(t)$ and $\Delta N(t)$ in a Fourier series

$$H(t) = \sum_{-\infty}^{+\infty} \alpha_n \exp(j\omega_n t) \qquad \textbf{Eq. 2.27}$$

$$\Delta N(t) = \sum_{-\infty}^{+\infty} \beta_n \exp(j\omega_n t) \qquad \textbf{Eq. 2.28}$$

By substituting Eq. 2.27 and Eq. 2.28 into Eq. 2.26, we may find

$$\beta_n = \frac{\alpha_n \tau}{1 + j\omega_n \tau} \qquad \textbf{Eq. 2.29}$$

The power spectral density of $H(t)$ and $\Delta N(t)$ is defined as the following.

$$S_H(f) = \lim_{T \to \infty} \overline{2T\alpha_n \alpha_n^*} \qquad \textbf{Eq. 2.30}$$

$$S_{\Delta N}(f) = \lim_{T \to \infty} \overline{2T\beta_n \beta_n^*} \qquad \textbf{Eq. 2.31}$$

Since $H(t)$ is a white noise source, then $S_H(f) = S_H(0)$. From Eq. 2.30 and Eq. 2.31, then we may find

$$S_N(f) = \frac{S_H(0)\tau}{1 + \tau^2 \omega^2} \qquad \textbf{Eq. 2.32}$$

$$\overline{\Delta N^2} = \int_0^{+\infty} S_N(f) df = \frac{S_H(0)\tau}{4} \qquad \textbf{Eq. 2.33}$$

Widely used expression for generation-recombination noise can be obtained with substituting Eq. 2.33 into Eq. 2.32. As we may find

$$S_N(f) = 4\overline{\Delta N^2}\,\frac{\tau}{1+\tau^2\omega^2} \qquad \textbf{Eq. 2.34}$$

The spectrum of the fluctuations in Eq. 2.34 is in the form of a Lorentzian type with two parameters, *i.e*., the variance of number fluctuations and the characteristic time of charge carriers. A typical noise curve of the current in small device as a result of carrier interactions with a single trap center is illustrated in Fig 2.2. The noise spectrum is of the shape of Debye-Lorentzian type.

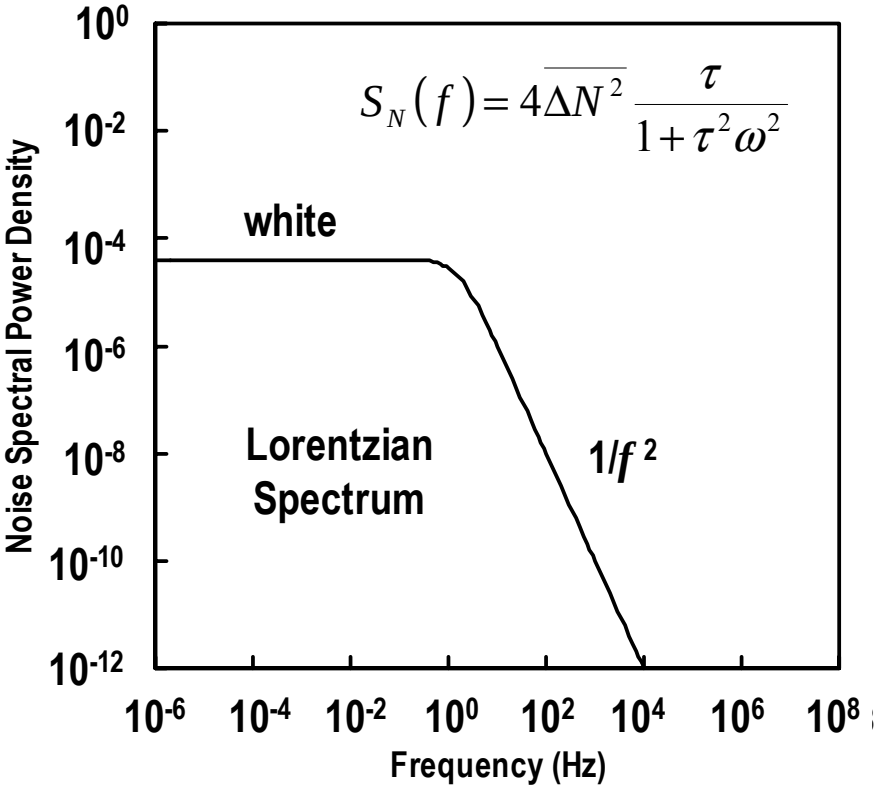

Fig. 2.2 Typical noise curve of the current in small device as a result of carrier interactions with single trap center. The noise spectrum is of the shape of Debye-Lorentzian type.

2.2.3 Low-Frequency Noise Originated from G-R Mechanism

A superposition of a large number of Lorentzian spectra might result is a 1/*f* spectrum. To investigate this problem, we rewrite Eq. 2.34 instead of in the following form.

$$S_N(f) = 4\overline{\Delta N^2}\int_0^{+\infty} \frac{\tau g(\tau)}{1+\tau^2\omega^2} d\tau \qquad \textbf{Eq. 2.35}$$

where the probability $g(\tau)d\tau$ is normalized by requiring

$$\int_0^{+\infty} g(\tau) d\tau = 1 \qquad \textbf{Eq. 2.36}$$

In a particular case, we find

$$g(\tau)d\tau = \frac{d\tau}{\tau \ln(\tau_1/\tau_0)} \qquad \textbf{Eq. 2.37}$$

for $\tau_0 \le \tau \le \tau_1$ and $g(\tau)d\tau = 0$ otherwise, so that $g(\tau)$ is normalized, we may obtain the following expression.

$$S_N(f) = \frac{2\overline{\Delta N^2}}{\pi f \ln(\tau_1/\tau_0)}\left\{\tan^{-1}(\omega\tau_1) - \tan^{-1}(\omega\tau_0)\right\} \qquad \textbf{Eq. 2.38}$$

This is correspond to

$$S_N(f) = \frac{2\overline{\Delta N^2}\tau_1}{\ln(\tau_1/\tau_0)} \qquad for \quad \omega << \frac{1}{\tau_1} \qquad \textbf{Eq. 2.39}$$

$$S_N(f) = \frac{\overline{\Delta N^2}}{f \ln(\tau_1/\tau_0)} \qquad for \quad \frac{1}{\tau_1} << \omega << \frac{1}{\tau_0} \qquad \textbf{Eq. 2.40}$$

$$S_N(f) = \frac{\overline{\Delta N^2}/\tau_0}{\pi^2 f^2 \ln(\tau_1/\tau_0)} \qquad for \quad \omega >> \frac{1}{\tau_0} \qquad \textbf{Eq. 2.41}$$

Thus, we see that the spectrum is white at low frequencies, goes $1/f^2$ at very high frequencies, and varies as 1/*f* over a wide intermediate frequency range. A graphic

representation of the discussion above is shown in Fig 2.3. From the figure, ten Lorentzian spectra have been added, each with time constant 10 times higher than the previous one. The resultant summation of the spectra gives a 1/*f* type spectrum.

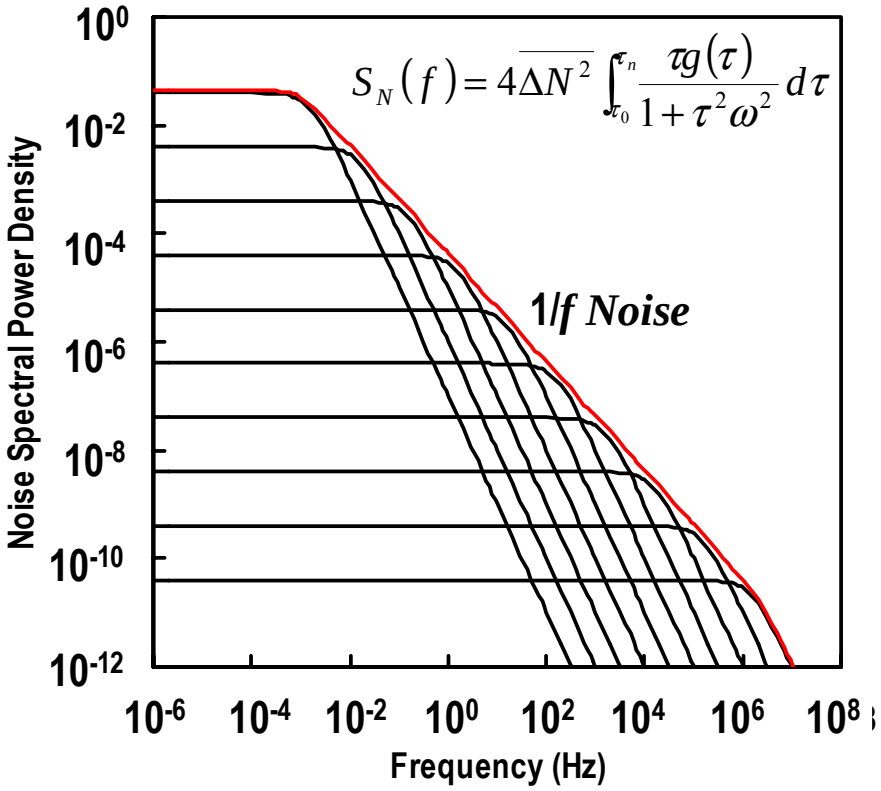

Fig. 2.3 Graphical representation of 1/*f* noise as a result of summation of ten Lorentzian spectra.

A variety of models have been proposed to explain 1/*f* noise in MOSFETs. After much controversy, it is now widely accepted that the noise of MOSFETs is associated with the capture and emission of charge carriers in the conducting channel from traps in the oxide, very near to the Si/SiO_2 interface. Fluctuations in the oxide-trap charge couple to the channel, both directly through fluctuations in the numbers of inversion

charges, and indirectly through fluctuations in scattering associated with changes in trap occupancy. Data from narrow-channel MOSFETs confirm that both effects can be important. In general, noise studies on n-channel MOSFETs tend to follow a number fluctuation model, at least to first order. In p-channel devices, noise is often attributed to both number and mobility fluctuations.

2.2.4 Low-Frequency Noise Originated from Mobility Fluctuation

F. N. Hooge proposed mobility fluctuation model for the first time. It was modeled base on a number of experiments in metal thin film. He found that the noise in film conductors could be characterized by

$$\frac{S_V(f)}{V^2} = \frac{\alpha_H}{N_C f} \qquad \textbf{Eq. 2.42}$$

where α_H is a dimensionless Hooge's empirical parameter and N_C is the number of charge carrier in the conductor. Later, Hooge found that dimensionless α_H parameter is due to electron phonon scattering that is related to the crystalline quality of film conductors. Hooge's theory gives a pure $1/f$ spectrum in all frequency range.

In this work, we measure the noise spectral power density of the drain currents. The La_2O_3 gate insulated NMISFET devices are operated from weak to strong inversion in both linear and saturation regions. As previously reported, high-κ gate insulated NMISFETs are usually suffering from the degradation of channel mobility. From this reason, a combined number fluctuation, correlated number - mobility fluctuation and mobility fluctuation models approach will be used for analyzing the noise power density instead of pure number fluctuation.

2.3 Electrical Characteristics of p/n Junction

All semiconductors contain impurities. Some impurities are intentionally introduced as dopant atoms (shallow-level impurities), recombination centers (deep-level impurities) to reduce the device lifetime, or deep-level impurities to increase substrate resistivity. Many impurities are intentionally incorporated during crystal growth or device processing. The impurities may be foreign impurities (e.g., metal), crystallographic point defects (e.g., vacancies and interstitials, or structural defects (e.g., stacking faults and dislocations). In this subsection, we will review the statistical generation and recombination in semiconductor and its effect to pn junction leakage mechanism.

2.3.1 Generation and Recombination in Semiconductor

The band diagram of a perfect single crystal semiconductor consists of a valence band and a conduction band separated by the band gap. When foreign atoms or crystal defects perturb the periodicity of the single crystal, discrete energy levels are introduced into the band gap, shown by the E_T lines in Fig. 2.4. Each line represents one such defect with energy E_T. Such defects are commonly called generation-recombination (G-R) centers or traps. G-R centers lie deep in the band gap and are well known as deep energy level impurities, or simply deep-level impurities. They act as recombination centers when there are excess carriers in the semiconductor and as generation centers when the carrier density is below its equilibrium value as in the reverse-bias space charge region of pn junctions or MOS-capacitors.

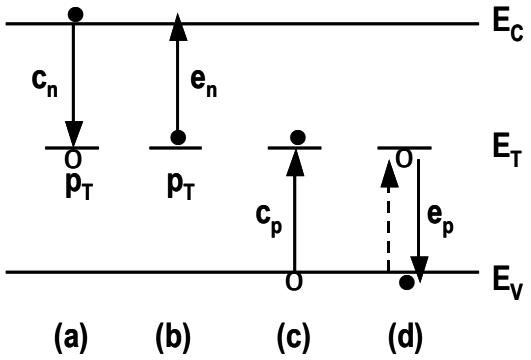

Fig. 2.4 Energy band diagram for semiconductor with deep-level impurities. The capture and emission processes for electron is shown in (a) and (b), while (c) and (d) is for hole.

Considering the deep level impurity shown in Fig. 2.4, it has an energy E_T and consists of N_T impurities/cm^3 uniformly distributed through out the semiconductor. To follow the various capture and emission processes, the G-R center first capture an electron from the conduction band (a), and characterized by the capture coefficient c_n. After electron capture, one of two events takes place. The center can either emit the electron back to the conduction band from where it came, called electron emission e_n (b), or it can capture a hole from the valence band as c_p (c). After either of these events, the G-R center is occupied by a hole and again has two choices, either it emits the hole back to the valence band e_p (d) or captures an electron c_n (a). A *recombination* event is (a) followed by (c) and *generation* is (b) followed by (d), while the *trapping* event is (a) followed by (b) or (c) followed by (d). Whether the impurity acts as a trap or a G-R center depends on the location of the Fermi level in the band gap, the temperature, and the cross sections of the impurity. Generally those impurities whose energies lie near the middle of the band gap behave as G-R centers, whereas those near the band edges act as traps.

A G-R center can be one of two charge states, i.e., n_T state when occupied by electron and p_T state when occupied by a hole. The concentration of G-R centers occupied by electrons n_T and holes p_T must equal the total concentration N_T, or $N_T = n_T + p_T$. When electron and holes recombine or are generated, the electron concentration in the conduction band n, the hole concentration in the valence band p, and the charge state of the center n_T or p_T are all function of time. The time rate of change for electron n due to G-R mechanisms is given by,

$$\left.\frac{dn}{dt}\right|_{G-R} = (b) - (a) = e_n n_T - c_n n p_T \qquad \textbf{Eq. 2.43}$$

While for hole p, we may find the similar expression,

$$\left.\frac{dp}{dt}\right|_{G-R} = (d) - (c) = e_p p_T - c_p p n_T \qquad \textbf{Eq. 2.44}$$

The capture coefficient cn is defined by,

$$c_n = \sigma_n \upsilon_{th} \qquad \textbf{Eq. 2.45}$$

where ν_{th} is the thermal velocity of the electrons and σ_n is the electron capture cross section of the G-R center. Whenever an electron or hole is captured or emitted, the center occupancy changes, and that rate of change is given by,

$$\left.\frac{dn_T}{dt}\right|_{G-R} = \frac{dp}{dt} - \frac{dn}{dt} = \left(c_p n + e_p\right)\left(N_T - n_T\right) - \left(c_p p + e_n\right) n_T \qquad \textbf{Eq. 2.46}$$

This equation is in general nonlinear, with n and p being time-dependent variables. It can be solved easily if the equation can be linearized. Two cases allow this simplification: (1) In a reverse-biased space-charge region both n and p are small and can, to first order, be neglected. (2) In the quasi-neutral regions n and p are reasonably constant. Solving Eq. 2.46 for condition (2) gives $n_T(t)$ as

$$n_T(t) = n_T(0) e^{-t/\tau} + \frac{e_p + c_n n}{e_n + c_n n + e_p + c_p p} N_T \left(1 - e^{-t/\tau}\right) \qquad \textbf{Eq. 2.47}$$

where $n_T(0)$ is the concentration of G-R centers occupied by electrons at t = 0 and t = $1/(e_n + c_n n + e_p + e_p p)$. The steady state concentration as $t \to \infty$ is

$$n_T = \frac{e_p + c_n n}{e_n + c_n n + e_p + c_p p} N_T \qquad \textbf{Eq. 2.48}$$

This equation shows the steady-state occupancy of n_T to be determined by the electron and hole concentrations as well as by the emission and capture rates.

2.3.2 Rectifying Characteristics of p/n Junction

The basic rectifying characteristics of p/n junction can be described with the ideal current-voltage equation. Total current in p/n junction for forward-bias and reverse-bias condition can be given as

$$J = J_n + J_p = \left(\frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p} \right) \left\{ \exp\left(-\frac{qV}{kT} \right) - 1 \right\} \qquad \textbf{Eq. 2.49}$$

where n_{p0} and p_{n0} are respectively electron and hole densities on p- and n- side.

$$L_n \equiv \sqrt{D_n \tau_n} \qquad \textbf{Eq. 2.50}$$

$$L_p \equiv \sqrt{D_p \tau_p} \qquad \textbf{Eq. 2.51}$$

where τ_n and τ_p are recombination lifetime for electrons and holes, respectively. The saturation current is defined as

$$J_S \equiv \left(\frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p} \right) \qquad \textbf{Eq. 2.52}$$

So, Eq. 2.49 can be simplified into the following.

$$J = J_S \left\{ \exp\left(-\frac{qV}{kT} \right) - 1 \right\} \qquad \textbf{Eq. 2.53}$$

The above equation is ideal current-voltage equation and well known as Shockley equation, as he derives the equation for the first time.

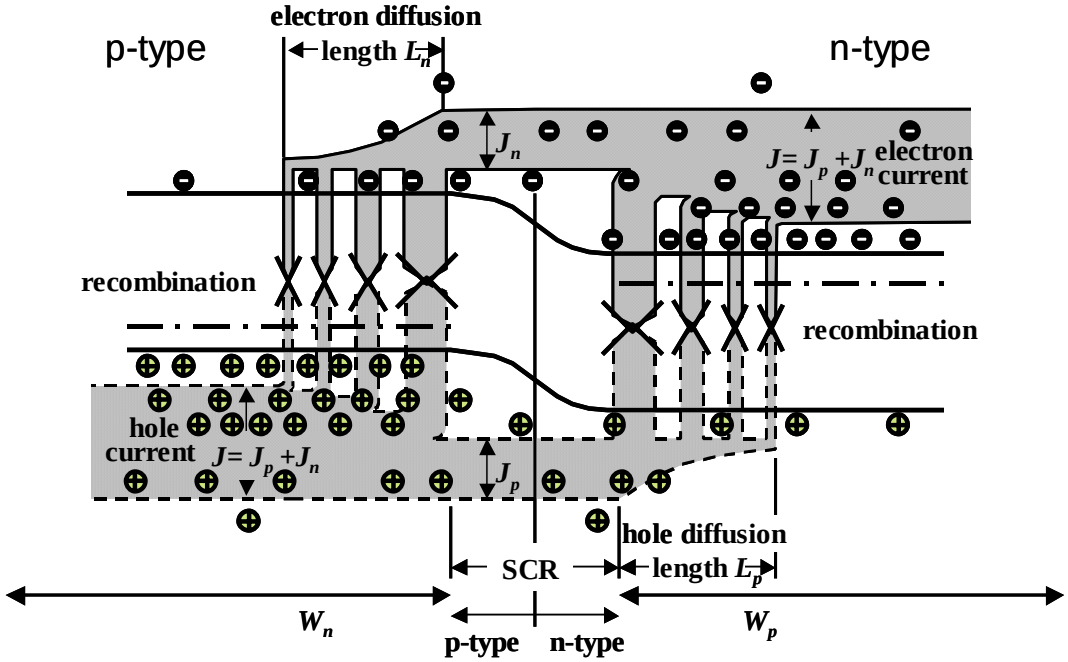

Fig. 2.5 Principal diffusion current mechanism of in p/n junction. The total current are determined by recombination of excess minority carriers in neutral region.

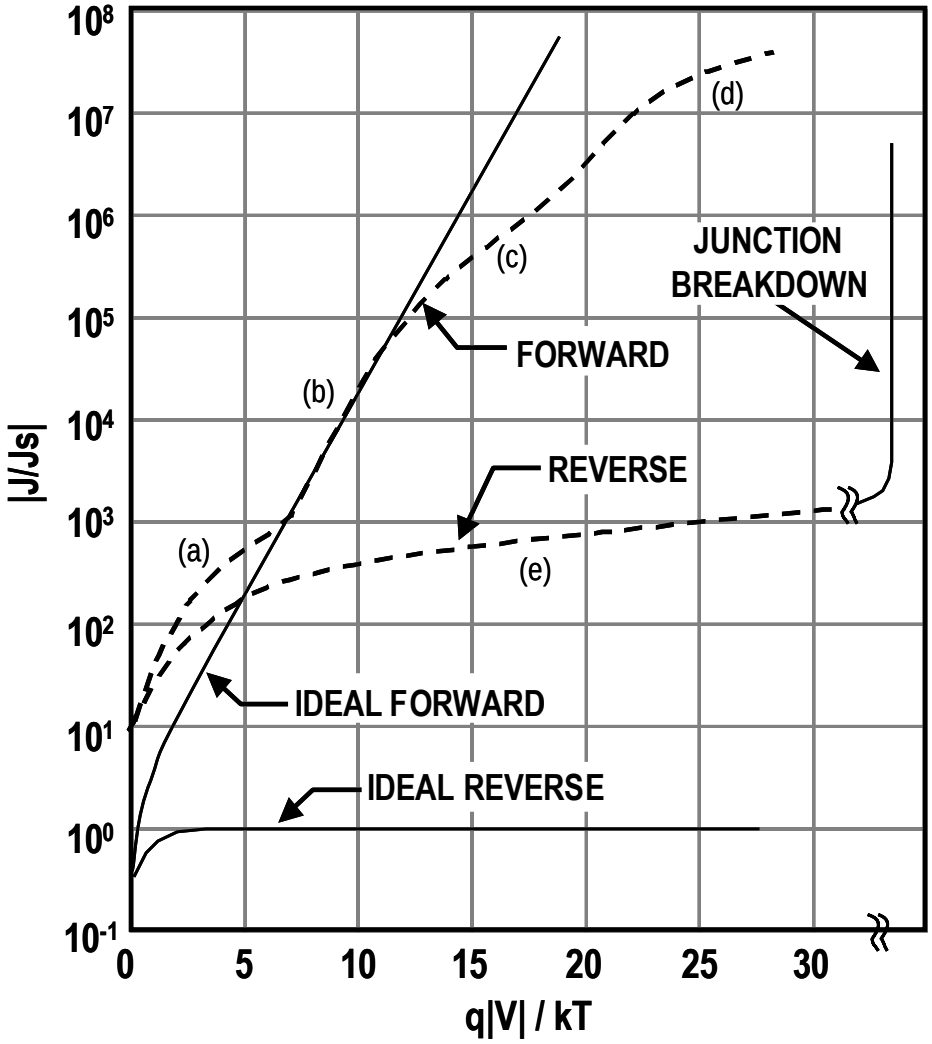

Fig. 2.6 *C-V* characteristics of a practical Si p/n junction. (a) G-R current region. (b) Diffusion current region. (c) High-injection current region. (d) Series resistant effect. (e) Reverse leakage current due to G-R processes and surface effects.

Chapter 3. Device Fabrication and Characterization Methods

Semiconductor devices are case sensitive to the process fabrications that cleanliness, material formations, chemical purities are much important in the effect to their electrical characteristics. The cleanliness of a clean room is determined with the number of particles in a cubic feet or its class. Most of LSIs (Large Scale Integrations) are produced in an automated ultra-clean room that only an extremely very small amount of particles are tolerated. In the next place, material formations that produce more defect in crystals or cavities in amorphous might decrease the device quality due to uncontrollable characteristics. As an example, thermally grown SiO_2 has a better quality for gate oxide than that of deposited as deposited SiO_2 produce more interface state and trap densities. Subsequently, impurities of the chemical solutions may produce chemical contamination that decrease the device characteristics like excess of light cation species such as sodium or potassium lowered the gate oxide quality since they act as mobile charge in insulators. Wafer cleaning like a standardized RCA cleaning method are frequently used to remove these of particle contaminations.

In this chapter, we describe the details of procedures, instrumentations, appliances, and tools for fabrications and characterizations of La_2O_3 NMISFET and ultra-shallow p^+/n junction devices. Depending on its necessity, basic physics or operations are sometimes illustrated.

3.1 Fabrication Method for La_2O_3 NMISFET

Miss in fabrication processes may directly influence the device characteristics and even its performances. On the contrary, failing in the expected device characteristics sometimes can be traced from how the device was fabricated. In this sub section, we explain the detail of our experimental procedure for fabricating La_2O_3 NMISFETs.

3.1.1 Device Fabrication Procedure

The device fabrication flow chart and the top view micrograph for La_2O_3 NMISFET are illustrated in Fig 3.1, while the cross-sectional description in La_2O_3 NMISFET device fabrication is shown in Fig 3.2. NMISFET device fabrication was started from S/D implanted Si(100) substrate. The wafer was cut in 2 cm×2 cm. After removing the initial oxide of 300 nm with buffered-HF for about 2 min, the substrate was rinsed with standard RCA cleaning process. Chemical oxide surface treatment by dipping in H_2O_2 for 30 min was applied to obtain Si-O passivation layer. La_2O_3 thin film was deposited by e-beam evaporation at substrate temperature 250^{o}C. Because as-deposited samples are usually of low electrical quality with many defects or oxygen vacancies, the sample was annealed in O_2 ambient at 400^{o}C for 5 min. After Al metal gate deposition with bell jar vacuum evaporation, the gate area was defined with photolithography followed by Al metal etching with H_3PO_4 solution at 55^{o}C. The PAD area was formed with lift-off process under acetone solution. Lastly, after removing the native oxide, the Al back electrode was deposited with vacuum thermal evaporator.

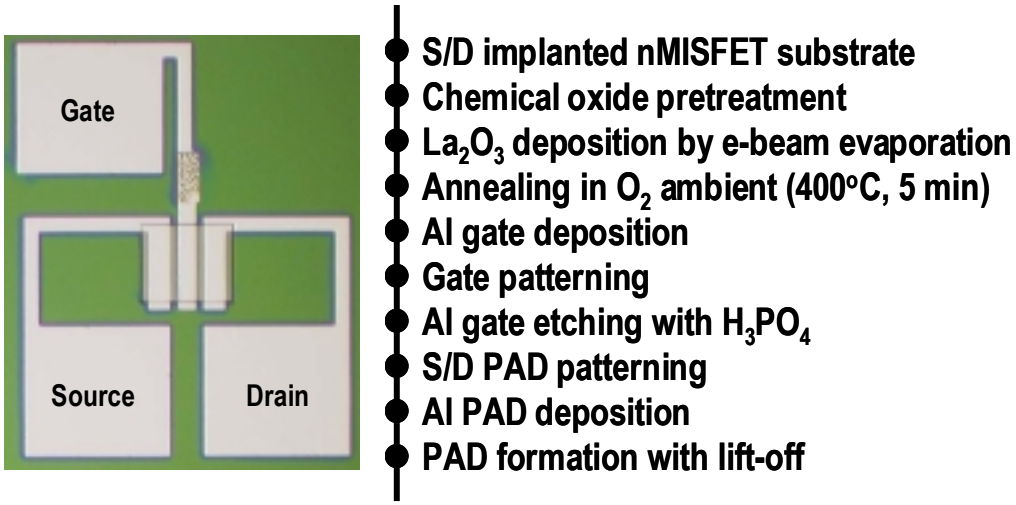

Fig. 3.1 The top view micrograph of La_2O_3 NMISFET with W×L = 54 μm × 10 μm and the device fabrication flow chart.

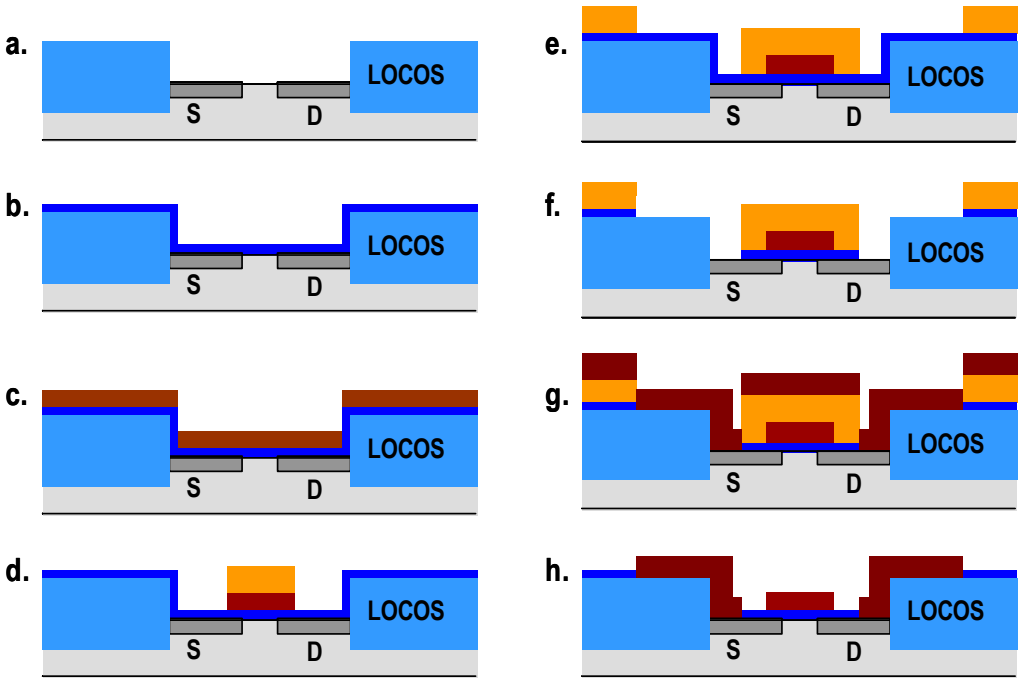

Fig. 3.2 Cross-sectional description in La_2O_3 NMISFET device fabrication.

3.1.2 Substrate Cleaning and Surface Pre-treatment

Before depositing the La_2O_3 thin films with e-beam evaporation, Si substrate cleaning is applied to avoid particle contaminations like metallic or organic species and to remove native oxide. A standard RCA wet cleaning procedure is used for removal of that contamination species and the native oxides. Metallic and organic contaminants are removed with Sulfuric-Peroxide Mixture (SPM), a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) with composition of H_2SO_4: H_2O_2 = 4:1. Subsequently, the native oxide is removed by dipping in 1% fluoric acid (HF) for 5 minutes. In the later, as-cleaned substrate with HF is called HF-last.

In semiconductor processes, de-ionized, highly purified and filtered ultra-pure water is utilized for cleaning process, since this can remove many traces like particulate or bacterial contaminations. Water resistivity is often used for monitoring their purity. Theoretically, pure water at 25^{o}C has resistivity of 18.3 MΩ-cm. In this experiment, ultra-pure water with resistivity of more than 18.2 MΩ-cm, fewer than 1.2 bacterial colonies per milliliter, and no particle larger than 0.25 μm are used.

Surface pre-treatment with hydrogen peroxide for 30 minutes was applied to coverage the silicon surface with chemical oxide. This chemical oxide coverage substrate is called CO. There are significant differences between HF-last and CO for high-κ gate dielectrics. The superiority of La_2O_3 over CO to HF-last has been previously reported as the CO may enhance the dielectrics and surface quality. La_2O_3 with CO promises film quality with La_2O_3-riched that gives lower EOT and lower leakage currents. This procedure of wafer cleaning process is shown in Fig. 3.3. As to avoid particle contamination or oxidation from air exposure, the wafer is immediately

loaded into the e-beam evaporation-loading chamber.

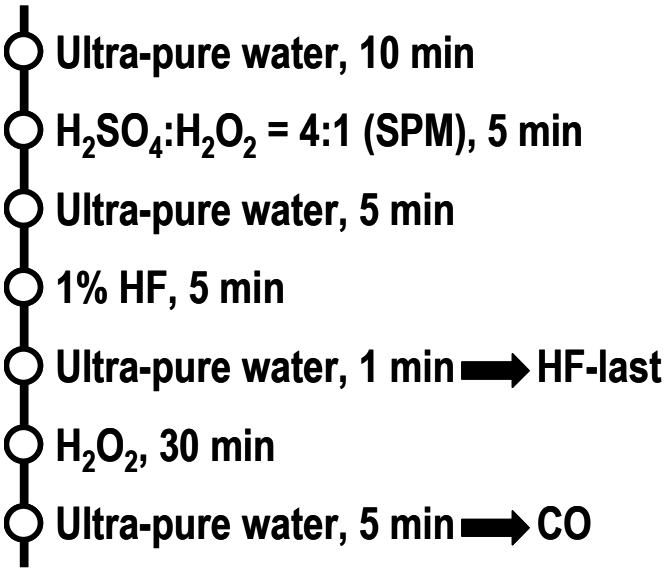

Fig. 3.3 Flowchart for the wafer cleaning process. The wafer is immediately loaded into the e-beam evaporation-loading chamber to avoid particle contamination and oxidation from air exposure.

3.1.3 E-Beam Evaporation Method

It is different from SiO_2, high-κ gate dielectric materials must be deposited or epitaxially growth over Si substrate. As originated substrate is silicon, a high quality of thermal grown SiO_2 can be obtained by oxidizing the wafer at high temperature. However, we cannot get high-κ thin films by this technique. Deposited thin films are usually suffered from the risk of defects, cavities, or compositions that act as carrier trap centers. The epitaxial growth is requiring the material lattice matching with the original substrate to maintain the crystallinity. Growing crystalline thin films over a wide

mismatch surface yield lattice with dislocations that function as paths for carrier to get through. For gate dielectric applications, amorphous or perfect crystallinity of thin films is recommended. In this experiment, we deposited La_2O_3 by ultra high-vacuum e-beam evaporation system.

The schematic drawing of e-beam evaporation system for dielectric deposition is depicted in Fig. 3.4. It can be seen that the system is utilized with 4 e-guns and 4 dielectric sources. The evaporated source is bombarded with electron beam with acceleration voltage of -5 kV. The substrate is heated of ~250^{o}C to evaporate any suspected moisture. Background pressure of the growing chamber is of ~10^{-10} Torr, and the pressure during deposition is kept at ~10^{-9} to ~10^{-7} Torr. Such ultra-high vacuum pressure can be obtained with utilizing an ion pump, titanium sublimation pump and even cooling the chamber with liquid nitrogen.

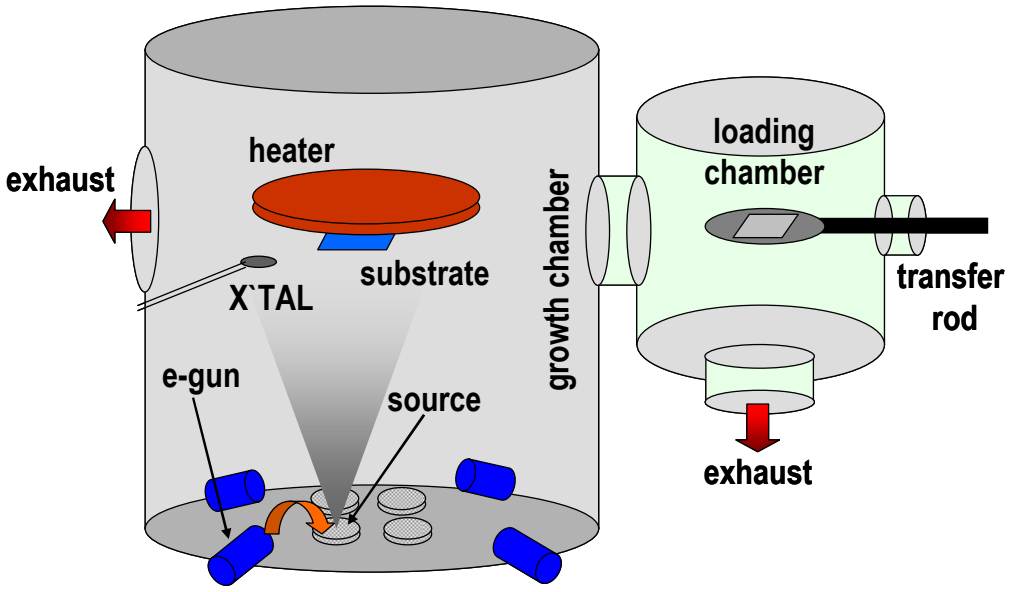

Fig. 3.4 Schematic drawing of e-beam evaporation system for dielectric deposition. The system is utilized with 4 e-guns and 4 dielectric sources. The background pressure is of ~10^{-10} Torr, and the deposition pressure is kept ~10^{-9} to ~10^{-7} Torr.

3.1.4 Rapid Thermal Annealing

Thermal processes are often used for defects recovery or molecular introduction to dielectric thin films, for lattice recovery or impurity electrical activation of doped or ion implanted wafers. In this experiment, Rapid Thermal Processing MILA-3000 from ULVAC is used for annealing deposited La_2O_3 thin films. Fig. 3.5 illustrated the schematic drawing for MILA-3000. High purity gas ambience can be obtained by pumping out and purging with the in use ambient gas. This RTP system is heated-up by infrared lamp heating furnace and cooled-down by flowing water radiator. The furnace temperature is of the range from room temperature to around 1200^{o}C with ramp-up of less than 50^{o}C/sec and much slower on cooling-down. The available of ambient gases are N_2 and O_2 at atmospheric pressure by keeping the flowing gas at the rate of 1 lt./min.

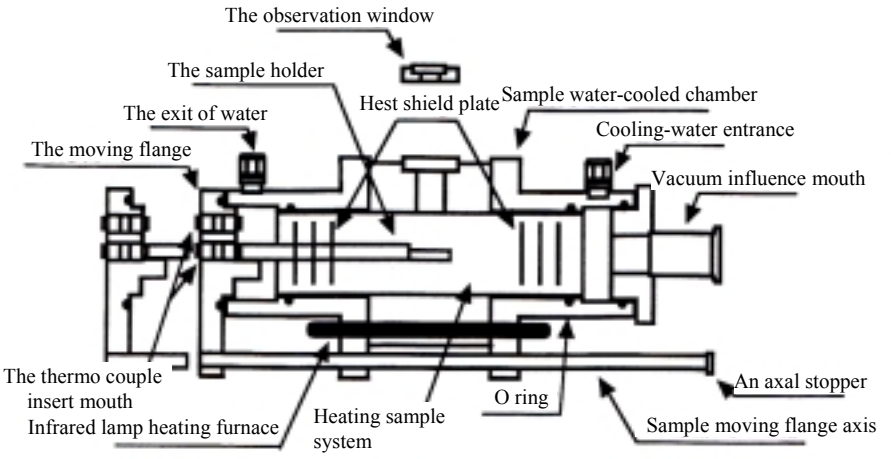

Fig. 3.5 Schematic drawing for Rapid Thermal Annealing (RTA) MILA-3000. High purity gas ambience can be obtained by pumping out and ambient gas purging.

3.1.5 Vacuum Thermal Evaporation Method

All of Al metals in this work were obtained from deposition with bell jar vacuum thermal evaporation. Fig. 3.6 illustrates a schematic drawing for vacuum thermal evaporation system. The system is utilized with Turbo Molecular Pump (TMP) to pump down to several 10^{-5} Torr. In case of MIS capacitor fabrication, metal shadow mask with circle opening of 100 μm and 200 μm diameters was used. Filament is made of tungsten, was used for heating the Al source up to its vapor temperature. Both filaments and Al sources are made of Nilaco, inc. with material purity of 99.999%.

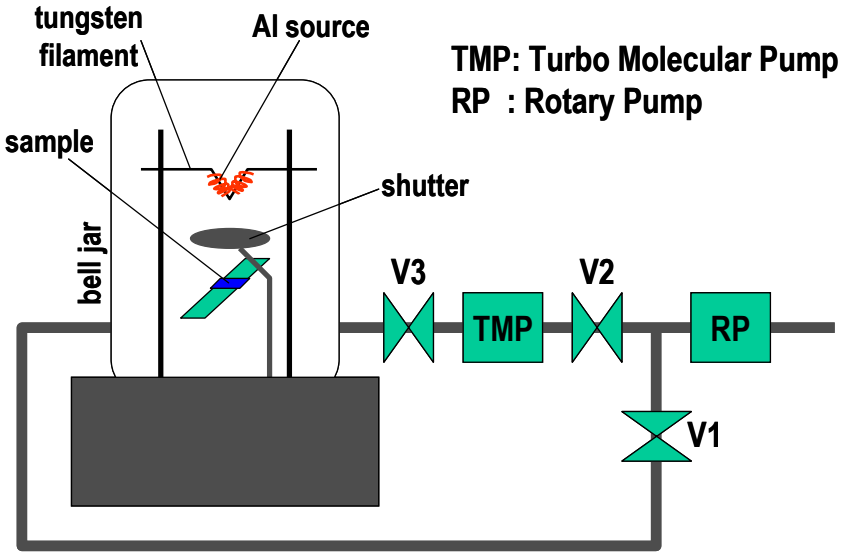

Fig. 3.6 Schematic drawing for vacuum thermal evaporation system. The system is utilized with Turbo Molecular Pump (TMP) to pump down to several 10^{-5} Torr.

The physics of vacuum thermal evaporation is based on thermodynamics of the evaporated materials. There have been experiments performed for evaluating the thermodynamic properties of material. Careful evaluation may reveal that the vapor

pressure of liquid Al is given by the following.

$$\log P_{torr} = \frac{15{,}993}{T} + 12.409 - 0.999 \log T - 3.52 \times 10^{-6} T \quad \textbf{Eq. 3.1}$$

Neglecting the last two terms, the Arrhenius character of log P vs. 1/T can be essentially preserved. Fig. 3.7 presents thermal equilibrium for metal evaporations in form of Arrhenius plots. The dot marks are the metal melting points. Two modes of evaporation can be distinguished in practice, depending whether the vapor effectively emanates from liquid or solid source. Usually, a melt will be required if the element in question does not achieve a vapor pressure greater than 10^{-3} torr at its melting point. Most metals, like Al, Ag, Au, and so on, fall into this category, and effective film deposition is attained only when the source is heated into the liquid phase. On the other hand, elements such as Cr, Ti, Mo, Fe, and Si reach sufficiently high vapor pressures of 10^{-2} torr some 500°C below the melting point.

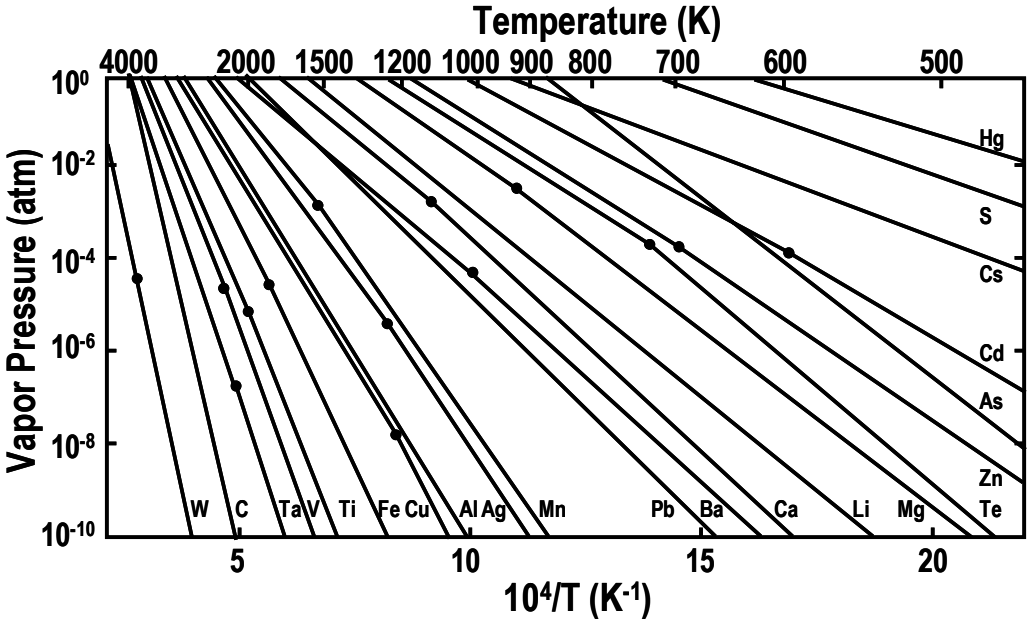

Fig. 3.7 Thermal equilibrium for metal evaporations in form of Arrhenius plots. The dot marks are the metal melting points.

3.2 Characterization Method of La_2O_3 Gate Insulator

Characterization methods of physical and electrical properties of La_2O_3 thin films are explained in this subsection.

3.2.1 Spectroscopic Ellipsometry

Spectroscopic ellipsometry technique is frequently used to estimate the optical thickness of La_2O_3 thin films. Fig. 3.8 shows conception for measuring optical thickness of thin film with spectroscopic ellipsometry. The polarized incident light is illuminated into the sample at the angle Φ_0 of 70^o. Afterward, the reflected light is polarized once again to detect the elliptic angle Ψ and the phase difference Δ. The film thickness is obtained from the fitting parameter of n-Cauchy model calculation. The best fitting result of the elliptic angle Ψ and phase difference Δ of various light wavelength λ may give a reliable optical thickness.

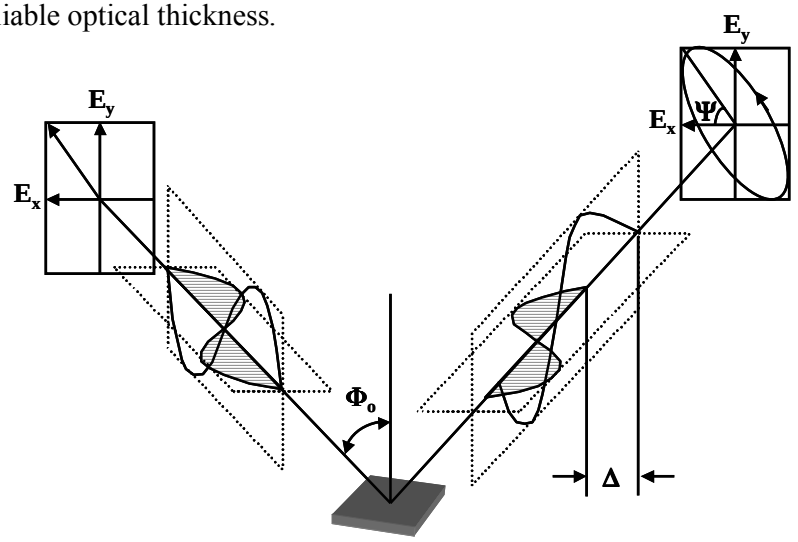

Fig. 3.8 Conception for measuring optical thickness of thin film with spectroscopic ellipsometry.

3.2.2 Transmission Electron Microscopy (TEM)

Cross-sectional TEM (Transmission Electron Microscopy) is often used to observe the physical thickness or the thin film's morphology. It is compatible for observing nano regime structure, as image resolution as high as 0.2-0.3 nm can be reached by TEM. Fig. 3.9 illustrates schematic diagram for TEM observation. The principle is pretty similar to optical microscope since several magnetic lenses are used to magnify the object image. To penetrate the electron beam, sample as thin as 5-500 nm is. Interaction of electron beam with atomic arrangement in sample may produce interference pattern in transmitted electron beam. High-resolution image can be obtained from imaging the magnified transmitted electron beam.

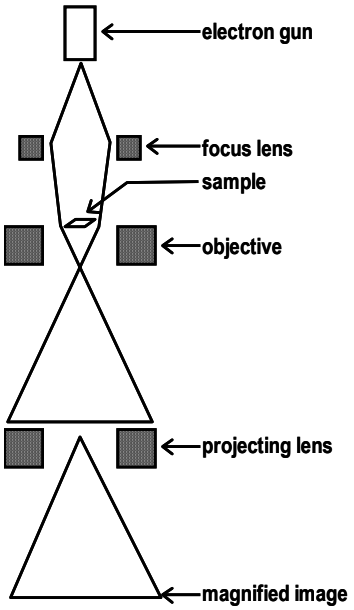

Fig. 3.9 A schematic diagram for TEM (Transmission Electron Microscopy) observation. Several magnetic lenses are used to magnify the object image.

3.3 Measurement Technique of Low-Frequency Noise

The noise signals of high quality devices are usually very small. To measure such signals, nearly noiseless and high sensitivity appliances are highly required. Fig. 3.10 shows schematic diagram for 1/*f* noise measurement system. The grounding is very important to reject the outside signal interferences. Since long and very long wave radio frequencies, it is recommended to measure the low frequency noise under a shielded-chamber. The 1/*f* noise measurement system is utilized with several equipments, i.e., DC monitor, low-noise DC source, signal analyzer, low-noise amplifier, wafer probe, 1/*f* noise interface unit, and ground unit. The first tree equipments are automatically controlled with Personal Computer (PC) via *GPIB* network interface. 1/*f* noise measurement program running under Agilent VEE (Visual Engineering Environment) software is used to manipulate the complexity of noise measurements.

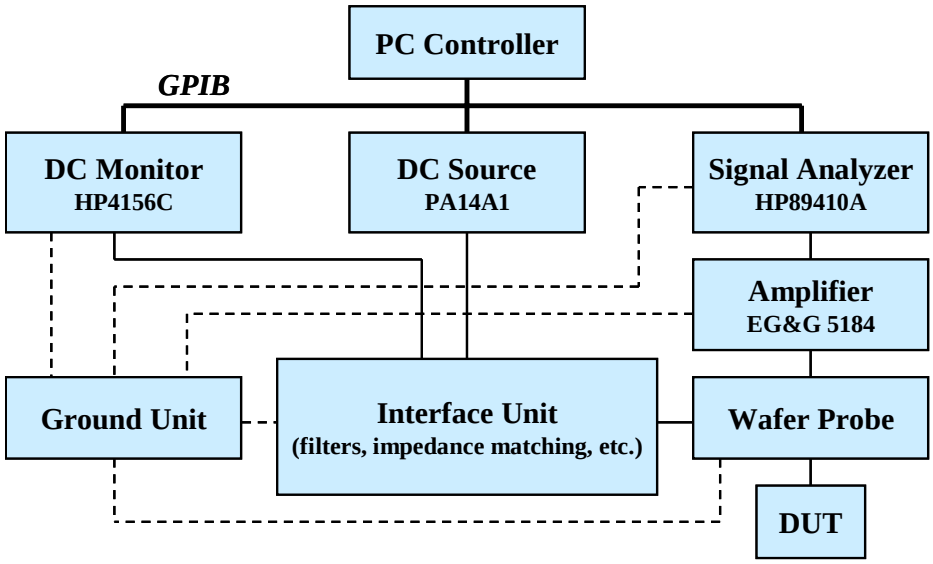

Fig. 3.10 Diagram for 1/*f* noise measurement system. As the noise signal is usually very small, nearly noiseless and high sensitivity appliances are in used. Grounding is important to reject the outside signal interferences.

3.3.1 Vector Signal Analyzer

The noise power density of the device under test (DUT) is measured and analyzed with signal analyzer. In this experiment, we use Agilent HP89410A vector signal analyzer (VSA) as its photograph shown Fig. 3.11. To measure the noise signal, this equipment modulates signal in vector forms. We may measure noise signal as low as –160 dBv = 10 nVrms at 1kHz directly without pre-amplifier by setting the sensitivity of this equipment into the highest level. This equipment supports signal measurements over DC to 10 MHz frequency range, however, the 1/*f* noise measurement system allows 10 Hz to 10 MHz for measurement without pre-amplifier or 10 Hz to 100 kHz for measurement with amplifier.

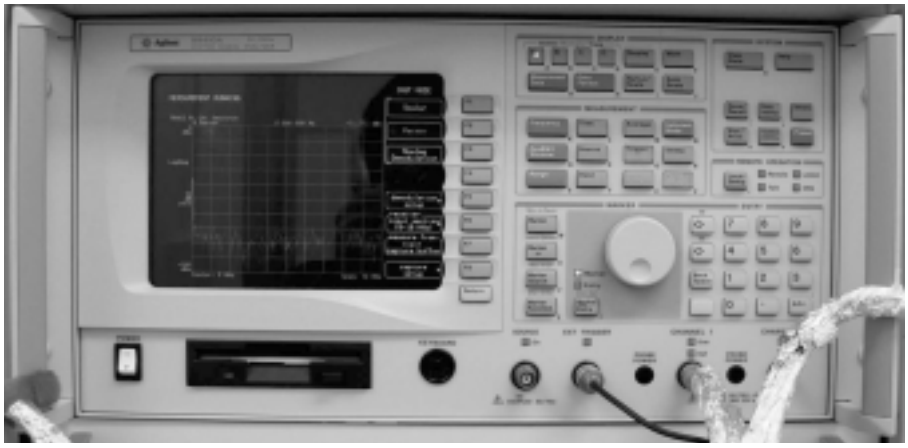

Fig. 3.11 High sensitivity Agilent HP89410A vector signal analyzer (VSA).

3.3.2 Ultra-Low Noise DC Source

In 1/*f* noise measurements, DUT must be operated properly by DC biasing. Shibasoku PA14A1 ultra-low noise DC source shown in Fig. 3.11 is used in this experiment to satisfy the requirements. This equipment is accommodated with 2 channels with sufficiently low enough noise, i.e., CH 1: -126 dBv = 0.5 μVrms and CH 2: -132 dBv = 0.5 μVrms at 1 kHz. Furthermore, these noise levels can be suppressed with RC Low-Pass (LP) filters that is utilized inside the 1/*f* noise interface unit. In case of nMISFET device, it is recommended to use CH 1 for biasing the gate and CH 2 for the drain, since the CH 2 has a half lower than CH 1 in noise power and the 1/*f* noise signal measured from the drain terminal. It is noted that PA14A1 DC source can not inverse its polarity and it should be done manually through the interface unit.

Fig. 3.12 Shibasoku PA14A1 ultra-low noise DC source photograph.

3.3.3 Ultra-Low Noise Pre-Amplifier

It is difficult to measure 1/*f* noise of high quality devices, since they have very low noise signals. To facilitate measurement of a very low noise, high gain ultra-low noise pre-amplifier is required to increase the measurement sensitivity. In this system, Pelkin Elmer EG&G 5184 ultra-low noise pre-amplifier is used to obtain noise floor as low as –178 dBv = 1.2 nVrms at 1 kHz as shown in Fig 3.13. This noise floor can be measured by shorting the pre-amplifier input with 50 Ω terminal stubs. As this equipment has flat gain of 60 dB along frequency range of 3 Hz to 300 kHz, it covers the supported frequency range of 10 Hz to 100 kHz of noise measurement. This pre-amplifier can be powered with either AC line or dry cell batteries. It is recommended to unplug the connector to the AC line, since it directly couple the AC line signal to the system.

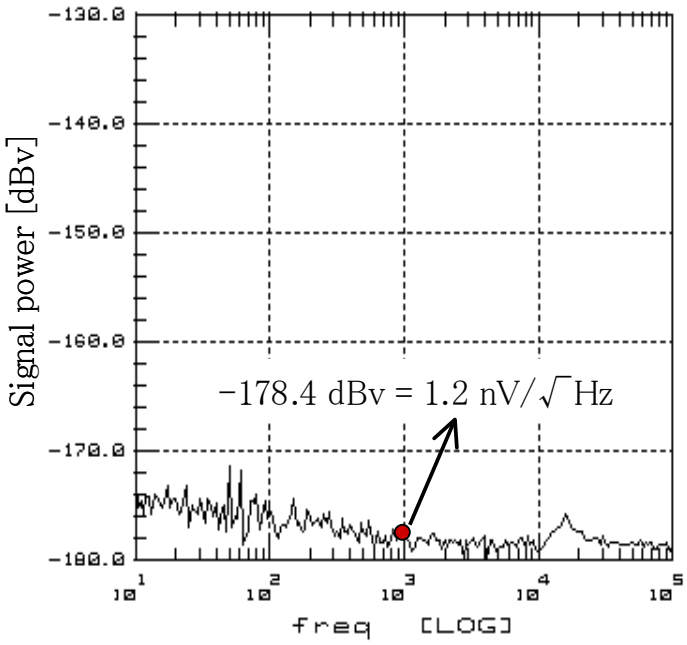

Fig. 3.13 Noise floor of the 1/*f* noise measurement system after utilized by EG&G 5184 ultra-low noise pre-amplifier.

3.3.4 DC Source Monitor

Before 1/*f* noise measurement, the device DC characteristics, such as transconductance, input and output resistance, must be measured for setting the expected bias of PA141A and for calculating or converting input reference noise power. Agilent 4156C semiconductor parameter analyzer is used in this system. Long, medium and short integration are available depending on the measured current value. It is recommended to use long or medium for bias setting of the order of nA.

3.3.5 1/*f* Noise Interface Unit, Battery Unit and Ground Unit

1/*f* noise interface unit is specifically designed to coordinate and assist all of equipments to be practical for 1/*f* noise measurement. It contains low-pass filters, load impedances, impedance matching, switching, and substrate bias controller. Most of cable connectors are using triaxial BNC to isolate the signals. The substrate bias can be applied with rechargeable battery unit controlled with high precision variable resistors. The photograph of 1/*f* noise interface unit, battery unit and ground unit is shown in Fig. 3.14.

Fig. 3.14 Photograph of 1/*f* noise interface unit, battery unit and ground unit.

3.4 Fabrication Method of Ultra-Shallow p^+/n Junctions

In this subsection, we discuss the fabrication process for ultra-shallow p^+/n junctions.

3.4.1 Device Fabrication Procedure

Top view micrograph of p^+/n junction with device area of 220μm×220μm and device fabrication flow chart is depicted in Fig. 3.15. Moreover, cross-sectional description of p^+/n junction fabrication process is illustrated in Fig. 3.16. Device fabrication is beginning with plasma doping process and electrical activation annealing of 8 inches bare silicon wafers. The sample is cut into about 2 cm × 2 cm. The first lithography processes are for defining the junction device area. Post-baking is brought at higher temperature of 120^{o}C. It is performed make the photo resist to have higher endurance against fluoride nitric acid etchant. Hydrogen fluoride (HF), nitric acid (HNO_2), and DI water with composition of HF: HNO_2: H_2O = 1:1:2 in volume are used for etching silicon that is uncovered by photo resist. The second lithography process is done for defining the metal PAD region. After the Al metal deposition with vacuum thermal evaporation, PAD area is formed with lift-off process under acetone solution. Lastly, after taking native oxide in the back surface, back metal electrode is deposited once again with bell jar Al metal evaporator.

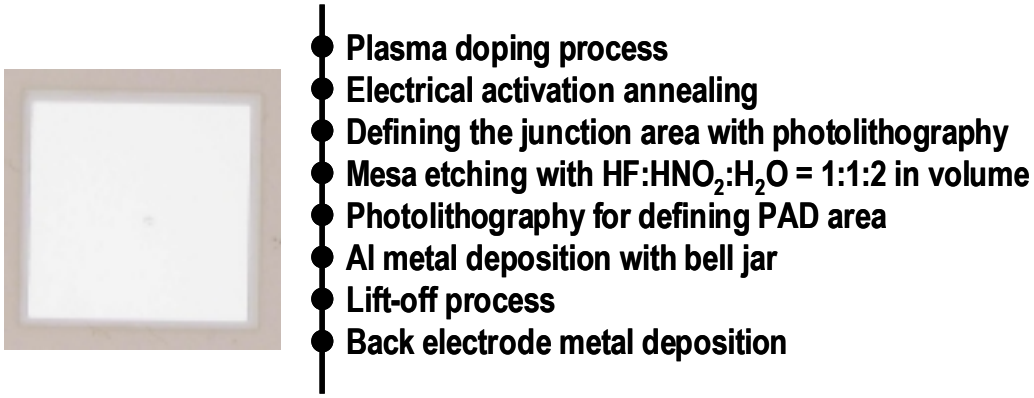

Fig. 3.15 Top view micrograph of p^+/n junction with device area of 220 μm × 220 μm and device fabrication flow chart.

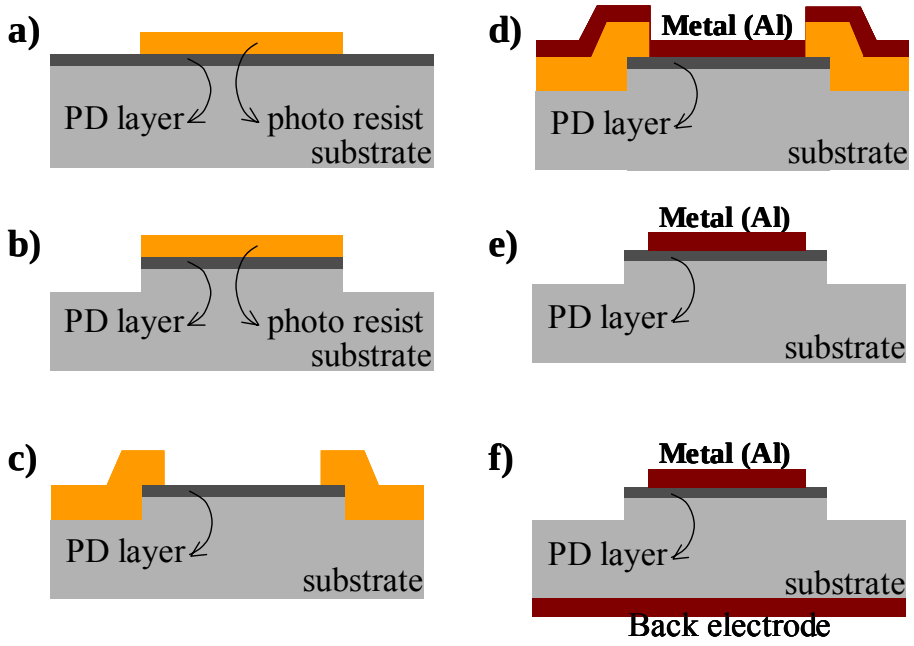

Fig. 3.16 Cross-sectional description of p^+/n junction fabrication process.

3.4.2 Plasma Doping Method

Plasma doping technique is different from ion implantation. Simplification like omitting the intermediate stages of ion source, beam extraction, focusing and scanning,

make plasma doping compatible for mass doping. The gas source is immersed in plasma environment into radicals, ions, or neutrals. Charge particles like ions can be accelerated in direction to the target wafer by means of a series of pulsed negative high-voltage.

Photograph of plasma doping system and schematic diagram illustrating general conception of doping mechanism is depicted in Fig. 3.17. Two chambers (i.e., loading chamber and process chamber) and two high voltage RF-power supplies (i.e., for source and for acceleration bias) and Langmuir probe for measuring plasma distribution are utilized in the system. Helicon source give the system to have low-pressure and high-density plasma source. The process chamber is accommodated with turbo molecular pump with background pressure of 10^{-5} Pa. The doping process is carried out at pressure of 0.1 to 2.5 Pa. Several gases like helium (He), argon (Ar), neon (Ne), and diborane (B_2H_6) are available to be plasma targets in the process chamber.

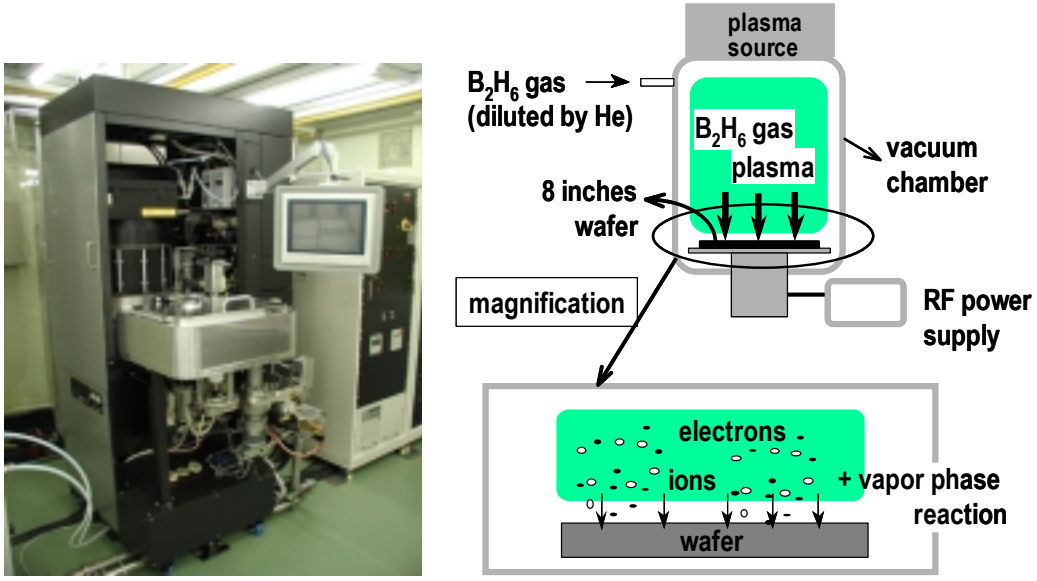

Fig. 3.17 Photograph of plasma doping system and schematic diagram illustrating general conception of doping mechanism.

3.4.3 Impurity Electrical Activation

The impurity electrical activation is usually performed with annealing at high temperature for a very short time to avoid impurity diffusion into the deeper location. USJ are formed by high dose ultra-shallow doping method followed by nearly diffusion less annealing method. Plasma doping combined with millisecond annealing like Flash Lamp Annealing (FLA) or non-melt Laser Annealing (LA) appears to be the most likely alternatives for sub-10-nm USJ formations.

3.5 Characterization of Ultra-Shallow Junctions

In this subsection, we explain the physical and electrical characterization method for ultra-shallow junction.

3.5.1 Sheet Resistance Measurements

In ultra-shallow junction, formation of shallower junction depth with lower sheet resistance is the main obstacle. There are many ways on measuring sheet resistance of a layer range from permanent contact, temporary contact to contactless techniques. For a semiconductor with resistivity ρ, the resistivity is defined by

$$\rho = \frac{1}{q\left(n\mu_n + p\mu_p\right)} \qquad \textbf{Eq. 3.2}$$

where n and p are the free electron and hole concentrations, and μ_n and μ_p are the electron and the hole mobilities, respectively. The sheet resistance is defined by

$$R_s = \frac{\rho}{t} \qquad \textbf{Eq. 3.3}$$

where t is the layer thickness. The simplest way on measuring sheet resistance is by two-point probe (2pp) method. However, this technique is suffering from the contact resistance R_c at each metal probe/material contact and from the spreading resistance R_{sp} under each probe. Hence, it is difficult to obtain the correct sheet resistance value with two-point probe.

The contact resistance R_c and spreading resistance R_{sp} can be eliminated with four-point probe (4pp) method. Fig. 3.18 shows schematic drawing for sheet resistance measurement with four point probes. The spaces among the probes are 1 mm. The

photograph of four-point probe instrument is given in Fig. 3.19. An appropriate weight of 50 ~ 150 grams are used to make punch through to the native oxides. This technique assumes that the sample is infinite in lateral area. For finite sample, geometrical correction factor must be applied to obtain the correct result. Fig. 3.20 depicts the correction factor for measurement of resistivity using four-point probe.

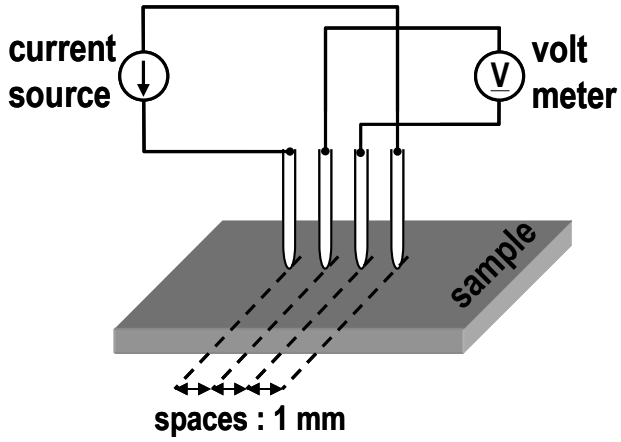

Fig. 3.18 Schematic drawing for sheet resistance measurement with four point probes. Spaces among the probes are 1 mm.

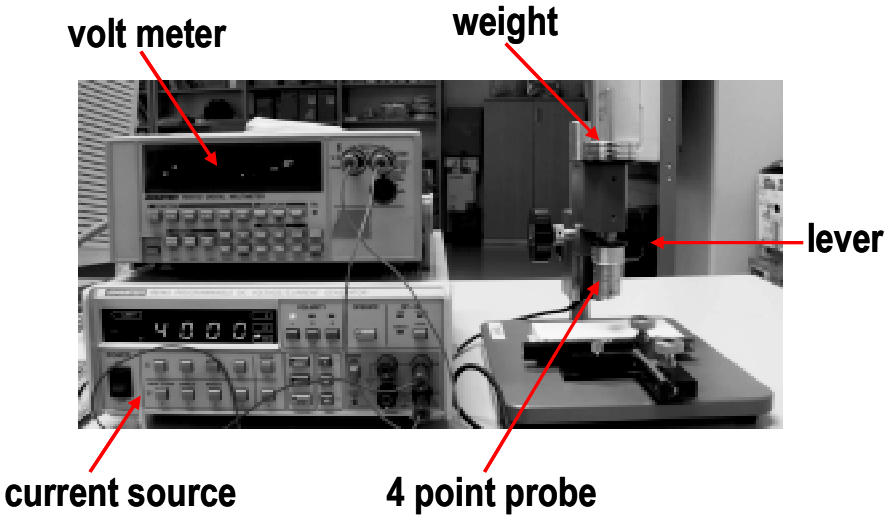

Fig. 3.19 Photograph of four-point probe instrument. An appropriate weight of 50 ~ 150 grams are used to make punch through to the native oxides.

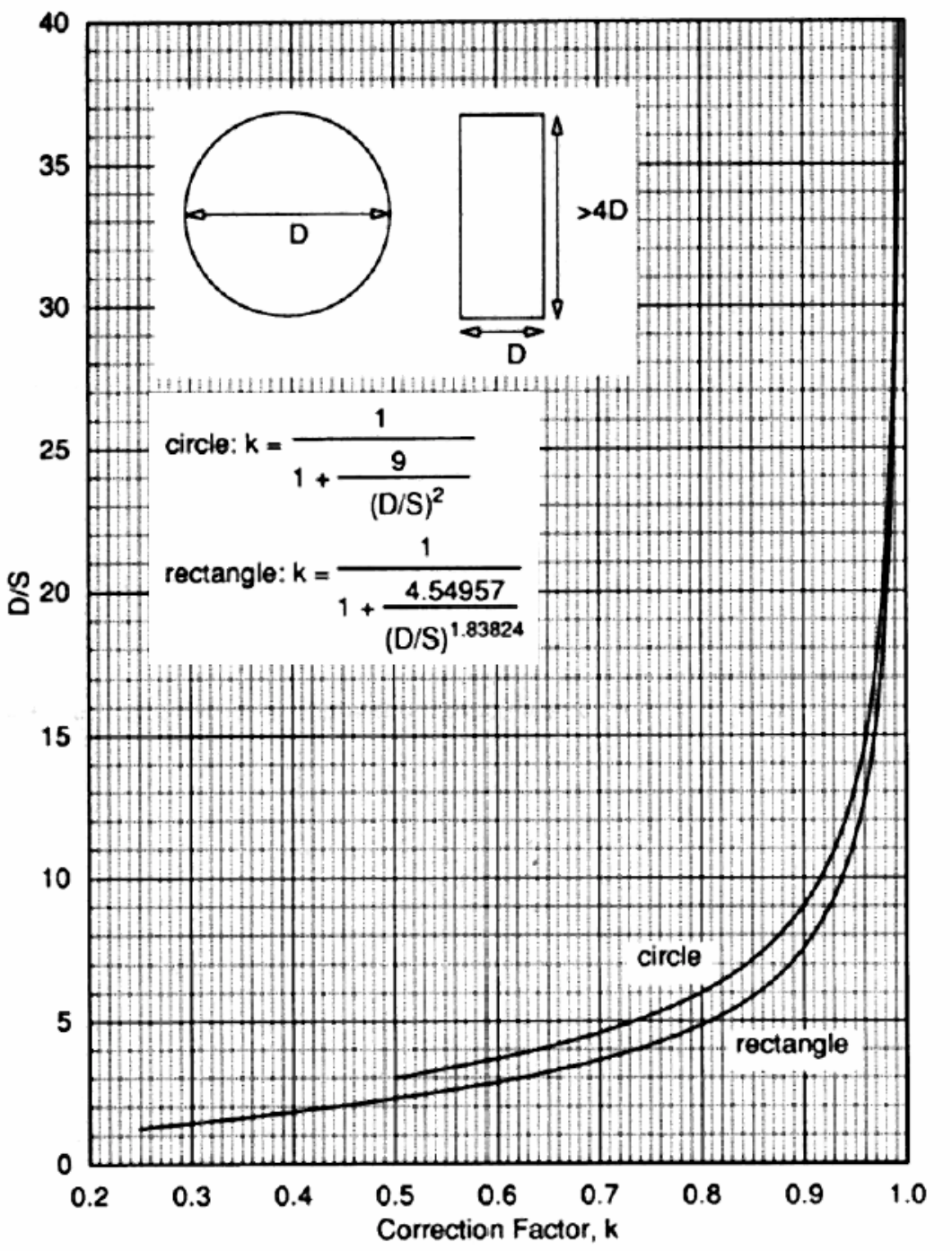

Fig. 3.20 Correction factor for measurement of resistivity using four-point probe.

3.5.2 Secondary Ion Mass Spectrometry (SIMS)

Fig. 3.21 shows measurement for analyzing element compositions, depth profiles, and surface properties with Secondary Ion Mass Spectroscopy (SIMS). This technique is limited to element detection and capable for analyzing most of elements, isotopes or molecular species. As shown in the figure, the basically SIMS measurement is destructive. It is bombarding the sample with primary ions (i.e., Ar^+, O_2^+, Cs^+, and so on), the sputtered secondary ions are detected with energy analyzed and separated with mass spectrometer.

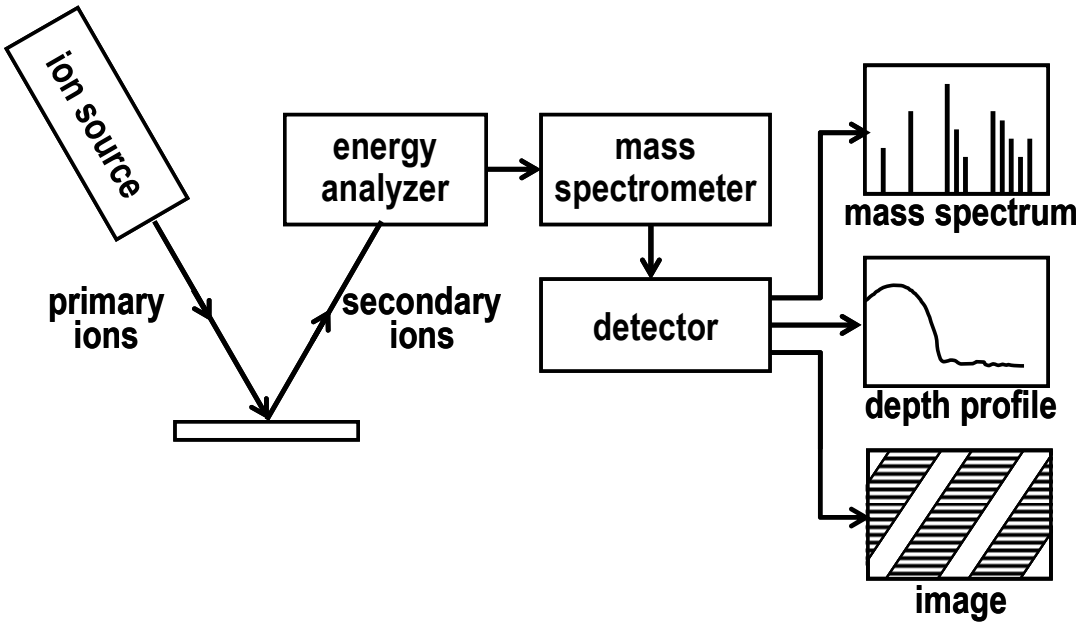

Fig. 3.21 Measurement for analyzing element compositions, depth profiles, surface properties with Secondary Ion Mass Spectroscopy (SIMS).

3.5.3 Atomic Force Microscopy (AFM)

Schematic diagram for surface morphology observation with Atomic Force Microscopy (AFM) is shown in Fig. 3.22. In this experiment, tapping mode AFM observation is performed with Nano Scope 3 from Digital Instrument, co. ltd. In tapping mode AFM, the cantilever probe is vibrated at its resonance frequency, and scanned through the sample surface. The distortion is detected with deflection of the reflected angle of laser beams. While keeping the distance to the sample constant, the cantilever probe is scanned to in x-y directions. The surface morphology is three dimensionally imaged with computer.

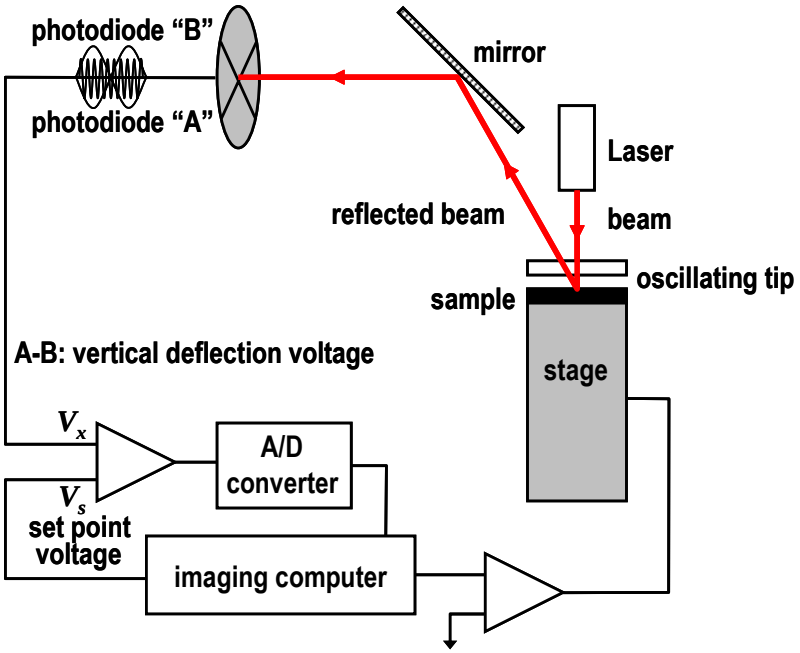

Fig. 3.22 A schematic diagram for surface morphology observation with Atomic Force Microscopy (AFM). The surface morphology is three dimensionally imaged with computer.

3.5.4 Electrical Characterization

Leakage current in p^+/n junctions has strong dependencies in temperature. The activation energy of generation caused by deep traps or diffusion current caused by recombination in neutral regions can be separated with temperature dependence *I-V* measurements. Fig. 3.23 shows photographs for wafer probes and stage temperature controller. Wafer measurements at temperature -40°C to 150°C are enabled with Temptronic temperature controller. For electrical measurement below room temperature, purging with air is needed to blow out the water moisture. The *I-V* characteristic is measured with Agilent 4156C semiconductor parameter analyzer, while the reverse-bias *C-V* characteristic is measured with Agilent 4284A multi-frequency LCR meter.

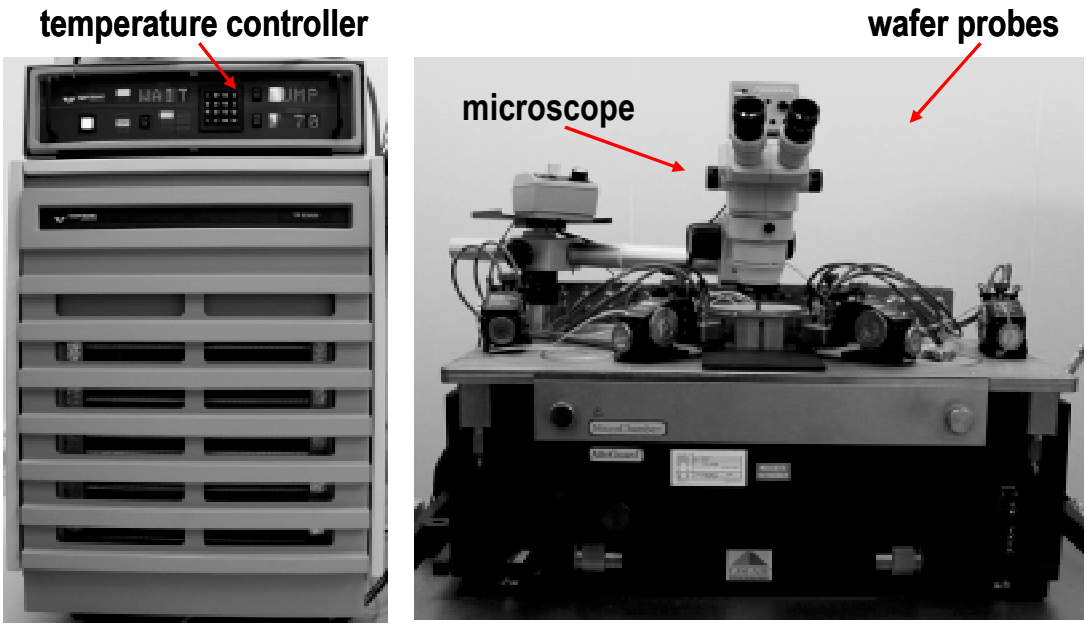

Fig. 3.23 Photographs for wafer probes and stage temperature controller. Wafer measurements at temperature -40°C to 150°C are enabled with Temptronic temperature controller.

Chapter 4. Low-Frequency Noise of La_2O_3 Gate Insulated NMISFET

Low-frequency noise in MOSFET is usually in form of $1/f^{\gamma}$ noise with $0.8 < \gamma < 1.2$ so as it is called "$1/f$ noise". $1/f$ noise is an important parameter in analog or mixed-signals design, as excess in this kind of noise may limit the device performances and functionalities. In high frequency (HF) applications, the $1/f$ noise spectrum is up converted to give rise to phase noise in oscillator, mixer, or modulator. It is difficult to obtain low power with high precision frequency by noisy ($1/f$ noise) active device, as higher Q value is needed. On the other hand, in device process fabrication, $1/f$ noise is useful to analyze or control of the silicon-insulator interface quality. In this chapter, we discuss the measurement and analytical results of La_2O_3 gate insulated NMISFET.

4.1 Measurement Technique of the Low-Frequency Noise

Fig. 4.1 depicts the equivalent circuit of the $1/f$ noise measurement system. The Device-Under-Test (DUT) is biased with two channels low noise DC source. The bias currents or voltages are filtered with RC low-pass filters to reject the interference noises coming from DC source. The current noises in MOSFET's channel influence the drain voltage fluctuations. As the drain noise signals are very small, the signals must be amplified properly. In this experiment, a typical 60 dB ultra low noise a pre-amplifier power-supplied by batteries is used. The amplified noise signals are measured and

analyzed with vector signal analyzer (VSA). Performing measurements under a shielded chamber is highly recommended, as much of interferences from long wave radio frequency can be reduced.

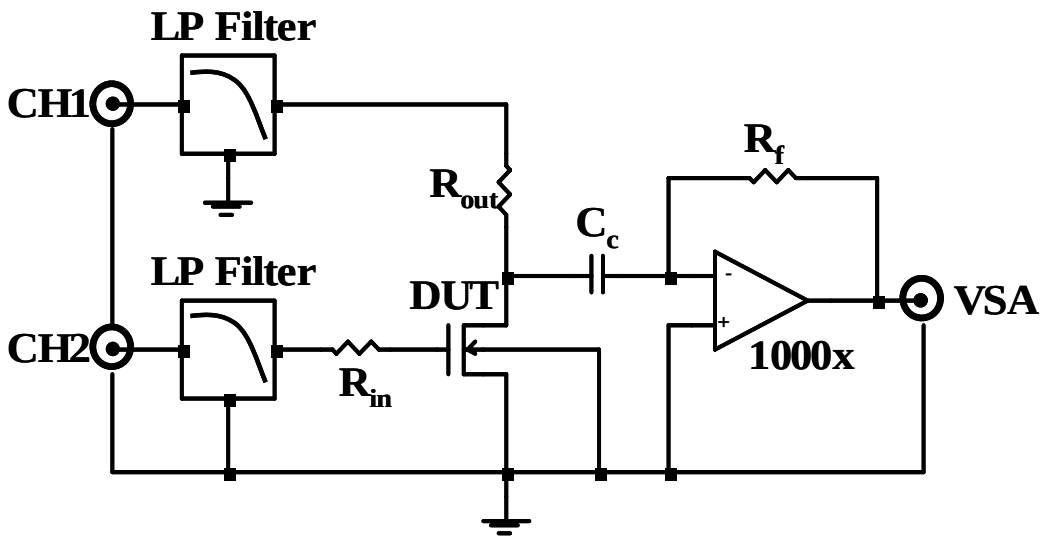

Fig. 4.1 Equivalent circuit of 1/*f* noise measurement systems. RC low-pass filters are applied to reject noises coming from the DC source. The drain noise signals are amplified with a 60 dB pre-amplifier before measuring them with vector signal analyzer (VSA).

4.2 La_2O_3 Films Morphology

In this experiment, La_2O_3 thin film was deposited with e-beam evaporator at 250^oC over chemical oxide surface treated Si substrate. Fig. 4.2 shows the cross-sectional TEM photograph of Al/La_2O_3/Si MIS capacitor. The La_2O_3 film is in the form of amorphous with good silicon interface after post deposition annealing in O_2 ambient at 400^oC for 5 min. The physical thickness is about 3 nm.

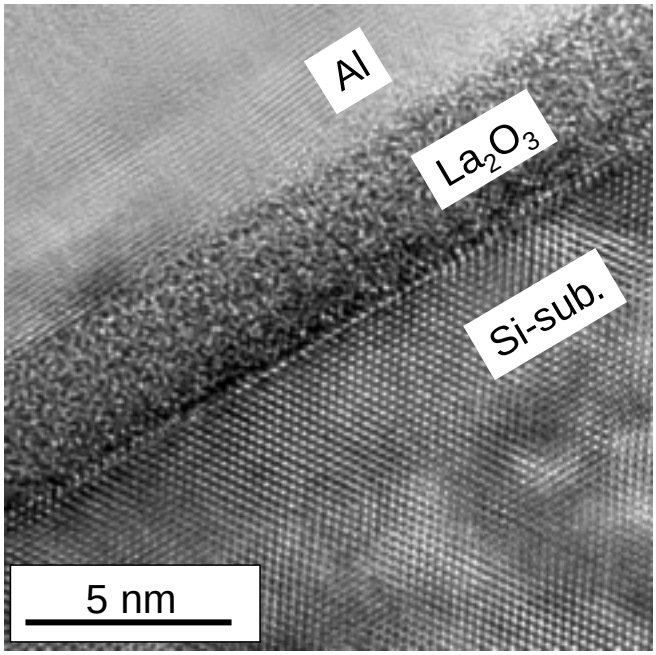

Fig. 4.2 The cross-sectional TEM photograph of Al/La_2O_3/Si MIS capacitor. The La_2O_3 physical thickness of about 3 nm and a good silicon interface were obtained after post deposition annealing in O_2 ambient at 400^{o}C for 5 min.

4.3 *C-V* and *J-V* Characteristics of La_2O_3 MIS Capacitor

The performances of high-κ gate dielectrics films are described by their *C-V* and *J-V* characteristics. Parameters like equivalent oxide thickness (EOT), flatband voltage or flatband shift, surface potential, *etc.* can be obtained by fitting the measured *C-V* with MIS capacitor *C-V* model. Fig 4.3 provides the *C-V* characteristics of t_{ox} ~ 3 nm Al/La_2O_3/Si MIS capacitor. Significant negative flatband shift of 1 V caused by positive fixed charge in insulator and small hysteresis of less than 100 mV was observed. The fitting result with NCSU software by taking account of quantum effect gives EOT of 1.1

nm. Relation between the physical thickness t_{ox} and EOT can be given as the following.

$$\frac{\varepsilon_{high-\kappa}}{t_{ox}} = \frac{\varepsilon_{SiO_2}}{EOT} \qquad \textbf{Eq. 4.1}$$

Where, $\varepsilon_{high-\kappa}$ and ε_{SiO2} is dielectric constant of high-κ and SiO_2, respectively. As a result, by assuming the dielectric constant of SiO_2 is 3.9, the dielectric constant of La_2O_3 thin film of 10.6 can be calculated with the Eq 4.1 above. The calculated fix charge Q_{fix} from flatband shift is around 2×10^{13} $eV^{-1}cm^{-2}$. Assuming the fix charge distributed in uniformly in the insulator, we obtain charge density of 6.5×10^{13} $eV^{-1}cm^{-3}$.

The *J-V* characteristic of t_{ox} ~ 3 nm Al/La_2O_3/Si MIS capacitor is given in Fig 4.4. From Fig 4.4, it is clear that La_2O_3 with EOT as low as 1.1 nm has low leakage current density of 9×10^{-2} A/cm^{-2} at +1 V. This result is comparable to Zr-silicate or Alumina (Al_2O_3) as plotted in Fig 1.7 in Chapter 1.

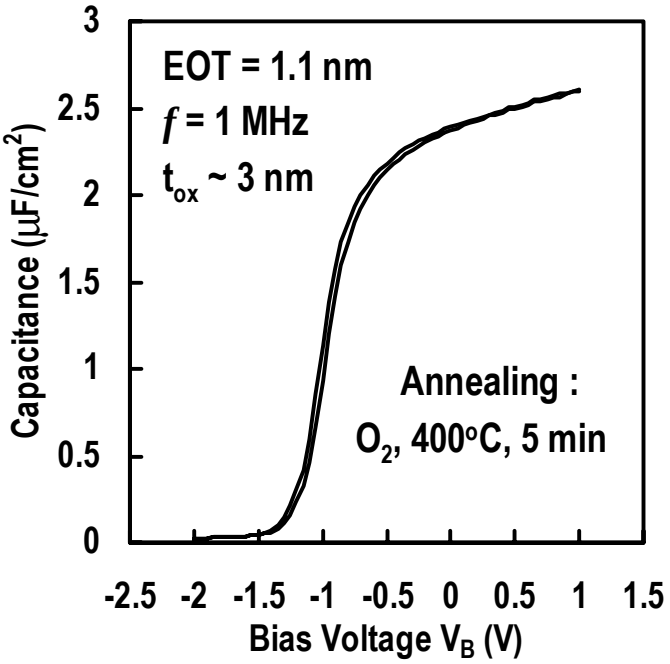

Fig. 4.3 The *C-V* characteristics of t_{ox} ~ 3 nm Al/La_2O_3/Si MIS capacitor. Significant negative flatband shift of ~1 V caused by positive fixed charge in insulator and small hysteresis of less than 100 mV was observed.

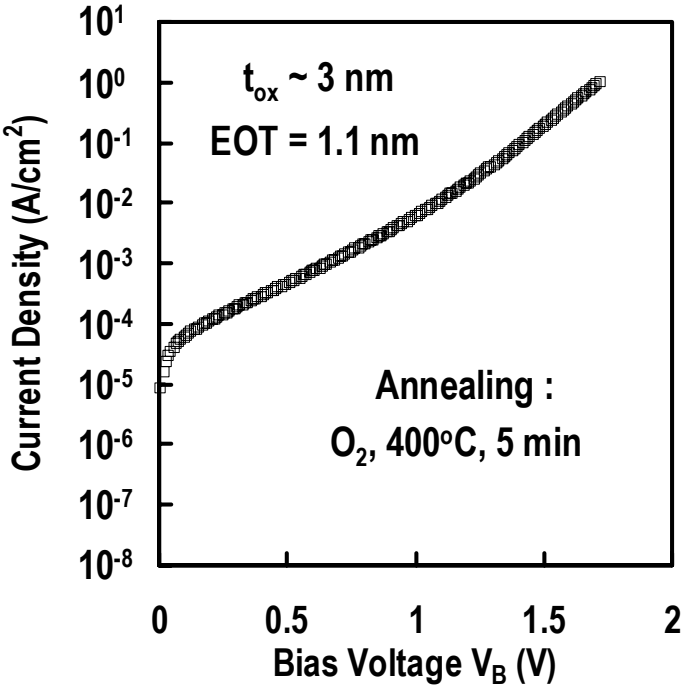

Fig. 4.4 The *J-V* characteristics of t_{ox} ~ 3 nm Al/La_2O_3/Si MIS capacitor. La_2O_3 with EOT of 1.1 nm and leakage current density of 9×10^{-2} A/cm^{-2} at +1 V was obtained.

4.4 DC Characteristics of La_2O_3 NMISFET

In NMISFET fabrication, the La_2O_3 thin film with physical thickness of about 8 nm and EOT of 3 nm is used. The calculated dielectric constant is 10.4, which is of nearly the same value with La_2O_3 thin film used in MIS capacitor. Our purpose of lowering the EOT of gate dielectrics is to give rise to drive current and transconductance for MISFET channel with electrically of the same bias voltage. To evaluate the above properties, DC characterizations like I_d-V_g and I_d-V_d are the most usual technique to be used. Fig. 4.5 illustrates Typical static characteristics of La_2O_3

gate insulated NMISFET with channel area of $W \times L$ = 54 μm×2.5 μm. From the figure, it can be found that La_2O_3 NMISFET with t_{ox} ~ 8 nm shows low subthreshold swing value of 105 mV/dec, high peak transconductance of 400 μS, and good DIBL characteristics as V_d was changed from 0.1 V to 1 V. However, negative subthreshold voltage V_{th} of –0.6 V that gives the transistor to normally on was observed. This is probably caused by excess of positive fixed charge in the thin films.

The I_d-V_d characteristics of $W \times L$ = 54 μm×2.5 μm NMISFET is shown in Fig. 4.6. It shows that high drive current of 110 μA/μm at V_g = 1.2 V and good saturation characteristics with low short channel effects can be obtained with La_2O_3 NMISFET. The normally on transistor as explained in the I_d-V_g above is observed as saturation currents of 20 μA/μm at V_g = 0 V.

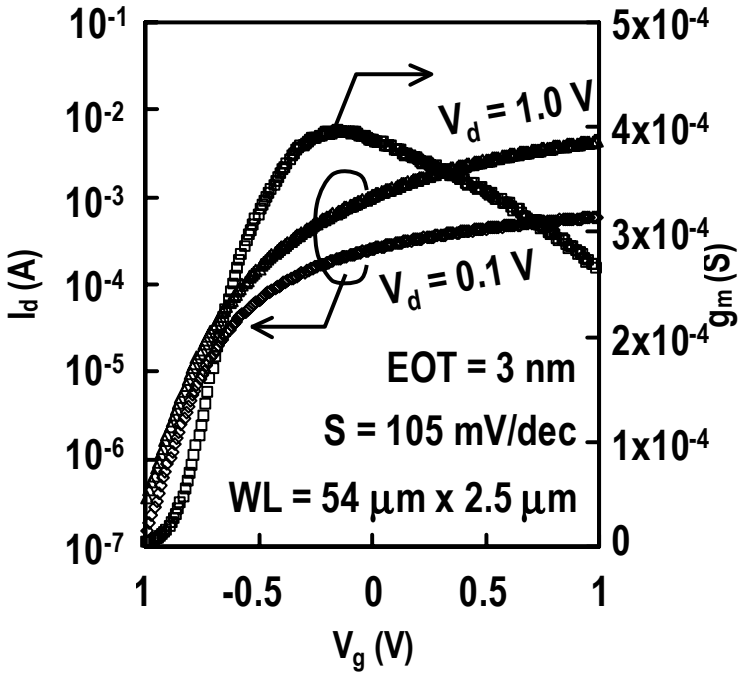

Fig. 4.5 Typical static characteristics of NMISFET with channel area $W \times L$ = 54 μm×2.5 μm. Subthreshold swing value of 105 mV/dec and good DIBL characteristics was obtained with t_{ox} ~ 8 nm La_2O_3 NMISFET.

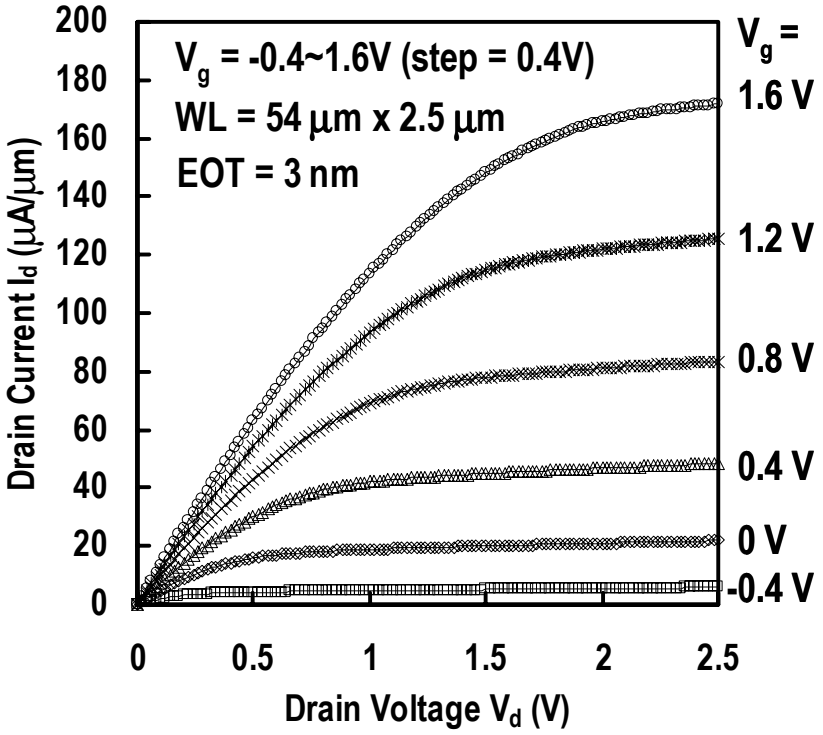

Fig. 4.6 The I_d-V_d characteristics of $W \times L$ = 54 μm×2.5 μm NMISFET. Good drive current and saturation characteristics can be obtained with La_2O_3 gate insulated NMISFET.

4.5 Low-Frequency Characteristics of La_2O_3 NMISFET

There are very few reported results on low-frequency (1/*f*) noise properties of MISFETs with high-k gate dielectrics. Low-frequency noise appears in frequency range of less then 1 MHz. As it spectrum is showing $1/f^{\gamma}$ behavior with $0.8 < \gamma < 1.2$, it is often called 1/*f* noise. In this experiment, the low-frequency noise is measured in frequency range of 10 Hz to 100 kHz.

To interpret the experiment results, we analyze the NMISFET's 1/*f* noise characteristics with standard unified 1/*f* noise model approach. It assumes that 1/*f* noise

is generated from the combination of correlated carrier number and mobility fluctuation (Δn-Δμ) and pure mobility fluctuation (Δμ). Correlated carrier number and mobility fluctuation is modified 1/*f* noise model originated from McWhorter's generation and recombination (GR) noise model. While pure mobility fluctuation is a semi empirical model based on Hooge's 1/*f* noise model.

Pure carrier number fluctuation is a physical model developed by McWhorter for the first time. It explains that fluctuation in drain current is originated from dynamic carrier trapping-detrapping in near silicon-insulator interface traps. In the later, it is modified into correlated carrier number and mobility fluctuations. This modified model takes into account modulation of coulomb scattering induced by trap charges or trapping-detrapping phenomena. From correlated number and mobility fluctuations, the normalized spectral power density of drain current noise S_{id}/I_d^2 can be expressed as the following.

$$\left(\frac{S_{id}}{I_d^2}\right)_{\Delta n-\Delta\mu} = S_{vg}\frac{g_m^2}{I_d^2}\left(1+\alpha_{sc}\mu_{eff}C_{ox}\frac{I_d}{g_m}\right)^2 \qquad \textbf{Eq. 4.2}$$

Where g_m is the device transconductance, μ_{eff} is the effective carrier mobility, C_{ox} is the gate dielectrics capacitance, and α_{sc} is coulomb scattering coefficient. The input-referred spectral power density S_{vg} is described by the following expression.

$$S_{vg} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f^{\gamma}} \qquad \textbf{Eq. 4.3}$$

Where λ is the tunnel attenuation distance (≈0.1 nm), N_t the trap density (in $eV^{-1}cm^{-3}$) of the gate dielectrics at Fermi level energy, k Boltzmann's constant, T the absolute temperature, f the frequency, W the channel width and L the channel length.

The first term in the parenthesis in Eq. 4.2 is the original form of carrier number fluctuation, while the second term accounts for the correlated mobility fluctuation, where its strength is shown by the α_{sc} coefficient.

A part from correlated carrier number and mobility fluctuation, an empirical *1/f* noise model was built up by Hooge, so-called pure mobility fluctuation. According to Hooge's hypothesis, the drain current fluctuation is originated by variation of carrier mobility induced by lattice scattering. The normalized current noise spectral density is illustrated in the following expression.

$$\left(\frac{S_{id}}{I_d^2}\right)_{\Delta\mu} = \frac{q\alpha_H}{WLQ_{inv}f} = \frac{q\alpha_H\mu_{eff}V_d}{fL^2I_d} \qquad \textbf{Eq. 4.4}$$

Where α_H is Hooge's empirical parameter and Q_{inv} is the total inversion charge. The original of Hooge's parameter α_H was a universal constant with value of about 2×10^{-3} for homogeneous samples. However, recent results have shown that the dimensionless α_H may vary several orders of magnitude, depending on the crystalline quality of the materials. A newly refined Hooge's parameter is given as the following equation.

$$\alpha_H = \alpha_{latt}\left(\frac{\mu_{eff}}{\mu_{latt}}\right)^2 \qquad \textbf{Eq. 4.5}$$

Where α_{latt} is Hooge's constant ($\approx2\times10^{-3}$, the original of Hooge's parameter) and μ_{latt} is carrier mobility due to lattice scattering only. Defect less good materials have low α_H value, correspond to low *1/f* noise and vise versa. Values in the range of $\sim10^{-6}$ to $\sim10^{-3}$ have been found for silicon.

At very high current density region, fluctuations due to source-drain access resistance might be accounted. Normalized current noise spectral power density caused

by access resistance fluctuation is given in the following relation.

$$\left(\frac{S_{id}}{I_d^2}\right)_{\Delta R} = \frac{S_R}{R_{sd}^2} = S_R\left(\frac{I_d}{V_d}\right)^2 \qquad \textbf{Eq. 4.6}$$

Where R_{sd} is source-drain series resistance and S_R is resistance power spectral density. The total current noise in MISFET is the summation of the above all fluctuations. As a result, it takes in the following form.

$$\frac{S_{id}}{I_d^2} = \left(\frac{S_{id}}{I_d^2}\right)_{\Delta n-\Delta\mu} + \left(\frac{S_{id}}{I_d^2}\right)_{\Delta\mu} + \left(\frac{S_{id}}{I_d^2}\right)_{\Delta R} \qquad \textbf{Eq. 4.7}$$

The above all fluctuations is usually discriminated with S_{id}/I_d^2-I_d and $(g_m/I_d)^2$-I_d in plots. Pure number fluctuation performs dependency to second order of (g_m/I_d), while correlated mobility fluctuation remote the first and zero order. On one hand, pure mobility fluctuation shows independency to (g_m/I_d). However, it is in the form of I_d^{-1}.

4.5.1 Effect of Biasing to the Noise Power Level

The dynamic characteristics of noise power spectrum is changing depend on the biasing conditions that determine the basic MISFET parameters. The gate voltage V_g defines the number of inversion charge, while the drain voltage V_d allows the number carrier that flow from source to drain. Fig. 4.7 illustrates typical spectrum power density of drain current noise characteristics of $W \times L$ = 54 μm×2.5 μm NMISFET with different drain bias voltages. From the figure, it can be explained that 1/f noise spectrum increases with the drain voltage, and noise saturation are obtained as the transistor switches to saturation region. It can be seen that the noise spectrums perform no specific

humps that related to dominancy of single level generation-recombination noise. Immediate jump of the noise power spectrum in frequency increases with factor 50 Hz is caused by the interference of a certain harmonic of AC line, as several appliances are powered by AC line.

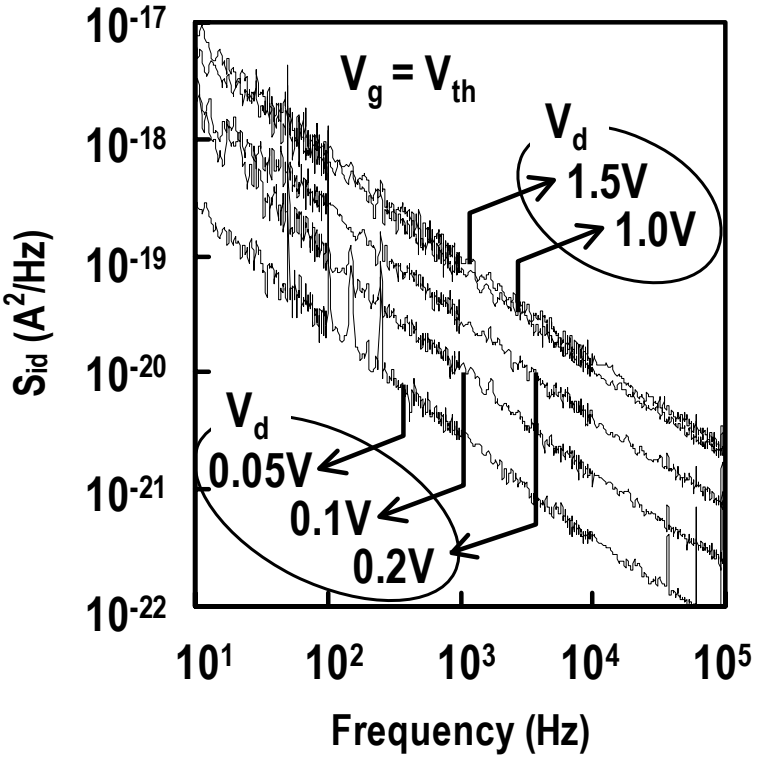

Fig. 4.7 Typical spectrum power density of drain current noise characteristics of $W \times L$ = 54 μm×2.5 μm NMISFET with different drain bias voltages. 1/f noise spectrums show no specific humping and increases as the drain voltage increases.

4.5.2 Frequency Index

According to carrier trapping/detrapping model, frequency index γ of 1/f noise is suspected to the distribution of accessible traps in the insulator. The farther the location

of trap from the surface, the longer the time needed for tunneling. As a result, 1/*f* noise with $\gamma < 1$ shows the dominancy of fast traps or traps with shallower distances from the surface. Then, for 1/*f* noise with $\gamma > 1$, slow traps or traps with deeper distances from the surface will much more dominant.

Fig 4.8 and 4.9 provide the frequency index γ for La_2O_3 and thermal SiO_2 NMISFET, respectively. As depicted in the figures, the frequency indexes tend to increase with the gate voltage V_g-V_{th}, showing that access to traps located in the deeper is dominant as the gate voltage increases. Variation in trap distribution for thermal SiO_2 is smaller than La_2O_3, providing better traps uniformity. A small dip of frequency index in lower gate voltage might be as a result of carrier interaction with high density of interface states that are caused by un-terminated Si dangling bonds.

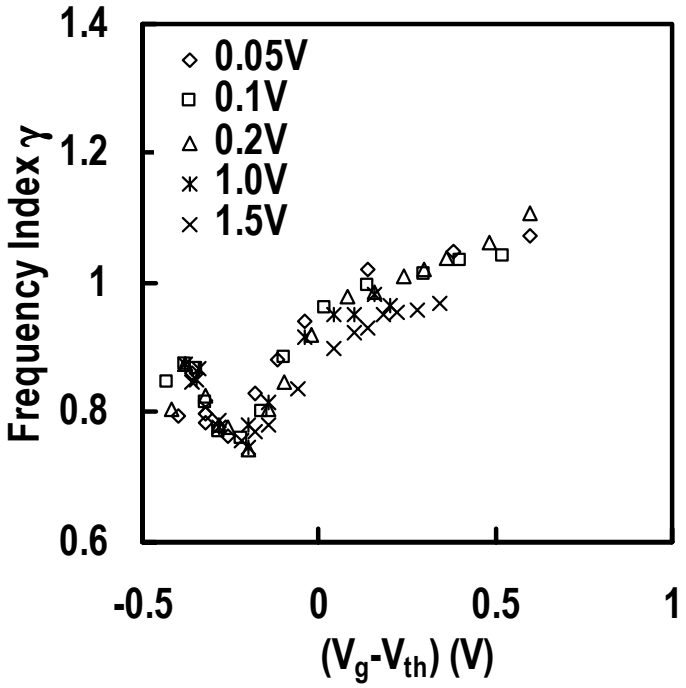

Fig. 4.8 Frequency index γ distribution of for La_2O_3 NMISFET. Small dip in lower gate voltage might be caused by high density of the interface states.

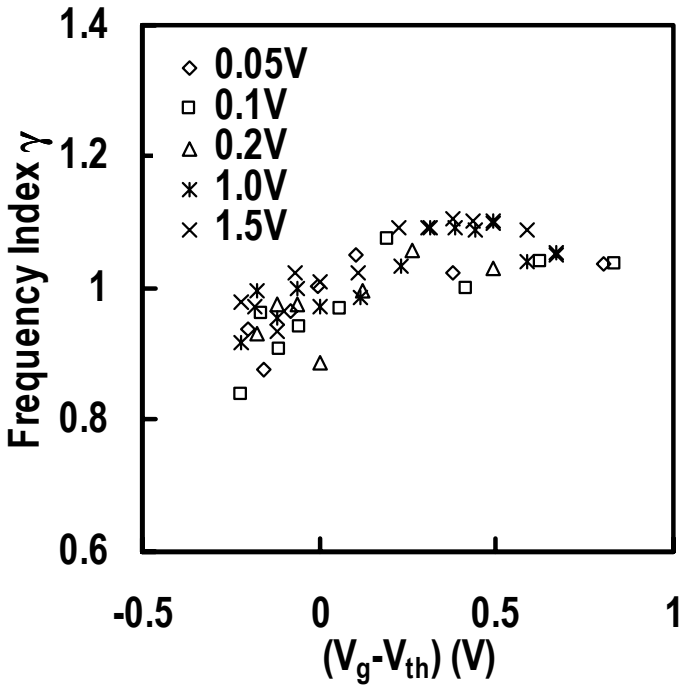

Fig. 4.9 Frequency index as a function of V_g-V_{th} for thermal SiO_2 NMISFET. Thermal SiO_2 performs a good uniformity in trap distribution.

4.5.3 Impact on Channel Length Scaling to the Noise Level

The Impact of channel length scaling to the noise power density of drains current noise in La_2O_3 NMISFETs is depicted in Fig 4.10. The drain current noise power densities S_{id} increase with the channel length scaling; following L^{-3} rule. This is a common phenomenon for NMISFET that can be explained with converting Eq. 4.3 into the following. The transconductance g_m can be obtained with differentiating the drain current equation by the gate voltage as shown in the following.

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{W}{L}\mu_{eff} C_{ox} V_d \qquad \textbf{Eq. 4.8}$$

In split-*CV*, the effective mobility μ_{eff} is measured as following formula.

$$\mu_{eff} = \frac{L}{W}\frac{I_d}{Q_{inv}V_d} \qquad \textbf{Eq. 4.9}$$

From Eq. 4.8 and Eq. 4.9, the inversion charge can be expressed as below.

$$Q_{inv} = C_{ox}\frac{I_d}{g_m} \qquad \textbf{Eq. 4.10}$$

Finally, by substituting Eq. 4.4, Eq. 4.8 and Eq. 4.10 into Eq. 4.2, we can get

$$S_{id} = \frac{q^2 kT\lambda N_t}{f^{\gamma}}\frac{W}{L^3}\mu_{eff}V_d\left(1+\alpha_{sc}\mu_{eff}Q_{inv}\right) \qquad \textbf{Eq. 4.11}$$

According to this equation, when everything else is held constant, it is clear that the noise power density of drain current is proportional to L^{-3}.

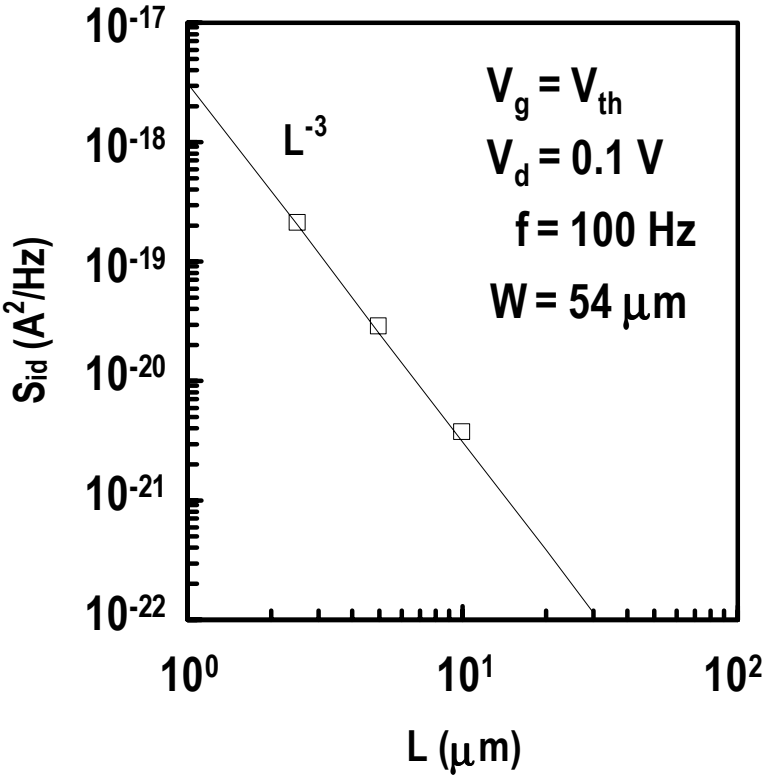

Fig. 4.10 Impact of channel length scaling to the noise power density of drain current noise in La_2O_3 NMISFETs. The noise level follows L^{-3} rule with the channel length scaling.

4.5.4 Access Resistance Noise and Shot Noise

The normalized noise power density of drain current $WL \times S_{id}/I_d^2$ as a function of gate voltage can be found in Fig. 4.11. From the figure, it can be seen that no specific shot noise and access series resistance noise were observed along the measured bias regions. The solid lines are the calculation results from the $1/f$ noise model. The noise levels are decrease with the increasing gate voltage.

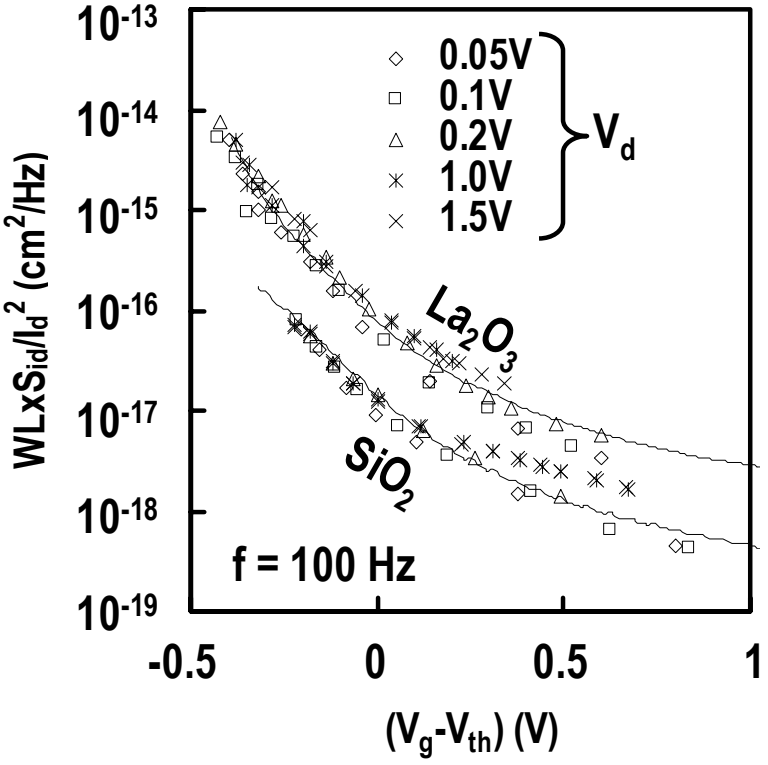

Fig. 4.11 Normalized drain current noise power density $WL \times S_{id}/I_d^2$ as a function of gate voltage. The noise is decreases as the gate voltage increases. No specific shot noise and access series resistance noise were observed at the measured bias regions.

4.5.5 Discrimination to the Mechanism of the Noise

To discriminate the mechanism in low-frequency range, S_{id}/I_d^2-I_d and $(g_m/I_d)^2$-I_d is plotted as shown in Fig. 4.12. The experiment results of normalized drain current noise power density $WL\times S_{id}/I_d^2$ is in symbol marks, normalized square transconductance $g_m^2/I_d^2\times Const.$ ($Const. = q^2kT\lambda N_t/C_{ox}^2 f$) obtained from I_d-V_g is in solid-lines. $WL\times S_{id}/I_d^2$ plots following $g_m^2/I_d^2\times Const.$ curves are noises caused by pure number fluctuation, while plots following the I_d^{-1} curve line are thought to be the mobility fluctuation.

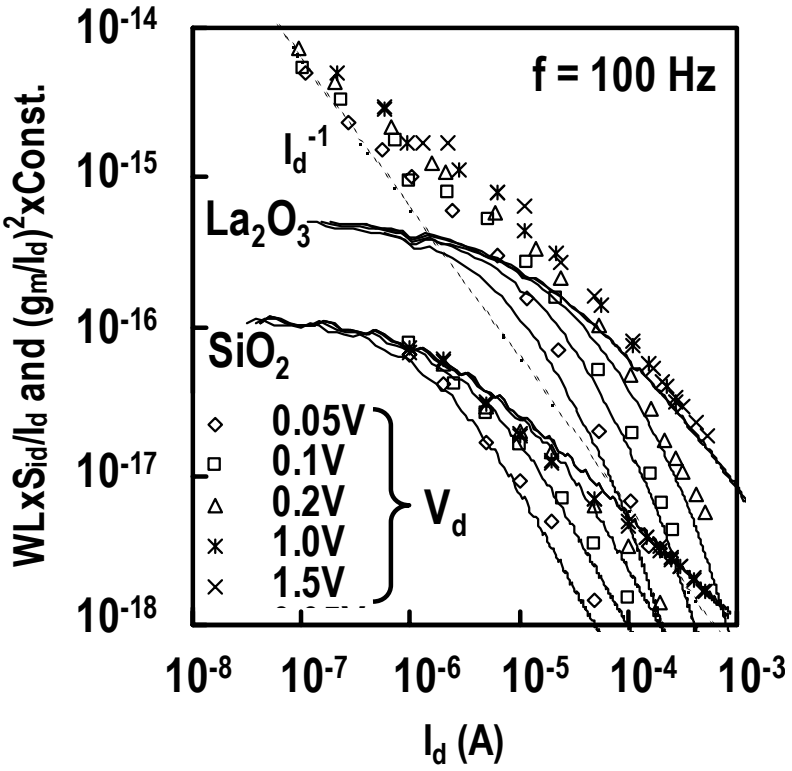

Fig. 4.12 Normalized drain current noise power density $WL\times S_{id}/I_d^2$ (symbols) and normalized square transconductance $g_m^2/I_d^2\times Const.$ (solid-lines) as a function of drain bias current, where $Const. = q^2kT\lambda N_t/C_{ox}^2 f$. Channel mobility fluctuation follows I_d^{-1} rule, while number fluctuation follows normalized square transconductance.

4.5.6 Fitting Results from the Modeled Noise

Fitting results of noise level from unified model low-frequency noise can be found solid lines in Fig. 4.13. This model is based on combined number fluctuation, correlated number – mobility fluctuation and mobility fluctuation models as mention in the above. For calculation, we suggest the trap density of $N_t \sim 4\times10^{19}$ $eV^{-1}cm^{-3}$ for La_2O_3 NMISFET, while for thermal SiO_2 is $N_t \sim 2\times10^{18}$ $eV^{-1}cm^{-3}$. The trap density value for La_2O_3 NMISFET is of the same order of fix charge density obtained from flatband shift. Discrepancy to the exact value might be due to non-uniformity distribution of fixed charge in the film or the precision in fitting calculation.

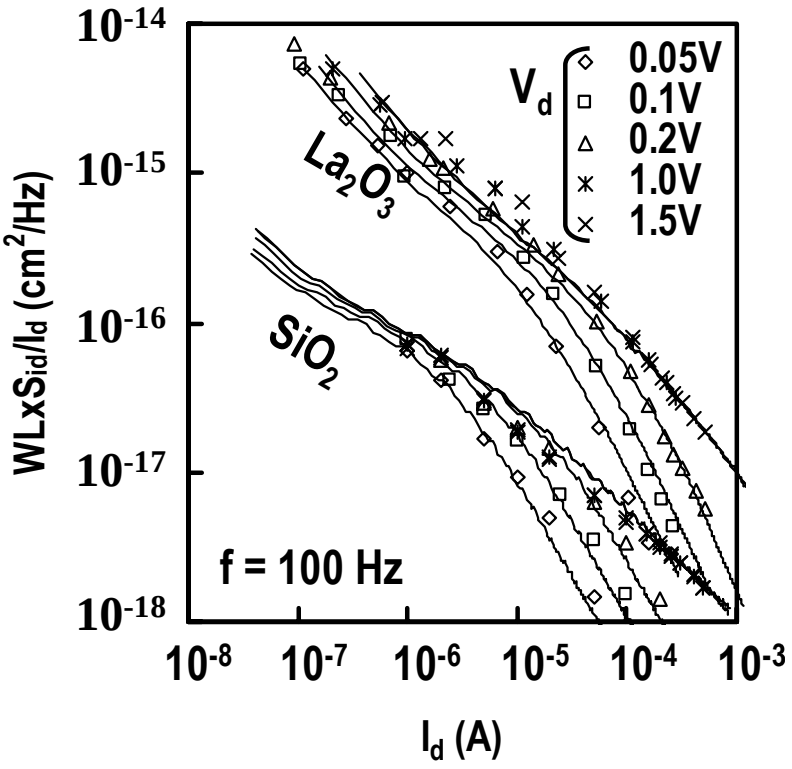

Fig. 4.13 Calculation results (solid-lines) of the low-frequency unified modeled based on combined number fluctuation, correlated number – mobility fluctuation and mobility fluctuation models.

Fig. 4.14 demonstrated the normalized drain current noise level $WL \times S_{id}/I_d^2$ in symbol marks and the calculation results in solid lines plotted as a function of normalized square transconductance $gm^2/I_d^2 \times Const.$ The noise linearity against normalized transconductance near the threshold voltage shows the domination of noise due to carrier trapping /detrapping fluctuations.

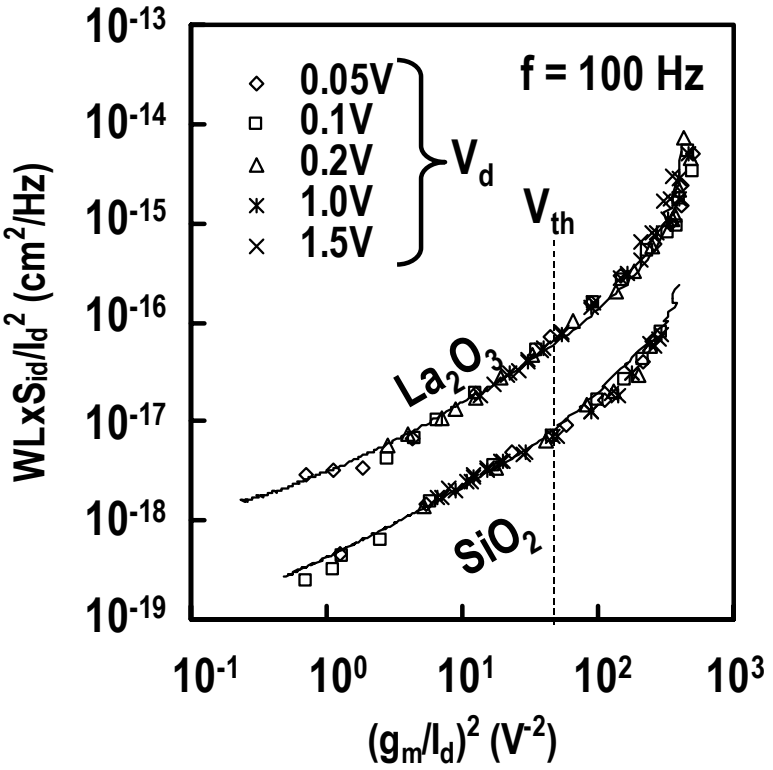

Fig. 4.14 Normalized drain current noise level $WL \times S_{id}/I_d^2$ (symbols) and calculation results (solid lines) as a function of normalized square transconductance $g_m^2/I_d^2 \times$Const. Linearity near the threshold voltage shows the domination of noise due to carrier trapping /detrapping events.

Fig. 4.15 depicts Hooge's empirical parameters α_H obtained from the fitting results of normalized drain current noise level ($WL \times S_{id}/I_d^2$) plotted as a function of drain voltage. As demonstrated in the figure, the dimensionless α_H decreases with drain voltage V_d showing that the carrier feels less phonon scattering as the higher electric field applied. The experiment result gives the apparent α_H value for thermal SiO_2 NMISFET of several 10^{-6} that is of the same value to the reported data. On the other hand, La_2O_3 NMISFET exhibits two orders higher than SiO_2, *i.e.*, several 10^{-4}. This might be due to carrier scattering by higher state densities in Si-La_2O_3 interface.

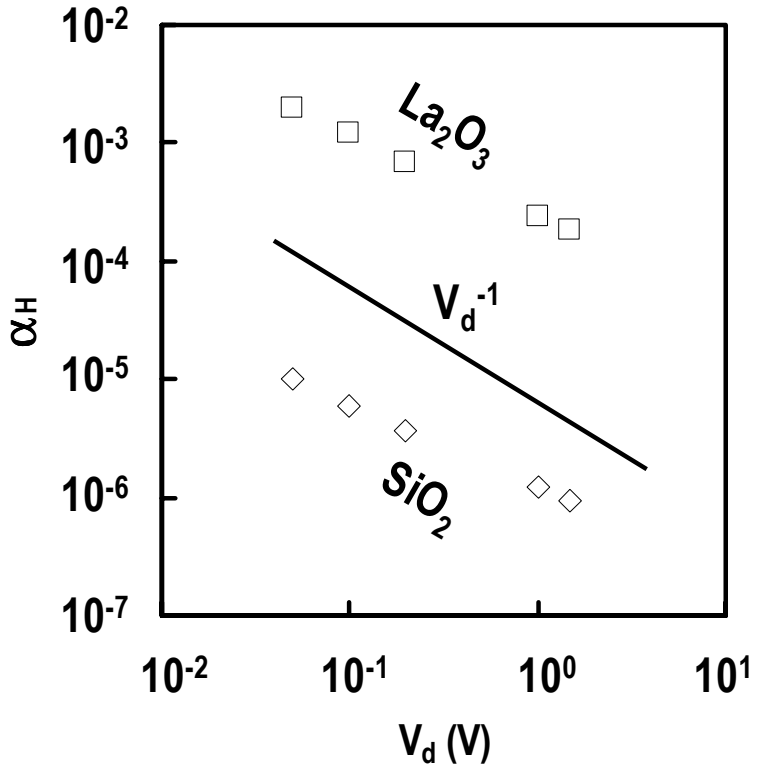

Fig. 4.15 Hooge's constant parameters α_H obtained from the fitting results of normalized drain current noise level ($WL \times S_{id}/I_d^2$) as a function of drain voltage.

4.5.7 Benchmarking with Roadmap Requirements

Fig. 4.16 exhibits comparison the gate reference noise normalized by EOT^2/WL with 1/*f* noise requirements for NMOS analog speed device in ITRS 2004 update version. Excess of 1/*f* noise of 1~2 orders for La_2O_3 gate insulator was observed. This might be a severe problem for the use La_2O_3 gate insulator for analog speed device.

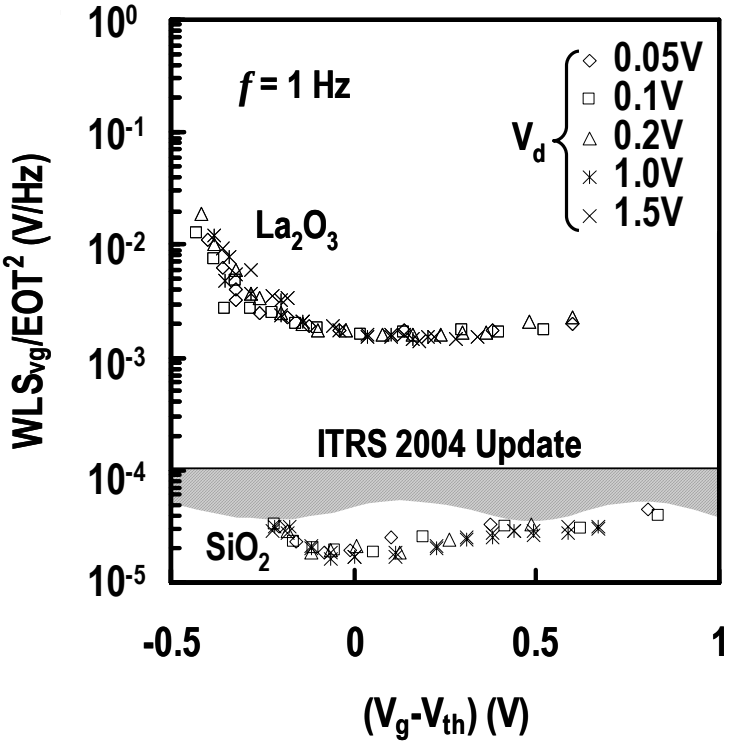

Fig. 4.16 Gate reference noise normalized by EOT^2/WL compares to 1/*f* noise requirements for NMOS analog speed device in ITRS 2004 update version. Excess of 1/*f* noise of 1~2 orders might be a severe issue for use of La_2O_3 gate dielectric for analog speed device.

4.6 Summary of This Chapter

So far, we have been evaluating the low-frequency characteristics of La_2O_3 gate insulated NMISFET. The noise power density of MISFET has dependency on the DC biasing conditions. Measurements from weak to strong in both linear and saturation were carried out in a shielded chamber. The noise spectra exhibit no specific hump that corresponds to dominancy of single trap. However, the frequency index γ was varied from 0.75 to 1.1 for La_2O_3 NMISFET. It indicated that the traps give a particular distribution in the insulator. It might be concluded that La_2O_3 NMISFET performs high state density at the Si-La_2O_3 interfaces.

For relatively long channel NMISFETs, it could be shown that the noise levels follow proportionality with L^{-3} when the metallurgical channel lengths are scaled down. Our experiment data give the same characteristics. However, in practical scaling method, both lateral and vertical dimensions of MISFET are reduced with the same factor. As a result, we still get the advantage of $1/f$ noise reduction, as the noise level is proportional to C_{ox}^2.

Fitting results of noise level from unified low-frequency noise model suggested the trap density of $N_t \sim 4\times10^{19}$ $eV^{-1}cm^{-3}$ for La_2O_3 NMISFET, while for thermal SiO_2 is $N_t \sim 2\times10^{18}$ $eV^{-1}cm^{-3}$. The trap density value for La_2O_3 NMISFET was of the same order of fix charge density obtained from flatband shift. Discrepancy to the exact value might be due to non-uniformity distribution of fixed charge in the film or the fitting error. La_2O_3 NMISFET exhibited higher apparent α_H value than that of thermal SiO_2. Mobility fluctuation might be due to carrier scattering by higher state densities in Si-La_2O_3 interface rather than the damaged Si crystalline.

Finally, by comparing with 1/*f* noise requirements for NMOS analog speed device in ITRS 2004 update version, we can get the excess of 1/*f* noise of 1~2 orders for La_2O_3 gate insulator. This might be a severe problem for the use La_2O_3 gate insulator for analog speed device. Suppressing interface state densities as well as fix charge densities should be addressed as they are suspected to be the main factor of the increasing such noise.

Chapter 5. Electrical Properties of Ultra-Shallow p^+/n Junctions

The main objective of forming ultra-shallow junctions in source/drain extension is to suppress the short channel effects in transistors. The shallower the junction depth, the more short channel effect can be suppressed. Generally, shallower the junction gives higher sheet resistance which is correlated to drive current degradation. While maintaining the sheet resistance, forming shallower junction depth is a must in ultra-shallow junction formation.

5.1 Calculation on Activated Dopant Concentration

The effectiveness of electrical activation annealing can be examined by activation rate that is defined as below.

$$activation\,rate(\%) = \frac{electrically\,activated\,carrier\,dose}{total\,dose} \times 100\% \quad \textbf{Eq. 5.1}$$

The electrically activated carrier dose is usually measured with Hall-Van der Pauw method that is difficult to perform. Estimation of the electrical activated dose can be calculated with SIMS profile and R_s. Fig. 5.1 illustrates calculation of activation dopant concentration or dose by using SIMS profile, carrier mobility, and sheet resistance value. The carrier mobility is assumed to be dependence on the impurity concentration as describe in Appendix D.

The activated dose N_S at x_n is calculated as the following.

$$N_S(x_n) = x_n S(x_n) + \sum_{i=n}^{N} S(x_i) \cdot \Delta x_i \qquad \textbf{Eq. 5.2}$$

At this point the activated dose may give the sheet resistance R_s

$$R_S(x_n) = \frac{1}{qN_S(x_n)\mu_p(S(x_n))} \qquad \textbf{Eq. 5.3}$$

We may increase the dopant concentration up to calculated sheet resistance giving the same value to the measure Rs. Here, we get both activated dopant concentration and dose. The total dose is integration of the SIMS profile to the depth. Finally, activation rate can be estimated with Eq. 5.1 above.

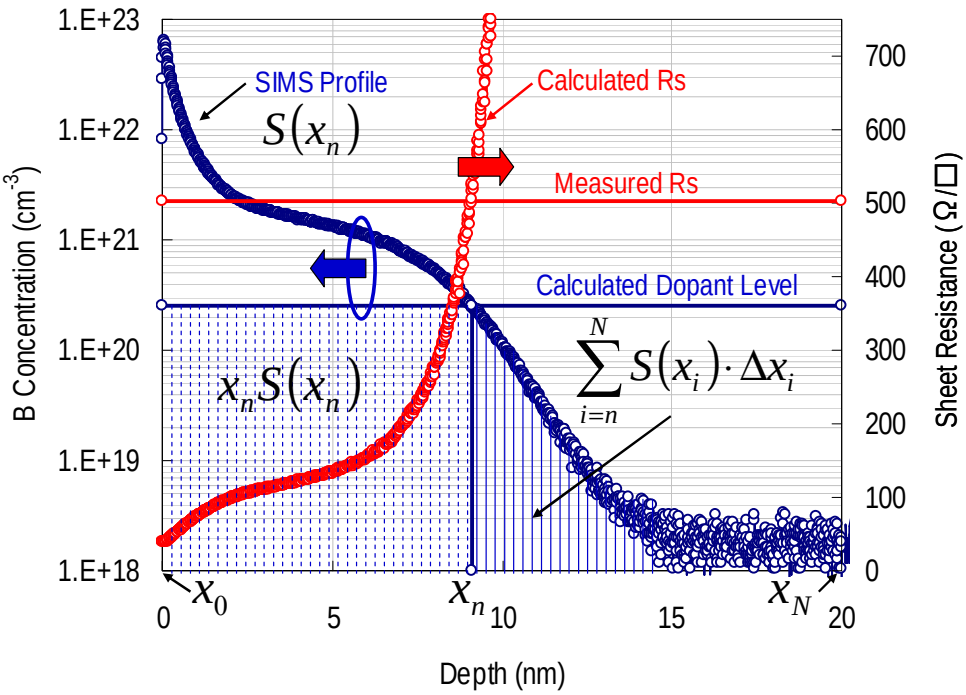

Fig. 5.1 Illustration of activation dopant concentration or dose by using SIMS profile, carrier mobility, and sheet resistance value.

5.2 Junction Leakage Characteristics of Ultra-Shallow p^+/n Junctions

Leakage current of p/n junction is one of the main parameter affecting the performances of devices such as photodiodes, charge couple devices (CCDs), dynamic random access memories (DRAMs), or off-state leakage current MOSFET devices. It is also related to fundamental properties of silicon materials such as recombination lifetime, generation lifetime, and surface recombination velocity. It is well known that there are three major components in p/n junction leakage: diffusion, generation, and surface generation components. The first two components are proportional to the area of the junction, and thus are called are components. The latter is proportional to the perimeter of the junction, and is thus called a perimeter component. Using junctions with the same area and different perimeters, we can separate the area and the perimeter components. However, it is not possible to separate the two area components, and only one of them is considered to dominate by the results of temperature dependence measurements.

The area and the perimeter components can be separated with two different geometrical junctions. Suppose two junctions with square type. Their perimeter length ratio is x and the area ratio is x^2. Total current flowing in the first junction is I_1, and the second is I_2. Then we may find,

$$I_1 = I_{area} + I_{perimeter} \qquad \textbf{Eq. 5.4}$$

$$I_2 = x^2 I_{area} + xI_{perimeter} \qquad \textbf{Eq. 5.5}$$

From Eq. 5.4 and Eq. 5.5, we may calculate I_{area} and $I_{perimeter}$ in the first junction as the

following.

$$I_{area} = \left(xI_1 - I_2\right) / \left(x - x^2\right) \quad \textbf{Eq. 5.6}$$

$$I_{perimeter} = -\left(x^2 I_1 - I_2\right) / \left(x - x^2\right) \quad \textbf{Eq. 5.7}$$

Hence, for the second junction, we get the area and the perimeter components as $x^2 I_{area}$ and $xI_{perimeter}$, respectively.

The three major components of one sided p^+/n junction leakage current are expressed as the following.

(1) Diffusion component

$$J_{diff,p} = \frac{qD_p n_i^2}{L_p N_D}\left\{\exp\left(-\frac{qV_R}{kT}\right) - 1\right\} \quad \textbf{Eq. 5.8}$$

where q is the electron charge, D_p is the diffusion constant of holes, n_i is the intrinsic carrier density, N_D is the donor density, and L_n is the diffusion length of hole.

(2) Generation component

$$J_g = \frac{qn_i W}{\tau_g}\left\{\exp\left(-\frac{qV_R}{2kT}\right) - 1\right\} \quad \textbf{Eq. 5.9}$$

where τ_g is generation lifetime and W is the depletion width.

(3) Surface generation component

$$J_{sg} = qS_0 n_i W_s \frac{L}{A}\left\{\exp\left(-\frac{qV_R}{2kT}\right) - 1\right\} \quad \textbf{Eq. 5.10}$$

where S_0 is the surface recombination velocity and W_s is the depletion width at the surface, L is the perimeter length of the junction, and A is the junction area.

The diffusion current is caused by generation in the neutral region and diffusion to the depletion region. The generation current is caused by generation in depletion region. Lastly, the surface generation current is caused by generation in depletion region at the junction edges. It can be due to Si/SiO_2 interfaces or structural defects.

5.2.1 Perimeter Currents, Physical Stress Effects, and Device-to-Device Dispersion

Mesa-typed p^+/n junctions may have very large peripheral currents due to lattice structural defects at the edges. The ratio of area to perimeter component currents as function of side length of the junctions and pictorial of the origins of peripheral currents is illustrated in Fig. 5.2. To obtain area current of 10 times larger then its peripheral, junctions with 6mm×6mm is required. Somehow, the perimeter component value may increase depending on the etching results.

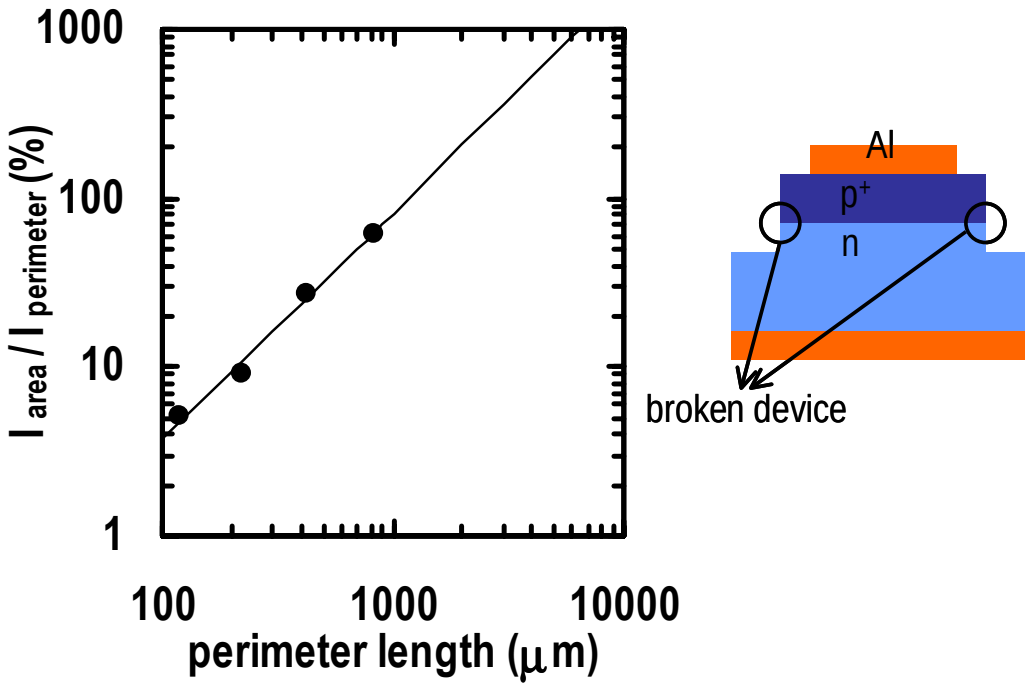

Fig. 5.2 The ratio of area to perimeter component currents as function of side length of the junctions and pictorial of the origins of peripheral currents. To obtain area current of 10 times larger then its peripheral, junctions with 6mm×6mm is required.

Considerably, edge rinsing or recovery can reduce the perimeter current component of mesa-typed junction. Edge recoveries by oxidation are worsening the case, since low quality of silicon dioxide give addition to the peripheral current. Fig. 5.3 shows the I-V characteristics after chemical oxide edge treatment by dipping in hydrogen peroxide H_2O_2 for 30 min. The reverse bias current is increasing up to three orders higher than the initial value.

Edge recovery with oriental selectivity silicon etchant might be the solution to lower the peripheral currents regarding to improve the quality of the edges. Fig. 5.4 shows calculated peripheral currents of mesa-type p^+/n junctions after dipping in photo resist developer for 15 min. While, the calculated area component of sample after edge treatment with photo resist developer for 15 min is shown in Fig. 5.5. Junction with 820μm×820μm gives 5 times higher in area component current than its perimeter.

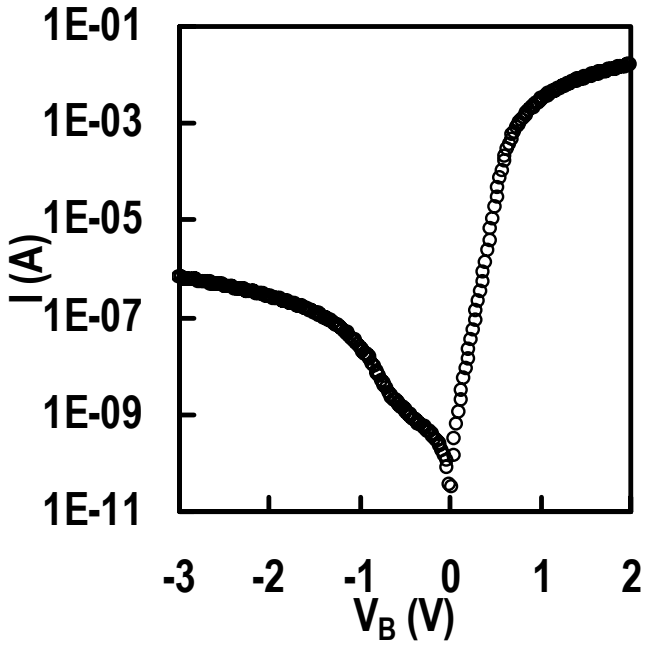

Fig. 5.3 *I-V* characteristics after edge treatment with hydrogen peroxide H_2O_2 for 30 min.

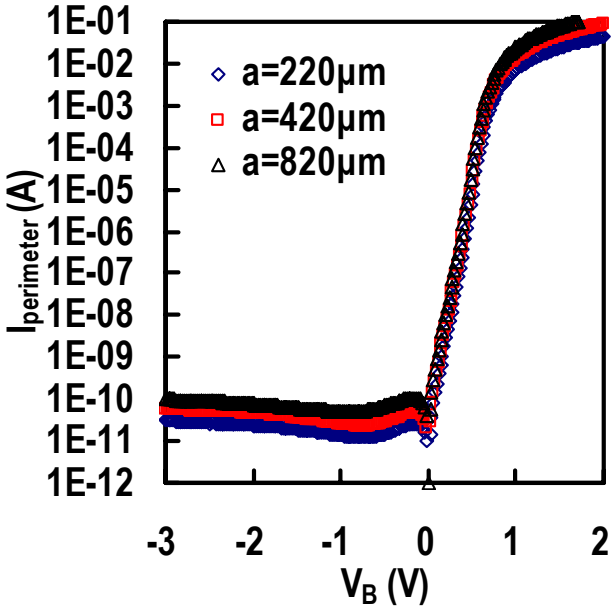

Fig. 5.4 Calculated peripheral currents of mesa-type p^+/n junctions after dipping in photo resist developer for 15 min.

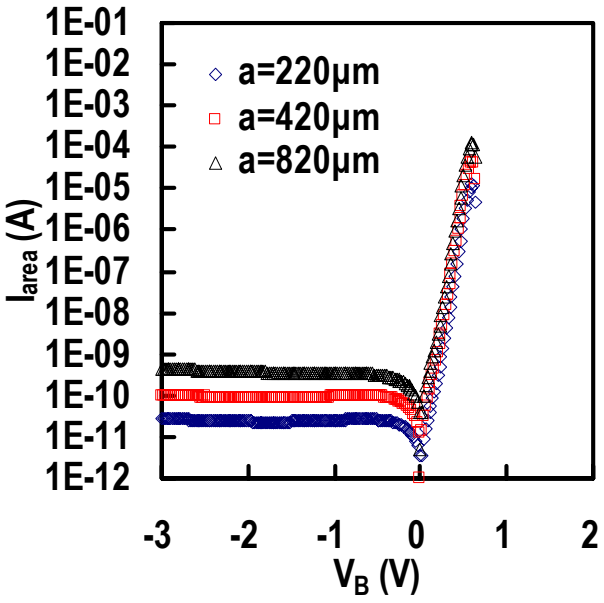

Fig. 5.5 Calculated area component of sample after edge treatment with photo resist developer for 15 min. Junction with 820μm×820μm gives 5 times higher in area component current than its perimeter.

Device-to-device variation in the same sample is shown in Fig. 5.6, and it is considerably small and negligible. The probe's physical stress result is given in Fig. 5.7. Device with junction depth X_j of 5.2 nm is relatively strong enough against physical stress. The junction is showing spurious currents after stressing by lowering the probe of about 100 μm. Fig. 5.8 provides reverse-biased currents as a function of time after temperature indicator giving the setting value. The currents are fluctuated due to instability of temperature near room temperature.

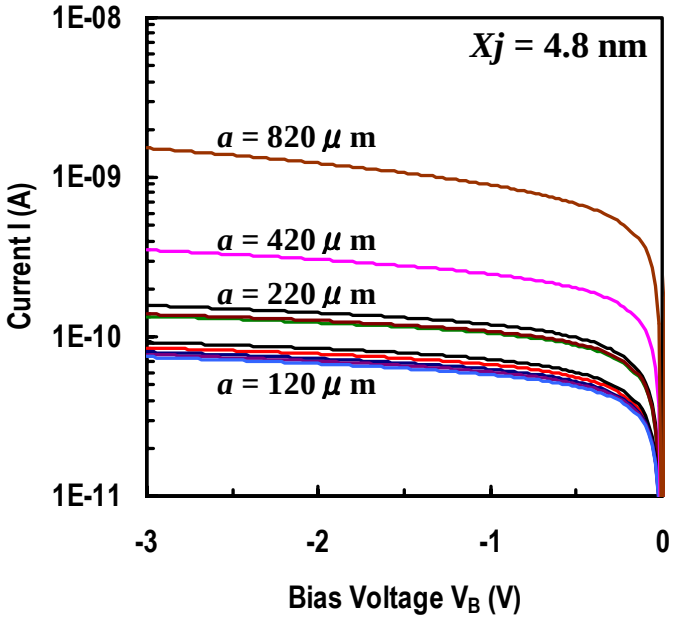

Fig. 5.6 Device-to-device variation in the same sample is considerably small.

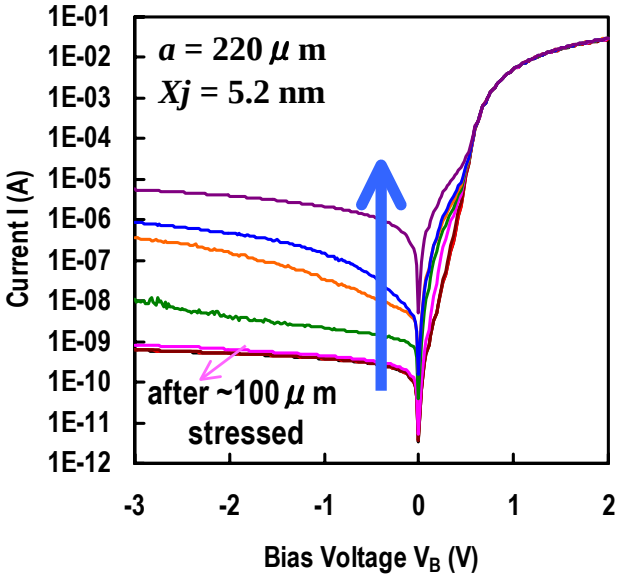

Fig. 5.7 Device with junction depth X_j of 5.2 nm is relatively strong against physical stress. The junction is showing spurious currents after stressing by lowering the probe of about 100 μm.

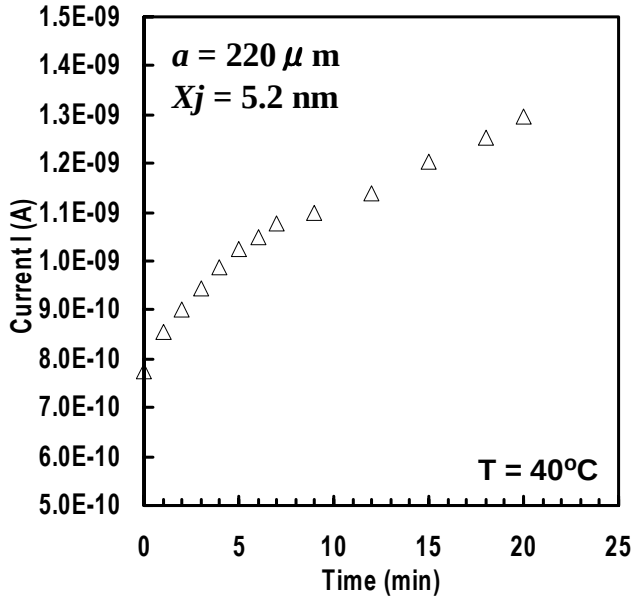

Fig. 5.8 Reverse-biased currents as a function of time after temperature indicator giving the setting value. The currents are fluctuated due to instability of temperature near room temperature.

5.2.2 Leakage Current Characteristics of Plasma Doped Ultra-Shallow p^+/n Junctions

Plasma doping (PD) achievements with spike RTA and flash lamp annealing (FLA) is provided in Fig. 5.9. Shallow junction with X_j ranges from 15 nm to 45 nm can be obtained with spike RTA, while X_j of less than 15 nm flash lamp activation annealing should be used. Fig. 5.10 shows comparison of reverse leakage current of plasma doping with both spike RTA and flash lamp annealing combinations. The peripheral currents are eliminated with dual-geometrical devices. Flash lamp annealing gives one order higher than spike RTA in leakage current. For overall result of reverse leakage current measured with V_B = -1V at room temperature is given in Fig. 5.11. These are total current of junction devices with 220μm×220μm.

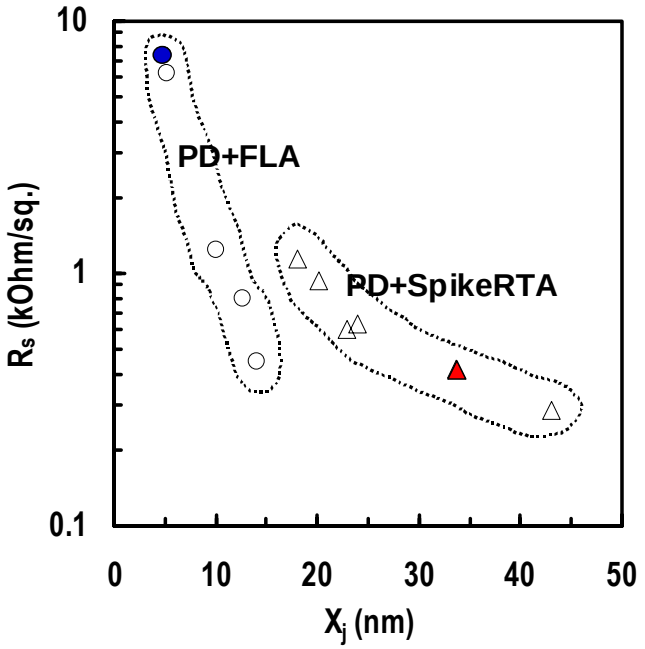

Fig. 5.9 Plasma doping (PD) achievements with spike RTA and flash lamp annealing (FLA).

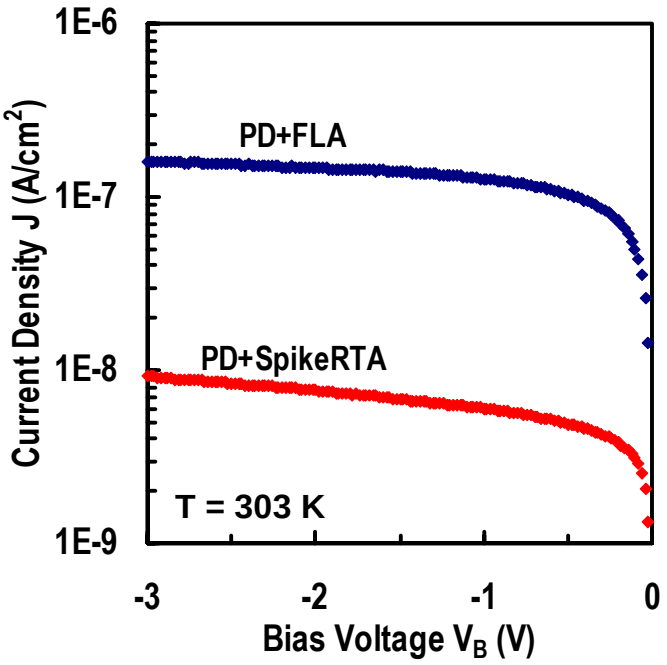

Fig. 5.10 Comparison of reverse leakage current of plasma doping with both spike RTA and flash lamp annealing combinations. The color corresponds to the plotted R_s-X_j in Fig 5.9. The peripheral currents are eliminated with dual-geometrical devices.

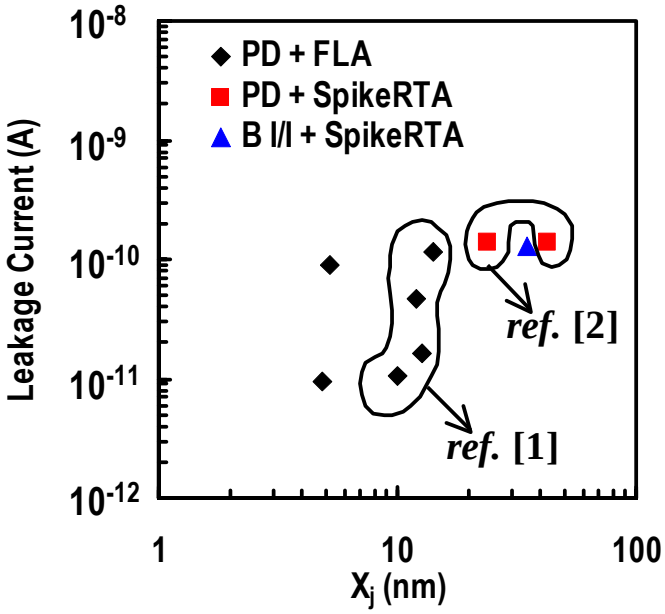

Fig. 5.11 Overall result of reverse leakage current measured with V_B = -1V at room temperature. These are total current of junction devices with 220μm×220μm.

5.2.3 Plasma Doping and Spike RTA Combination

Temperature dependence of reverse biased *J-V* corrected with dual geometrical devices of Spike RTA annealed plasma doping sample is given in Fig. 5.12, while the Arrhenius plots at V_B = -0.3 V is shown in Fig. 5.13. The activation energy of the deep-trap level is observed as the silicon band gap. This shows that diffusion currents are dominant at the measured temperature.

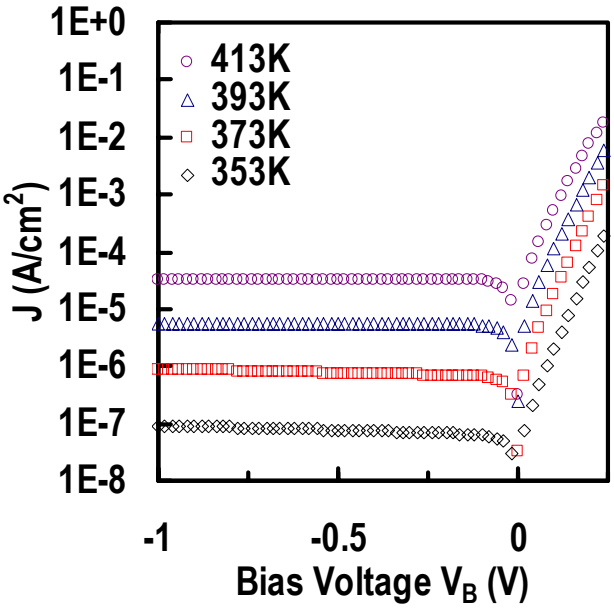

Fig. 5.12 Temperature dependence of reverse biased *J-V* corrected with dual geometrical devices of PD + Spike RTA sample.

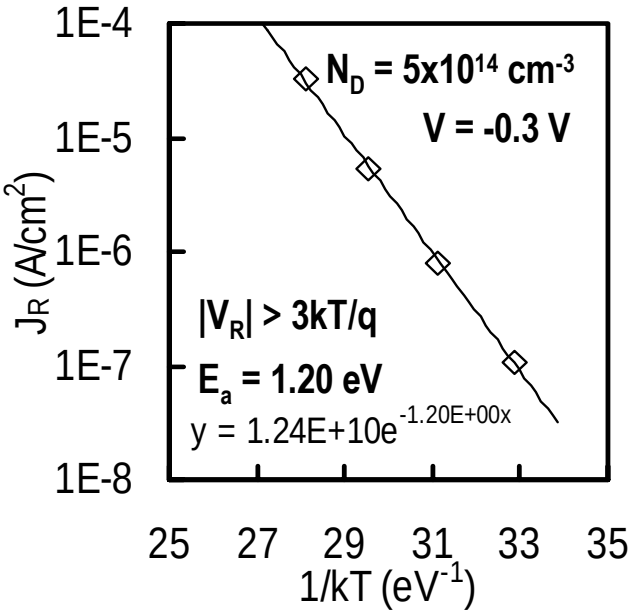

Fig. 5.13 Activation energy of the deep-trap level is observed as the silicon band gap. This shows that diffusion currents are dominant at the measured temperature.

5.2.4 Plasma Doping and Flash Lamp Annealing Combination

Temperature dependence of reverse biased *J*-*V* corrected with dual geometrical devices of PD + FLA sample with X_j = 4.8 nm is shown in Fig. 5.14. While the Arrhenius plots of activation energy of the deep-trap level is provided in Fig. 5.15. From the figure, the activation energy is observed as E_a = 0.77 eV. Fig. 5.16 gives high frequency of C^{-2}-*V* and *W*-*V* plots for flash lamp annealed plasma doping samples with X_j = 4.8 nm. From the slope and intersection with *x*-axis of C^{-2}-*V* curve, substrate doping N_D of 5×10^{14} cm^{-3} and junction built-in potential V_{bi} of 0.7 V can be calculated. Fig. 5.17 shows generation lifetime τ_g calculated from *J*-*W* curve. Generation lifetime decreases with the increase of depletion width.

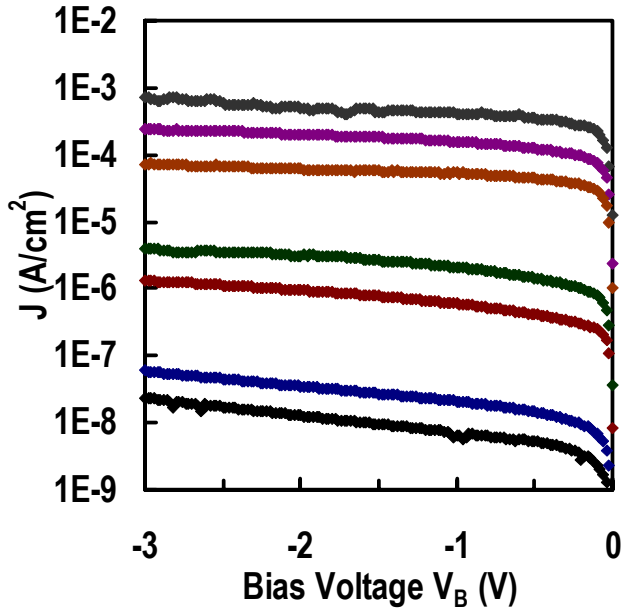

Fig. 5.14 Temperature dependence of reverse biased *J-V* corrected with dual geometrical devices of PD + FLA sample with X_j = 4.8 nm.

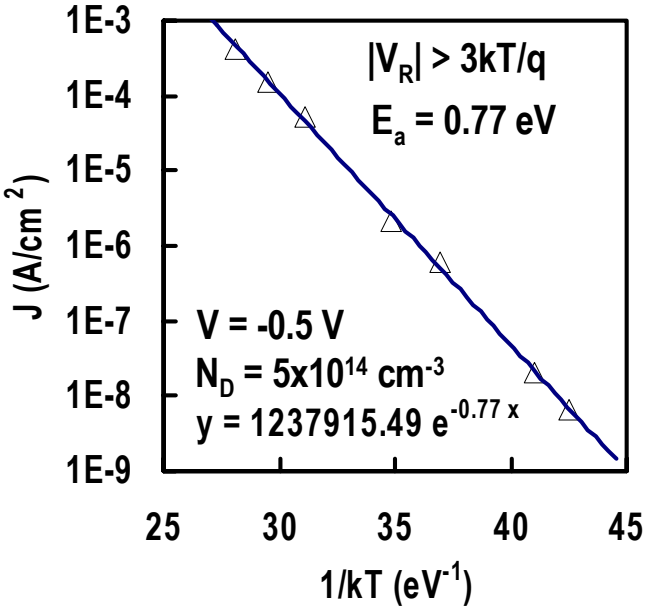

Fig. 5.15 Activation energy of the deep-trap level is observed as E_a = 0.77 eV.

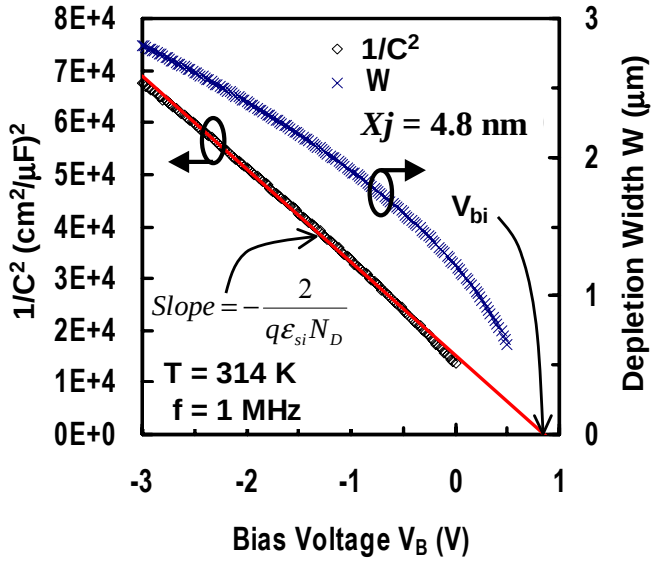

Fig. 5.16 High frequency of C^{-2}-V and W-V plots for PD + FLA samples with X_j = 4.8 nm. From the slope and intersection with x-axis of C^{-2}-V curve, substrate doping N_D and junction built-in potential V_{bi} can be calculated.

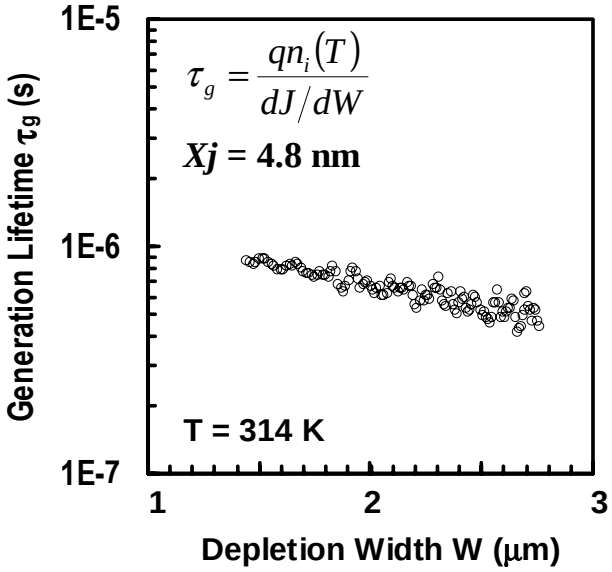

Fig. 5.17 Generation lifetime calculated from J-W curve.

5.3 Total Trap Densities with Capacitance Method

There are many ways in measuring the deep level trap densities of p/n junction with each having strengths and weaknesses. Deep level transient spectroscopy (DLTS) seems to be the most commonly used because of its measurement sensitivity. However, steady-state capacitance measurement technique might be considerable due to its simplicity. For semiconductor with shallow level donors and deep level acceptors, $1/C^2$ is given as the following.

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_0\varepsilon_{Si}} \frac{V_{bi} - V}{N_D - n_T(t)} \qquad \textbf{Eq. 5.11}$$

The slope can be obtained by differentiating Eq. 5.11 against bias voltage V, that is

$$\frac{dV}{d\left(1/C^2\right)} = -\frac{q\varepsilon_0\varepsilon_{Si}}{2}\left(N_D - n_T(t)\right) \qquad \textbf{Eq. 5.12}$$

For high frequency (HF) reverse-biased capacitance measurement gives $t \rightarrow \infty$, and consequently $n_T(\infty) \approx 0$. On the contrary, for steady-state (LF) measurement, it gives $t \rightarrow 0$, and $n_T(0) \approx N_T$. This is applicable for $e_n >> e_p$. The difference of the slopes gives the deep-level impurity as expresses in the following form.

$$\left.\frac{dV}{d\left(1/C^2\right)}\right|_{HF} - \left.\frac{dV}{d\left(1/C^2\right)}\right|_{LF} = -\frac{q\varepsilon_0\varepsilon_{Si}}{2} N_T \qquad \textbf{Eq. 5.13}$$

Steady-state reverse-biased capacitance can be measured with quasi-static *C-V* measurements with Agilent 4156C semiconductor analyzer. However, this requires extremely low leakage current.

Frequency dependence of C^{-2} curves vs. bias voltage V_B is plotted in Fig. 5.17. The lowest three curve lines are measured with quasi-static technique with different junction area, while the highest curves are measured high frequency of 1 MHz. Dispersion of quasi-static C^{-2} curves is considered to be the effects of peripheral defects.

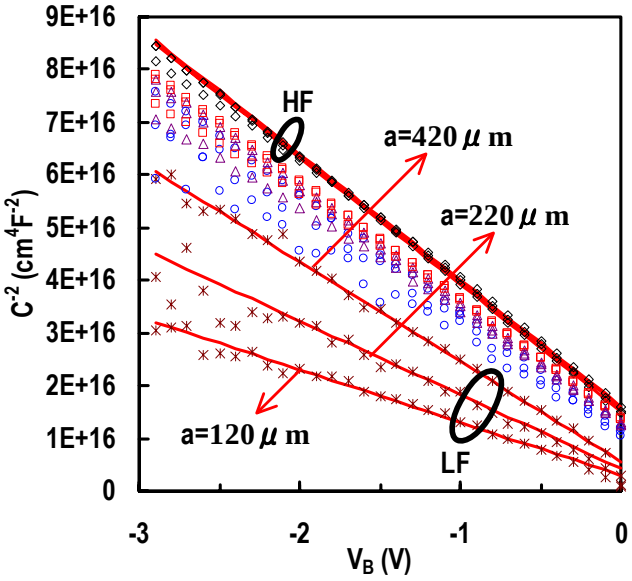

Fig. 5.18 Frequency dependence of C^{-2} plots vs. bias voltage V_B. The lowest three curve lines are measured with quasi-static technique with different junction area, while the highest curves are measured at 1 MHz.

5.4 Summary of This Chapter

Junction device parameter extraction can be performed with *J-V* and *C-V* measurements. Deep-level traps can be characterized by their temperature dependence. However, in mesa-typed junctions, this is very difficult to do that because of intolerable perimeter current dominations.

Very low reverse-biased currents were obtained with PD and spike RTA or flash lamp annealing by using substrate doping of about 5×10^{14} cm^{-3}. The recombination lifetime is several 10^{-7} sec. The depletion width stretches in substrate direction for several μm.

Chapter 6. Conclusions and Future Issues

We have been so far evaluating the low-frequency noise in NMISFET with e-beam evaporated La_2O_3 gate dielectrics and with thermal SiO_2 for comparative study. Furthermore, the electrical properties of ultra-shallow p^+/n junction formed by plasma doping process over high resistivity substrate of 8-12 Ω-cm were explored extensively. In this chapter, we may take several conclusions and state the expected formation, and future issues.

6.1 Conclusions

This work contains two studies, i.e., low-frequency noise and ultra-shallow p^+/n junction studies. The results of this work are stated accordingly as below.

6.1.1 Low-Frequency Noise

The La_2O_3 NMISFET exhibits high $1/f$ noise. The gate reference noise normalized by EOT^2/WL is in the order of 1-2 orders higher than roadmap requirement for NMOS high-speed analog device. This problem can be traced from the origins of $1/f$ noise, which is mainly caused by the excessive of trap densities of $N_T \sim 4\times10^{19}$ /eV-cm^3 and high phonon scattering coefficient of $\alpha_H \sim 10^{-4} - 10^{-3}$. The excessive of trap densities may raise the remote scattering coefficient of $\alpha_{sc} \sim 8\times10^{-4}$ Vs. Traps in the insulator is

on positive fix charge type. This is probably caused by oxygen vacancies since La_2O_3 thin film was deposited in ultra-high vacuum condition (10^{-7} – 10^{-8} Torr) and insufficiency in introducing oxygen during post deposition annealing. In the second hand, it is difficult to make a statement to the main factor of phonon scattering. However, phonon scattering seems to be in existence for most of NMISFETs with high-k gate dielectric since mobility lowering at middle electric field often to be observed. It can be speculated that phonon scattering is probably as a result of ionic bonding of the high-k materials, metal gate lattice, or e-beam radiation. There has been report that e-beam radiation may physically bombard the quality of metal lattice and give rise to phonon scattering coefficient. After all, high 1/*f* noise level may restrict the adoption of La_2O_3 gate dielectrics in NMOS for HF or AMS applications, and solutions to this issue should be addressed.

6.1.2 Ultra-shallow p^+/n Junctions

When characterizing very low leakage currents, mesa-typed p^+/n junctions are suffering from the peripheral current effect that is determined according to how they were etched. Oxidizing the edge was not the solution since low quality of the oxide may enhance the perimeter currents. Edge recovery with oriental selectivity silicon etchant may lower the peripheral currents regarding to improvement the quality of the edges. Otherwise, we may ignore the perimeter currents by using junction area as wide as 6mm×6mm. It is due to area to perimeter ratio is about one order.

To extract the activation energy of deep-level traps, reverse-biased current measurements over temperature range is required. Higher temperature gives the silicon

band gap energy level, since diffusion current is strong function against temperature. Lower temperature will extract the activation energy of the deep-level traps. In mesa-typed junctions, this is very difficult to do because of intolerable perimeter current dominations in lower temperature.

6.2 Future Issues

For low-frequency noise in La_2O_3 NMISFET, suppressing the trap density might be the first priority in thin film formation. It could be carried out with lower vacuum pressure deposition process or sufficiently annealing the thin films under the best-suited ambient gases. Condition in deposition must be optimized to obtain high quality thin films. The second, the most suitable metal gate with middle band gap work function should be applied to control the threshold voltage. The third, an attempt to use another surface treatment like nitridation may lead to improvement of the channel interfaces with lower 1/*f* noise level. Lastly, if the phonon scattering is caused by electron beam radiation, sintering process may recover the crystalline quality of the Si channel.

For ultra-shallow p^+/n junction, peripheral current must be suppressed to allow deep-level traps extraction. This should be able to be done with LOCOS separated junction device with at least two device areas. While for trap that is very near to doping layers, higher doped substrate must be used to make the depletion width narrower. Impurity doping for higher doped substrate might be different to lower doped substrate since there are many active carriers that must neutralize the initial opposite carrier. Considering the next channel substrate doping for MOSFET, doping technique with this substrate must be established.

Appendixes

There have been many measurements on the physical characteristics of semiconductor materials like resistivity, band gap, intrinsic carrier concentration, drift mobility or minority carrier mobility. These physical characteristics are important in modeling or understanding the electrical characteristic behaviors. In these appendixes, we show several physical characteristics in the form of equation expressions or graphs.

Appendix A. Conversion between Resistivity and Impurity Concentration for Boron- and Phosphorus-Doped Silicon

It is important to select the resistivity ρ of a semiconductor for starting material as well as for semiconductor devices. The resistivity of a wafer is determined by the impurity concentration, and it can be modified during device processing by impurity doping like diffusion or ion implantation.

Conversion between resistivity and impurity concentration for boron- and phosphorus-doped silicon can be calculated with the following empirical formula. For boron-doped silicon, the impurity concentration and the resistivity is

$$N_B = \frac{1.330\times10^{16}}{\rho} + \frac{1.082\times10^{17}}{\rho\left[1+(54.56\rho)^{1.105}\right]} \qquad \textbf{Eq. A.1}$$

$$\rho = \frac{1.305\times10^{16}}{N_B} + \frac{1.133\times10^{17}}{N_B\left[1+\left(2.580\times10^{-19}N_B\right)^{-0.737}\right]} \qquad \textbf{Eq. A.2}$$

where ρ is the resistivity in Ω.cm and N_B the boron concentration in cm^{-3}. For phosphorus-doped silicon, the impurity concentration is

$$N_P = \frac{6.242\times10^{18}10^{Z}}{\rho} \quad \textbf{Eq. A.3}$$

$$Z = \frac{A_0 + A_1 x + A_2 x^2 + A_3 x^3}{1 + B_1 x + B_2 x^2 + B_3 x^3} \quad \textbf{Eq. A.4}$$

$$x = \log_{10} \rho \quad \textbf{Eq. A.5}$$

where A_0 = -3.1083, A_1 = -3.2626, A_2 = -1.2196, A_3 = -0.13923, B_1 = 1.0265, B_2 = 0.38755, and B_3 = 0.041833. The resistivity is

$$\rho = \frac{6.242\times10^{18}10^{Z}}{N_P} \quad \textbf{Eq. A.6}$$

$$Z = \frac{C_0 + C_1 y + C_2 y^2 + C_3 y^3}{1 + D_1 y + D_2 y^2 + D_3 y^3} \quad \textbf{Eq. A.7}$$

$$y = \log_{10}(N_P) - 16 \quad \textbf{Eq. A.8}$$

where C_0 = -3.0769, C_1 = 2.2108, C_2 = -0.62272, C_3 = 0.057501, D_1 = -0.68157, D_2 = 0.19833, and D_3 = -0.018376. Finally, the resistivity plots as a function of impurity concentration are showed in Fig. A.1. From the figure, the linearity deviations of ρ-N in high doped region are known as the effect of coulomb scattering.

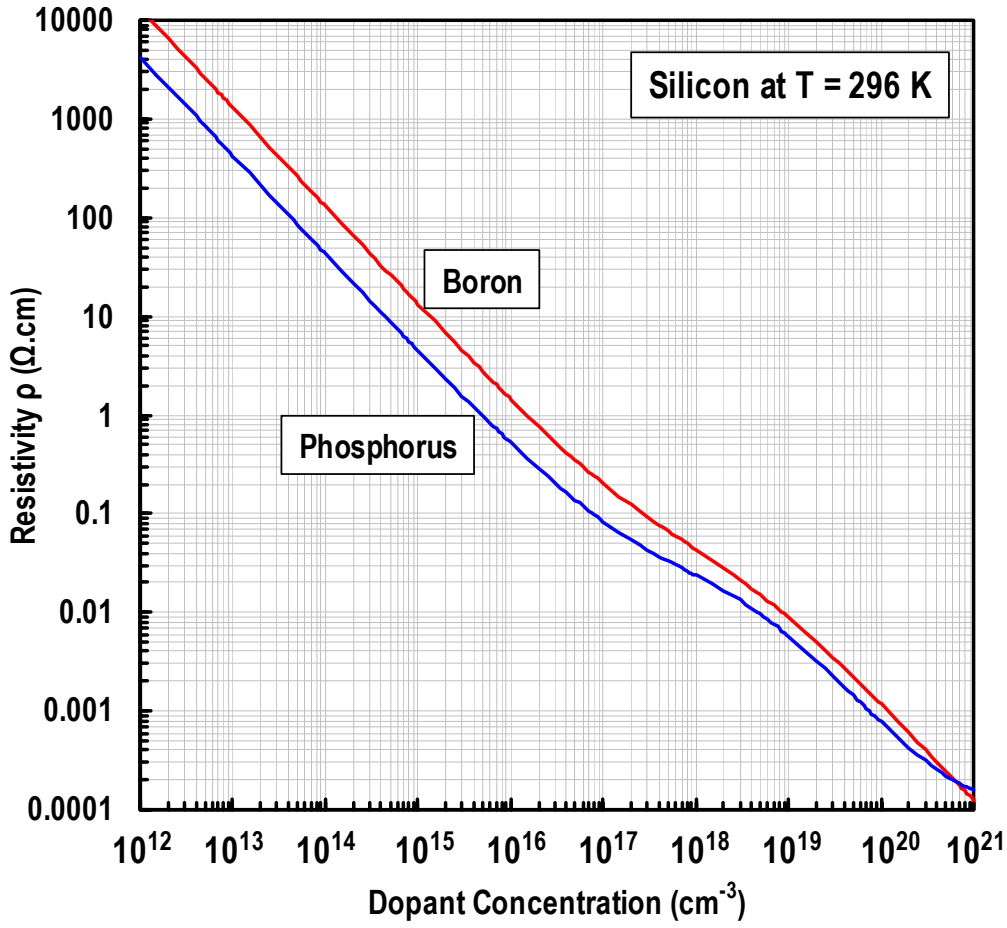

Fig. A.1 Resistivity as a function of impurity concentration for p-type (boron-doped) and n-type (phosphorus-doped) silicon at 296 K. Linearity deviations from impurity of 10^{17} are known as coulomb scattering effects.

Appendix B. Temperature Dependent of Energy Band gap

The energy band gap of semiconductors is a fundamental parameter to explain carrier behaviors and electrical properties. The temperature dependent of band gaps can be expressed with universal function given as below.

$$E_g = E_{g0} - \frac{\alpha T^2}{T + \beta} \qquad \textbf{Eq. A.9}$$

where, E_{g0}, α, and β are given in the following table.

Table A-1 E_{g0}, α, and β for Si, Ge, and GaAs

	Si	Ge	GaAs
E_{g0}	1.170	0.7437	1.519
α	4.730×10^{-4}	4.774×10^{-4}	5.405×10^{-4}
β	636	235	204

The band gaps of Si, Ge, and GaAs over temperature up to 900K are shown in Fig. A.2. At room temperature, the band gap values of high-purity semiconductors are 1.12 eV for Si, 0.66 eV for Ge, and 1.42 eV for GaAs. For highly-doped semiconductors, these values become smaller.

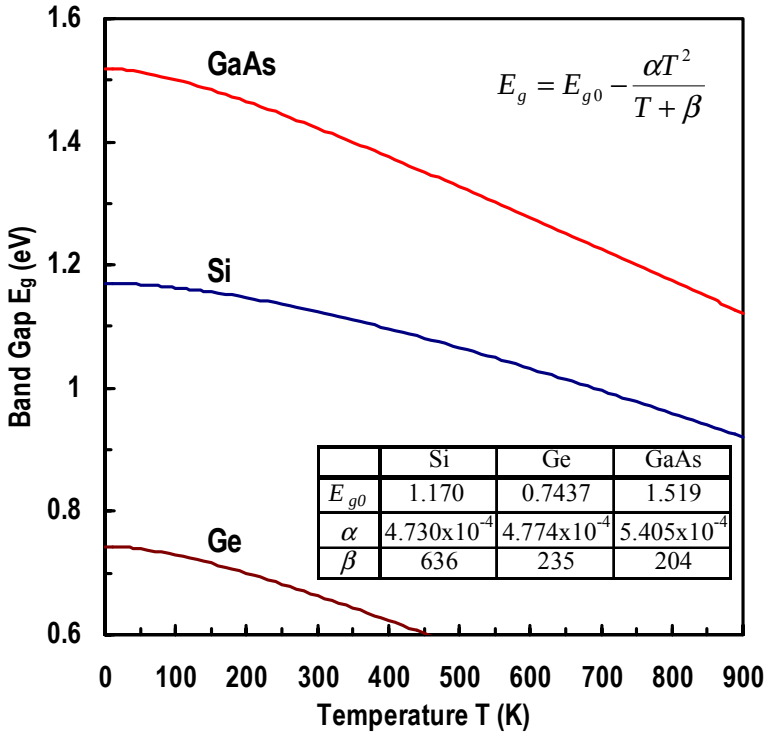

Fig. A.2 Energy band gaps as a function of temperature for Si, Ge, and GaAs. High purity silicon has 1.12 eV at room temperature.

Appendix C. Temperature Dependent of Intrinsic Carrier Density for Silicon

The intrinsic carrier concentration n_i is an important parameter needed for modeling semiconductor properties and devices. An accurate measurement of n_i for silicon has been refine for temperature range over 77-400K. Empirical expression of n_i for Si is given by,

$$n_i = 1.640 \times 10^{15} T^{1.706} e^{-E_g / 2kT} \qquad \textbf{Eq. A.10}$$

The plots of this expression at temperature range of 200-400K are shown in Fig. A.3. At 300K, Si intrinsic carrier concentration n_i can be found of 1.0×10^{10} cm^{-3}.

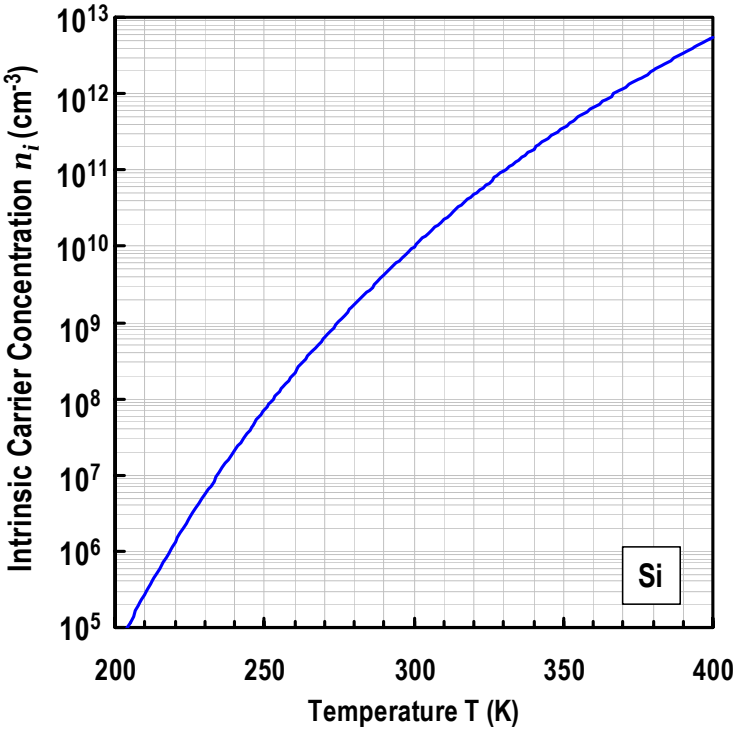

Fig. A.3 The plotted intrinsic carrier concentration as a function of the temperature for Silicon. The intrinsic carrier concentration is of about two times in every ten degrees of the increasing temperature.

Appendix D. Impurity Concentration Dependent of Majority Carrier Mobility for Boron- and Phosphorus-Doped Silicon

Drift mobility is an essential parameter defining the current and speed of unipolar devices, where majority carriers are dominant in carrier transport. When an electric field is applied to a material, carriers are accelerated and acquire a drift velocity superimposed upon random thermal motion. For low-doped semiconductors, the drift mobilities are mainly limited by carrier collisions with silicon lattice or acoustic phonons. While for highly-doped semiconductors, collisions with ionized impurity atoms through coulomb interaction become more important in decreasing the mobilities. For silicon at room temperature, the ionized impurity concentration dependent of electron and hole mobilities can be expressed with the following empirical expressions.

$$\mu_n(N_D) = 68.5 + \frac{(1414 - 68.5)}{1 + \left(\frac{N_D}{9.2\times10^{16}}\right)^{0.711}} \quad (cm^2/V-s) \qquad \textbf{Eq. A.11}$$

$$\mu_p(N_A) = 44.9 + \frac{(470.5 - 44.9)}{1 + \left(\frac{N_A}{2.23\times10^{17}}\right)^{0.719}} \quad (cm^2/V-s) \qquad \textbf{Eq. A.12}$$

where N_A and N_D are the ionized impurity atoms. The plot these expressions can be found in Fig. A.4. The electron mobility is approximately three times the hole mobility, since the effective mass of electrons in conduction band is much lower than that of the holes in valence band.

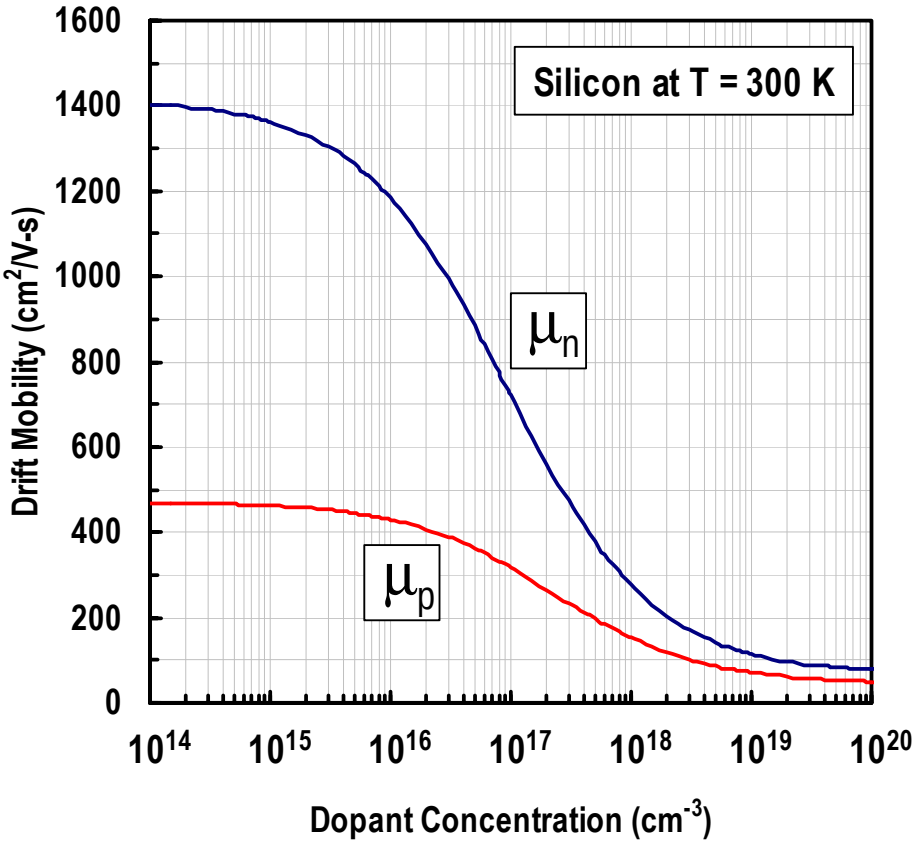

Fig. A.4 Electron and hole mobilities as a function of impurity concentration for silicon at 300 K.

Appendix E. Impurity Concentration Dependent of Minority Carrier Mobility, Lifetime, and Diffusion Length for Silicon

The minority-carrier mobility μ, lifetime τ and diffusion length L are important in modeling the electrical behavior of p-n junction. The empirical equations for minority-carrier electron and minority-carrier holes are given as the following.

$$\mu_n = 232 + \frac{1180}{1 + \left(\frac{N_A}{8 \times 10^{16}} \right)^{0.9}} \quad (cm^2 / V - s) \qquad \textbf{Eq. A.13}$$

$$\mu_p = 130 + \frac{270}{1 + \left(\frac{N_D}{8 \times 10^{17}} \right)^{1.25}} \quad (cm^2/V-s) \qquad \textbf{Eq. A.14}$$

$$\frac{1}{\tau_n} = 3.45 \times 10^{-12} N_A + 0.95 \times 10^{-31} N_A^2 \quad (s^{-1}) \qquad \textbf{Eq. A.15}$$

$$\frac{1}{\tau_p} = 7.8 \times 10^{-13} N_D + 1.8 \times 10^{-31} N_D^2 \quad (s^{-1}) \qquad \textbf{Eq. A.16}$$

where N_A and N_D are the ionized impurity atoms. The diffusion lengths are calculated from the mobilities and lifetimes using the relation $L = (kT\mu\tau/q)^{1/2}$. The minority-carrier mobilities, lifetime, and diffusion lengths as a function impurity concentration are shown in Fig. A.5, A.6, and A.7, respectively.

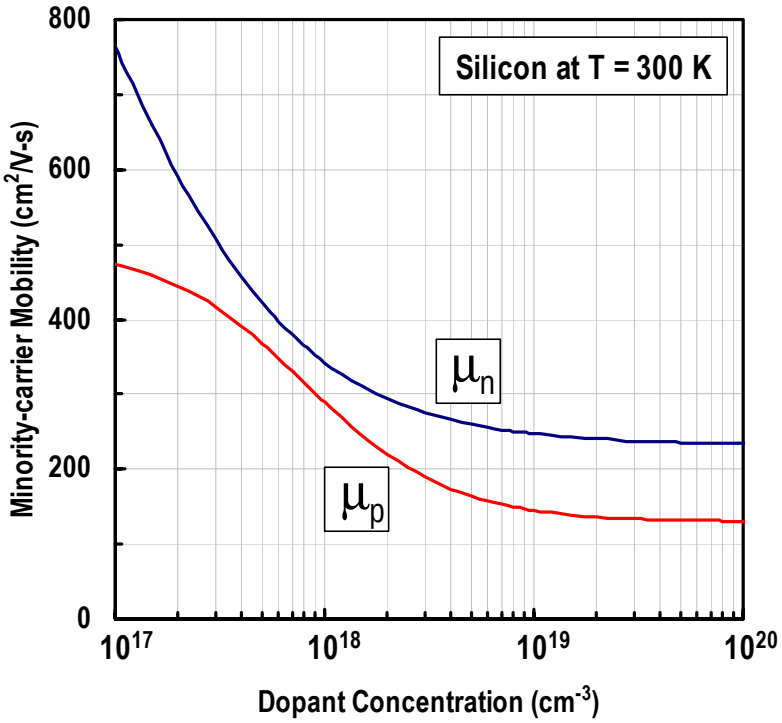

Fig. A.5 Minority-carrier mobilities as a function of impurity concentration.

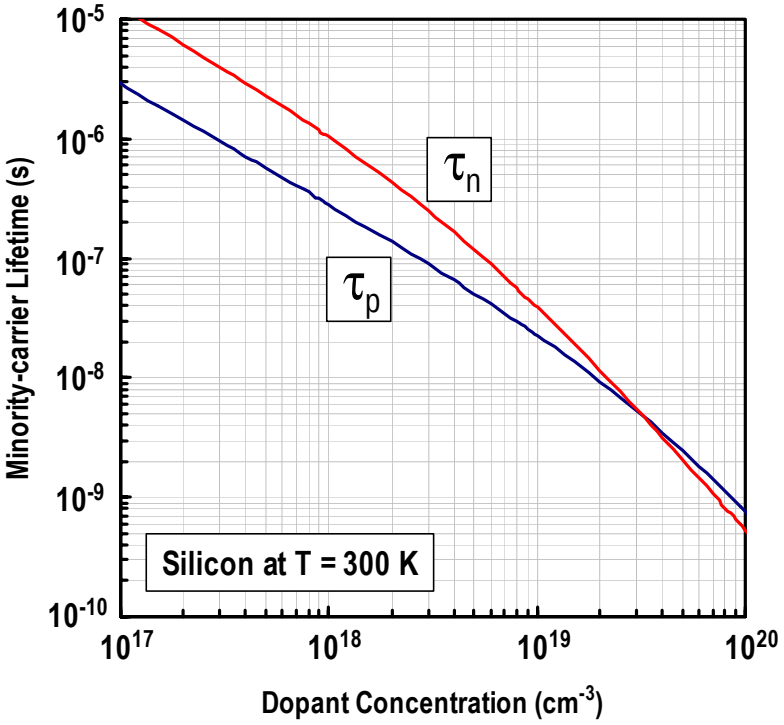

Fig. A.6 Minority-carrier lifetimes as a function of impurity concentration.

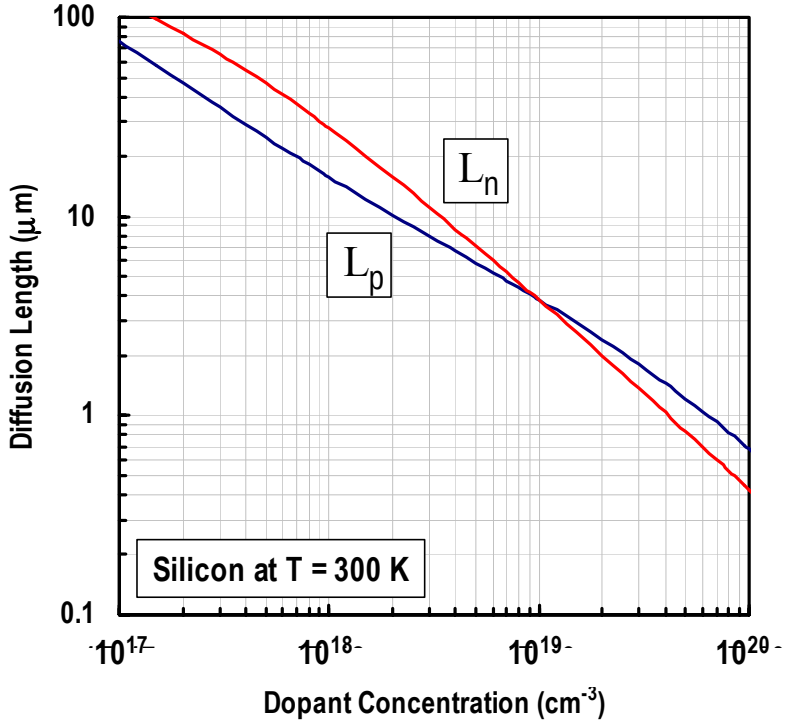

Fig. A.7 Diffusion lengths as a function of impurity concentration.

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