Master Thesis

A study on High-k Stacked Gate Dielectric Thin Films of Rare Earth Oxides

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Contents

Chapter 1 Introduction

1.1 Background…… 2
1.2 Physical Properties of Rare Earth Oxides…….. 7
1.3 Purpose of This Study…… 8

Chapter 2 Fabrication and Characterization Method

2.1 Fabrication Methods…….. 10
2.1.1 Si Substrate Wet Cleaning Process…... 11
2.1.2 Molecular Beam Deposition (MBE) Process…12
2.1.3 Rapid Thermal Annealing (RTA) Process…13
2.1.4 Vacuum Evaporation Process …….. 14
2.1.5 Transistor (n-MISFET) Process….... 15
2.2 Measurement Equipment of Samples
2.2.1 Capacitance – Voltage (C-V) Measurement…..16
2.2.2 Current Density – Voltage (J-V) Measurement…17
2.2.3 Atomic Force Microscopy (AFM)….... 18
2.2.4 X-ray Photoelectron Spectrometry (XPS)….... 19
2.2.5 Spectrum Ellipsometer…..21

Chapter 3 Experiment Results of MIS Capacitors
3.1 Properties of Single Layer Thin Films…………………………………..… 25
3.1.1 Characteristics of La_2O_3………………………………………………26
3.1.2 Characteristics of Lu_2O_3……………………………………………..… 32
3.1.3 Consideration to Improving Properties
of Single Layers…………………. 38
3.2 Effect of Stack Structure Thin Films……………………………………. 41
3.2.1 Dependence of Annealing Temperature…………………………...….43
3.2.2 Dependence of Physical Thickness……………………….…………..50
3.2.3 Dependence of Deposition Temperature…………………….………..54
3.2.4 Effect of Chemical Oxides……………………………………………56
3.3 Analysis for Interfacial Layer with XPS …………………………. 57
3.4 Discussion……………………………………………………………..58

Chapter 4 Operation Confirmation of Devices
4.1 Electrical Characteristics of n-MISFET …………………………. 61
4.1.1 Characteristics of
Stacked Dielectric Films Transistors………………………. 62
4.1.2 Characteristics of
Single High-k Gate Insulator Transistors…………….……… 65
4.2 Discussion……………………………………………………………..66

Chapter 5 Conclusions
5.1 Results of This Study…………………………………………….…..... 68
5.2 Future Issues…………………………………………………………... 70

References
Acknowledgements
Appendix

Chapter 1

Introduction

1.1 Background of This Study

Various high-quality electric products such as the personal computers, digital camera, DVD recorder, mobile phone, and so on are in the life of our personal appearance. IT is also depended on the benefits. The contents of the products are assembled with circuit systems composed with the Large-Scale-Integration (LSI) technology. The LSI technology is progressing with high density and high integration every year. Existence of Metal-Oxide-Semiconductor FET (MOSFET) made from Silicon is indispensable in constituting the LSI circuit system. In order to progress the high density and high integration for the system, downsizing of the MOSFET's physical sizes according to the scaling law is necessary [1]. The device miniaturized by scaling factor "k" is also useful to improvement in switching operation speed from shrinking the channel length, and reduce the power consumption (as shown in Fig 1.1 and Table 1.1). The latest LSI raised capability of the whole performances for this improvement will create the new tips from the LSI circuit systems and will produce better the products. Therefore, the researches for the devices downsizing are very important and has been keeping up beyond centuries.

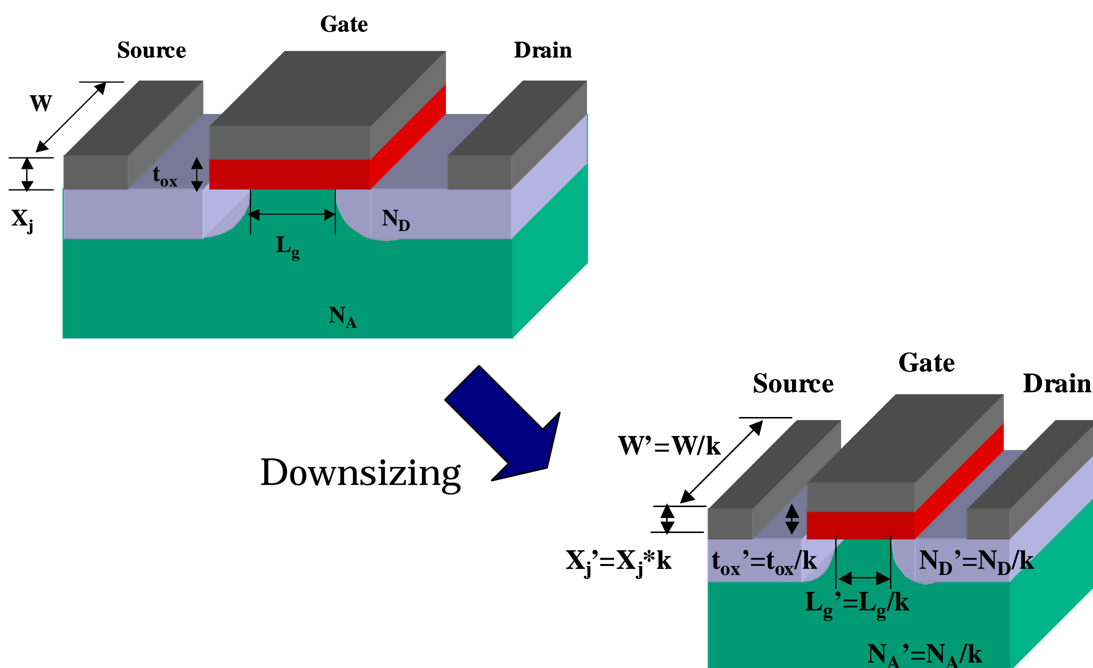


Fig 1.1 Schematic of Scaling Method

Table 1.1 Scaling of MOSFET by the scaling factor of k

Quantity	Before Scaling	After Scaling
Channel Length	L_g	L_g'=L/k
Channel Width	W	W'=W/k
Device Area	A	A'=A/k^2
Gate Oxide Thicknes	t_{ox}	T_{ox}'=t_{ox}/k
Gate Capacitance per Unit Area	C_{ox}	C_{ox}'=k*C_{ox}
Junction Depth	X_j	X_j'=k*X_j
Power Supply Voltage	V_{DD}	V_{DD}'=V_{DD}/k
Threshold Voltage	V_{th}	V_{th}'=V_{th}/k
Doping Densities	N_A	N_A'=k*N_A
	N_D	N_D'=k*N_D

Improving the insulators of the gate dielectric films for MOSFET is greatly concerned with the whole devices performances. However, MOSFET has some problems that are able not to minimize more than now by manufacture technologies. Table 1.2 shows the International Roadmap for Semiconductor (ITRS) 2003 edition [2]. According to ITRS, the film thickness becomes 1 nm or less within several years. In such the thin films of SiO_2, increase of the leakage current by the direct tunneling becomes remarkable, and there are serious problem that brings trouble to operation of the devices. There will the increase of the power consumption and degradation of LSI reliability.

Therefore, ITRS requires the replacement of SiO_2 MOSFET gate dielectric materials as a "Grand Challenge" to the historical progression of device down sizing. To reduce the leakage current, the physical thickness of gate insulator should be kept large while the capacitance still should increase. This can be accomplished by the use of dielectric materials with high dielectric constant. Typically, for high-k materials, the dielectric constant is in the 10 – 40 range, a factor of approximately 3 – 10 higher than of SiO_2 (k=3.9).

It is anticipated that new materials will be requirement by 90 nm node to provide 0.9 – 1.4 nm Tox electrical equivalent (EOT).

Table 1.2 ITRS 2003 edition

Low Operating Power (LOP) Logic Technology Requirements

Year	2004	2007	2010	2013	2016
MPU Node(nm)	90	65	45	32	22
MPU L_g(nm)	37	25	18	13	9
EOT(nm)	0.8 - 1.5	0.7 - 1.2	0.4 – 0.9	0.4 – 0.8	0.4 – 0.7
Gate Leakage (A/cm^2)	1.89	5.21	11	21	91
V_{dd}(V)	0.9	0.8	0.7	0.6	0.5

Additionally, Physical limits in SiO_2 gate insulators comes now because direct tunneling leakage current is following

$$I \propto \exp\left[-(m\phi)^{1/2} \cdot D\right] \qquad (1)$$

m: electron effective mass ϕ: barrier height from Si D: physical thickness

The direct tunneling current is known that appeared remarkably when total thickness is order of nano meter. The SiO2 thin films only did not prevent from leakage current and not promote below 1 nm. Even if substituted for SiNxOy thin films, this effect has only mere a little. Figure 1.2 shows leakage current vs. EOT plots.

Therefore, high-k alternated to Si is necessary immediately.

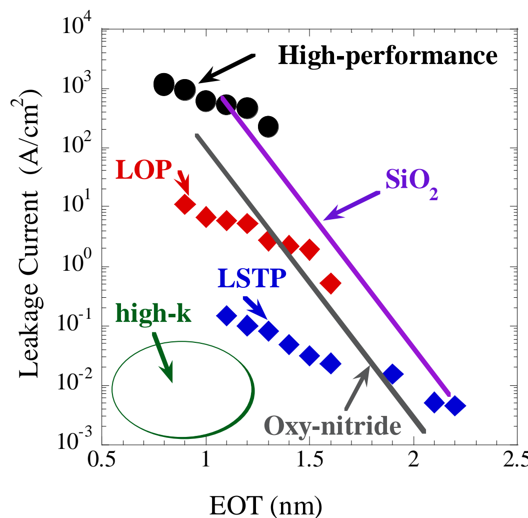


Fig 1.2 Leakage current vs. EOT plots from ITRS 2003 dates

ITRS requires the necessity of the replacement of SiO_2 gate dielectric films by high-k materials, immediately. The requirements for high-k materials are as follows.

(1) Large dielectric constant (k= 10 - 30)

(2) Small leakage current density

(3) Chemically stable at the Si interface at high process temperature (1000K)

(4) Small densities of interface state and fixed charge

(5) High mobility and reliability

Then, thing for which other insulated material (High-k) which changes to SiO_2 is used as one of the means to solve this problem physical thickness is increased maintaining an efficiency-dielectric constant. It can make that a result of leak current decreasing. As the candidate to alternative SiO_2, there are ZrO_2, HfO_2, and Al_2O_3 have been widely studied for next generation materials for gate dielectrics since they have high dielectric constant and wide band gap [3-5]. Rare earth oxide (lanthanide oxides) is also attracting attention in recent years. Recently, excellent results of rare earth oxides, such as La_2O_3, CeO_2, Pr_2O_3, Gd_2O_3, Dy_2O_3 and their silicate have been reported [6-13].

The dielectric constant of Al_2O_3 is about 10, a factor of approximately 2.5 higher than that of SiO_2. And the biggest problem for the Al_2O_3 is that film thickness dependence of flat-band shift due to the fixed charge is so strong that controllability of the flat-band voltage is difficult.

ZrO_2 and HfO_2 become popular materials because their dielectric constants are relatively high and because they were believed to be stable at the Si inerface. However, in reality, formations and growths of interfacial layer made of silicate or SiO_2 at the Si interface and micro-crystal during the thermal process has been a serious problem. Recently, the most serious problems are found to ZrO_2 and HfO_2 that they formed silicide during the thermal process.

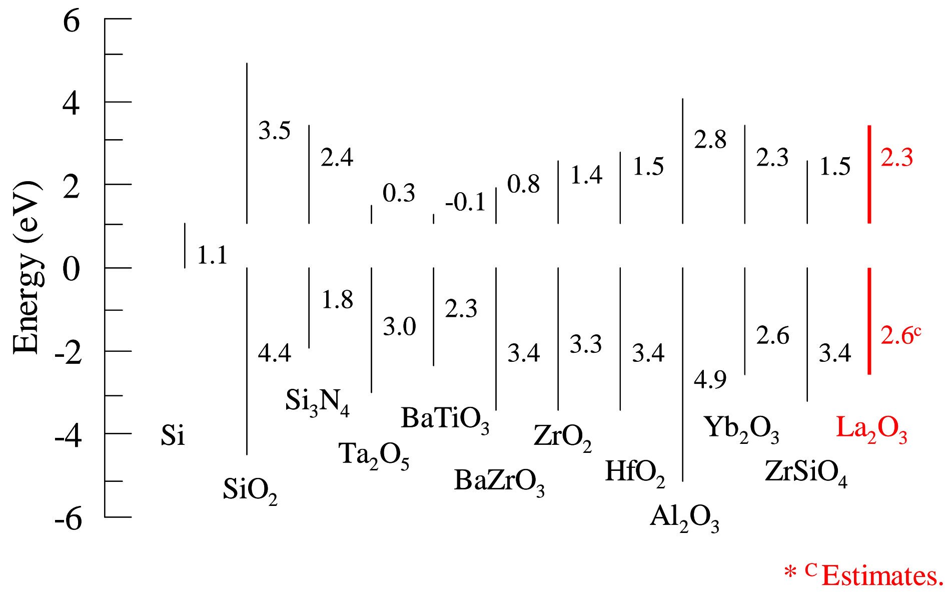


Fig 1.2 Candidates of the elements, which can be used for high-k gate insulators

Table 1.3 The reported high-k materials for gate insulators

Materials	SiO_2	Al_2O_3	La_2O_3	Pr_2O_3	Gd_2O_3	HfO_2	ZrO_2
EOT (nm)	0.8	1.5	0.48	1.4	1.5	0.8	0.8
Contact stability with Si (kJ/mol) $Si+MO_x\text{->}M+SiO_2$	Stable	+63.4	+98.5	+105.8	+101.5	+47.6	+42.3
Lattice energy (kJ/mol)	13125	15916	12687	12938	13330	a b c	11188
Bandgap (eV)	9	6 – 8	5.4	3.9	5.4	5.7	5.2 – 7.8
Structure	Amorphous	Amorphous	Amorphous	Crystal T>700℃	Crystal T>400℃	Crystal T>700℃	Crystal T>400 - 800℃
κ	3.9	8.5 – 10	27	13	17	24	11 – 18.5

1.2 Physical Properties of Rare Earth Oxides

Figure 1.3 shows the periodic table of lanthanide elements, rare earth materials. The number of them is 15, but Pm is an unstable artificial element and should be removed from the candidates. Although, the outer shell electron configurations are the same for quite different. Band gap and lattice energy for lanthanide oxides are shown in , Figure 1.4(a) and (b), respectively. The reported dielectric constants of rare earth oxides are about 10-30, and the energy gap is about 2.4-5.5eV. Lanthanides are called as “rare earth” elements, but it should be noted that are in reality “no rare” in the earth-shell and even their contents are larger than that of Hg, In, Ag, etc. Therefore, there are the materials possible, which can be used from now to future in manufacturing industry.

La^{57}	Ce^{58}	Pr^{59}	Nd^{60}	Sm^{62}	Eu^{63}	Gd^{64}	Tb^{65}	Dy^{66}	Ho^{67}	Er^{68}	Tm^{69}	Yb^{70}	Lu^{71}

Fig1.3 Lanthanide elements

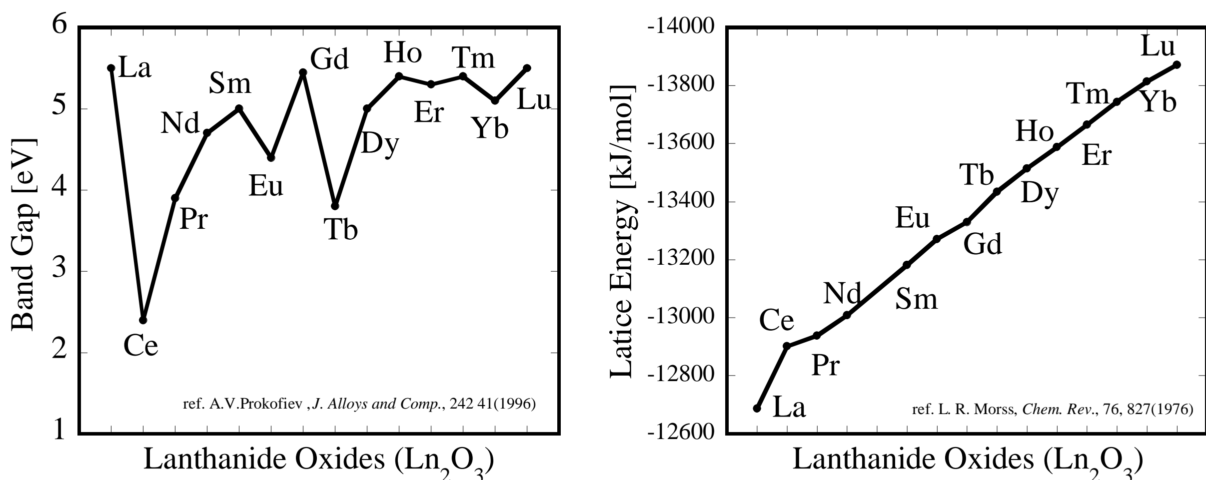


Fig1.4 (a) Band Gap of Rare Earth Oxides (b) Lattice Energy of Rare Earth Oxides

1.3 Purpose of This Study

Generally, the dielectric constant of ZrO_2 or HfO_2 is about 25, respectively. Although researched them is advanced as a near material practical, the growth of an interface layer and silicate, or silicide is anxious about decline in the dielectric constant by heat process. Moreover, increase of leakage currents is also problem caused such as micro crystallization. On the other hand, although rare earth oxides still have a little research, there are known that stable chemically to Si and most of them are maintaining amorphous is acquired in heat treatment. However, rare earth oxides have a hygroscopic and carbonic problem by some research. Especially, La_2O_3, which is one of the most useful in high dielectric constant about 27, is the worse damp-proof material in rare earth oxides (reported, recently [14,15]). Moreover, we are anxious about the reaction with La_2O_3 contacted aluminum as electrode from the latest researches [16,17], and the technique of preventing these is needed.

The purpose of this study is improvement of the electrical characteristics to gate dielectric thin films as stacked insulator (shown as Figure 1.5). Since La_2O_3 is comparatively stables to Si substrate, it is mainly used for films as a buffer layer. Then, Lu_2O_3 is deposited on the top of the La_2O_3 films, which is the highest lattice energy and damp-proof outstanding in lanthanides, and the band gap are closely. These results are summarized to chapter the following.

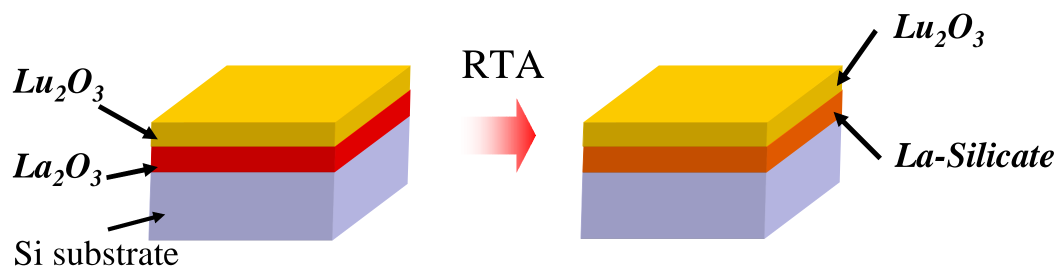


Fig 1.5 Schematic of Stacked thin films

Chapter 2

Fabrication and Characterization Methods

2.1.1 Si Substrate Wet Cleaning

For deposition of high quality thin films, ultra clean Si surface is required, without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination, The theoretical resistivity of pure water at 25°C is 18.25 MΩcm. Ultra-pure water (UPW) systems used in this study provided UPW with more than 18.2 MΩcm resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle (fΦ0.1μm) per milliliter.

In this study, the substrate cleaning process was based on RCA cleaning process, was proposed by W.kern et al. But some steps were reduced. The steps were shown in Fig.2.1. First, a cleaning steps in a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2=4:1) was performed to remove any organic material and metallic impurities. And then, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:100). Finally, the cleaned wafer was dipped in DI water and loaded to chamber immediately.

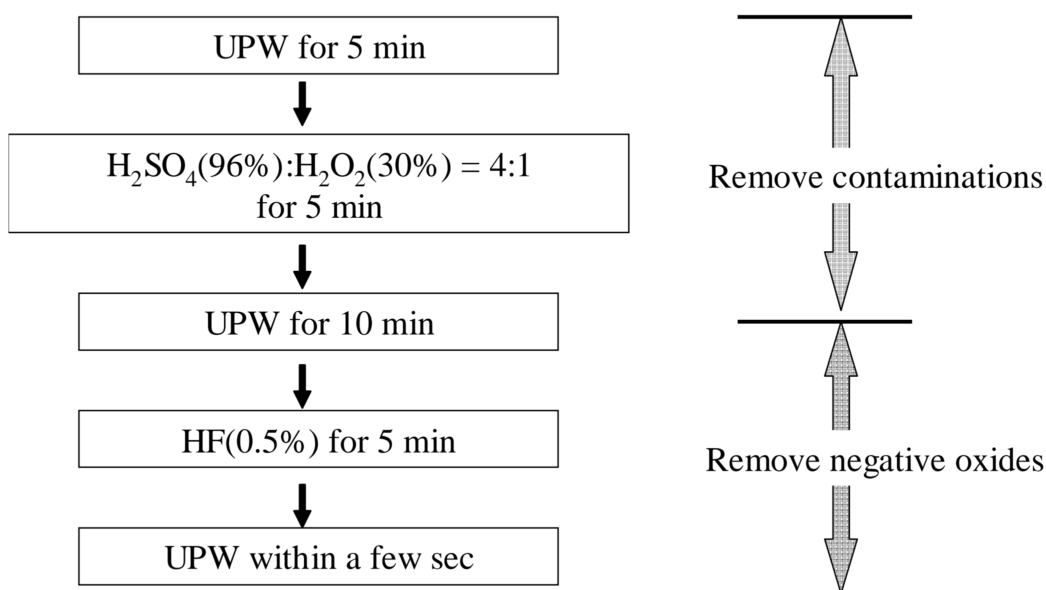


Fig 2.1 Cleaning process of Si substrate

2.1.2 Si Substrate Wet Cleaning

In order to reduce leakage current and interfacial layer, chemical oxidation on Si surface is attempted. In this study, Oxidation method is used by dipping 30% H_2O_2 that seem to make suitable oxide layer and oxidation rate is 0.7nm by 30min at room temperature.

After cleaning process, Si substrate was dipped in H_2O_2 and then substrate was dipped in DI water and load to chamber immediately. The steps were shown in Fig.2.2.

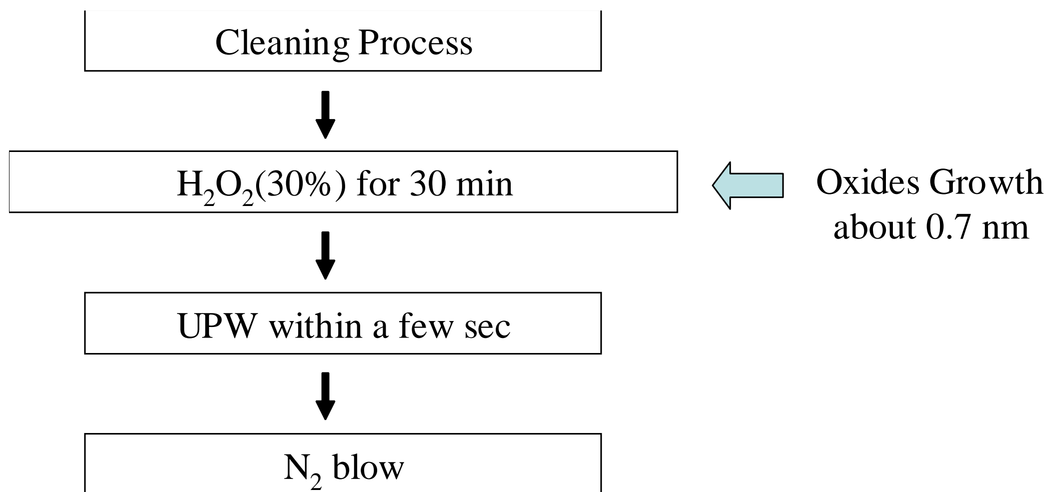


Fig 2.2 Cleaning process of Si substrate

2.1.3 Molecular Beam Deposition (MBE) Process

MBD method is one of the PVD (physical vapor Deposition) methods using molecular beam epitaxy (MBE) system. The material is evaporated by using E-beam and deposited on Si substrate. Only molecular beam is used for depositing in ultra high vacuum (~10^{10} Torr). This method prevents contaminants in film that C-VD method has and provides controllable nanometer order thin films. This method is suitable for research basic characteristics of high-k thin films.

Figure 2.3 and Fig.2.4 shows MBE system, which was used in this study. There are two chambers and four pumps to make ultra high vacuum, four E-guns in deposition chamber and two power supplies that are capable to evaporate two materials in the same time. (Not use plural E-guns in this study.) And there are crystal meter for measurements thickness and RHEED for Analysis.

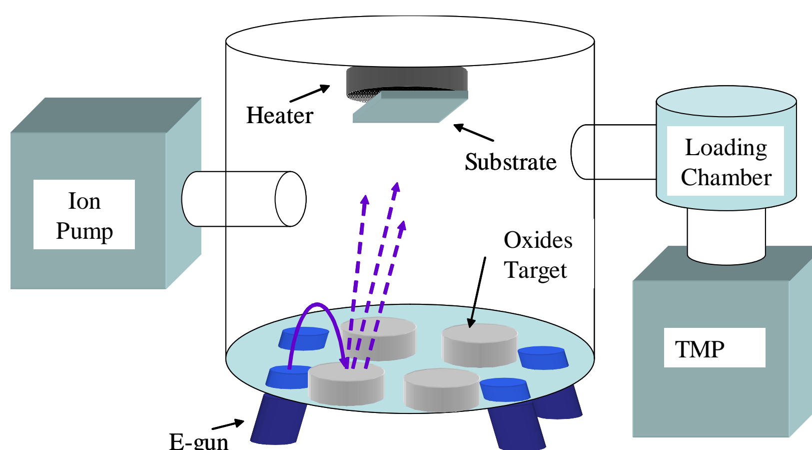


Fig2.3 Schematic of the MBE System

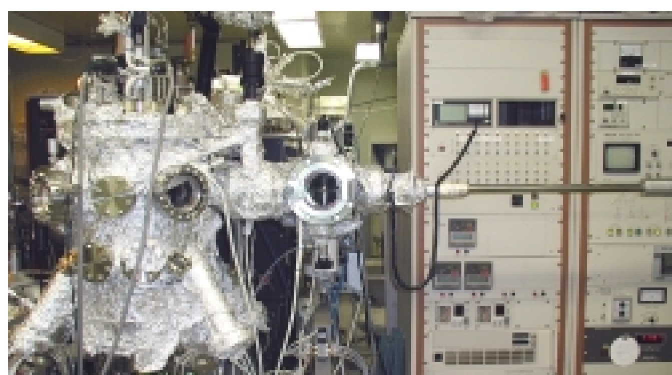


Fig2.4 Photo of the MBE system

2.1.4 Rapid Thermal Annealing (RTA)

In this study, RTA (rapid thermal annealing) is used for thermal process after depositing process. The silica tube filled O_2 or N_2 (flow rate are 1.2 L/min) in atmospheric pressure. Therefore it is impossible to remove contaminant gas perfectly in tube. Equipment image was show in Fig.2.5.

Fig2.5 RTA (MILA3000 made in SNKU-RIKO company)

2.1.5 Vacuum Evaporation Method

High-vacuum evaporation was simple method for forming metal electrode like Pt, Al and Ag. In high vacuum chamber, metal source is evaporated by thermal heating with high voltage and is deposited on substrate covered metal mask. In this study, tungsten electrical resister is used for heating Al source that has low melting point (660.37°C) in case by n type substrate and Ag source (961.93°C). This method is possible to contaminate films. Equipment image was show in Fig.2.6 and Fig 2.7(Photo).

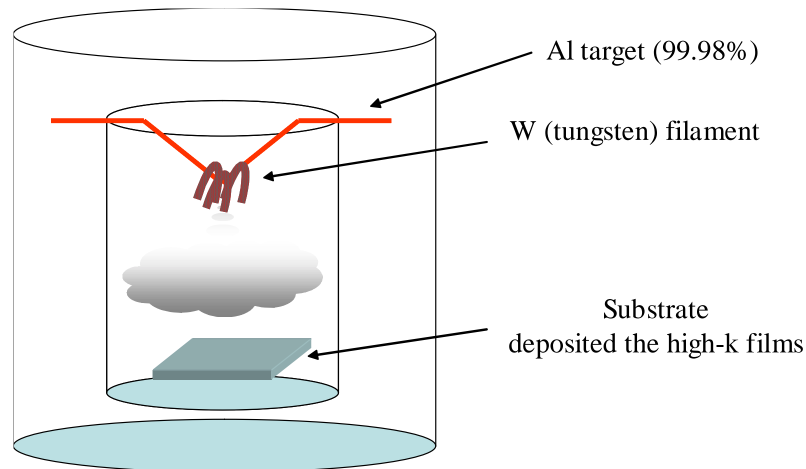


Fig2.6 Metal electrode deposition

Fig2.7 High-vacuum bell jar for metal deposition

2.1.6 Transistor (n-MISFET) process

In this study, the transistor is using n-channel Metal-Insulator-Silicon Field Effect Transistor (n-MISFET). The fabrication process is the identical to n-MIS Capacitor until Al electrode deposition. After photo process is carried out, the gate or source and drain are generated through wet processes as etching. Finally, Al is left from Si substrate as lift-off with Supersonic wave (SSW). Figure 2.8 shows n-MISFET process flow. The photo process flow is shown Figure 2.9.

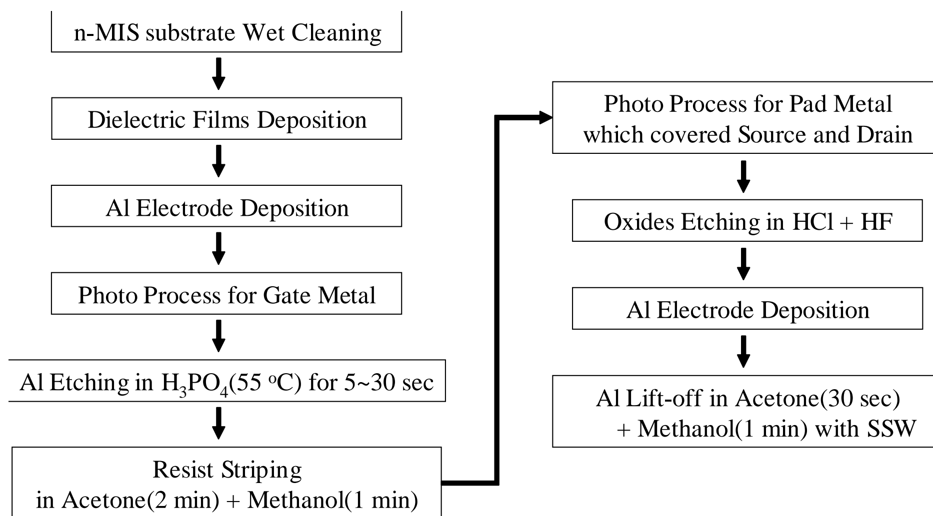


Fig2.8 n-MISFET process flow

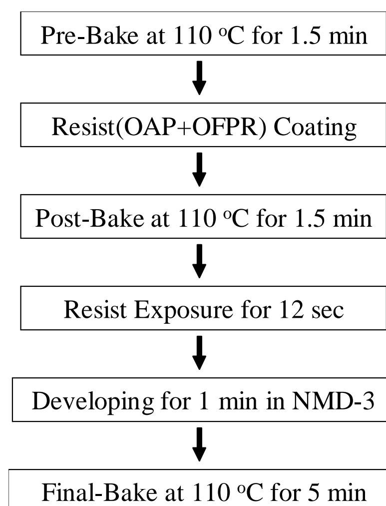


Fig2.9 Photo process flow

2.2.1 C-V Measurement

In this study, 4284A precision LCR meter made by HP measured C-V characteristics. Measurement frequency was 1 kHz~1MHz. Figure 2.10 shows the photo in front of LCR meter equipment.

Fig 2.10 LCR meter HP 4284A.

2.2.2 J-V measurement

The one of important electrical properties to estimate high-k films is I-V characteristics. I-V characteristics were measured to evaluate leakage current characteristics. Measurement range were 10^{-14} A ~ 0.4 A. 4156C type precision semiconductor parameter analyzer made by HP measured them.

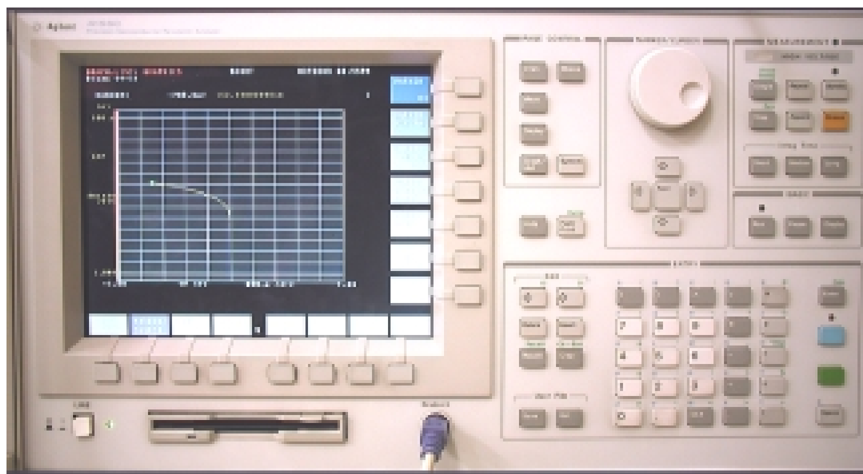


Fig 2.11 Semiconductor parameter analyzer HP 4156C

2.2.3 Atomic Force Microscopy (AFM)

AFM enables to measure surface morphology by utilizing force between atoms and approached tip. The roughness of sample surface is observed precisely by measurement of x-y plane and z. Fig.2.12 shows the principle of AFM.

Tip is vibrated during measurement, and displacement of z direction is detected. This method is called tapping mode AFM (TM-AFM). Resolution limit for normal AFM is 5 ~ 10nm depending on distance between sample surface and tip. On the other hand, resolution limit for TM-AFM is depended on size of tip edge. Thus, resolution limit for TM-AFM is about 1nm.

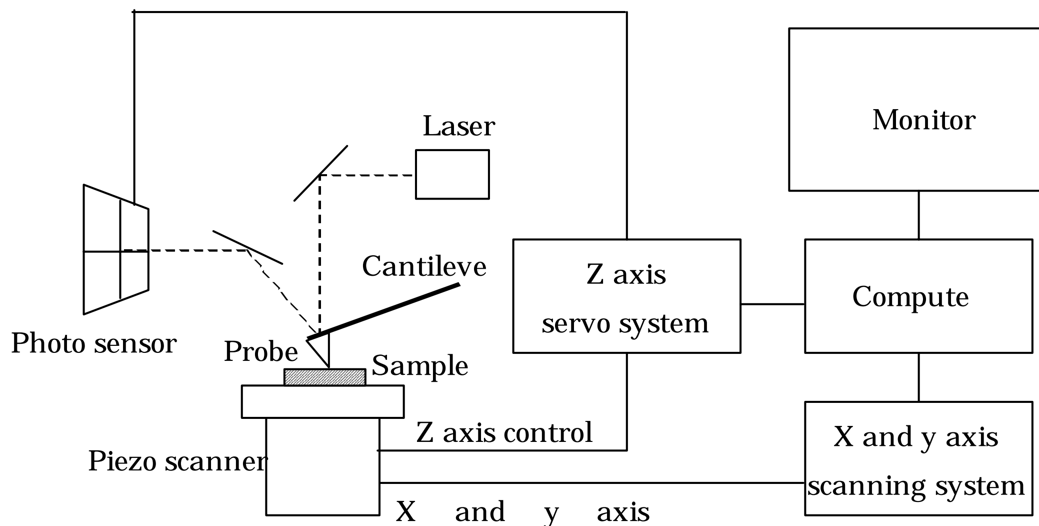


Fig.2.12 Principle of AFM

2.2.4 X-ray Photoelectron Spectroscopy (XPS)

XPS, also known as Electron spectroscopy for chemical analysis (ESCA) is one of the availability methods that estimate thin film and Si interface.

Fig.2.13 shows the schematic drawing of XPS equipment that was used in this study. During analysis, the pressures of main chamber were about 10^{-9} Torr vacuums with turbo pomp. Surface analysis by XPS is accomplished by irradiating a sample with monoenergetic soft X-ray and analyzing the energy of the detected electrons. Non-monochromatic MgKα (1253.6 eV) X-ray is used in this study. The method is illustrated with the energy band diagram in Fig.2.14. This photoelectron has limited penetrating power in a solid on the order of 1-10 μm. They interact with atoms in the surface region, causing electrons to be emitted by the photoelectric effect. The emitted electrons have measured kinetic energies given by

$$KE = h\nu - BE - \phi_s \qquad (2.1)$$

where hυ is the energy of the photoelectron, BE is the binding energy of the atomic orbital from which the electron originates and ϕs is the spectrometer work function (4.8 eV).
The binding energy may be regarded as the energy difference between the initial and final states of the ion from each type of atom, there is a corresponding variety of kinetic energies of the emitted electron. Because each element has a unique set of binding energies, XPS can be used to identify and determine the concentration of the elements in the surface. Variation in the elemental binding energies (Chemical shift) arises from difference in the chemical potential and polarizability of compounds. These chemical shifts can be used to identify the chemical states of the materials being analyzed.

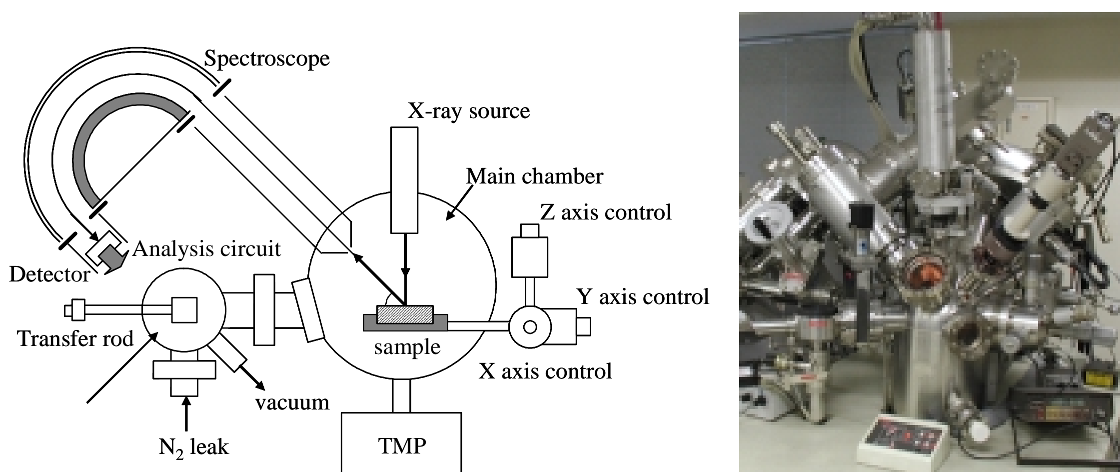


Fig. 2.13 XPS schematic, physical electronics PHI5600 ESCA spectrometer

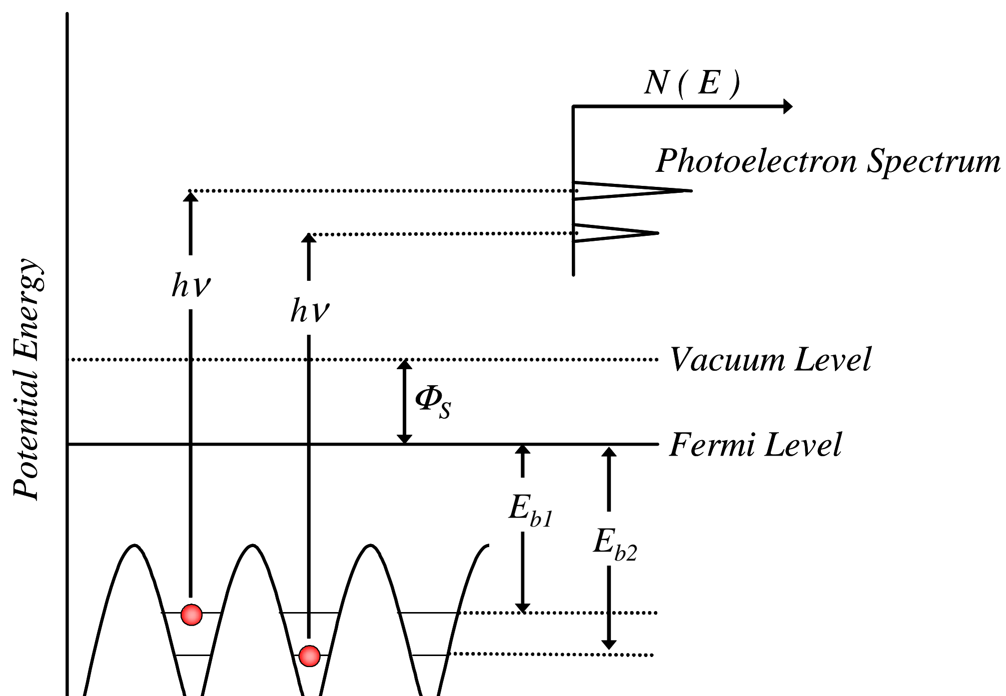


Fig. 2.14 Illustration of measurement method with the energy band diagram

2.2.5 Ellipsometer

Ellipsometory is the method to estimate the optical property of material or surface film thickness measuring the change of polarization condition caused by the reflection of light. Generally, when light is illuminated to a material, the polarization condition of incident light and reflected light are different. This method evaluates the surface condition from this difference. P component of polarized light is horizontal to the plane formed by incident and reflected light and vertical component is S. Ordinary non-polarized light becomes linear polarized light in which the phase and intensity are the same between P and S polarization component when it was passed through 45°-declined polarizer. When the linear polarized light is illuminated to the material, phase different Δ arises between P and S component in the reflected light. Also, the reflection intensity is different between P and S component of polarized light because the reflectance of P and S component is different at the material surface (Fig. 2.15).

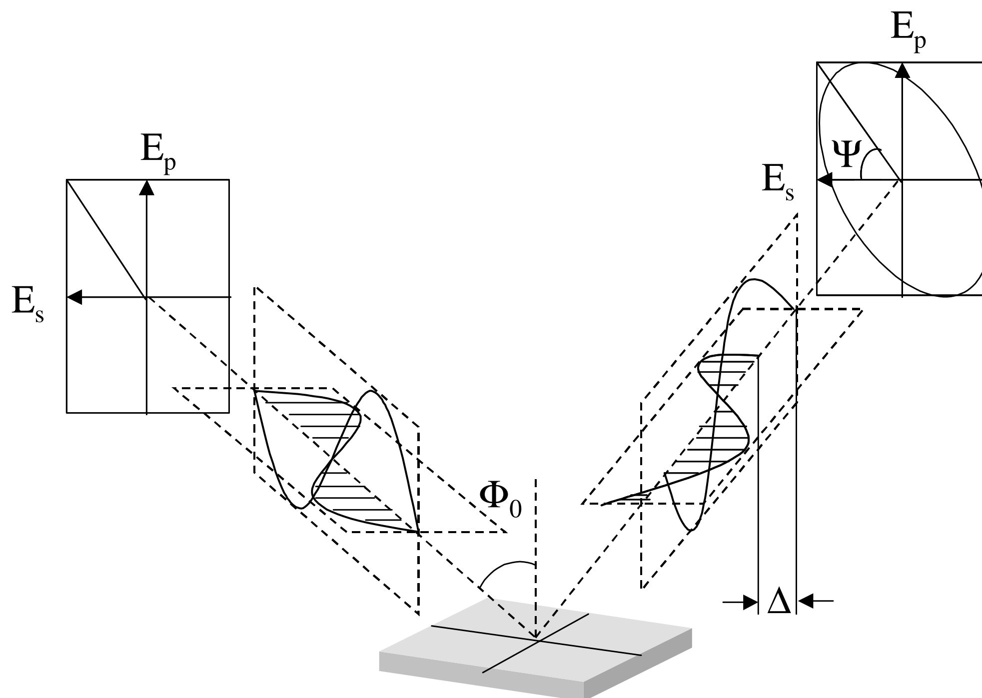


Fig. 2.15 Illustration of the measurement principle for ellipsometer

P and S component in electric field vector of the reflected light are given by

$$E_p = a_p \cos(\omega t - \delta_p)$$
$$E_s = a_s \cos(\omega t - \delta_s) \qquad (2.1)$$

Here, a_p, a_s, are amplitudes of P and S direction respectively. δ_p and δ_s express the phase deviations in the each component. Introducing the relation $\delta_p - \delta_s = \Delta$, the following equation is obtained.

$$\frac{E_p^{\ 2}}{a_p^{\ 2}} + \frac{E_s^{\ 2}}{a_s^{\ 2}} - 2\frac{E_p}{a_p}\frac{E_s}{a_s}\cos\Delta = \sin^2\Delta \qquad (2.2)$$

This equation expresses ellipse in general. The condition of elliptically polarized light is determined by the relative phase difference Δ and reflection amplitude ratio. Taking the tangent, reflection amplitude ration is expressed as reflection amplitude angle ψ. Ellipsometer measures and determines Δ and Ψ or $\cos\Delta$ and $\tan\Psi$.

Following system is assumed for the typical measurement. The system consists of ambient, thin film, and substrate.

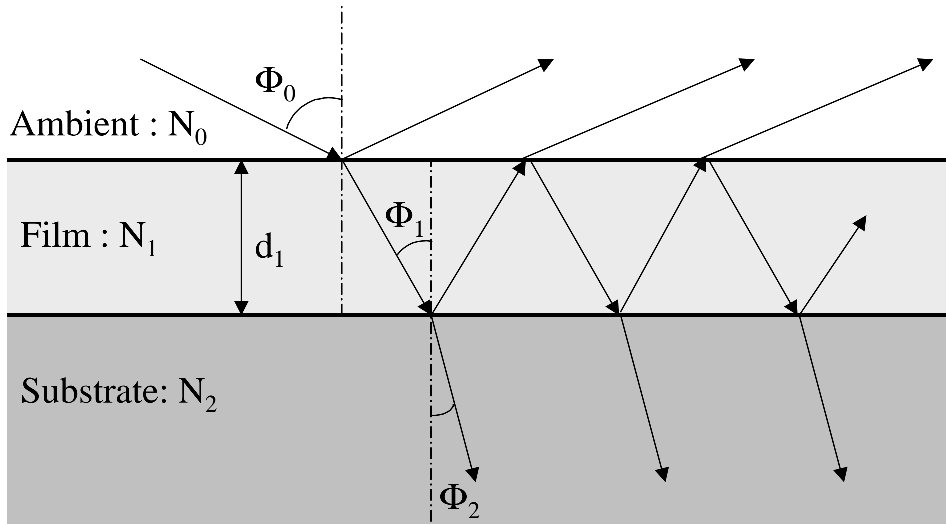


Fig. 2.16 System of three layers for typical measurement

The relation between reflectance ratio in P, S component of polarized light and ellipso parameter is expressed as

$$\tan\Psi e^{j\Delta} = \frac{R_p}{R_s} \tag{2.3}$$

Here, Rp and Rs are complex reflection constant (Fresnel constant). Giving complex refraction $N_i = n_i - jk_i$, Fresnel constant at the each interface is given by

$$r_{i,i+1p} = \frac{N_i \cos\Phi_{i-1} - N_{i-1}\cos\Phi_i}{N_i \cos\Phi_{i-1} + N_{i-1}\cos\Phi_i}$$
$$r_{i,i+1s} = \frac{N_{i-1} \cos\Phi_{i-1} - N_i\cos\Phi_i}{N_{i-1} \cos\Phi_{i-1} + N_i\cos\Phi_i} \tag{2.4}$$

The phase angle β_i in the i layer film is

$$\beta_i = 2\pi\left(\frac{d_i}{\lambda}\right)N_i \cos\Phi_i \tag{2.5}$$

Here, d_i is film thickness, λ is wavelength of incident light and φ_i is incident angle in the i layer. Using these parameter,

$$R_p = \frac{r_{o1p} + r_{12p}e^{-j2\beta_1}}{1 + r_{o1p}r_{12p}e^{-j2\beta_1}}$$
$$R_s = \frac{r_{o1s} + r_{12s}e^{-j2\beta_1}}{1 + r_{o1s}r_{12s}e^{-j2\beta_1}} \tag{2.6}$$

Therefore, if complex refraction in each layer, incident angle and wavelength of light at measurement are known, film thickness can be calculated by measuring ellipso parameter.

Chapter 3

Experiment Results of MIS Capacitors

3.1 Properties of Single Layer Thin Films

The electrical characteristics of the thin films were evaluated by using Metal-Insulator-Semiconductor (MIS) capacitor. The fabrication flow of MIS structure for single layer as insulator is showed in Fig. 3.1.

First, n-Si substrate was cleaning in wet process. Next, the rare earth oxides were deposited on the Si by the MBE system. Then, post annealing was executed with RTA for 5 min. Finally, Al electrodes were deposited for contact.

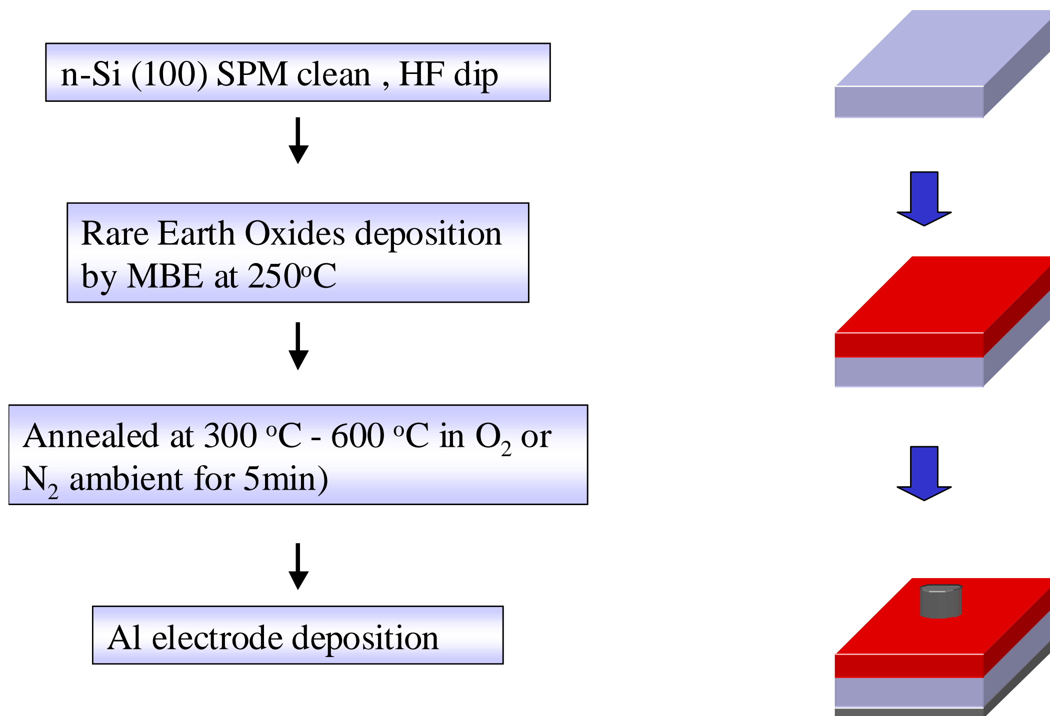


Fig 3.1 Process Flow for MIS capacitor

3.1.1 Characteristics of La_2O_3

Lanthanum Oxide (La_2O_3) is one of the materials with the largest band gap (5.5eV) in rare earth oxide. The lattice energy is the lowest (–12687 kJ/mol). There were shown in Figure 3.2. The dielectric constant of La_2O_3 was reported 27, which is expected to be the closest to practical use in rare earth oxides. Although HfO_2 and ZrO_2 were crystallizing at about 700 °C and 400 to 800 °C, respectively, La_2O_3 like to not be crystallizing for heat process and stable condition to Si. But La_2O_3 has also a problem in moisture resistance. Table 3.1 shows that kind of crystal structure if crystallizing La_2O_3. It has two structure types, which are hexagonal and cubic.

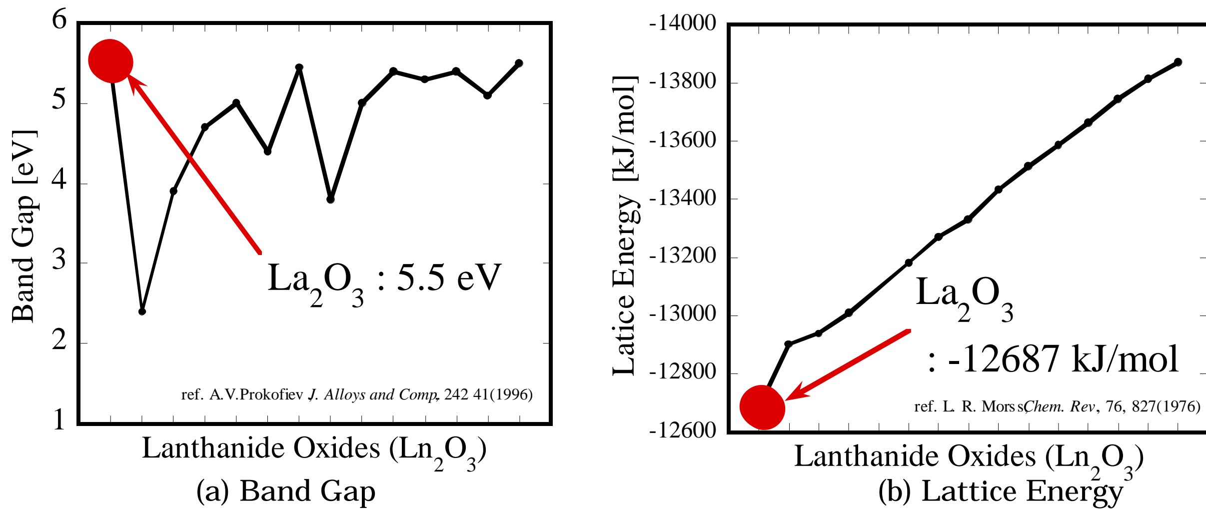


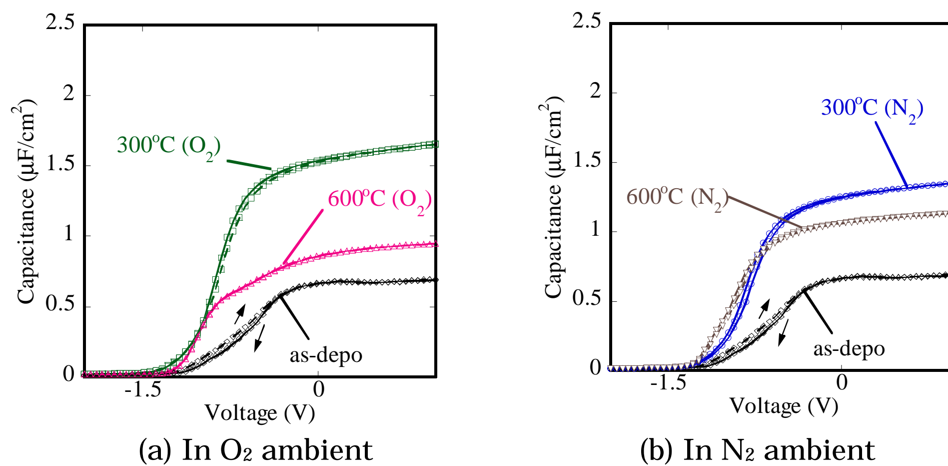
Fig 3.2 Properties of La_2O_3

Table3.1 Crystal structure of La_2O_3

Crystal Structure	Lattice Constant			Axis Angle
	a (nm)	b (nm)	c (nm)	β (°)
hexagonal	0.3937	=a	0.6129	=α=90 ,γ=120
cubic	1.0391±0.0005			=α=γ=90

The first, the electrical characteristics for the annealing condition was investigated for about 4 nm-thick La_2O_3. This was deposited at 250 °C by MBE.

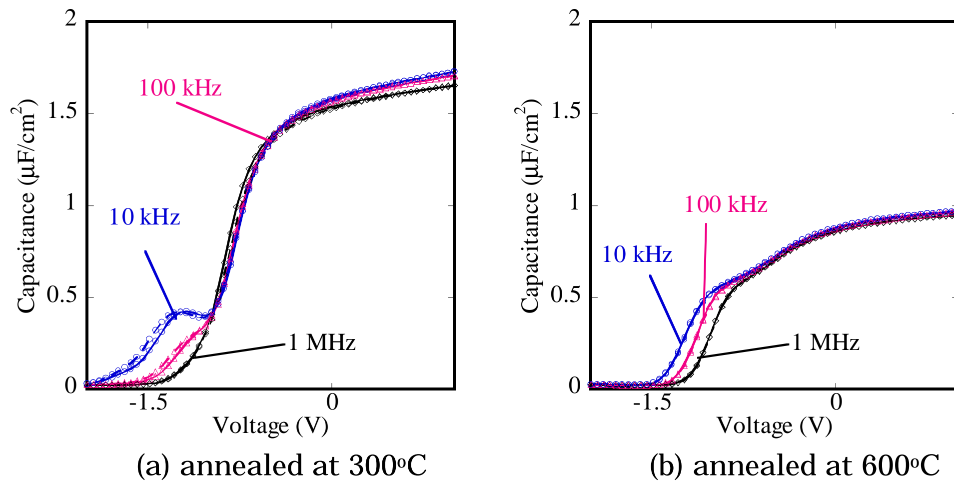
Figure 3.3 shows C-V characteristics with annealing temperature as a parameter, the annealing in both of O_2 and N_2 ambient and annealing time was 5 min. The measurement frequency was 1 MHz. The as-deposited film was observed a little hysterisis. Although as-deposited film was small capacitance in accumulation region, annealed films were higher capacitor and than as-deposited. Moreover, the hysterisis that the as-deposited film has, it was disappeared after 300 °C annealing. As Al electrode for n-Si, ideal flat band voltage is about –0.2 V, however the flat band voltage of these samples calculated from C-V curve were about –1.2 V, similarly. Their negative flat band shift was about 1 V. It was considered that a lot of positive fixed charges exist at the interface. The decrease of accumulation capacitance from 300 °C to 600 °C-annealed films in N_2 ambient was small compare to annealed films in O_2 ambient. This result was considered because of the growth low dielectric interfacial layer during the annealing, and the films in O_2 ambient were more affected than in N_2 ambient due to reaction of oxygen and silicon. The EOT of as-deposited films was 4.48 nm. The annealed films at 300 °C and 600 °C in O_2 ambient were 1.79 nm and 3.43 nm, respectively. On the other hand, the annealed films at 300 °C and 600 °C in N_2 ambient were 2.25 nm and 2.72 nm, respectively. The film annealed at 300 °C in O_2 ambient was most optimized for capacitance in this result.



(a) In O_2 ambient (b) In N_2 ambient

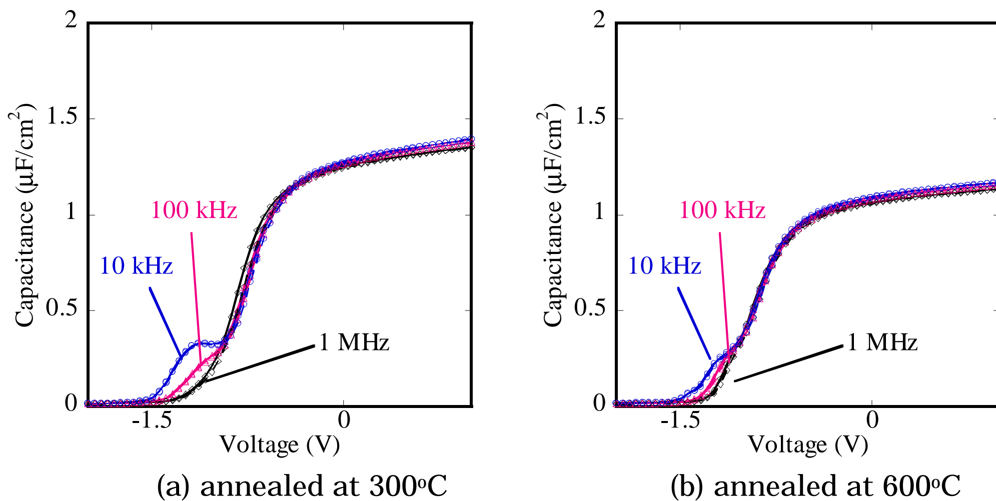
Fig3.3 C- V characteristics with annealing temperature as a parameter (measured by 1 MHz)

Figure 3.4 shows C-V characteristics for the films annealed at 300 °C and 600 °C in O_2 ambient with frequency as a parameter. The measurement frequencies were 1 MHz, 100kHz and 10k Hz. In case of N_2 ambient, which were shown Figure 3.5. It observed that films annealed at 300 °C in both O_2 ambient and N_2 ambient were similar frequency dependence at depletion regions. However, at 600 °C annealing films were different in the point of depletion regions. The case of N_2 ambient was a little frequency dependence, but the case of O_2 ambient was a lot of frequency dependence. This result was considered that in O_2 ambient annealing films was tender to growth of interfacial layer of SiO_2-rich than in N_2 ambient. Therefore, there are a lot of interfacial traps in O_2 ambient annealing.



(a) annealed at 300°C (b) annealed at 600°C

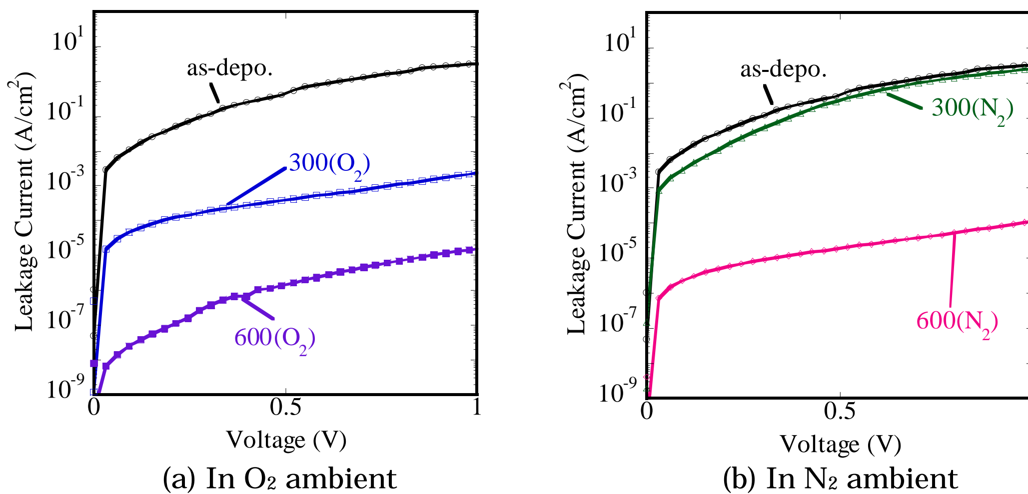
Fig3.4 C-V characteristics with frequency as a parameter in O_2 ambient



(a) annealed at 300°C (b) annealed at 600°C

Fig3.5 C-V characteristics with frequency as a parameter in N_2 ambient

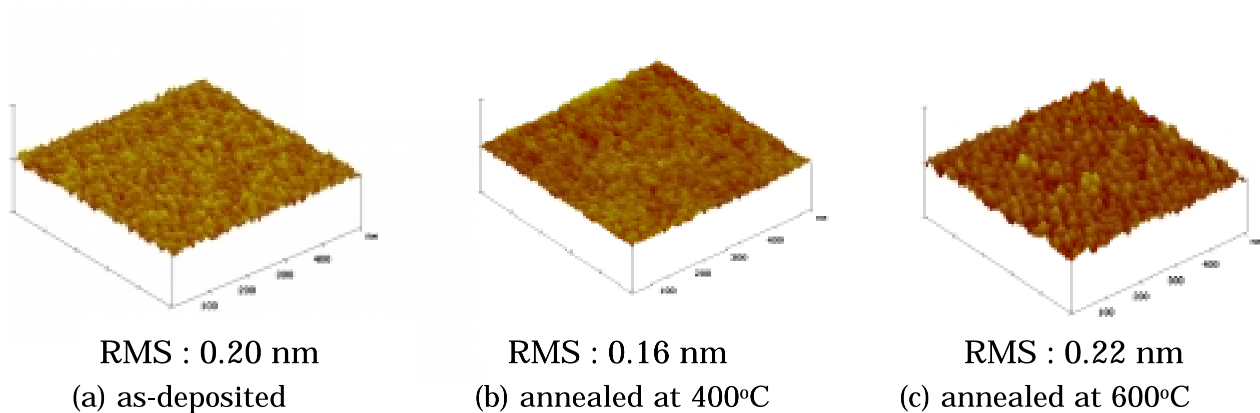
Figure 3.6 shows J-V characteristics for dependence of annealing temperature in O_2 ambient and N_2 ambient. More increase of annealing temperature, leakage current densities was more decrease significantly in O_2 ambient. However, the leakage current of 300 °C-annealing films was hardly different to as-deposited in N_2 ambient. The leakage current of 600 °C-annealing films was decreased more than 6 orders magnitudes from that of as-deposited in N_2 ambient. This result was consider that interfacial layer growth was a little for 300 °C annealing in N_2 ambient.



(a) In O_2 ambient (b) In N_2 ambient

Fig 3.6 J-V characteristics with annealing temperature as a parameter

Figure 3.7 shows the 3D-AFM images of surface morphologies for the films before and after RTA in O_2 ambient. The scan size was 500 x 500 nm and the z direction was 5 nm/div. Their surfaces were observed smooth less about 0.2 nm. In other word, the transformation of surface roughness for about 4 nm thick films annealed in O_2 ambient until 600°C, is not existing at all. Therefore, it was considered that crystallization of the La_2O_3 films was not appeared until at 600 °C annealing for 4 nm thicknesses. The root mean square (RMS) of as-deposited film, annealed films at 400°C and at 600°C was 0.20 nm, 0.16 nm and 0.22 nm, respectively.



RMS : 0.20 nm (a) as-deposited

RMS : 0.16 nm (b) annealed at 400°C

RMS : 0.22 nm (c) annealed at 600°C

Fig 3.12 AFM images of the surface morphologies for La_2O_3 films annealed in O_2 ambient for 5 min (500 x 500 nm, Z: 5 nm/div)

Figure 3.13 shows the wide scan spectrum for the 4nm-thick La_2O_3 film after RTA at 600°C in O_2 ambient by the XPS measurement. The measurement take-off angles (θ) were 30°, 45° and 60°. Higher the number of the take-off angle, closer the distance into Si substrate. This spectrum was confirmed that the spectrum of La-4d, La-4p, C-1s, O-1s and La3d are appeared mainly from low binding energy for each angles.

The narrow scan spectrum for the films before and after 600°C annealing in O_2 ambient were shown Figure 3.14 and Figure 3.15, respectively. The Si-2s spectrums were normalized at 151 eV for Si-Si binding peaks. Although peaks except the peak at 151 eV are hardly seen in Si-2s spectrum region before RTA, the peak at high-energy side from Si-Si binding peaks was appeared after RTA. It seems that the interfacial layer was grown upward top of the film gradually, since bigger take-off angle higher the peak of the layer if the interfacial layer were grown uniformly. In O-1s spectrum, the transformation of the peak was observed after RTA compare to that before RTA. This transformation is chemical shift that the peak at low-energy side moves to high-energy side. This means that the low binding such as La-O binding combine with another atoms such as Si and changes to high binding such as La-O-Si. On the other hand, the La-$3d_{3/2}$ spectrum after RTA was almost similar to that before RTA. These results were considered that the 4 nm-thick La_2O_3 films changes to silicate upward top of the films gradually after RTA.

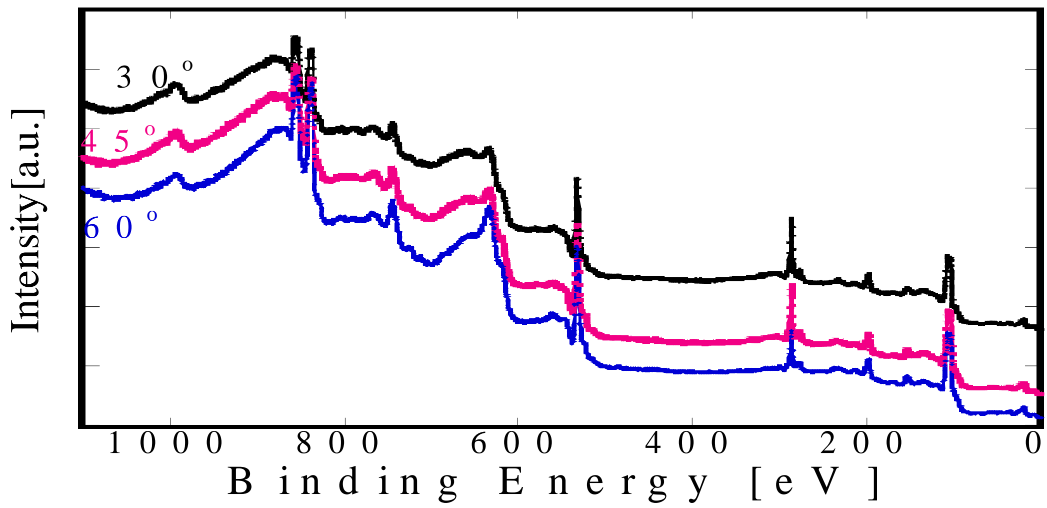
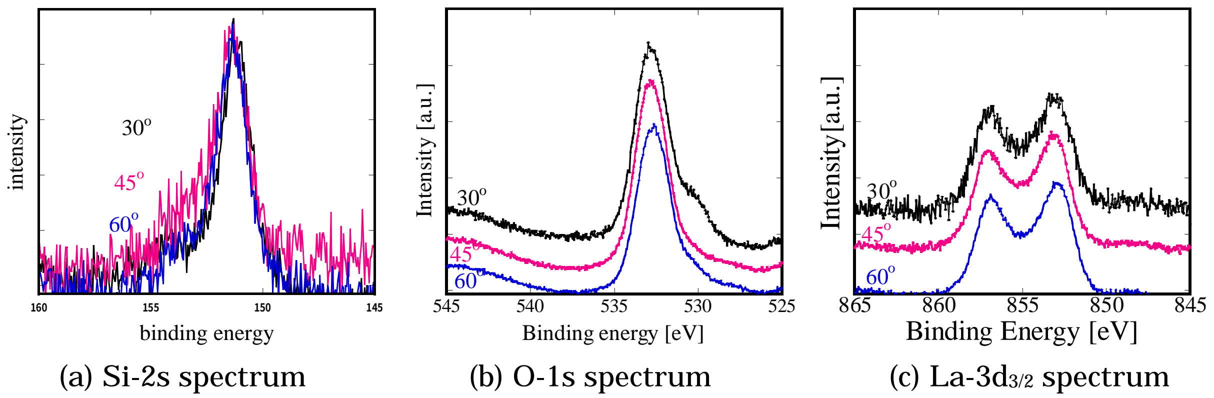
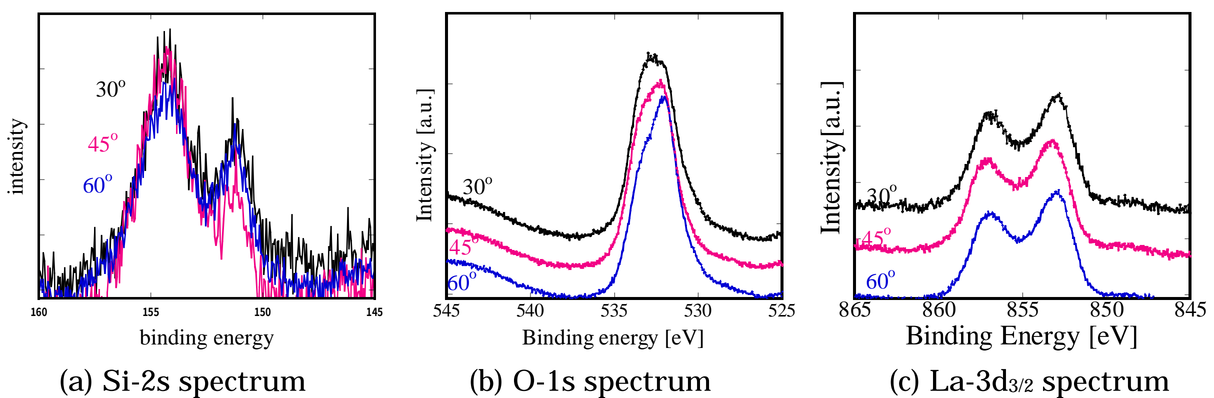


Fig 3.13 the wide spectrum of 4 nm-thick La_2O_3 films from 0 to 1100 eV after RTA in O_2 ambient



(a) Si-2s spectrum (b) O-1s spectrum (c) La-$3d_{3/2}$ spectrum

Fig 3.14 the narrow spectrums of 4 nm-thick La_2O_3 films before RTA



(a) Si-2s spectrum (b) O-1s spectrum (c) La-$3d_{3/2}$ spectrum

Fig 3.15 the narrow spectrums of 4 nm-thick La_2O_3 films after RTA in O_2 ambient

3.1.2 Characteristics of Lu_2O_3

Lutetium Oxide (Lu_2O_3) is one of the materials with the largest band gap (5.5eV) in rare earth oxide as well as La_2O_3. On the contrary to La_2O_3, the lattice energy of Lu_2O_3 is the highest (–1387 kJ/mol). There were shown in Figure 3.16. This means that Lu_2O_3 seems suspiciously to have a problem of micro crystallization by heat process as HfO_2 and ZrO_2 were crystallizing at about 700 °C and 400 to 800 °C, respectively. However, the point excellent in moisture resistance, which is one of the Lu_2O_3 characteristics in rare earth oxides, attracts attention. Although the dielectric constant of Lu_2O_3 is lower than that of La_2O_3, reported 12.5, it is necessary to research more. Table 3.2 shows that kind of crystal structure if crystallizing Lu_2O_3. It has two structure types, which are monoclinic and cubic.

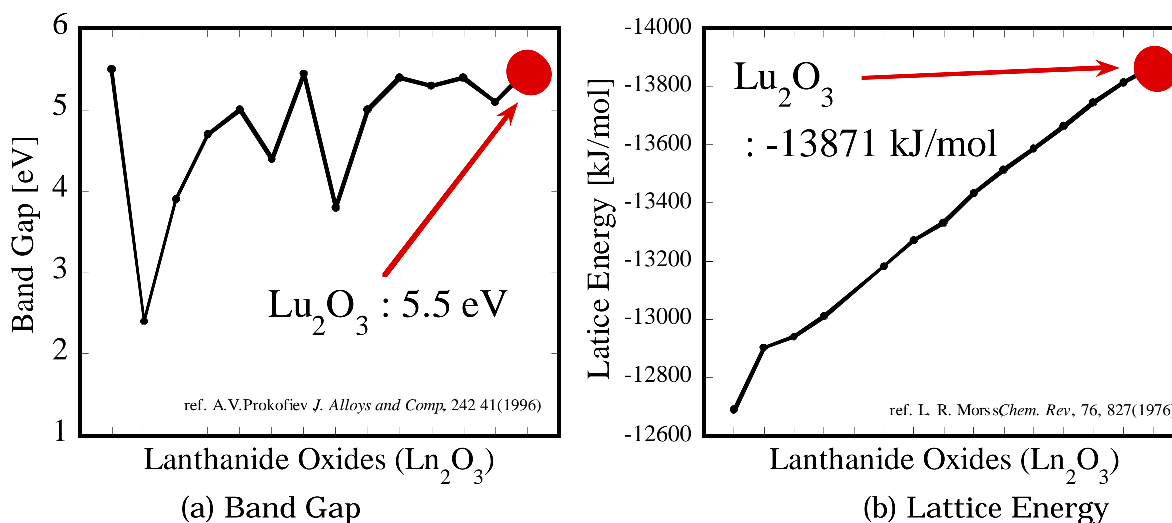


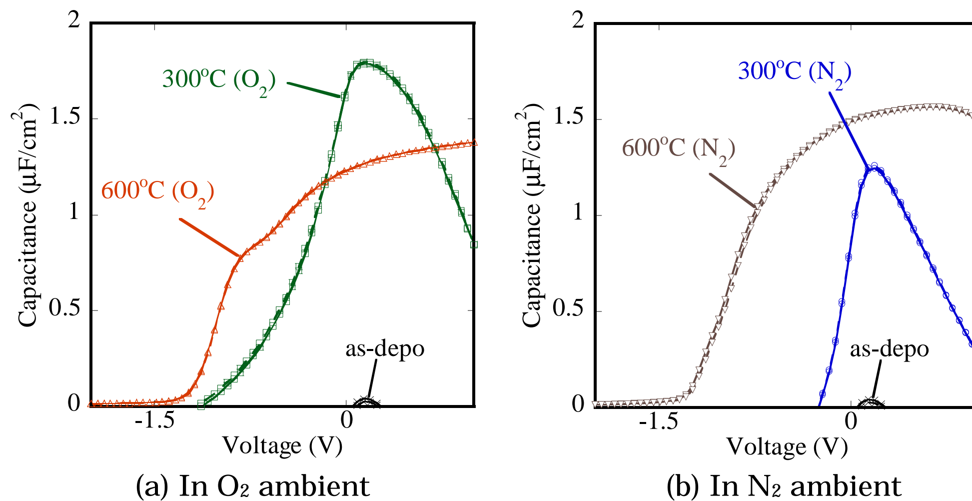
Fig 3.16 Properties of Lu_2O_3

Table3.2 characteristics of Lu_2O_3

Crystal Structure	Lattice Constant			Axis Angle
	a (nm)	b (nm)	c (nm)	β (°)
monoclinic	1.370±0.001	0.3410±0.0003	0.8425±0.0008	100.22±0.0005
cubic	1.0391±0.0005			=α=γ=90

In the reported results, the leakage currents of Lu_2O_3 films could not be suppressed compare to other dielectric films in rare earth oxides due to crystallizations. But it was results that the thickness is more than 10 nm. This study is that the electrical characteristic for the annealing condition was investigated for about 4 nm-thick Lu_2O_3. This was deposited at 250 ^oC by MBE.

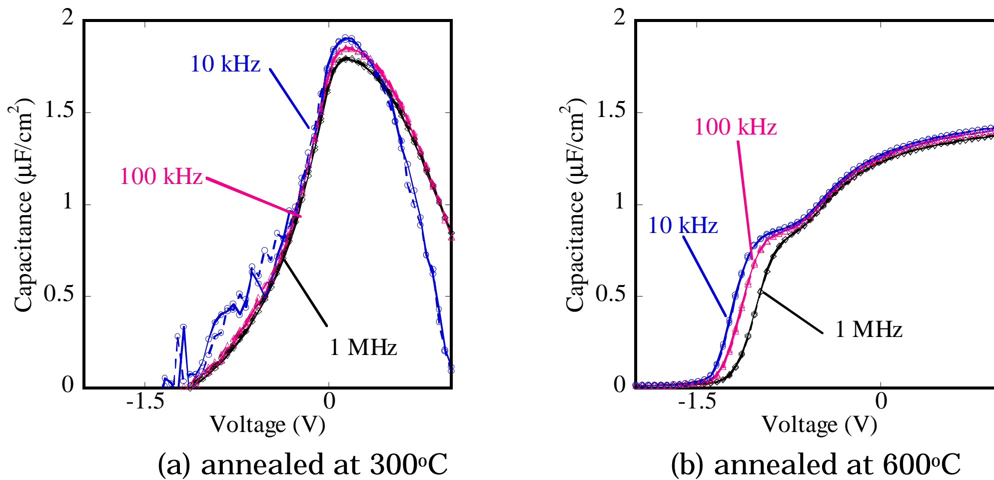
Figure 3.17 shows C-V characteristics with annealing temperature as a parameter, the annealing in both of O_2 and N_2 ambient and annealing time was 5 min. The measurement frequency was 1 MHz. The as-deposited film was not observed C-V characteristics. Although the C-V characteristics for the films after 300 ^oC annealing was appeared, the C-V curve was not useful at all in both of O_2 and N_2 ambient. After 600 ^oC annealing, the C-V curve was a little utility. In other word, after 600 ^oC annealing the films was improved. This result was considered that the growth low dielectric interfacial layer such as SiO_2 during the annealing, and the films could be store the charge for C-V curve. Additionally, it was observed that charge trap from accumulation region to depletion region in O_2 ambient. The flat band voltage of these samples was similar to that of La_2O_3, their negative flat band shift was about 1 V. It was considered that a lot of positive fixed charges exist at the interface. The annealed films at and 600 ^oC in O_2 and N_2 ambient were 2.28 nm and 1.90 nm, respectively. These results suggest that the number of thickness of Lu_2O_3 films should to be larger than 4 nm over to obtain good electrical characteristics.



(a) In O_2 ambient (b) In N_2 ambient

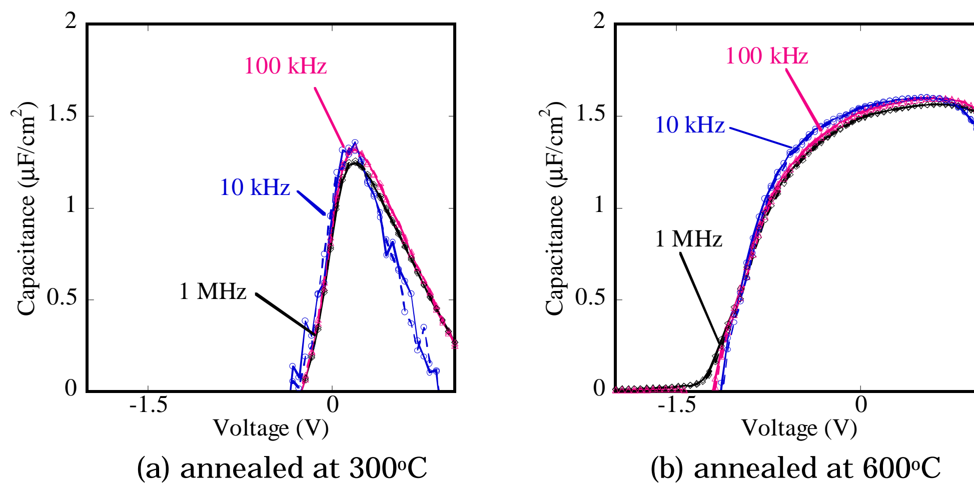
Fig 3.17 C- V characteristics with annealing temperature as a parameter

Figure 3.18 shows C-V characteristics for the films annealed at 300 °C and 600 °C in O_2 ambient with frequency as a parameter. The measurement frequencies were 1 MHz, 100kHz and 10k Hz. In case of N_2 ambient, which were shown Fig. 3.19. It observed that films annealed at 300 °C in both O_2 ambient and N_2 ambient were not useful at all to electric characteristics. At 600 °C annealing films were different in the point of depletion regions. The case of N_2 ambient was a little frequency dependence, but the case of O_2 ambient was a lot of frequency dependence. This result was considered that in O_2 ambient annealing films was tender to growth of interfacial layer of SiO_2-rich than in N_2 ambient. Therefore, there are a lot of interfacial traps in O_2 ambient annealing. These considerations were similar to that when La_2O_3 films are measured.



(a) annealed at 300°C (b) annealed at 600°C

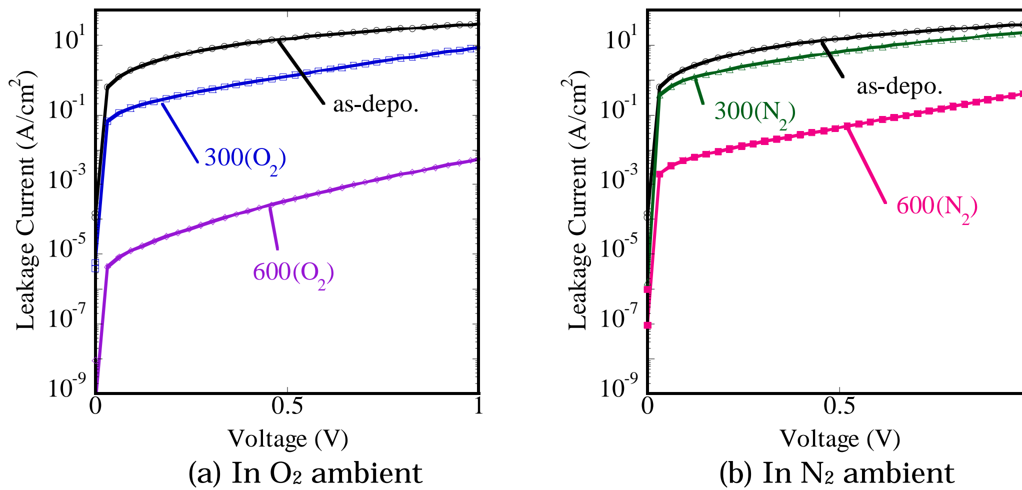
Fig3.18 C-V characteristics with frequency as a parameter in O_2 ambient



(a) annealed at 300°C (b) annealed at 600°C

Fig3.19 C-V characteristics with frequency as a parameter in N_2 ambient

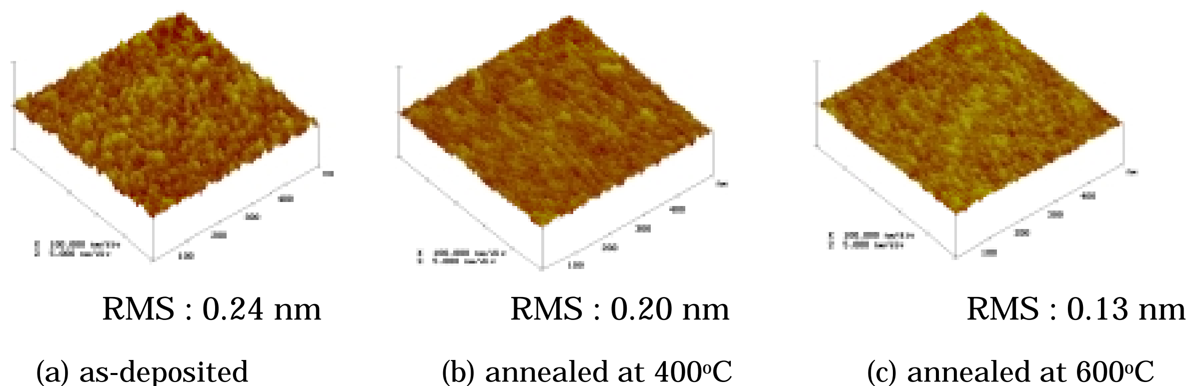
Figure 3.20 shows J-V characteristics for dependence of annealing temperature in O_2 ambient and N_2 ambient. Regard less of increase of annealing temperature, the improvement of leakage current densities was a little at 300 °C annealed in O_2 and N_2 ambient. The improvement was less one-order magnitudes compare to as-deposition films. On the other hand, the leakage currents of 600 °C-annealing films were decreased about 4 orders and about 2 orders magnitudes compare to that of as-deposited in O_2 and N_2 ambient, respectively.



(a) In O_2 ambient (b) In N_2 ambient

Fig 3.20 J-V characteristics with annealing temperature as a parameter

Figure 3.21 shows the 3D-AFM images of surface morphologies for the films before and after RTA in O_2 ambient. The scan size was 500 x 500 nm and the z direction was 5 nm/div. Their surfaces were observed smooth less about 0.2 nm. In other word, the transformation of surface roughness for about 4 nm thick films annealed in O_2 ambient until 600 °C, is not existing at all. Therefore, it was considered that crystallization of the La_2O_3 films was not appeared until at 600 °C annealing for 4 nm thicknesses. The root mean square (RMS) of as-deposited film, annealed films at 400°C and at 600°C was 0.24 nm, 0.20 nm and 0.13 nm, respectively.



RMS : 0.24 nm　　RMS : 0.20 nm　　RMS : 0.13 nm

(a) as-deposited　　(b) annealed at 400°C　　(c) annealed at 600°C

Fig 3.21　AFM images of the surface morphologies for Lu_2O_3 films annealed in O_2 for 5 min　(500 x 500 nm,　Z: 5 nm/div)

Figure 3.22 shows the wide scan spectrum for the 4nm-thick Lu_2O_3 film after RTA at 600°C in O_2 ambient by the XPS measurement.　The measurement take-off angles (θ) were 30°, 45° and 60°.　Higher the number of the take-off angle, closer the distance into Si substrate.　This spectrum was confirmed that the spectrum of Lu-4f, Lu-4d, C-1s, Lu-4p and O-1s are appeared mainly from low binding energy for each angles.

The narrow scan spectrum for the films before and after 600°C annealing in O_2 ambient were shown Fig. 3.23 and Fig. 3.24, respectively.　The Si-2s spectrums were normalized at 151 eV for Si-Si binding peaks.　Although peaks except the peak at 151 eV are hardly seen in Si-2s spectrum region before RTA, the peak at high-energy side from Si-Si binding peaks was appeared after RTA.　It seems that the interfacial layer was grown.　In both of O-1s spectrum and Lu-4f spectrum, the transformation of the peak was hardly observed after RTA compare to that before RTA.　These results were considered that the 4 nm-thick Lu_2O_3 films have interfacial layer like SiO_2-rich layer between Si and the films after RTA, and maybe the interfacial layer are grown uniformly.

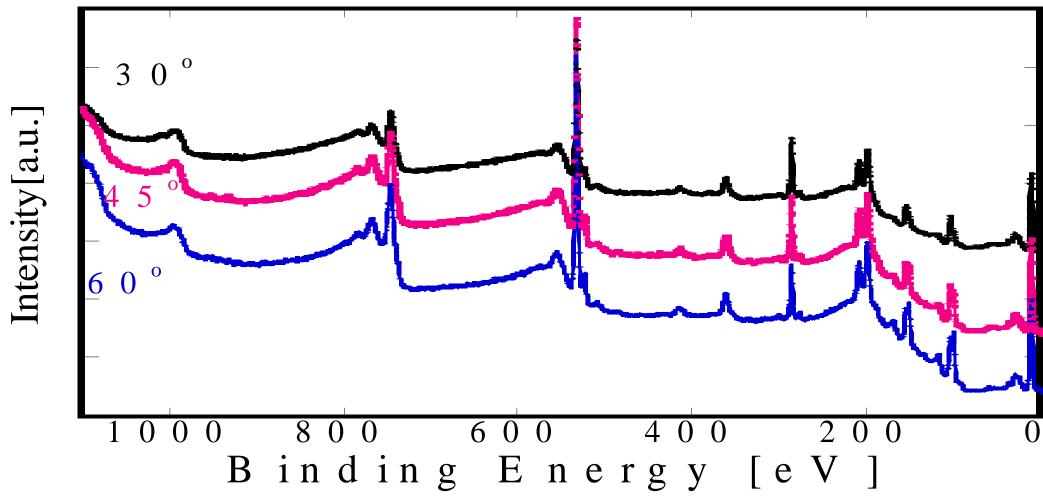
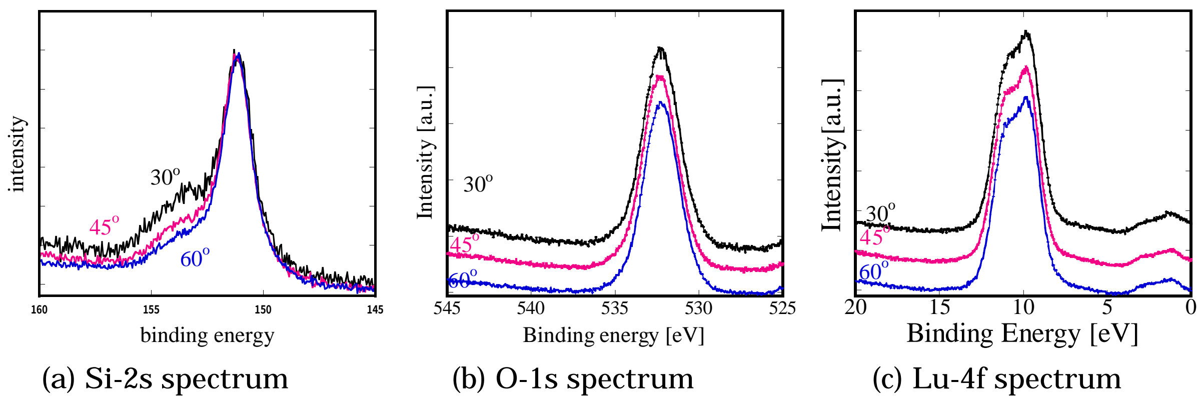
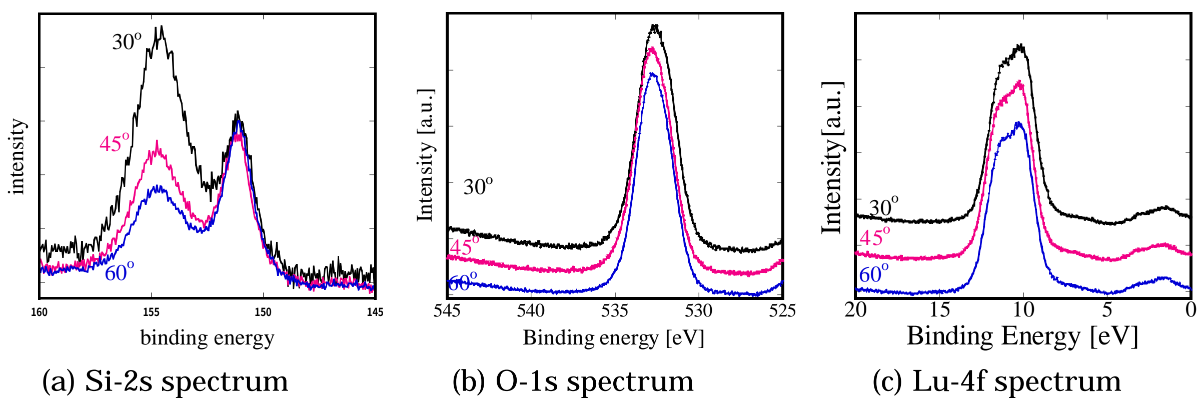


Fig 3.22　the wide spectrum of 4 nm-thick Lu_2O_3 films from 0 to 1100 eV after RTA in O_2 ambient



(a) Si-2s spectrum　(b) O-1s spectrum　(c) Lu-4f spectrum

Fig 3.23　the narrow spectrums of 4 nm-thick Lu_2O_3 films before RTA



(a) Si-2s spectrum　(b) O-1s spectrum　(c) Lu-4f spectrum

Fig 3.24　the narrow spectrums of 4 nm-thick Lu_2O_3 films after RTA in O_2 ambient

3.1.3 Consideration to Improving Properties of Single Layers

It turned out that La_2O_3 thin films are excellent in the electrical property in a single layer for 4nm-thicness as seen until this section. On the other hand, Lu_2O_3 could not acquire an electrical property in 4nm-thikness films, but it should be known that electrical characteristics could be improved for post annealing at 600 °C. These data are set to EOT vs J plot, and is shown in Fig. 3.25.

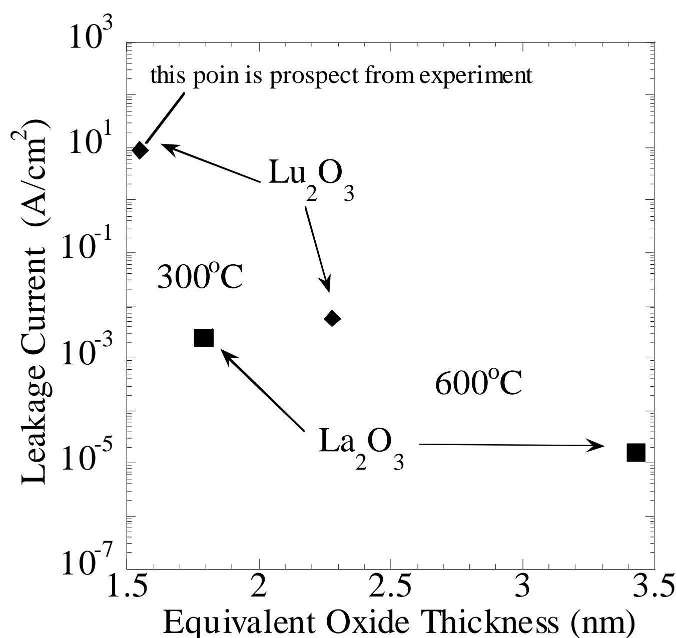


Fig 3.25 EOT vs J plot annealed films in O_2 ambient

Figure 3.26 shows AFM images of La_2O_3 and Lu_2O_3 for about 10 nm after RTA in N_2 ambient. Although RMS of as-deposited films for both of La_2O_3 and Lu_2O_3 were 0.18 nm each other, the increase of RMS after RTA was different, and RMS of that were 1.09 nm and 3.04 nm, respectively. The surface roughness of Lu_2O_3 was 3 times larger than that of La_2O_3 after RTA. This result is considered that Lu_2O_3 formed crystallization for 10 nm-thick films by heat process.

Table 3.3 shows summary of this section for Properties of La_2O_3 and Lu_2O_3. Figure 3.27 shows AFM images of La_2O_3 and Lu_2O_3 for about 10 nm after RTA in O_2 ambient. This result was similar to in N_2 ambient.

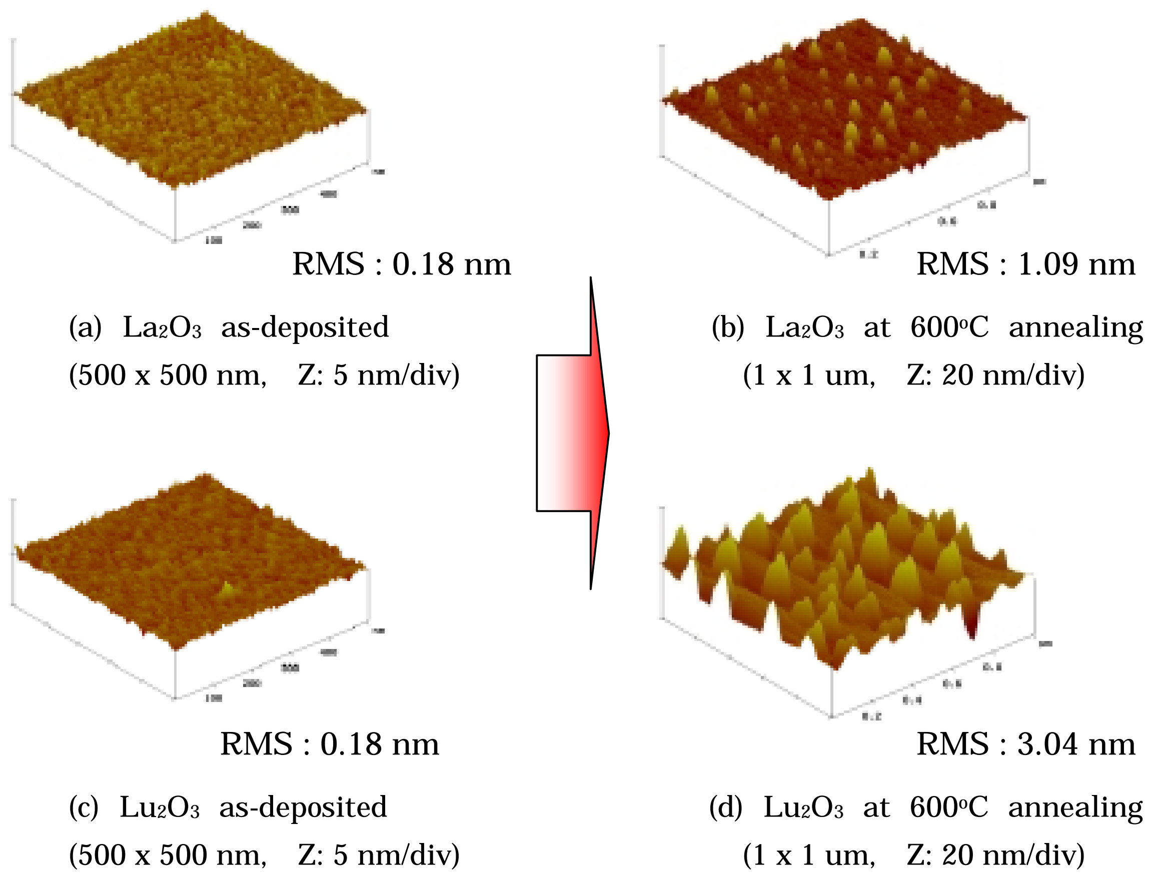
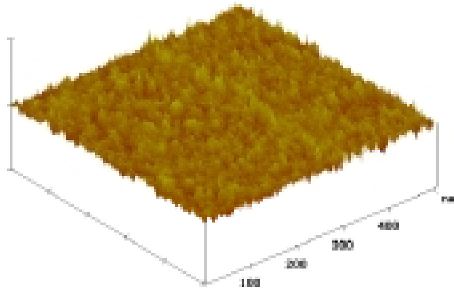


Fig 3.26 AFM images of La_2O_3 and Lu_2O_3 with thickness about 10 nm after RTA in N_2 ambient

Table 3.3 Properties of La_2O_3 and Lu_2O_3

	La_2O_3	Lu_2O_3
Bandgap	**5.5 eV**	**5.5 eV**
Dielectric constant	**~ 27 eV**	**12.5 eV**
Lattice energy	**-12687 eV**	**-13871 eV**
moisture-resistant	<	

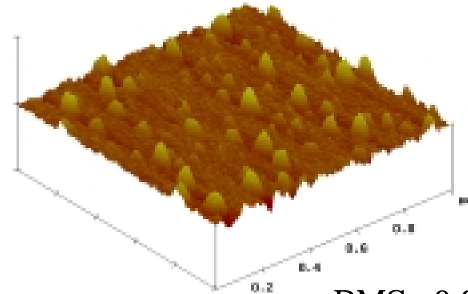
La_2O_3



RMS : 0.25 nm

(a) La_2O_3 at 300°C annealing

(500 x 500 nm, Z: 5 nm/div)

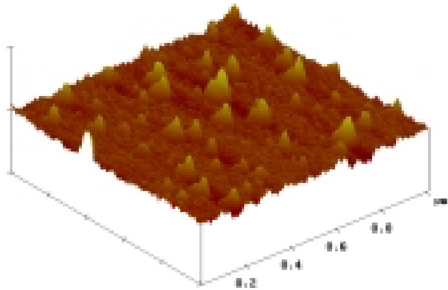


RMS : 0.94 nm

(b) La_2O_3 at 600°C annealing

(1 x 1 um, Z: 20 nm/div)

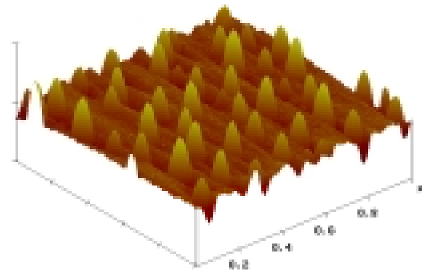
Lu_2O_3



RMS : 1.15nm

(c) Lu_2O_3 at 300°C annealing

(500 x 500 nm, Z: 5 nm/div)



RMS : 2.41nm

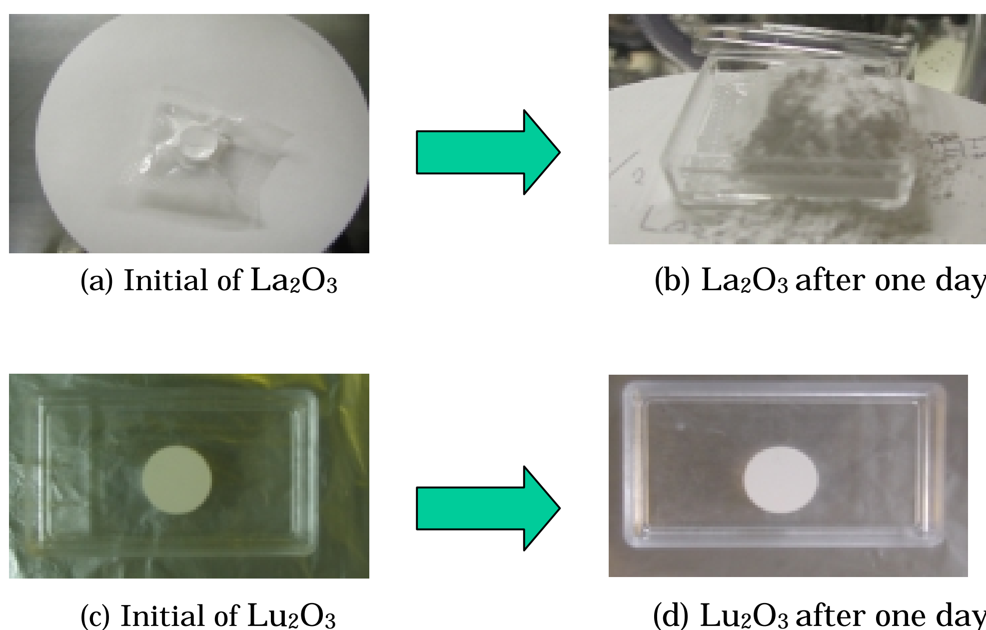
(d) Lu_2O_3 at 600°C annealing

(1 x 1 um, Z: 20 nm/div)

Figure 3.27 AFM images of La_2O_3 and Lu_2O_3 with thickness about 10 nm after RTA in O_2 ambient

3.2 Effect of Stack Structure Thin Films

As seen previous section, it is confirm that La_2O_3 thin films were comparatively stable at Si interface. However, when the surface touches atmospheric water and atmospheric carbon, it is known that the surface likely to form carbonate/ alkoxylate or hydroxide easily. Moreover, the silicates of whole La_2O_3 thin films are promoted by heat-treating, and this is anxious matter about decline in an efficiency-dielectric constant. On the other hand, at Lu_2O_3, in a thin film single layer, despite the difficulty to use, it is thought that moisture resistance is larger than La_2O_3, and is comparatively stable for the surface in the atmosphere. Although the particularly experiments are not carried out, the photograph of time degradation of these sources that are exposed for one day in the clean room, is shown in Fig. 3.23. These sources are used this experiment inserted the MBE chamber. At first time figure were ceramic completely in both of the sources, but La_2O_3 ceramic became in pieces and expanded contrast to Lu_2O_3 keeping the figure. This phenomenon were consider that the La_2O_3 ceramic have highly hygroscopic.



(a) Initial of La_2O_3 (b) La_2O_3 after one day

(c) Initial of Lu_2O_3 (d) Lu_2O_3 after one day

Fig 3.28 Photo of source inserted in MBE chamber used for experiment, which was taken in the clean room.

With this section, it is carrying out for the purpose of the improvement of an electrical property by setting La_2O_3 as buffer layer and by depositing Lu_2O_3 on that, which is the stacked structure of Lu2O3/La2O3/n-Si. The flow of MIS capacitor created with this section is shown Fig 3.29.

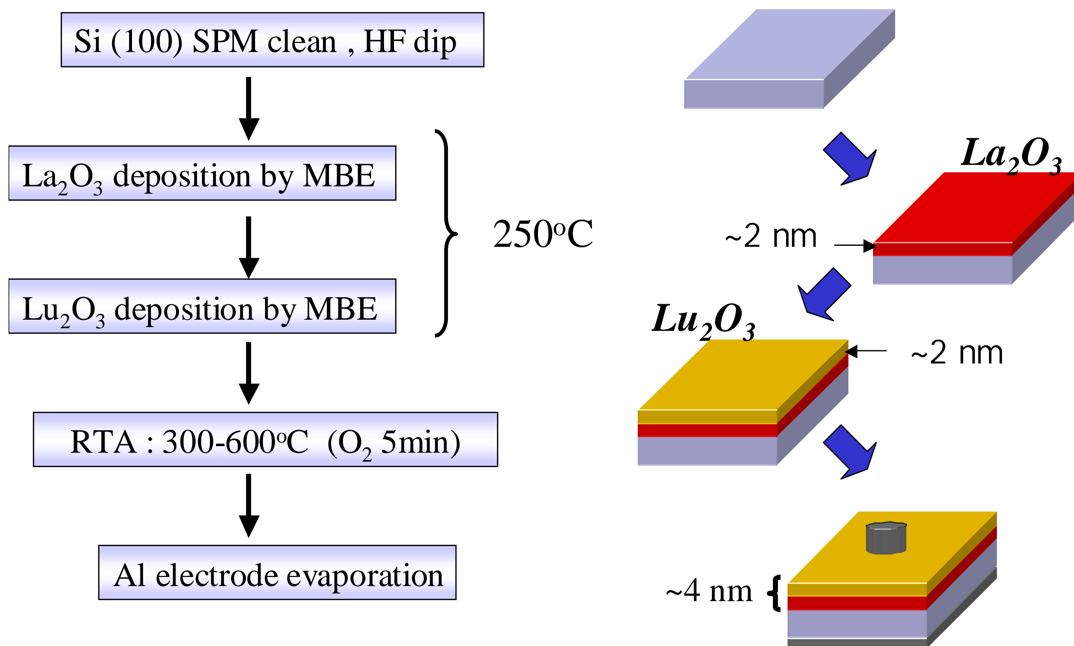
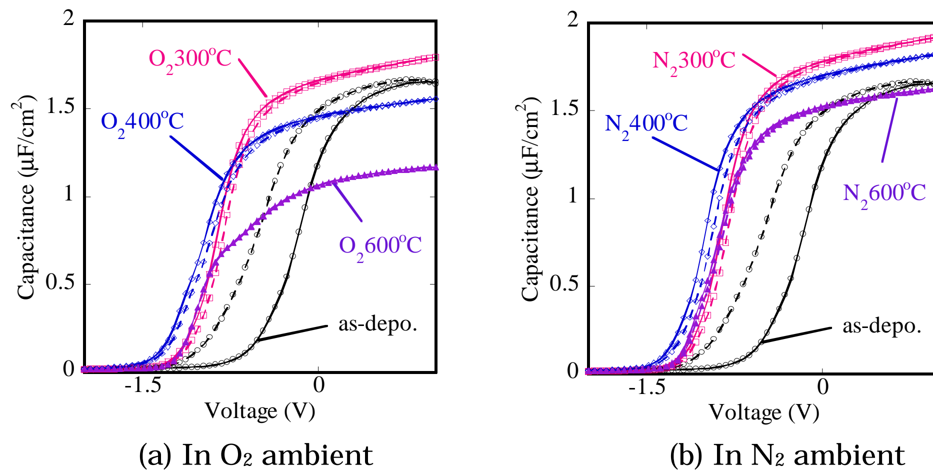


Fig 3.29 Process Flow of Lu_2O_3/La_2O_3/n-Si for MIS capacitor

3.2.1 Dependence of Annealing Temperature

The first, the electrical characteristics for the annealing condition was investigated for the structure of Lu_2O_3/La_2O_3/n-Si as 4 nm-thick stacked layers. This was deposited at 250 ^oC by MBE.

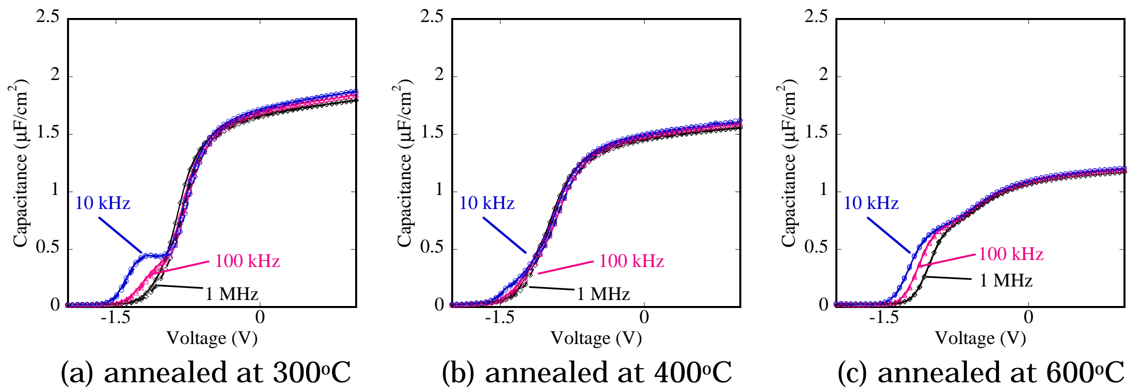
Figure 3.30 shows C-V characteristics with annealing temperature as a parameter, the annealing in both of O_2 and N_2 ambient and annealing time was 5 min. The measurement frequency was 1 MHz. The as-deposited film was observed a huge hysterisis whose width was measured about 400 mV. Although as-deposited film had a huge hysterisis, the flat band shift of that was smaller than annealed films for both trace and retrace measurement. Although the hysterisis was disappeared after more 300-^oC annealing, their negative flat band shift was increase to about 1 V. It was considered that a lot of positive fixed charges exist at the interface after RTA. Almost annealed films at 300^oC to 400^oC in O_2 and N_2 ambient were similarly. However, it was observed that the decrease of accumulation capacitance at 600 ^oC-annealed films in N_2 ambient was small compare to that in O_2 ambient. This result was considered because of the growth low dielectric interfacial layer during the annealing, and the films in O_2 ambient were more affected than in N_2 ambient due to reaction of oxygen and silicon. The EOT of as-deposited films was 1.69 nm. This value was great compare to La_2O_3 produced for same condition. The annealed films at 300 ^oC, 400 ^oC and 600 ^oC in O_2 ambient were 1.63 nm, 1.93 nm and 2.62 nm, respectively. On the other hand, the annealed films at 300 ^oC, 400 ^oC and 600 ^oC in N_2 ambient were 1.50 nm, 1.61 nm and 1.81 nm, respectively.



(a) In O_2 ambient (b) In N_2 ambient

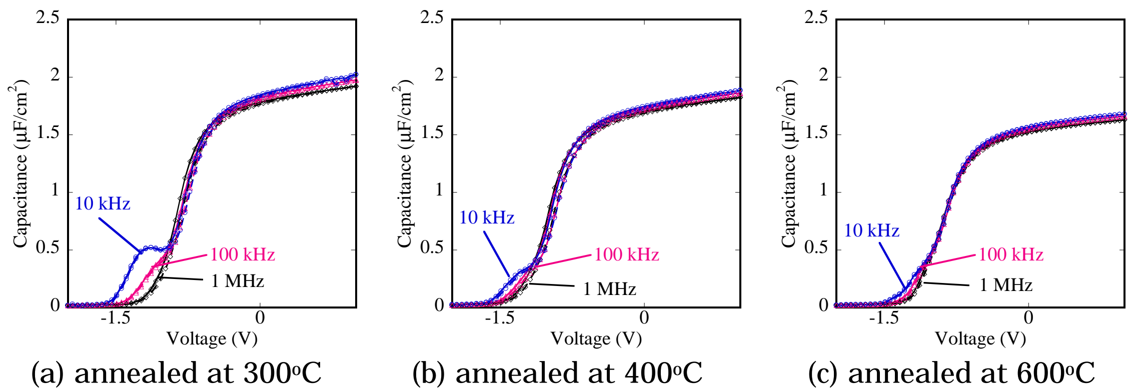
Fig 3.30 C- V characteristics with annealing temperature as a parameter

Figure 3.31 shows C-V characteristics for the films annealed at 300 °C, 400 °C and 600 °C in O_2 ambient with frequency as a parameter. The measurement frequencies were 1 MHz, 100kHz and 10k Hz. In case of N_2 ambient, which were shown Figure 3.32. It observed that films annealed at 300 °C in both O_2 ambient and N_2 ambient were similar frequency dependence at depletion regions, and in the case of 400 °C annealing, similarly. However, at 600 °C annealing films were different in the point of depletion regions. The case of N_2 ambient was a little frequency dependence, but the case of O_2 ambient was a lot of frequency dependence. This result was considered that in O_2 ambient annealing films was tender to growth of interfacial layer of SiO_2-rich than in N_2 ambient. Therefore, there are a lot of interfacial traps in O_2 ambient annealing.



(a) annealed at 300°C (b) annealed at 400°C (c) annealed at 600°C

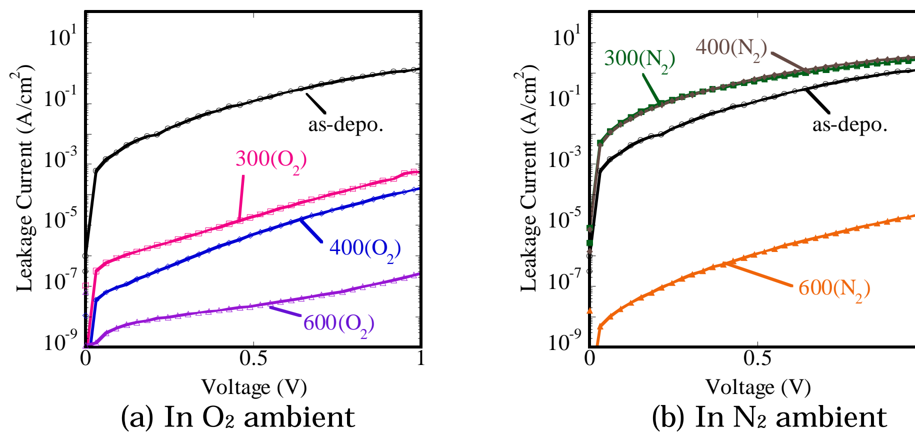
Fig 3.31 C-V characteristics with frequency as a parameter in O_2 ambient



(a) annealed at 300°C (b) annealed at 400°C (c) annealed at 600°C

Fig 3.32 C-V characteristics with frequency as a parameter in N_2 ambient

Figure 3.33 shows J-V characteristics for dependence of annealing temperature in O_2 ambient and N_2 ambient. More increase of annealing temperature, leakage current densities was more decrease significantly in O_2 ambient. However, the leakage current of both 300 °C and 400 °C annealed films was hardly different to as-deposited in N_2 ambient. The leakage current of 600 °C-annealing films was decreased about 6 orders magnitudes from that of as-deposited in N_2 ambient. This result was consider that interfacial layer growth was a little until 400 °C annealing in N_2 ambient.

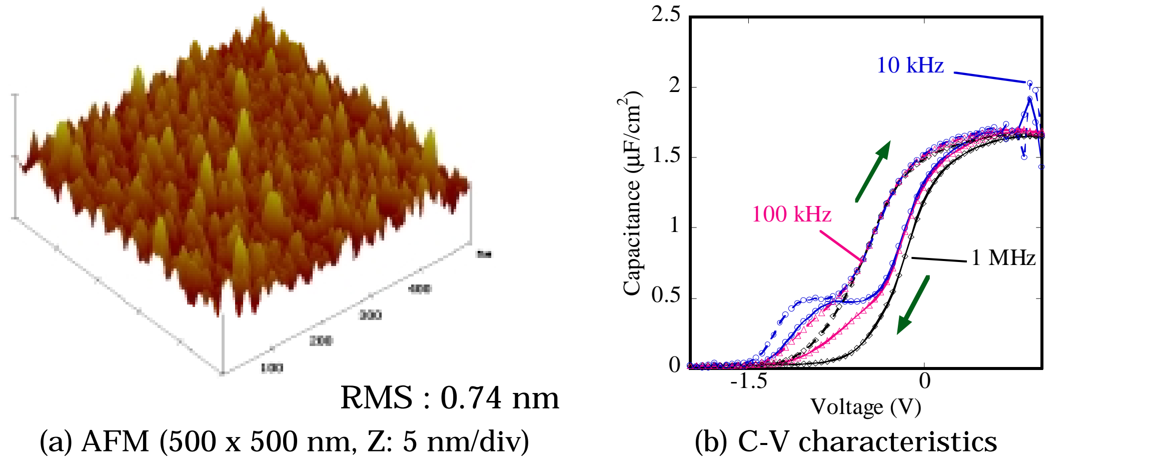


(a) In O_2 ambient (b) In N_2 ambient

Fig 3.33 J-V characteristics with annealing temperature as a parameter

Figure 3.34 shows the 3D-AFM images of surface morphologies and C-V characteristics of frequency dependence for as-deposited films. The scan size of AFM image was 500 x 500 nm and the z direction was 5 nm/div. This surface was observed large roughness about 0.74 nm. The roughness was lager than that of both La_2O_3 and Lu_2O_3 as single layer for as-deposited films with 4 nm thicknesses. However, raise RTA temperature, the surface roughness were improved in both O_2 and N_2 ambient until 600 °C gradually, which were shown Fig 3.35. Generally in the single layer, higher RTA temperature, more increase the value of RMS. By the way, the frequency dependence at depletion region was observed and the figure was seemed to be lager than that after 300 °C annealing. Therefore, it was considered that the surface roughness of the as-deposited film was not crystallization, and the roughness was occurred due to deposition condition. The RMS of annealed films at

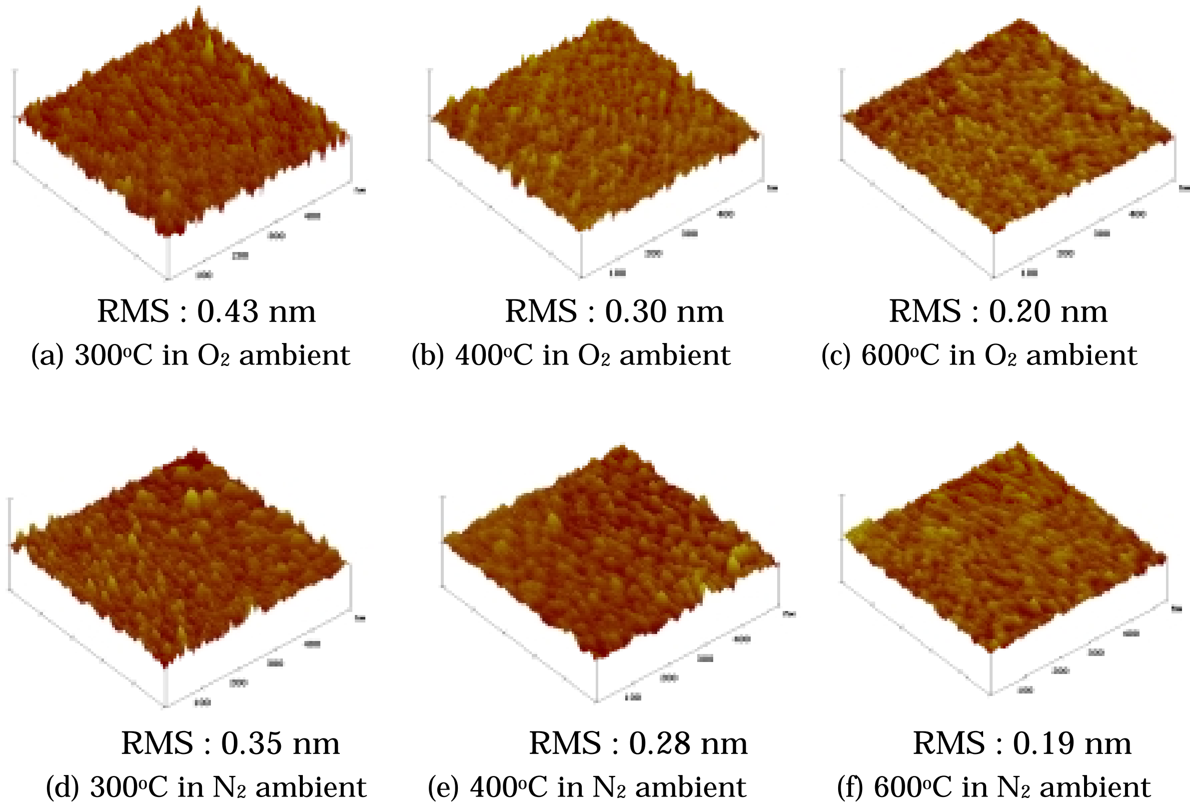
300°C, 400°C and 600°C in O_2 ambient was 0.43 nm, 0.30 nm and 0.20 nm, respectively. On the other hand, in the case of N_2 ambient the RMS at 300 °C, 400 °C and 600 °C was 0.35 nm, 0.28 nm and 0.19 nm, respectively.



RMS : 0.74 nm

(a) AFM (500 x 500 nm, Z: 5 nm/div) (b) C-V characteristics

Fig 3.34 AFM images and C-V characteristics for as-deposited films



RMS : 0.43 nm — (a) 300°C in O_2 ambient

RMS : 0.30 nm — (b) 400°C in O_2 ambient

RMS : 0.20 nm — (c) 600°C in O_2 ambient

RMS : 0.35 nm — (d) 300°C in N_2 ambient

RMS : 0.28 nm — (e) 400°C in N_2 ambient

RMS : 0.19 nm — (f) 600°C in N_2 ambient

Fig 3.35 AFM images after annealed in O_2 and N_2 ambient

(500 x 500 nm, Z: 5nm/div)

Figure 3.36 shows the wide scan spectrum for the 4nm-thick stacked film as structure of Lu_2O_3/La_2O_3/n-Si after RTA at 600 °C in O_2 ambient by the XPS measurement. The measurement take-off angles (θ) were 30°, 45° and 60°. Higher the number of the take-off angle, closer the distance into Si substrate. This spectrum was confirmed that the spectrum of Lu-4f, La-4d, La-4p, C-1s, Lu-4p, O-1s and La3d are appeared mainly from low binding energy for each angles.

The narrow scan spectrum for the films before and after RTA shown Fig 3.37 and Fig 3.38, respectively. The Si-2s spectrums were normalized at 151 eV for Si-Si binding peaks. Although peaks except the peak at 151 eV are hardly seen in Si-2s spectrum region before RTA, the peaks at high-energy side from Si-Si binding peaks were appeared after RTA, and the peaks were strong in order with a low angle. It seems that the interfacial layer was grown. In O-1s spectrum, the transformation of the peak was observed that annealing temperatures were changed from 300 °C to 600 °C, although the figure of the as-deposited film similar to that of 300 °C annealing film. This transformation is chemical shift that the peak at low-energy side moves to high-energy side. Therefore, it was thought to change the silicate. Although both the La-$3d_{3/2}$ and the Lu-4f spectrum after RTA were seem to be almost similar to that before RTA, it was observed that both of spectrum figures of the films after 600°C became a sharp a little. It means that metal oxides changed to silicides such as $(La_x,Lu_y)O_z$. Therefore, these results were considered that in the 4 nm-thick staked films as structure of Lu_2O_3/La_2O_3/n-Si changes to the films as structure of $(La_x,Lu_y)O_z$/La-silicate/n-Si after RTA.

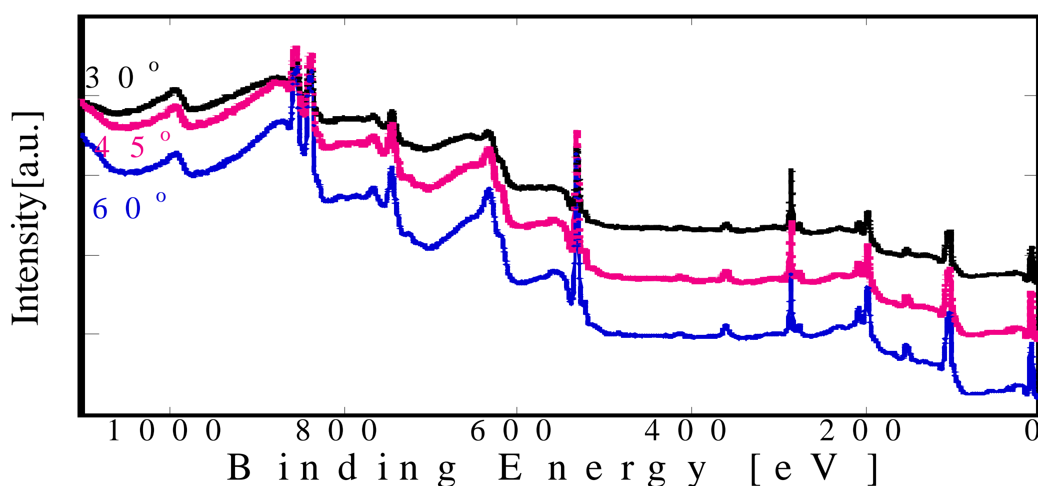
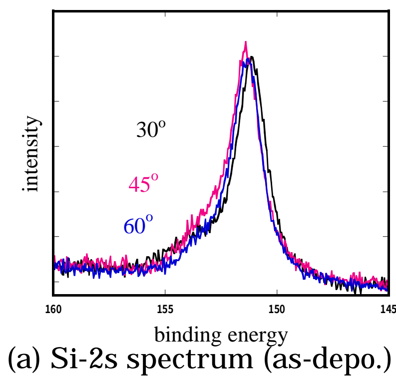
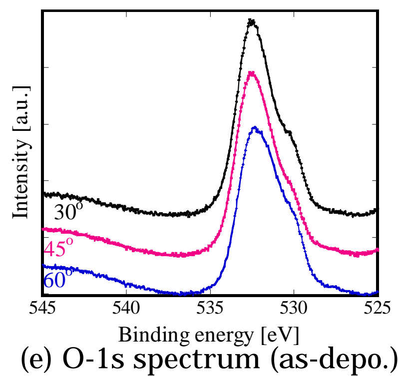


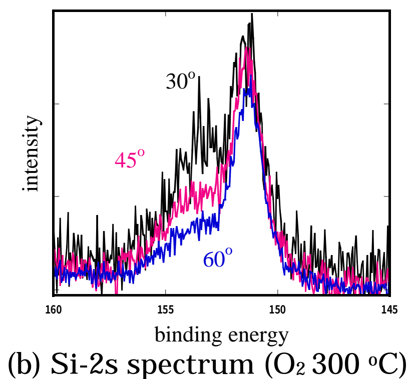
Fig 3.22 the wide spectrum of 4 nm-thick stacked film as structure of Lu_2O_3/La_2O_3/n-Si after RTA from 0 to 1100 eV after RTA in O_2 ambient



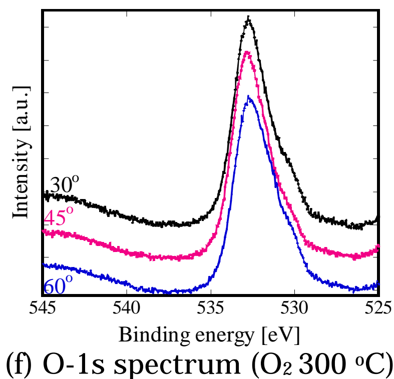
(a) Si-2s spectrum (as-depo.)



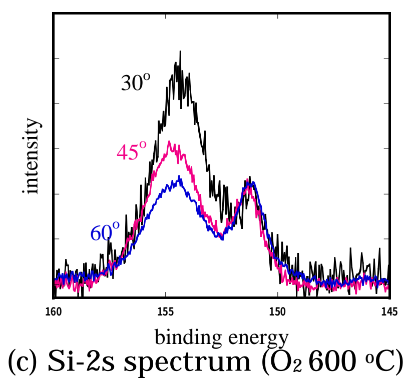
(e) O-1s spectrum (as-depo.)



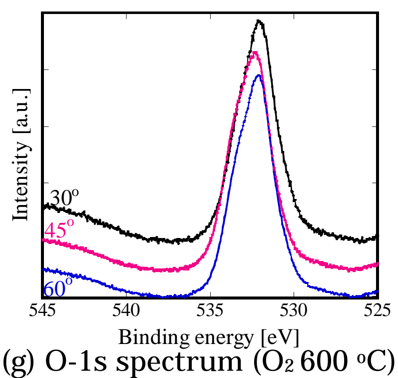
(b) Si-2s spectrum (O_2 300 °C)



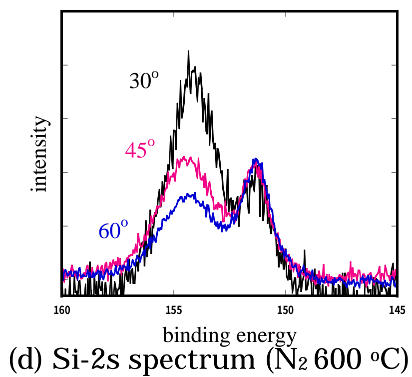
(f) O-1s spectrum (O_2 300 °C)



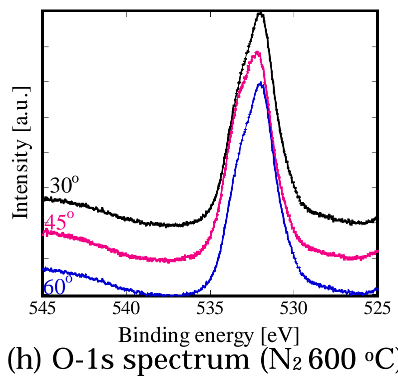
(c) Si-2s spectrum (O_2 600 °C)



(g) O-1s spectrum (O_2 600 °C)

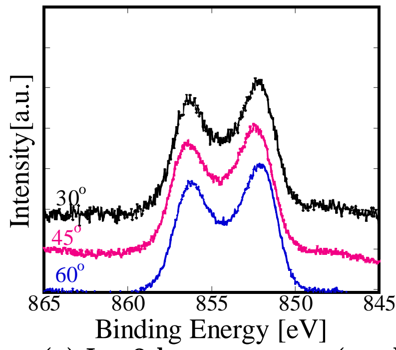


(d) Si-2s spectrum (N_2 600 °C)

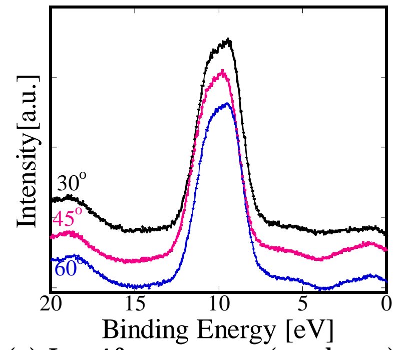


(h) O-1s spectrum (N_2 600 °C)

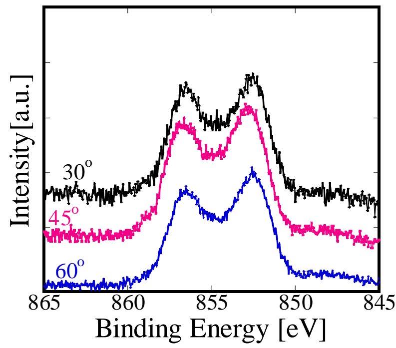
Fig 3.36 the narrow spectrums of 4 nm-thick stacked films as structure of Lu_2O_3/La_2O_3/n-Si after RTA



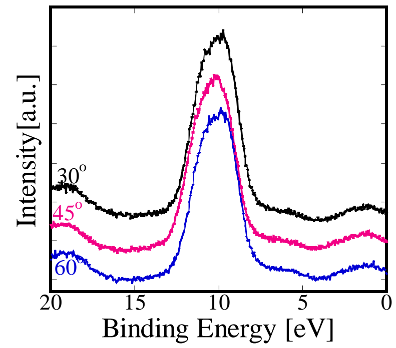
(a) La-3d3/2 spectrum (as-depo.)



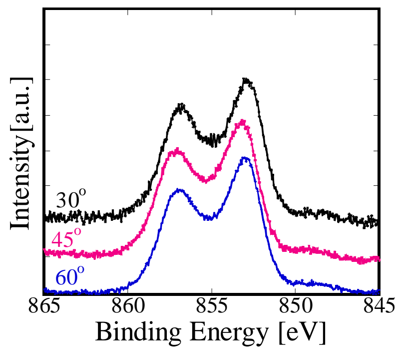
(e) Lu-4f spectrum (as-depo.)



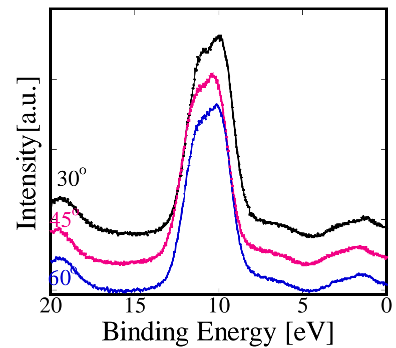
(b) La-3d3/2 spectrum (O_2 300 °C)



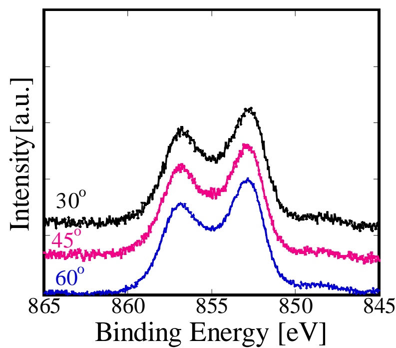
(f) Lu-4f spectrum (O_2 300 °C)



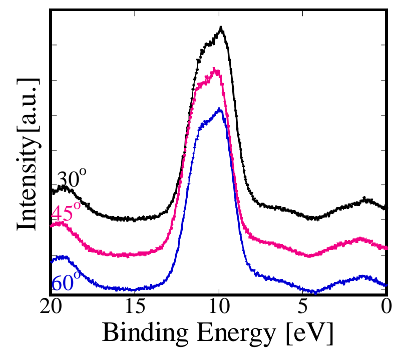
(c) La-3d3/2 spectrum (O_2 600 °C)



(g) Lu-4f spectrum (O_2 600 °C)



(d) La-3d3/2 spectrum (N_2 600 °C)



(h) Lu-4f spectrum (N_2 600 °C)

Fig 3.37 the narrow spectrums of 4 nm-thick stacked films as structure of Lu_2O_3/La_2O_3/n-Si after RTA

3.2.3 Dependence of Physical Thickness

It was the research for 4 nm thick films in until previous section. This section shows the electrical characteristics for the annealing condition was investigated for 10 nm-thick films, and especially shows the stacked structure of Lu_2O_3/La_2O_3/n-Si. This was also deposited at 250 °C by MBE. There were prepared that stacked layers as structure of 2 nm-thick Lu_2O_3/ 8 nm-thick La_2O_3/n-Si and of 5 nm-thick Lu_2O_3/ 5 nm-thick La_2O_3/n-Si. As comparison, single layer of Lu_2O_3 and La_2O_3 for 10 nm-thick films were deposited.

Figure 3.38 shows C-V characteristics with annealing temperature as a parameter, the annealing in both of O_2 and N_2 ambient and annealing time was 5 min. The measurement frequency was 1 MHz.

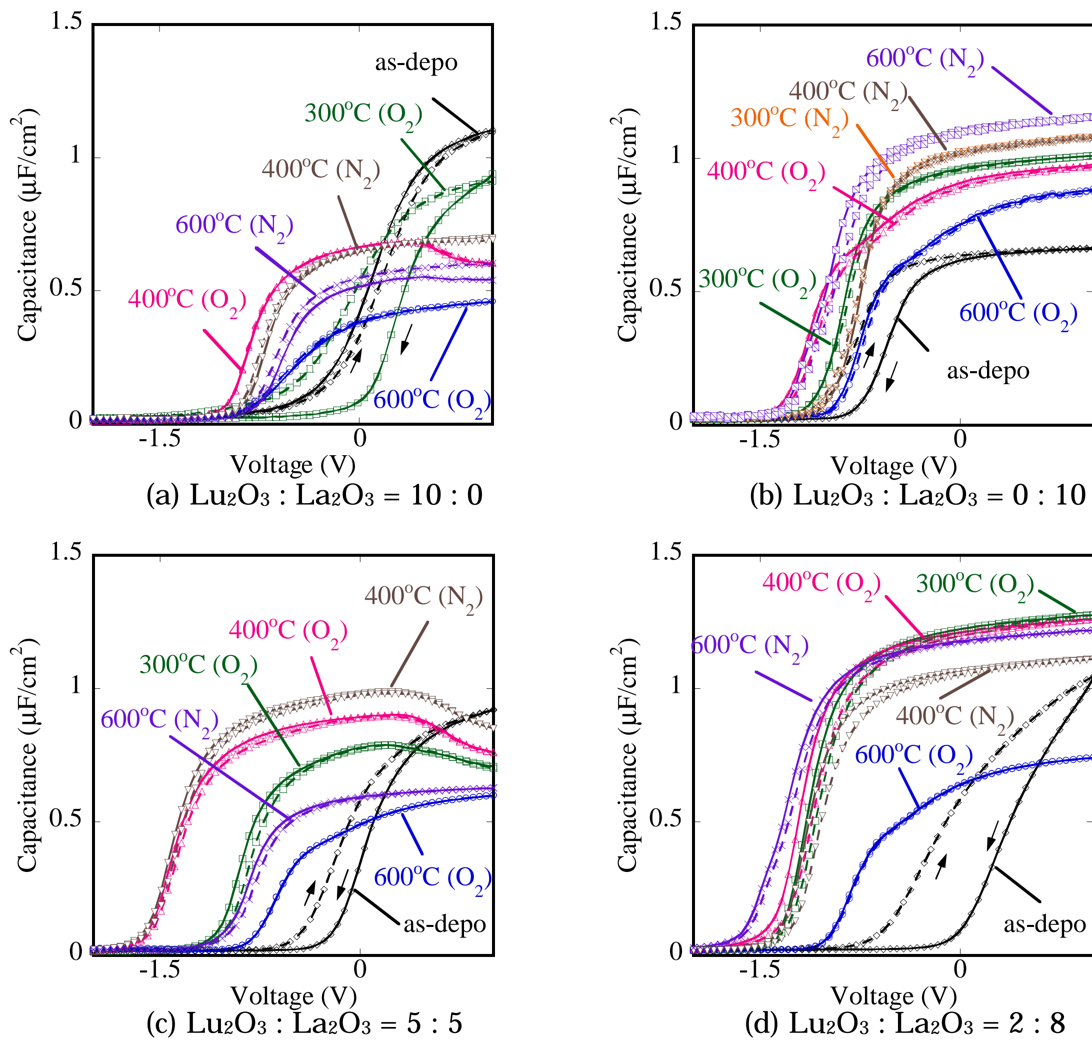
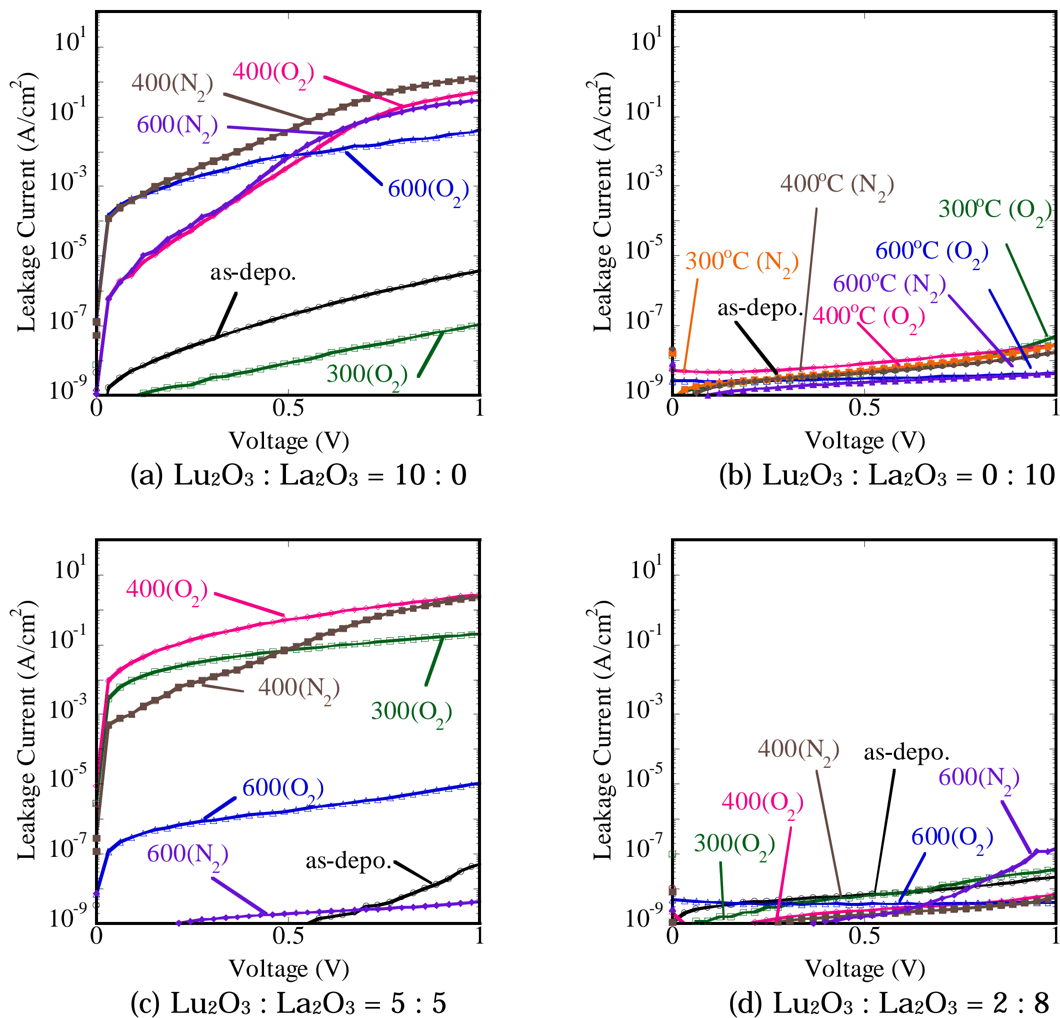


Fig 3.38 C-V characteristics for 10 nm-thick films

The capacitance at accumulation region of stacked layers as structure of 2 nm-thick Lu_2O_3/ 8 nm-thick La_2O_3/n-Si was largest in four condition layers. It is consider that it is effective condition for the stacked films that the stacked layer ratio is Lu_2O_3 : La_2O_3 = 2 : 8, or the 2 nm-thick Lu_2O_3 films as on the top of the La_2O_3 films is the optimum thickness for the cap of buffer layers.

Figure 3.39 shows J-V characteristics with annealing temperature as a parameter, the annealing in both of O_2 and N_2 ambient and annealing time was 5 min. This result shows stacked layers as structure of 2 nm-thick Lu_2O_3/ 8 nm-thick La_2O_3/n-Si was suppressed the leakage current remarkably. Therefore, it is seen that stacked layers as structure of 2 nm-thick Lu_2O_3/ 8 nm-thick La_2O_3/n-Si was optimum condition for 10 nm thick films.

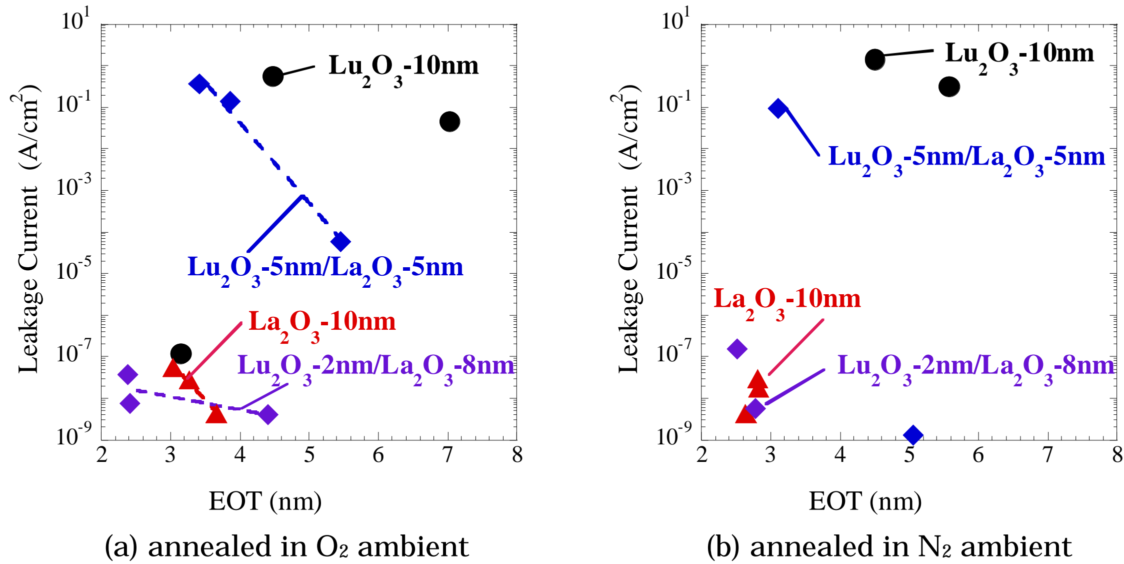
These results were shown Fig 3.40 as J vs EOT plots.



(a) Lu_2O_3 : La_2O_3 = 10 : 0 (b) Lu_2O_3 : La_2O_3 = 0 : 10

(c) Lu_2O_3 : La_2O_3 = 5 : 5 (d) Lu_2O_3 : La_2O_3 = 2 : 8

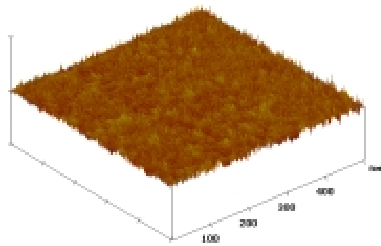
Fig 3.39 J-V characteristics for 10 nm-thick films



(a) annealed in O_2 ambient (b) annealed in N_2 ambient

Fig 3.40 J. vs. EOT. plot in O_2 and N_2 ambient for 10 nm-thick films

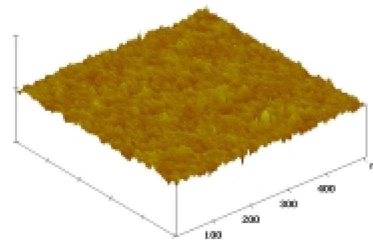
Figure 3.41 shows AFM images of stacked films for 10 nm thick films. These films were annealed at 300 °C and 600 °C in O_2 ambient, and annealed at 600 °C in N_2 ambient. The surface roughness of stacked layers as structure of 2 nm-thick Lu_2O_3/ 8 nm-thick La_2O_3/n-Si were almost flat before and after RTA. On the other hand, the roughness of stacked layers as structure of 5 nm-thick Lu_2O_3/ 5 nm-thick La_2O_3/n-Si were flat similarly until 300 °C, however, that was very large (RMS was 1.92 nm in O_2 ambient) after 600 °C annealing in both O_2 and N_2. Refer to Fig 3.26 and 3.27 for 10 nm-thick films as single layer, the RMS of Lu_2O_3 films after 600 °C annealing in O_2 ambient was 2.41 nm, and that of La_2O_3 was under 1 nm. Therefore, these results mean that over 5 nm-thick Lu_2O_3 films on the la_2O_3 are crystallized after 600 °C annealing. It was considered that the influence was observed the electrical characteristics of films.



RMS : 0.19 nm

(a) Lu_2O_3 : La_2O_3 = 2 : 8 (as-depo.)

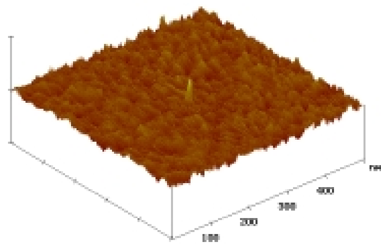
(500 x 500 nm, Z: 5 nm/div)



RMS : 0.20 nm

(e) Lu_2O_3 : La_2O_3 = 5 : 5 (as-depo.)

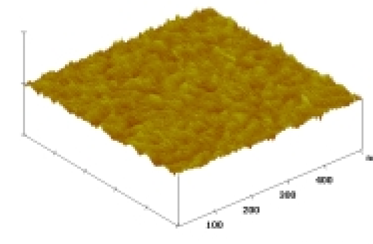
(500 x 500 nm, Z: 5 nm/div)



RMS : 0.23 nm

(b) Lu_2O_3 : La_2O_3 = 2 : 8 (O_2 300 ^oC)

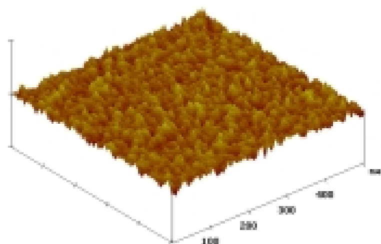
(500 x 500 nm, Z: 5 nm/div)



RMS : 0.16 nm

(f) Lu_2O_3 : La_2O_3 = 5 : 5 (O_2 300 ^oC)

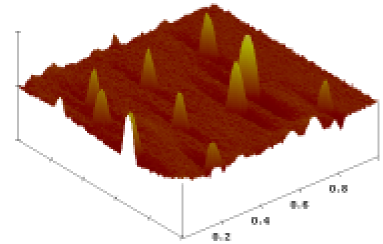
(500 x 500 nm, Z: 5 nm/div)



RMS : 0.23 nm

(c) Lu_2O_3 : La_2O_3 = 2 : 8 (O_2 600 ^oC)

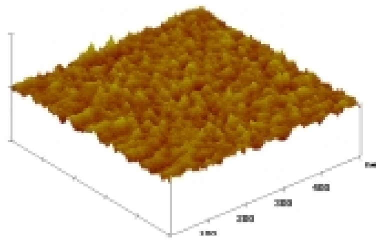
(500 x 500 nm, Z: 5 nm/div)



RMS : 1.93 nm

(g) Lu_2O_3 : La_2O_3 = 5 : 5 (O_2 600 ^oC)

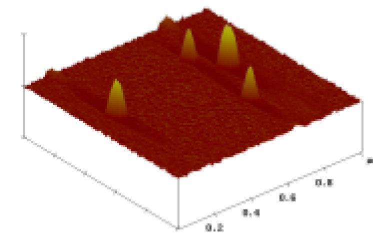
(1 x 1 um, Z: 20 nm/div)



RMS : 0.23 nm

(d) Lu_2O_3 : La_2O_3 = 2 : 8 (N_2 600 ^oC)

(500 x 500 nm, Z: 5 nm/div)



RMS : 1.23 nm

(h) Lu_2O_3 : La_2O_3 = 5 : 5 (N_2 600 ^oC)

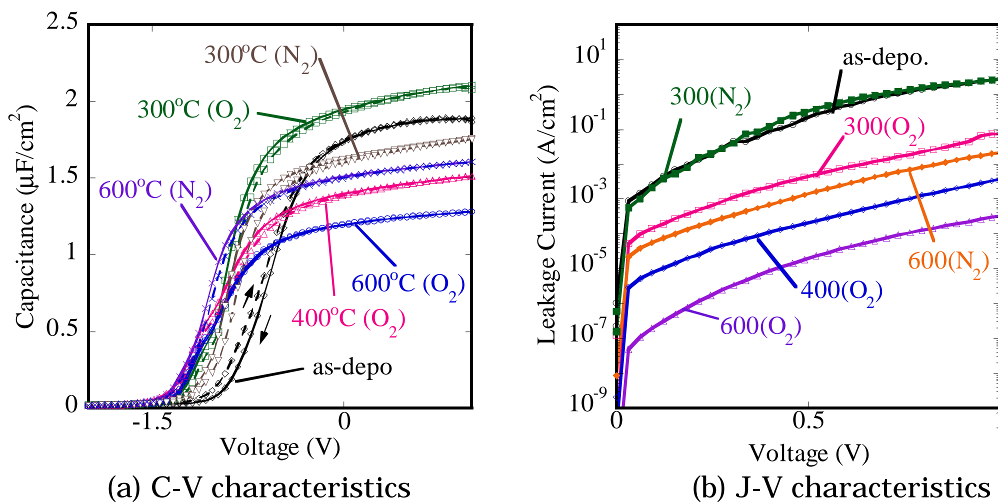
(1 x 1 nm, Z: 20 nm/div)

Fig 3.41 AFM images of 10 nm thick films

3.2.4 Dependence of Deposition Temperature

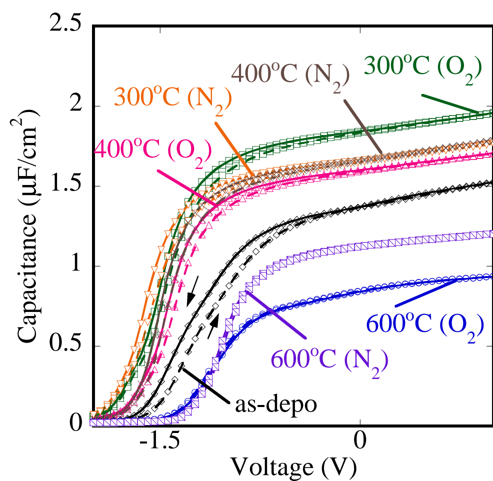
It was the research that deposition temperature was 250°C constantly in until previous section. This subsection shows the electrical characteristics of dependence of the deposition condition were investigated for Room temperature deposition (RT-depo.) and 400°C. It is shows the stacked structure of Lu_2O_3/La_2O_3/n-Si. This thickness was 2 nm for Lu_2O_3 and La_2O_3 layer, respectively. Figure 3.42 and 3.43 shows C-V and J-V characteristics with annealing temperature as a parameter, the annealing in both of O_2 and N_2 ambient and annealing time was 5 min. The measurement frequency was 1 MHz.

Figure 3.44 shows J. vs. EOT plots. This result shows that deposition temperature at 250 °C was the good condition rather than RT deposited.

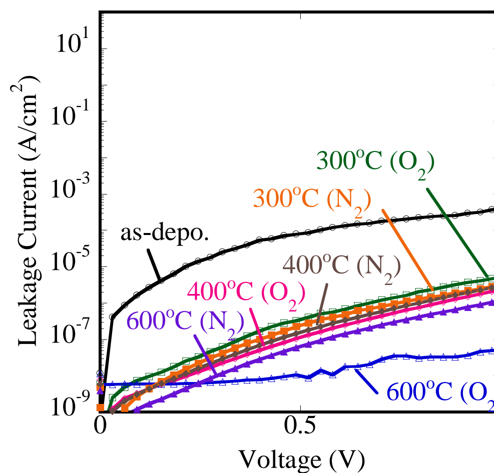


(a) C-V characteristics (b) J-V characteristics

Fig 3.42 C-V and J-V characteristics for stack structure deposited at Room Temperature.

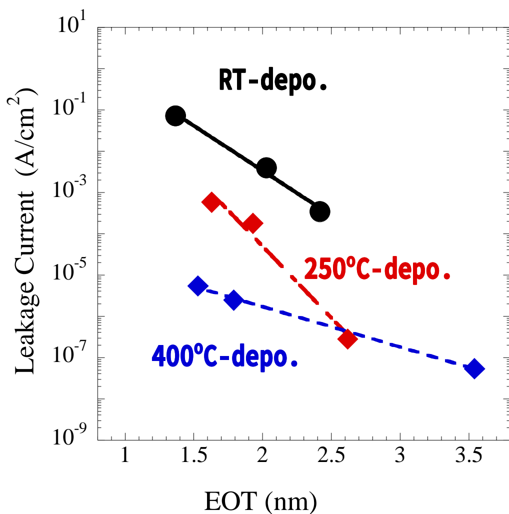


(a) C-V characteristics

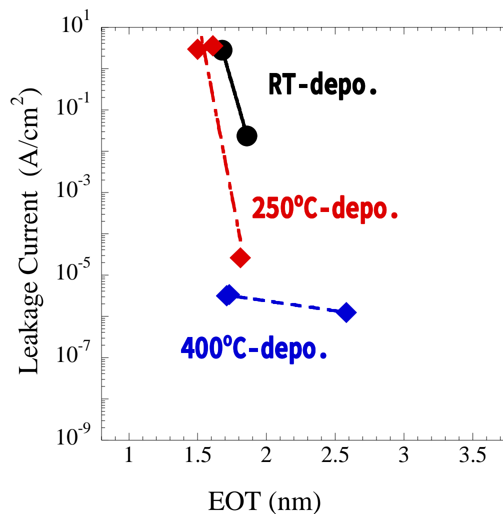


(b) J-V characteristics

Fig 3.42 C-V and J-V characteristics for stack structure deposited at 400°C.



(a) In the case of O_2 ambient

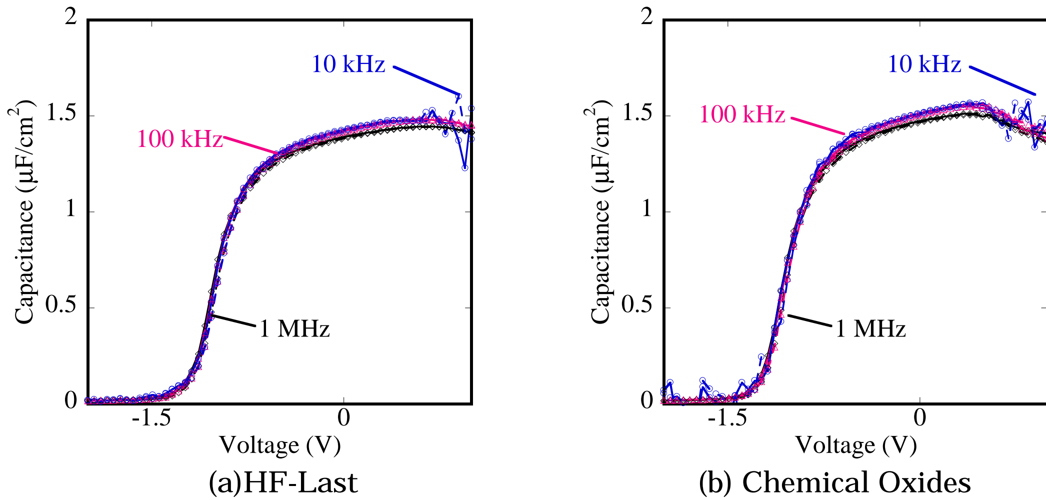


(b) In the case of N_2 ambient

Fig 3.43 J. vs. EOT plot

3.2.6 Effect of Chemical Oxides

Generally, the electrical characteristics are improved when it inserts the chemical oxides as interfacial layer between dielectric films and Si substrate. Figure 3.44 and 3.45 shows C-V and J-V characteristics of stacked films annealed at 400°C in N_2 ambient, the annealing time was 5 min. The structure of staked films was Lu_2O_3/La_2O_3/n-Si, and the thickness was 2 nm for Lu_2O_3 and La_2O_3 layer, respectively. The measurement frequency was 1 MHz, 100 kHz and 10 kHz. It was not observed that improvement of chemical oxides effect, the electric characteristics was similar to HF-Last. Unfortunately, there was not carry out the chemical oxides under condition in O_2 ambient.



(a)HF-Last (b) Chemical Oxides

Fig 3.44 J. vs. EOT plot

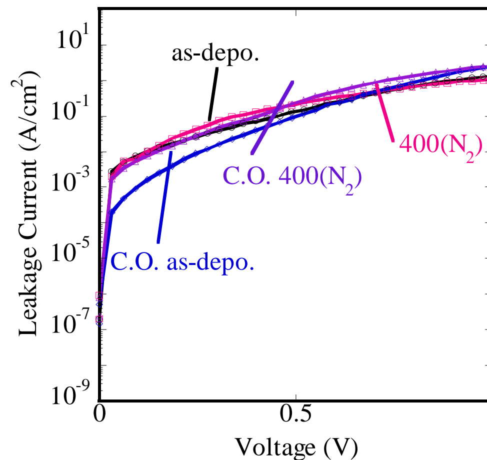


Fig 3.45 J. vs. EOT plot

3.3 Analysis for Interfacial Layer with XPS

To investigate the interfacial layer component, the peak separation from Si spectrum was carried out. The interfacial layer was distinguished from silicate or SiO_2-rich. This method in detail is referred appendix. Figure 3.45 shows the peak separation with Si-2s spectrum of Lu_2O_3/La_2O_3/n-Si annealed at 300 ^oC and 600 ^oC in O_2 ambient under 45° angle. The Experiment plot was identical spectrum where the Si-2s indicated Fig 3.36(a). The separated spectrums of stacked film annealed at 300 ^oC were similar to as-deposited in point of SiO_2/Silicate ratio. However, in the case of 600 ^oC annealing, SiO_2 peak was appeared obviously. The integral of the peak separated was calculated as SiO_2/Silicate ratios under angles, and were summarized in Table 3.4. This table indicates that the numbers of SiO_2/Silicate ratios under 45° and 60° angle at 600°C was larger than others. This result was considered that SiO_2-rich layer was grown annealed at 600°C in O_2 ambient, although interfacial layer grown at 300°C was mainly silicate. Figure 3.46 shows the schematics of structure images after RTA in O_2 ambient.

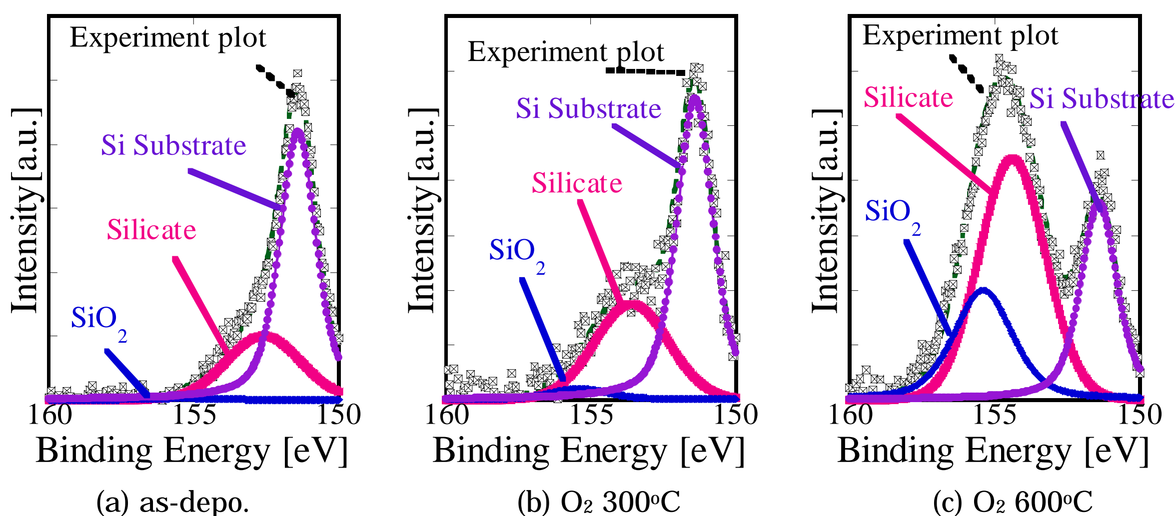


Fig 3.45 peak separated from Si-2s spectrum

Table 3.4 SiO2 / Silicate rations of Lu_2O_3/La_2O_3/n-Si by peak separation

Take-off angle [θ]	**SiO_2 / Silicate Ratios**		
	as-depo.	O_2 300°C	O_2 600°C
30°	0.01	0.09	0.06
45°	0.02	0.05	0.46
60°	0.02	0.16	0.68

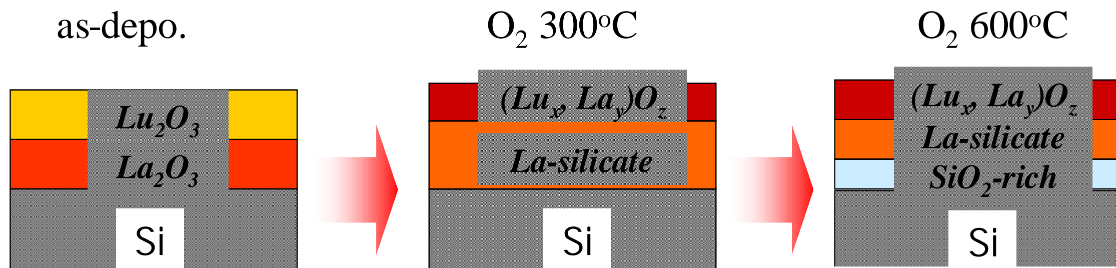


Fig 3.46 the schematic of Lu_2O_3/La_2O_3/n-Si with temperature in O_2 ambient

3.4 Discussion

In this chapter, we discussed the Experiment Results of MIS Capacitors with the rare earth oxides dielectric thin films.

When total thickness was 4 nm, we obtained excellent electrical characteristics of stack films as Lu_2O_3/La_2O_3/n-Si compare to that of single La_2O_3 films. The surface roughness of the stack films were improved by RTA. When the La_2O_3 layer is deposited on top of the Si surface, it is found that the interfacial layer is mainly silicate. Therefore, the stacked films as Lu_2O_3/La_2O_3/n-Si were thought to become $(La_x, Lu_y)\ O_z$/La-silicate/n-Si after RTA. However, the La-silicate was mainly grown under low anneal temperature at 300-400 ^oC, it was grown SiO_2-rich layer between La-Silicate and Si substrate at 600^oC as high anneal temperature. This result means that optimum annealing temperature is 300-400 ^oC.

Chapter 4

Operation Confirmation of Devices

4.1 Electrical Characteristics of n-MISFET

The operation confirmations of the gate Insulator Devises were evaluated by using n-MIS transistor (n-MISFET). The fabrication flow of n-MISFET process for stacked layer as insulator is showed in Fig. 4.1.

First, n-MISFET substrate was cleaning in wet process. Next, the rare earth oxides were deposited on the Si by the MBE system. Then, post annealing was executed with RTA for 5 min. After the annealing, Al electrodes for gate insulators were deposited on the top of the rare earth oxides. Etch the Al electrodes, the La_2O_3 and the Lu_2O_3 of dielectric thin films for making the Gate before resist coating. After coat the resist, etch the resist for Al electrode of the Source and Drain. Finally, Al electrodes were deposited for the Source and the Drain, and rift off the whole resists with Al electrode on that.

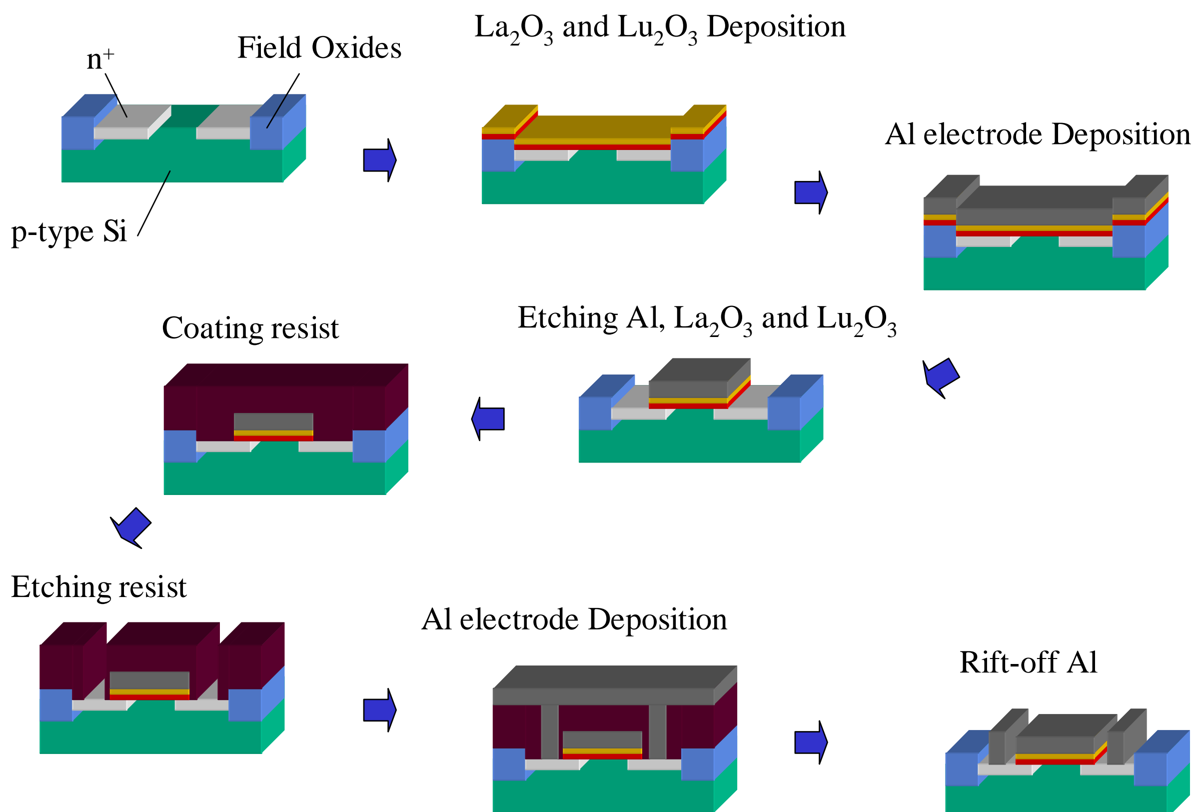
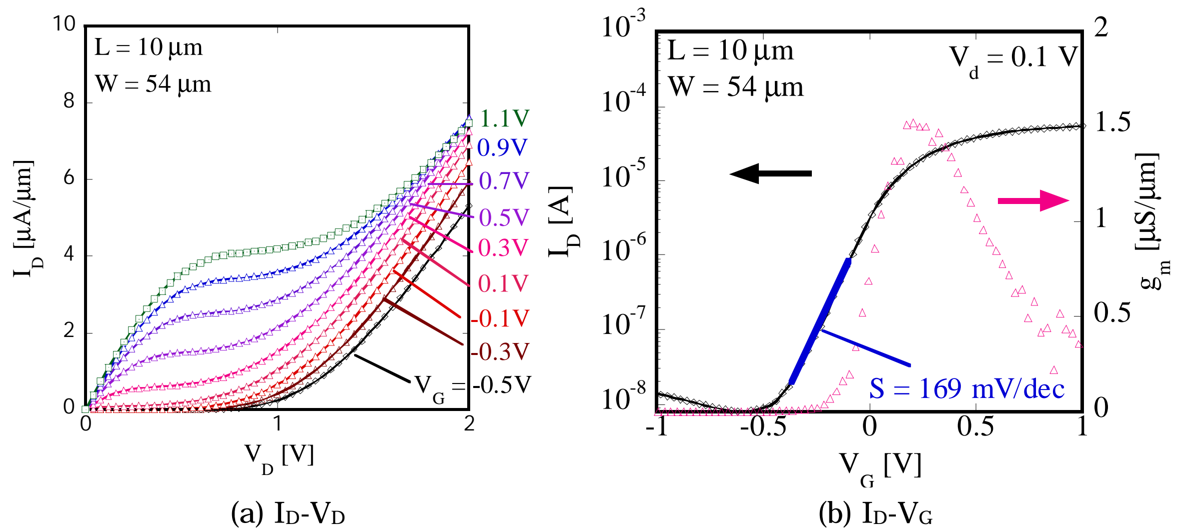


Fig 4.1 Process Flow for n-MISFET

4.1.1 Characteristics of Stacked Dielectric Films Transistors

This section is reported that stacked dielectric films for 4 nm-thick gate transistors were operating. First, as-deposited films were measured whether it operate collect or not. Figure 4.2 shows I_D –V_D characteristics and I_D-V_G for the films. The measured area was 10 um gate length and 54 um gate width. The gate voltage parameter was given from –0.5 V to 1.1 V for every 0.2 V on I_D - V_D characteristics. Regrettably, they were not better to be operated as Tr, because that the brake down was appeared from 1 V toward 2 V. Moreover, the drain current was a bit poor, and S parameter of S Slope was a little large. This result was considered that the leakage current at the gate insulator is large and destruction of the insulator is occurred to charge. The mobility was 73 cm²/V-s calculated from the maximal value of gm parameter as EOT = 1.69 nm. This is too small.

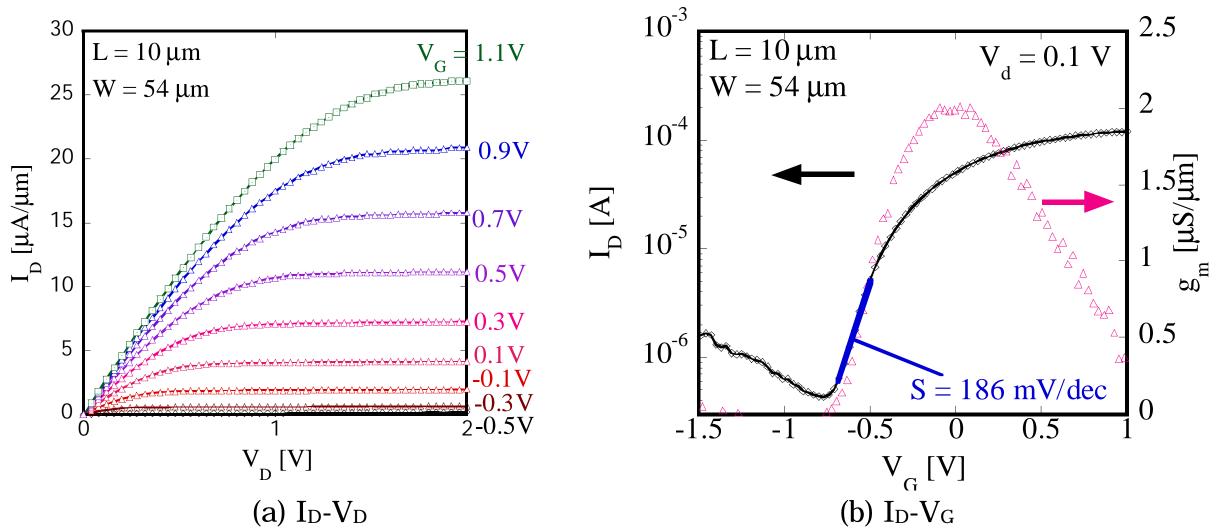


(a) I_D-V_D (b) I_D-V_G

Fig 4.2 the electrical characteristics of Lu_2O_3/La_2O_3/Si n-MISFET for as-deposited

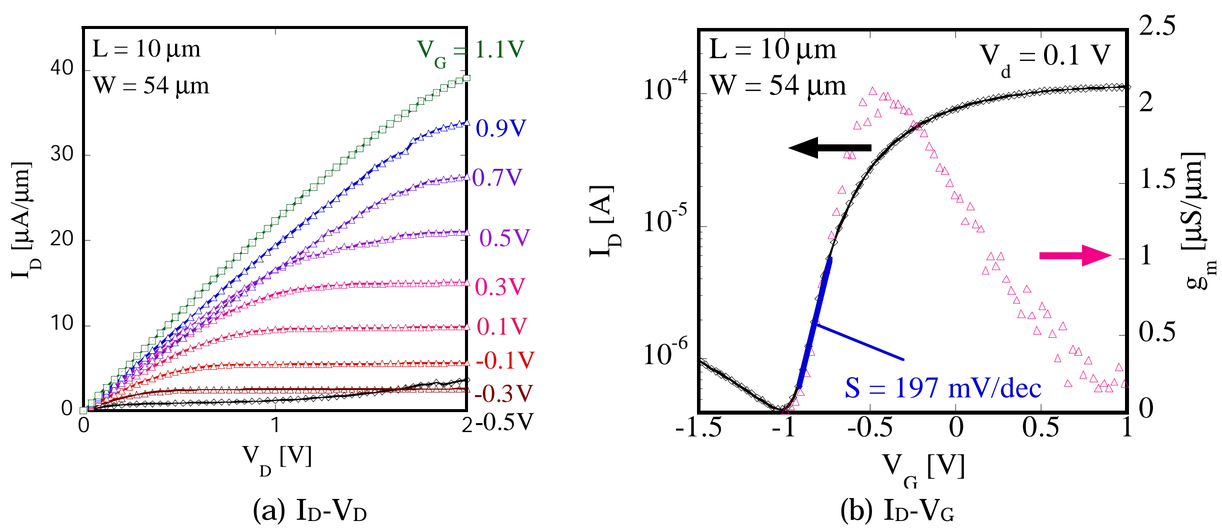
Next, the electrical characteristics of La_2O_3/Lu_2O_3/n-MIS Tr after annealing at 300°C in both of O_2 and N_2 ambient were measured. The case in O_2 and N_2 ambient were shown Fig. 4.3 and Fig. 4.4, respectively. The I_D –V_D characteristics of the films annealed in O_2 ambient was observed the saturation region of drain current, obviously. On the other hand, in N_2 ambient, the saturated lines of drain

currents of the films were not cleanly. It is considered that the defects of inner films are a lot of presence after annealing in N_2 ambient compare to in O_2. Therefore, S parameter of 300oC-annealed films in O_2 ambient was larger a little than that in N_2. However, the maximum of the gm characteristics in both of them was same mostly each other. The mobility of films annealed in O_2 and N_2 ambient was 93 (EOT was 1.63 nm) and 90 cm^2/V-s (EOT was 1.50 nm) , respectively.



(a) I_D-V_D (b) I_D-V_G

Fig 4.3 the electrical characteristics of Lu_2O_3/La_2O_3/Si n-MISFET for annealed at 300°C in O_2 ambient



(a) I_D-V_D (b) I_D-V_G

Fig 4.3 the electrical characteristics of Lu_2O_3/La_2O_3/Si n-MISFET for annealed at 300°C in N_2 ambient

In the Above results, it seems that electrical characteristics of n-Tr for 4 nm-thick films was prefer to anneal by RTA in O_2 ambient. However, it is possibility that the annealing temperature at more than 300°C was excellent characteristics for thin films. Additionally, it is considered that the optimum condition of annealing is 400°C rather than 600°C since the interfacial layer 300 to 400 °C annealing was grown but a little layer in the case of MIS capacitors. Thus, the film annealed at 400oC in O2 ambient was measured, and this result was greatest characteristics in previous results as expected. Figure 4.4 shows the sample. In the point of this result, it should be note that S parameter was very good small, which was 80 mV/dec. It is considered that this sample, which is stacked buffer La_2O_3 layer and covered by Lu_2O_3, has overcome the wet-process since S parameter means degradation of the transistor to operate quickly, for example, switch from ON to OFF. If this parameter is small, 80 – 90 ordinary for SiO_2-Tr, it would be operated correctly. Moreover, it found to be excellent condition that 400°C annealing as high-temperature is better than 300°C as low-temperature in spite of tending to be grown. The mobility of this sample was 154 cm²/V-s, and EOT was 1.93 nm.

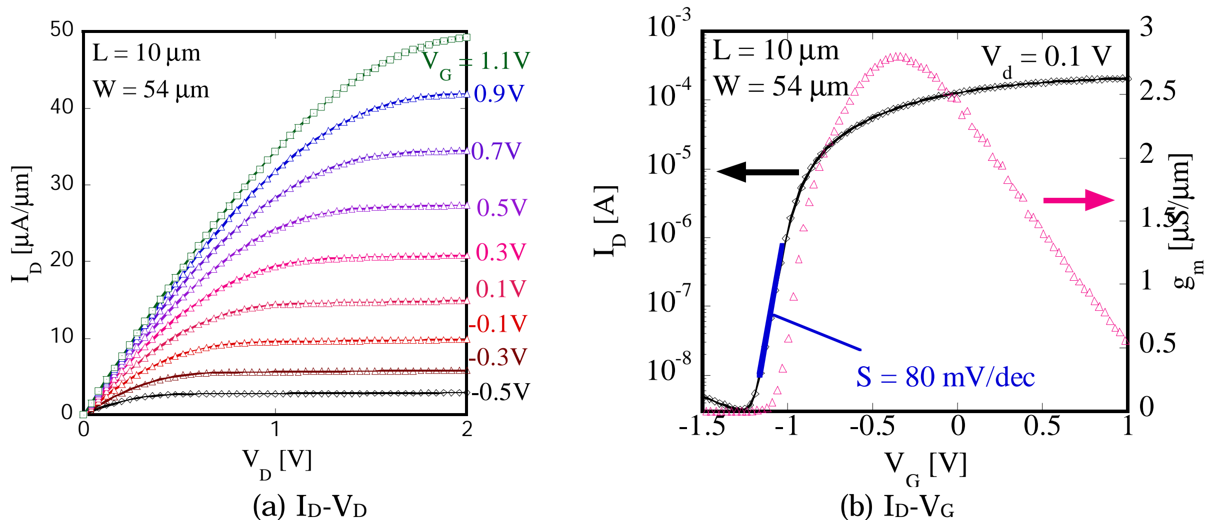
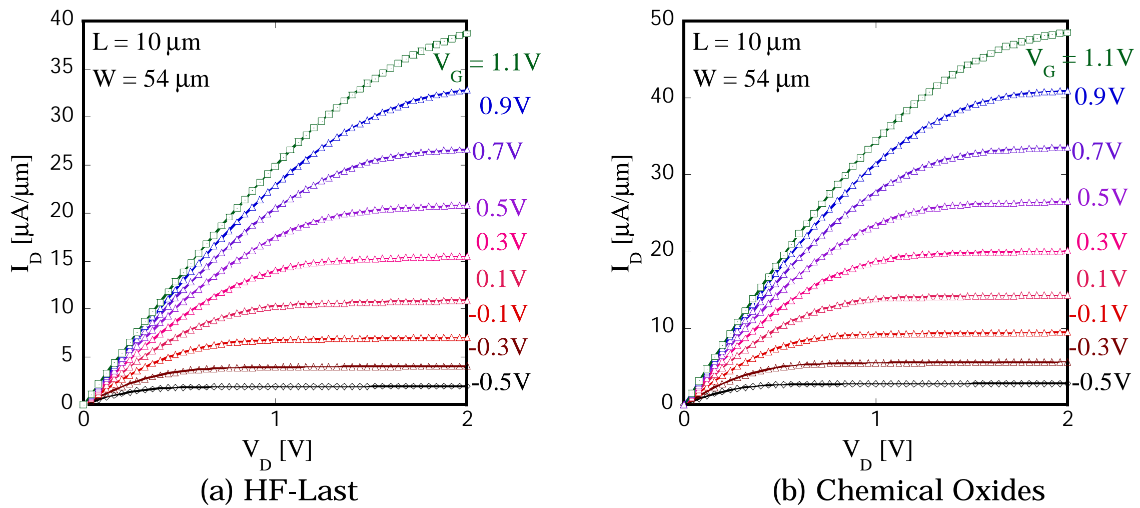


Fig 4.4 the optimum electrical characteristics of $Lu_2O_3/La_2O_3/Si$ n-MISFET for annealed at 400°C in O_2 ambient

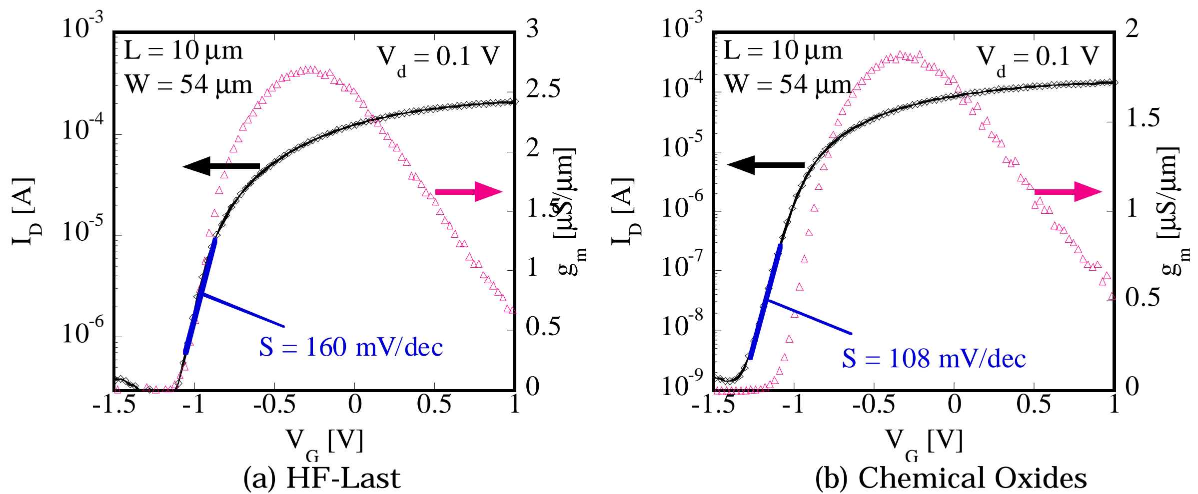
4.1.2 Characteristics of Single High-k Gate Insulator Transistors

As Comparison, 4-nm thick La_2O_3 n-Tr was measured. Figure 4.5 shows I_D-V_D characteristics of La_2O_3 transistor for HF-Last and Chemical Oxides. These characteristics were seemed that the MISFET for Chemical Oxides was excellent rather than for HF-Last.



(a) HF-Last (b) Chemical Oxides

Fig 4.5 I_D-V_D of La_2O_3/Si n-MISFET annealed at 400°C annealing in O_2 ambient



(a) HF-Last (b) Chemical Oxides

Fig 4.6 I_D-V_G of La_2O_3/Si n-MISFET at 400°C annealing in O_2 ambient

4.2 Discussion

In this chapter, we discussed the operation confirmation of device with the rare earth oxides dielectric thin films.

Making the transistor of stacked dielectric films, we obtained excellent electrical characteristics compare to that of single La_2O_3 films. Moreover, the electrical characteristics of $Lu_2O_3/La_2O_3/Si$ n-MISFET after 400°C annealing in O_2 ambient were superior to as-depoited films. This result was considered that the MISFET with stacked dielectric thin films have usefulness rather than that with the single dielectric thin films.

Chapter 5

Conclusion

5.1 Results of This Study

In this study, we aim to improve the electrical characteristics to gate dielectric thin films as stacked insulator. We carried out the measurements for MIS capacitor and MISFET with stacked dielectric films. These results show that excellent electrical characteristics compare to them with single dielectric films.

The conclusions of this study as follows:

The first, we investigated the MIS capacitor with single dielectric thin films of rare earth oxides, in this study, we used La_2O_3 and Lu_2O_3.

From these results, the electrical characteristics of the La_2O_3 thin films were improved by post anneal until low temperature such as 300°C. However, in the case of high temperature annealing such as 600°C, the electrical characteristics of that were deteriorated as the accumulation capacitance decrease. This thickness was 4 nm. Therefore, it was considered that the whole film became silicate. On the other hand, the electrical characteristics of the Lu_2O_3 thin films were not obtained general C-V curve until low temperature. Contrast to La_2O_3 thin films, the Lu_2O_3 thin films annealed at 600°C were improved the accumulation capacitance. It was considered that the interfacial layer such as SiO_2-rich was grown for RTA at 600°C.

The second, the effect of gate stacked dielectric thin films as structure of Lu_2O_3/La_2O_3/n-Si was investigated with MIS capacitors.

In this study, the improvement for the absorption of the single layer as La_2O_3 characteristics was observed from measurement for C-V and J-V characteristics. However, at 600°C annealing process, this effect was a little small due to interfacial growth that was thought to be the SiO_2-rich layer. Therefore, the optimum condition of stacked layer was at 300°C annealing process as low temperatures. In that case, the interfacial layer was considered to silicate layer mainly. Obtained excellent result is as follow;

EOT : 1.63 nm (under the 300oC annealing in O_2 ambient)
Leakage current : 5.84 x 10^{-4} (under the 300oC annealing in O_2 ambient)
RMS : 0.43 nm (under the 300oC annealing in O_2 ambient)

The third, the n-MISFET of gate stacked dielectric thin films were investigated for the structure of Lu_2O_3/La_2O_3/n-Si.

This result shows that the electrical characteristics of Lu_2O_3/La_2O_3/n-MISFET after 400°C annealing in O_2 ambient was superior to single La_2O_3 thin films as La_2O_3/n-MISFET. This result was considered that the MISFET with stacked dielectric thin films have usefulness rather than that with the single dielectric thin films.

5.2 Future Issues

In this study, we obtained excellent result for gate dielectric thin films of rare earth oxides. However, we remained some unresolved problems and new potential for rare earth gate dielectrics.

In these results, the effect of stacked gate dielectric thin films, were always annealed due to hysterisis and surface roughness. Surly, it is not required; since dependence of deposition condition was influence the as-deposited films for hysterisis and the surface roughness. Moreover, we were obtained the EOT under 1 nm. Therefore, in this point the more excellent characteristics are shown us and if it is improved as the next challenges.

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Appendix

This chapter is the appendix described the method of the peak separation of Si-2s spectrums. The equation and the method were shown Fig a .1, and the results of the separation were shown Fig a.2, Fig a.3 and Fig a.4 for La_2O_3/Si, Lu_2O_3/Si and Lu_2O_3/La2O_3/Si, respectively.

The parameters of the equation were explained the following

H : peak height

PG : percent of Gaussian

x : binding energy value

pp : the peak's center point

FWHM : Full Width at Half Maximum of the peak

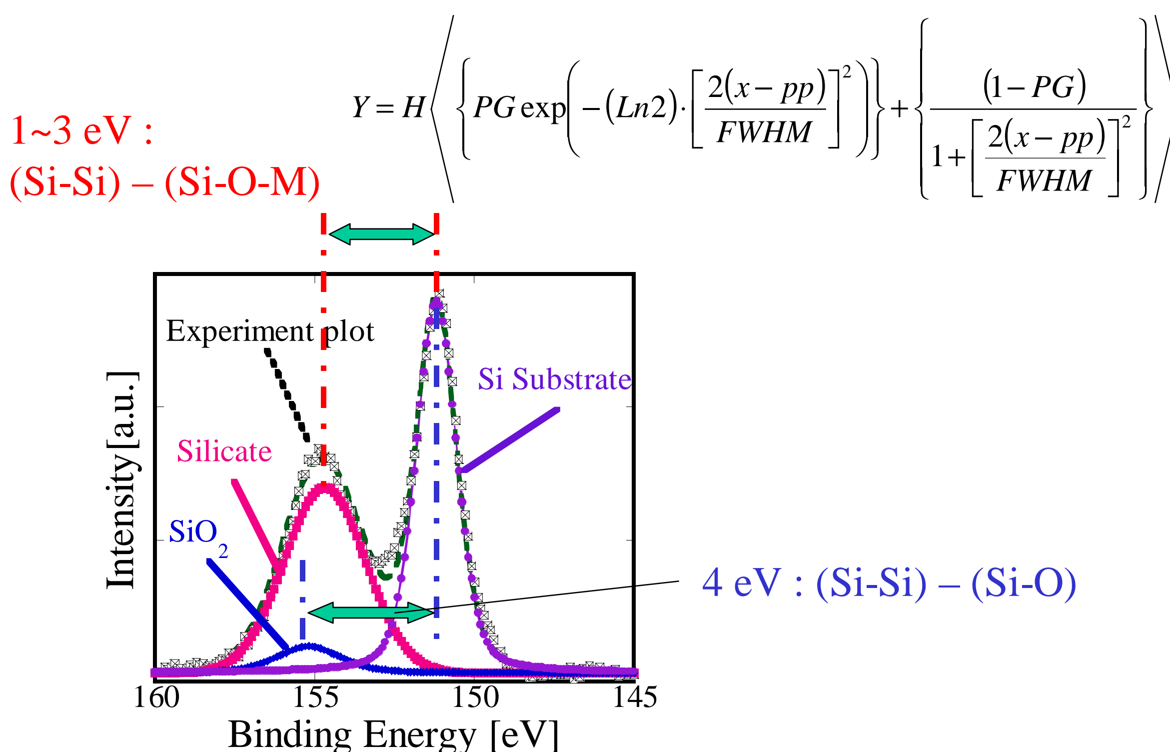

Fig a.1 the peak separated method

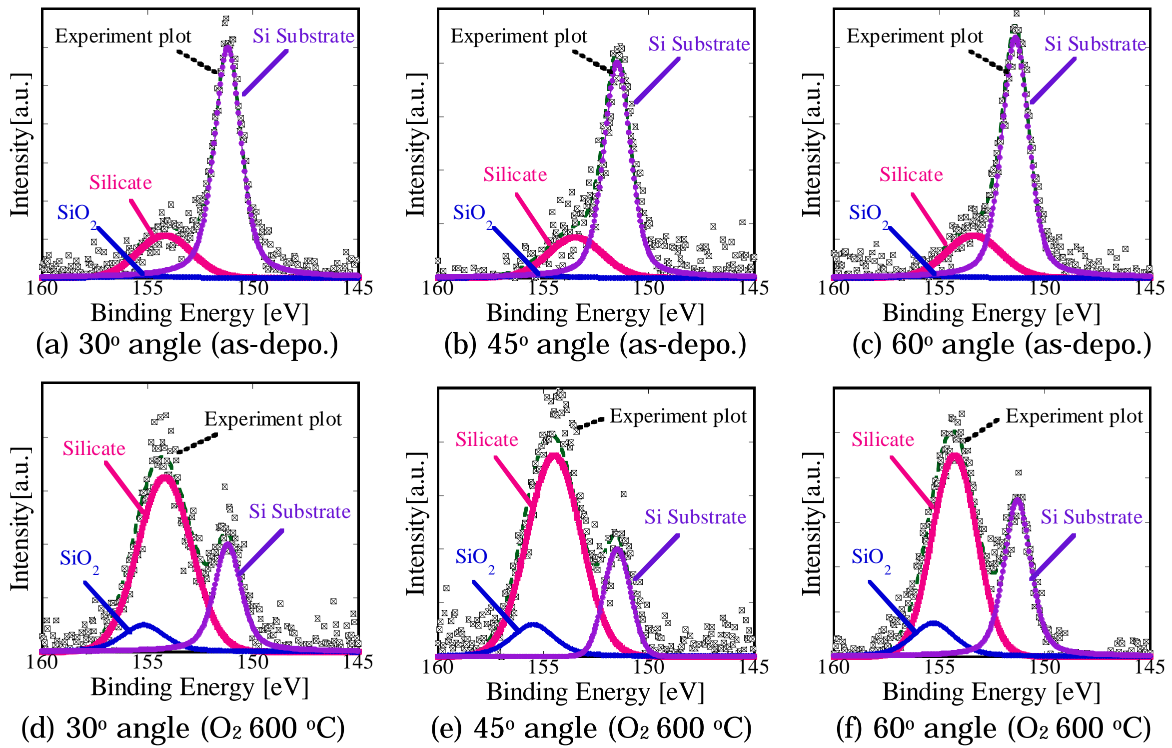

Fig a.2 peaks separated Si-2s spectrums of La_2O_3/n-Si

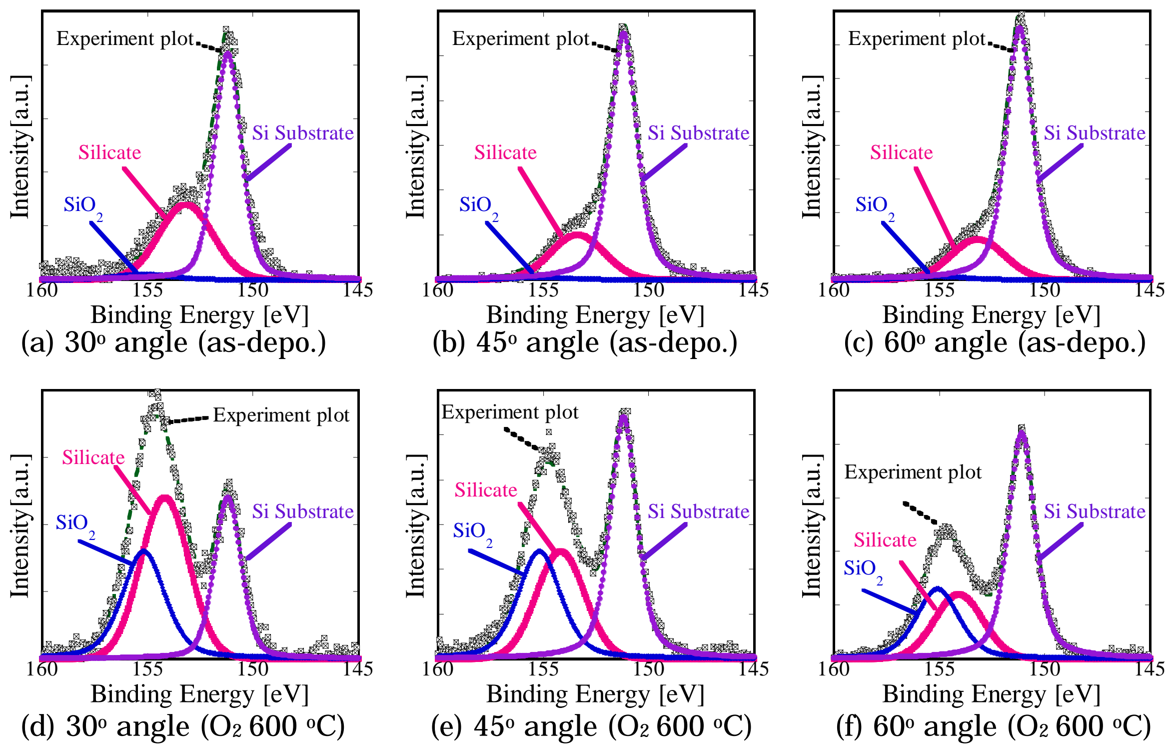

Fig a.3 peaks separated Si-2s spectrums of Lu_2O_3/n-Si

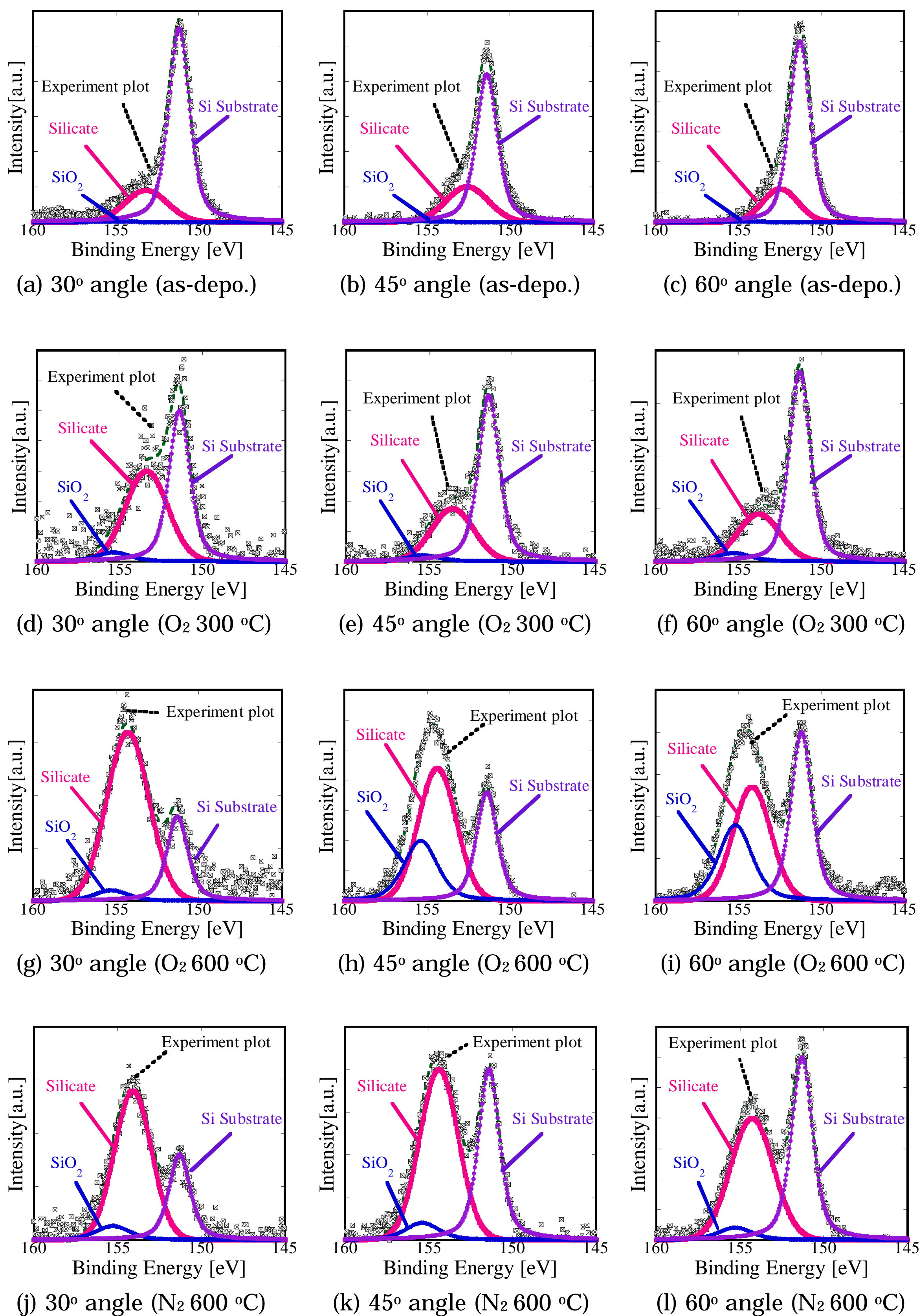

Fig a.4 peaks separated Si-2s spectrums of Lu_2O_3/La_2O_3/n-Si