Master Thesis

A Study on the Ultra-High Vacuum Anneal Method for the Rare Earth Gate Dielectrics

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Chapter 1

Introduction

1.1Background of This Study

Our social life has been changed well with the development of the recent Si-LSI technology, and progress of computerization in various fields. Development of LSI greatly depends on the high-characterization of semiconductor devices (Si-MOSFET) that constituting LSI circuit system. The performance of MOSFET is improved according to the scaling law [1]. As shown in Fig.1.1 and Table 1.1, by miniaturizing the physical size of the device with the same factor S according to the scaling method, high-speed switching operation is obtained resulting from shrinking the channel length. The power consumption is also reduced. Simultaneously, the operation speed of the circuit becomes higher by increasing the number of the devices that integrated on the LSI, so the whole performance of the LSI system is improved in terms of high-speed, high frequency, and so on. Therefore, the research for the device downsizing has been done in the world universities and companies.

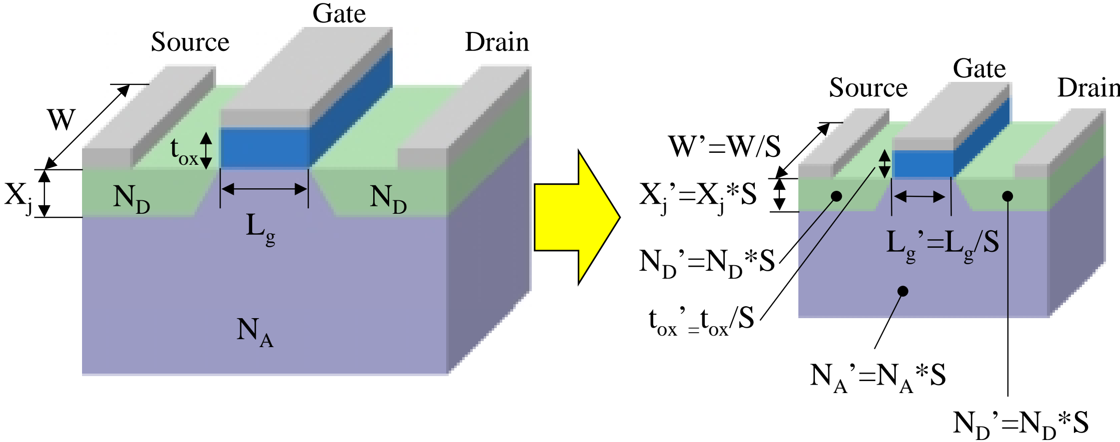


Fig. 1.1: Scaling Method

Table.1.1: Scaling of MOSFET by a scaling factor of S

Quantity	Before Scaling	After Scaling
Channel Length	L_g	$L'_g=L/S$
Channel Width	W	W'=W/S
Device Area	A	$A'=A/S^2$
Gate Oxide Thickness	t_{ox}	$t_{ox}'=t_{ox}/S$
Gate Capacitance Per Unit Area	C_{ox}	$C_{ox}'=S*C_{ox}$
Junction Depth	X_j	$X_j'=X_j*S$
Power Supply Voltage	V_{DD}	$V_{DD}'=V_{DD}/S$
Threshold Voltage	V_{th}	$V_{th}'=V_{th}/S$
Doping Densities	N_A	$N_A'=N_A*S$
	N_D	$N_D'=N_D*S$

With the miniaturizing the device, thickness of the gate insulator becomes thinner rapidly. According to International Technology Roadmap for Semiconductor (ITRS) that is used commonly as the industrial timetable of the technical development, the film thickness becomes below 1 nm within several years (Table. 1.2). It is correspond to a few atomic layers in the case of SiO_2, which is used for the gate dielectrics. In such a ultra thin film domain, the direct tunnel leakage current through the gate insulator increases, and it causes the serious trouble to the device operation.

Then, in order to overcome the problem, the trend that introduces new materials replaced with SiO2 is increasing. It is the attempt that the leakage current can be suppressed by using the high dielectric constant (high-k) material as the gate insulator because of its physical thickness with keeping the electrical equivalent oxide thickness (EOT) small (Fig. 1.2). As the candidates for the high-k thin film materials, the metal oxides of the elements shown in Fig. 1.3 are expected in consideration of non-toxicity, non-radioactivity and the chemical stability at the contact with Si substrate. Various high-k materials have been investigated for the alternative gate oxide of SiO_2 [3-5]. Recently, good characteristics of the rare earth oxide thin films have been reported [6-9]. They are thought to be promising candidates for the next generation gate dielectrics as well as the other high-k materials such as HfO_2, ZrO_2, and Al_2O_3. Typical properties of the high-k materials including rare earth oxides are shown in Table. 1.3.

Table.1.2: High-performance logic technology requirements

Year	2005	2006	2007	2010	2016
T_{ox} (nm)	0.8~1.3	0.7~1.2	0.6~1.1	0.5~0.8	0.4~0.5
Gate Leakage (A/cm^2)	$9.4x10^2$	$2.5x10^3$	$4.0x10^3$	$1.7x10^4$	$1.1x10^5$

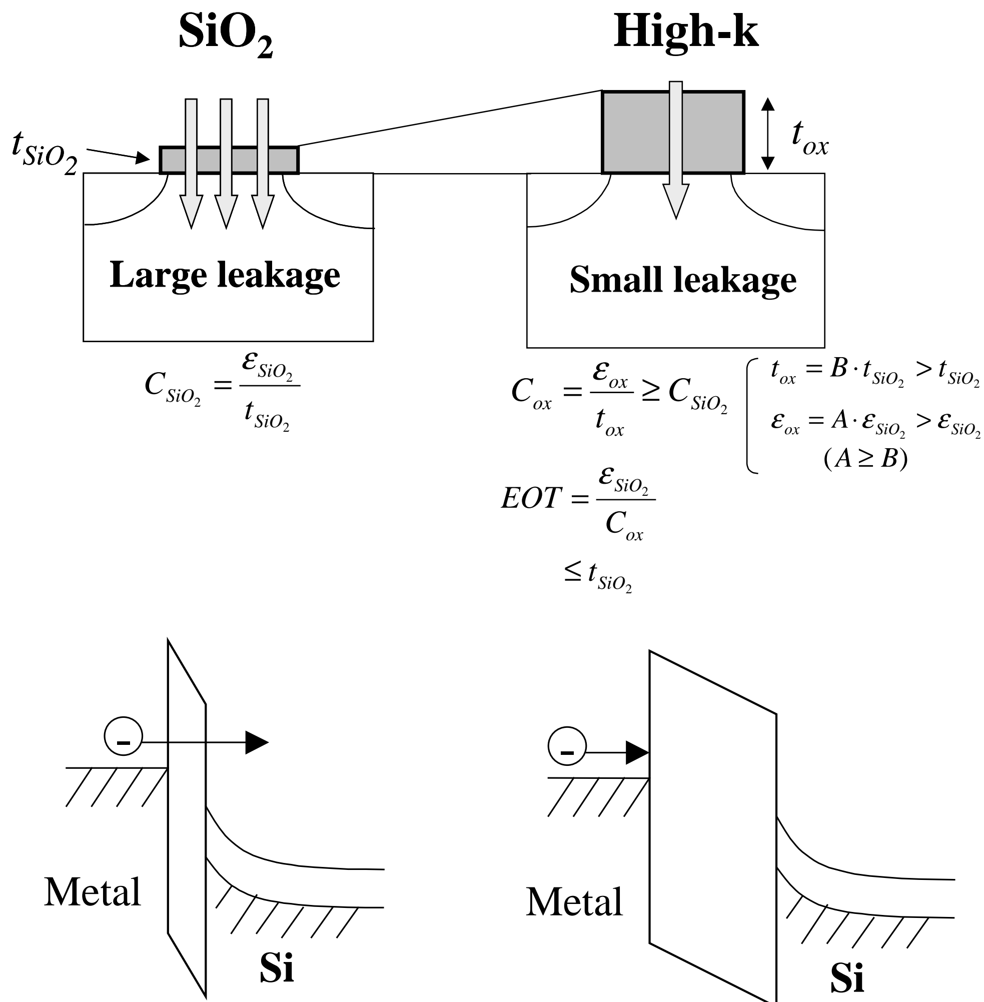


Fig. 1.2: Difference between the cases using SiO_2 and high-k material for gate insulator in the metal-insulator-semiconductor (MIS) structure

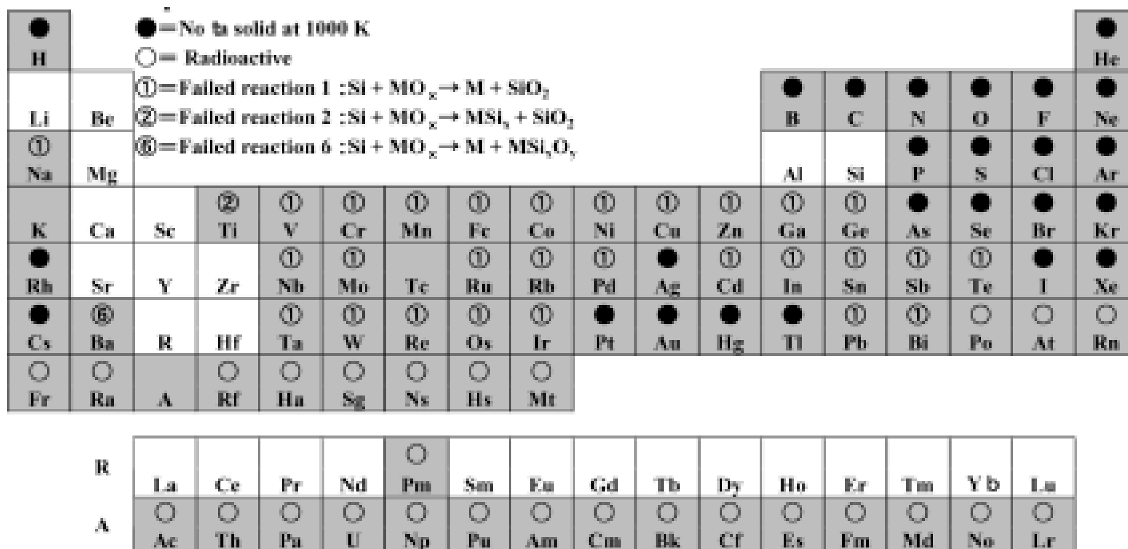


Fig.1.3: Candidates of the elements which can be used for the high-k gate insulators

Table.1.3: Properties of typical high-k materials

Materials	SiO_2	Al_2O_3	La_2O_3	Pr_2O_3	Gd_2O_3	HfO_2	ZrO_2
EOT (nm)	0.8	1.5	0.48	1.4	1.5	0.8	0.8
Contact stability with Si (kJ/mol) $Si+MO_x \rightarrow M+SiO_2$	Stable	+63.4	+98.5	+105.8	+101.5	+47.6	+42.3
Lattice energy (kJ/mol)	13125	15916	12687	12938	13330		11188
Bandgap (eV)	9	6 – 8	5.4	3.9	5.4	5.7	5.2 – 7.8
Structure	Amorphous	Amorphous	Amorphous	Crystal T>700℃	Crystal T>400℃	Crystal T>700℃	Crystal T>400 - 800℃
κ	3.9	8.5 – 10	27	13	17	24	11 – 18.5

1.2Physical Properties of Rare Earth Oxides

All rare earth oxides take sesquioxide, and five types of polymorphism are found by present. At lower than 2000°C three type phases exist such as A, B and C (Fig. 1.4). Type A takes hexagonal system that has 7-coordinated rare earth ions. Type B has monoclinic, which is distorted system of type A. Rare earth ions take 6 or 7-coordination in this type. Type C has cubic system of bixbyite, in which rare earth ions take 6-coorination. At higher than 2000°C phase H and X exist. Fig. 1.5 shows the temperature domains where five type polymorphisms exist stably.

The lattice energies and band gap energies of rare earth oxides are shown in Fig. 1.6. The lattice energy becomes larger with the increase of the element number. A periodicity appears in the band gap energy, and La, Gd and Lu take maximum point.

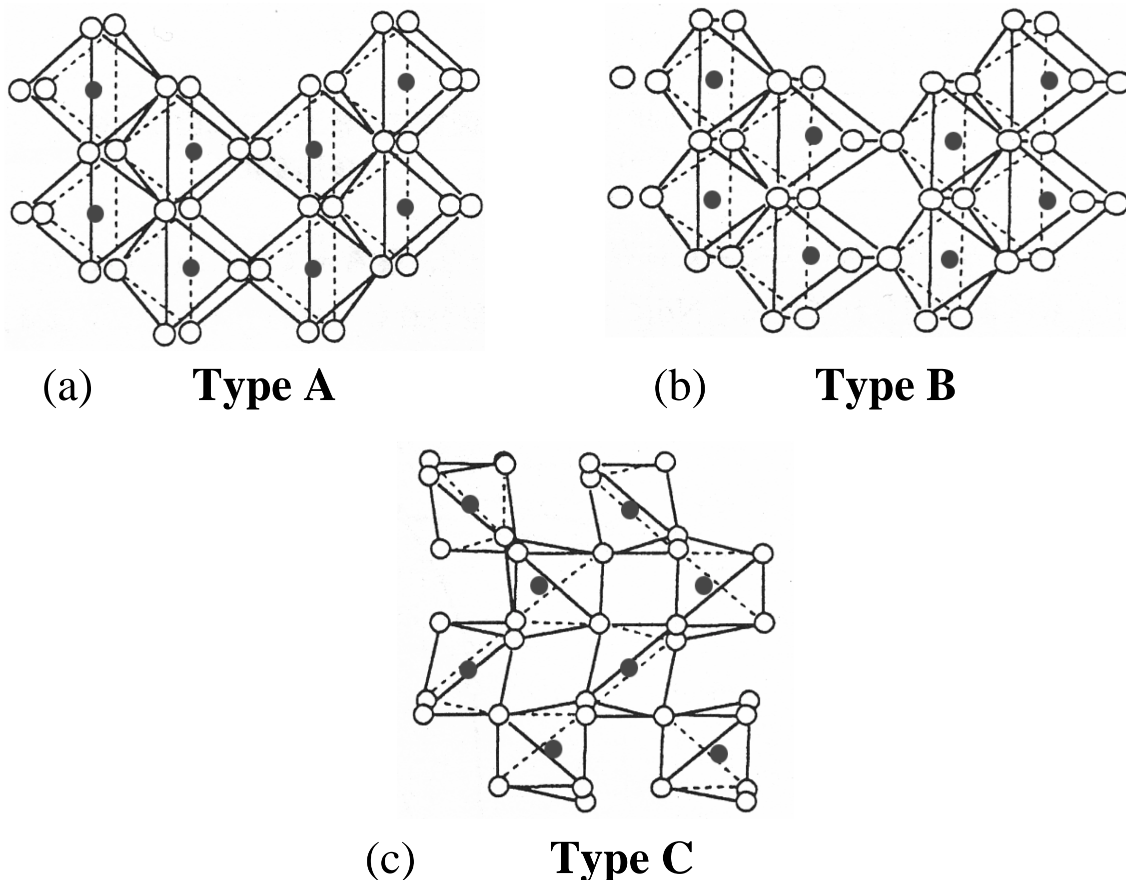


Fig.1.4: Crystal structures of rare earth oxides (a) type A, (b) type B and (c) type C

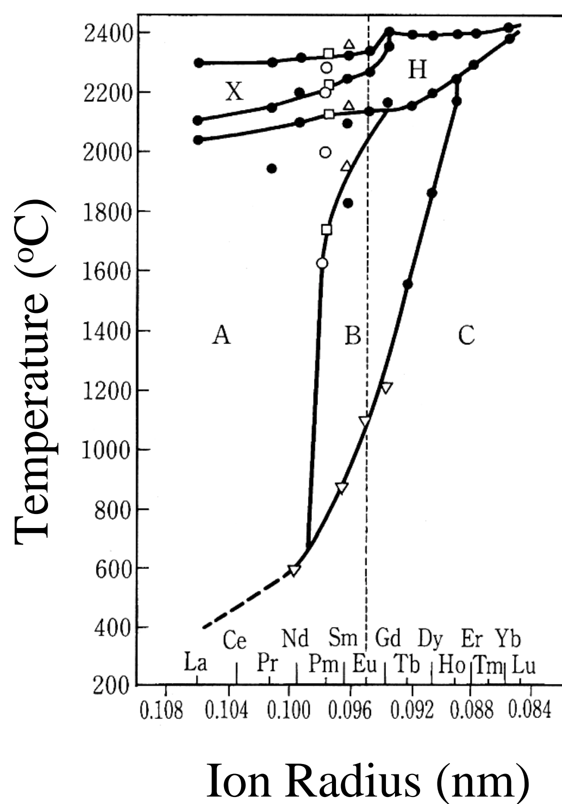


Fig.1.5: Temperature domains where five type polymorphisms exist stably

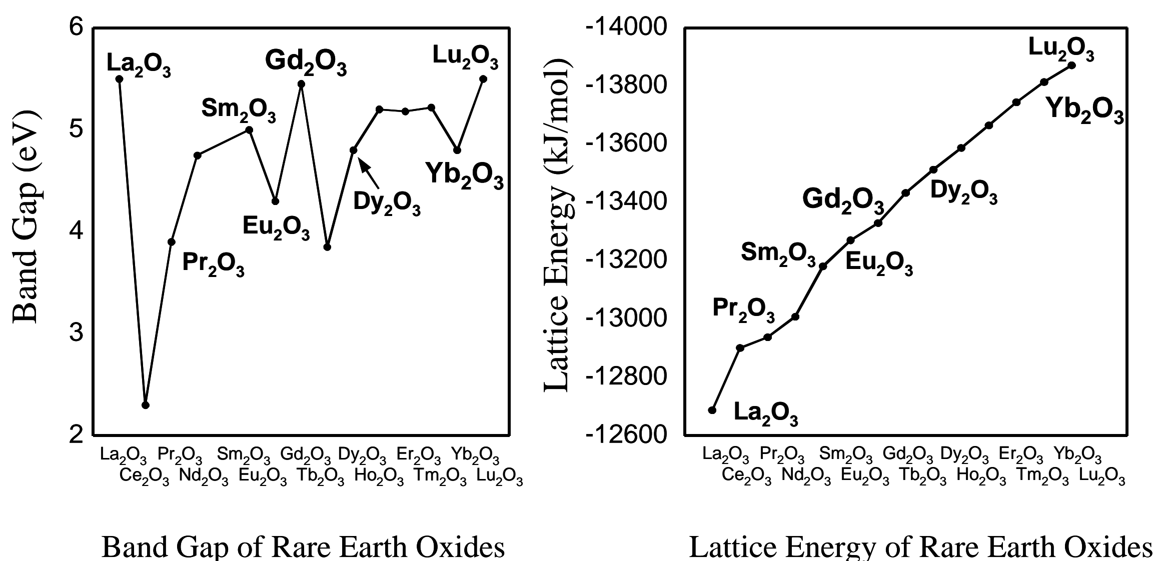


Fig.1.6: (a) Lattice energies and (b) band gap energies of rare earth oxides

1.3Purpose of This Study

One of the serious problems for the high-k gate insulator is thermal stability on Si substrate. As shown in Fig. 1.3, there are several candidates that are thought to be theoretically stable on Si. However, it cannot be said necessarily that they are stable because the thermodynamic property of thin film is different from the bulk case by the influences of the difference from the stoichiometric composition, interfacial stress and so on. In general, high-k materials react with Si easily during the annealing process after deposition, and low dielectric interfacial layer consisting of SiO_2 or silicate is formed. It is bad influence of decreasing the oxide capacitance to high-k thin films (Fig.1.7). One of the evaluation bases of electrical characteristics for the high-k thin films is the relation of EOT and leakage current, and small EOT and low leakage are expected (Fig. 1.8). EOT is expressed as equation 1.1, so decreasing oxide capacitance is equivalent to increasing EOT. Therefore, formation of interfacial layer is a serious problem for the characteristics of thin films.

$$EOT = \frac{\varepsilon_{SiO_2}}{C_{ox}} \qquad (1.1)$$

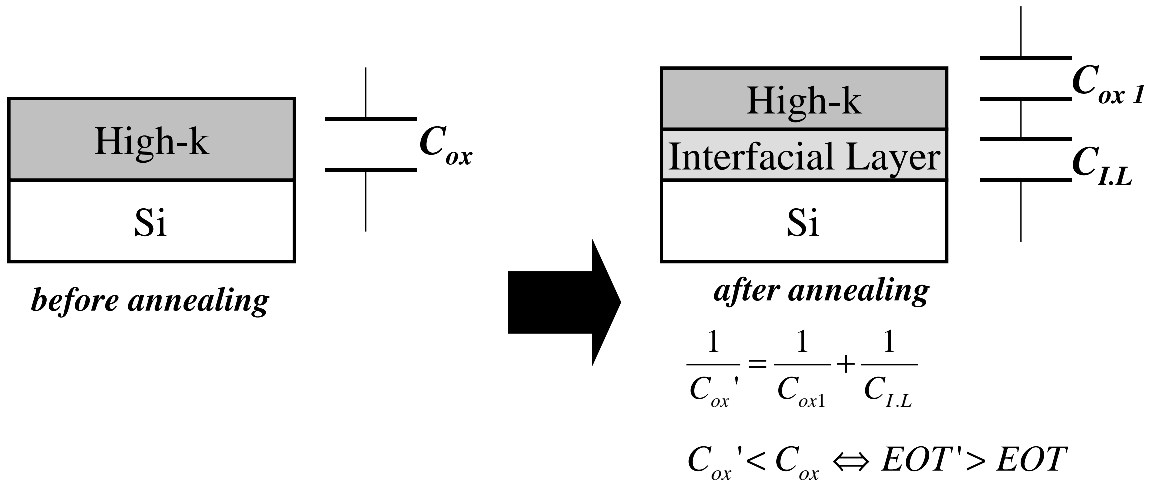


Fig.1.7: Change of the electrical characteristic by forming of the interfacial layer

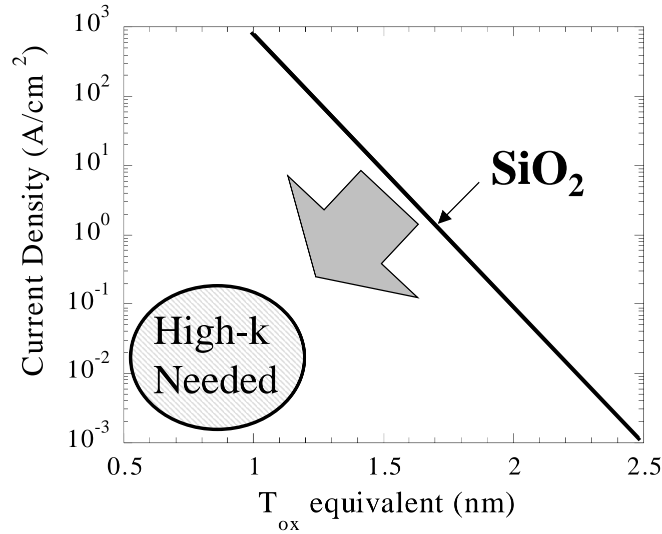
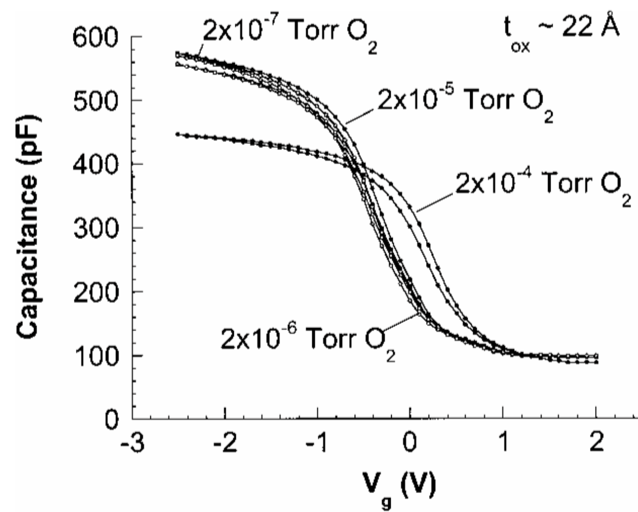


Fig.1.8: EOT-J characteristic for which high-k thin film is expected

High-k thin films are formed on Si substrate by deposition. In general, as-deposited film has many defects or traps in itself. Since the electrical characteristics show huge hysteresis in the C-V curve, the deposited films need to be annealed to suppress the charge traps. Therefore, it is necessary to investigate the annealing method that improves film quality with suppressing the formation of interfacial layer. It is considered that interfacial layer formation is closely related to the surrounding atmosphere during the annealing. Recently, it was reported that the capacitance degradation was controlled by lowering the partial pressure of O_2 for La_2O_3 thin film (Fig. 1.9) [10]. Purposes of this study is to investigate the effect of ultra-high vacuum annealing method for rare earth oxide thin films and explore the condition to form the thin film which has small EOT and low leakage characteristics. In this work, effect of ultra-high vacuum anneal was investigated using Dy_2O_3 thin films as the typical material in the rare earth oxides. It is one of the promising materials, and good characteristics were reported [11].



J.-P. Maria et al., JAP, vol. 90, # 7, (2001)

Fig.1.9: Set of C-V Curves for a 20 Å thick La_2O_3 film deposited on (001) Si with an ~10 Å thick chemical SiO_2 interface. The samples were exposed to a 900°C anneal under oxygen partial pressures indicated in the figure.

Chapter 2

Fabrication and Characterization Methods

2.1. Fabrication Method

The electrical characteristics of the thin films were evaluated by using Metal-Insulator-Semiconductor (MIS) capacitor. The fabrication flow of MIS structure is showed in Fig. 2.1.

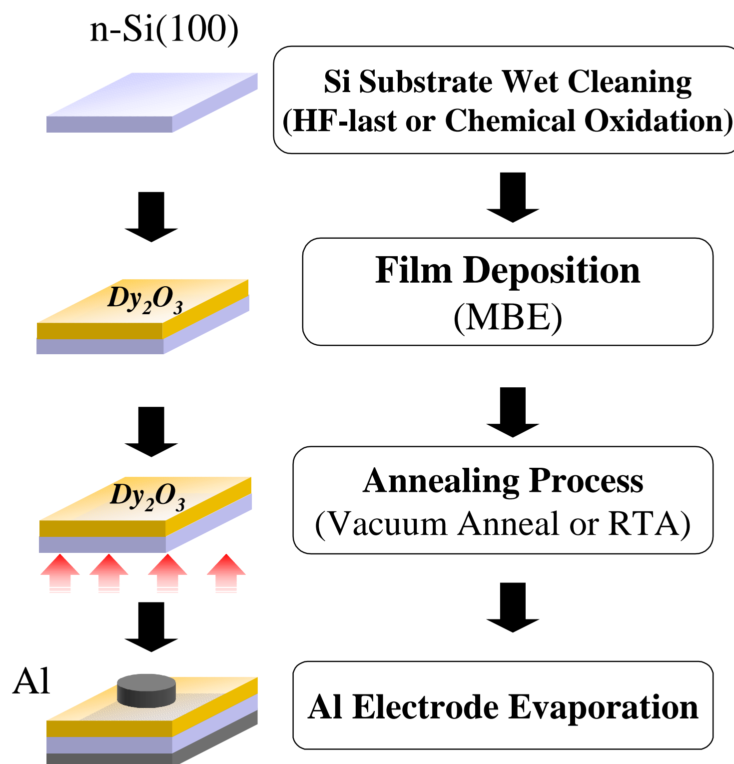


Fig. 2.1: Fabrication method of MIS capacitor.

2.1.1. Si Substrate Wet Cleaning

For deposition of high quality thin films, ultra clean Si surface is required, without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination, The theoretical resistivity of pure water at 25°C is 18.25 MΩcm. Ultra-pure water (UPW) systems used in this study provided UPW with more than 18.2 MΩcm resistivity.

In this study, the substrate cleaning process was based on RCA cleaning process, was proposed by W.kern et al. But some steps were reduced. The steps were shown in Fig.2.6. First, a cleaning steps in a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4:H_2O_2=4:1) was performed to remove any organic material and metallic impurities. And then, the native or chemical oxide was removed by diluted hydrofluoric acid (HF:H_2O=1:100). Finally, the cleaned wafer was dipped in DI water and loaded to chamber immediately.

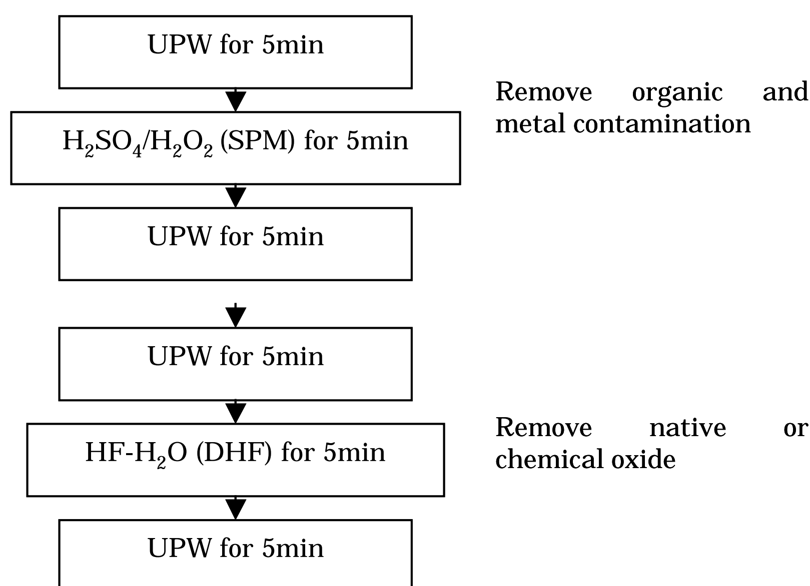


Fig. 2.2: Si substrate wet cleaning.

2.1.2 Chemical Oxidation

In order to reduce leakage current and interfacial layer, chemical oxidation on Si surface is attempted. In this study, Oxidation method is used by dipping 30% H_2O_2 that seem to make suitable oxide layer and oxidation rate is 0.5nm by 30min at room temperature.

After cleaning process, Si substrate was dipped in H_2O_2 and then substrate was dipped in UPW and load to chamber immediately. The steps were shown in Fig.2.7.

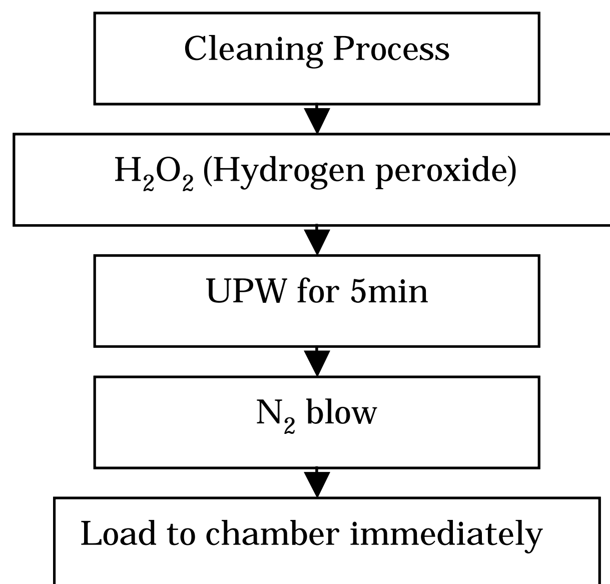


Fig. 2.3: Chemical oxidation.

2.1.3. Molecular Beam Deposition (MBD)

MBD method is one of the PVD (physical vapor Deposition) methods using molecular beam epitaxy (MBE) system. The material is evaporated by using E-beam and deposited on Si substrate. Only molecular beam is used for depositing in ultra high vacuum (~10^{10} Torr). This method prevents contaminants in film that C-VD method has and provides controllable nanometer order thin films. This method is suitable for research basic characteristics of high-k thin films.

Figure 2.4 and Fig.2.5 shows MBE system, which was used in this study. There are two chambers and four pumps to make ultra high vacuum, four E-guns in deposition chamber and two power supplies that are capable to evaporate two materials in the same time. (Not use plural E-guns in this study.) And there are crystal meter for measurements thickness and RHEED for Analysis.

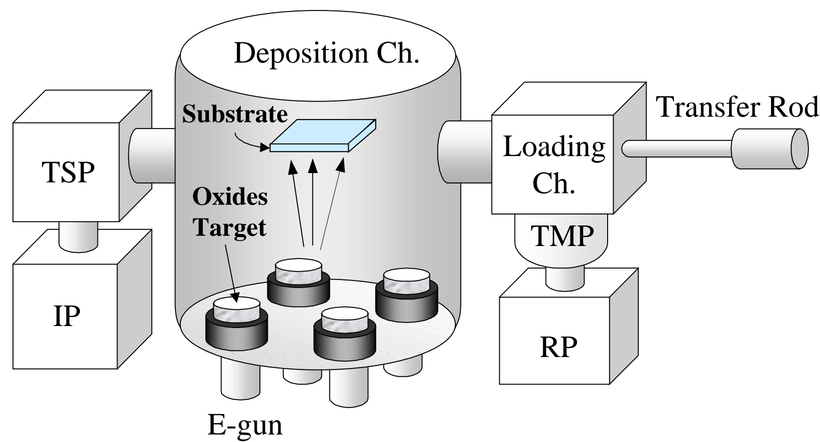


Fig. 2.4: MBE System

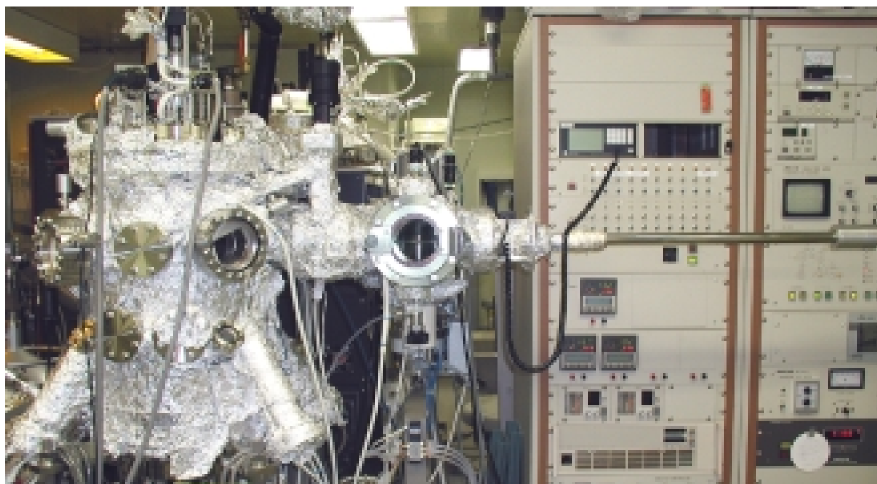


Fig. 2.5 MBE System

2.1.4. Rapid Thermal Annealing (RTA)

In this study, RTA (rapid thermal annealing) is used for thermal process after depositing process. The silica tube filled O_2 or N_2 (flow rate are 1.2 L/min) in atmospheric pressure. Therefore it is impossible to remove contaminant gas perfectly in tube. Equipment image was show in Fig.2.6.

Fig. 2.6: RTA (MILA3000 made in SINKU-RIKO company) (right)

2.1.5 Vacuum Evaporation Method

High-vacuum evaporation was simple method for forming metal electrode like Pt, Al and Ag. In high vacuum chamber, metal source is evaporated by thermal heating with high voltage and is deposited on substrate covered metal mask. In this study, tungsten electrical resister is used for heating Al source that has low melting point (660.37^{o}C) in case by n type substrate and Ag source (961.93^{o}C). This method is possible to contaminate films. Equipment image was show in Fig.2.7.

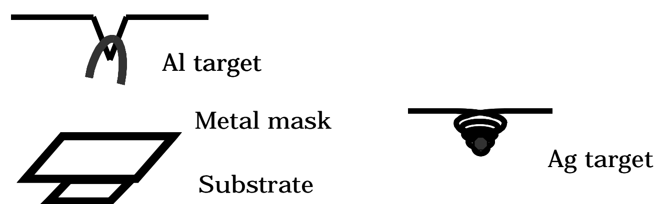


Fig. 2.7: Metal electrode deposition

Fig.2.8: High-vacuum bell jar for metal deposition

2.2 Characterization Methods

This sub chapter introduces methods for MIS capacitors characterization

2.2.1 Electrical Measurement

2.2.1.1 C-V measurement

Fig.2.9 shows ideal high frequency C-V characteristics for Metal-Insulator-Semiconductor (MIS) structure. Fig.2.9 shows films on p- type Si. Threshold voltage depends on work function of metal and semiconductor. When typical electrode of Al is used for n-type Si, threshold voltage in C-V characteristic is about 0V. On the other hand, when Al or Pt is used for p-type Si, threshold voltage in C-V characteristic is about –0.9V or 0.2V. But experimentally threshold voltage were generally shifted by

Interfacial state affects the slope of the curve, and threshold voltage changes depending on fixed charge. In addition, C-V characteristic shows hysteresis depending on charge pumping or movable ion in insulator as shown in Fig.2.10 (a) or (b).

In this study, C-V characteristics were measured by 4284A precision LCR meter made by HP. Measurement frequency was 1 kHz~1MHz.

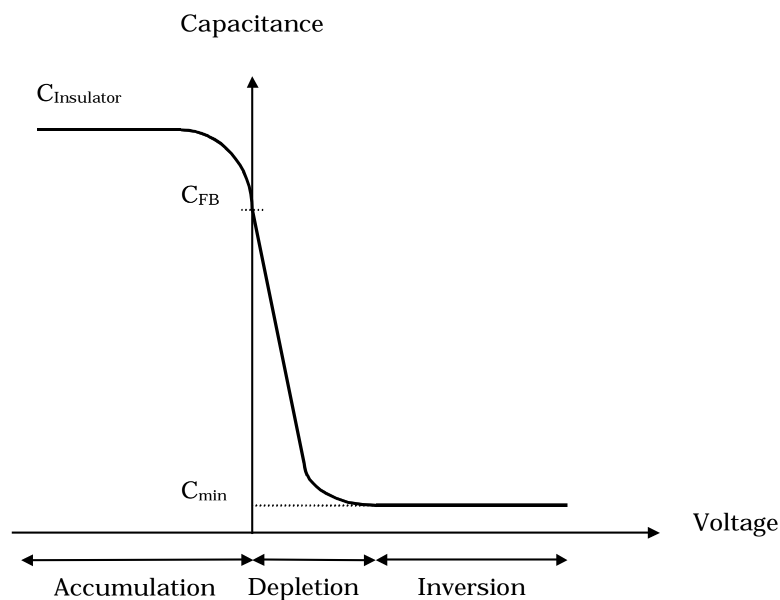


Fig. 2.9: Ideal C-V curve of MIS capacitor at high frequency

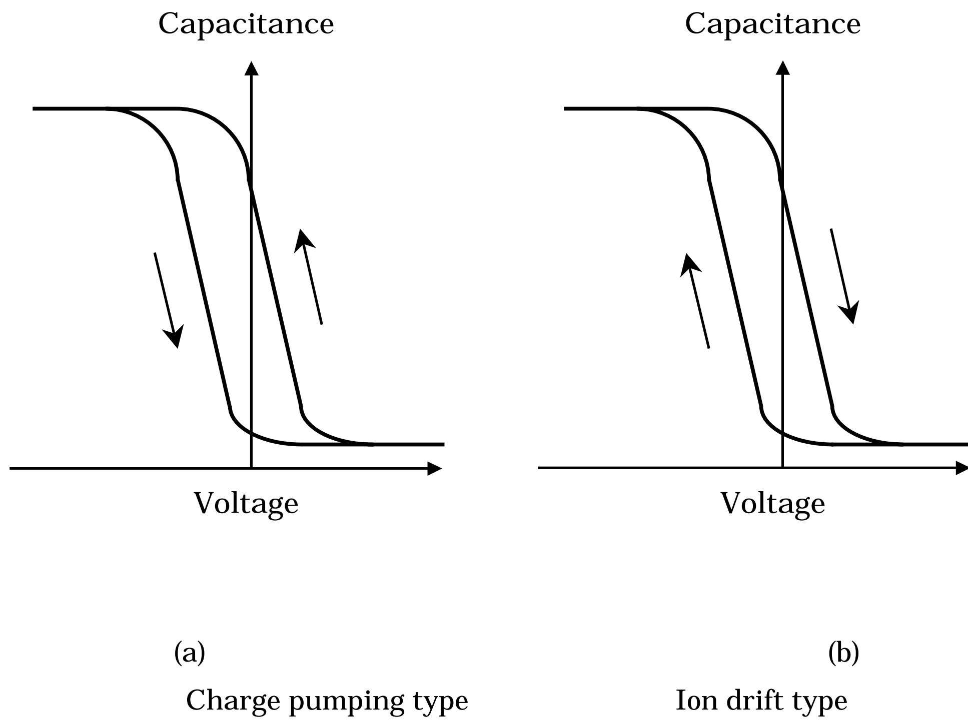


Fig. 2.10: Hysteresis in C-V characteristic

Fig. 2.11: LCR meter HP 4284A.

2.2.1.2 I-V measurement

The one of important electrical properties to estimate high-k films is I-V characteristics. I-V characteristics were measured to evaluate leakage current characteristics. They were measured by 4156C type precision semiconductor parameter analyzer made by HP.

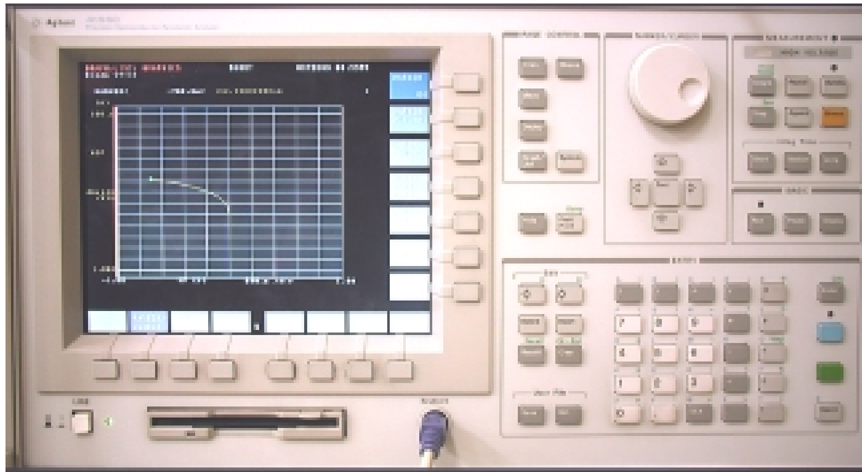


Fig. 2.12: Semiconductor parameter analyzer HP 4156C.

2.2.2 Atomic Force Microscopy (AFM)

AFM enables to measure surface morphology by utilizing force between atoms and approached tip. The roughness of sample surface is observed precisely by measurement of x-y plane and z. Fig.2.11 shows the principle of AFM.

Tip is vibrated during measurement, and displacement of z direction is detected. This method is called tapping mode AFM (TM-AFM). Resolution limit for normal AFM is 5 ~ 10nm depending on distance between sample surface and tip. On the other hand, resolution limit for TM-AFM is depended on size of tip edge. Thus, resolution limit for TM-AFM is about 1nm.

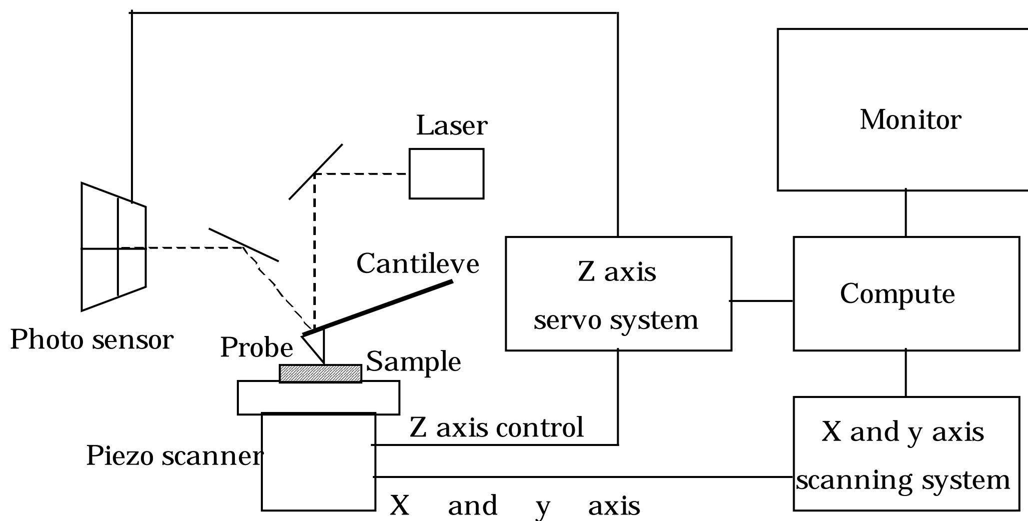


Fig.2.13 Principle of AFM

2.2.3 X-ray Photoelectron Spectroscopy (XPS)

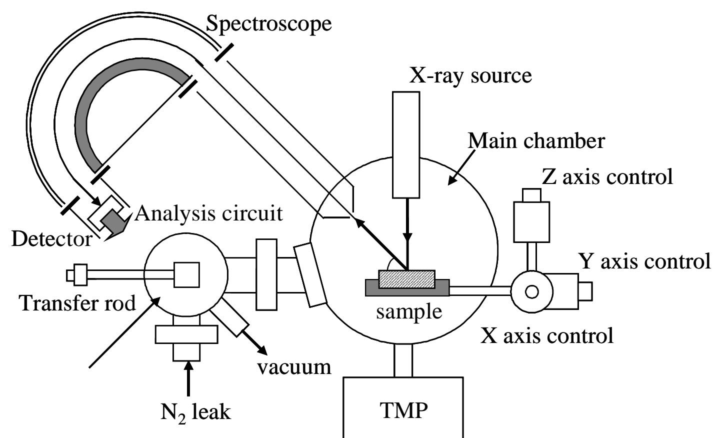
XPS, also known as Electron spectroscopy for chemical analysis (ESCA) is one of the availability methods that estimate thin film and Si interface.

Fig.2.14 shows the schematic drawing of XPS equipment that was used in this study. During analysis, the pressures of main chamber were about 10^{-9} Torr vacuums with turbo pomp. Surface analysis by XPS is accomplished by irradiating a sample with monoenergetic soft X-ray and analyzing the energy of the detected electrons. Non-monochromatic MgKα (1253.6 eV) X-ray is used in this study. The method is illustrated with the energy band diagram in Fig.2.15. This photoelectron has limited penetrating power in a solid on the order of 1-10 μm. They interact with atoms in the surface region, causing electrons to be emitted by the photoelectric effect. The emitted electrons have measured kinetic energies given by

$$KE = h\nu - BE - \phi_s \qquad (2.1)$$

where hυ is the energy of the photoelectron, BE is the binding energy of the atomic orbital from which the electron originates and ϕs is the spectrometer work function (4.8 eV).

The binding energy may be regarded as the energy difference between the initial and final states of the ion from each type of atom, there is a corresponding variety of kinetic energies of the emitted electron. Because each element has a unique set of binding energies, XPS can be used to identify and determine the concentration of the elements in the surface. Variation in the elemental binding energies (Chemical shift) arises from difference in the chemical potential and polarizability of compounds. These chemical shifts can be used to identify the chemical states of the materials being analyzed.



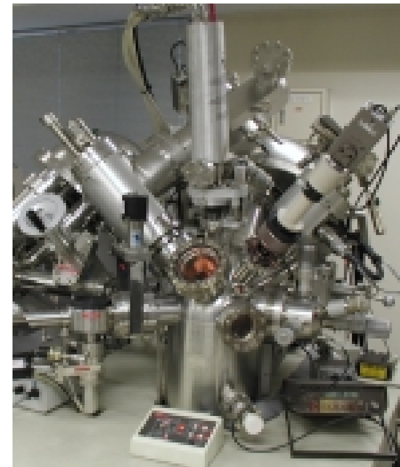


Fig. 2.14: XPS schematic, physical electronics PHI5600 ESCA spectrometer.

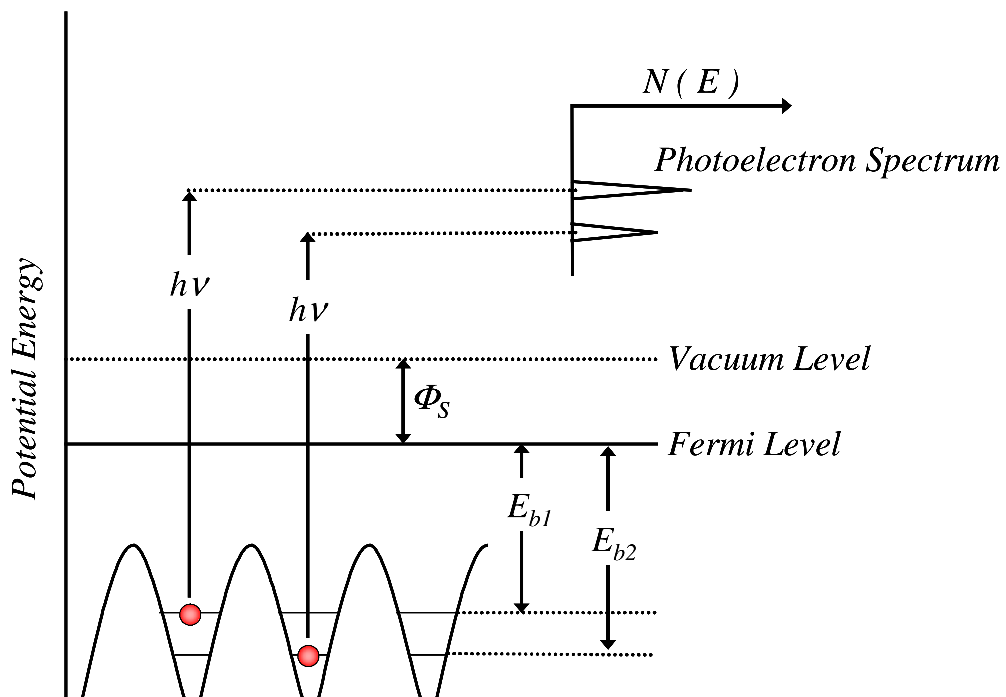


Fig. 2.15: Illustration of measurement method with the energy band diagram.

2.2.4 Ellipsometer

Ellipsometory is the method to estimate the optical property of material or surface film thickness measuring the change of polarization condition caused by the reflection of light. Generally, when light is illuminated to a material, the polarization condition of incident light and reflected light are different. This method evaluates the surface condition from this difference. P component of polarized light is horizontal to the plane formed by incident and reflected light and vertical component is S. Ordinary non-polarized light becomes linear polarized light in which the phase and intensity are the same between P and S polarization component when it was passed through 45°-declined polarizer. When the linear polarized light is illuminated to the material, phase different Δ arises between P and S component in the reflected light. Also, the reflection intensity is different between P and S component of polarized light because the reflectance of P and S component is different at the material surface (Fig. 2.16).

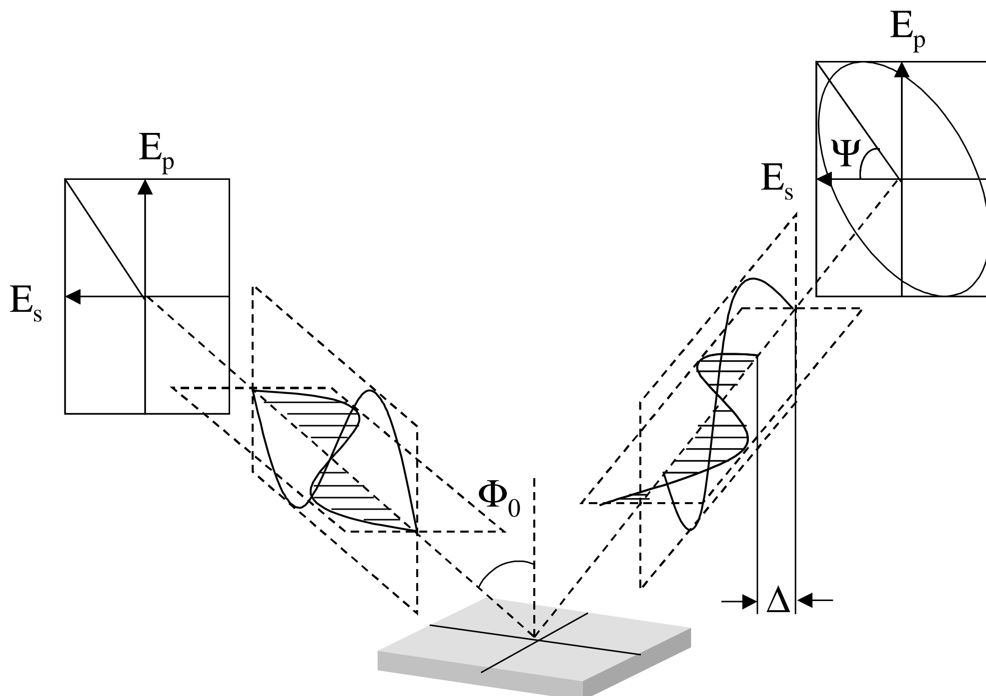


Fig. 2.16: Illustration of the measurement principle for ellipsometer.

P and S component in electric field vector of the reflected light are given by

$$E_p = a_p \cos(\omega t - \delta_p)$$
$$E_s = a_s \cos(\omega t - \delta_s) \qquad (2.1)$$

Here, a_p, a_s, are amplitudes of P and S direction respectively. δ_p and δ_s express the phase deviations in the each component. Introducing the relation δ_p - δ_s = Δ, the following equation is obtained.

$$\frac{E_p^{\ 2}}{a_p^{\ 2}} + \frac{E_s^{\ 2}}{a_s^{\ 2}} - 2\frac{E_p}{a_p}\frac{E_s}{a_s}\cos\Delta = \sin^2\Delta \qquad (2.2)$$

This equation expresses ellipse in general. The condition of elliptically polarized light is determined by the relative phase difference Δ and reflection amplitude ratio. Taking the tangent, reflection amplitude ration is expressed as reflection amplitude angle ψ. Ellipsometer measures and determines Δ and Ψ or $\cos\Delta$ and $\tan\Psi$.

Following system is assumed for the typical measurement. The system consists of ambient, thin film, and substrate.

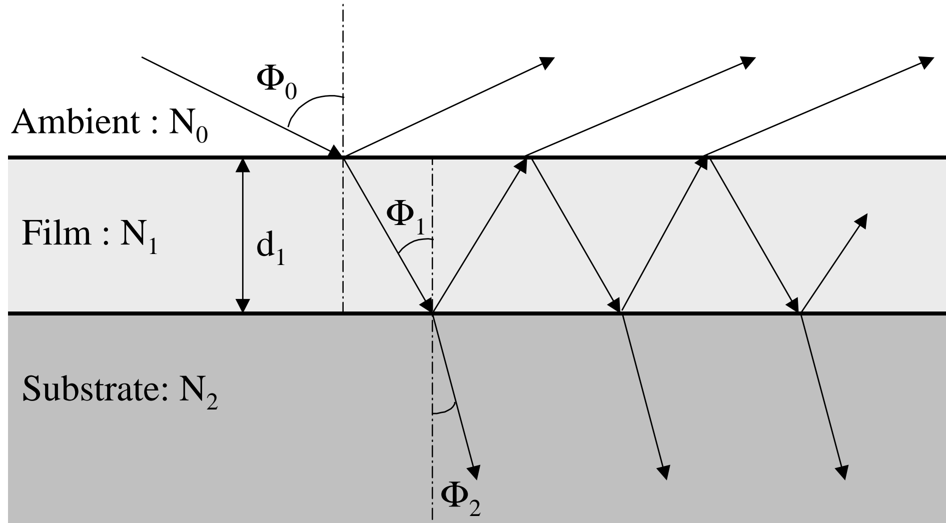


Fig. 2.17: System of three layers for typical measurement.

The relation between reflectance ratio in P, S component of polarized light and ellipso parameter is expressed as

$$\tan\Psi e^{j\Delta} = \frac{R_p}{R_s} \tag{2.3}$$

Here, Rp and Rs are complex reflection constant (Fresnel constant). Giving complex refraction $N_i = n_i - jk_i$, Fresnel constant at the each interface is given by

$$r_{i,i+1p} = \frac{N_i \cos\Phi_{i-1} - N_{i-1}\cos\Phi_i}{N_i \cos\Phi_{i-1} + N_{i-1}\cos\Phi_i}$$
$$r_{i,i+1s} = \frac{N_{i-1} \cos\Phi_{i-1} - N_i\cos\Phi_i}{N_{i-1} \cos\Phi_{i-1} + N_i\cos\Phi_i} \tag{2.4}$$

The phase angle β_i in the i layer film is

$$\beta_i = 2\pi\left(\frac{d_i}{\lambda}\right)N_i\cos\Phi_i \tag{2.5}$$

Here, d_i is film thickness, λ is wavelength of incident light and φ_i is incident angle in the i layer. Using these parameter,

$$R_p = \frac{r_{o1p} + r_{12p}e^{-j2\beta_1}}{1 + r_{o1p}r_{12p}e^{-j2\beta_1}}$$
$$R_s = \frac{r_{o1s} + r_{12s}e^{-j2\beta_1}}{1 + r_{o1s}r_{12s}e^{-j2\beta_1}} \tag{2.6}$$

Therefore, if complex refraction in each layer, incident angle and wavelength of light at measurement are known, film thickness can be calculated by measuring ellipso parameter.

2.2.5 Rutherford Backscattering Spectrometry (RBS)

Rutherford backscattering spectrometry (RBS) is based on bombarding a sample with energetic ions–typically He ions of 1 to 3 MeV energy-and measuring the energy of the backscattered ions. It allows determination of the masses of the elements in a sample, their depth distribution over distances from 100 Å to a few microns from the surface, and crystalline structure in a non-destructive manner. The method is illustrated in Fig. 2.18. Ions of mass M_1, atomic number Z_1, and energy E_0 are incident on a solid sample or target composed of atoms of mass M_2 and atomic number Z_2. Most of the incident ions come to rest within the solid losing their energy through interactions with valence electrons. The incident ions lose energy, traversing the sample until they experience a scattering event and then lose energy again as they travel back to the surface leaving the sample with reduced energy. For those incident ions scattered by surface atoms, conservation of energy and momentum leads to a relationship of their energy after scattering E_1 to the incident energy E_0 through the kinematic factor K

$$K = \frac{E_1}{E_0} = \frac{\left(\sqrt{1-(R\sin\theta)^2} + R\cos\theta\right)^2}{(1+R)^2} \approx 1 - \frac{2R}{(1+R)^2}(1-\cos\theta) \tag{2.7}$$

where $R=M_1/M_2$ and θ is the scattering angle. The kinematic factor is a measure of the primary ion energy loss. The unknown mass M_2 is calculated from the measured energy E_1 through the kinematic factor.

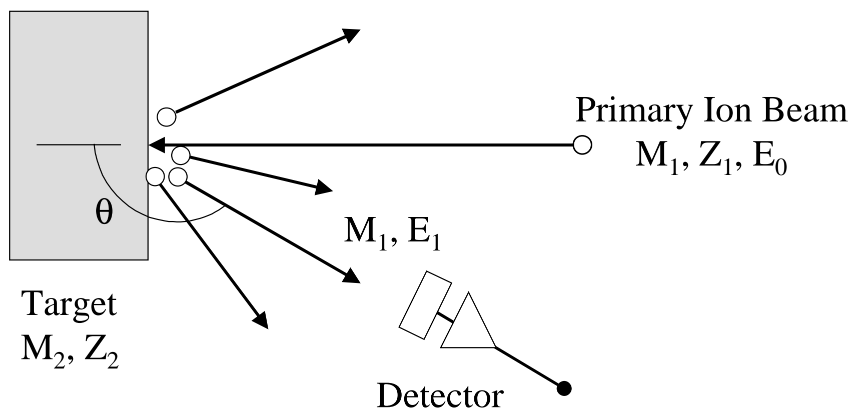


Fig. 2.18: Rutherford backscattering schematic.

2.3 Analysis Methods

This sub chapter introduces methods for MIS capacitors analysis

2.3.1 Ideal High Frequency C-V Curve

For measuring surface reliability characteristics, it is important to estimate C-V characteristics of MIS diodes. Above all, Terman method is generally used for estimating surface state. But to estimate surface state by Terman method, ideal C-V curve should be calculated. These calculate methods are reported by Sah at el. in 1960th.

Debye length was defined below formula.

$$L_D = \sqrt{\left(\frac{\varepsilon_S kT}{2q^2 n_i}\right)} \qquad C_D = \frac{\varepsilon_S}{L_D} \qquad (2.8) \quad (2.9)$$

First, change formulas to no dimension proposed by Sah.

$$\frac{q\phi(x)}{kT} \equiv U(x) \qquad \frac{q\phi_S}{kT} \equiv U_S \qquad (2.10) \quad (2.11)$$

High frequency ideal C-V curve was calculated below in case of n type Si.

$U_S \geqq 0$

$$C_S = C_D \hat{U}_S \frac{\sinh(U_S + U_F) + \sinh(-U_F)}{\left[e^{-U_F}(e^{-U_S} + U_S - 1) + e^{U_F}(e^{U_S} - U_S - 1)\right]^{\frac{1}{2}}} \qquad (2.12)$$

$0 \geqq U_S \geqq 2U_F$

$$C_S = \mathrm{sgn}\{U_S\} C_D \frac{e^{\frac{U_F}{2}} \cdot \{e^{U_S} - 1\}}{2\{e^{-U_S} - U_S - 1\}^{\frac{1}{2}}} \qquad (2.13)$$

$$F\{U_S, U_F\} \equiv \{\exp(-U_F)[\exp(-U_S) + U_S - 1] + \exp(U_F)[\exp(U_S) - U_S - 1]\}^{\frac{1}{2}}$$

(2.14)

$2U_F \geqq U_S$

$$C_S = \frac{\varepsilon_S}{W_m} = \frac{C_D}{\int_0^{U_S} (e^{U(x)} - 1) \frac{dU(x)}{f\{U(x), U_F\}}} \qquad (2.15)$$

High frequency ideal C-V curve was calculated below in case of p type Si.

$U_S \leqq 0$

$$C_S = C_D \hat{U}_S \frac{\sinh(U_S - U_F) + \sinh(U_F)}{\left[e^{U_F}(e^{-U_S} + U_S - 1) + e^{-U_F}(e^{U_S} - U_S - 1)\right]^{\frac{1}{2}}} \tag{2.16}$$

$0 \leqq U_S \leqq 2U_F$

$$C_S = \mathrm{sgn}\{U_S\} C_D \frac{e^{\frac{U_F}{2}} \cdot \{1 - e^{U_S}\}}{2\{e^{-U_S} + U_S - 1\}^{\frac{1}{2}}} \tag{2.17}$$

$$F\{U_S, U_F\} \equiv \{\exp(U_F)[\exp(-U_S) + U_S - 1] + \exp(-U_F)[\exp(U_S) - U_S - 1]\}^{\frac{1}{2}}$$

$2U_F \leqq U_S$ (2.18)

$$C_S = \frac{\varepsilon_S}{W_m} = \frac{C_D}{\int_0^{U_S} (1 - e^{-U(x)}) \frac{dU(x)}{f\{U(x), U_F\}}} \tag{2.19}$$

2.3.2 Terman Method

When measurement in high frequency, interfacial state was regarded fixed charge. In this case, interfacial state density was calculated by shift value from ideal C-V curve to experimental C-V curve. In order to calculate interfacial state, fitting between ideal and experimental curve was needed. After fitting, capacitance change value of experimental and ideal curve against surface potential were calculated. And this results works out interfacial state density.

To calculate interfacial state density, these symbols were defined. Q_{SS} : interfacial charge density, N_{SS} : interfacial state density, C_I : capacitance of insulator, C_1,C_2 : different random capacitance, ΔV_{exp} : experimental gate voltage between C_1-C_2, ΔV_{th} : ideal gate voltage between C_1-C_2, ϕ_1 : surface potential against C_1, ϕ_2 : surface potential against C_2, $\Delta\phi$: ϕ_1-ϕ_2 A : size of electrode

From shift between ideal and experimental curve, interfacial charge density by unit size was calculated.

$$Q_{SS} = \frac{C_I(\Delta V^{\exp} - \Delta V^{th})}{A} \qquad (2.20)$$

Capacitance value of ideal curve correspond surface potential. And interfacial charge density Q_{SS} differentiates by surface potential ϕ. Then, interfacial state density by unit size was calculated.

$$N_{SS} = \frac{1}{q} \cdot \frac{\partial Q_{SS}}{\partial \phi_S} = \frac{C_I}{qA}\left[\frac{\partial V_{\exp}}{\partial \phi_S} - \frac{\partial V_{th}}{\partial \phi_S}\right] \qquad (2.21)$$

$$N_{SS} = \frac{C_I}{qA\Delta\phi}\left(\Delta V^{\exp} - \Delta V^{th}\right) \qquad (2.21)$$

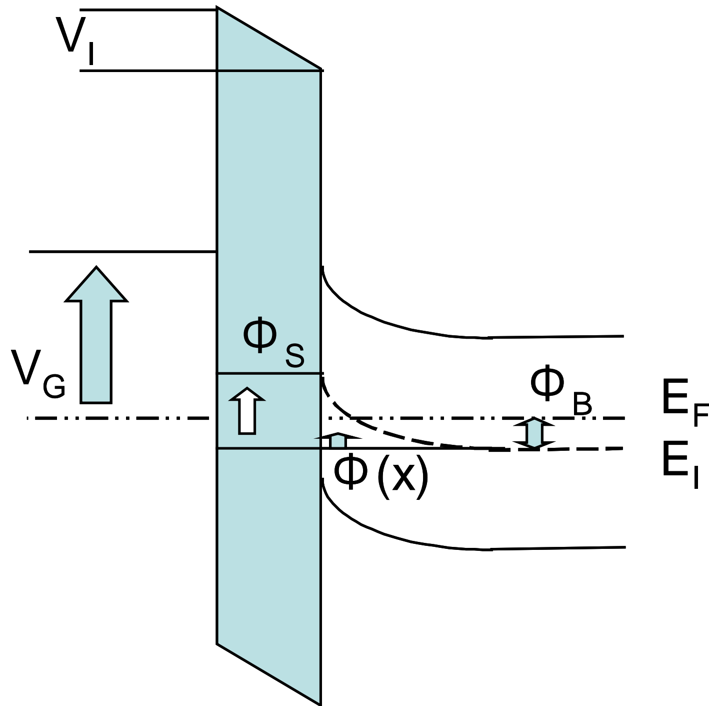


Fig. 2.19: band diagram of MIS capacitor on n-Si

2.3.3 Leakage Mechanism

Fig.2.20 shows the electrons and holes conduction mechanism in high-k materials. It indicates that two transport mechanisms. Poole-Frenkel model is trap-assist conduction. The traps are created in film and electron hops on them. Fowler-Nordheim model is direct tunneling leakage. Peculiar type plots are used for judgment both models. P-F plot was shown by formula 2.22. It depends on thermal value. If these plots indicate on a straight line, leakage current was controlled that models. And the depth of trap is calculated from the slope of straight line.

$$J \sim \varepsilon \exp\left[\frac{-q(\phi_B - \sqrt{q\varepsilon / \pi\varepsilon_i})}{kT}\right] \sim V \exp(+2a\sqrt{V}/T - q\phi_B / kT) \quad (2.22)$$

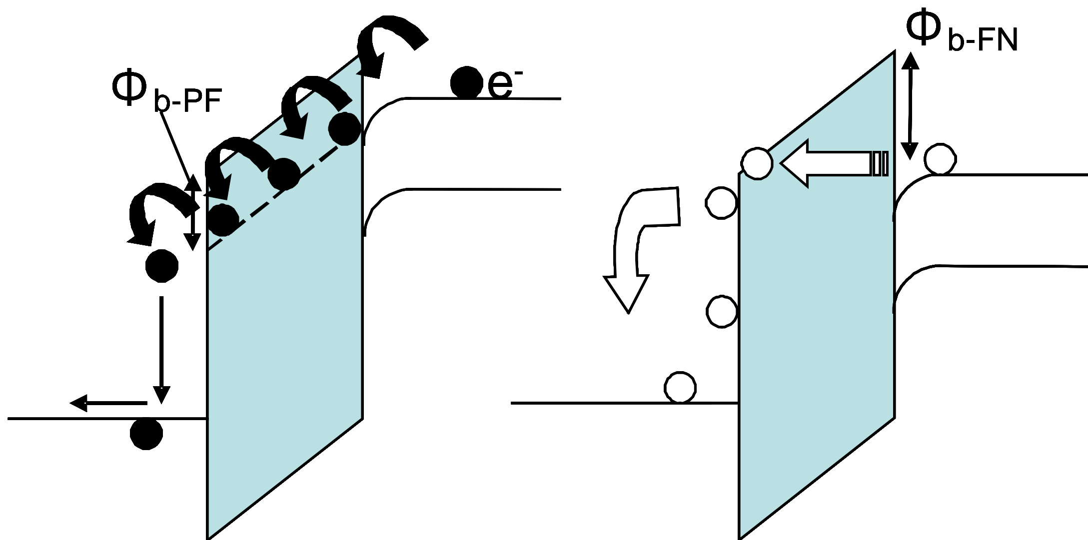


Fig.2. 20: Leakage mechanism in high-k material

Chapter 3

Experimental Results

3.1Problem of the Conventional RTA Method

In this section, the effect of the conventional annealing method which is 5min RTA in O_2 or N_2 are reported.

The process flow is showed in Fig. 3.1. First, n-Si (100) substrate was chemically cleaned. Dy_2O_3 thin films were deposited on Si (100), then, annealed *ex-situ* by RTA for 5 min in O_2 and N_2 ambience at normal pressure. The background pressure in the vacuum chamber of MBE was 10^{-10} ~ 10^{-9} Torr. The pressure during deposition was 10^{-9} ~ 10^{-7} Torr. Deposition rate was 0.2 ~0.5 nm/min. The electrical characteristics of the fin films were evaluated by Al/Dy_2O_3/n-Si(100)/Al MIS structures, and the surface morphologies were observed by AFM.

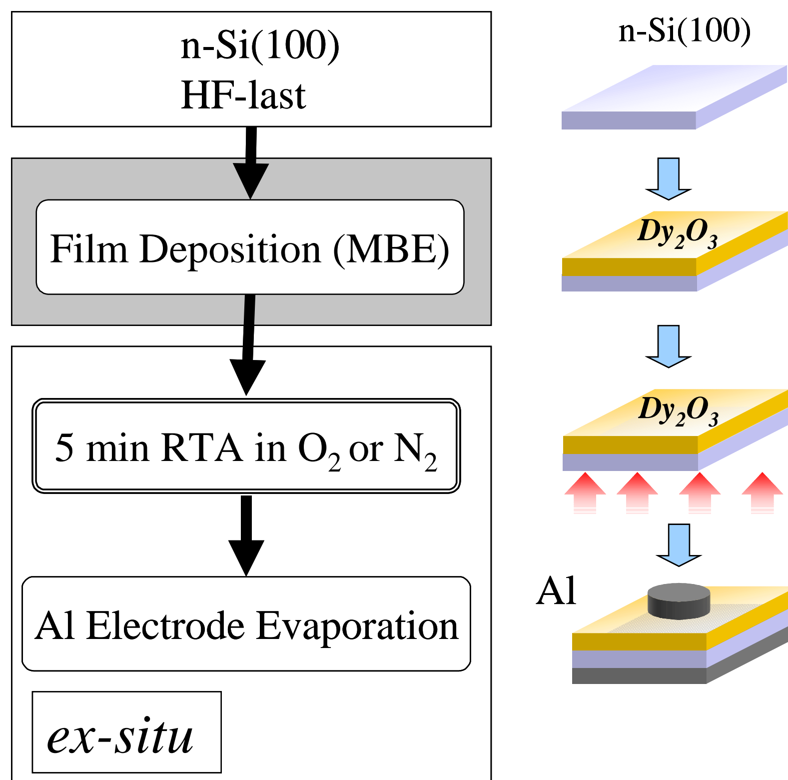


Fig. 3.1: Process flow of the conventional annealing method.

3.1.1 Characteristics in the Case of O_2 RTA

Fig. 3.2 shows the set of C-V characteristics of Dy_2O_3 thin films. The films were deposited at room temperature (R.T.) and 250°C, then annealed in O_2 at 200°C ~ 1000°C respectively. The hysteresis resulting from the injected charges was observed in the C-V characteristics for as-deposited films formed at the both temperatures, R.T. and 250°C. Comparing the R.T. deposition, the as-deposited film at 250°C showed wider width of hysteresis. This suggests that the film deposited at 250°C had more defects or charge traps in itself than the sample of R.T. deposition. Both hysteresis disappeared by RTA. However, accumulation capacitance decreased as annealing temperature increased. For example, in the case of R.T. deposition, although EOT of as-deposited film was 1.3 nm, that of O_2 400°C RTA became 1.8 nm. The leakage currents were also suppressed with the RTA temperature increase (Fig. 3.3). These tendencies were observed in the both deposition temperatures, R.T. and 250°C. These results indicate that the low dielectric interfacial layer was formed by the *ex-situ* O_2 RTA. Fig.3.4 shows the 3-D AFM images of the surfaces morphologies for the films before and after RTA. The scan size was 500 nm x 500 nm and the one scale of the height was 5 nm. It was found that the surface roughness did not change during the annealing process so much. The root mean square (RMS) value of the surface roughness became large slightly as the annealing temperature increased.

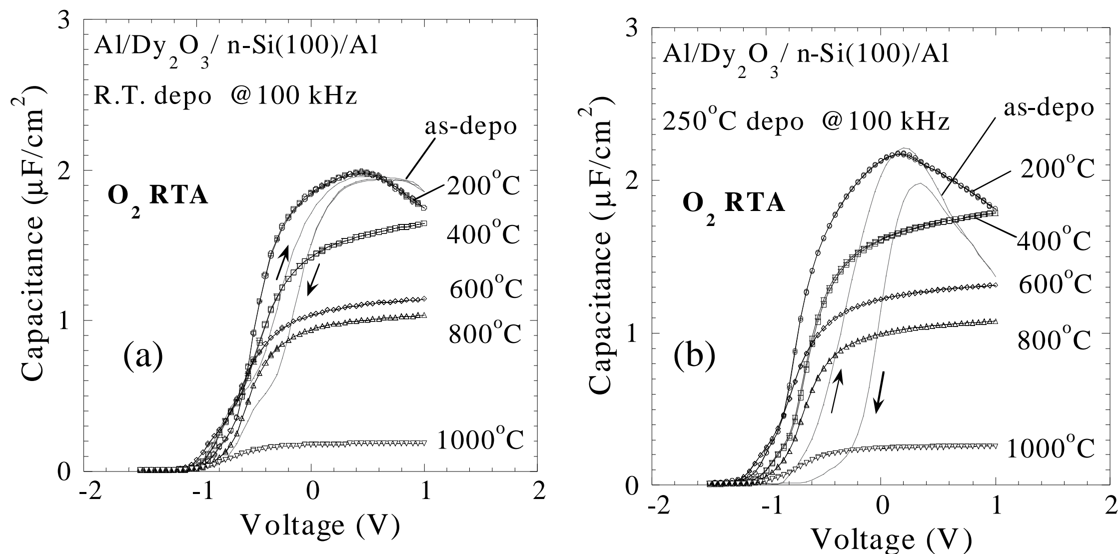


Fig. 3.2: C-V characteristics for the Dy_2O_3 films fabricated by RTA in O_2 for 5min. (a) R.T. deposition, (b) 250°C deposition

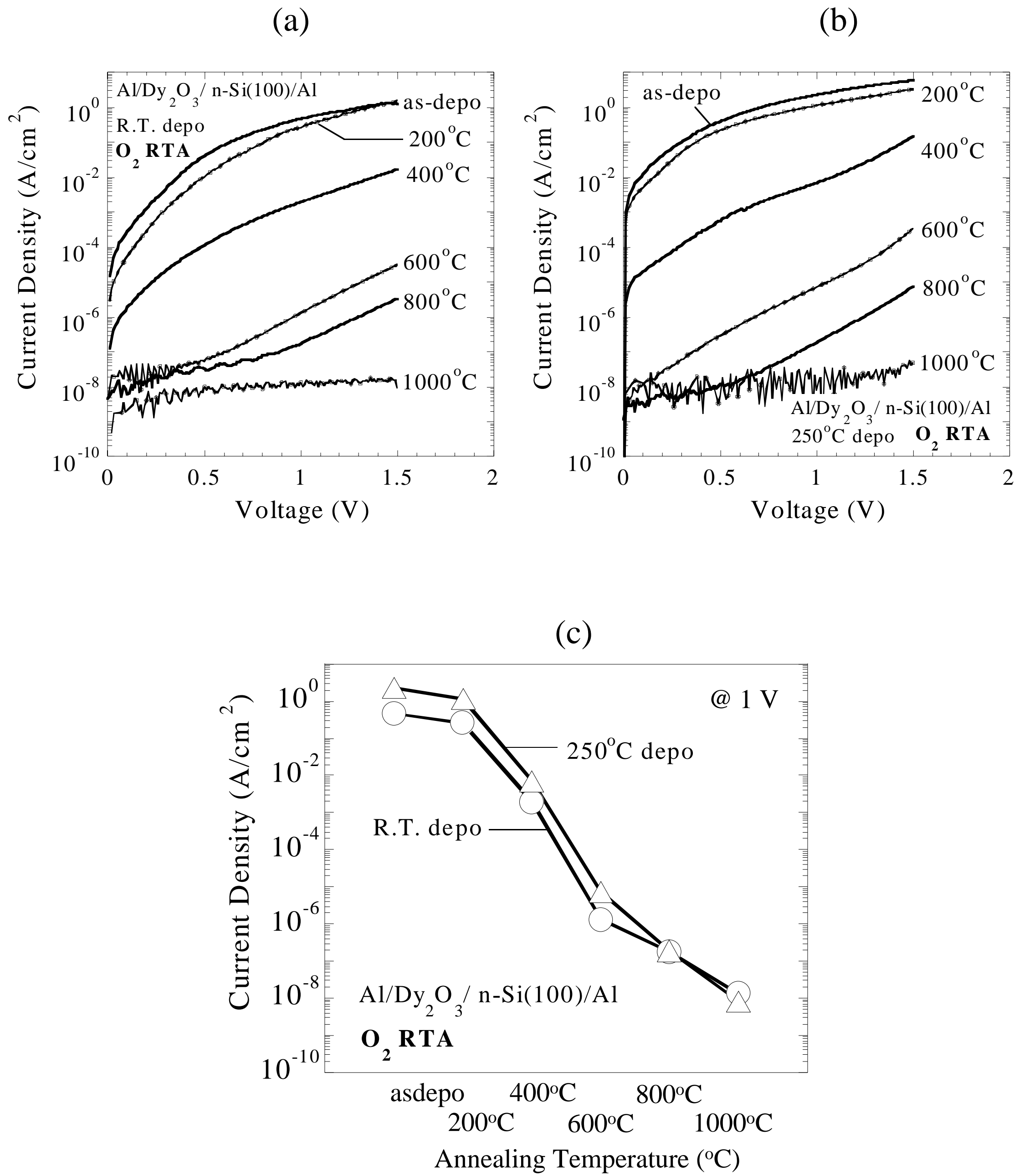
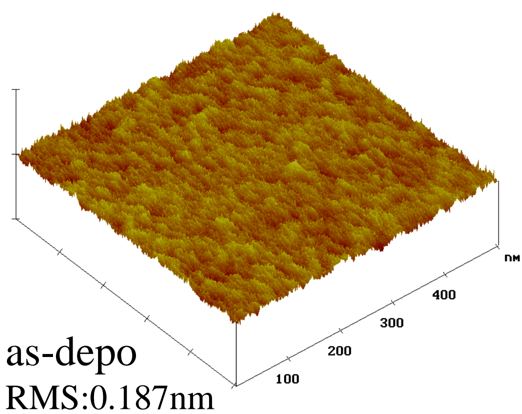
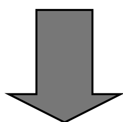


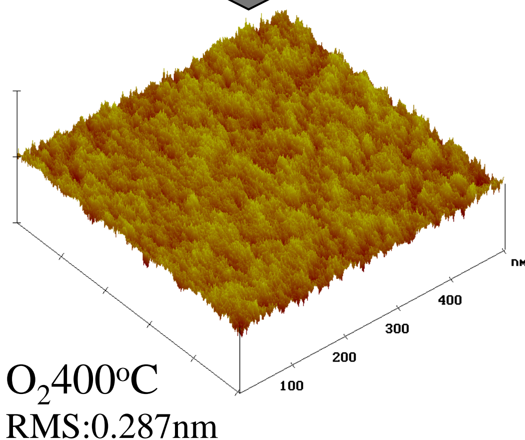
Fig. 3.3: J-V characteristics for the Dy_2O_3 films fabricated by RTA in O_2 for 5min.
(a) R.T. deposition, (b) 250°C deposition,
(c) Leakage currents depending on the annealing temperature.

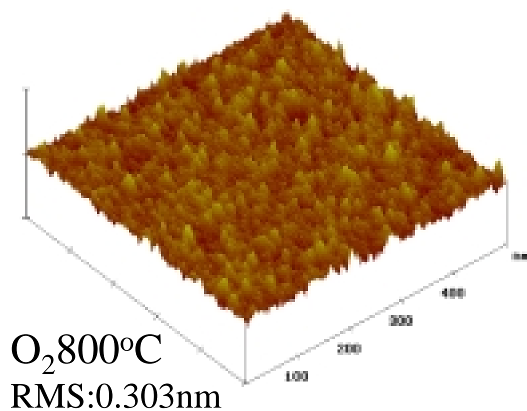
R.T. deposition

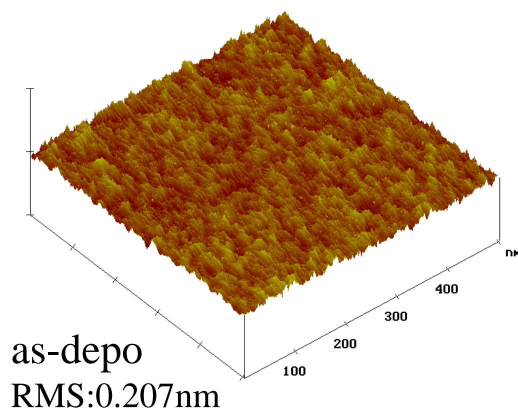
250°C deposition

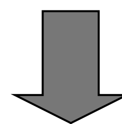


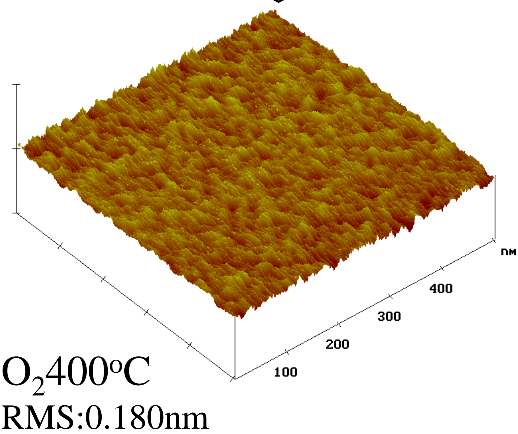












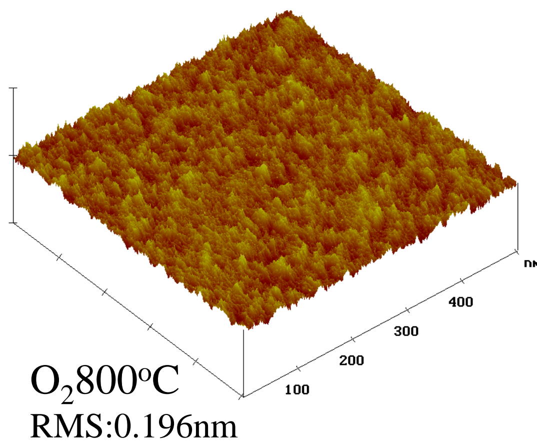


Fig.3.4: AFM images of the surface morphologies for Dy_2O_3 thin films annealed by RTA in O_2 for 5min. (500 x 500 nm, Z: 5 nm/div)

3.1.2 Characteristics in the Case of N_2 RTA

Dy_2O_3 films were deposited at R.T. and 250°C, then annealed in N_2 at 200°C ~ 1000°C respectively. The accumulation capacitances in the C-V characteristics decreased with annealing temperature increase as well as the case of O_2 RTA (Fig. 3.5). However, capacitance values at above 0 V rolled down by the high temperature annealing such as 800°C and 1000°C. Similarly, leakage currents of 800°C and 1000°C annealed samples showed the different results to the O_2 RTA (Fig. 3.6). It was found that these results were closely related to the surface roughness of the thin films after RTA. The AFM images of surface morphologies for thin films annealed in N_2 were showed in Fig. 3.7 and Fig. 3.8. Below 600°C, surface roughness did not change by N_2 RTA (Fig. 3.7). However, for the high temperature RTA above 800°C, surface morphologies changed dramatically (Fig. 3.8). Many grains like microcrystal were observed in the image of the film annealed at 800°C, and RMS value of surface roughness increased. In the case of 1000°C, more intense surface roughness was observed. Therefore, it is considered that current paths were formed caused by the electric field concentration depending on the surface morphology of the fin film. These results indicate that Dy_2O_3 thin film is not stable at high temperature above 800°C, so it can be said that the suitable temperature of annealing is less than 800°C for Dy_2O_3 film.

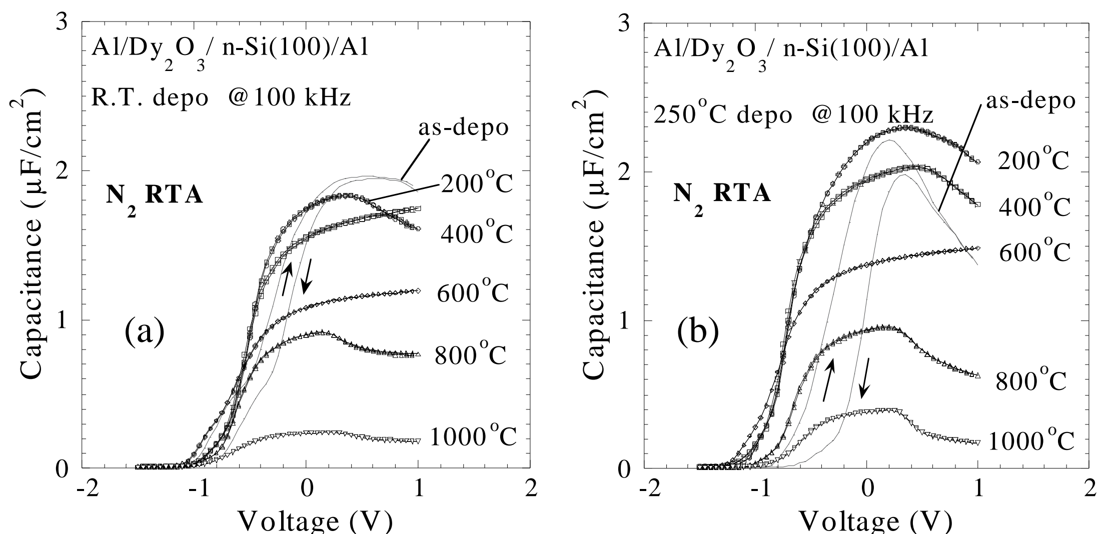


Fig. 3.5: C-V characteristics for the Dy_2O_3 films fabricated by RTA in N_2 for 5min. (a) R.T. deposition, (b) 250°C deposition

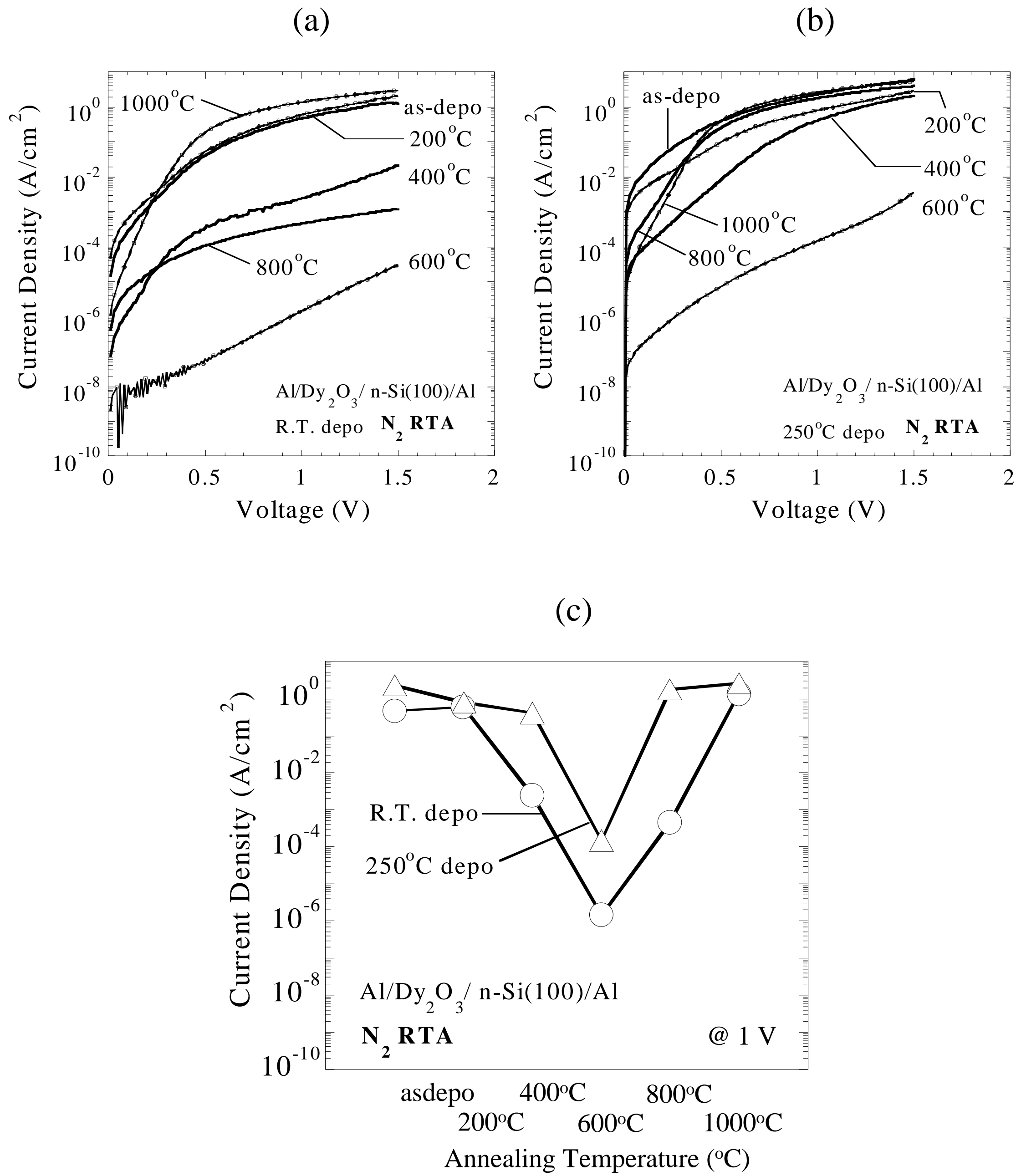
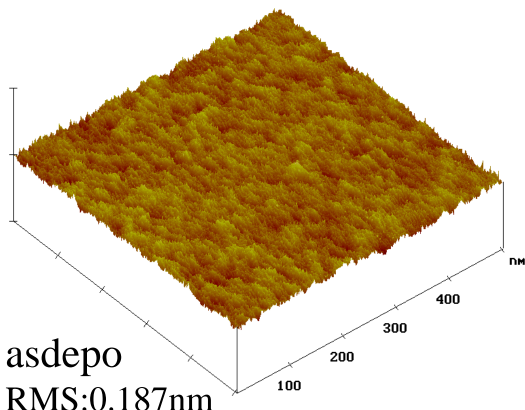


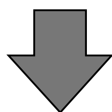
Fig. 3.6: J-V characteristics for the Dy_2O_3 films fabricated by RTA in N_2 for 5min. (a) R.T. deposition, (b) 250°C deposition, (c) Leakage currents depending on the annealing temperature.

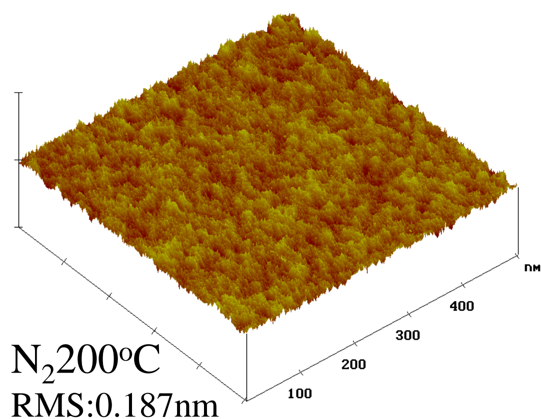
R.T. deposition

250°C deposition

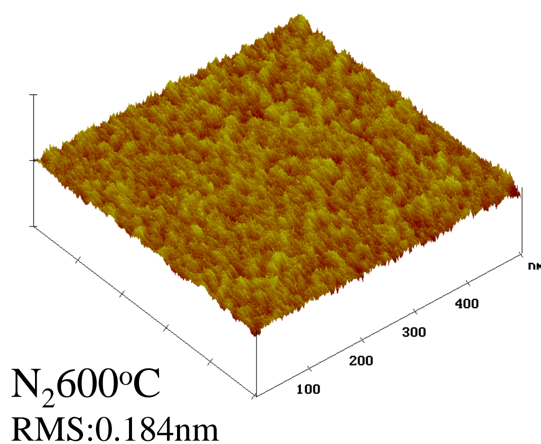


asdepo
RMS:0.187nm

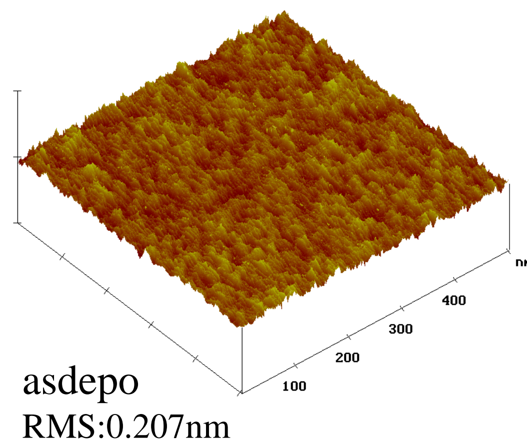




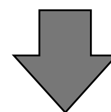
$N_2$200°C
RMS:0.187nm

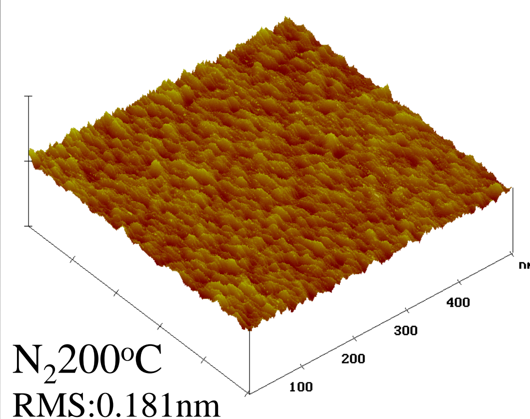


$N_2$600°C
RMS:0.184nm

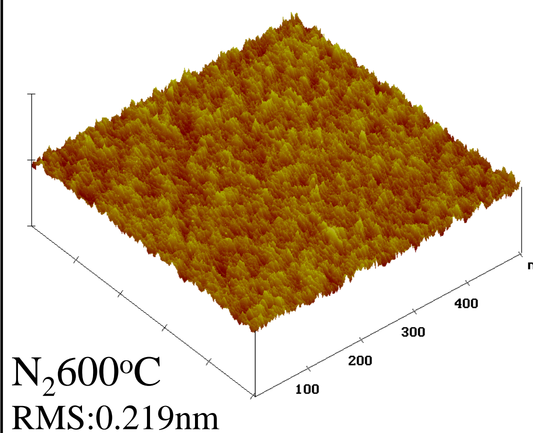


asdepo
RMS:0.207nm





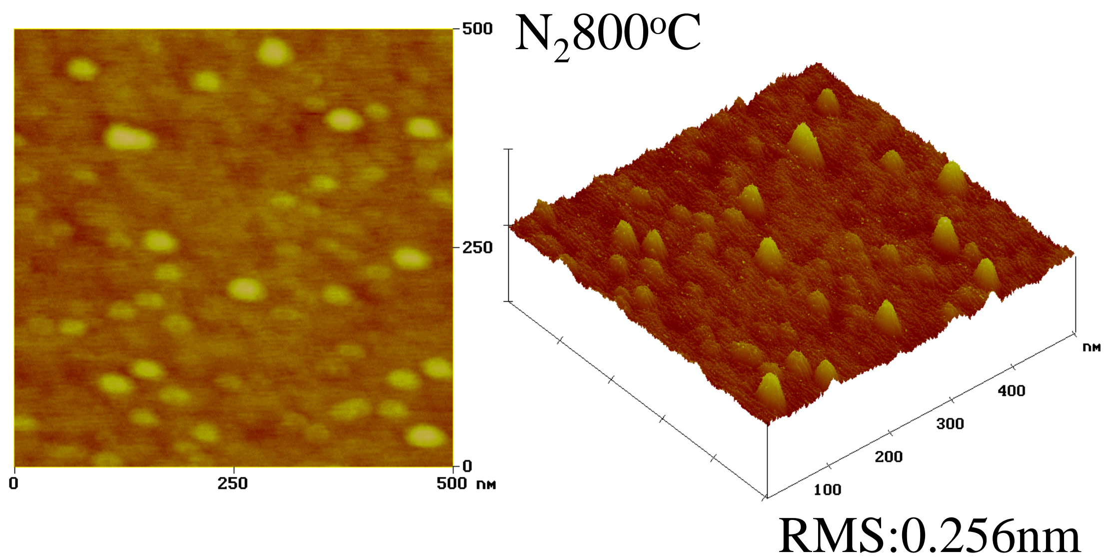
$N_2$200°C
RMS:0.181nm



$N_2$600°C
RMS:0.219nm

Fig.3.7: AFM images of the surface morphologies for Dy_2O_3 thin films annealed by RTA in N_2 for 5min. (500 x 500 nm, Z: 5 nm/div)

250°C deposition



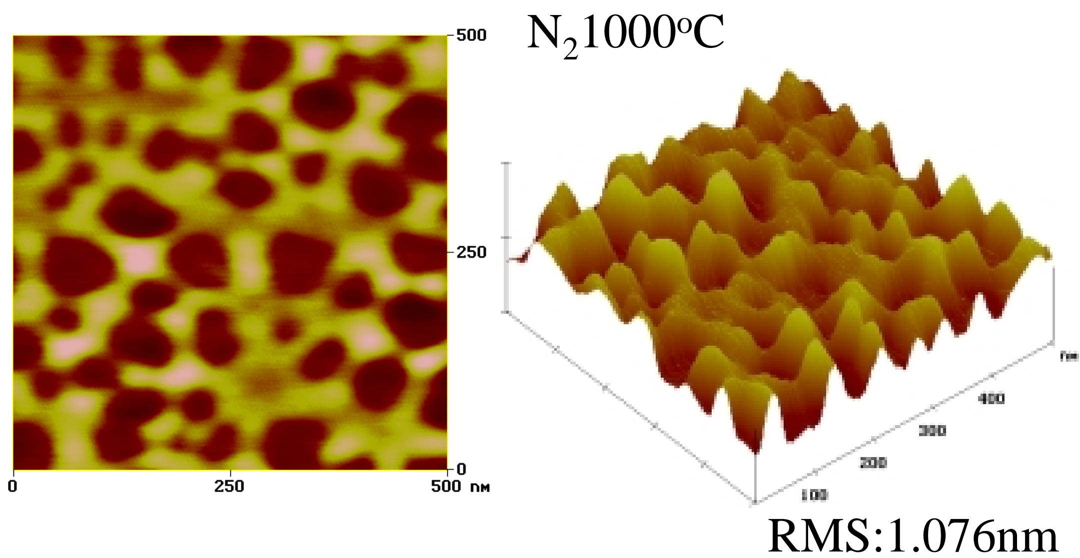


Fig.3.8: 2D and 3D AFM images of the surface morphologies for the Dy_2O_3 thin films annealed at high temperature, 800°C and 1000°C after 250°C deposition. (500 x 500 nm, Z: 5 nm/div)

3.1.3 Summary of the Characteristics for Dy_2O_3 Thin Films Formed by RTA

As the summary of the characteristics for Dy_2O_3 films formed by RTA, the relation between EOT and leakage current was showed in Fig. 3.9. From this EOT-J plot, following results were obtained. First, in the case of R.T. deposition, EOT-J characteristics were almost not affected by the difference of the annealing ambience, which were shown as surrounded by the open circles in the graph. Contrarily, in the case of 250°C deposition, the characteristics were different by the annealing ambience. N_2 RTA samples had smaller EOT and higher leakage density than O_2 RTA. Considering this results and the difference in hysteresis width of the C-V curve for the as-deposited film at R.T. and 250°C (mentioned in section 3.1.1), it is suspected that the film quality of R.T. deposition was tighter than that of 250°C deposition case. Furthermore, universal relation was observed between EOT and leakage current except for N_2 800°C RTA. This relation was independent to the individual process conditions such as deposition temperature, annealing temperature, and annealing ambience. In other words, even if how those formation conditions were arranged, improvement on the electrical characteristics cannot be expected as long as using the method of RTA at normal pressure. Therefore, in order to acquire smaller EOT with low leakage, a quite different annealing method to the conventional RTA should be investigated.

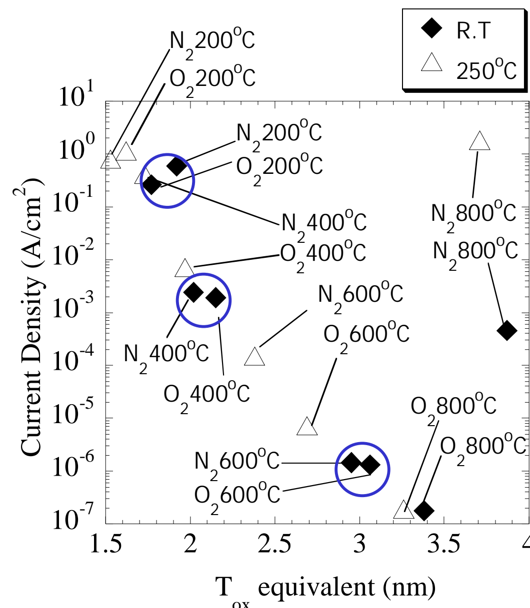


Fig. 3.9: EOT-J plot for Dy_2O_3 films fabricated by RTA in O_2 and N_2 ambience.

3.2 Effect of Ultra-High Vacuum Anneal

3.2.1 Electrical Characteristics for Dy_2O_3 Thin Films Formed by *In-situ* Vacuum Anneal

The process flow is showed in Fig. 3.10. Dy_2O_3 thin films were deposited on Si (100) at R.T., then, annealed *in-situ* in the ultra-high vacuum for 90 min by the heater equipped in MBE system. The time transition of the annealing temperature is shown in Fig. 3.11. The pressure in the chamber during annealing was 10^{-10} - 10^{-8} Torr.

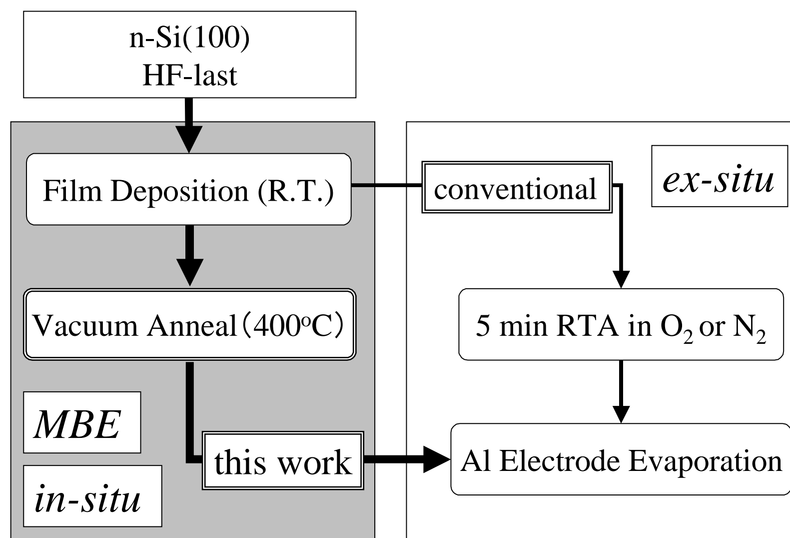


Fig. 3.10: The process flow of *in-situ* vacuum anneal.

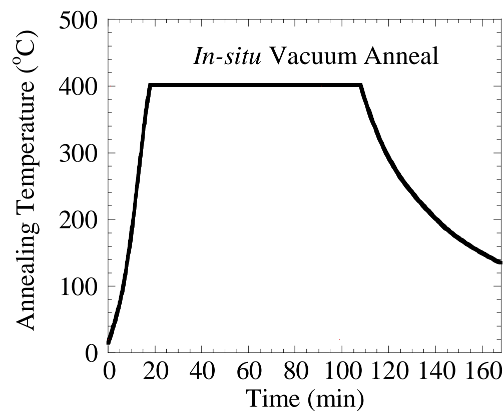


Fig. 3.11: Time transition of the annealing temperature.

Fig. 3.11 shows electrical characteristics for Dy_2O_3 thin films before and after *in-situ* vacuum anneal (IVA) at 400°C for 90 min. It should be noted that hysteresis in the C-V curve of the as-deposited sample disappeared by the *in-situ* vacuum anneal without decreasing the accumulation capacitance, which suggested that the interfacial layer was not formed or very thin (Fig. 3.11 (a)). As the result, small EOT of 1.1 nm was obtained. These results were quite different from the conventional annealing case, 5 min RTA in O_2, in which significant decrease of the accumulation capacitance is observed (section 3.1.1). The leakage current did not decrease by the annealing (Fig. 3.11 (b)), however, notice that the C-V curve for the vacuum annealed sample shifted to the negative side (flat band voltage shift ΔV_{FB} is –0.96 V). Therefore, by comparing the leakage current at the effectively same electric field that applied on the thin film, the leakage current for the sample after *in-situ* vacuum anneal was lower than the as-deposited film as shown in Fig. 3.12. Fig. 3.13 shows AFM images of surface morphologies for the films before and after *in-situ* vacuum anneal. The surface roughness did not change during this annealing process as well as the conventional case.

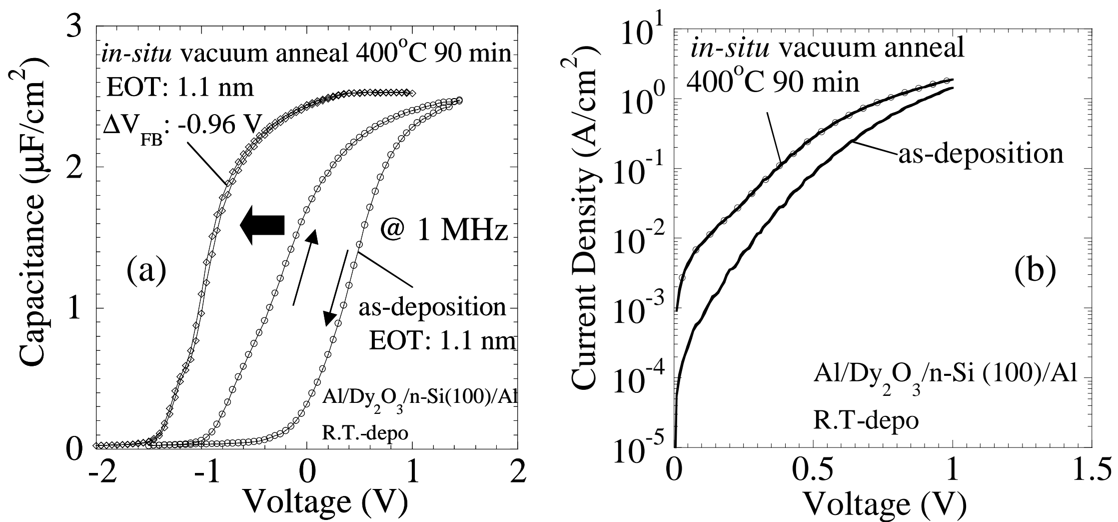


Fig. 3.11: (a) C-V and (b) J-V characteristics for the Dy_2O_3 films fabricated by *in-situ* vacuum anneal 400°C 90 min.

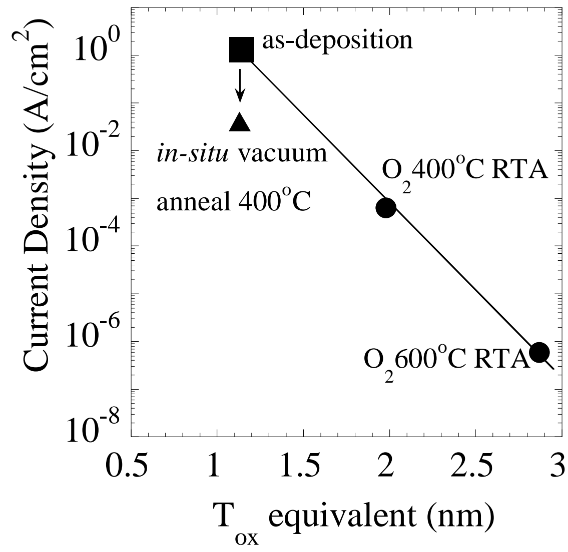


Fig. 3.12: EOT-J plot of *ex-situ* RTA in O_2 and *in-situ* vacuum anneal

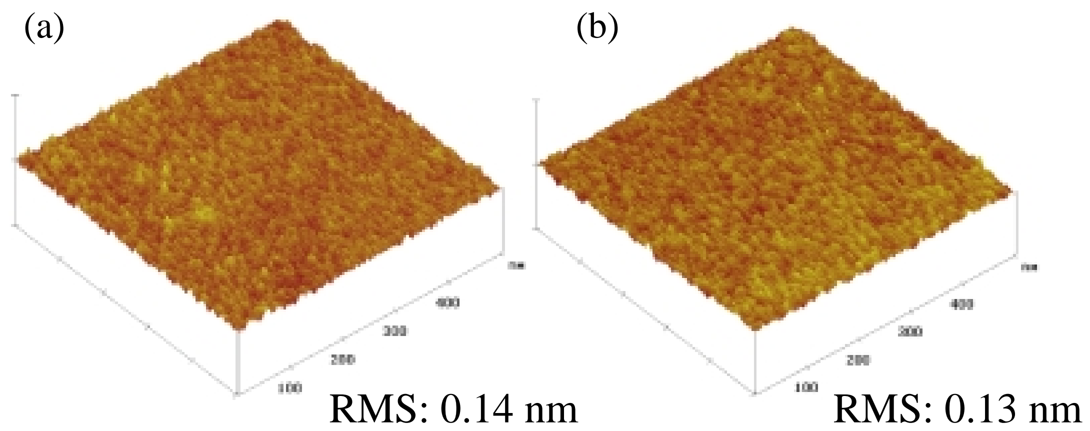


Fig. 3.13: AFM images of the surface morphologies for Dy_2O_3 films.
(500 x 500 nm, 5 nm/div)
(a) as-deposed, (b) after *in-situ* vacuum anneal.

As the summary of the electrical characteristics improvements by the *in-situ* vacuum anneal, EOT-J (leakage current) plots for the conventional and *in-situ* vacuum annealed samples were showed in Fig. 3.14. In this graph, the leakage currents for all samples were compared at +1.5 V from the V_{FB}. As shown in this plot, the leakage currents of the *in-situ* vacuum annealed samples were significantly smaller than those of the conventional O_2 RTA at the same EOT. From these results, following points are showed as the summary of the effects of *in-situ* vacuum anneal.

1. The accumulation capacitance did not decrease by *in-situ* vacuum anneal.
2. Compared with the conventional RTA, electrical characteristics were improved.
3. V_{FB} shifted to the negative side.

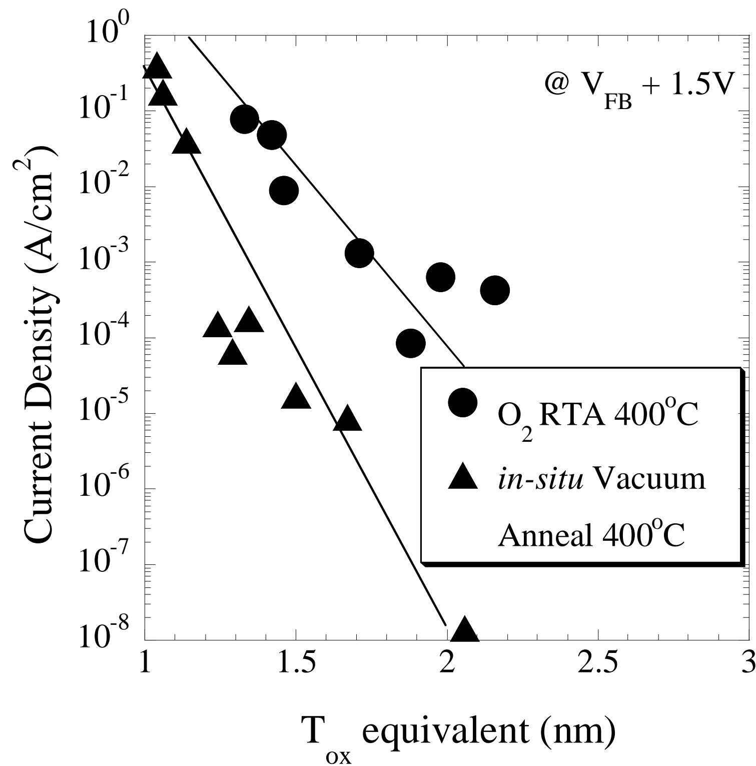


Fig. 3.14: EOT-J plot for the Dy_2O_3 films formed by the conventional O_2RTA and *in-situ* vacuum anneal.

3.2.2 Mechanism of *In-situ* Vacuum Anneal

The dielectric constant ε of the films were estimated from the relation between EOT and physical thickness (T_{pyhs}). The physical thickness was measured by ellipsometer. EOT-T_{phys} plot was showed in Fig. 3.16. At the same EOT, T_{phys} of the film formed by IVA was smaller than that of O_2 RTA. Here, in this assumed model, the interfacial layer thickness is same for any film fabricated by the same annealing method. The relation between EOT and T_{phys} are expressed as following.

$$\frac{1}{C_{ox}} = \frac{1}{C_{Dy_2O_3}} + \frac{1}{C_{I.L}}$$

$$\Rightarrow \frac{EOT}{\varepsilon_{SiO_2}} = \frac{(T_{phys} - T_{I.L})}{\varepsilon_{Dy_2O_3}} + \frac{T_{I.L}}{\varepsilon_{I.L}}$$

$$\Rightarrow EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{Dy_2O_3}} T_{phys} + \left(\frac{1}{\varepsilon_{I.L}} - \frac{1}{\varepsilon_{Dy_2O_3}} \right) \cdot \varepsilon_{SiO_2} \cdot T_{I.L} \quad (3.1)$$

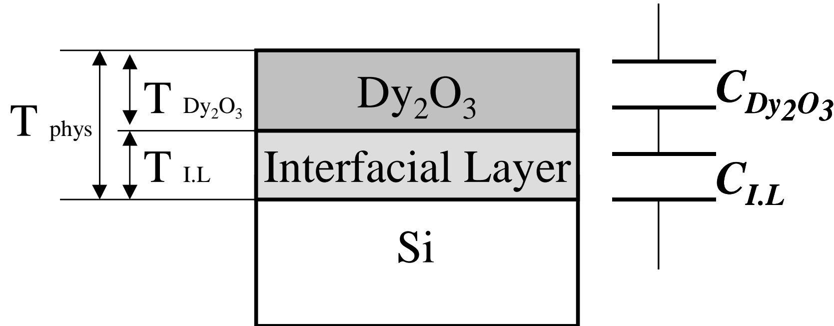


Fig. 3.15: Physical model of the Dy_2O_3 thin film after anneal.

Using the slope of the line, ε for the film after IVA and O_2 RTA were estimated as 18 and 16 respectively. It was also found that the intercept value of IVA line was smaller than O_2 RTA. The intercept of line represents the second term in the right side of equation 3.1. This is considered that the interfacial layer for the film of IVA was thinner or the ε was higher than those of O_2 RTA sample.

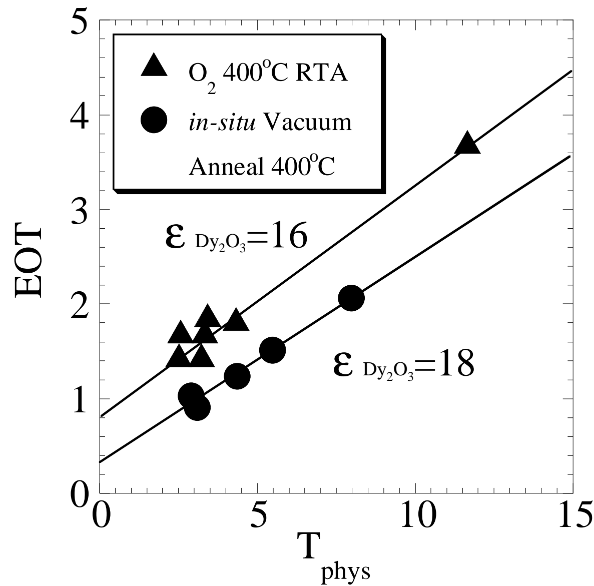


Fig. 3.16: Plots of EOT and physical thickness measured by ellipsometer for the Dy_2O_3 films after O_2 RTA and *in-situ* vacuum anneal

In order to verify the prospect mentioned above, chemical bonding conditions of the thin films were investigated by XPS measurement. Fig. 3.17 is XPS measurement of Si_{2p} spectrum for Dy_2O_3 films of as-deposition, O_2 400°C RTA and IVA 400°C. The graphs showed the measurement results for the different two kind of take-off angle for photoelectron. First, in the case of 45° measurement (Fig. 3.17(a)), chemical shifted Si peak was observed at about 102.5 eV of the binding energy for O_2 RTA sample,. This binding energy was smaller than that of SiO_2 bonding, therefore it is considered that the interfacial layer consisting of silicate was formed by RTA. In the case of IVA, silicate peak was also observed at about 101.7 eV. However, the binding energy and peak intensity was smaller than those of O_2 RTA film. It means that the interfacial layer of IVA was thinner and its dielectric constant was higher than O_2 RTA sample. This result can be the proof that supports the prospect mentioned above.

On the other hand, for the as-deposited film, the similar peak appeared at the same energy with IVA in the measurement for the small take-off angle of photoelectron (Fig. 3.17 (b)). This result suggests that the very thin interfacial layer exits in the as-deposited film even if it was formed at R.T. Furthermore, it is suspected that the interfacial layer structure in the film of IVA was identical to the as-deposited one. So this can be considered as the reason why the accumulation capacitance did not decrease after vacuum anneal.

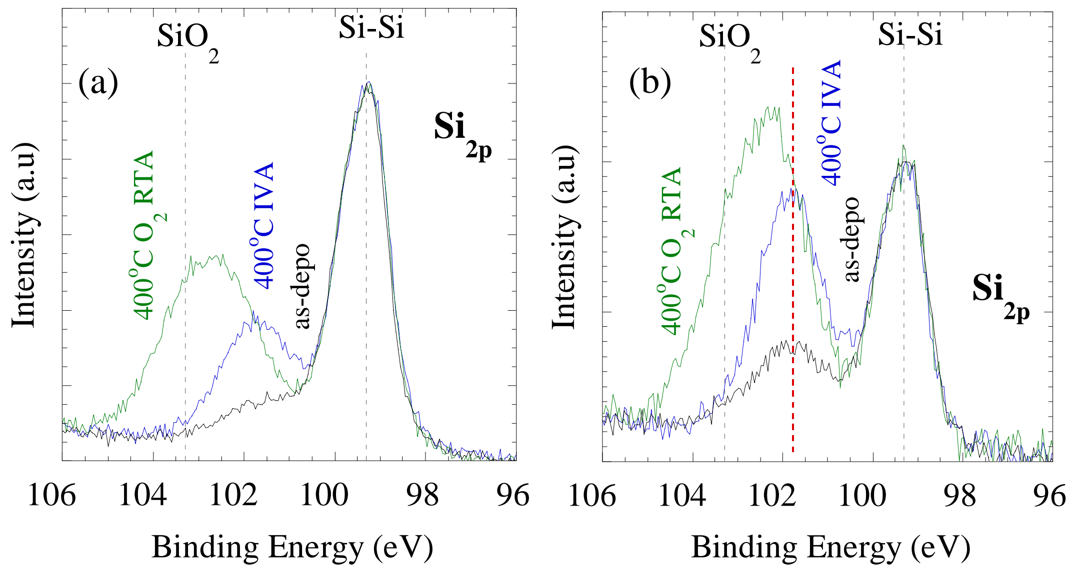


Fig. 3.17: XPS measurement of Si_{2p} spectrum for Dy_2O_3 films of as-deposition, O_2 400°C RTA and IVA 400°C.
Take-off angle of photoelectron was (a) 45°, (b) 20°.

3.2.3 Measurement Temperature Dependence of Leakage Current

Measurement temperature dependence of leakage current was examined for Dy_2O_3 films before and after *in-situ* vacuum anneal or O_2 RTA. Fig 3.18 shows leakage currents measured at 25°C ~ 150°C for the film with the thickness of 2.5 nm (measured by ellipsometer). Both films of as-deposition and after RTA showed temperature dependence of leakage current. The leakage current became larger as the measurement temperature increased. This result indicates that the Pool-Frenkel (P-F) leakage was dominant for these films. Next, *in-situ* vacuum annealed sample (film thickness was 2.9 nm) was also measured. In this case, measurement temperature dependence was not observed so much as shown in Fig. 3.19 (a). However, when the thickness became larger, temperature dependence was found in the leakage characteristics (Fig. 3.19 (b)).

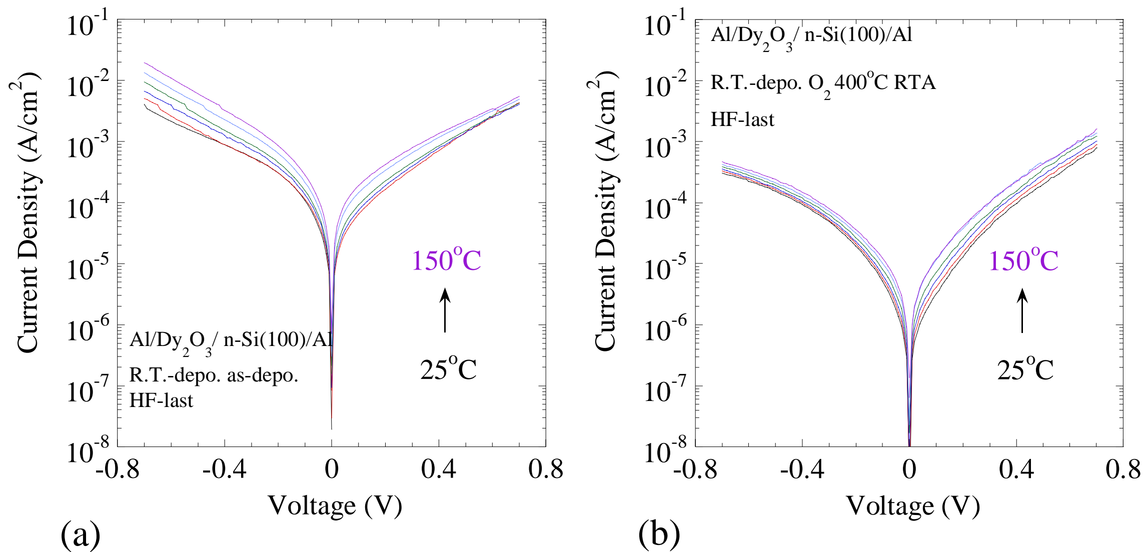


Fig. 3.18: Measurement temperature dependence of the leakage currents for the film of (a) as-deposition and (b) O_2 RTA. The film thickness was 2.5 nm.

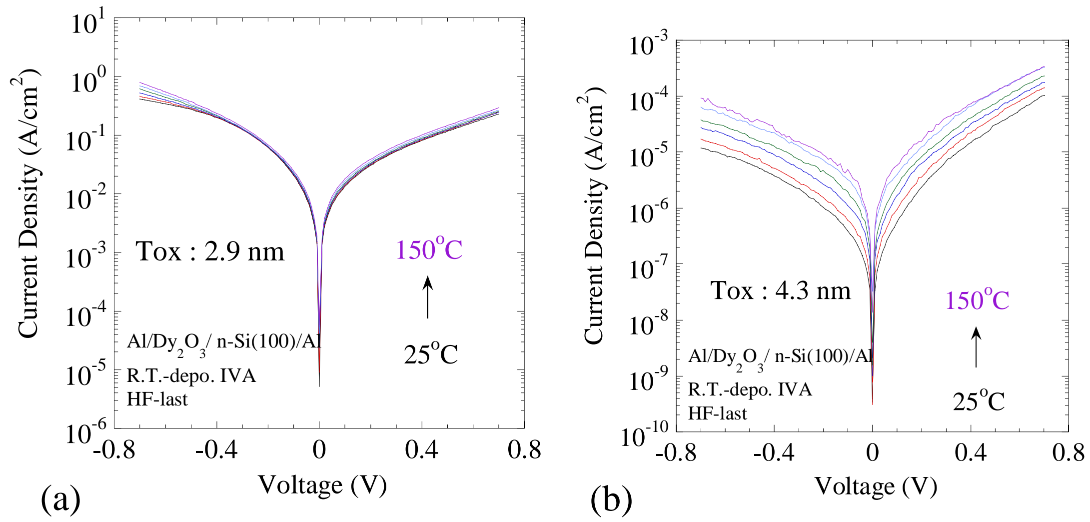


Fig. 3.19: Measurement temperature dependence of the leakage currents for the film after *in-situ* vacuum anneal. The film thickness was (a) 2.9 nm and (b) 4.3 nm.

3.3 Optimum Formation Condition for suppression of V_{FB} Shift with Ultra-High Vacuum Anneal

From the previous subsection, it was found that the problem of the capacitance degradation after annealing process can be resolved by *in-situ* vacuum anneal method. However, negative flat band voltage shift after *in-situ* vacuum anneal should be improved. In this section, the optimum formation condition for the thin film was investigated for the purpose of controlling the V_{FB}.

3.3.1 Annealing Temperature Dependence of Vacuum Anneal

To investigate the annealing temperature dependence, Dy_2O_3 films were annealed *in-situ* at 200°C and 600°C. In the case of 200°C annealing, the accumulation capacitance and V_{FB} shift did not show significant difference from those of the 400°C annealing (Fig. 3.21). The leakage current was slightly smaller than that of 400°C annealed film. On the other hand, C-V characteristics for the sample annealed at 600°C changed. Fig. 3.20 shows the C-V characteristics and RBS measurement result for the film as-deposited and after 600°C *in-situ* vacuum anneal. It is found that the film thickness after 600°C *in-situ* vacuum anneal was about 50% to the as-deposited film from the RBS results. It is considered that the film became thinner presumably because of the reevaporation of the deposited Dy_2O_3 film at high temperature such as 600°C. Considering these results, 400°C is thought to be the optimum temperature condition for vacuum anneal.

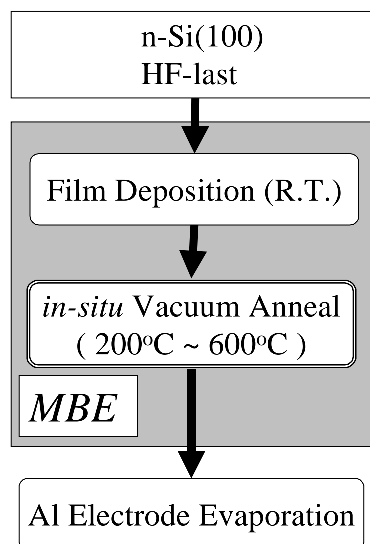
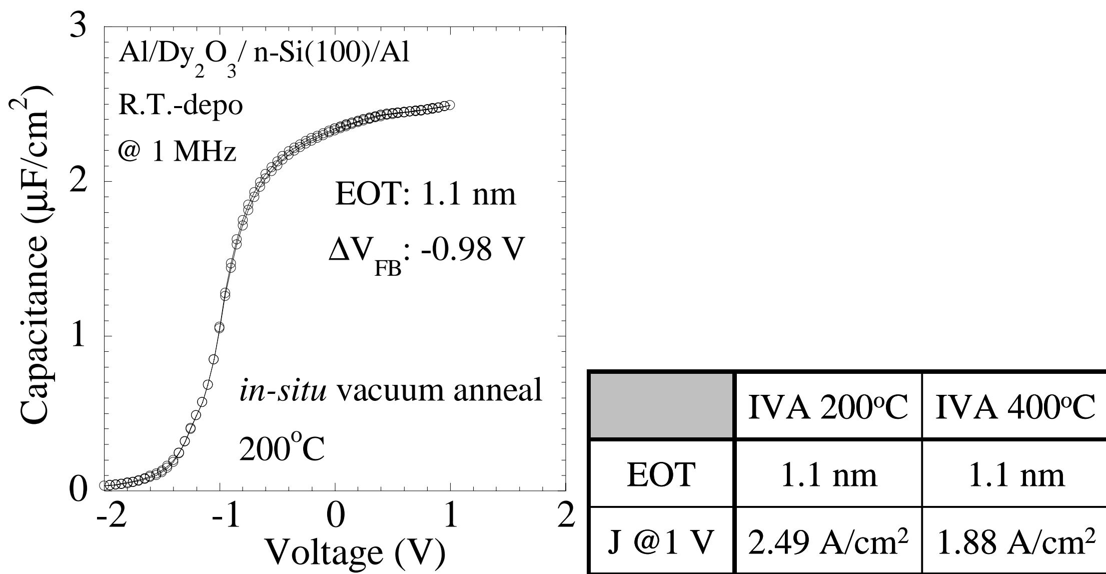


Fig. 3.20: Process flow.



	IVA 200°C	IVA 400°C
EOT	1.1 nm	1.1 nm
J @1 V	2.49 A/cm²	1.88 A/cm²

Fig. 3.21: C-V characteristics for the Dy_2O_3 films annealed *in-situ* at 200°C.

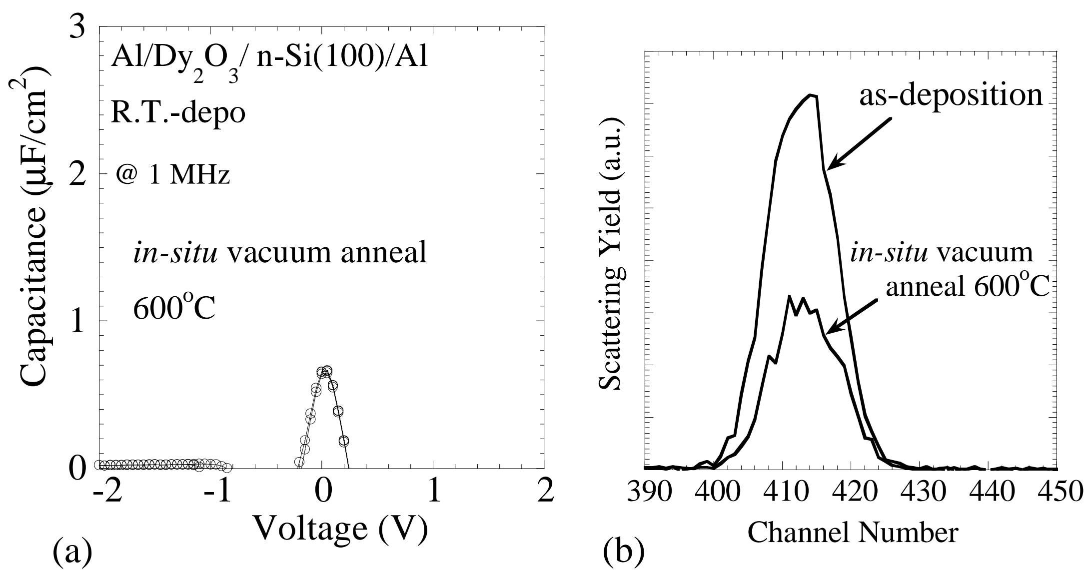


Fig. 3.22: (a) C-V characteristic and (b) RBS measurement for the Dy_2O_3 films annealed *in-situ* at 600°C.

3.3.2 Effect of the Surface Pretreatment of Si Substrate

In order to investigate the effect of the interfacial condition, Dy_2O_3 films were deposited on the different surface conditions, which were bare Si substrate (HF-last) and chemically oxidized substrate by H_2O_2. The formed chemical oxide layer thickness was ~ 0.5 nm. Both were annealed *in-situ* in the vacuum at 400°C after deposition. Their C-V and J-V characteristics were compared in Fig. 3.24. It is found that the accumulation capacitance value for the film on the chemical oxide was lower than that of the film on HF-last because of its additional thickness due to the chemical oxide. However, negative V_{FB} shift was smaller about 0.1 V than that of the HF-last film. By inserting chemical oxide at the interface, the positive interfacial charges were suppressed. Leakage current was also suppressed by the chemical oxide. The AFM images of the surface morphologies for the films before and after IVA with chemical oxide were showed in Fig. 3. 25. As well as the case of HF-last, flat surfaces were observed for the films deposited on the chemical oxide. The interfacial state density (D_{it}) values were estimated roughly by Terman method. Fig. 3.26 shows the D_{it} values for the samples with and without chemical oxide pretreatments. It was confirmed that the chemical oxide pretreatment improved D_{it} values for both *in-situ* vacuum anneal and non-anneal cases. In terms of the D_{it}, the films deposited on the chemical oxide and annealed *in-situ* showed the excellent electrical characteristics.

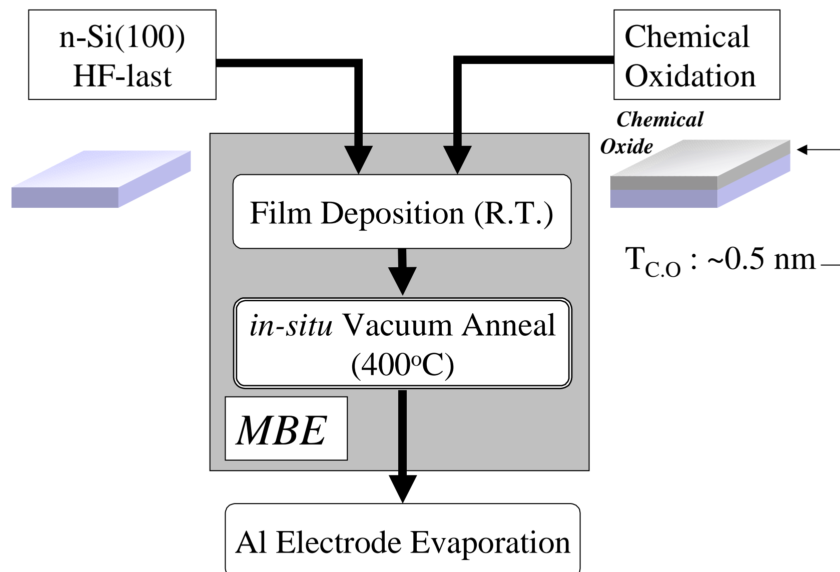


Fig. 3.23: Process flow.

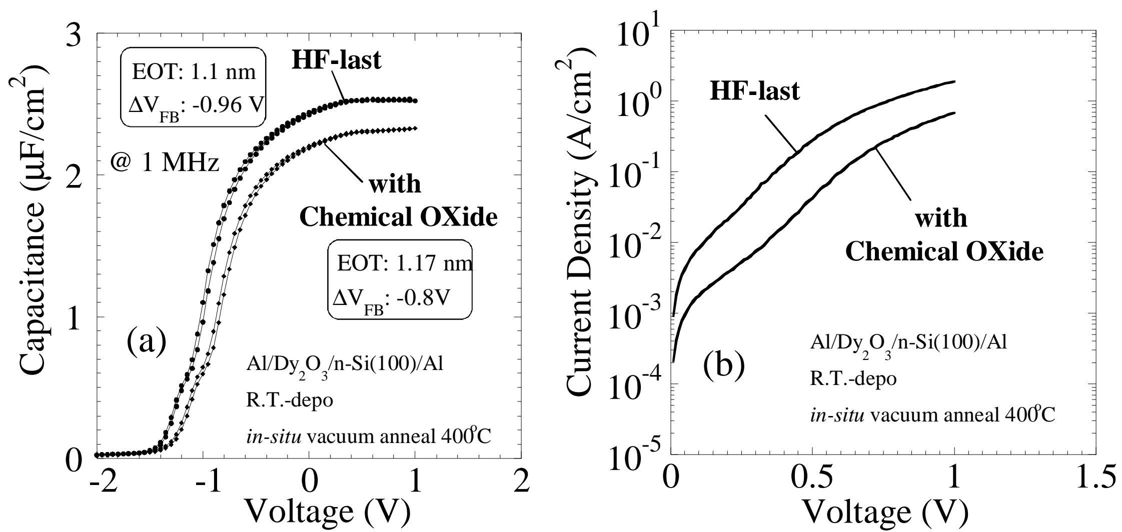


Fig. 3.24: (a) C-V and (b) J-V characteristics for the Dy_2O_3 films deposited on HF-last and chemical oxide

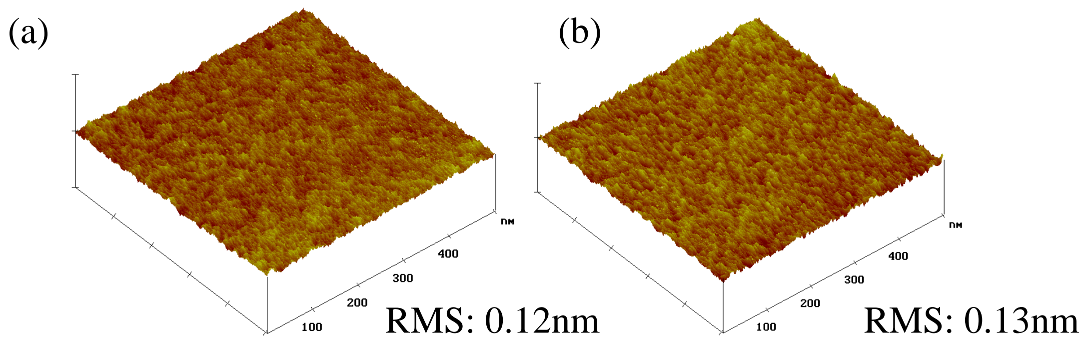


Fig. 3.25: AFM images of the surface morphologies for Dy_2O_3 films deposited on the chemical oxide. (500 x 500 nm, 5 nm/div)
(a) as-deposed, (b) after *in-situ* vacuum anneal.

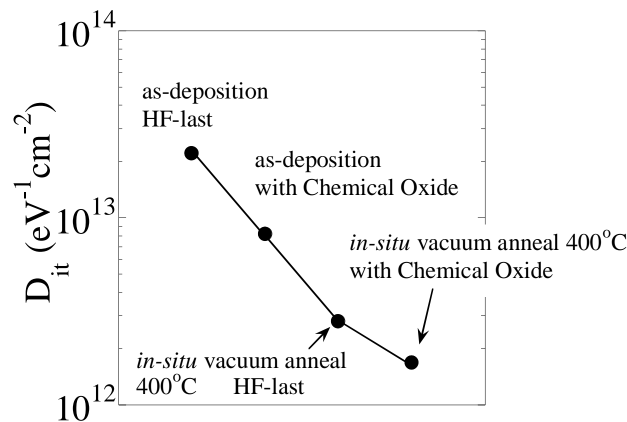


Fig. 3.26: Interfacial state density Dit depending on the annealing and wafer pretreatments.

3.3.3 V_{FB} Shift and Oxide Charge

For the purpose of searching the origin of the V_{FB} shift caused by *in-situ* vacuum anneal, dependence of ΔV_{FB} on the film thickness was investigated. Dy_2O_3 films of different thickness were deposited at R.T. on HF-last and chemical oxide. Then, they were annealed *in-situ* in the vacuum at 400°C for 90min. ΔV_{FB} of the films were calculated from the C-V characteristics measured at 1 MHz. Thickness dependence of the C-V characteristics was showed in Fig. 3.27 for HF-last and chemical oxide smples. Fig. 3.28 shows the relation between ΔV_{FB} and EOT. Generally, as the film thickness increase (rightward of the horizontal axis), ΔV_{FB} increases (upward of the vertical axis). However, correlation between ΔV_{FB} and thickness was not observed in the case of HF-last. At the same EOT, ΔV_{FB} changed for every deposition. On the other hand, a slight correlation was found in the case of chemical oxide. It was considered that the film characteristics of HF-last samples were affected by the little difference of interfacial condition that was formed during chemical cleaning or transportation to the vacuum chamber. Therefore, analysis of ΔV_{FB} was carried out using the experimental results for the films on chemical oxide.

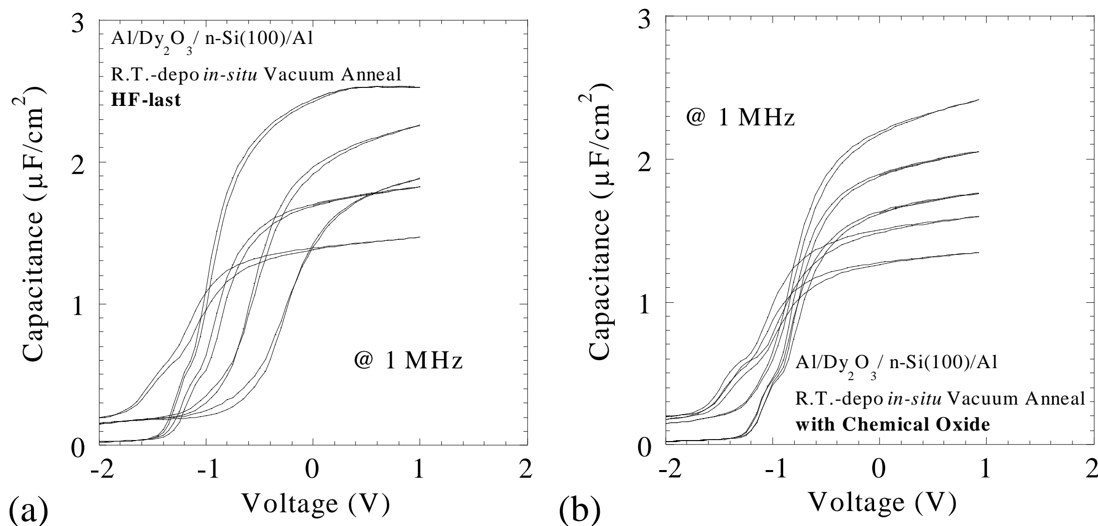


Fig. 3.27: Set of typical C-V curves for the films on (a) HF-last (b) chemical oxide.

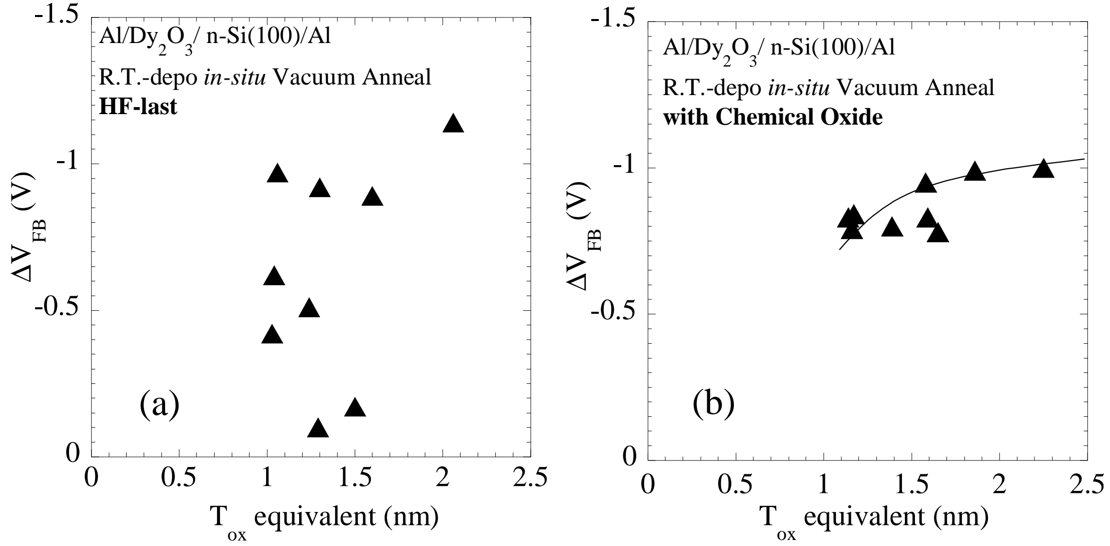


Fig. 3.28: Relation between EOT and ΔV_{FB}.
(a) HF-last, (b) chemical oxide

The equivalent oxide charge density per unit area Q_{ox} was estimated from the following equation. Here, Q_{ox} is located at the interface between Si and insulator.

$$Q_{ox} = -C_{ox} \cdot \Delta V_{FB} \quad (3.2)$$

Q_{ox} depending on the physical thickness was showed in Fig. 3.29. Film thicknesses were measured by ellipsometer. As shown in this plots, Q_{ox} increased as the thickness decreased. As the simple approximation, 1-dimentional MOS structure was considered (Fig. 3.30). Assuming a physical model that the oxide charge was distributing uniformly in the insulator, the charge density ρ was calculated. Relation between Q_{ox} and ρ was expressed as following.

$$Q_{ox} = -\int_0^{t_{ox}} \frac{x}{t_{ox}} \rho(x) dx + Q_{it}(\varphi_s) \quad (3.3)$$

Here, Q_{it} is interfacial trap density. To simplify, Q_{it} was neglected by considering that measurement frequency was sufficient to suppressed carrier response. In this model, ρ(x) is constant, so it was given by

$$\rho = \frac{2Q_{ox}}{T_{ox}} . \quad (3.4)$$

Substituting experimental results of Q_{ox} in this equation, ρ was estimated as shown in Fig. 3.31. It was found that oxide charge density increased as the film became thinner. It seemed a strange result because the whole films were fabricated by the same formation condition. Therefore, it was natural to consider the fixed charges were distributing locally at somewhere in the film rather than uniform.

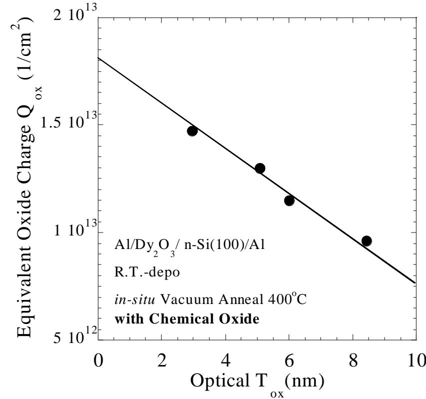


Fig. 3.29: Equivalent oxide charge per unit area.

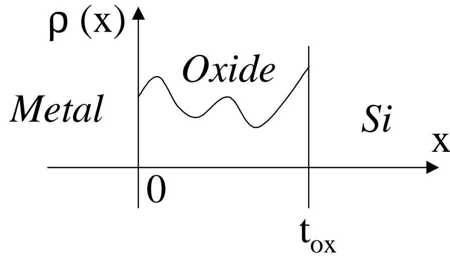


Fig. 3.30: 1D model of oxide charge density.

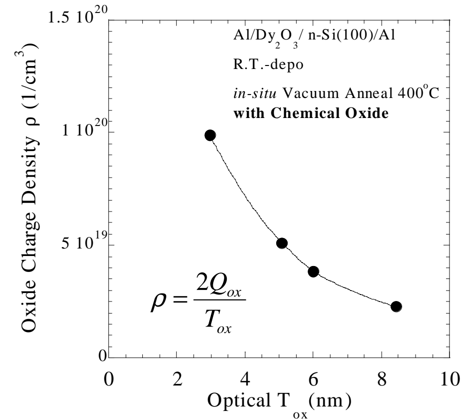


Fig. 3.31: Calculated oxide charge density.

Next, considering the charge distributions which have constant value of ρ and Q_{ox} for any thickness, T_{ox}-ΔV_{FB} characteristics were calculated. ΔV_{FB} was calculated by using the following equation.

$$\Delta V_{FB} = -\frac{e}{\varepsilon_{ox}}\left(\int_0^{t_{ox}} x \cdot \rho(x)dx + Q_{it}(\varphi_s)\cdot t_{ox} \right) \tag{3.5}$$

Fig. 3.32 shows the case of constant ρ. Because ρ is constant, ΔV_{FB} is quadratic function for film thickness. The calculation result did not show good fitting to the experimental. Also, in the case of the model that sheet charge is located at the interface of Si-oxide in δ-function, the slope of the calculation curve is abrupt to the experimental result (Fig. 3.33). Then, another charge model was considered. Sheet charges locate at the Si-oxide interface and fixed distance from the metal-oxide interface. In this model, calculation curve showed good fitting to the experimental plots, as shown in Fig. 3.34. In this calculation, sheet charge in the oxide was located at 1nm from the metal-oxide interface. Therefore, fixed oxide charges may exit at not only Si-oxide interface but also near the metal-oxide interface from this result.

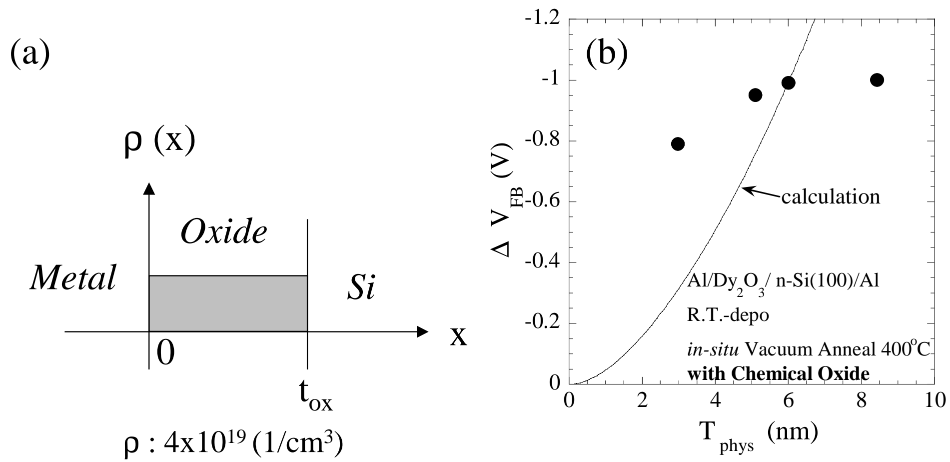


Fig. 3.32: (a) Model of oxide charge density and (b) calculation of ΔV_{FB}.

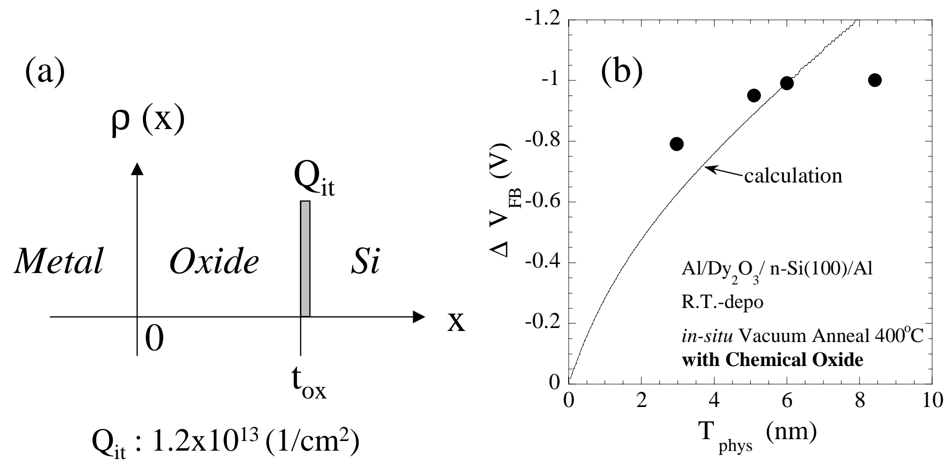


Fig. 3.33: (a) Model of oxide charge density and (b) calculation of ΔV_{FB}.

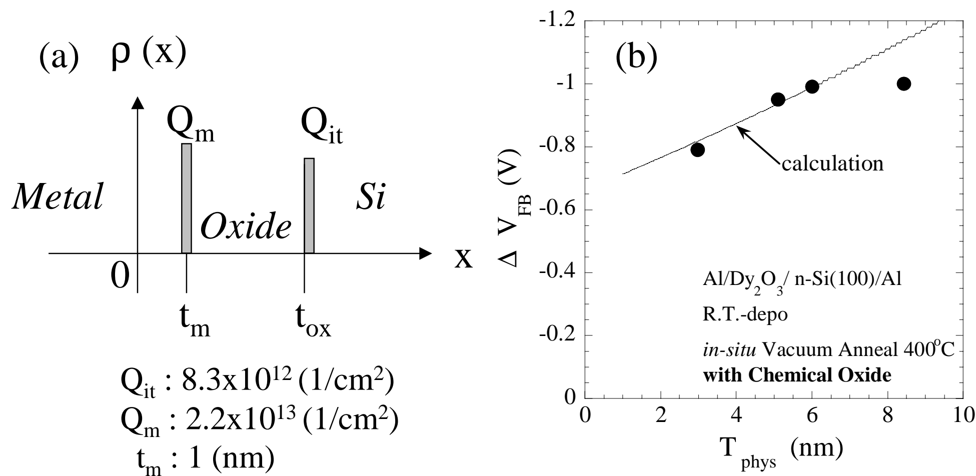


Fig. 3.34: (a) Model of oxide charge density and (b) calculation of ΔV_{FB}.

Another distribution functions of the oxide charge density were assumed. In these functions, charge density decreases gradually as it keeps away from the interface. Then, Q_{ox} and ΔV_{FB} were calculated by substituting the function into equation 3.3 and 3.5. First, a model that oxide charges are located at near the interface of Si and oxide was assumed (Fig. 3.35 (a)). However, in this approximation, calculated Q_{ox} and ΔV_{FB} did not fit the experimental result of them well as shown Fig. 3.35 (b) and (c). Next, a model that oxide charges distributed highly at the interface of not only Si-oxide but also metal-oxide was assumed (Fig. 3.36 (a)). In this model, calculated values of Q_{ox} and ΔV_{FB} showed good fitting to the experimental as shown in Fig. 3.36 (b) and (c). Therefore, oxide charges may be located at the metal-oxide interface from these analyses. However, these analyses were not sufficient to determine the profile of oxide charge distribution.

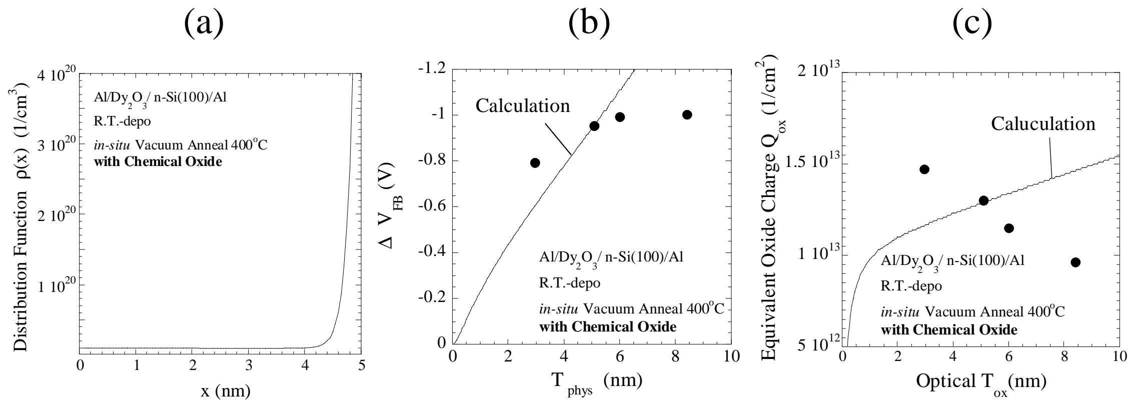


Fig. 3.35: (a) Distribution function of oxide charge density.
Calculated (b) ΔV_{FB} and (c) Q_{ox} using the function.

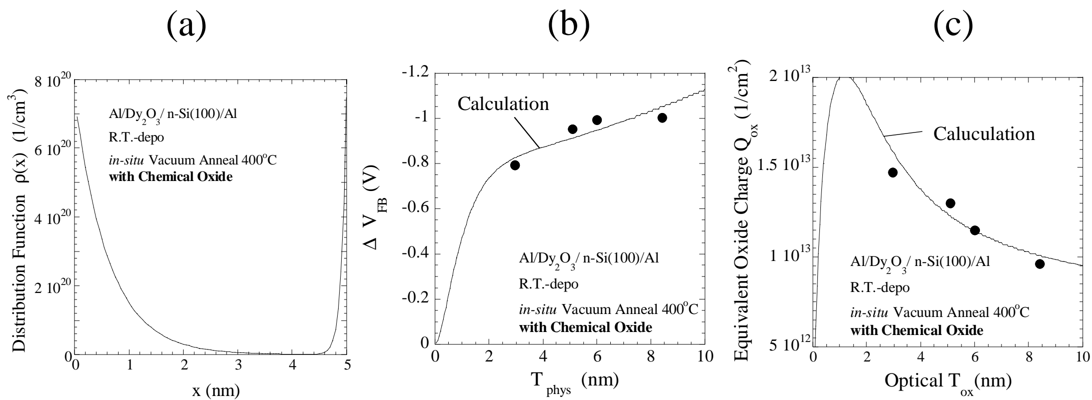


Fig. 3.36: (a) Distribution function of oxide charge density.
Calculated (b) ΔV_{FB} and (c) Q_{ox} using the function.

3.3.4 *In-situ* Vacuum Anneal and Subsequent RTA

Dy_2O_3 thin films were annealed by RTA (400°C and 600°C) in O_2, after 400°C *in-situ* vacuum anneal. In the case of 400°C RTA, (the same temperature with *in-situ* vacuum anneal) EOT slightly increased (about 0.1nm) by the RTA, but V_{FB} were not improved. (Fig. 3.38 (a)) On the other hand, V_{FB} shifted to positive direction from the initial position by the 600°C RTA. Additionally, it was found that the difference of capacitances for the film with and without chemical oxide is observed even after RTA. This difference is not observed in the case of without *in-situ* anneal (Fig. 3.38 (b)). This suggests that the chemical oxide quality is improved by the *in-situ* vacuum anneal.

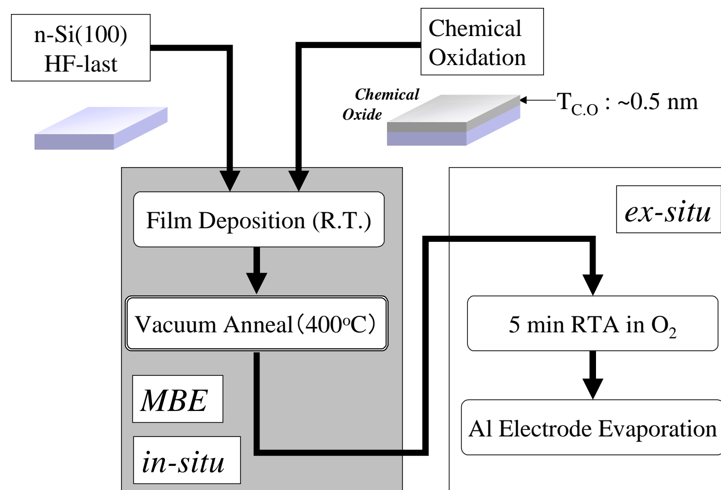


Fig. 3.37: Process flow

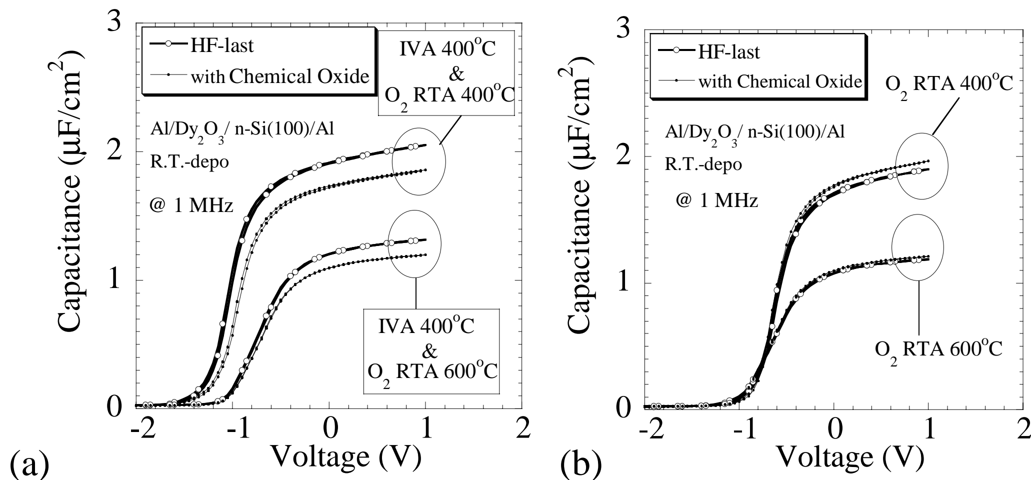


Fig. 3.38: C-V characteristics for the films after RTA (a) with and (b) without *in-situ* vacuum anneal

3.3.5 Deposition Temperature Dependence

Dy_2O_3 thin films were deposited on HF-last and chemically oxidized Si substrate at 250°C and 400°C, then annealed *in-situ* at 400°C for 90 min. C-V, J-V characteristics of the films deposited at 250°C and 400°C were showed in Fig. 3.40 and Fig. 3.41 respectively. Huge hysteresis of charge injection type in the C-V curve was observed for the HF-last film in the both deposition temperature case. For the case of chemical oxide, hysteresis was also observed and capacitance rolled down at high voltage. These results were not seen in the case of R.T. deposition as shown in Section 3.3.2. Here, remind the result obtained in the previous section. In Section 3.1.3, it is suspected that the film quality of R.T. deposition was tighter than that of 250°C deposition. All these results considered together, it is suspected that the Dy_2O_3 film quality became leaky because of oxygen atom deficit during the high temperature deposition. However, it should be notice that V_{FB} did not shift to the negative side for the films on the chemical oxide. It indicates that the good interfacial condition was formed by the combination of high deposition temperature and chemical oxide.

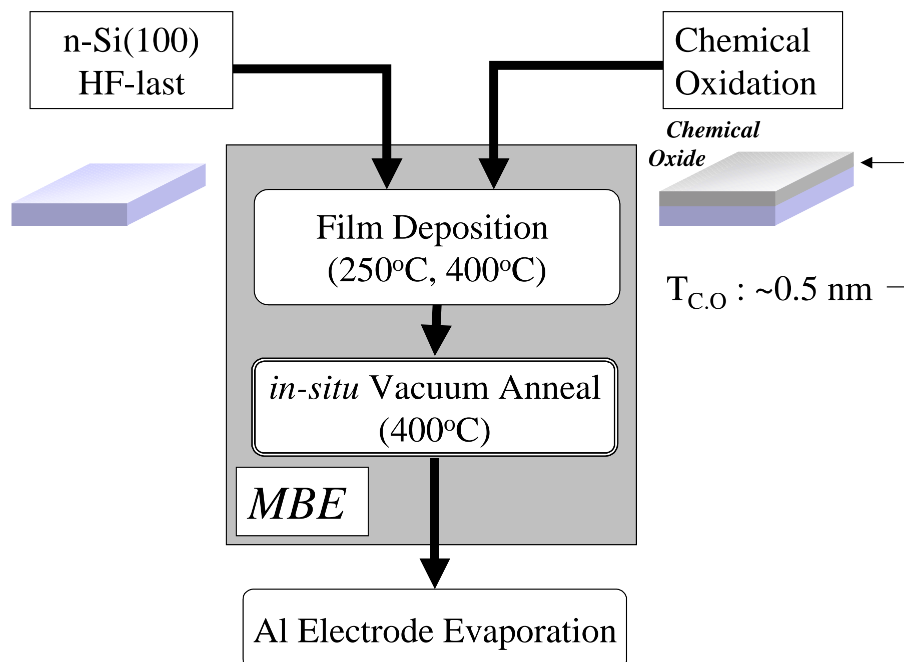


Fig. 3.39: Process flow

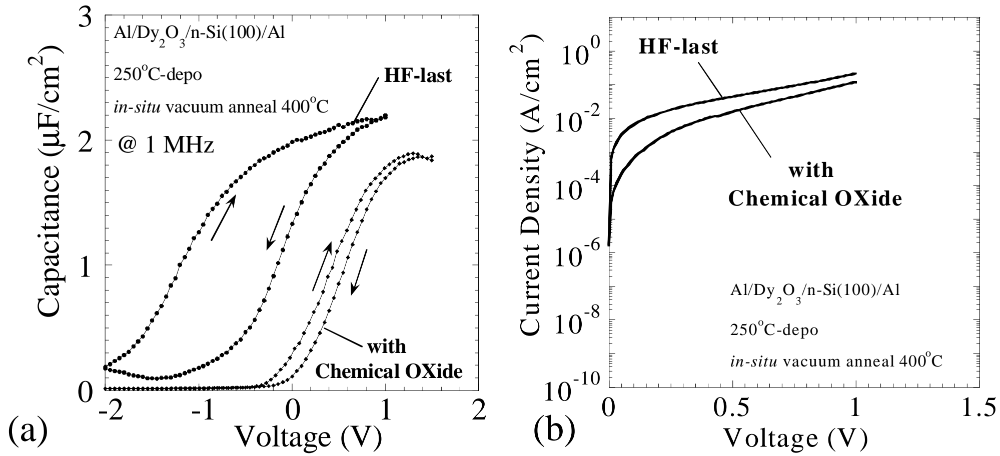


Fig. 3.40: (a) C-V and (b) J-V characteristics for the films deposited on HF-last or chemical oxide at 250°C.

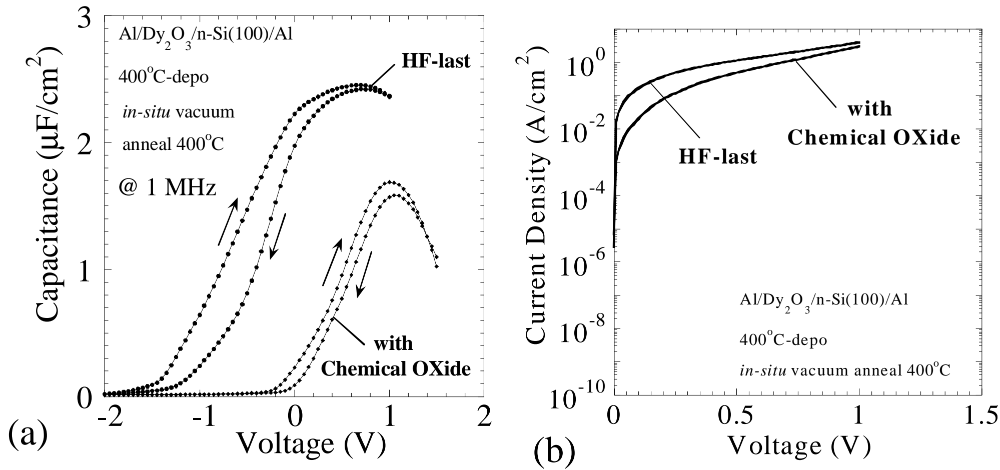


Fig. 3.41: (a) C-V and (b) J-V characteristics for the films deposited on HF-last or chemical oxide at 400°C.

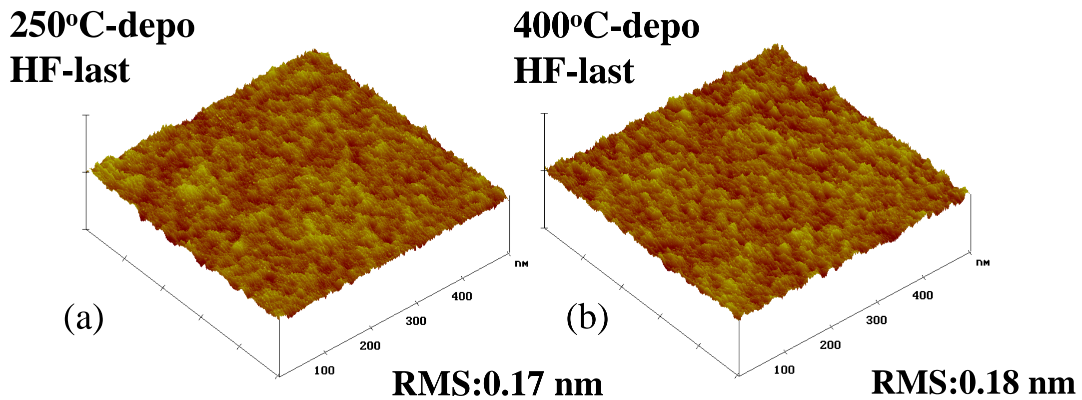


Fig. 3.42: AFM images of the surface morphologies for Dy_2O_3 films after *in-situ* vacuum anneal deposited at (a) 250°C, (b) 400°C. (500 x 500 nm, 5 nm/div)

3.3.6 Effect of *Ex-situ* Vacuum Anneal

Effects of *in-situ* vacuum anneal were investigated from the previous sections. In this section, effect of *ex-situ* vacuum anneal was studied for the purpose of investigating the influence of atmosphere exposure. Dy_2O_3 thin films were deposited on Si substrate of HF-last or chemical oxide at R.T.~400^oC. Next, the films were exposed to the atmosphere for a few minutes. Then, they were transferred to the ultra-high vacuum chamber of MBE again and annealed at 400^oC for 90min.

Fig 3.44 shows the electrical characteristics for the R.T.-deposited films on HF-last substrate before and after *ex-situ* vacuum anneal and O_2 RTA. As shown in the C-V plots, the accumulation capacitance did not decrease after *ex-situ* vacuum anneal comparing the as-deposited film. Similarly, EOT-J plots for the *ex-situ* vacuum anneal (EVA) were on the line of *in-situ* vacuum anneal (IVA) as shown in Fig 3.45. Therefore, change of characteristic of the thin film caused by atmosphere exposure was not confirmed for the case of R.T. deposition.

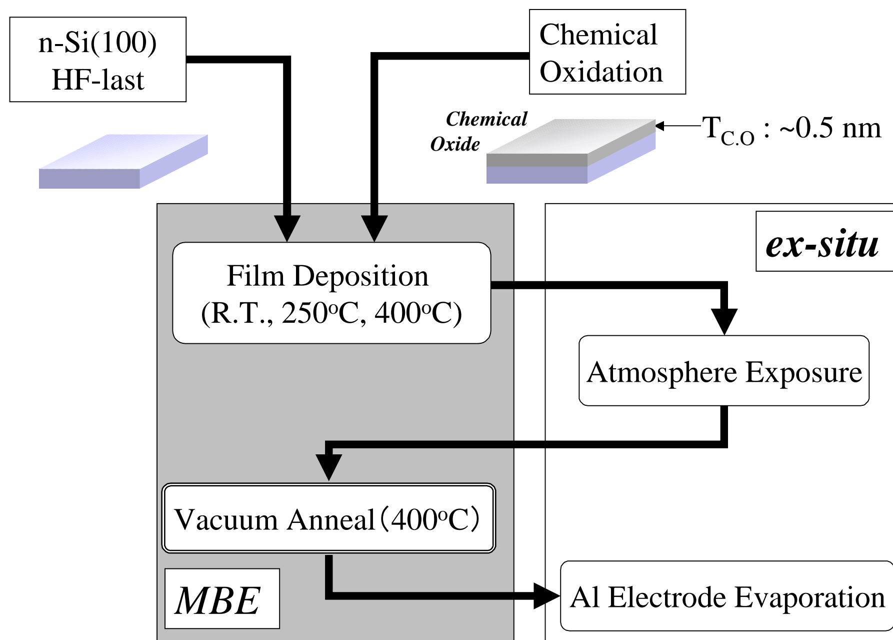


Fig. 3.43: Process flow

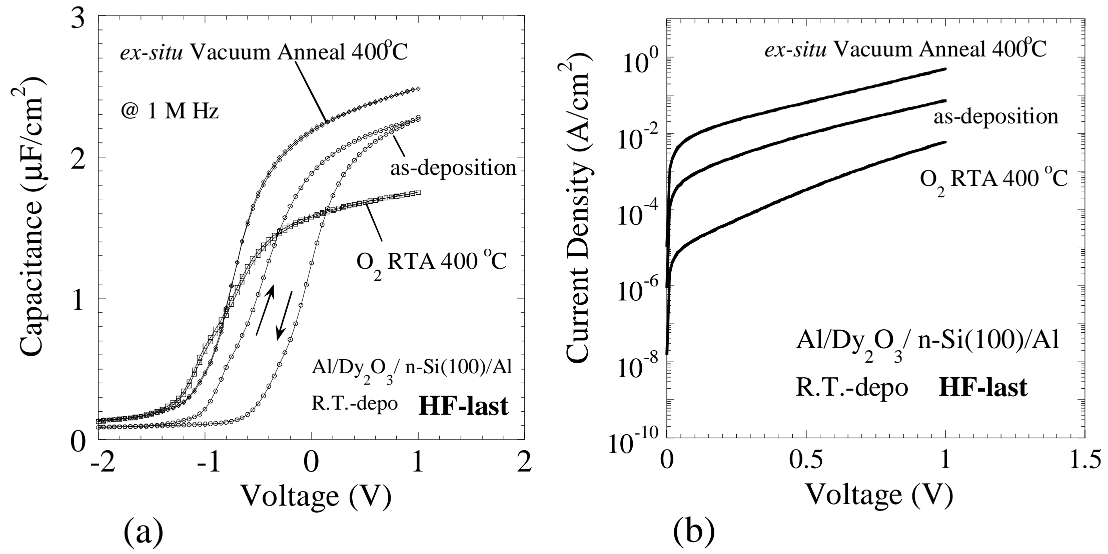


Fig 3.44: (a) C-V and (b) J-V characteristics for the films deposited on HF at R.T.

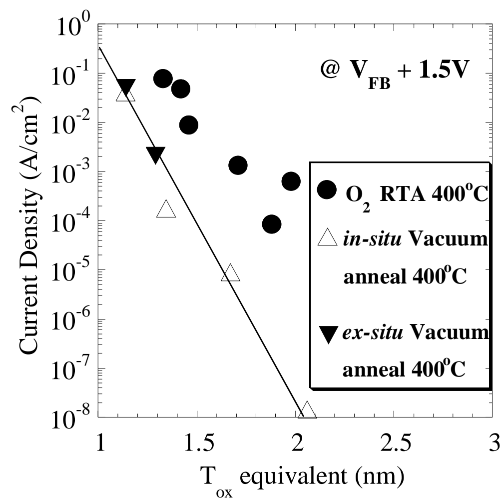


Fig. 3.45: EOT-J plot for the film after *in-situ*, *ex-situ* vacuum anneal and O_2 RTA.

However, the case of 250°C and 400°C deposition showed the different result from *in-situ*. Fig. 3.46 and Fig. 3.47 showed the C-V, J-V characteristics for the films deposited on HF-last substrate at 250°C and 400°C, respectively. They are the samples of as-deposition and after *ex-situ* vacuum anneal and O_2 RTA. It was found that hysteresis which observed in the C-V curves for the films of as-deposition and IVA (Fig. 3.40 (a)) disappeared after *ex-situ* vacuum anneal. It is considered as following. The moisture or oxygen in the air was absorbed on the surface or inside of the film when it was exposed to atmosphere. Then, absorbed oxygen complemented the deficit site in the thin film during the annealing. In this way, hysteresis in the C-V curve was improved by the effect of atmosphere exposure. However, V_{FB} shift was not improved still.

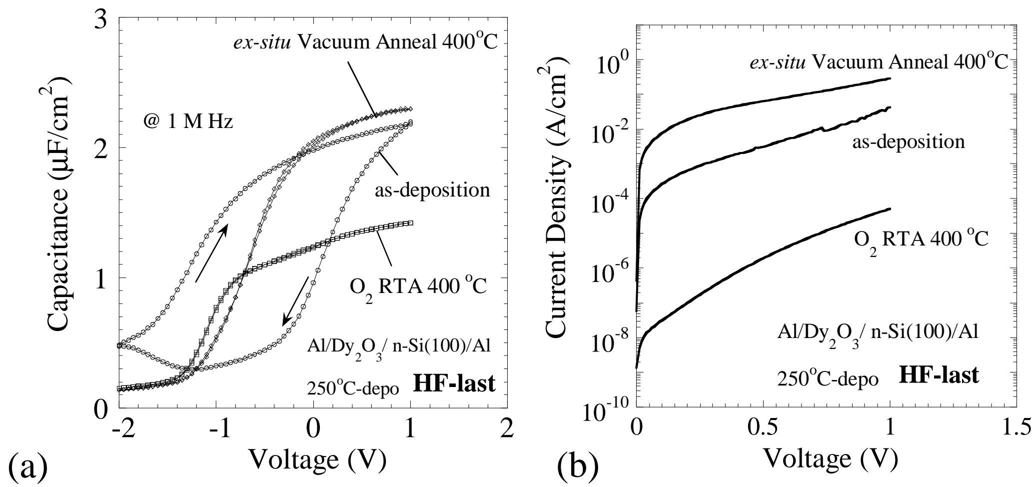


Fig. 3.46: (a) C-V and (b) J-V characteristics for the films deposited at 250°C.

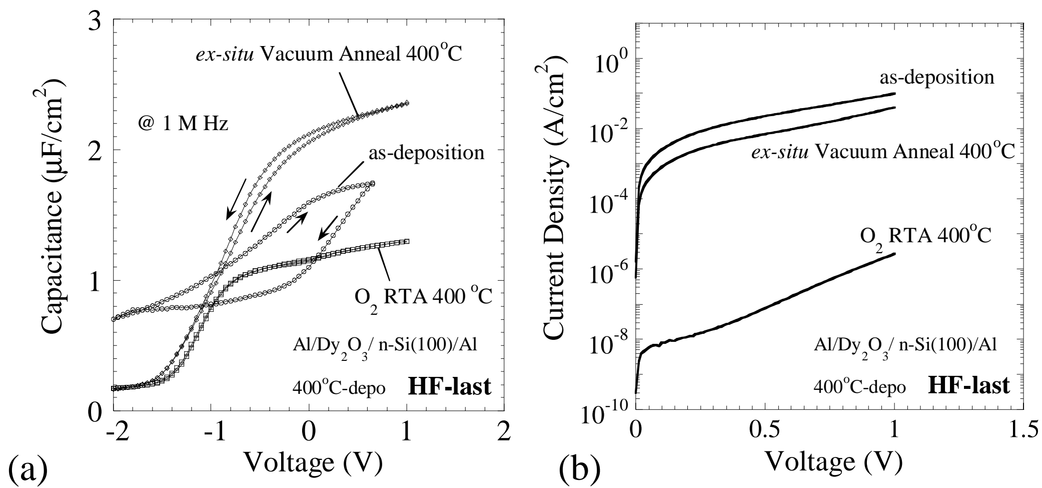


Fig. 3.47: (a) C-V and (b) J-V characteristics for the films deposited at 400°C.

In the case of *in-situ* vacuum anneal after high temperature deposition, V_{FB} did not shifted to the negative side for the film on the chemical oxide (Section 3.3.5). Therefore, by combing the effect of *ex-situ* vacuum anneal and chemical oxide, ideal C-V characteristic was expected. Fig. 3.48 showed the C-V, J-V characteristics for the films deposited on the chemical oxide at 250°C. They are the samples of as-deposition, after *ex-situ* vacuum anneal and O_2 RTA. Although small hysteresis was observed, ideal C-V curve without V_{FB} shift was obtained by *ex-situ* vacuum anneal. The EOT and ΔV_{FB} was 1.1 nm and 0.08 V, respectively. Fig. 3.49 showed the measurement frequency dependence of the C-V characteristics for the film. As shown in the graph, frequency dispersion was not observed. This is the optimum formation condition for Dy_2O_3 thin film in this work.

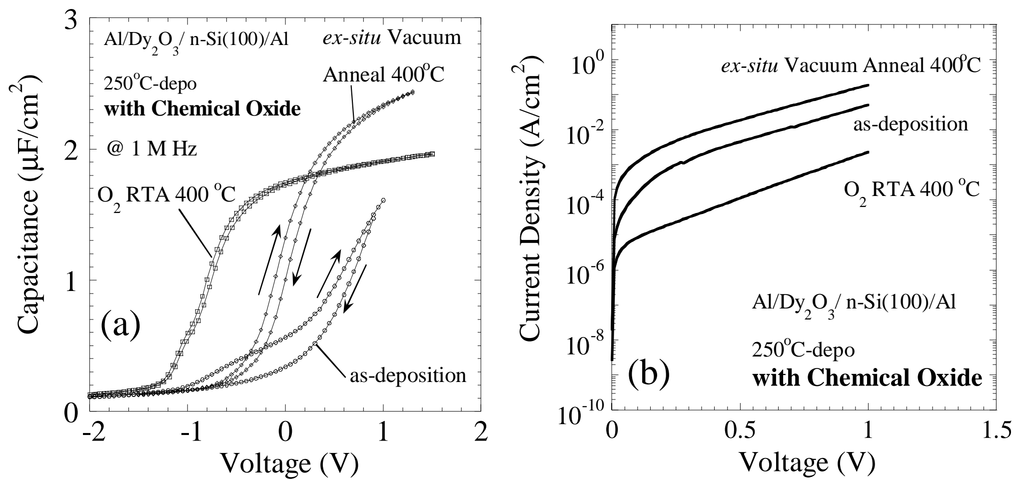


Fig. 3.48: (a) C-V and (b) J-V characteristics for the films deposited on the chemical oxide at 250°C.

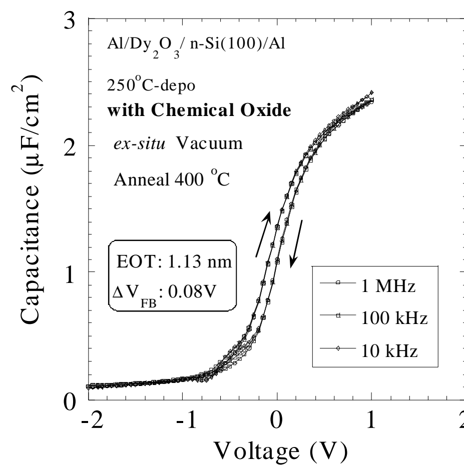


Fig. 3.49: frequency dispersion of the C-V characteristics for the film deposited on the chemical oxide at 250°C.

Chapter 4

Conclusions

4.1 Results of This Study

Dy_2O_3 thin films deposited at R.T. ~ 400°C by MBE. They were annealed *in-situ* or *ex-situ* at 200°C ~ 600°C in the ultra-high vacuum chamber of MBE system. Excellent C-V characteristics without hystersis were obtained with suppressing the accumulation capacitance decrease by vacuum anneal at R.T.-deposition. Comparing with the conventional RTA method, the electrical characteristics were improved by vacuum anneal. It was found that by the conventional O_2 RTA, low-dielectric interfacial layer consisted of silicate was formed. On the other hand, although the interfacial layer was formed by *in-situ* vacuum anneal, its dielectric constant was larger and the thickness was smaller than the RTA case. The interfacial layer structure of vacuum annealed sample was similar to that of as-deposited film. It cased excellent electrical characteristics on the Dy_2O_3 films.

V_{FB} shift was observed in the C-V characteristics of the films after *in-situ* vacuum anneal with R.T.-deposition. It was caused by the equivalent oxide charges of high density such as 10^{13} ($1/cm^2$). It was suspected that fixed charges distributed at the interface of not only Si-oxide but also metal-oxide from this analysis. V_{FB} shift was suppressed by 250°C ~ 400°C deposition on the chemical oxidized substrate. It is considered that good interfacial condition was formed by the combination of chemical oxide and high-temperature deposition. During this study, the best formation condition to suppress ΔV_{FB} was *ex-situ* vacuum anneal after 250°C-deposition with chemical oxide. EOT of 1.13 nm and ΔV_{FB} of 0.08 V were obtained for the film formed by the condition.

4.2 Future Issue

The mechanism of ΔV_{FB} was not clarified completely. It is necessary to study about the relation between ΔV_{FB} and the distribution of the oxide charges. For the purpose of clarifying the mechanism of oxide charge generation during the fabrication process, more detail analyses should be carried out from both the sides of electrical characteristics and physical or chemical measurements. With studying these problems, farther optimization of the formation condition for ultra-high vacuum anneal is necessary. For example, improvement of small hysteresis observed in C-V curve for *ex-situ* vacuum annealed sample on chemical oxide at 250°C. Also, Good C-V characteristics may be obtained by depositing at lower temperature than 250°C with *in-situ* vacuum anneal without atmosphere exposure. Simultaneously, for the

application to the gate insulator of transistor, the characteristics of MOSFET with the film formed by this annealing method should be investigated.

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Appendix

For the purpose of examining material dependence, the effects of ultra-high vacuum anneal for La_2O_3 were investigated. La_2O_3 is one of rare earth oxides and has larger bandgap than Dy_2O_3 (Fig. A.1). La_2O_3 thin films were deposited on the HF-last and chemical oxidized Si substrate at R.T. Then, they were annealed *in-situ* in the ultra-high vacuum chamber at 400°C for 90 min. Their electrical characteristics were showed in Fig. A.2. As well as Dy_2O_3, good C-V characteristics without hysteresis were observed by *in-situ* vacuum anneal. The ΔV_{FB} was about –1 V for both the samples of HF-last and chemical oxide. About V_{FB} shift, significant difference was not found by compared with Dy_2O_3 case. As shown in table A.1, leakage current was smaller than Dy_2O_3 thin film that has the same EOT to this La_2O_3 sample. It is considered that leakage current was suppressed by large bandgap of La_2O_3. AFM images of surface roughness for the film before and after in-situ vacuum anneal were showed in Fig. A.3. Surface roughness did not changed by *in-situ* vacuum anneal as well as Dy_2O_3 case. Fig. A.4 shows electrical characteristics for *in-situ* vacuum annealed La_2O_3 films deposited on HF-last and chemical oxide at 250°C. Similarly, Fig. A.5 shows the case of 400°C deposition. Hysteresis were observed in the C-V characteristics for both the cases of deposition temperatures. ΔV_{FB} was suppressed by combination of 400°C deposition and chemical oxide. Measurement temperature dependence of leakage current was showed in Fig. A. 6 for the films on HF-last and chemical oxide after *in-situ* vacuum anneal. Leakage currents increased as measurement temperature became higher. Therefore, leakage current was dominant for P-F transmission.

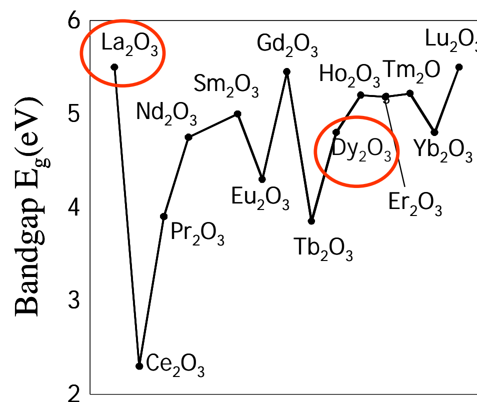

Fig. A.1: Bandgap of rare earth oxides.

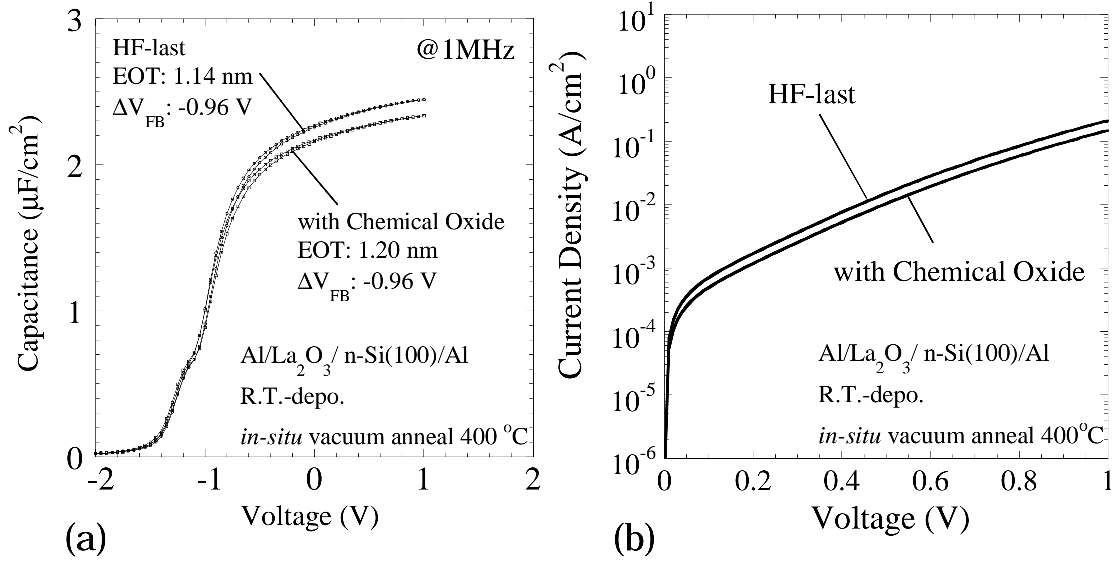

Fig. A.2: (a) C-V and (b) J-V characteristics for the La_2O_3 films fabricated by *in-situ* vacuum anneal 400°C 90 min after R.T. deposition.

Table. A.1: Comparison of electrical characteristics between La_2O_3 and Dy_2O_3.

R.T-depo. *in-situ* vacuum anneal 400°C
HF-last

	La_2O_3	Dy_2O_3
EOT	1.14 nm	1.14 nm
J @ V_{FB} + 1 V	5×10^{-3} (A/cm²)	4×10^{-2} (A/cm²)

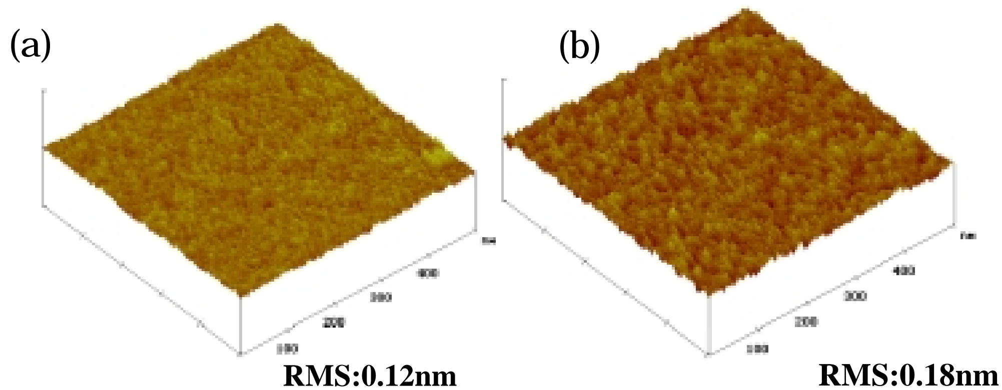

Fig. A.3: AFM images of the surface morphologies for La_2O_3 films.
(500 x 500 nm, 5 nm/div)
(a) as-deposited, (b) after *in-situ* vacuum anneal.

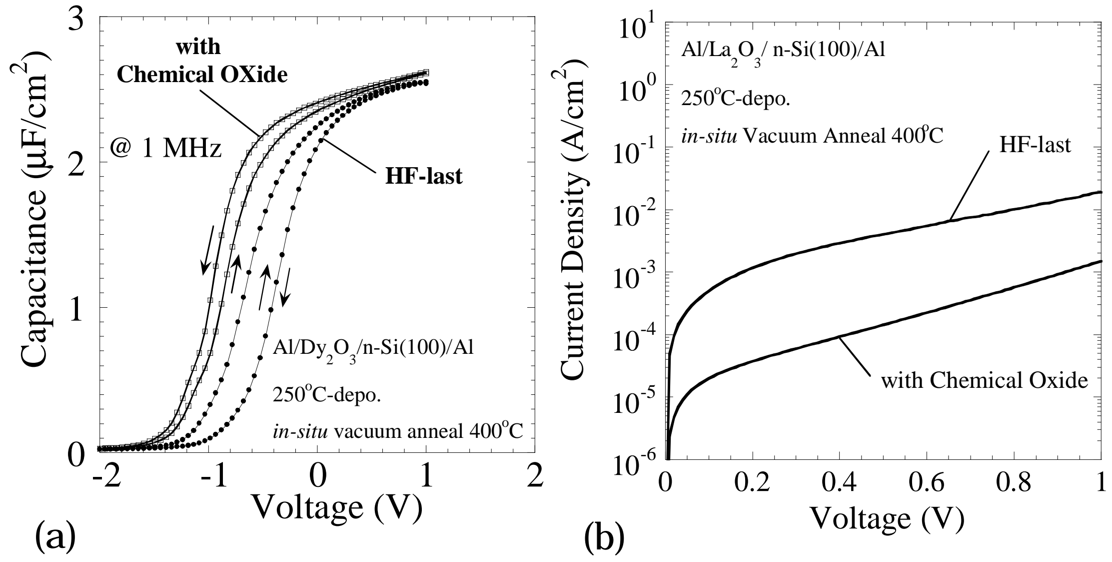

Fig. A.4: (a) C-V and (b) J-V characteristics for the La_2O_3 films fabricated by *in-situ* vacuum anneal 400°C 90 min after 250°C deposition.

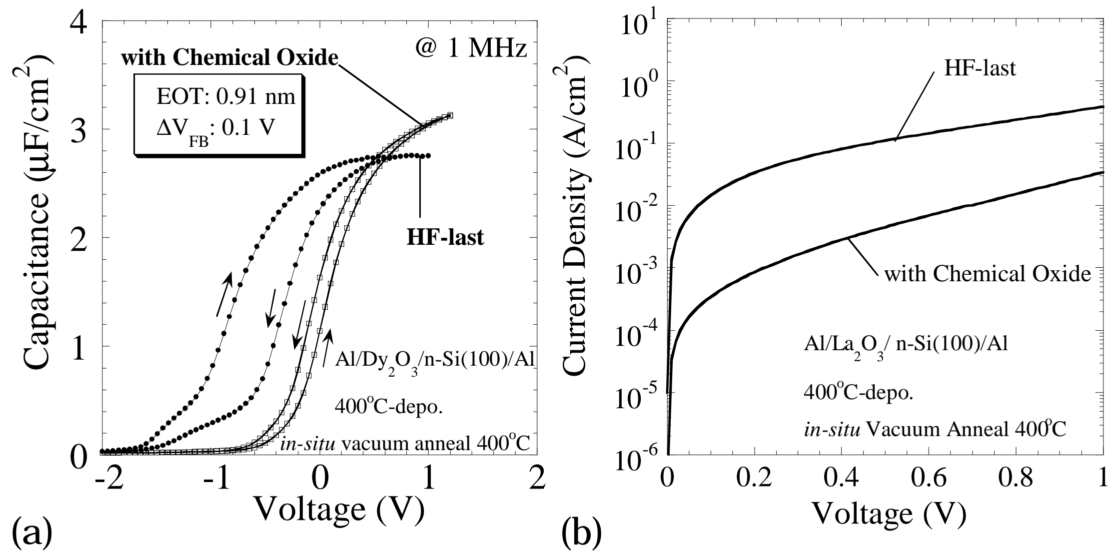

Fig. A.5: (a) C-V and (b) J-V characteristics for the La_2O_3 films fabricated by *in-situ* vacuum anneal 400°C 90 min after 400°C deposition.

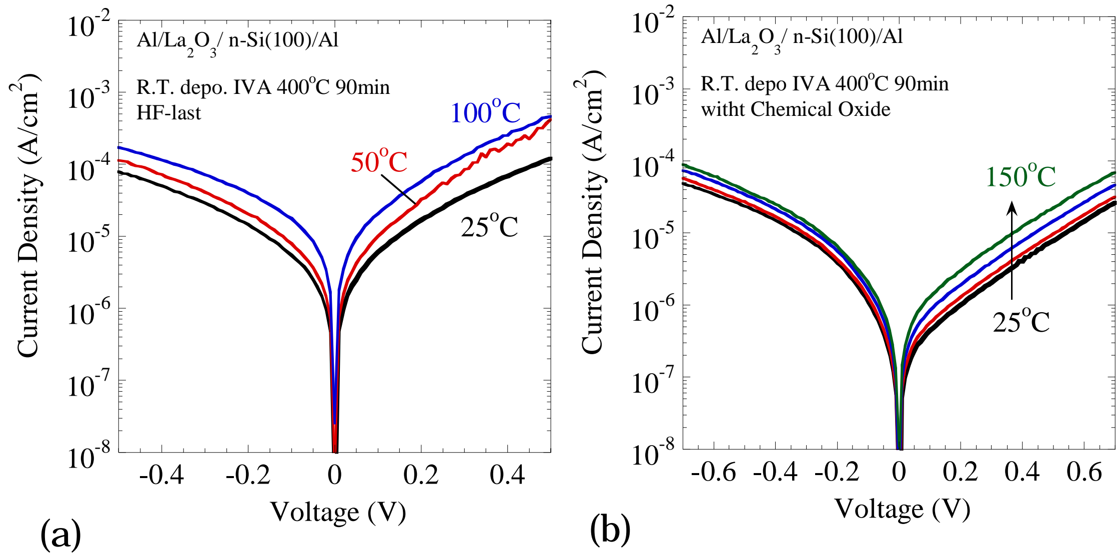

Fig. A.6: Measurement temperature dependence of the leakage currents for the films on (a) HF-last and (b) chemical oxide with in-situ vacuum anneal.
The film thickness was 2.5 nm.