3. The effect of the low temperature long time anneal for Dy_2O_3

Master thesis

A study on the effect of the low temperature long time anneal for Dy_2O_3 and fabrication process of TaN gate electrode

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3. The effect of the low temperature long time anneal for Dy_2O_3

CONTENTS

3. The effect of the low temperature long time anneal for Dy_2O_3

3. The effect of the low temperature long time anneal for Dy_2O_3

Chapter 1

Introduction

With aggressive scaling of Si-LSI, SiO_2 cannot suppress the gate leakage current, due to the oxide thinning. Therefore, SiO_2 should be replaced with High-k martial, which shows high dielectric constant.

In this chapter, brief overviews of background, and some issues of High-k gate dielectric were introduced.

3. The effect of the low temperature long time anneal for Dy_2O_3

1.1 Background of this study

Now, information technology is one of the most important technologies in our society. It improves the quality of our society by making social and personal activities more efficient using communication and computer networks. Resent rapid advance in information technology depends on the progress of semiconductor technologies, especially to that of Silicon Large-Scale Integrated Circuits (Si-LSIs).

And the progress of Si-LSIs is dependent on down sizing their components such as metal-oxide-semiconductor field effect transistor (MOSFTEs).

The downsizing has been accomplished by the scaling method. In order lateral and vertical dimensions and supply voltage are scaled down by the factor S, while Si-substrate impurity concentration is increased by the factor S as shown in Figure 1.1 and Table 1.1.

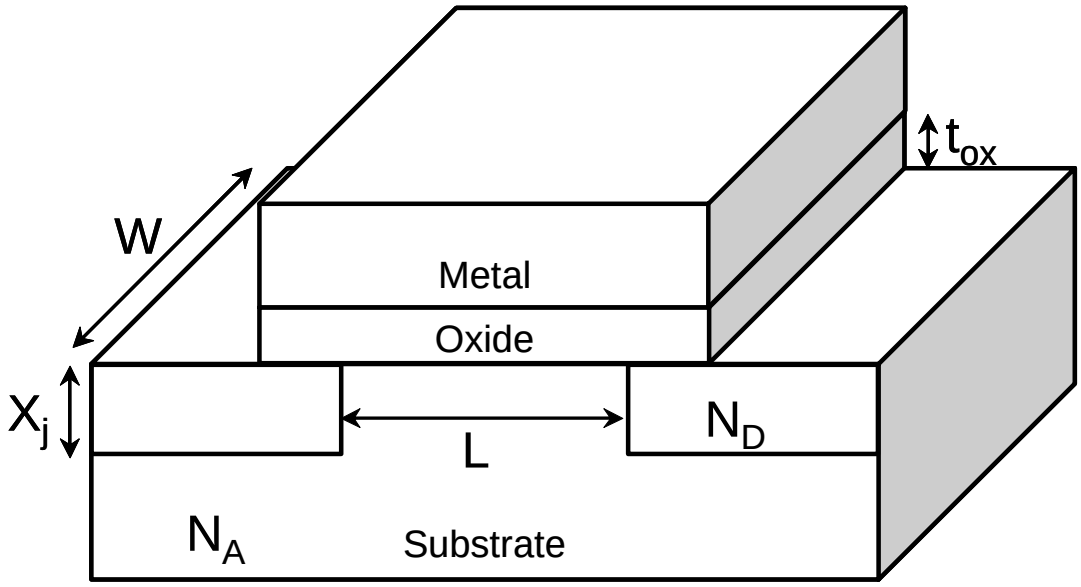

Figure 1.1 Schematic structure of a typical MOSFET

Table 1.1 Scaling of MOSFES by a scaling factor of k

MOSFET Device and Circuit Parameters	Multiple Factor (k>1)
Device dimension (t_{ox}, L, W, x_j)	1/k
Doping concentration (N_a, N_d)	k
Voltage (V)	1/k
Electric field (E)	1
Carrier velocity (v)	1
Capacitance ($C = \varepsilon LW/t_{ox}$)	1/k

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Since early sixties, (C)MOS device has relied on SiO_2 as the gate insulator. Further size reduction and the ever demanding technology roadmaps have imposed scaling constraints on gate insulator thickness to the point where excessive tunneling currents make transistor design untenable. The leakage current of 1nm-thick SiO_2 is $100A/cm^2$, therefore, power consumption becomes very huge. In order to suppress the huge leakage current below 1 nm regime, the replacement of SiO_2 with a high dielectric constant material which allows an increase in the physical oxide thickness maintaining a low equivalent oxide thickness (EOT) and low gate leakage current is necessary as shown in Table 1.2. Therefore, the replacement SiO_2 with High-k is promising to thick the film, keeping EOT as shown in Figure 1.2.

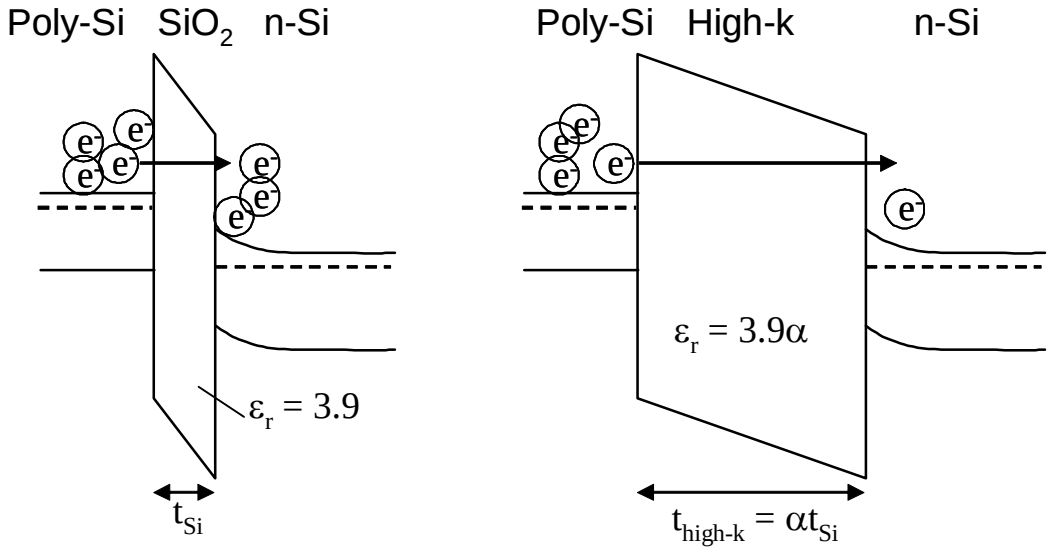


Figure 1.2 Reduction of leakage current by replacement SiO_2 with High-k material.

High-k material, which shows α times dielectric constant as much as SiO_2, allow to α times thickness with keeping the capacitance of insulator as following equation

$T_{eq} = \varepsilon_{si}/t_{si} = \varepsilon_{High\text{-}k}/t_{High\text{-}k}$

Table 1.2 ITRS for high performance logic

High-performance Logic Technology Requirements

Year	2001	2005	2013
L_G (nm)	65	32	18
T_{eq} (nm)	1.3 - 1.6	0.8 - 1.3	0.4 – 0.6

1.2 High-k gate insulator

Requirements to candidate dielectrics are:

1. a high dielectric constant k
2. stable in contact with silicon substrate at high temperature
3. a low density of defects in bulk ($Q_{tot} < 5x10^{10}$ cm^{-2}) and at the interface ($D_{it} < 5x10^{10}$ cm^{-2})
4. high offset barriers of 1 eV for both electrons and holes

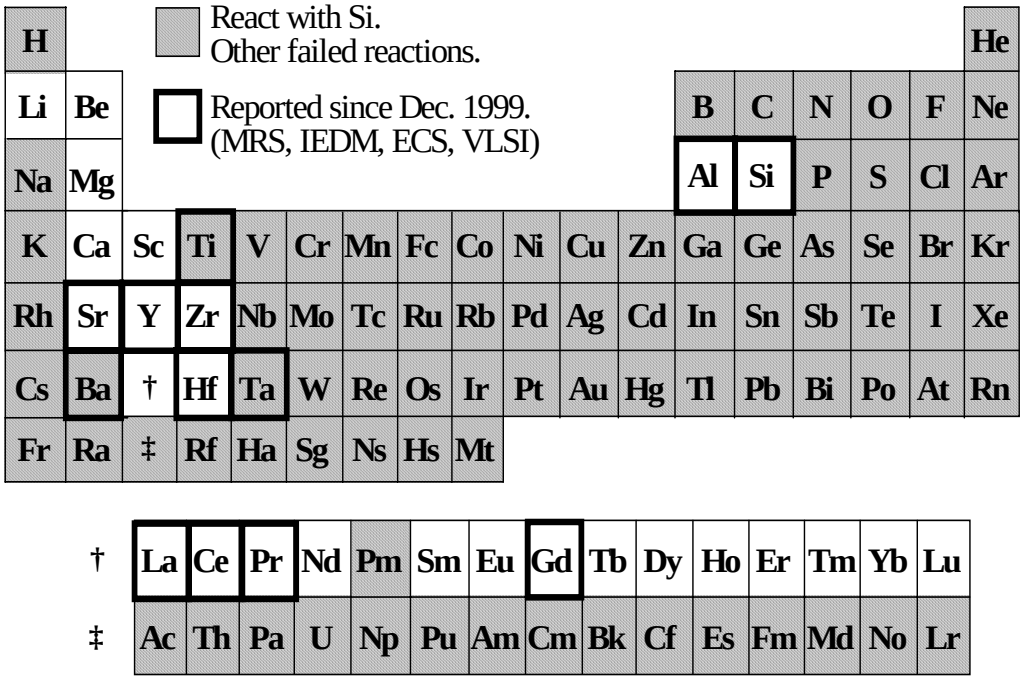
Metal oxides (MO_x) are promising candidates for the High-k gate material. Important properties needed for those metal oxides are:

1. no-radioactivity,
2. being solid at the temperature of LSI process
3. chemical stability at Si interface.

Table 1.3 shows candidates for the metal oxides that are thought to satisfy the above conditions (1-3)

Recently, many High-k materials such as Al_2O_3, ZrO_2, HfO_2, La_2O_3 or thereof (silicates, aluminates) have been investigated as gate insulator (shown in Figure 1.3) and promising results were obtained for the characteristics of J-EOT as shown in Figure. 1.4.

Table 1.3 Candidates for metal, oxide of which has possibility to be used as High-k gate insulator on periodic table



3. The effect of the low temperature long time anneal for Dy_2O_3

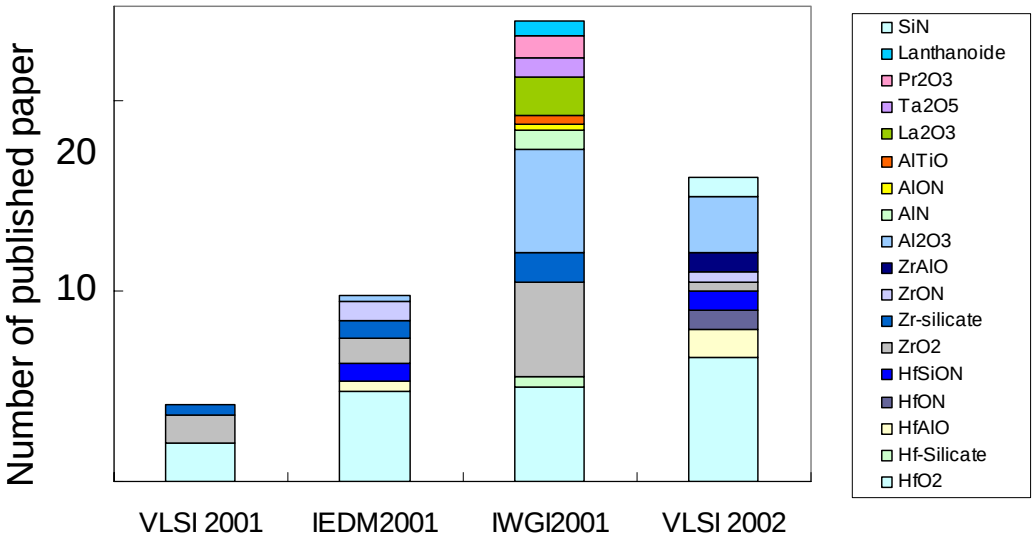


Figure 1.3 Reported materials as High-k gate insulator on VLSI symp., IEDM and IWGI

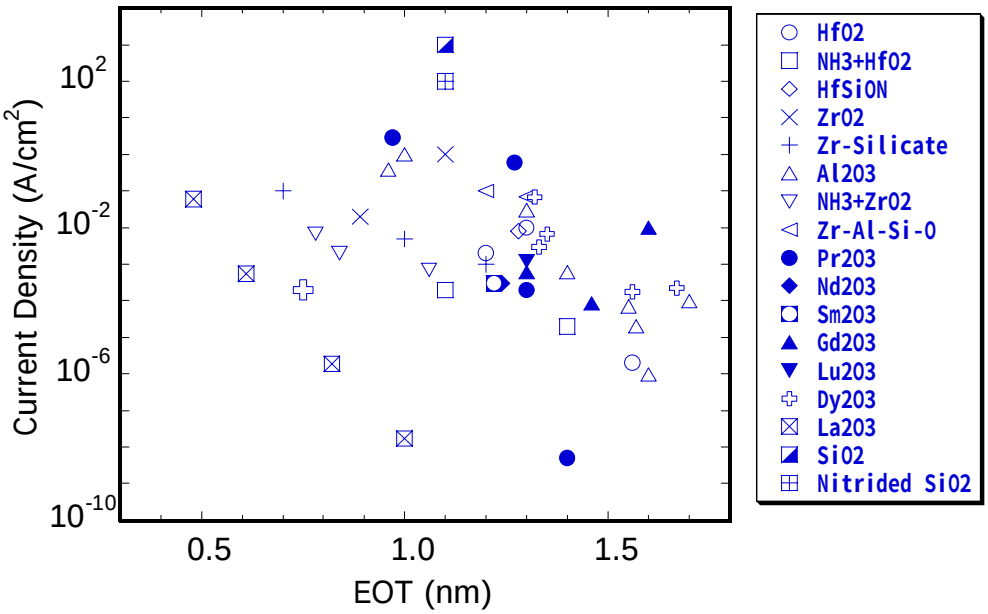


Figure 1.4 Current density – EOT characteristics for various High-k material

3. The effect of the low temperature long time anneal for Dy_2O_3

1.3 Issues of processing High-k material

However, one should realize there are still a number of problems to be solved. A brief overview of some these issues were given.

1.3.1 Crystallization during thermal process

During subsequent processing, High-k thin film must withstand thermal anneals at high temperatures up to 1000^{o}C during which they should not re-crystallize. Single oxide layers of ZrO_2 and HfO_2 are known to re-crystallize at fairly low temperatures (400 – 600 ^{o}C), depending on layer thickness. These crystallization causes leakage current and issues of reliabilities. To overcome this problem, silicate or aluminate of these oxides have been studied recently. Mixtures of HfO_2 or ZrO_2 with Al_2O_3 are found to re-crystallize only at much high temperature, up to 1000 ^{o}C.

1.3.2 Interfacial layer growth

Secondly, there is a issue of interfacial layer growth. The interfacial layer (SiO_x, silicate) that shows a low dielectric constant lower the effective dielectric constant of total insulator stacks. As shown figure 1.5, ZrO_2 tends to react with Si substrate. To overcome this problem, surface treatment (oxidized, nitrided) was known to be effective to suppress the interfacial reaction between Si and High-k materials.

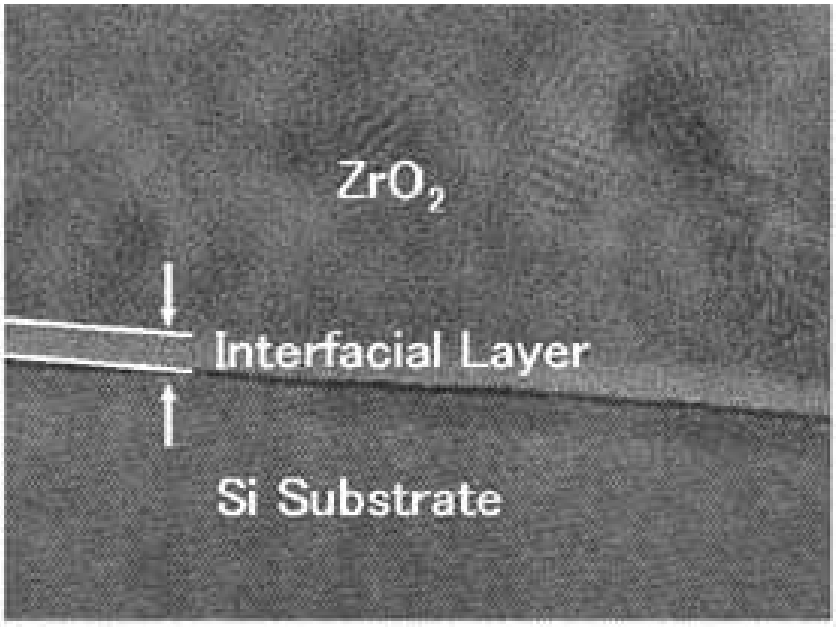


Figure 1.5 interfacial layer growth and micro crystallization

3. The effect of the low temperature long time anneal for Dy_2O_3

1.3.3 Reduction of carrier mobility in High-k devices

C-V and J-V characteristics on High-k capacitors are used to show the promising results of those new materials for gate insulator. However, recent result of mobility on MOSFET have indicated that electron and hole mobility underneath High-k layers is quite often strongly reduces as compared to SiO_2. A summary of recent data published at IEDM 2001 (Figure 1.6) indicates that this mobility is strongly influenced by the presence and characteristics of an interfacial layer, either SiO_2 or silicate-like. This mobility reduction is said to be due to phonon scattering. This could become a showstopper in view of the final aim of very low EOT values.

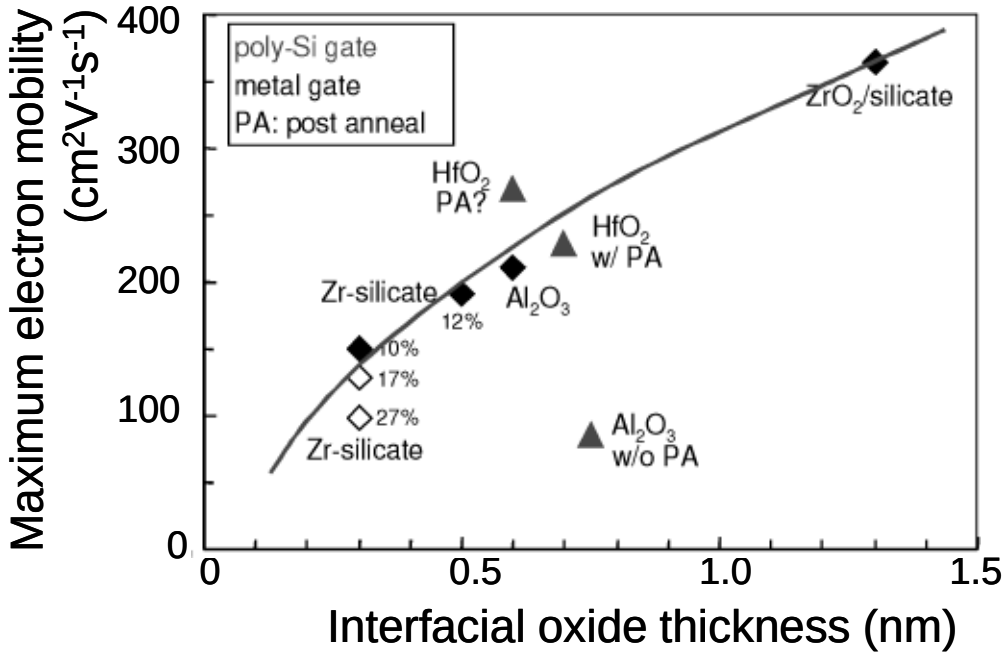


Figure 1.6 Electron mobility for various High-k material

1.4 Introduction of TaN gate electrode

In order to suppress the interfacial layer growth, the films were annealed after the gate metal deposition. Therefore, it is necessary to investigate on the metal electrode, which shows high thermal stability. In this study, TaN was investigated as gate electrode. This material is now researched at institutes all over the world in order to solve Poly-depletion effect.

As CMOS devices are scaled into sub-0.1 μm regime that High-k material is necessary for gate insulator, poly-depletion effects become a significant concern. They increase the effective oxide thickness, degrade the device performance, and make further gate

oxide scaling problematic.(Figures. 1.7, 1.8)

Therefore, metal gate electrodes are being explored to replace the Poly-Silicon gate to minimize the poly-depletion effects in addition to reduction of gate –line sheet resistance. The metal gates must have suitable work function and required thermal and chemical stability with underlying thin gate insulator for CMOS processing. Several materials have been studied as a replacement for poly-Si, such as TiN, Mo, Ta, TaN etc.

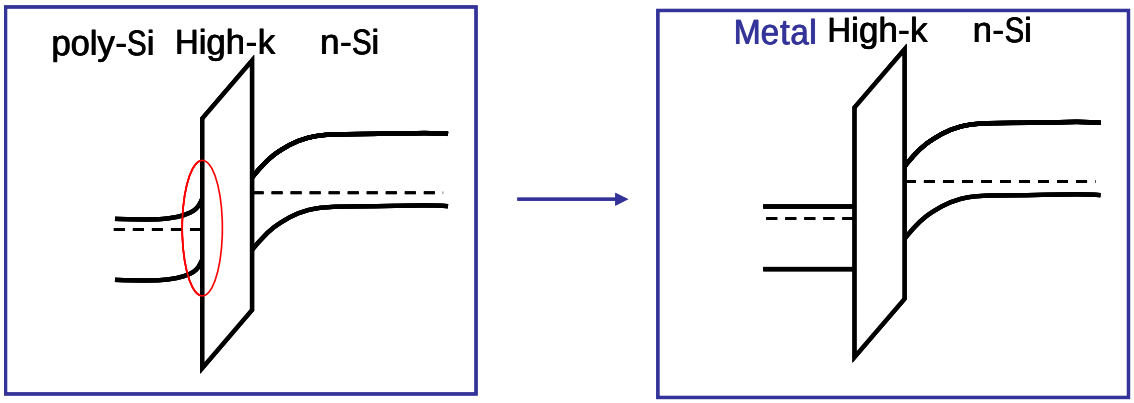


Figure 1.7 Schematic diagram of Poly-depletion effect

3. The effect of the low temperature long time anneal for Dy_2O_3

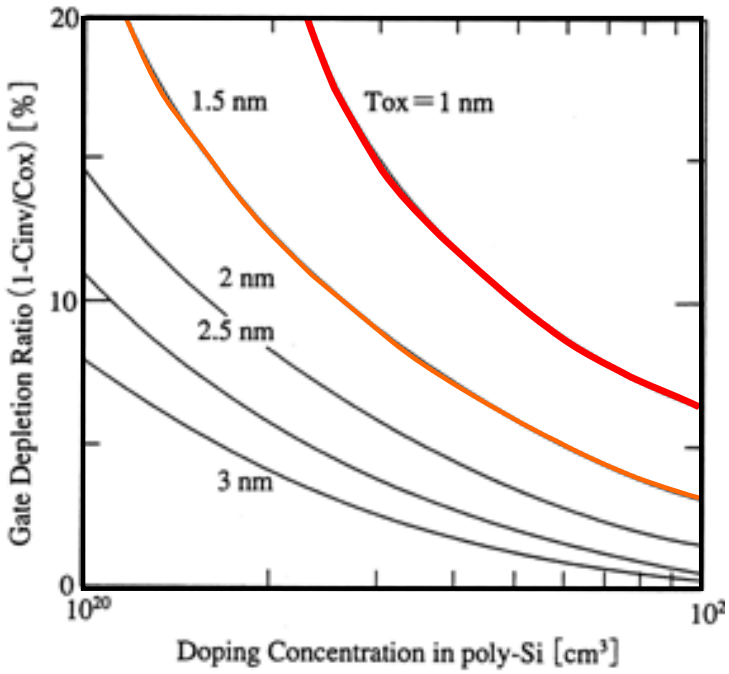


Figure 1.8 Acceleration of poly-depletion effect due to oxide thining

In this study, TaN is studied for gate electrode with thermal stability. Some excellent results were reported such as high thermal stability and interface properties during for TaN gate electrode at IEDM 2001 (Figure 1.9). These reports indicate TaN is promising material as gate electrode with thermally stable.

3. The effect of the low temperature long time anneal for Dy_2O_3

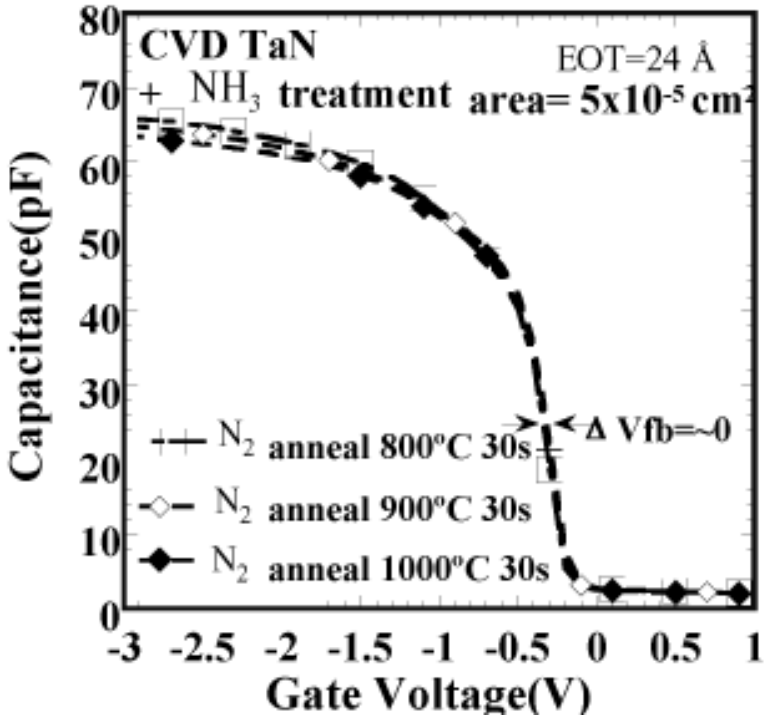


Figure 1.9 Excellent thermal stability for TaN/SiO_2 structure

1.5 Purpose of this study

Several High-k material such as HfO_2 and ZrO_2 have been studied and show excellent result. However, they are not the complete solution for High-k gate material because of some issues mentioned above. In this study, amorphous Dy_2O_3, which is one of the rare earth oxides, is studied for gate insulator application. Dy_2O_3 MIS capacitor has few reports and characteristics aren't well known. So, the purpose of this study is to investigate fundamental characteristics of Dy_2O_3 thin film, and improve the film quality with out crystallization and interfacial layer growth And in order to research the annealing effect after the metal deposition, the fabrication process of TaN electrode was researched for thermally stable gate metal.

3. The effect of the low temperature long time anneal for Dy_2O_3

Chapter 2

Fabrication and characterization methods

In this chapter, the fabrication and characterization methods of MIS diode were introduced briefly.

3. The effect of the low temperature long time anneal for Dy_2O_3

2.1 Fabrication methods and equipments

2.1.1 Cleaning procedure of Si substrate

Prior to use a bare Si substrate, it should be chemically cleaned to remove the particles as well as any traces of organic, ionic and metallic impurities from the surface. The procedure of cleaning of substrate in this study is shown in Table 2.1.

Table 2.1 Substrate cleaning procedure

Cleaning procedure	Removal object
1. Wash in DI water for 10 min 2. Immerse in (4:1) solution of H_2SO_4-H_2O_2 (SPM) for 5 min 3. Wash in DI water for 10 min	Organic, metal contamination
4. Immerse in (1:100) solution of HF-H_2O for 60 sec	Oxide layer

2.1.2 MBE system

Electron Beam Evaporation (EBE) method using MBD equipment is employed for depositing Dy_2O_3 in this study.

Figure 2.1 shows the schematic drawings of the equipment and inside of its growth chamber. Air in the loading chamber is removed to degree of a vacuum of 10^{-8} Torr by a turbo molecular pump connected to a rotary pump. Vacuum in the growth chamber reaches as high as 10^{-10} Torr by the removal of air with an ion pump and the introduction of liquid N_2 trap.

In the growth chamber, sintered Dy_2O_3 target, which is evaporation source, is irradiated with electron beam accelerated by -5 kV. The target is heated up and Dy_2O_3 molecules are evaporated. Then ultra thin Dy_2O_3 film is deposited on the Si-substrate. The degree of a vacuum is around 10^{-7} Torr while deposition. The substrate rotates 10 times per 1 minute horizontally to uniform the film thickness. Physical thickness of the film is monitored with a film thickness counter using crystal oscillator. The temperature of the substrate is controlled by a substrate heater and is measured by a thermocouple.

The significant features of this method are as follows:

1. Because the film is evaporated by using its own constituent as a raw material, contaminants, e.g. carbon, chloride, included in this method are much less than those in CVD (Chemical Vapor Deposition) which use precursor.
2. Damages caused by the depositing of this method are much less than those of sputtering.

3. The effect of the low temperature long time anneal for Dy_2O_3

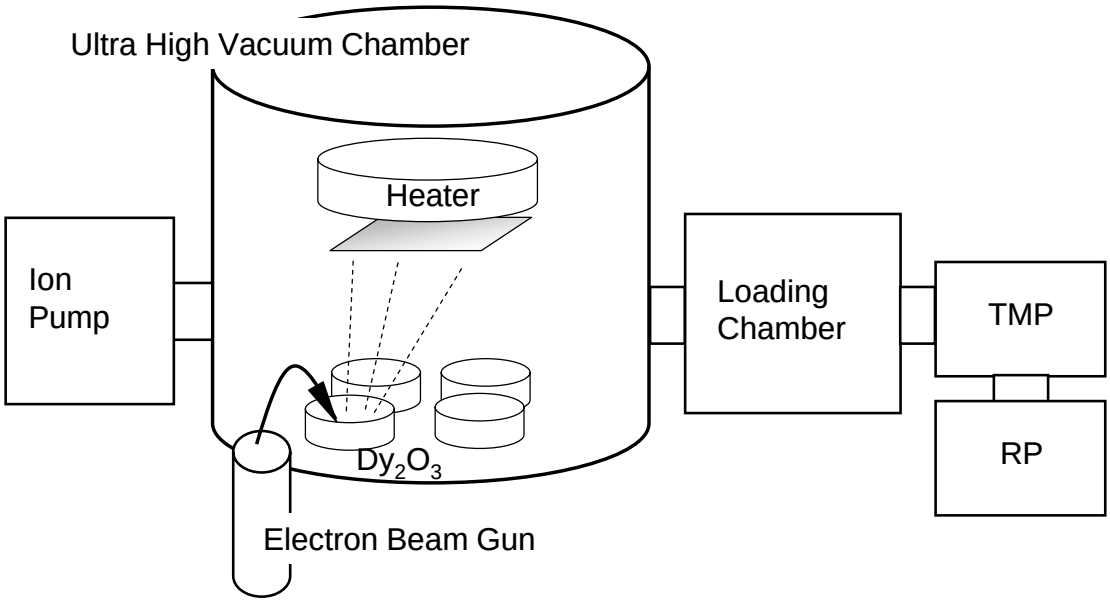


Figure 2.1 MBE system

2.1.3 RTA Rapid Thermal Anneal

RTA (Rapid Thermal Anneal) equipment (MILA-3000, ULVAC Co. Ltd.) was used for annealing sample of before/after metal gate deposition. The schematic diagram is shown in Figure 2.2. The temperature was controlled by PID controller. Before the anneal, the ambient of the furnace was replaced with O_2 or N_2 gas. The rate of temperature increase was set to 400 ^{o}C/min in this study.

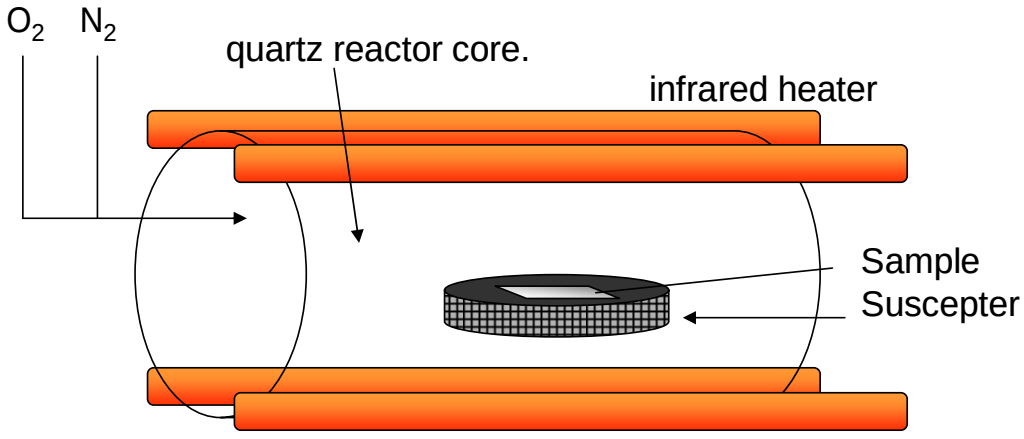


Figure 2.2 RTA equipment

2.1.4 Vacuum evaporation system

Top and bottom electrodes of Al were deposited by a vacuum evaporation equipment with a bell jar shown in Figure 2.3. In a vacuum of approximately 10^{-5} Torr, Al is

evaporated with resistance heating of W filament and Al film is deposited on samples.

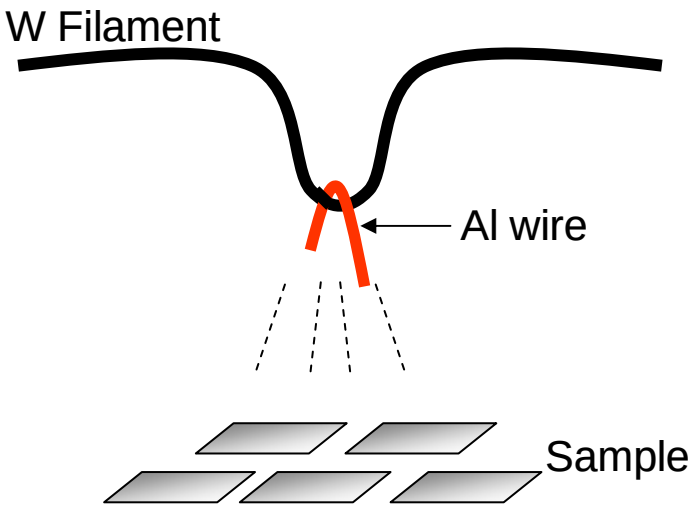


Figure 2.3 Vacuum evaporation of Al

2.1.5 RF magnetron sputtering system

TaN gate electrode was deposited by RF magnetron sputtering system (JEC-SP360R), schematic diagram of which was shown in Figure 2.4. This equipment deposits metal films by means of physical sputtering that occurs in a magnetically-confined RF plasma discharge of an inert Ar gas. Before the introduction of gases (Ar, Kr, N_2 or O_2), the process chamber was evacuated to degree of 10^{-5} Pa by a turbo molecular pump connected to a rotary pump and a liquid N_2 trap. The flow rate of gases is controlled by mass flow. The RF power supply system has auto impedance matching equipment and its capability of power supply is ~ 500W. In the process chamber, there is a substrate heater, which can heat samples from RT to 800 ^{o}C

3. The effect of the low temperature long time anneal for Dy_2O_3

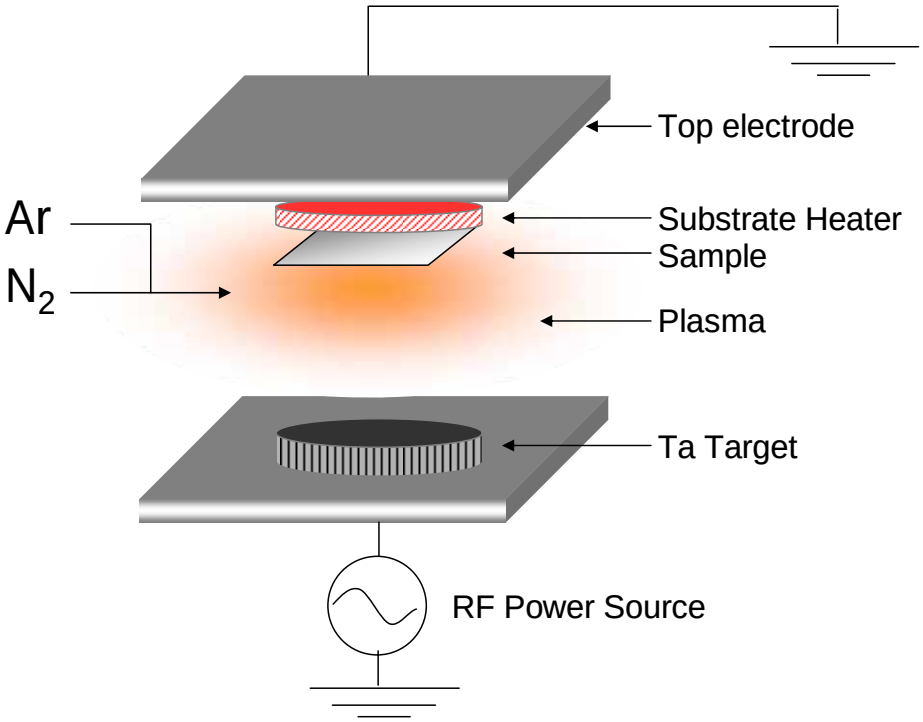


Figure 2.4 RF magnetron sputtering system

2.1.6 Mask aligner

The spin-coated photoresist was exposed through the mask with high-intensity ultraviolet light (405 nm). In this study, the exposure process was performed by contact-type mask aligner, MJB3 (Karl Suss Co. Ltd.). The exposure time was set to 12 sec. The photoresist was developed using the specified developer (MND-3, Tokyo Ohka Co. Ltd.).

2.1.7 RIE Reactive Ion Etching

RIE system was employed for etching TaN gate electrode. RIE combined the plasma and sputter etching process. Plasma systems are used to ionize reactive gases, and the ions are accelerated to bombard the surface. Etching process occurs though a combination of chemical reaction and momentum transfer from the etching species.

3. The effect of the low temperature long time anneal for Dy_2O_3

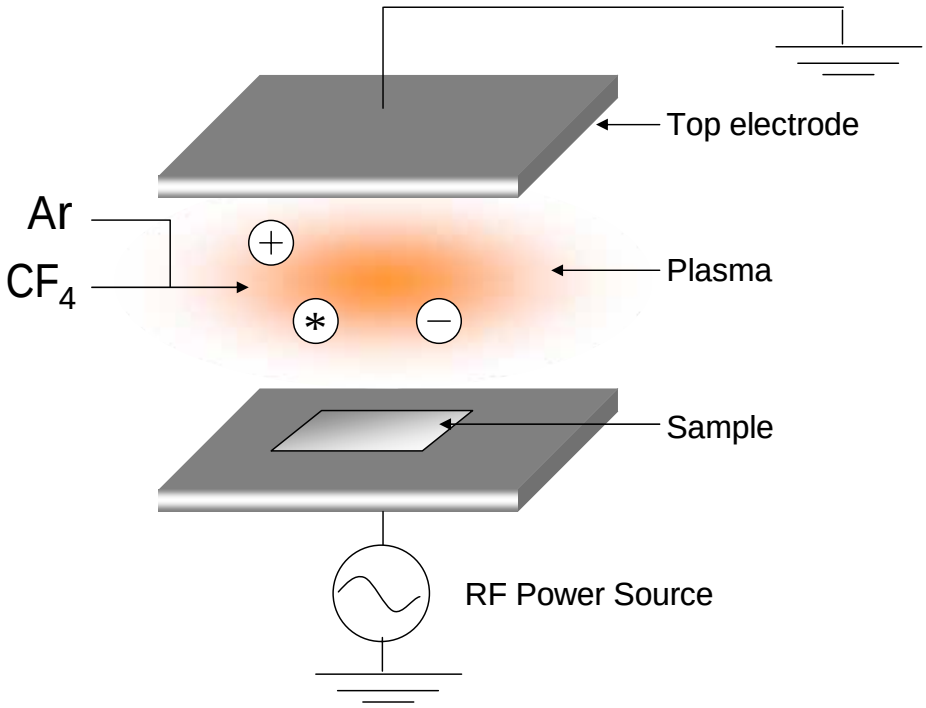


Figure 2.5 RF magnetron sputtering system

2.2 Characterization methods

2.2.1 C-V characteristics

C-V (Capacitance - Voltage) characteristics were measured by LCR meter (HP-4284C) with the measurement frequency range of 20Hz to 1MHz.

2.2.1.1 Ideal C-V curves

In order to analyze the experimental C-V characteristics, the comparison between ideal and experimental C-V is necessary. C-V curve is divided into three regime, inversion, depletion and accumulation. Capacitance of Si depends on the surface potential while the insulator capacitance is constant. So, in order to reach the ideal curves, the capacitance of Si should be calculated, which is expressed by following equation;

1) $U_S \geq 0$

$$C_S = C_D \hat{U}_S \frac{\sinh(U_S + U_F) + \sinh(-U_F)}{\left[e^{-U_F}(e^{-U_S} + U_S - 1) + e^{U_F}(e^{U_S} - U_S - 1)\right]^{\frac{1}{2}}} \quad (2\text{-}1)$$

2) $0 \geq U_S \geq 2U_F$

$$C_S = \mathrm{sgn}\{U_S\} C_D \frac{e^{\frac{U_F}{2}} \cdot \left\{e^{U_S} - 1\right\}}{2\left\{e^{-U_S} - U_S - 1\right\}^{\frac{1}{2}}} \quad (2\text{-}2)$$

3) $2U_F \geq U_S$

$$C_S = \frac{\varepsilon_S}{W_m} = \frac{C_D}{\int_0^{U_S} (e^{U(x)} - 1) \frac{dU(x)}{F\{U(x), U_F\}}} \quad (2\text{-}3)$$

$$F\{U_S, U_F\} \equiv \{\exp(-U_F)[\exp(-U_S) + U_S - 1] + \exp(U_F)[\exp(U_S) - U_S - 1]\}^{\frac{1}{2}} \quad (2\text{-}4)$$

U(x) and *Us* in above equation is follow,

$$U(x) \equiv \frac{q\phi(x)}{kT} \qquad \boldsymbol{U_s} \equiv \frac{\boldsymbol{q\phi_s}}{\boldsymbol{kT}}$$

and the capacitance of MIS diode can be calculated as formula (2-5),

$$\boldsymbol{C} = \frac{\boldsymbol{C_i C_s}}{\boldsymbol{C_i} + \boldsymbol{C_s}} \quad (2\text{-}5)$$

2.2.2 J-V characteristics

J-V (leakage Current – Voltage) characteristics were measured by semiconductor parameter analyzer (HP4284C, Agilent Technologies).

2.2.3 AFM Atomic Force Microscopy

The roughness of the surface of the film is evaluated by Atomic Force Microscope (AFM, Nano Scope III, Digital Instrument Co. Ltd.) in tapping mode.

AFM is a microscopic equipment for observing surface of a sample with high magnification. Figure 2.6 shows the principle of AFM. As the sample approaches the probe of AFM slowly and the distance between them becomes a certain value, attractive or repulsive force is generated between them. A cantilever to which the probe is attached distorts because of the force. The distortion is detected by a variation of reflection angle of laser beam which is irradiated to the cantilever. The distance is controlled to keep the distortion constant while scanning the surface of the sample with the probe. An image of the surface is obtained by the scanning in x and y directions and the control of the distance in z direction. Spatial resolution of AFM used in this study is around 1.0 nm.

3. The effect of the low temperature long time anneal for Dy_2O_3

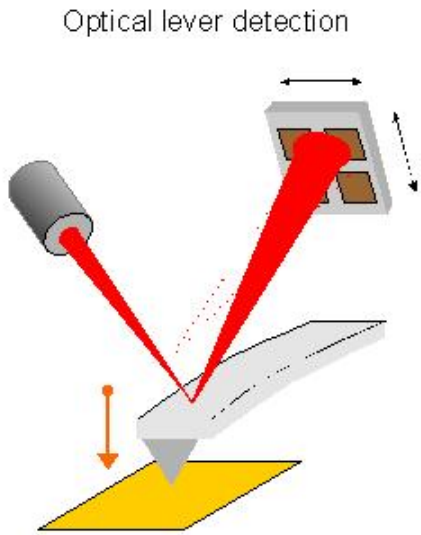


Figure 2.6 Atomic Force Microscopy

2.2.4 XPS X-ray photoelectron spectroscopy

Photoelectron spectroscopy is based upon a single photon in/electron out process and from many viewpoints this underlying process is a much simpler phenomenon than the Auger process.

The energy of a photon is given by the Einstein relation:

$$E = h\nu \tag{2.6}$$

where h-Plank's constant (6.62×10^{-34} Js), ν-frequency (Hz) of the radiation.

In XPS the photon is absorbed by an atom in a molecule or solid, leading to ionization and the emission of a core (inner shell) electron. The kinetic energy distribution of the emitted photoelectrons can be measured using any appropriate electron energy analyzer and a photoelectron spectrum can thus be recorded. The process of photo ionization can be considered in following equation:

$$A + h\nu \rightarrow A^+ + e^- \tag{2.7}$$

Conservation of energy then requires that:

$$E(A) + h\nu = E(A^+) + E(e^-) \tag{2.8}$$

Since the electron's energy is present solely as kinetic energy (KE), this can be rearranged to give the following expression for the KE of the photoelectron:

$$KE = h\nu - [E(A^+) - E(A)] \tag{2.9}$$

The final term in brackets, representing the different in energy between the ionized and neutral atoms, is generally called the binding energy (BE) of the electron – this then leads to the following commonly quoted equation:

$$KE = h\nu - BE \quad (2.10)$$

For each element, there is a characteristic binding energy associated with each core atomic orbital i.e. the presence of peaks at particular energies therefore indicates the presence of a specific element in the sample. Furthermore, the intensity of the peaks is related to the concentrations of the element. Thus, the technique is capable of yielding a quantitative analysis. And the binding energy depends not only on the level from photoemission is occurring, but also on the formal oxidation state of the atom and the local chemical and physical environment. They give rise to small shifts in peak positions in the spectrum. From the peak shifts, the binding condition of the elements was obtained.

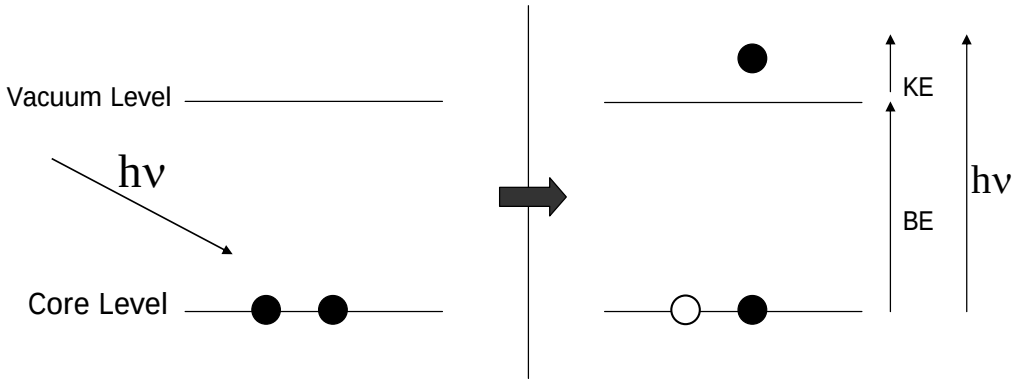


Figure 2.7 Schematic diagram of photo emission by X-ray

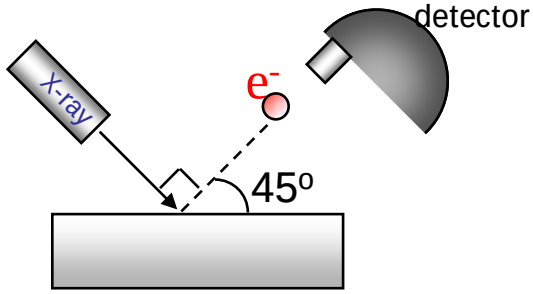


Figure 2.8 Schematic diagram of XPS System

2.2.5 RHEED

Reflection High Energy Electron Diffraction or RHEED is a surface sensitive technique which allows to qualitatively measure properties of the surface of a sample. This technique can also be carried out quantitatively to measure the in-plane surface lattice parameters and the in-plane coherence length of a sample.

In RHEED an electron beam has an incident angle of about one degree. Due to the

strong interaction of the electron beam and the electronic system of the sample the penetration depth is limited to a few Å.

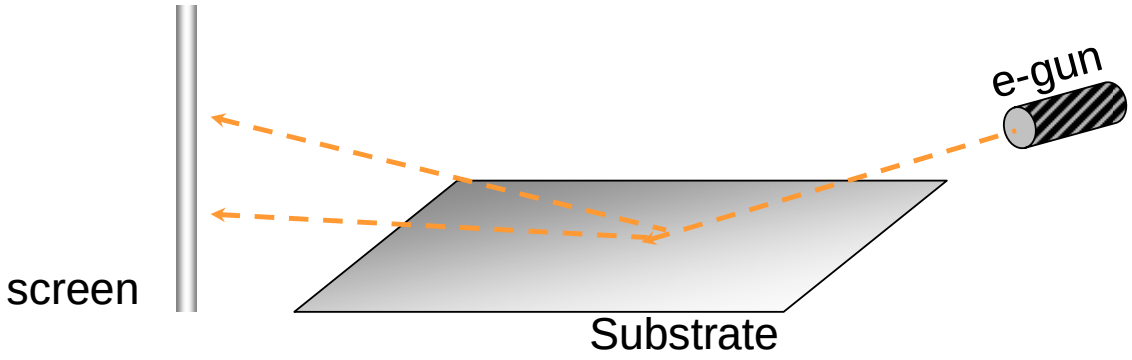


Figure 2.9 Principle of RHEED

2.2.6 TEM Transmission Electron Microscope

TEM (Transmission Electron Microscope) was used for observing cross sectional images of high-k/Si substrate interface in this study.

The electron high-energy beam of the order of 100 keV passes through the sample of less than 10 nm thickness. From transmitted electrons, a diffraction pattern or a high resolution image in atomic level can be obtained.

3. The effect of the low temperature long time anneal for Dy_2O_3

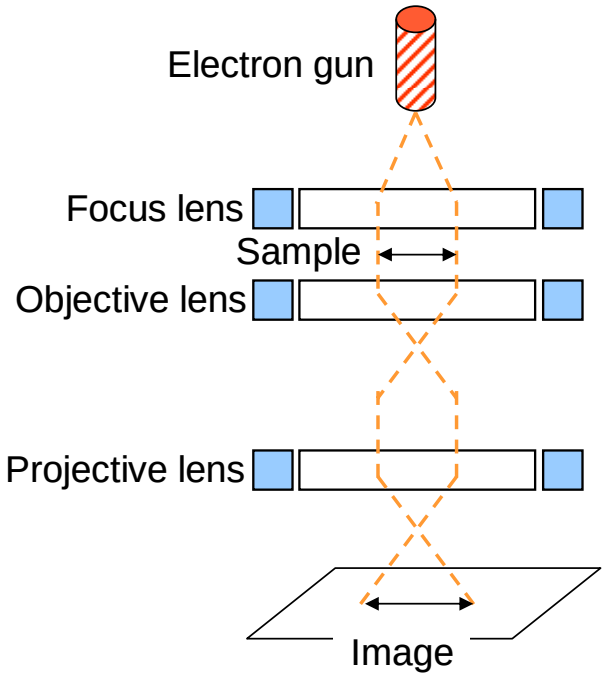


Figure 2.10 Principle of RHEED

2.2.7 XRD X-ray diffraction

Film crystallization was characterized by XRD. In principle XRD measurements come down to measuring distances between planes with plane x-ray waves (wavelength of a few tenths of a nm). When 2d equals $n\lambda = 2d \sin\theta$, the Bragg condition $n\lambda = 2d \sin\theta$ is satisfied and a peak can be measured.

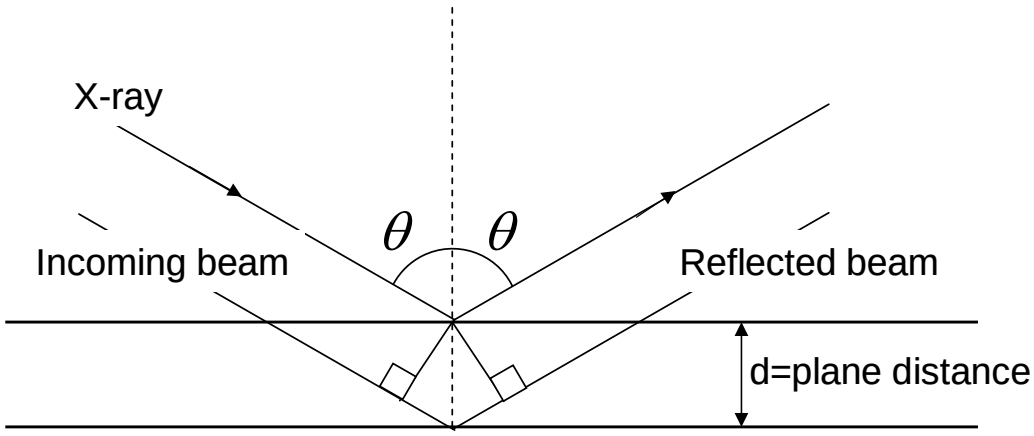


Figure 2.11 Principle of XRD

3. The effect of the low temperature long time anneal for Dy_2O_3

2.2.8 4 probe method

The resistivity of metal electrode was evaluated by 4 prove method. The schematic diagram was shown in Figure 2.12. A small current (I) is passed though two outer probes and voltage (V) is measured between the two inner probes. If the spacing between the probes is much greater than the film thickness but much smaller than the size of the conducting film, the resistance of the film can be obtained from following equation:

$$\rho = \frac{\pi}{\ln 2} t(\frac{V}{I}) \qquad (2.10)$$

where t -film thickness, V -outer probe voltage, I -inner probe current.

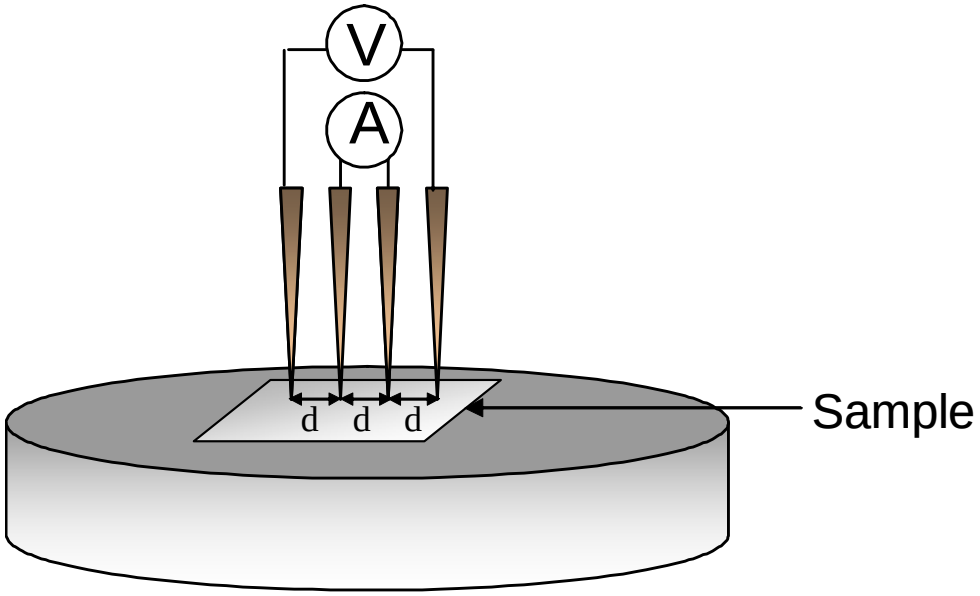


Figure 2.12 4 prove method

3. The effect of the low temperature long time anneal for Dy_2O_3

Chapter 3

The effect of the low temperature long time anneal for Dy_2O_3

In this chapter, fundamental electrical characteristics of MOS capacitors with a Al/Dy_2O_3/n-Si (100) structure were evaluated in advance. And the effects of the low temperature long time anneal and substrate preparation by H_2O_2 before the deposition

were researched.

3.1 Physical properties of Dy_2O_3

Dy is one of the rare earth elements, atomic number of which is 66. From its location in the periodic table, Dy belongs to heavy rare earth group. In this study, its oxide, Dy_2O_3 thin film was fabricated and evaluated.

Dy_2O_3 was deposited as amorphous thin film. However, it was crystallize in the case of the deposition on high temperature substrate. Its crystal systems are shown in Figure 3.1 and lattice constant of Dy_2O_3 is shown in Table 3.1.

Dy_2O_3 takes two types of crystal system, B type – monoclinic and C type – cubic. In the normal pressure, C-type structure is stable at various temperatures. On the other hand, B-type structure is stable in the high pressure. C-type crystal transit the phase into B type in the condition of $3.5x10^4$ atm, 1000 ^oC, and i.e. the density of these phase are $\rho_B > \rho_C$. And the transited phase on the high pressure condition re-transits to C type in a few hour in the normal pressure.

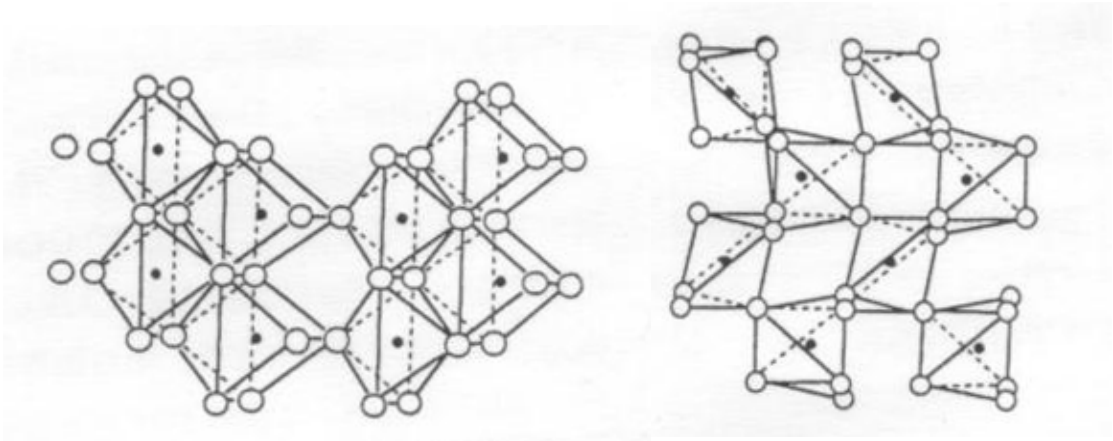


Figure 3.1 Crystal structure of Dy_2O_3 From top to bottom, B type and C type. Black point and small circles represents Dy and O, respectively.

3. The effect of the low temperature long time anneal for Dy_2O_3

Table 3.1 Lattice constant of Dy_2O_3

Structure system	a (nm)	b (nm)	c (nm)	β (degree)
Monoclinic (B type)	1.397	0.3519	0.8661	100.00
Cubic (C type)	1.0667			-

Table 3.2 shows the physical properties of various High-k materials. As to contact stability, Dy_2O_3 shows higher Gibbs free energy for the Si than the other High-k candidates listed in Table 3.2. As compared with the others, the suppression of the interfacial layer is expected for Dy_2O_3. With regard to bandgap, it is known as 4.8 eV, which is slightly less than the others, and dielectric constant is 12 – 18, which is almost the average value among the lanthanide oxide series.

Table 3.2 Physical properties for various High-k materials

	SiO_2	Al_2O_3	La_2O_3	HfO_2	ZrO_2	Dy_2O_3
Constant stability with Si (kJ/mol) $Si+MO_x \rightarrow M+SiO_2$	Stable	63.4	98.5	47.6	42.3	112.4
Lattice energy (kJ/mol)	-13125	-15926	-12452		-11188	-13514
Bandgap (eV)	8 - 9	8.8	5.4	5.7	5.2 - 7.8	4.8
Effective κ value	3.9	8.5 - 10	27	~24	11 - 18.5	12 - 18

3.2 Fabrication procedure of Al/Dy_2O_3/n-Si(100) structures

Fabrication process of MIS capacitor is shown in Figure 3.2. Dy_2O_3 films were deposited by electron beam evaporation in ultra high vacuum (UHV) chamber at room temperature or 250^oC on n-type Si(100) substrates treated by diluted HF (HF-last). Some of the samples were chemically oxidized by H_2O_2 dip to form 0.5nm SiO_2 layer

before the deposition of Dy_2O_3 films (Chemical Oxide). MBE system is used to deposit Dy_2O_3 thin film. The deposition rate of the film was about 0.7nm/min. The deposited samples were then annealed at 200°C - 1000°C for 5 - 90min in O_2 or N_2 ambient. Al electrode was deposited on the top of the oxide and Al back electrode was deposited on backside of n-Si (100) substrate. These MIS (Al/High-k/n-Si/Al) capacitors were characterized by C-V, J-V, AFM and XPS.

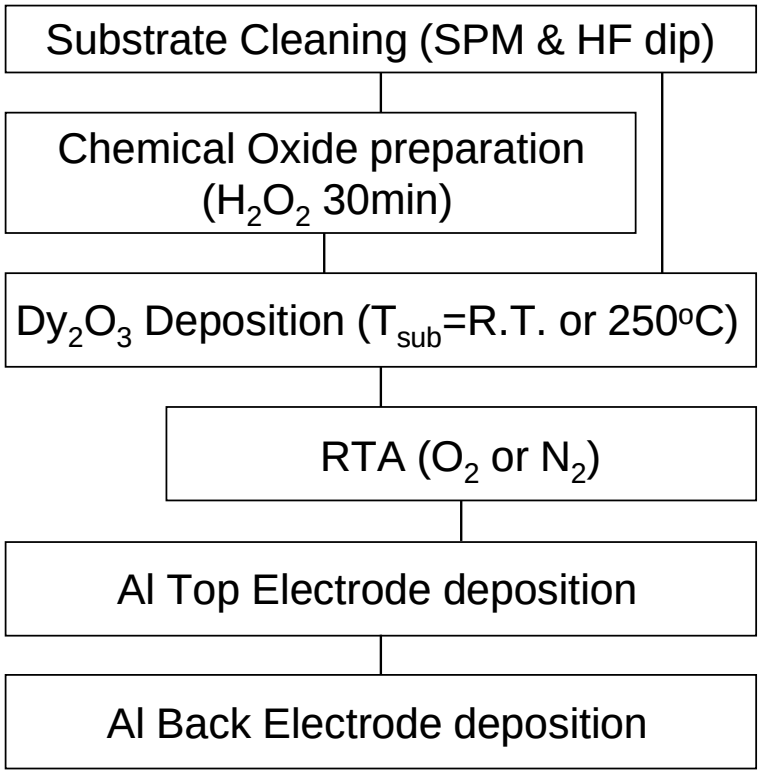


Figure 3.2 Fabrication procedure of MIS diode

3.3 Investigation on the low temperature long time anneal for Dy_2O_3

3.3.1 Annealing temperature dependence

Figures 3.3 – 3.6 show C-V characteristics of MIS capacitors for the HF last samples. The measurement frequency was 100 kHz. The film deposition temperature was room temperature or 250 °C, and the physical thickness of these films was about 5.5 nm for each temperature. The annealing temperature was 200°C – 1000°C. Annealing over 200°C, the hysteresis loop disappeared and the leakage current densities decreased (shown in Figures 3.7, 3.8). As annealing at higher temperature, the accumulation

capacitances decreased because of the formation of the interfacial layer growth.

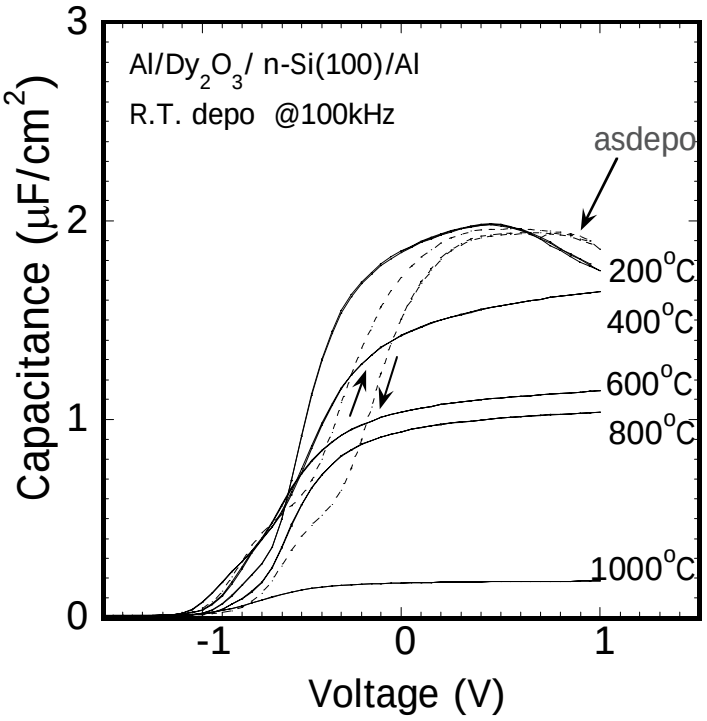
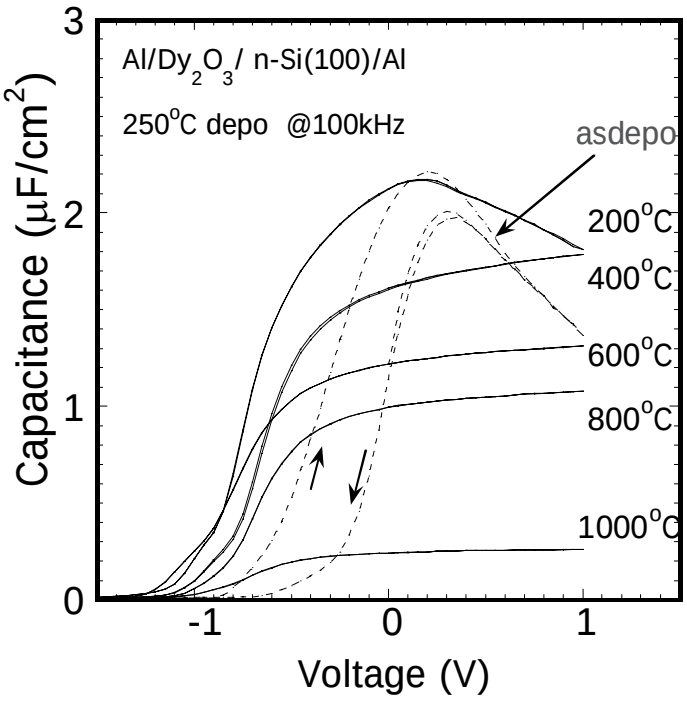


Figure 3.3 C-V characteristics for O_2 5min annealed samples deposited at RT



3. The effect of the low temperature long time anneal for Dy_2O_3

Figure 3.4 C-V characteristics for O_2 5min annealed samples deposited at 250 ^oC

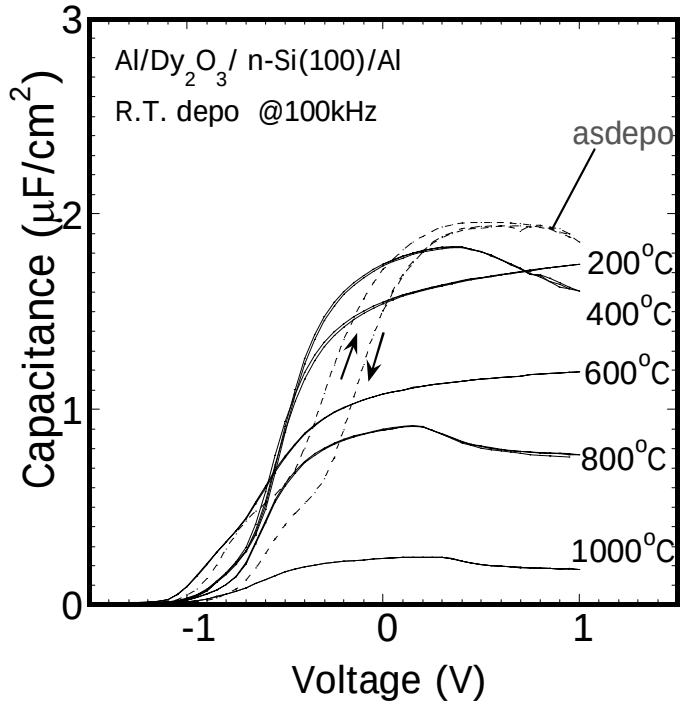
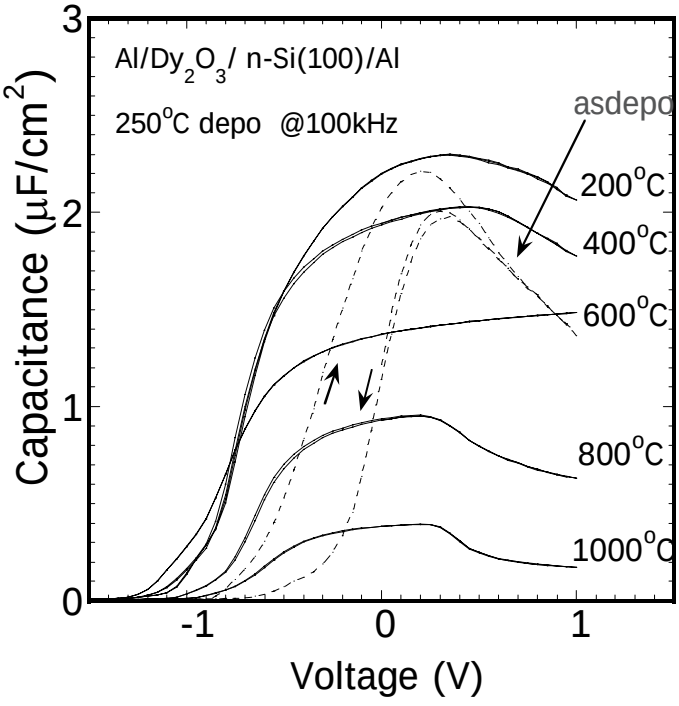


Figure 3.5 C-V characteristics for N_2 5min annealed samples deposited at RT



3. The effect of the low temperature long time anneal for Dy_2O_3

Figure 3.6 C-V characteristics for N_2 5min annealed samples deposited at 250 ^oC

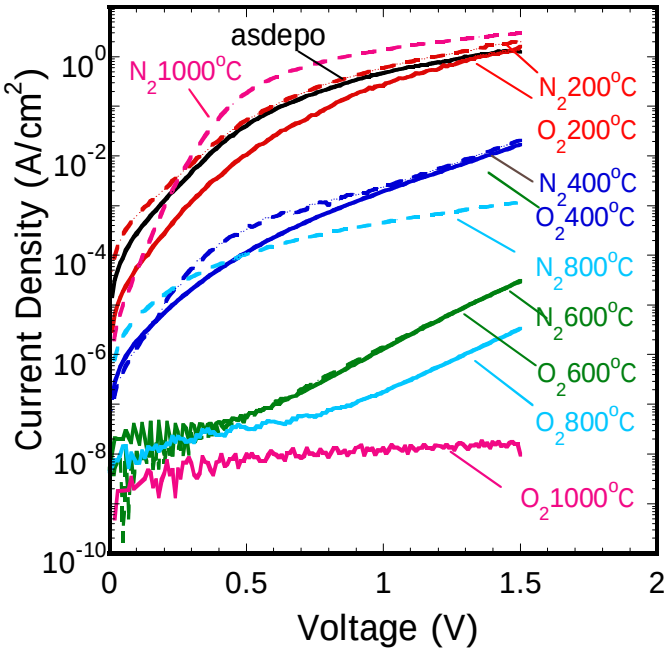


Figure 3.7 J-V characteristics for samples deposited at RT with annealing temperature and ambience as parameters solid: O_2 anneal, dotted; N_2 anneal

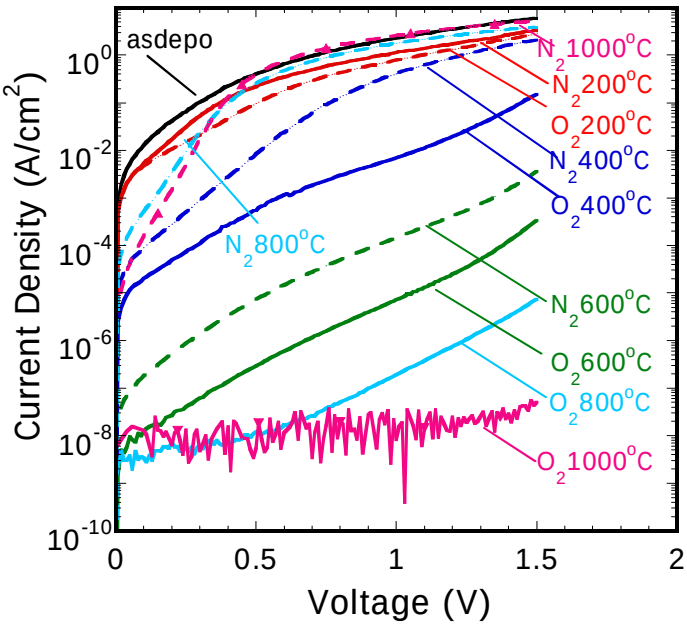


Figure 3.8 J-V characteristics for samples deposited at 250 ^oC with annealing temperature and ambience as parameters solid: O_2 anneal, dotted; N_2 anneal

3. The effect of the low temperature long time anneal for Dy_2O_3

Figure 3.9 shows the annealing temperature dependence of leakage current with annealing ambience and deposition temperature as parameters. In the case of O_2 annealing, the leakage current decreased with increase in annealing temperature. On the other hand, in the case of N_2 annealing, the leakage current densities start to increase above 600 ^oC. The leakage current for the sample annealed at 1000^oC was the same as that of as-deposited for each deposition temperature.

Figure 3.10 shows T_{ox} Electrical Equivalent dependence of current density (@Vg = +1V). With increase in T_{ox} Electrical Equivalent, the leakage current decreased in the case of O_2 annealing. However, N_2 annealing over 600 ^oC increased the leakage current in spite of the formation of interfacial layer. And deposition temperature dependence was not shown in this Figure. The characteristics of J - T_{ox} Electrical Equivalent are on the same fitting curve. However, the films deposited at 250 ^oC indicate the dependence of annealing ambience.

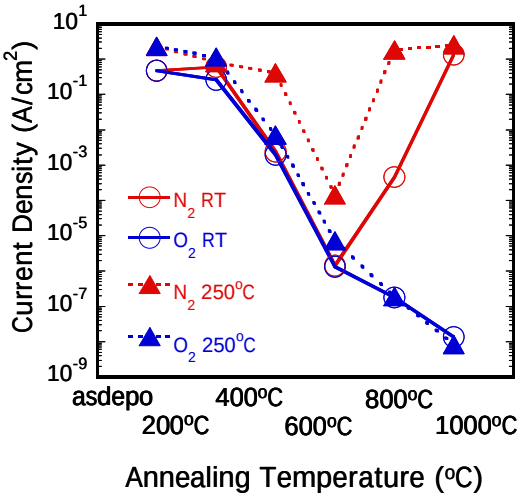


Figure 3.9 Annealing temperature dependence of leakage current densities with deposition temperature and annealing ambience as parameters

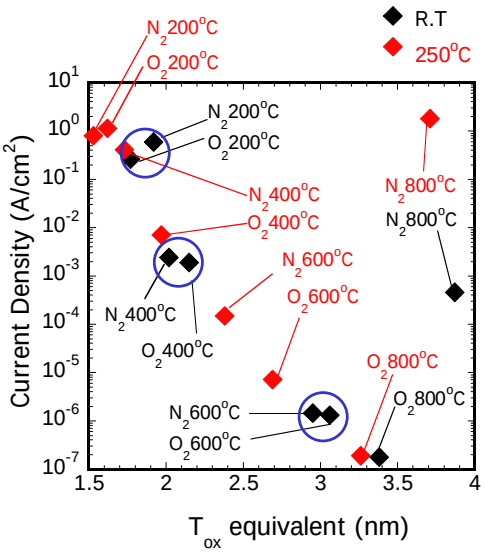


Figure 3.10 J- T_{ox} Electrical Equivalent characteristics

3. The effect of the low temperature long time anneal for Dy_2O_3

Figure 3.11 shows AFM images of the Dy_2O_3 films deposited at 250°C. The surface roughness of the films was very small (RMS: 0.2nm) for all of the samples except the cases of the 800 and 1000 °C N_2 anneals. The surface started to be rough with 800 °C N_2 anneal and became extremely rough with 1000 °C anneal (RMS: 1.0nm). On the other hand, the surface remained to be smooth in the case of O_2 anneal up to 1000°C. This suggests that the roughness is the cause of the large leakage current for high temperature N_2 anneal.

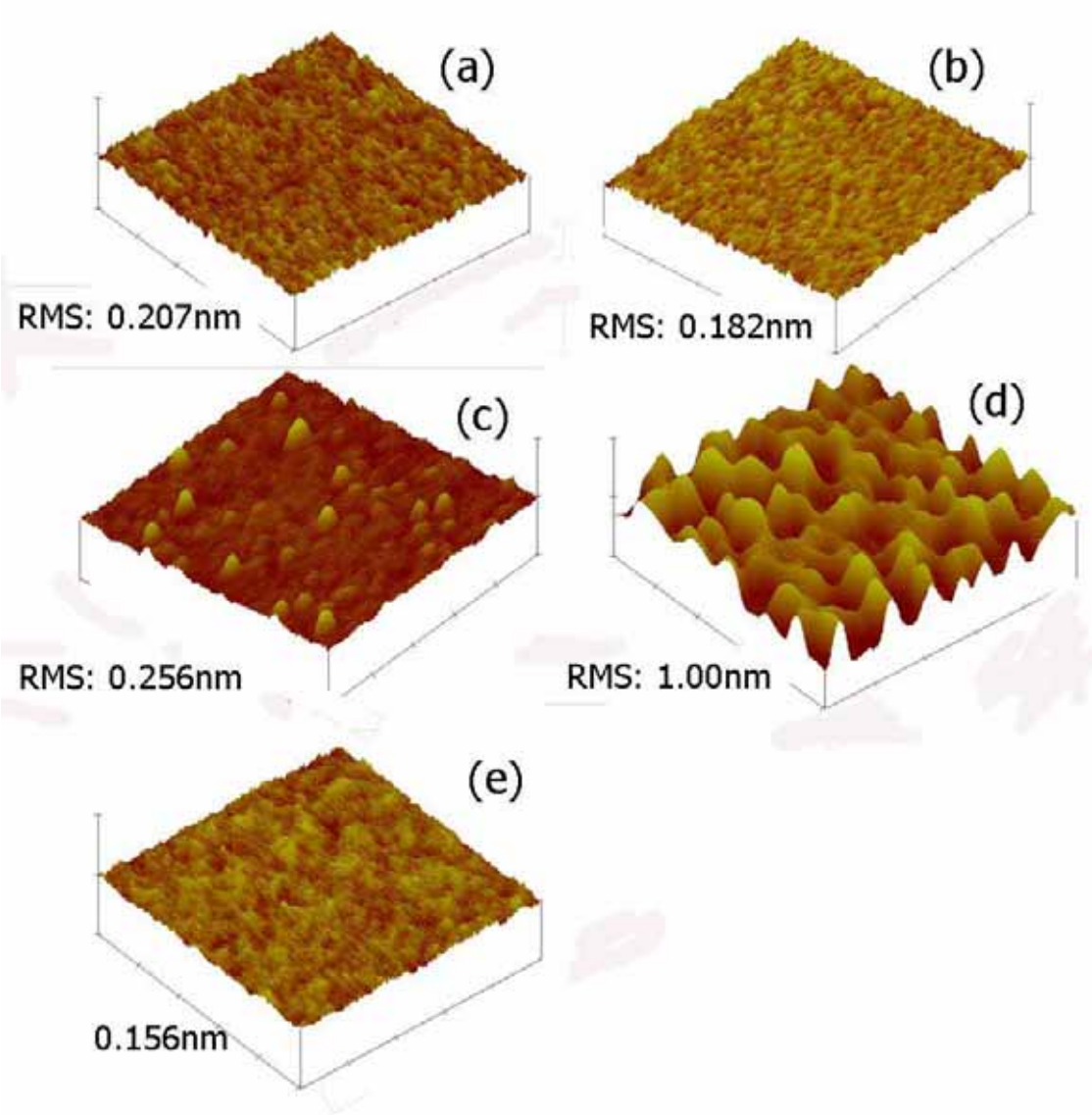


Figure 3.11 AFM images of films deposited at 250°C (0.5x0.5μm, 5nm/div) (a) as-deposited, (b) 400°C N_2 RTA, (c) 800°C N_2 RTA, (d) 1000°C N_2 RTA,

3. The effect of the low temperature long time anneal for Dy_2O_3

(e) 1000°C O_2 RTA.

3.3.2 Annealing time dependence

With increase in the annealing temperature, the leakage current decreased, but accumulation capacitance also decreased, because of the formation of the interfacial layer during high temperature anneal. In order to solve the problem, the effect of low temperature long time anneal (LLTA) for the Dy_2O_3 films have been studied.

Figures 3.12 and 3.13 show C-V and J-V characteristics of the 400°C O_2 annealed samples with annealing time as a parameter. The film deposition temperature was room temperature, and the physical thickness of these films was about 5.5nm. With increase in annealing time at 400°C, the leakage current density decreased significantly, while the accumulation capacitance decreased only slightly.

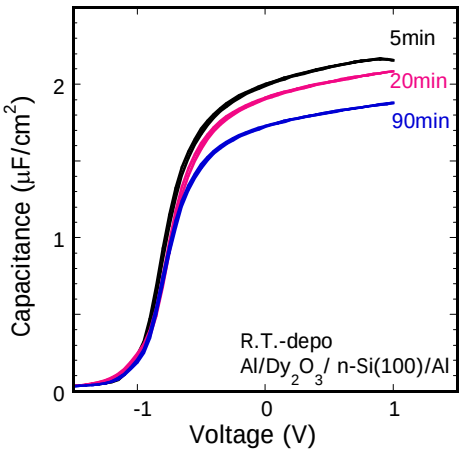


Figure 3.12 C-V characteristics for O_2 400 °C annealed samples with annealing time as a parameter (5 min, 20 min and 90 min)

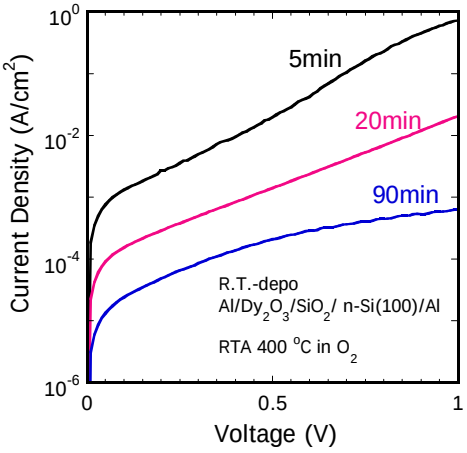


Figure 3.13 J-V characteristics for O_2 400 °C annealed samples with annealing time as a parameter (5 min, 20 min and 90 min)

3. The effect of the low temperature long time anneal for Dy_2O_3

Figure 3.14 shows annealing time dependences of leakage current and T_{ox} Electrical Equivalent. 90min 400°C O_2 anneal decreased the leakage current about 3 orders magnitude from that of the 5min annealed sample, while EOT of the film increased only 0.2nm.

Figure 3.15 shows T_{ox} Electrical Equivalent dependence of current density (@Vg = +1V). T_{ox} Electrical Equivalent of the sample for 400°C 90min anneal film was 0.2nm smaller than that of annealed at 600°C for 5min, which was almost the same leakage current @ Vg = +1 V.

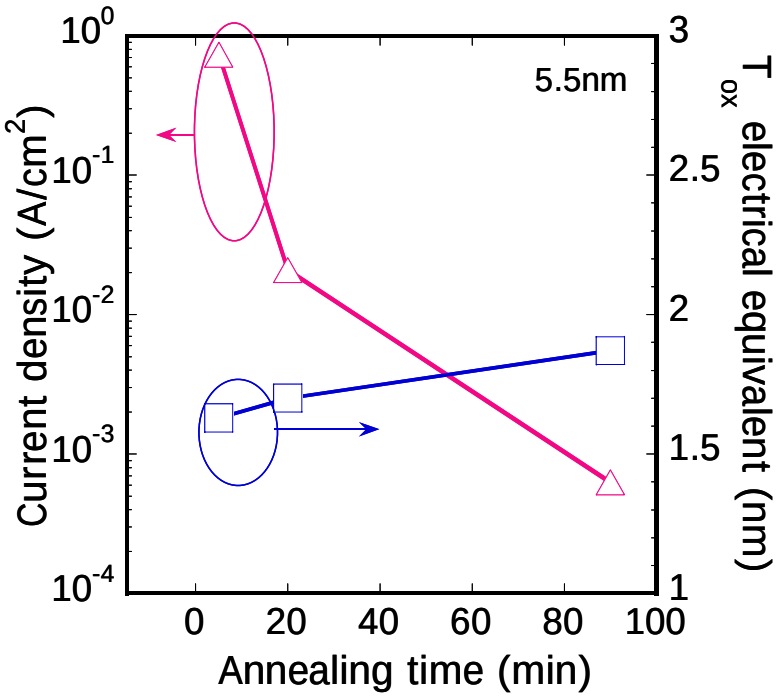


Figure 3.14 Annealing time dependences of Current density and T_{ox} Electrical Equivalent for O_2 400 °C annealed samples

3. The effect of the low temperature long time anneal for Dy_2O_3

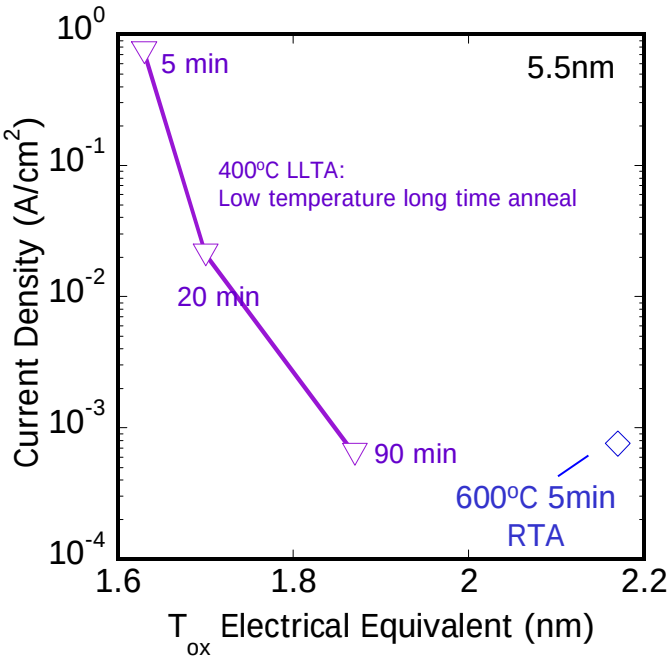


Figure 3.15 J - T_{ox} Electrical Equivalent characteristics for several annealing conditions

XPS spectra of the Si_{2p} for the HF last samples with different anneal conditions are shown in Figure 3.16. Here, physical thickness of the deposited Dy_2O_3 film was set thinner to be 2.9nm, for obtaining higher resolution of the interfacial layer. The films were deposited at R.T. In the case of 5.5 nm thickness, the sample annealed at 600 ^oC for 5min shows almost the same leakage current density at V_g = +1V as that of the sample annealed at 400^oC for 90min. EOT of the sample for 400 ^oC 90 min anneal film was 0.2nm smaller than that of annealed at 600 ^oC for 5min as shown in Figure 3.15. The peak intensity of Si-O for 400 ^oC 90min anneal increased slightly as compared with 400 ^oC 5min anneal. However, in the case of 600 ^oC 5min anneal, the intensity became much larger. This fact indicates formation of thicker interfacial layer by annealing at 600 ^oC.

3. The effect of the low temperature long time anneal for Dy_2O_3

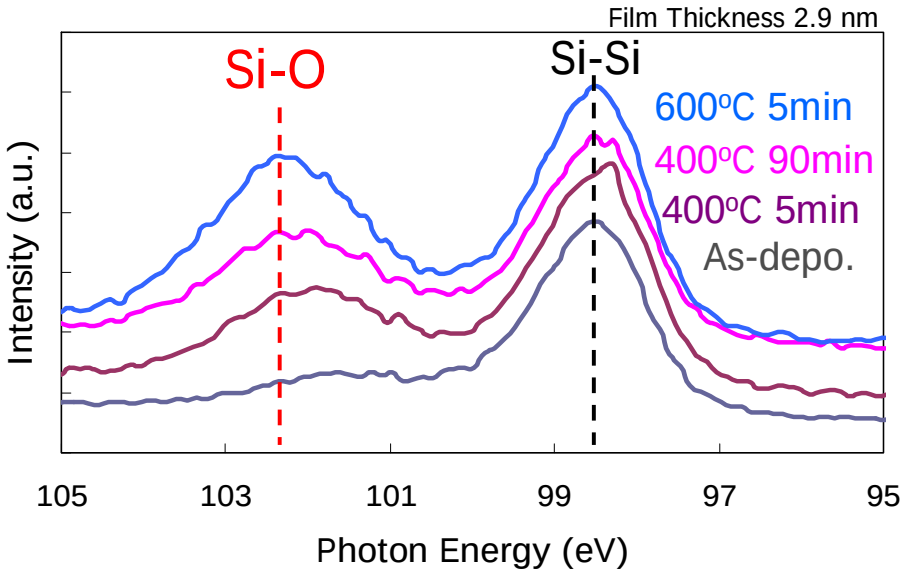
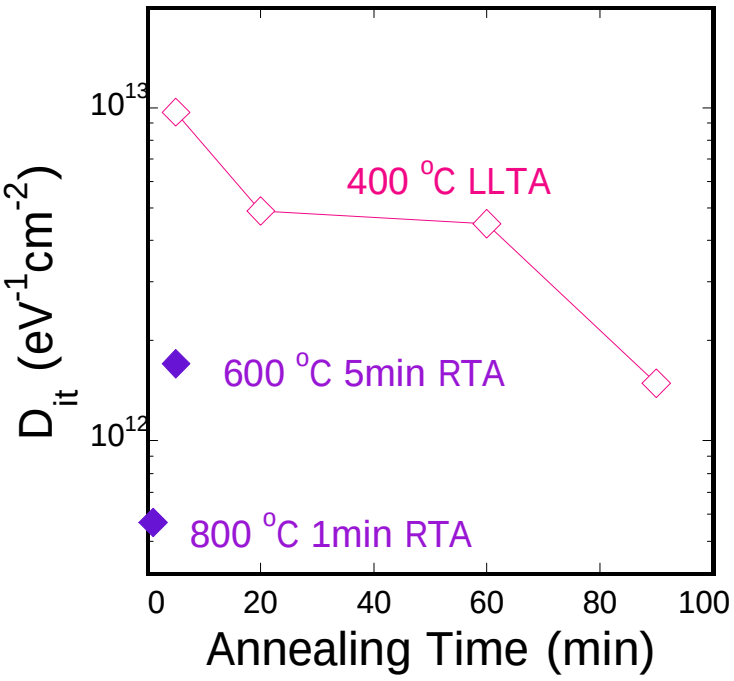


Figure 3.16 XPS spectra of Si 2p in the as-deposited and annealed Dy2O3 film

Figure 3.17 shows the 400 °C annealing time dependence of interfacial state densities (D_{it}). To determine interfacial state densities, Terman method was performed. With increase in the annealing time, D_{it} was improved. D_{it} was also improved by annealing at high temperature, especially at 800°C RTA.



3. The effect of the low temperature long time anneal for Dy_2O_3

Figure 3.18 Change of interface state density for Dy_2O_3/n-Si(100)

3.3.3 The effect of chemical oxide preparation

Figure 3.18 shows the C-V characteristics for the samples with and without chemical oxide preparation before the deposition, respectively. The Dy_2O_3 film was deposited at room temperature and that of thickness was about 5.5 nm. As for as-deposited samples, chemical oxide preparation suppresses the hysteresis width as compared with HF-last sample. And annealing over 400 ^oC, the accumulation capacitances of chemical oxide samples were almost the same as that of HF last samples in spite of existence of 0.5 nm SiO_x layer by H_2O_2 oxidation.

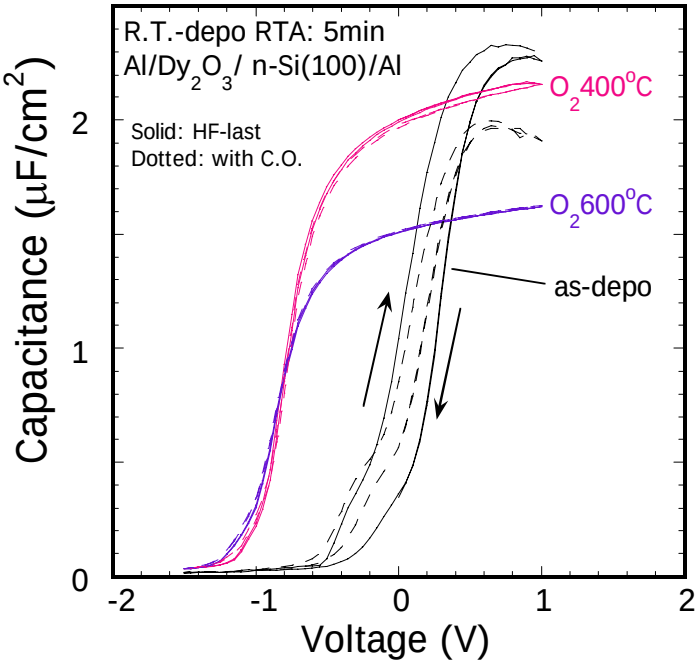


Figure 3.18 C-V characteristics for HF-last and chemical oxide prepared samples with annealing temperature as a parameter

3. The effect of the low temperature long time anneal for Dy_2O_3

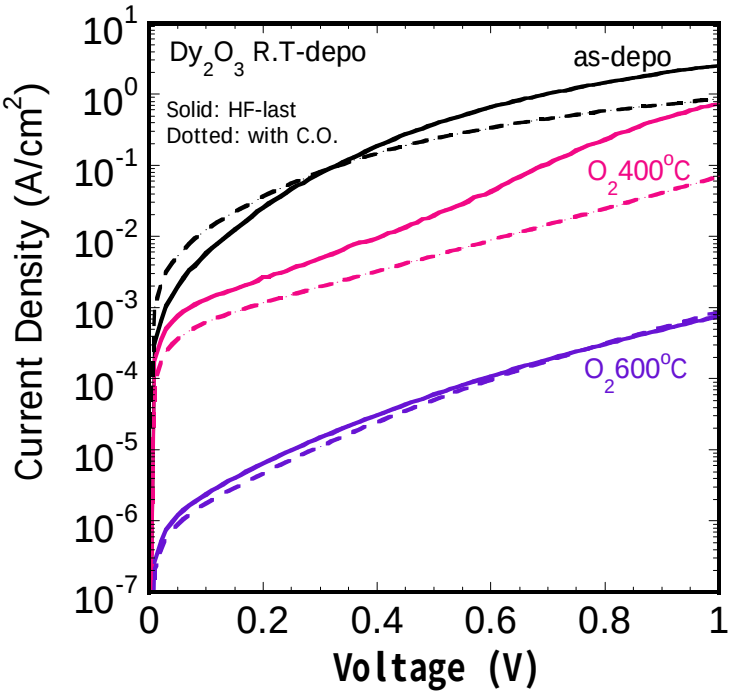


Figure 3.19 J-V characteristics for HF-last and chemical oxide prepared samples with annealing temperature as a parameter

Figure 3.19 shows the J-V characteristics for the samples with and without chemical oxide preparation before the deposition, respectively. Chemical oxide preparation decreased the leakage current about a half order of magnitude up to 400 ^{o}C as compared with HF last samples. However, there was no difference between HF-last and chemical oxide samples annealed at 600^{o}C.

3. The effect of the low temperature long time anneal for Dy_2O_3

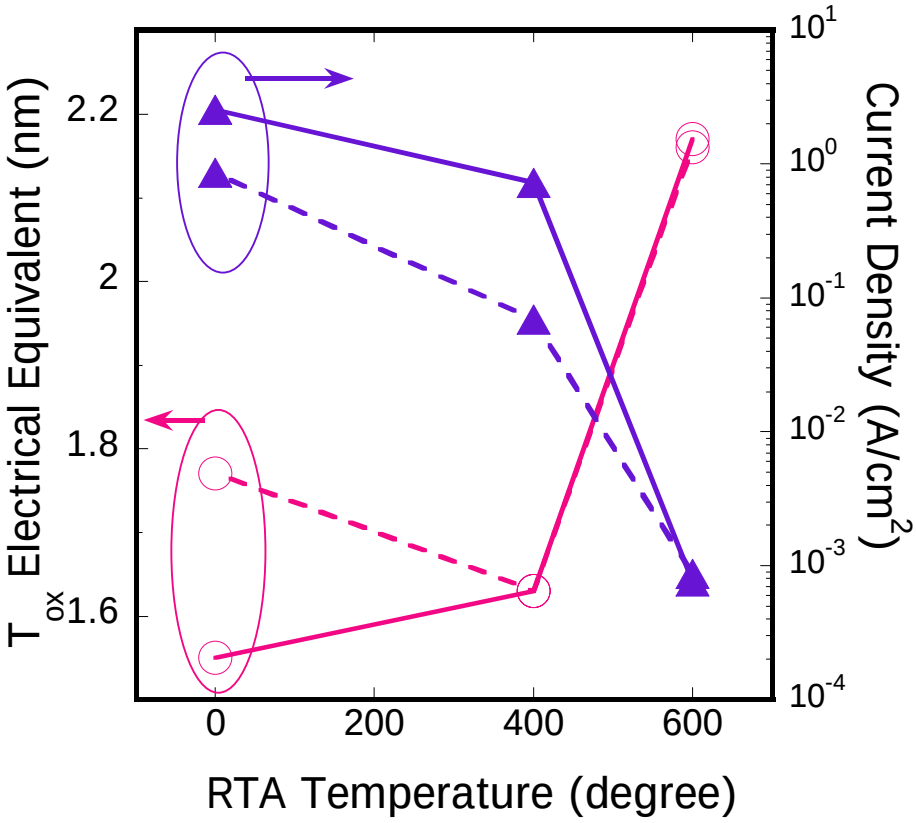


Figure 3.20 Annealing temperature dependence of T_{ox} Electrical Equivalent and Current density @ V_G = +1 V

Figure 3.21 shows J - T_{eq} characteristics of LLTA with and without chemical oxide. From this graph, the chemical oxide sample associated with LLTA shows further improvement of J – T_{eq} characteristic. Therefore, 400 ^oC LLTA is effective to apply the merit of chemical oxide preparation.

3. The effect of the low temperature long time anneal for Dy_2O_3

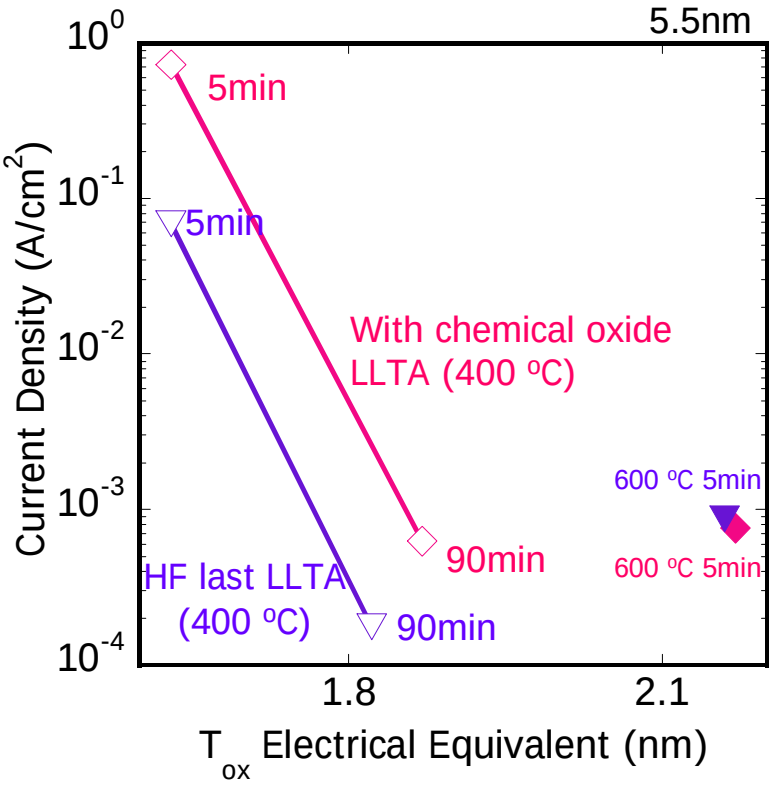


Figure 3.21 J - T_{ox} Electrical Equivalent characteristics for samples with and without chemical oxide

3.4 Summary of this chapter

As to annealing ambience, in the case of above 800 °C, N_2 annealed sample shows high leakage current. AFM images suggest that surface roughness was one of the causes for the high leakage current.

In regards in annealing time dependence, 400 °C 90 min annealed sample decrease the leakage current with slight decrease of accumulation capacitance as compared with high temperature anneal. From XPS result, it was found that 600 °C 5min anneal accelerated the formation of interfacial layer as compared with LLTA with 400 °C.

For the effect of the chemical oxide preparation, it was effective to reduce the leakage current by half order of magnitude up to 400 °C RTA. However, after 600 °C RTA, the reduction was not obtained as compared with HF-last sample. So, LLTA could make good use of substrate preparation before the deposition.

These results were promising, however, the accumulation capacitance was degraded for certain after anneal even though 400 °C LLTA. It seems to be due to O_2 penetration to interface between Dy_2O_3 and substrate.

3. The effect of the low temperature long time anneal for Dy_2O_3

Chapter 4

Fabrication and characterization of TaN for gate electrode application

If oxide films were annealed in oxygen, the interfacial layer growth could not be suppressed, over 400 ^oC annealing. Therefore, in order to solve this problem, the films were annealed after the gate metal deposition. In this chapter, fabrication process of TaN, thermally stable metal electrode, was researched.

3. The effect of the low temperature long time anneal for Dy_2O_3

4.1 Physical properties of TaN

Tantalum nitride is a hard material, chemically inert, corrosion resistant, and has good shock- and heat-resistant properties. These properties make this material attractive for many industrial applications. In the silicon technology, TaN have been used as diffusion barriers in copper metallization against interaction between Cu and the underlying substrates, and it have been recognized as excellent barriers for the prevention of Cu-diffusion. And recently TaN is attracted as CMOS gate electrode for the next generation.

As mentioned above, TaN shows good thermal stability and work function of 4.1 eV, which is suitable for NMOS electrode. However, the work function depends on the N content and deposition method as shown in Table 4.1.

Crystal systems of TaN and its lattice constant are shown in Table 4.2. TaN takes many systems depending on N contents.

Table 4.1 Work function of reported gate metal

n-MOS

Material	**Ta**	**Hf** [1)]	**Zr** [1)]	**TaN (PVD)** [3)]
Work Function(eV)	**4.2**	**4.0**	**4.0**	**4.15**

p-MOS

Material	**TaN (CVD)** [3)]	**$TiAlN_y$ (y~1)**	**Ta_xRu_y** [2)]	**RuO_2**
Work Function(eV)	**5.0**	**5.1**	**4.2~5.1**	**5.1**

Table 4.2 Structure type of TaN_x

	Structure	Space group	Lattice constants (nm)
α-Ta	Cubic	Im3m	a = 0.3306
β-Ta	Tetragonal	$P4_2/mnm$	a = 1.019, c = 0.531
TaN	Cubic	Im3m	a = 0.337
Ta_4N	Orthorhombic	C	A = 0.516, b = 0.311, c = 0.494
Ta_2N	Hexagonal	$P6_3/mmc$	a = 0.3044, c = 0.4914
TaN	Cubic	Fm3m	a = 0.433
TaN	Hexagonal	P6/mmm	a = 0.519, c = 0.2908

3. The effect of the low temperature long time anneal for Dy_2O_3

Table 4.3 shows resistivity of TaN_x. As increase in N content, the resistivity increases from 250 of $TaN_{0.60}$ to 2700 μW-cm of $TaN_{1.41}$.

Table 4.3 Resistivity of TaN_x

Ta/N ratio	Resistivity (μΩ-cm)
Ta	191
$TaN_{0.60}$	250
$TaN_{1.07}$	330
$TaN_{1.35}$	910
$TaN_{1.41}$	2700

4.2 Experimental procedure

In this chapter, sputtering condition during fabrication and heat stability test were studied. TaN was deposited on 5 nm SiO_2/Si substrate by RF magnetron sputtering system. Then, samples were annealed as post metallization anneal (PMA) for ~ 800^oC. These samples were characterized by 4-prove method, XRD, XPS AFM and SIMS.

4.3 Characterization

4.3.1 RF power dependence

Figure 4.1 shows RF power dependence of resistivity. In the case of RF power of 70 W, the resistivity is too high (~0.1 Ωcm). As RF power increased, resistivity was improved, however. The sample, which was deposited at 180 W of RF power, exhibited resistivity of 470 μΩ-cm. It is considered that reaction energy is important to formation of TaN film by reactive sputtering.

Figure 4.2 shows XPS spectra for the samples of w/o PMA with RF power as a parameter. This result indicates that reduction of resistivity was not due to the N_2 contents because all the spectra show almost same peak intensity ratio of N 1s and Ta 4p.

Figure 4.3 shows XRD patterns for the samples of different RF power, 100 W, 180 W. As compared with 100 W, the increase of peak intensity was obtained. This fact indicates the crystallization was accelerated by higher RF power. So, it seems that the

reduction of resistivity is due to the crystallization from this result.

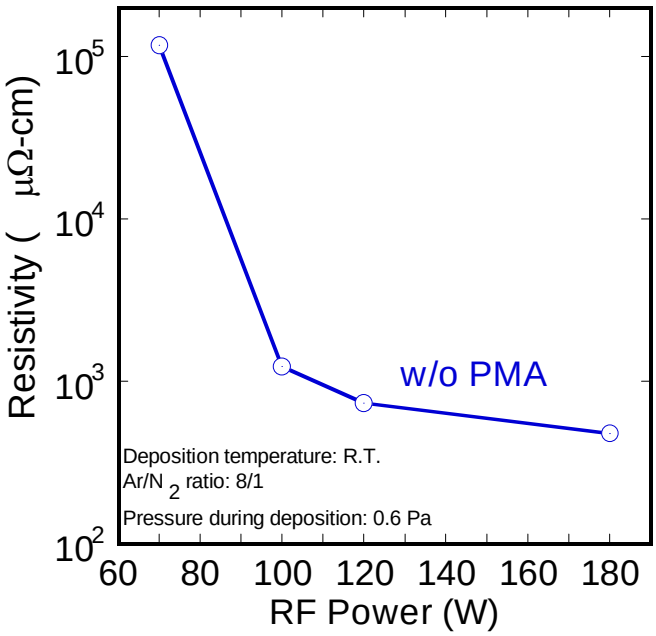


Figure 4.1 RF power dependence of Resistivity for the sample of w/o PMA

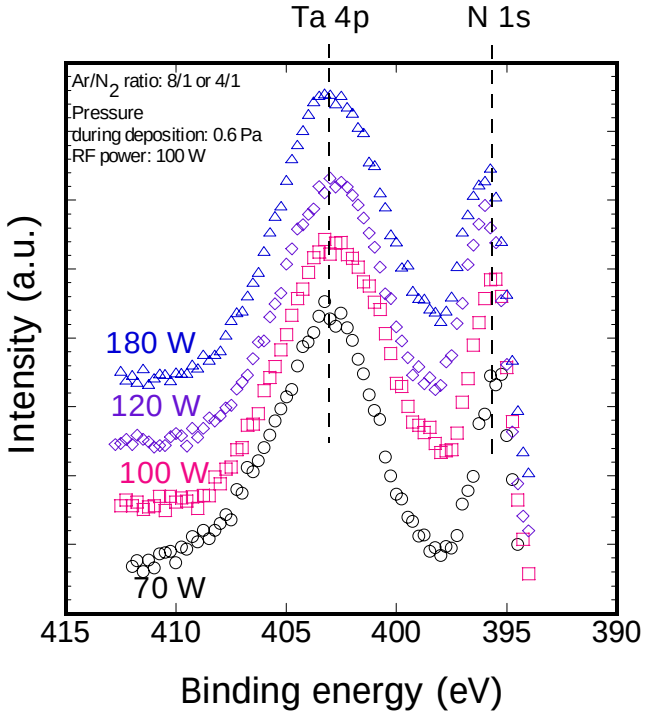


Figure 4.2 XPS spectra for the sample of w/o PMA with RF power as a parameter

3. The effect of the low temperature long time anneal for Dy_2O_3

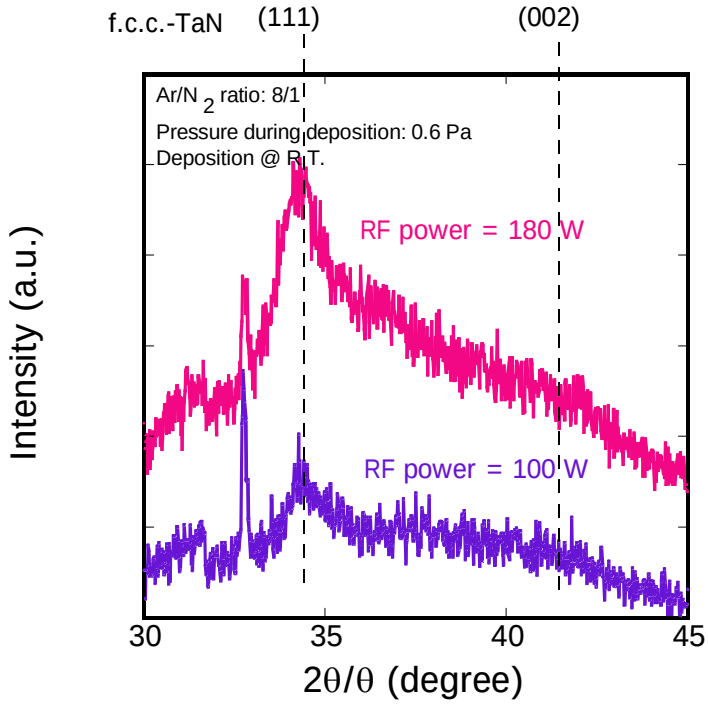


Figure 4.3 XRD patterns for the samples of different RF power

4.3.2 N_2 ratio dependence

In order to vary the N content, TaN was deposited at several Ar/N_2 ratios of sputtering ambience. RF power dependence of resistivity with Ar/N_2 ratio as a parameter was shown in Figures 4.4. As increase in N_2 ratio, resistivity was increased about a quarter order of magnitude in the case of 100 W.

From SIMS result, N content of sample for Ar/N_2 = 4/1 increased by 20 % as compared with 8/1 sample. The increase of resistivity was due to the increase of N content in TaN film.

XRD patterns for the samples of different Ar/N_2 ratio during sputtering were shown in Figure 4.5. In the case of Ar/N_2 = 4/1, the peak intensity of (100) grew as compared with 8/1 sample. From this result, it was found that the crystallization was accelerated at the ambience of Ar/N_2 = 4/1.

3. The effect of the low temperature long time anneal for Dy_2O_3

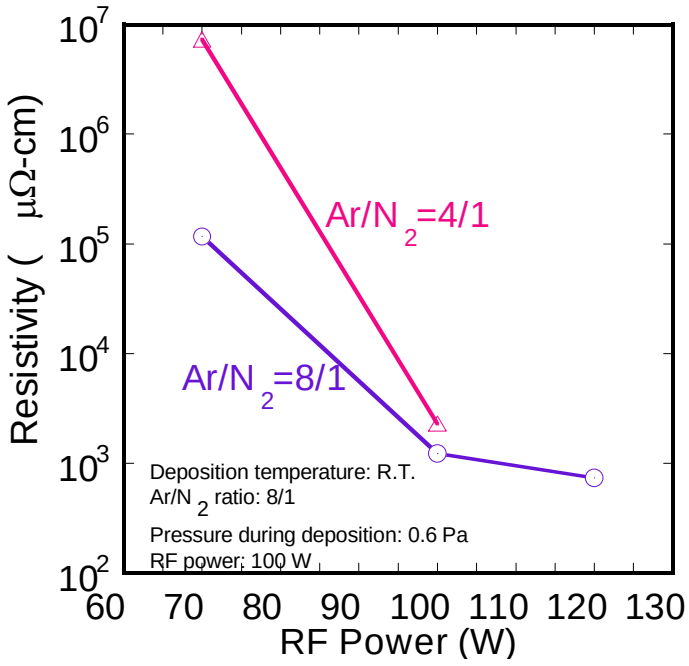


Figure 4.4 RF power dependence of Resistivity for the sample of w/o PMA with N_2 ratio as a parameter

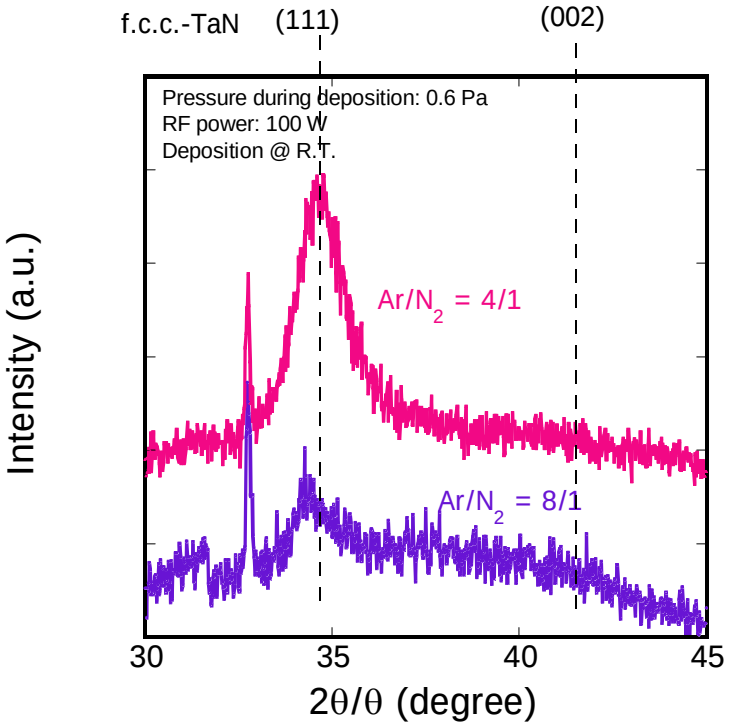


Figure 4.5 XRD patterns for the samples of different Ar/N_2 ratio during sputtering

3. The effect of the low temperature long time anneal for Dy_2O_3

4.3.3 Deposition temperature dependence

In order to deposit film with crystallization, deposition temperature dependence was researched. A crystal film is thought to show lower resistivity as compared to amorphous. Therefore, TaN depositions were carried out at R.T., 200°C and 400°C.

Figure 4.6 shows deposition temperature dependence of resistivity of w/o PMA sample. As increase in deposition temperature, resistivity was increased for all the case. XRD (Figure 4.7) result indicates no difference between RT deposition and 400°C deposition as to crystallization. So, the increase of deposition temperature is not so dominant to the crystallization in this case. To make matters worse, the resistivity of 400°C deposition sample exhibited the increase as compared with R.T. deposited sample for each RF Power. Deposition temperature dependence of background pressure was also shown in Figure 4.6. From this result, the pressure did not vary up to 200°C, however, swelled about a order of magnitude at 400°C. Therefore, the increase of resistivity at 400°C was caused in the degradation of background pressure.

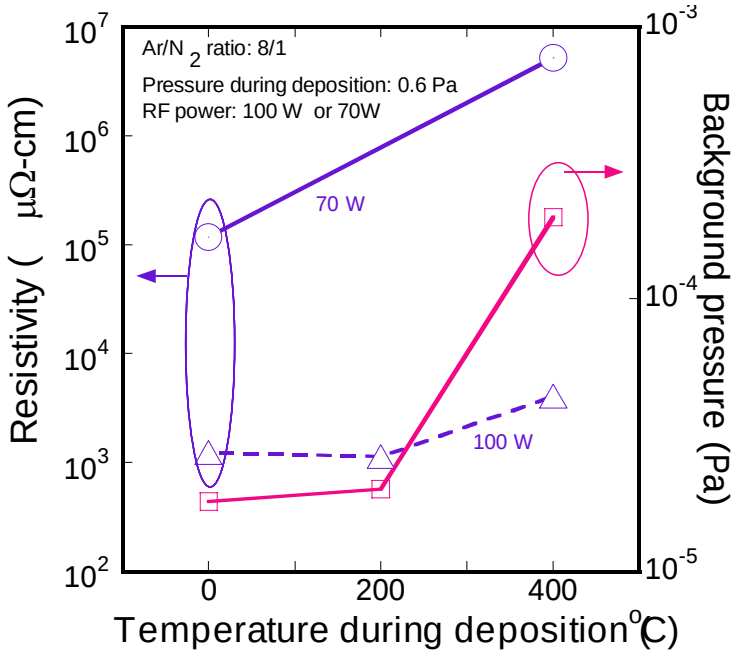


Figure 4.6 Deposition temperature dependence for the samples of w/o PMA with RF power as a parameter

3. The effect of the low temperature long time anneal for Dy_2O_3

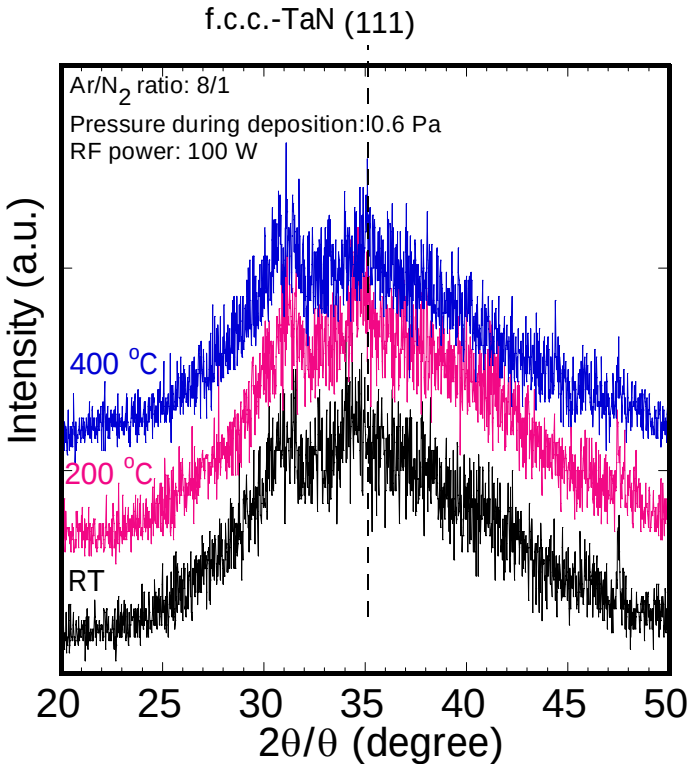


Figure 4.7 XRD patterns for the samples of deposited at R.T., deposited at 250°C

4.3.4 Thermal stability of TaN

Figures 4.8 and 4.9 show PMA temperature dependence of resistivity with RF power and Ar/N_2 ratio as parameters. After 800°C PMA, resistivity was degraded for all the samples.

Figure 4.10 shows XPS spectra for the sample of before and after PMA. Spectrum of 800°C PMA gave no N 1s peak. So it is supposed to reaction with oxygen or H_2O, which remains in PMA ambient.

Figure 4.11 shows XRD patterns, before and after PMA. The crystallization of TaN – Cubic was confirmed for the sample after 800°C PMA. However, (111) peak shift was observed. This fact indicates that the interplanar space was changed after PMA because of loss of N content.

3. The effect of the low temperature long time anneal for Dy_2O_3

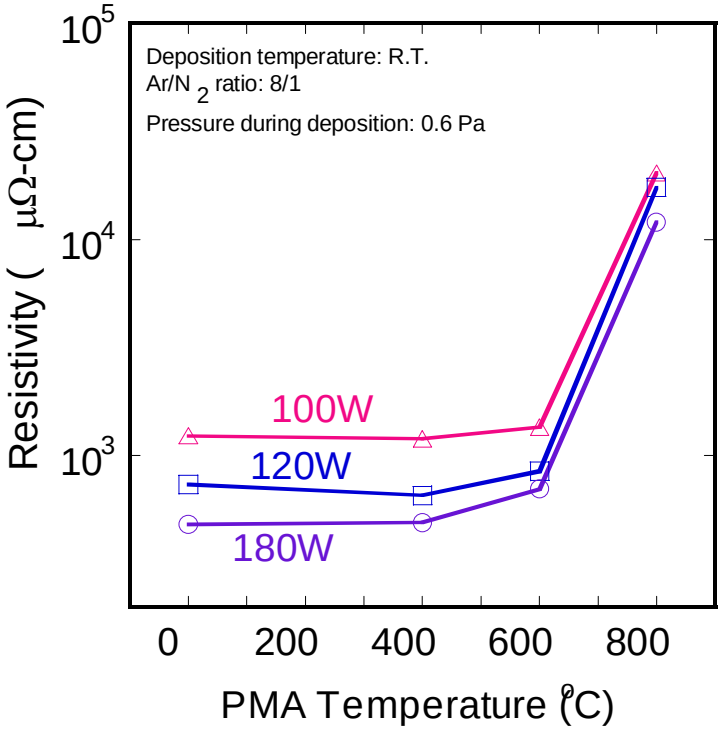


Figure 4.8 PMA temperature dependence of Resistivity with RF power as a parameter

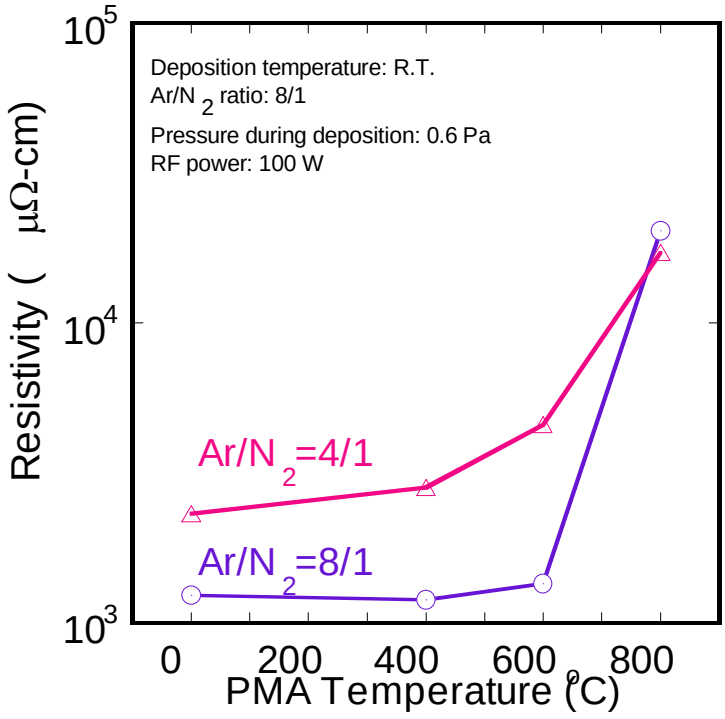


Figure 4.9 PMA temperature dependence of Resistivity with N_2 ratio as a parameter

3. The effect of the low temperature long time anneal for Dy_2O_3

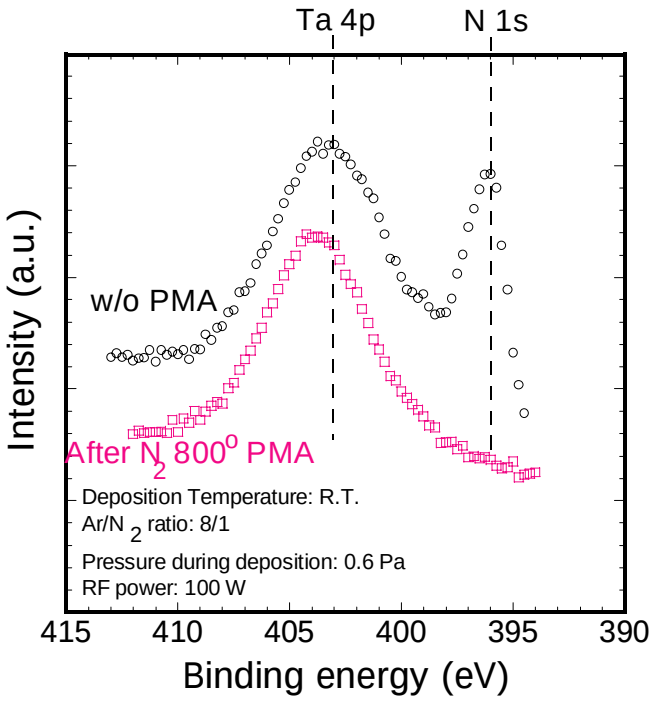


Figure 4.10 XPS spectra for the samples before and after PMA

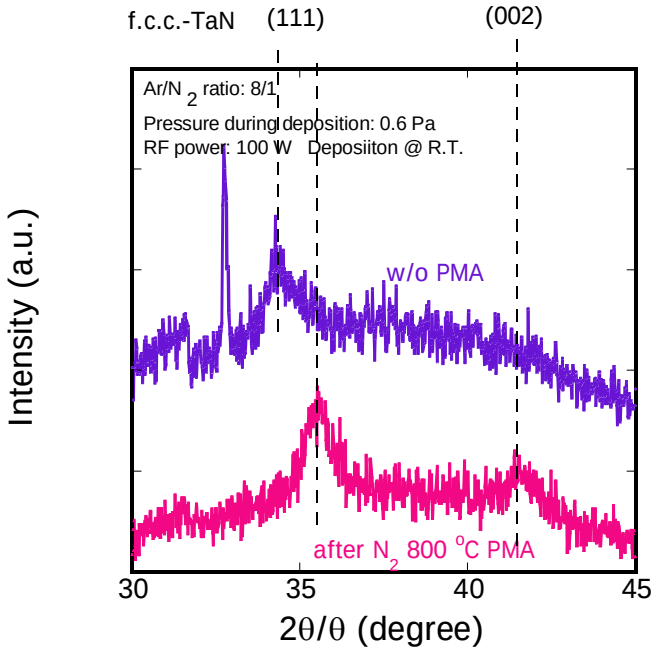


Figure 4.11 XRD patterns for the samples before and after PMA

3. The effect of the low temperature long time anneal for Dy_2O_3

4.4 Summary of this chapter

The fundamental properties of TaN film were examined. In this chapter, thermal budget test was mainly examined.

As to RF power during the sputtering, it was necessary to deposit the film at high sputtering power in order to reduce the resistivity. And it was confirmed that crystallization depended on RF power during the deposition from XRD patterns. The improvement of resistivity is due to the crystallization.

For N_2 ratio dependence during sputtering, the sample deposited at higher N_2 ratio shows higher N content. And the crystallization was accelerated in the case of Ar/N_2 = 4/1.

With deposition temperature dependence, acceleration of crystallization did not depend on the substrate temperature (~ 400^{o}C) in this experiment. To make matters worse, resistivity was degraded in the case of 400 ^{o}C deposition. It seems to be due to the degradation of background pressure before the deposition.

And these deposited films were examined into thermal stability.

The resistivity was increased over 600^{o}C for each condition. One of the reasons seems to be due to residual oxygen in PMA ambience, which reacted with metal during annealing.

3. The effect of the low temperature long time anneal for Dy_2O_3

Chapter 5

The effect of post metallization anneal with a structure of $TaN/Dy_2O_3/Si(100)$

If Dy_2O_3 film was annealed over 400 ^oC in O_2 ambience, T_{ox} Electrical Equivalent increased as compared with as-deposited film, as discussed in chapter 3. In this chapter, in order to solve this problem, the effect of annealing after the metal deposition was evaluated.

3. The effect of the low temperature long time anneal for Dy_2O_3

5.1 Fabrication procedure

Fabrication procedure of MIS capacitor is shown in Figure. 2.1. Dy_2O_3 films were deposited by electron beam evaporation in ultra high vacuum (UHV) chamber at room temperature or 250^oC on n-type Si(100) substrates treated by diluted HF. Some of the samples were chemically oxidized by H_2O_2 dip to form 0.5 nm SiO_x layer. The deposition rate of the film was about 0.7nm/min. Some of the deposited samples were then annealed at 600^oC for 5 min in O_2 ambient. TaN electrode was deposited on the top of the oxide. The TaN sputtering condition is shown in table 1, which was on the basis of results in chapter 4. And then, PMA (Post Metallization Anneal) was carried out at 400^oC or 600^oC. For gate patterning, photolithography was introduced. Metal etching condition is shown in Table 5.2. And then, Al back electrode was deposited on backside of n-Si (100) substrate.

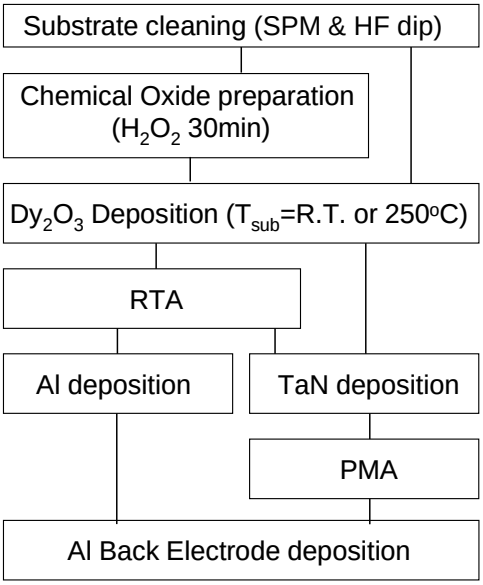


Figure 5.1 Experimental procedure

Table 5.1 TaN sputtering condition

Back ground pressure	~ 2.0 x 10^{-5} Pa
Pressure during sputtering	0.6 Pa
RF power	120 W
Ar/N_2 ratio	3.8/0.48 sccm
Substrate temperature	R.T.

3. The effect of the low temperature long time anneal for Dy_2O_3

Table 5.2 Metal etching conditions (Al and TaN)

Metal	Etching Condition
Al	Wet etching: Immerse in H_3PO_4 (55 °) with rate of 200 nm/30 sec
TaN	RIE: 1. Pressure during etching: 0.03 Torr 2. RF power: 50W 3. Ar/CF_4 ratio: 50/50sccm 4. etching time: 1 min 30sec x 7 times for 100 nm thick

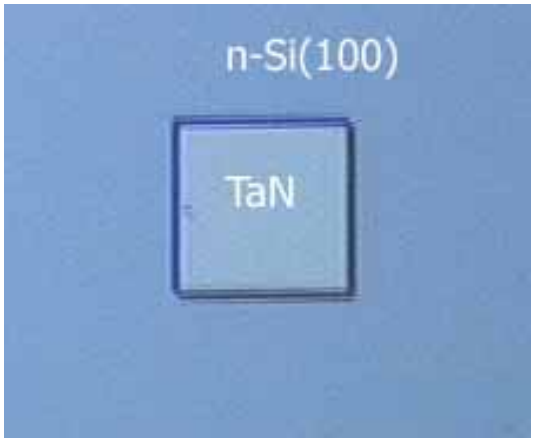


Figure 5.2 TaN electrode patterned by photolithography

5.2 Investigation on post metallization anneal

Figure 5.3 shows C-V characteristics for TaN/Dy_2O_3/n-Si(100) structures. Dy_2O_3 film was deposited at RT.

Samples, which were not annealed before metal deposition (as-depo/N_2 400°C PMA), showed higher accumulation capacitance. And hysteresis was improved by PMA, especially after 600°C PMA. On the other hand, for the sample annealed in O_2 at 600°C before TaN deposition exhibited severe decrease of accumulation capacitance.

Figure 5.4 shows the leakage current result for the same samples shown in Figure 5.3. Samples of only PMA showed high leakage current of 2×10^{1} A/cm^2 even though after the 400°C PMA, while RTA 600°C/PMA 400 °C sample exhibited low leakage current of 2×10^{-6} A/cm^2 @ V_G = +1V.

From these C-V and J-V, the formation of interfacial layer could be suppressed with improvement of hysteresis by annealing with metal electrode cover. By this method, oxygen penetration to the interface was almost suppressed.

3. The effect of the low temperature long time anneal for Dy_2O_3

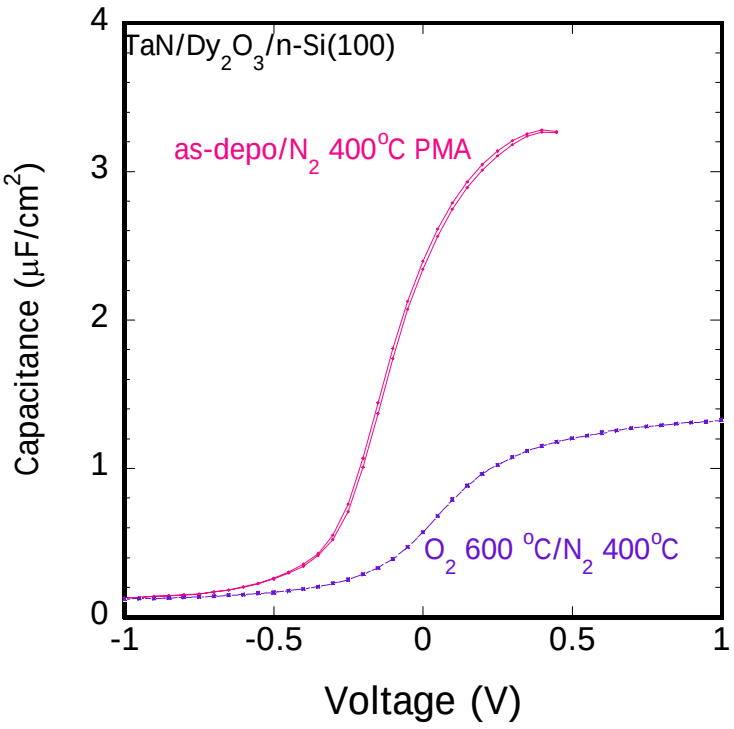


Figure 5.3 C-V characteristics for $TaN/Dy_2O_3/n\text{-}Si(100)$

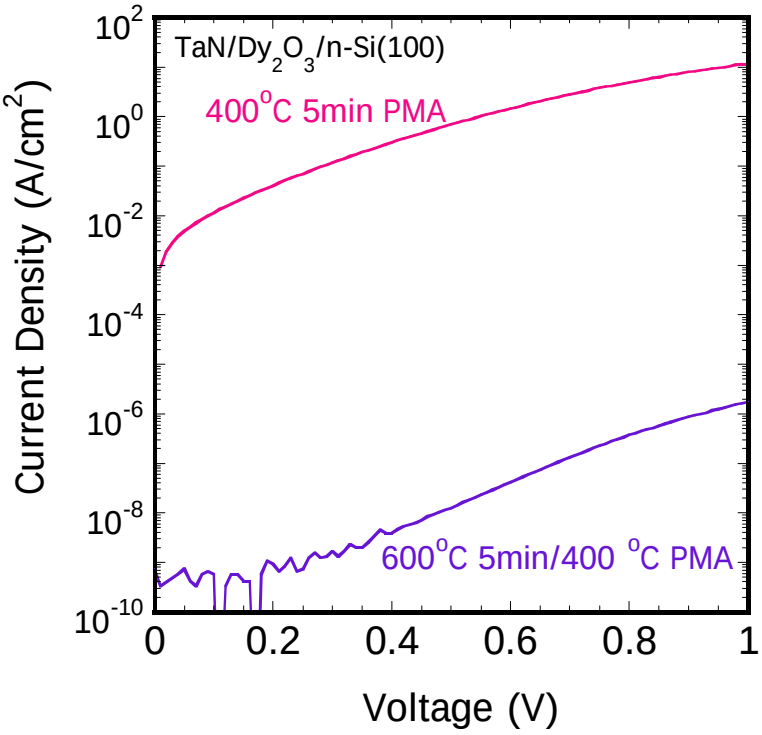


Figure 5.4 J-V characteristics for $TaN/Dy_2O_3/n\text{-}Si(100)$

3. The effect of the low temperature long time anneal for Dy_2O_3

Additionally, LLTA was also carried out as PMA. Metal deposited samples were annealed at 400°C 5min, 400°C 90min and 600°C as PMA, shown in Figures 5.5 and 5.6. In the case of direct annealing for oxide films, LLTA was effective for the reduction of leakage current, maintaining T_{eq} with slight increase.

However, LLTA did not give the effect as PMA. Oxygen activation occurred not only at the interfacial layer but also in the Dy_2O_3 film. Therefore, the effect of LLTA is dependent of the oxygen pressure

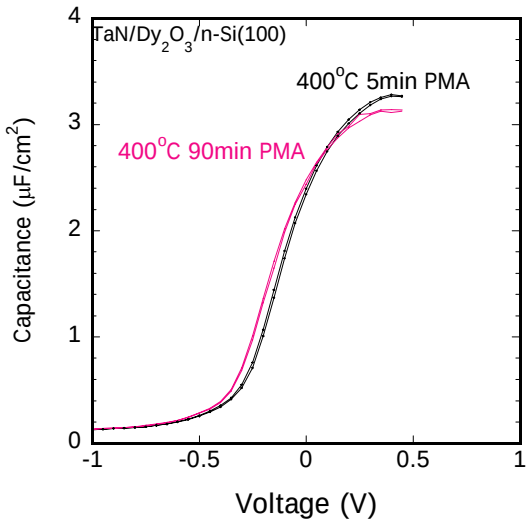


Figure 5.5 C-V characteristics for LLTA sample as PMA

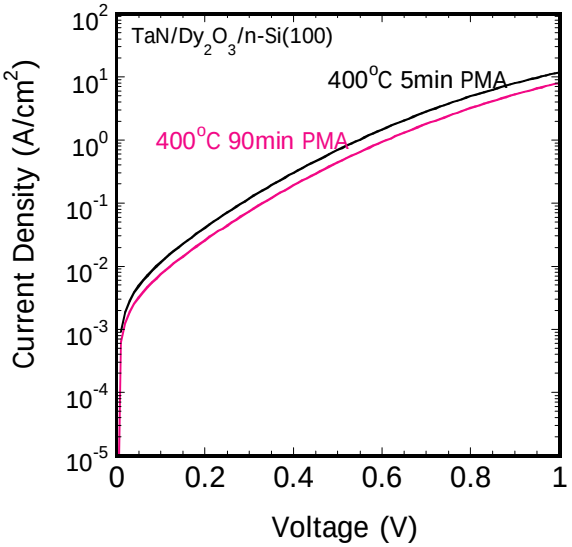


Figure 5.6 C-V characteristics for LLTA sample as PMA

3. The effect of the low temperature long time anneal for Dy_2O_3

Figure 5.7 shows C-V characteristics with PMA temperature as a parameter. From this result, for the sample of 600°C PMA, a shoulder in depletion region was indicated due to interface state.

These results suggest the oxygen defect was not improved by PMA because of the no supply of oxygen from outside. And after 600°C PMA, oxygen in Dy_2O_3 was taken into formation of interfacial layer. Therefore, influence of oxygen defect at interface became very much.

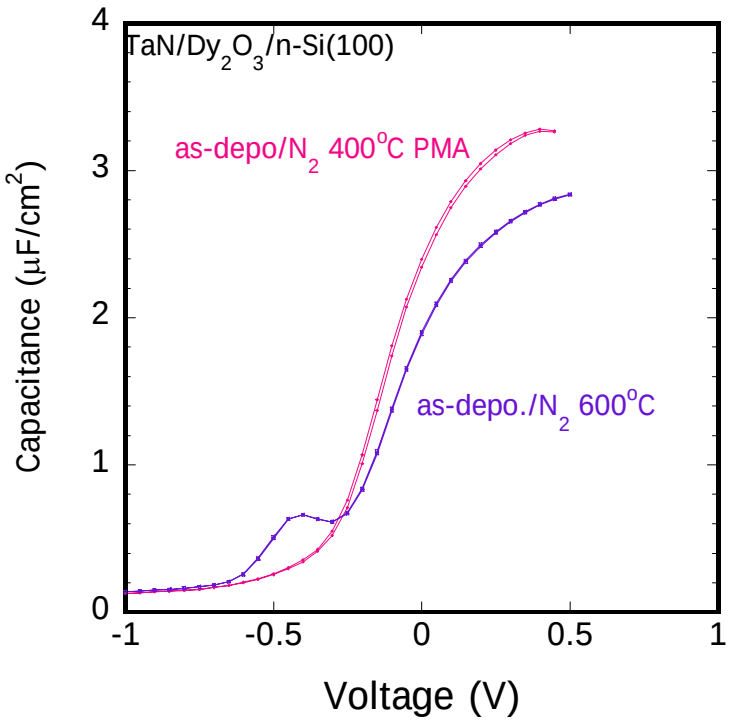


Figure 5.7 C-V characteristics with vertical axis as C/C_{max}

In order to improve the film with low defect, the effects of high temperature deposition of Dy_2O_3 and Si surface treatment by H_2O_2 were investigated.

Figure 5.8 shows C-V characteristics for samples with and without chemical oxide preparation. The Dy_2O_3 thin film was deposited at 250°C. The accumulation capacitance of 400 °C PMA sample without directly annealing for oxide in O_2 ambient (as-depo/N_2 400°C) exhibited excellent T_{ox} Electrical Equivalent of 1.03 nm for sample of HF-last and 1.01 nm for sample with chemical oxide, respectively. However, the huge interface state was also indicated for the 600°C PMA case.

Figure 5.9 shows J-V characteristics for the same samples shown in Figure 5.8. From this result, the effect of the chemical oxide showed the leakage current reduction of a

3. The effect of the low temperature long time anneal for Dy_2O_3

half order of magnitude. And similar to the case of RT deposition, the samples were divided into 2 groups, whether Dy_2O_3 films were before the metal deposition.

Figure 5.10 shows T_{ox} Electrical Equivalent dependence of current density. From this result, it was confirmed that 250°C deposited sample exhibited better characteristics than RT deposited sample, and the sample with chemical oxide at the interface showed further improvement.

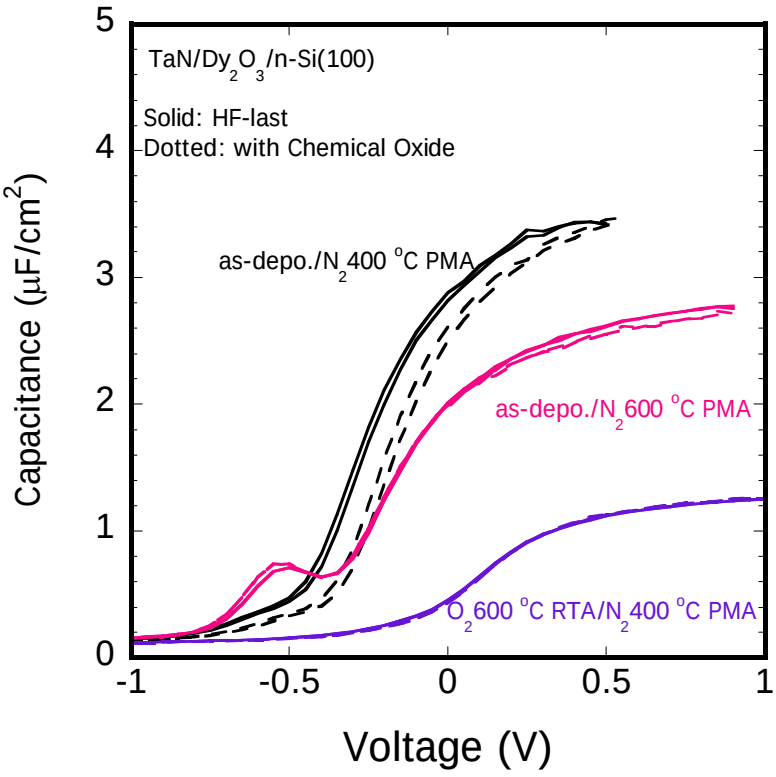


Figure 5.8 C-V characteristics for samples with and without chemical oxide preparation

3. The effect of the low temperature long time anneal for Dy_2O_3

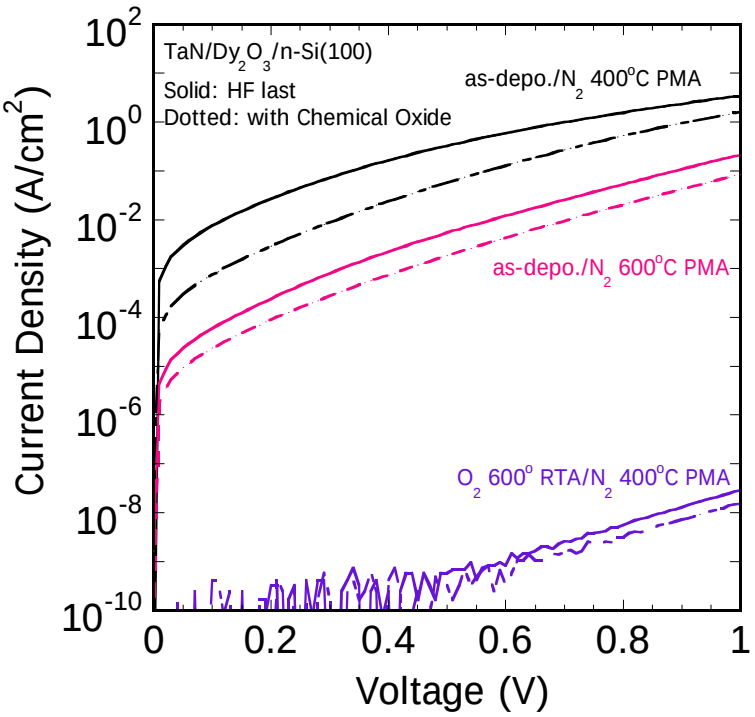


Figure 5.9 J-V characteristics for samples with and without chemical oxide preparation

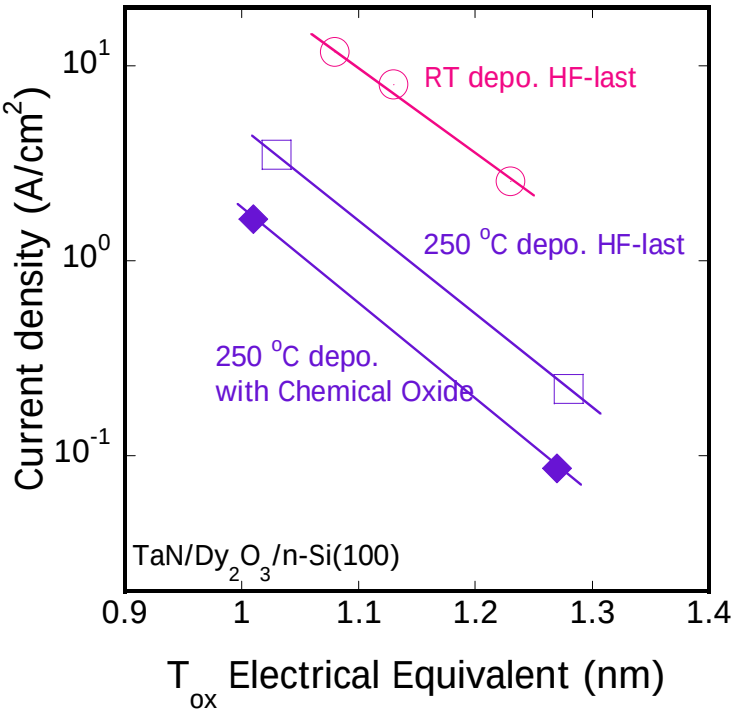


Figure 5.7 T_{ox} Electrical Equivalent dependence of current density

3. The effect of the low temperature long time anneal for Dy_2O_3

5.3 Summary of this chapter

In this chapter, the effect of annealing after metal deposition for slight growth of interfacial layer was confirmed. However, the oxygen defect was indicated from their negative shift and interface state after the PMA.

And films deposited at 250^{o}C exhibited the improvement as compared with R.T. deposited films in the characteristic of J-T_{eq}, and further improvement was obtained for chemical oxide prepared sample.

3. The effect of the low temperature long time anneal for Dy_2O_3

Chapter 6

Conclusions

3. The effect of the low temperature long time anneal for Dy_2O_3

6.1 Main results obtained from this study

In the case of annealing in oxygen without electrode, 400 ^oC/90 min anneal decreased the leakage current with slight decrease of accumulation capacitance as compared with 600^oC/5min anneal. It seems to be due to effective activation of Dy_2O_3. However, even the LLTA, the accumulation capacitance decreased as compared with as-depo. sample as shown in Figure 6.1.

This interfacial layer shows lower dielectric constant as compared with Dy_2O_3 ($\varepsilon_{Dy2O3} > \varepsilon_{il} > \varepsilon_{SiO2}$), therefore it influences T_{eq} strongly, as following equation (e.q. 6.1). So, T_{eq} and leakage current should be controlled by Dy_2O_3 thickness itself.

$$T_{eq} = \frac{T_{Dy_2O_3}}{\varepsilon_{Dy_2O_3}} \varepsilon_{SiO_2} + \frac{T_{il}}{\varepsilon_{il}} \varepsilon_{SiO_2} \tag{6.1}$$

In the case of annealing after the metal deposition, oxygen penetration to the interface was suppressed and the accumulation capacitance did not decrease i.e. the formation of interfacial layer could be suppressed by the cover of metal electrode (see Figure 6.2).

This annealing method suppressed the interfacial layer thickness ($T_{il} << T_{Dy2O3}$), therefore, T_{eq} and leakage current could be controlled by Dy_2O_3 thickness.

However, negative shift and interfacial state due to the defect of oxygen were indicated for PMA only samples. These results suggest the necessity of the sufficient oxygen in Dy_2O_3 film of as-deposited.

Finally, LLTA as PMA was not exhibited the effect of reduction of leakage current such as annealed in O_2 because sufficient activation was not given in the condition of no supply of oxygen from outside.

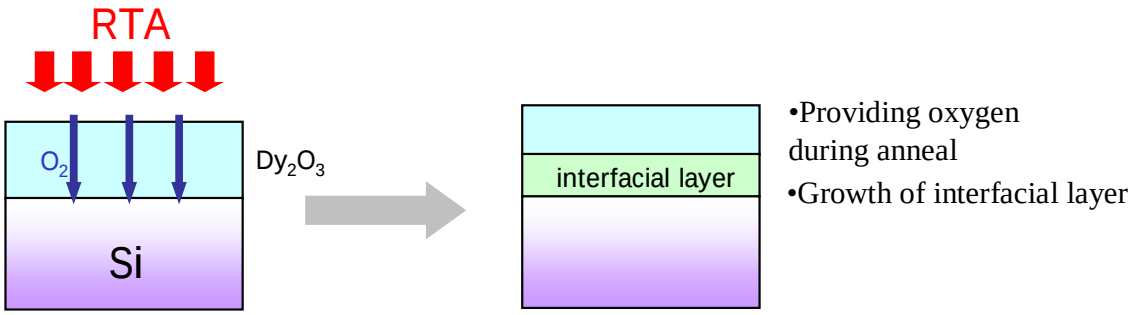


Figure 6.1 Interfacial layer growth due to annealing in oxygen

3. The effect of the low temperature long time anneal for Dy_2O_3

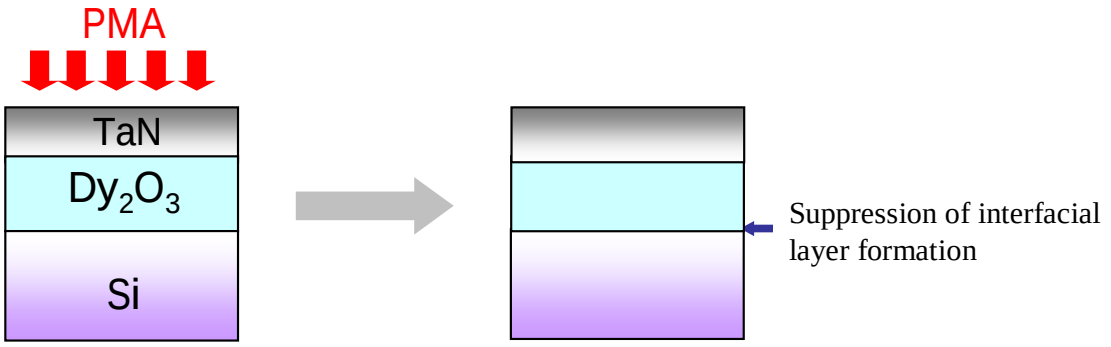


Figure 6.2 Suppression of oxygen penetration by TaN metal cover

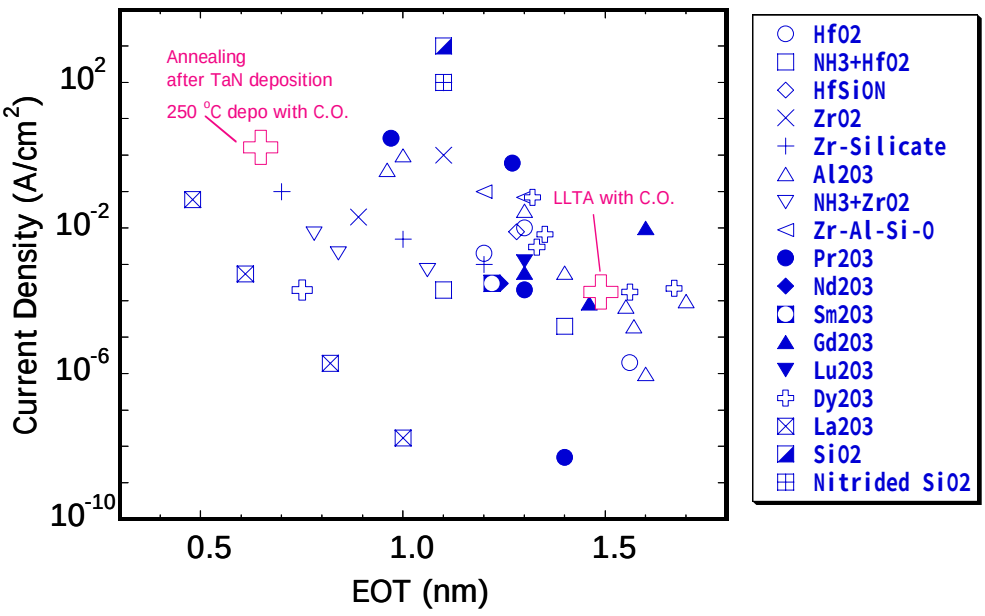


Figure 6.3 J-EOT characteristics with reported data

Figure 6.3 shows J-EOT characteristics with reported data. EOT of 0.65 nm with leakage current of 1.64 A/cm^2 was obtained for the film deposited at 250 °C, annealed at 400 °C after metal deposition. And for the sample of LLTA, 1.76×10^{-4} A/cm^2 was obtained with EOT of 1.49 nm.

3. The effect of the low temperature long time anneal for Dy_2O_3

6.2 Future study

To make the film with sufficient oxygen content, the effect of radical oxidation should be investigate.

And it is reported that the interfacial layer affects to carrier mobility, i.e. carrier mobility was improved by interfacial layer. Therefore, electron mobility for with or without interfacial layer samples should be characterized by evaluating MOSFET.

3. The effect of the low temperature long time anneal for Dy_2O_3

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Yokohama, JAPAN
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3. The effect of the low temperature long time anneal for Dy_2O_3

REFERENCE

[1] Y. H. Kim et al., “High quality CVD TaN gate electrode for sub-100 nm MOS devices”, IEDM Tech Dig., 2001

[2] B. H. Lee et al., “Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8A-12A)”, IEDM Tech. Dig., 2000 pp. 39-42.

[3] J. C. Chuang et al., “Properties of thin Ta-N films reactively sputtered on $Cu/SiO_2/Si$ substrate” Thin Solid Films 322, 1998 pp. 213-217.

[4] M. Stavrev et al., “Sputtering of tantalum-based diffusion barriers in Si/Cu metallization: effect of gas pressure and composition” Applied Surface Science 91, 1995 pp. 257-262.

[5] Ranjana Saha et al., “Effect of structure on the mechanical properties of Ta and Ta(N) thin films prepared by reactive DC magnetron sputtering” Journal of Crystal Growth 174 (1997) pp. 495-500.

[6] H. Zhong et al., “Properties of Ru-Ta Alloys as Gate Electrodes For NMOS and PMOS Silicon Devices” IEDM Tech Dig., 2000.

[7] D. G. Park et al., “Robust Ternary Metal Gate Electrodes for Dual Gate CMOS Devices” IEDM Tech Dig., 2000.

[8] C. H. Lee et al., “MOS Device with High Quality Ultra Thin CVD ZrO2 Gate Dielectrics and Self-Aligned TaN and TaN/Poly-Si Gate Electrodes” Symp. on VLSI Tech., 2001 pp. 137-138.

[9] C. H. Lee et al., “Self-Aligned Ultra Thin HfO_2 CMOS Transistors with High Quality CVD TaN Gate electrode” Symp. on VLSI Tech., 2002

[10] S. B. Samavedam et al., “Metal Gate MOSFETs with HfO_2 Gate Dielectric” Symp. on VLSI Tech., 2002

[11] JCPDS Card

[12] K. Radhakrishnan et al., “Reactive sputter deposition and characterization of tantalum nitride thin films” Materials Science and Engineering B57 (1999) pp. 224-227.

[13] S. Jeon et al., “Excellent Electrical Characteristics of Lanthanide (Pr, Nd, Sm, Gd, and Dy) Oxide and Lanthanide-doped Oxide for MOS Gate Dielectric Applications” IEDM Tech Dig., 2001 pp. 471-474

[14] U. Neuwald et al., “Chemical oxidation of hydrogen passivated Si(111) surfaces in H_2O_2” J. Appl. Phys. 78 1995 pp.4131-4136

[15] International Technology Roadmap for Semiconductors 2001 edition