Chapter 1
Introduction

1.1 Back ground

1.1.1 Introduction

Information Technology (IT) has become one of the most important technologies to improve the quality of our life. The cellular phone, Internet and the other mobile systems have spread very rapidly all over of the world. The progress of IT entirely owes to that of semiconductor technology.

Now, the performances of silicon large-scale integrated circuits (LSI), especially, complementary Metal-Oxide-Semiconductor large-scale Integrated circuits (CMOS LSI) require operating by high speed for PC and low power for mobile. In order to make high performance, Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) which are components of LSI are required downsizing. The downsizing of MOSFET leads to high performance and low power operation for LSI. And downsizing of MOSFET has been accomplished by the scaling method.

1.1.2 Limits of SiO_2 gate insulator

Figure 1-1 and Table 1-1 show the scaling method for MOSFET. In the method, gate length, gate width, gate oxide thickness, junction depth and supply voltage are decreased by factor S and Si substrate impurity concentration is increased by factor S.

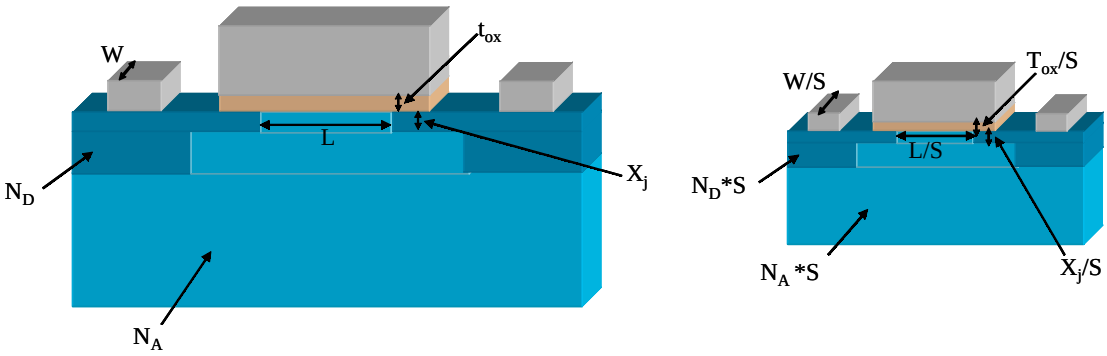


Fig. 1-1 scaling method for MOSFET

Quantity	*Before scaling*	*After scaling*
Channel length	L	L' = L/S
Channel width	W	W' = W/S
Device area	A	A' = A/S^2
Gate oxide thickness	t_{ox}	t_{ox}' = t_{ox}/S
Gate capacitance per unit area	C_{ox}	C_{ox}' = S*C_{ox}
Junction depth	x_j	x_j' = x_j/S
Power supply voltage	V_{DD}	V_{DD}' = V_{DD}/S
Threshold voltage	V_{T0}	V_{T0}' = V_{T0}/S
Doping densities	N_A	N_A' = S*N_A
	N_D	N_D' = S*N_D

Table 1-1 scaling method for MOSFET

Table 1-2 shows the International Technology Roadmap for Semiconductor (ITRS) 2001, SiO_2 gate insulator should require below 1 nm in 2004. Table 1-3 shows the electrical properties for 1 nm-thick SiO_2 gate insulator. In this table, when SiO_2 thickness decreased below 0.8 nm, direct tunneling will appear about 1 kA/cm^2 and problem in oxide reliability. From this result, there will cause the increase of the

power consumption and degradation of LSI reliability.

Therefore, ITRS requires the replacement of SiO_2 CMOS gate dielectric materials as a “Grand Challenge” to the historical progression of device downsizing. To reduce the leakage current, the physical thickness of gate insulator should be kept large while the capacitance still should increase. This can be accomplished by the use of dielectric materials with high dielectric constant. Typically, for high-k materials, the dielectric constant is in the 10–40 range, a factor of approximately 3–10 higher than that of SiO_2 (k=3.9).

It is anticipated that new materials will be requirement by 90 nm node to provide 0.9-1.4 nm Tox electrical equivalent (EOT).

Year	**2004**	**2007**	**2010**	**2013**	**2016**
Node (nm)	90	65	45	32	22
L_g (nm)	37	25	18	13	9
EOT (nm)	0.9-1.4	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
V_{dd} (V)	1.0	0.7	0.6	0.5	0.4

Table 1-2 ITRS 2001

EOT (nm)	1.0
Leakage current density (A/cm^2)	100
Gate length (μm)	0.1
Gate width (μm)	5
Gate area (cm^2)	5×10^{-9}
Functions per chip (transistors/chip)	10^8
Total gate area (cm^2)	5×10^{-1}
Total leakage current per chip (A/chip)	50

Fig. 1-3 Electrical properties for 1 nm-thick SiO_2 gate insulator

1.1.3 Requirements and Problems in High-k gate insulator

ITRS requires the necessity of the replacement of SiO_2 gate dielectric films by High-k materials until 2004. The requirements for high-k materials are as follows.

(1) Large dielectric constant (k=10~30)
(2) Small leakage current density
(3) Chemically stable at the Si interface at high process temperature (1000 K).
(4) Small densities of interface state and fixed charge
(5) High mobility and reliability

Table 1-4 shows the reported high-k materials for gate insulator. Al_2O_3, ZrO_2 and HfO_2 have been widely studied for next generation materials for gate dielectrics because they have high dielectric constants and wide band gap. Rare earth oxides (lanthanide oxides) also have high dielectric constant and been studied as promising candidates. Recently, excellent results of rare earth oxides, such as La_2O_3, CeO_2, Pr_2O_3, Gd_2O_3, Dy_2O_3 and their silicate have been reported.

However, high-k materials include of rare earth oxides have many unsolved problems -- narrow bang gap, formation interfacial layer, growth micro-crystal and moisture absorption etc. --, so the optimal material is not found yet.

	k	Contact stability with Si (kJ/mol)	Lattice energy (KJ/mol)	Band gap (eV)	Structure
SiO_2	3.9	Stable	13125	9	Amorphous
NO stack	5-7	Stable	-	-	Amorphous
Al_2O_3	10	+63.4	15916	6-8	Amorphous
Silicate ($Zr_xSi_yO_z$, $La_xSi_yO_z$ etc.)	10-15	-	-	-	Amorphous or crystal
ZrO_2 , HfO_2	20-30	~ +45	11188 (ZrO2)	5.0, 5.8	Amorphous or crystal
Rare earth oxide	15-30	~ +100	12687-13871	2.4-5.4	Amorphous or crystal

Table 1-4 The reported high-k materials for gate insulator

The dielectric constant of Al_2O_3 is about 10, a factor of approximately 2.5 higher than that of SiO_2. And the biggest problem for the Al_2O_3 is that film thickness dependence of the flat-band shift due to the fixed charge is so strong that controllability of the flat-band voltage is difficult.

ZrO_2 and HfO_2 become popular materials because their dielectric constants are relatively high and because they were believed to be stable at the Si interface. However, in reality, formations and growths of interfacial layer made of silicate or SiO_2 at the Si interface and micro-crystal during the thermal process has been a serious problem. Recently, the most serious problems are found to ZrO_2 and HfO_2 that they formed silicide during the thermal process.

Rare earth oxides are that no micro-crystal formation was found in high temperature process of MOSFET fabrication, and there might be a possibility that they have better characteristics for the gate insulator. Recently, amorphous La_2O_3 and epitaxial Pr_2O_3 and so on are reported to have small EOT and leakage current. However, moisture absorption is the biggest concern. The oxides become hydroxide and carbonate in H_2O and CO_2 ambient.

1.2 Physical properties of Rare Earth Oxides

Figure 1-2 shows a part of the periodic table, for lanthanide elements. There are 15 elements, but Pm is an unstable radioactive artificial element and should be removed from the candidates. Although, the outer shell electron configurations are the same for all the lanthanide elements, it was found that the properties of lanthanide oxides are quite different. Band gap and lattice energy for the lanthanide oxides are shown in, Fig.1-3 (a) and (b) respectively. The reported dielectric constants of rare earth oxides are about 15-30, and the energy band gap is about 2.4-5.4 eV. Lanthanides are called as 'rare earth' elements, but it should be noted that they are in reality 'no rare' in the earth-shell and even their contents are larger than that of Hg, In, Ag, etc.

The crystal structure of rare earth oxides at low temperature is divided into four types. Type A has hexagonal system, type B has monoclinic system and type C has cubic system.

La	Ce	Pr	Nd	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu

Fig. 1-2 Lanthanide elements

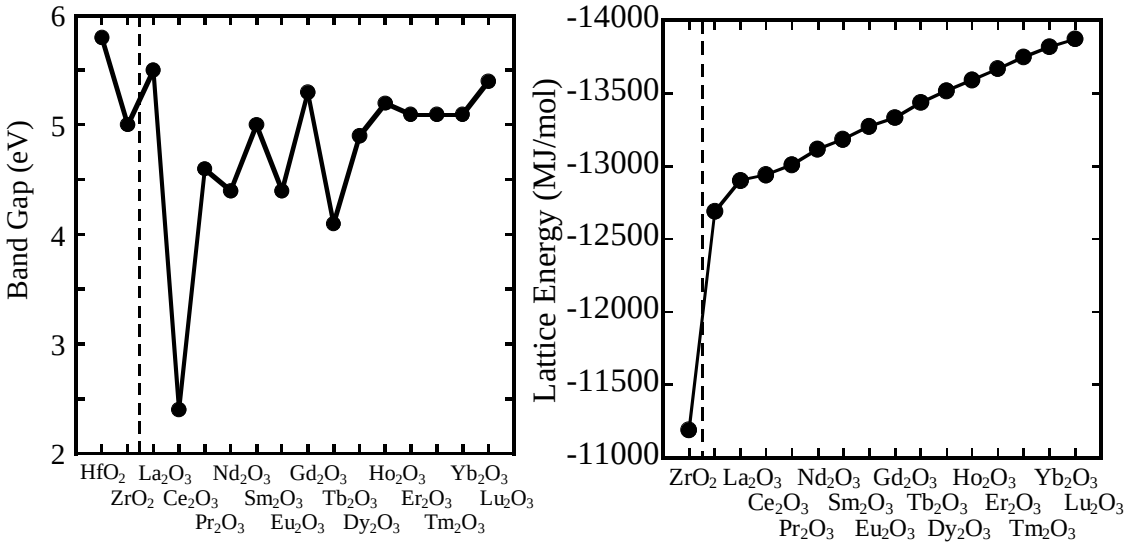


Fig.1-3 (a) Band gap (b) Lattice energy

1.3 Purpose of this study

Among the high dielectric constant materials, rare earth oxides seem to be the most promising, however still has some serious problems especially thin film and Si substrate interface. The purpose of this study is to improve the interfacial characteristic -- film uniformity, interface state density and leakage current -- by using MBD method. The thin film properties are evaluated by fabricating MIS capacitors, and investigated surface treatment for Si substrate before High-k films deposition.

Chapter 2
Fabrication and Characterization Method

2.1 Fabrication Methods

In this section, we will introduce the fabrication methods of MIS capacitors for this study.

2.1.1 Chemical cleaning of Si substrate

Prior to rare earth oxides deposition, Si substrate was chemically cleaned to remove impurities and particles from the surface.

Ultra-pure water (UPW) systems used in this study, the provided UPW with more than 18.2 MΩ·cm resistively. UPW is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination.

In this study, the substrate cleaning process was so designed as to control the ultra-clean Si surface, which was given in Fig. 2-1. First, the conventional chemical cleaning using SPM solution (sulfuric acid (H_2SO_4): hydrogen peroxide (H_2O_2)= 4:1) was performed to remove any organic material and metallic impurities. And then, the substrates dipped in hydrofluoric acid (HF) for 5 min to remove the native or chemical oxide. Finally, the cleaned wafer was dipped in UPW and loaded to chamber immediately (HF-last).

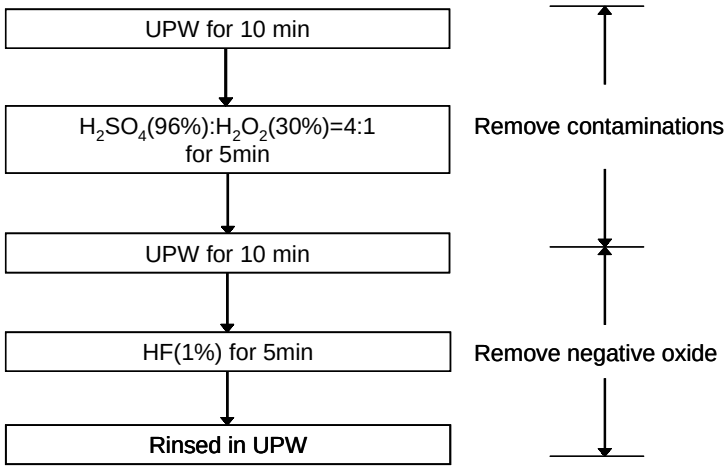


Fig. 2-1 Cleaning process of Si substrate

2.1.2 Surface treatment of Si substrate

In order to improve interfacial condition, formation of SiO_2 or SiOxNy prior to deposition was investigated.

After the conventional cleaning process, various surface treatments of Si substrate carried out.

There were two-way methods to form chemical oxide. First, the substrates were dipped in H_2O_2 solution for 30 min at R.T. followed by rinsing in UPW. At room temperature, oxidation rate is 0.5 nm by 30 min. The second method was using SPM solution, the substrates were dipped in SPM solution for 5 min followed by rinsing in UPW.

In this study, formation SiOxNy layer was using RTA. The detail of RTA equipment will explain at section 2.1.4.2. After HF-last or chemically oxidized by H_2O_2 substrate were annealing in NH_3 at 1050^{o}C for 10 sec.

These steps were shown in Fig. 2-2.

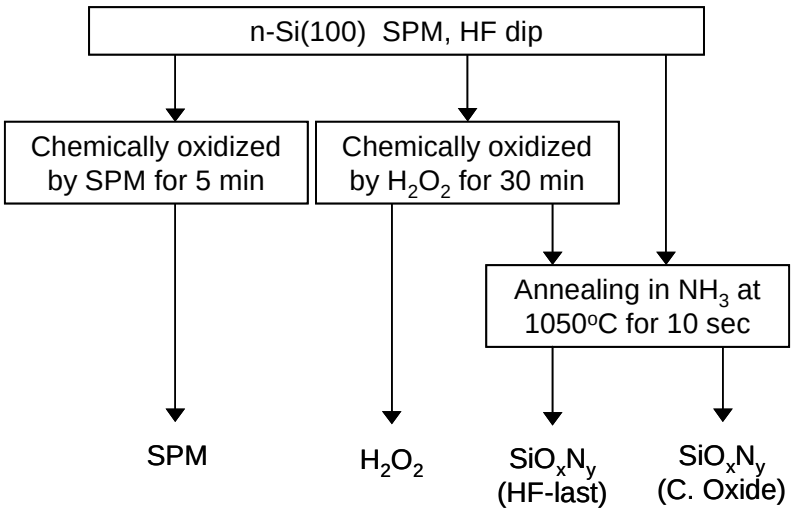


Fig. 2-2 Surface treatment process for Si substrate

2.1.3 Molecular Beam Deposition (MBD) Method

In this study, MBD method using MBE equipment is employed for rare earth oxides deposition. MBE is a low damage and low contamination method compared to sputtering or Chemical Vapor Deposition (CVD). This method is suitable for research basic characteristics of high-k thin films.

Figure 2-3 show the schematic drawings of the component of MBE equipment that was used in this study. The backpressure of growth chamber was about 10^{-10} Torr vacuums with an ion pump and the introduction of liquid N_2. During deposition, the pressure of growth chamber was about 10^{-7} to 10^{-9} Torr. In this study, sintered rare earth oxide target irradiated with electron beam, the accelerated voltage applied –5 keV. The physical thickness of the film was monitored with a film thickness counter using crystal oscillator. The temperature of the substrate was controlled by a substrate heater and is measured by a thermocouple.

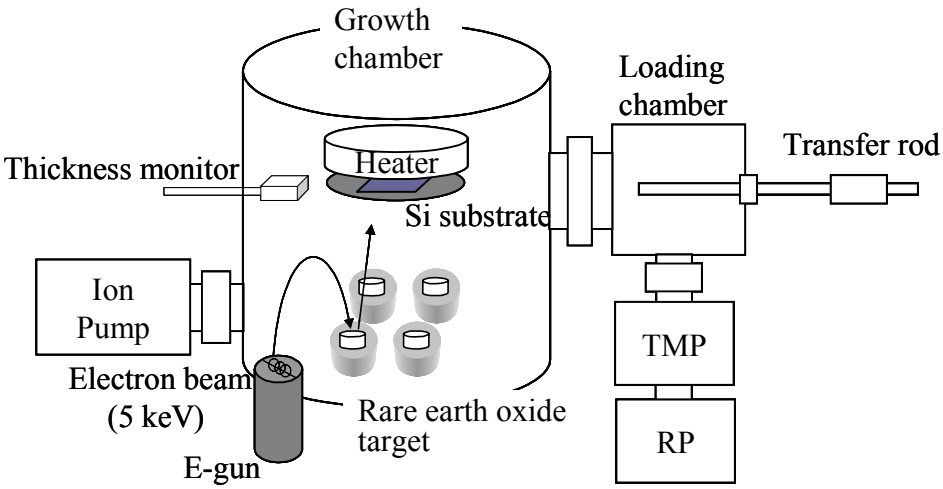


Fig. 2-3 Schematic drawings of MBE equipment

2.1.4 Rapid Thermal Annealing (RTA)

2.1.4.1 RTA

RTA equipment (MILA-3000, ULVAC Co. Ltd.) is used for post deposition anneal.

The method of annealing is lamp heating and water-cooling, and the schematic of RTA equipment is shown in Fig. 2-4. In this study, annealing in oxygen or nitrogen ambient in atmospheric pressure by flowing gas into the furnace, flowing rate of gas was 1.2 l/min. The furnace cannot be vacuumed, so the remaining air or moisture of the furnace cannot be completely replaced by the gas.

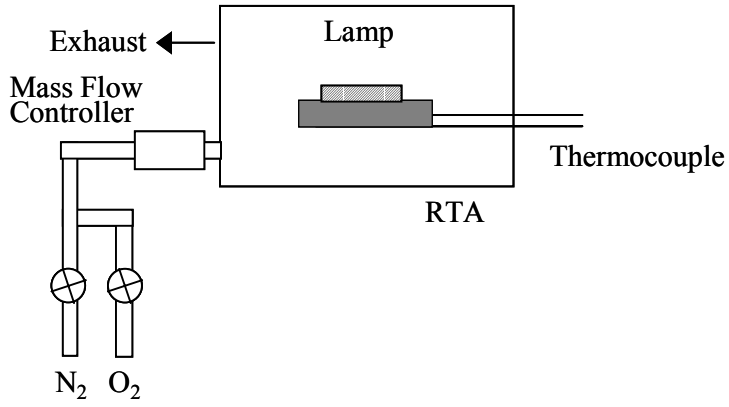


Fig. 2-4 RTA equipment

2.1.4.2 Nitrization RTA

Figure 2-5 shows the nitrization RTA that was used oxy-nitraided Si substrate. In this study, oxy-nitrization of Si substrate was using ammonia gas. The method of oxy-nitrided Si substrate were annealing in ammonia ambient in atmospheric pressure by flowing gas into the furnace, flowing rate of gas was 1 l/min. Prior annealing, the furnace vacuumed and displacement of nitrogen gas to atmospheric pressure. However, the problem is this equipment is pipeline leak, so the air of the pipeline induced inhibition pure nitrization.

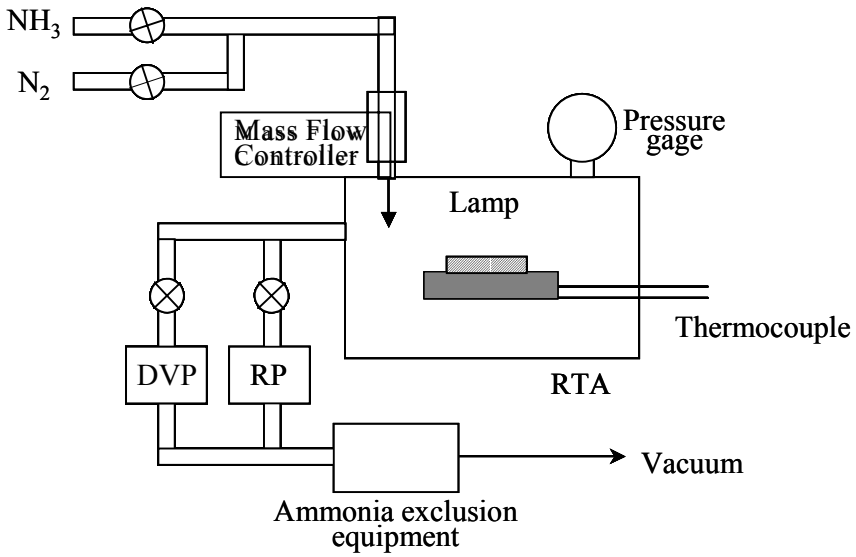


Fig. 2-5 Nitrization RTA equipment

2.1.5 Vacuum Evaporation Method

Top and bottom Al electrodes were deposited by vacuum evaporation equipment. Vacuum evaporation method is easy and speedy compared to sputtering.

Figure 2-6 shows the vacuum evaporation equipment. The pressure during evaporation was approximately 10^{-5} Torr, and Al was evaporated with resistance heating of tungsten filament and deposited on the sample. The top electrodes were deposited through the metal shadow mask. The size of Al circular electrodes was about 110 μm in diameter. After removed the negative oxide at backside of substrate, Al ohmic electrode was deposited.

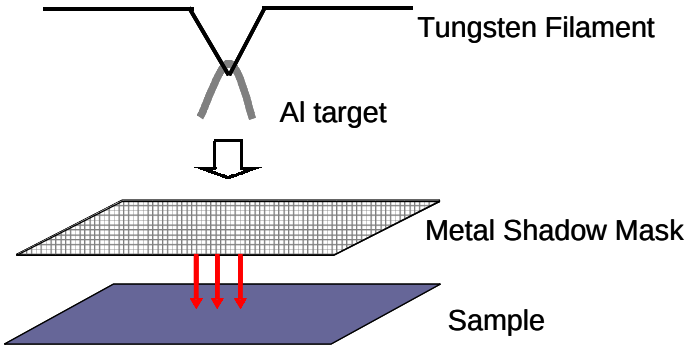


Fig. 2-6 Vacuum evaporation equipment

2.2 Characterization Methods

In this section, we will introduce the characterization methods and theory of MIS capacitors for this study.

2.2.1 Capacitance- voltage (C-V) Method

C-V characteristics of MIS capacitors were measured by using LCR meter (4284A, Hewlett Packard). The measurement range were 20 Hz - 1 MHz.

Figure 2-7 shows typical high frequency C-V characteristics for MIS capacitor of n-type Si. Flat band voltage depends on work function of metal and semiconductor. When Al electrode is used for n-type Si, flat band voltage in C-V characteristic is about 0 V. Interfacial state densities estimate the slope of the C-V curve, and flat band voltage depends on fixed charge.

From the accumulation capacitance at high frequency, C_{max}, Capacitance Equivalent Thickness (CET) is calculated as

$$CET = \frac{\varepsilon_0 \varepsilon_{SiO2} S}{C_{\max}}$$

where ε_0 is permittivity of vacuum, ε_{SiO2} is dielectric constant of SiO_2 (3.9) and S is the area of capacitor. In this study, the measurement frequencies are 1 kHz to 1 MHz.

In addition, C-V characteristic shows hysteresis depending on charge pumping or mobile ion in insulator as shown in fig. 2-8.

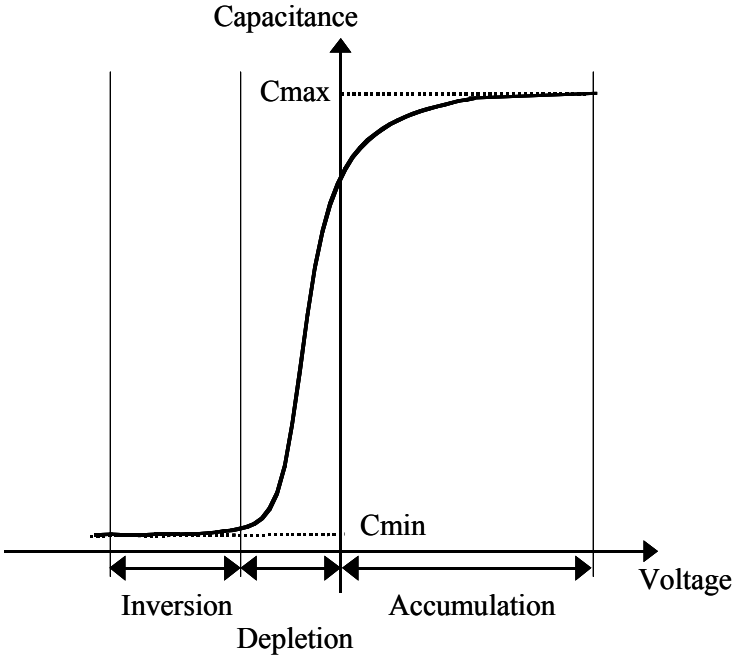
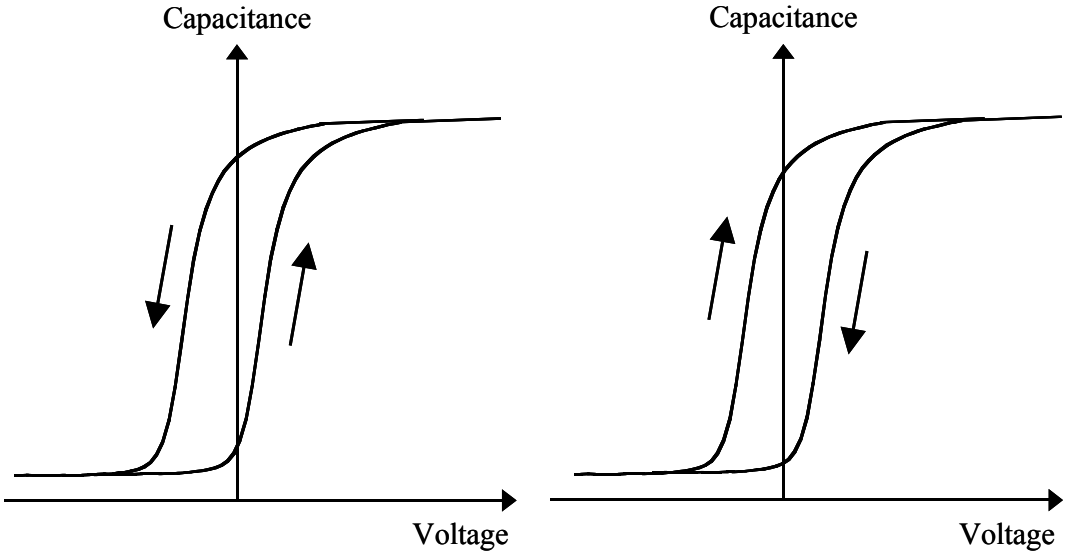


Fig. 2-7 Ideal C-V curve



Ion drift-type

Charge injection-type

Fig. 2-8 Hysteresis curve

The analysis of C-V characteristics is using Terman method.

When measurement in high frequency, interfacial state was regarded fixed charge. In this case, interfacial state density was calculated by shift value from ideal C-V curve to experimental C-V curve. In order to calculate interfacial state, fitting between ideal and experimental curve was needed. After fitting, capacitance change values of experimental and ideal curve against surface potential were calculated. And this results works out interfacial state density.

From shift between ideal and experimental curve, interfacial charge density by unit size was calculated.

$$Q_{SS} = \frac{C_I(\Delta V^{\exp} - \Delta V^{th})}{A}$$

Capacitance value of ideal curve correspond surface potential. And interfacial charge density Q_{SS} differentiates by surface potential φs. Then, interfacial state density by unit size was calculated.

$$N_{SS} = \frac{1}{q} \cdot \frac{\partial Q_{SS}}{\partial \phi_S} = \frac{C_I}{qA}\left[\frac{\partial V_{\exp}}{\partial \phi_S} - \frac{\partial V_{th}}{\partial \phi_S}\right]$$

$$N_{SS} = \frac{C_I}{qA\Delta\phi}\left(\Delta V^{\exp} - \Delta V^{th}\right)$$

The constant of above formula are as follow.

Q_{SS} : interfacial charge density, C_I : capacitance of insulator, C_1,C_2 : different random capacitance, $\triangle V_{exp}$: experimental gate voltage between C_1-C_2, $\triangle V_{th}$: ideal gate voltage between C_1-C_2, ϕ_1 : surface potential against C_1, ϕ_2 : surface potential against C_2, $\triangle\phi$: ϕ_1- ϕ_2 , A : size of electrode

2.2.1 Current density-Voltage (J-V) characteristic

J-V characteristics of MIS capacitors were measured by using semiconductor parameter analyzer (4156C, Hewlett Packard). The measurement range were 10^{-9} A ~ 0.4 A.

J-V characteristics were measured to evaluate leakage current densities.

From analysis of J-V characteristics, the mechanism of gate leakage current exist 3 types: Fowlwer-Nordheim tunneling, Direct tunneling and Pool-Frenkel model.

Fowlwer-Nordheim tunneling (F-N tunneling) occurs when electrons tunnel into the conduction band of the oxide. Figure 2-10 shows the model of F-N tunneling. When the effect of finite temperature and image-force barrier lowing are ignored. At the oxide field of 8 MV/cm, the measured F-N tunneling current density is about $5x10^{-7}$ A/cm^2, which is very small. Thus, for normal device operation, F-N tunneling current is negligible.

If the oxide layer is very thin, below 4 nm, then, instead of tunneling into the conduction band of the film, electrons from the inverted silicon surface can tunnel directly through the forbidden energy gap of the film (Direct tunneling). The theory of direct tunneling is even more complicated than that of F-N tunneling, and there is no simple dependence of the tunneling current density on voltage or electric field. This is illustrated in Fig. 2-9. The direct tunneling current can be very large for thin films.

Poole-Frenkel (P-F) model is trap-assist conduction. The traps are generated in the film and electrons hop on them. Figure 2-11 shows the model of P-F conduction. The P-F conduction current density is given by

$$J \sim \varepsilon \exp\left[\frac{-q(\phi_B - \sqrt{q\varepsilon/\pi\varepsilon_i})}{kT}\right] \sim V \exp(+2a\sqrt{V}/T - q\phi_B/kT)$$

P-F conduction is as a function of temperature, and then P-F plot depends on thermal characteristics. The depth of trap is calculated from the slope of P-F plot.

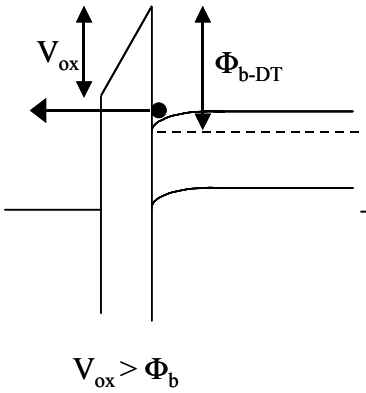


Fig. 2-9 Direct tunneling

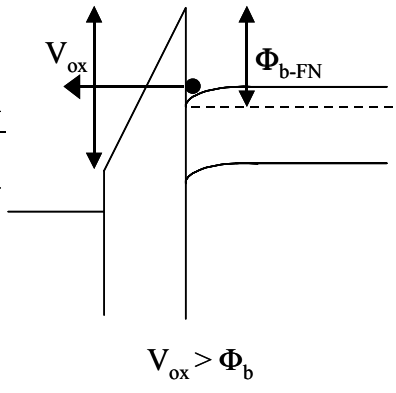


Fig. 2-10 F-N tunneling

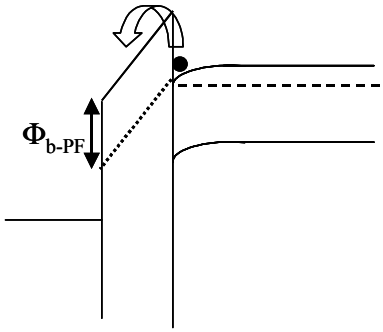


Fig. 2-11 P-F model

2.2.3 X-ray Photoelectron Spectroscopy (XPS)

XPS, also known as Electron spectroscopy for chemical analysis (ESCA) is one of the availability methods that estimate thin film and Si interface.

Figure 2-12 show the schematic drawing of XPS equipment (PHI5600) that was used in this study. During analysis, the pressures of main chamber were about 10^{-9} Torr vacuums with turbo pomp. Surface analysis by XPS is accomplished by irradiating a sample with monoenergetic soft X-ray and analyzing the energy of the detected electrons. Non-monochromatic Mg Ka (1253.6 eV) X-ray is used in this study. The method is illustrated with the energy band diagram in Fig. 2-13. This photon has limited penetrating power in a solid on the order of 1-10 μm. They interact with atoms in the surface region, causing electrons to be emitted by the photoelectric effect. The emitted electrons have measured kinetic energies given by

$$KE = h\nu - BE - \phi_s$$

where hυ is the energy of the photon, BE is the binding energy of the atomic orbital from which the electron originates and ϕs is the spectrometer work function (4.8 eV).

The binding energy may be regarded as the energy difference between the initial and final states of the ion from each type of atom, there is a corresponding variety of kinetic energies of the emitted electron. Because each element has a unique set of binding energies, XPS can be used to identify and determine the concentration of the elements in the surface. Variation in the elemental binding energies (Chemical shift) arises from difference in the chemical potential and polarizability of compounds. These chemical shifts can be used to identify the chemical states of the materials being analyzed.

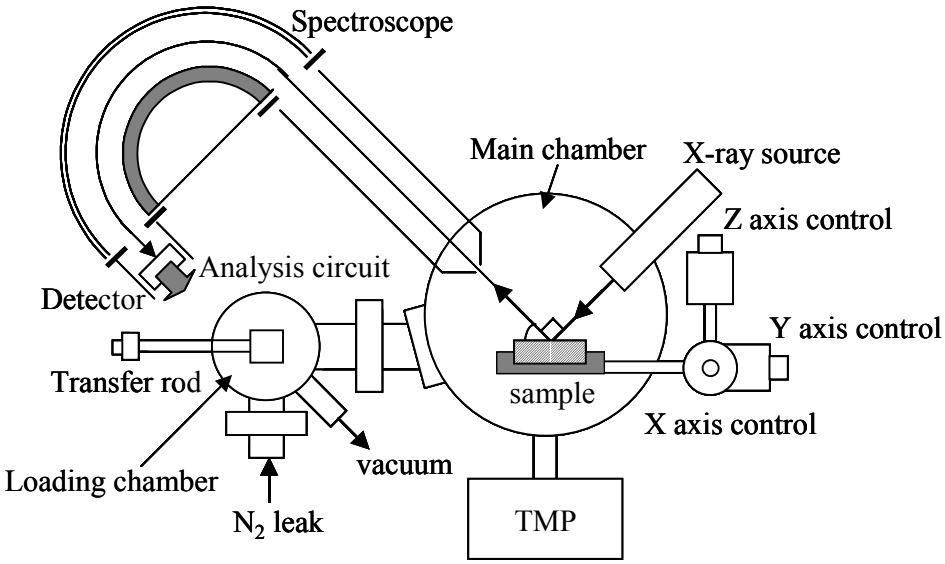


Fig. 2-12 XPS equipment

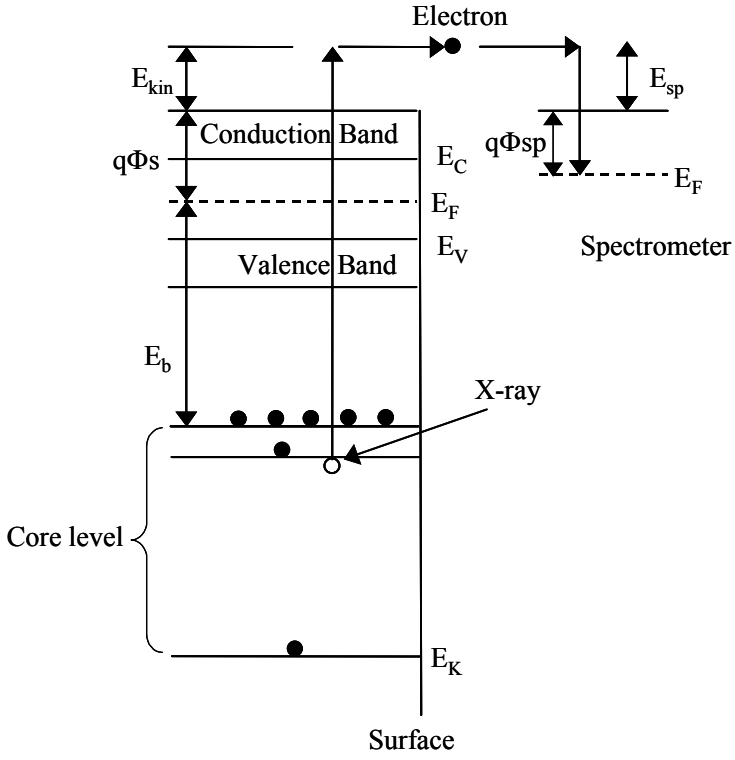


Fig. 2-13 Energy band diagram

To obtain the details of chemical binding of Si interface, we calculated to spin cut for $Si2p_{1/2}$ component. The theory of spin cut of Si $2p_{1/2}$ was as follow.

The measurement wave defined to

$$y(v) = x_1(v) + x_3(v) = Ax_3(v + \Delta v) + x_3(v) \qquad (1)$$

where $x_1(v)$: Si $2p_{1/2}$ spectra, $x_3(v)$: Si $2p_{3/2}$ spectra

A ：Intensity rate of $Si2p_{3/2}$ /$Si2p_{1/2}$=0.498 (reported)

Δv ：The shift of peak position is 0.608 eV (reported)

Then Fourier transform for formula (1) was shown in

$$Y(\omega) = Ae^{j\omega\Delta v} X_3(\omega) + X_3(\omega) = (1 + Ae^{j\omega\Delta v})X_3(\omega) \qquad (2)$$

Considered to formula (3) using delta function $\delta(v)$

$$d(v) = A\delta(v + \Delta v) + \delta(v) \qquad (3)$$

and, Fourier transform for formula (3) was shown in

$$D(\omega) = Ae^{j\omega\Delta v} + 1 = A\cos(\omega\Delta v) + 1 + j\sin(\omega\Delta v) \qquad (4)$$

Formula (2) divided to formula (4), and calculating to Fourier inversion transform, it was obtained only $x_3(v)$ component.

$$\frac{Y(\omega)}{D(\omega)} = \frac{(1 + Ae^{j\omega\Delta v})X_3(\omega)}{1 + Ae^{j\omega\Delta v}} = X_3(\omega) \qquad (5)$$

Figure 2-14 shows the one example of spin cut. This spectrum was measured for the HF-last Si substrate.

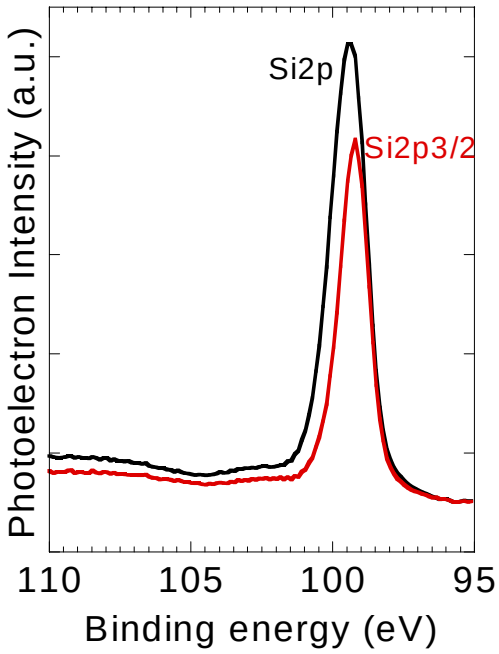


Fig. 2-14
Spin cut of Si2p spectra

2.2.4 Atomic Force Microscopy (AFM)

The observations of surface roughness are using tapping mode AFM (AFM, Nano Scope III, Digital Instrument Co. Ltd.).

Tapping mode AFM (TM-AFM) enables to measure surface morphology in high resolution depended on size of cantilever. In this study, the resolution limit is below 1 nm. Figure 2-15 shows the principle of AFM. As the sample approaches the cantilever and the distance between them becomes a certain value, cantilever is vibrated and scanning images of surface. An image of the surface is obtained by the scanning in x and y directions.

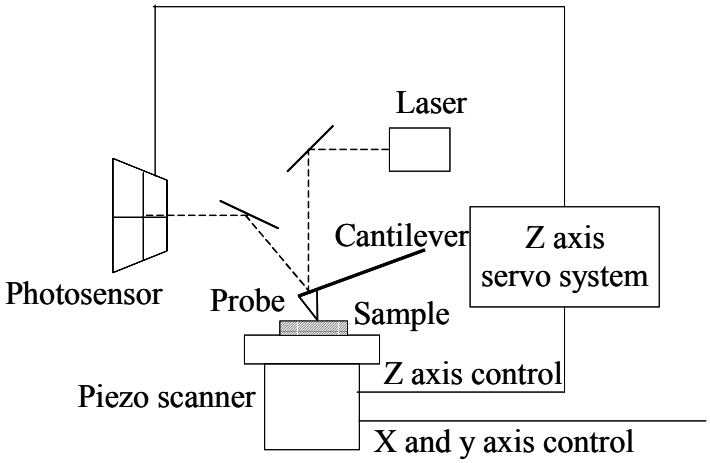


Fig. 2-15 principle of AFM

2.2.5 Ellipsometry

Ellipsometry is used predominantly to measure the thickness of thin dielectric films on highly absorbing substrates but can also be used to determine the optical constants of films or substrates.

Figure 2-16 shows the plane-polarized light incident on a plane surface. The incident polarized light can be resolved into a component p, parallel to the plane of incidence and a component s perpendicular to the plane of incidence. The light propagates as a fluctuation in electric and magnetic fields at right angles to the direction of propagation. The reflection coefficients

$$R_p = \frac{E_p(reflected)}{E_p(incident)}$$

$$R_s = \frac{E_s(reflected)}{E_s(incident)}$$

are not separately measurable. However, the complex reflection ratio ρ defined in terms of the reflection coefficients R_p and R_s or ellipsometric angles ψ and Δ

$$\rho = \frac{R_p}{R_s} = \tan(\psi)e^{j\Delta}$$

is measurable. Then, ψ and Δ are called ellipso parameter.

For the air(n_0)-thin film(n_1)-substrate(n_2-jk_2) substrate system, where n_x is the index of refraction and k_x the extinction coefficient. In case of Si substrate, n_2 and k_2 are known, then n_1 and film thickness may be calculated from the result of ψ and Δ measurement.

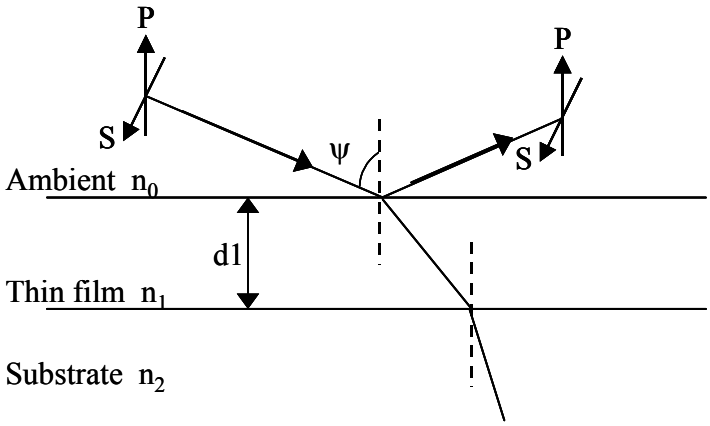


Fig. 2-16 principle of Ellipsometry

2.2.6 X-Ray Diffraction (XRD)

XRD was used for crystalline evaluation of deposited films.

X rays diffract in crystal lattice when the azimuth angle meets Bragg diffraction condition. Bragg diffraction condition is represented as follows:

$$2d\sin\theta = n\lambda$$

where, d is the distance of lattice planes, θ is the angle of incidence, n is a integer number, and λ is the wavelength of incidence X rays.

X rays source is Cu. The wavelength of specific X rays is as follows:

K α1: 0.15443 nm

K α2: 0.15405 nm

K β : 0.13922 nm

2.2.7 Transmission Electron Microscopy (TEM)

Cross-sectional TEM image is the most important analysis method to characterize physical thickness, film quality and interface condition.

Figure 2-17 shows TEM system. First, focus lenses change convergent angle and beam size. The electron beam transmitted through the thin fragment sample passes objective lens and projective lens, and finally projected on fluorescent screen. Recording of the image is performed by direct exposure on exclusive film for electron microscope set lower part of the fluorescent screen.
Electron interacts strongly with lattice by scattering. Thus, sample has to be very thin fragment. Required thickness of the sample is 5 – 500 nm at 100 kV. TEM images are obtained in very high resolution such as 0.2 – 0.3 nm at 200 kV.

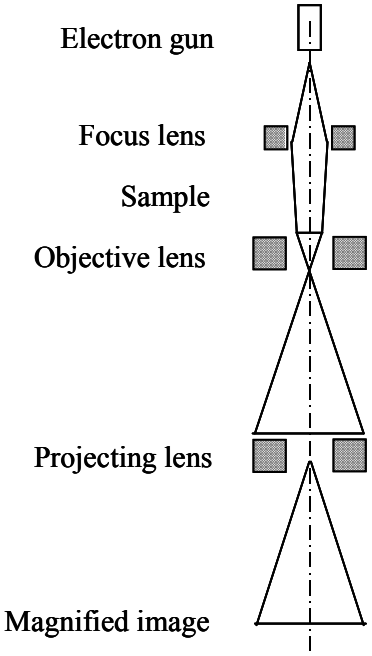


Fig. 2-17 TEM system

Chapter 3
Characterization of MIS Capacitor

3.1 Introduction

In this chapter, we will investigate the conventional characteristics for MIS capacitor using rare earth oxide. In this study, we investigated Yb_2O_3 and Gd_2O_3.

3.2 Fabrication process of MIS capacitor

The fabrication processes of MIS capacitor using rare earth oxides are as follows. In this study, we investigated the optimization of annealing condition, and obtain amorphous film.

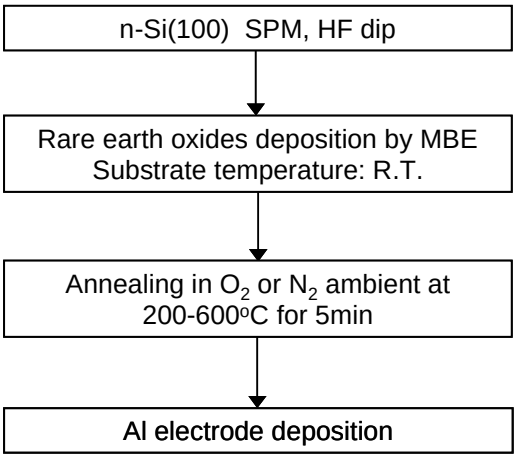


Fig.3-1 Fabrication process of MIS capacitor

3.3 Characterization of Al/Yb_2O_3/n-Si (100) structure

3.3.1 Physical properties of Yb_2O_3

Ytterbium oxide (Yb_2O_3) is one of the rare earth oxides that have middle band gap (4.8 eV) and high lattice energy (-13814 kJ/mol) shown in Fig. 3-2. The dielectric constant of Yb_2O_3 was reported 11, and it exhibits monoclinic structures (Table 3-1). As Yb_2O_3 has high lattice energy, it anticipates that the film is easy to crystallize. Recently, the result of Yb_2O_3 for high-k gate insulator has been reported. The report was shown as follow.

Kadoshima et al. studied Yb_2O_3 films formed on Si substrate using MOCVD. The film crystallized above 330°C formation, the dielectric constant of the film without interfacial layer was about 6. After annealing, further reactions result in the formation of Yb-silicate interfacial layer. At high temperature formation and annealing, C-V characteristic was improved and dielectrics of the film was about 10.

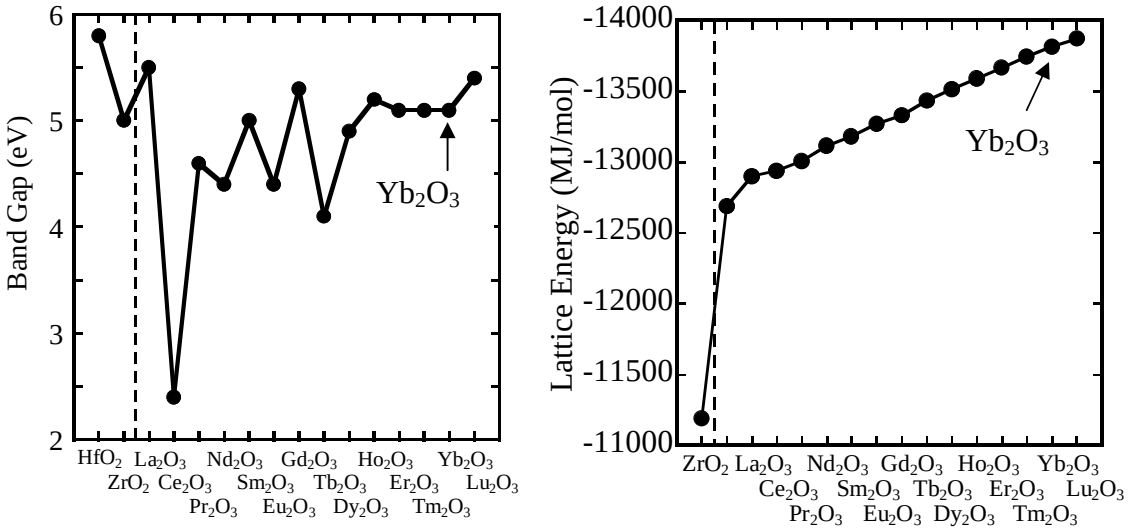


Fig.3-2 (a) Bad gap (b) Lattice energy

Crystal Structure	Lattice Constant (nm)			(º)
	A	B	c	β
Monoclinic	1.373	0.3425	0.8452	100.17

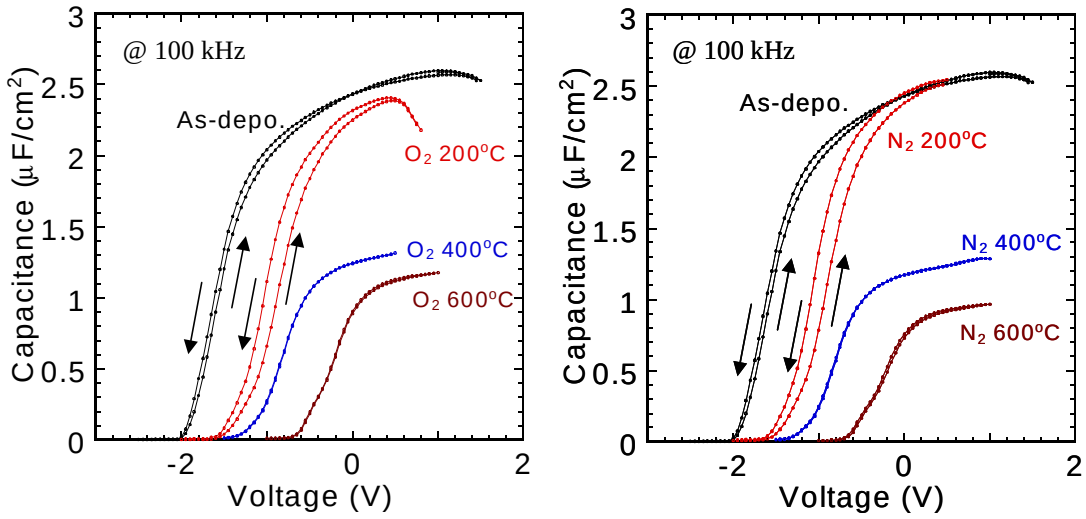
Table 3-1 Crystal structure of Yb_2O_3

3.3.2 Characterization of Yb_2O_3 thin films

In the reported result, Yb_2O_3 film was easy to crystallize at high temperature deposition, so that in this subsection, R.T. deposition Yb_2O_3 film will investigate.

The first, effect of the annealing condition was investigated for the 5.0 nm-thick Yb_2O_3 film was deposited at R.T..

Figure 3-3 shows C-V characteristics with annealing temperature as a parameter, the annealing in O_2 and N_2 ambient and annealing time was 5 min. The measurement frequency was 100 kHz. The as-deposited film was observed small hysterisis (50 mV), while after annealing O_2 and N_2 at 200^{o}C; hysterisis became large (150 mV). The direction of hysteresis curve, the hysteresises are caused by ion drift. As-deposited film obtained high accumulation capacitance and small CET value (1.3 nm), however, the flat band shift was very large. As Al electrode for n-Si, ideal flat band voltage is about +0.2 V, however the flat band voltage of this sample calculated from C-V curve was –1.9 V. The negative flat band shift was about 1.6 V. It was considered that many positive fixed charges exist at the interface. When the films were annealed at higher than 200^{o}C, the accumulation capacitance decreased and CET increased (from 1.4 to 3.6 nm) with during the annealing from 200-600^{o}C. This was because of the growth of low dielectric interfacial layer during the annealing. However, the interface conditions were significantly improved by the post-deposition anneal, because the negative flat band shift decreased while annealing temperature increased. And the hysteresis became negligibly small with annealing at higher than 400^{o}C.



(a) O_2 anneal (b) N_2 anneal

Fig.3-3 C-V characteristics with annealing temperature as a parameter

Figure 3-4 shows C-V characteristics for the O_2 400°C annealed sample with frequency as a parameter, the measurement frequency was 1 MHz, 100 kHz, 10 kHz and 1 kHz. It observed that there was large frequency dependence at accumulation and depletion regions. This fact was appeared another annealing conditions.

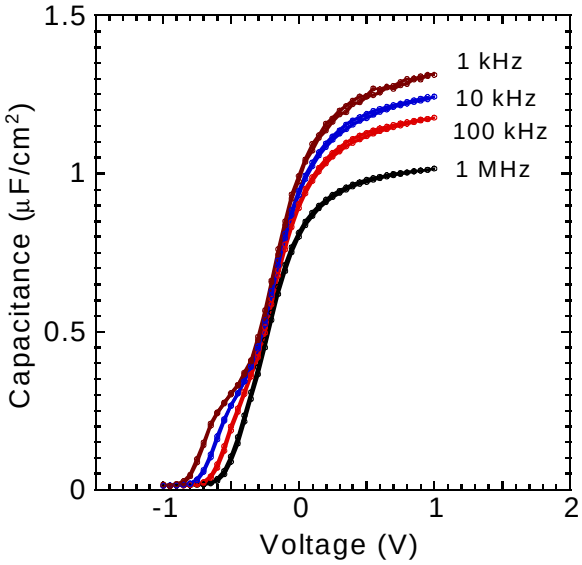
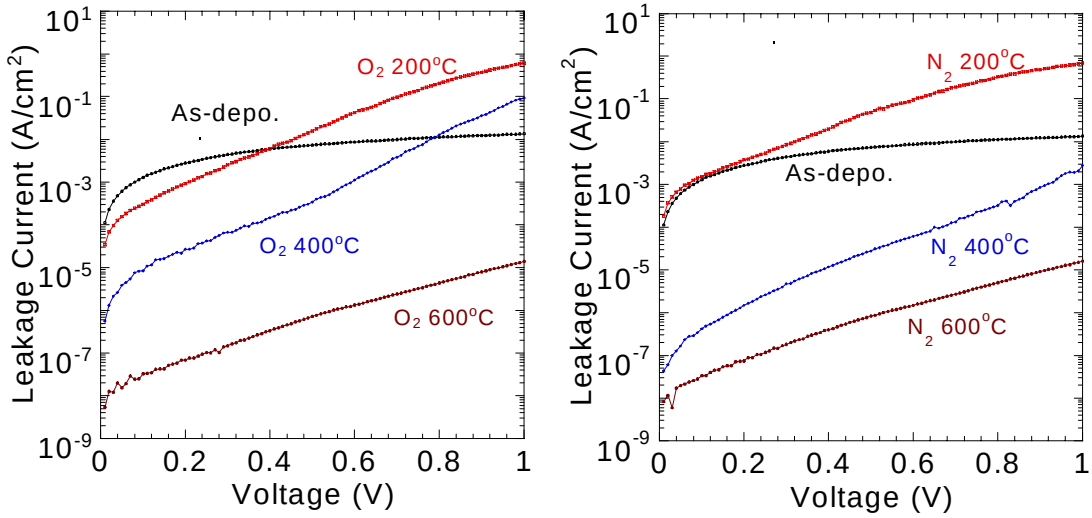


Fig.3-4 C-V characteristics with frequency as a parameter

Figure 3-5 shows J-V characteristics for the same samples. With increase of annealing temperature, leakage current densities decreased significantly, both O_2 and N_2 annealed samples. The leakage current for 600°C annealing sample decreased more than 3 orders magnitude from that for 200°C annealing sample (from 6.0×10^{-1} to 1.4×10^{-5} A/cm^2 @ +1 V).



(a) O_2 anneal (b) N_2 anneal

Fig.3-5 J-V characteristics with annealing temperature as a parameter

Figure 3-6 shows the AFM images and root mean square (RMS) of surface for the O_2 annealing samples. The scan size was 0.5x0.5 μm and the z direction was 5 nm/div. The as-deposited film was observed smooth surface (RMS: 0.062 nm). However, after annealing sample, large roughness was observed, RMS values were about 0.7-0.8 nm, though annealing temperature was different. In case of N_2 annealing, the same result was observed. It was considered that annealing in O_2 or N_2 were crystallized the film. Unfortunately, there was not carry out the XRD measurement or Reflective High Energy Electron Diffraction (RHEED) observation, so the films were crystallization or not have not found yet.

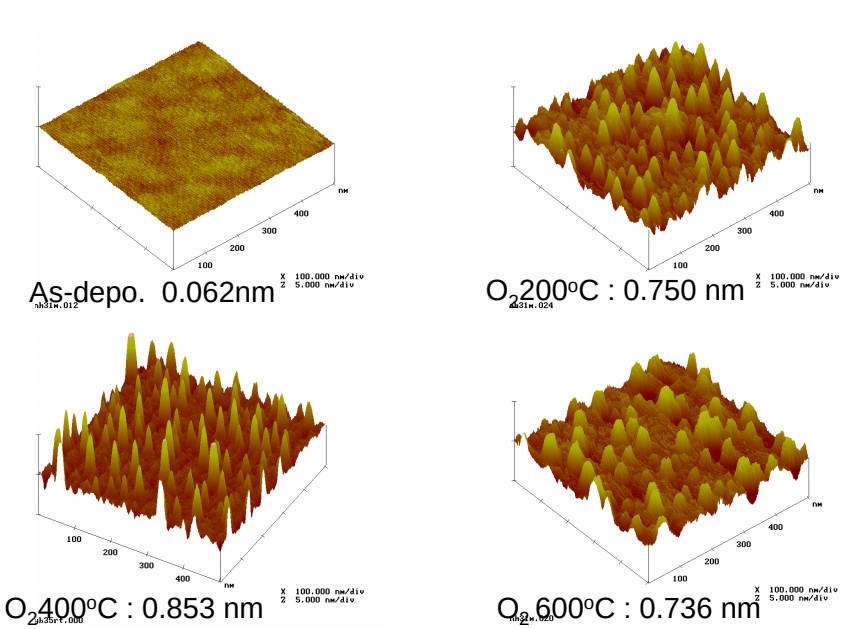


Fig.3-6 AFM images with annealing temperature as a parameter

A TEM image of the O_2 400°C-annealing sample is shown in Fig. 3-7. In this figure, the physical thickness of this film was about 5 nm and kept in the amorphous state even after annealing. There was thin the interfacial layer at Yb_2O_3/Si interface, though accumulation capacitance was not decreased. At Al/Yb_2O_3 interface, the surface roughness and a little interfacial layer growth were observed. As the post-metal anneal did not carry out, it is not found when the interfacial layer was growth.

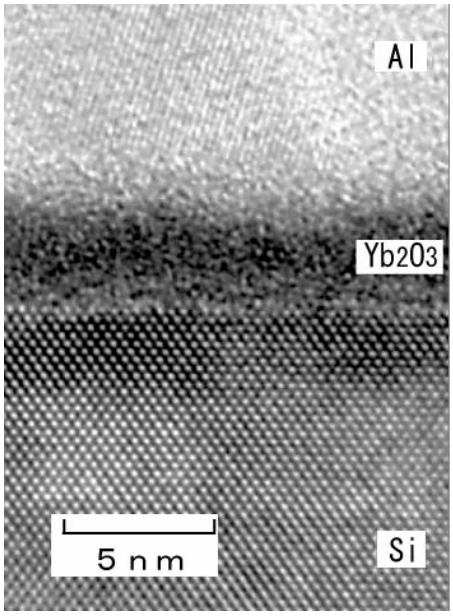


Fig.3-7 TEM image of the O_2 400°C-annealing

3.4 Characterization of Al/Gd_2O_3/n-Si (100) structure

3.4.1 Physical properties of Gd_2O_3

Gadolinium oxide (Gd_2O_3) is one of the rare earth oxides that have high band gap (5.4 eV) and middle lattice energy (-13330 kJ/mol) shown in Fig. 3-8. The dielectric constant of Gd_2O_3 was reported 8-20, and it exhibits two different crystal structures that are cubic and monoclinic (Table 3-2). Among the rare earth oxides, cubic Gd_2O_3 has one of the closest lattice matches to Si, where a(Gd_2O_3)=10.812 Å 2a(Si)=10.862 Å. Thermodynamic calculations, Gd_2O_3 is stable in contact with Si at 1000 K.

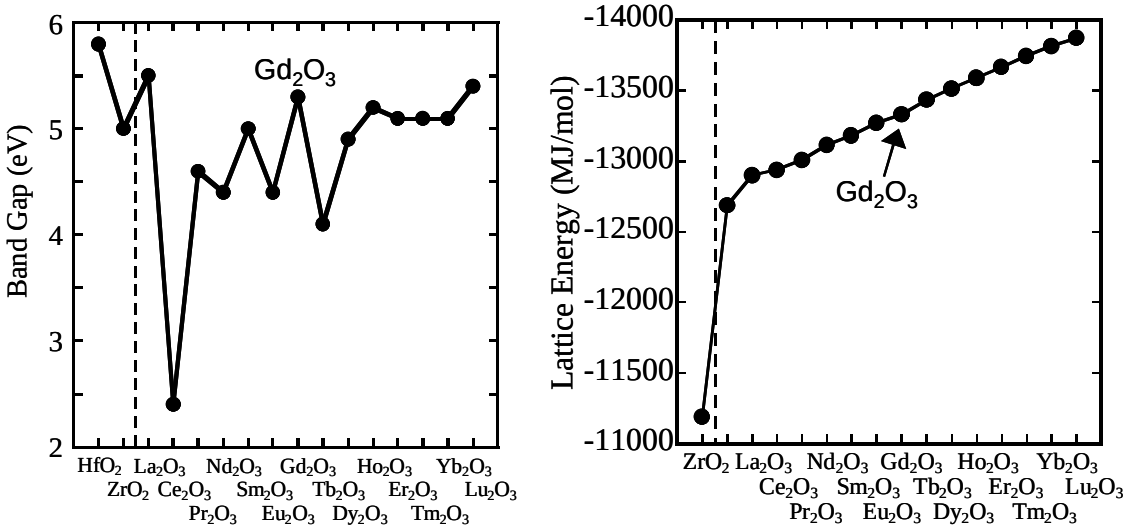


Fig.3-8 (a) Bad gap (b) Lattice energy

Crystal Structure	Lattice Constant (nm)			(º)
	A	B	c	β
Monoclinic	1.4061	0.3566	0.8760	100.10
Cubic	1.0813			

Table 3-2 Crystal structure of Gd_2O_3

Recently, some results of Gd_2O_3 and Gd-silicate for high-k gate insulator have been reported. Some excellent reports were shown as follows.

Chen et al. studied Gd and $GdSi_{2-x}$ films deposited on Si(111) and subsequently annealed in O_2. A complicated multilayer structure was found for the oxidized Gd films, while the annealed $GdSi_{2-x}$ films appeared to form a uniform silicate layer, separated from the substrate by thin oxide layer.

Kwo et al. demonstrated the growth of Gd_2O_3 films with properties suitable for gate insulator applications. Their samples exhibited three distinct structures: crystalline films deposited at 550°C having a two-fold symmetry, or single domain structure and amorphous films deposited on exact substrates at 10°C. Although the measured dielectric constant of a 196 Å-thick film was as high as 20, a 34 Å-thick film had a only 9.

Gupta et al. studied Gd_2O_3 films deposited on Si(001) substrate using electron-beam evaporation from pressed-powder target. The dielectric constant of Gd_2O_3 is about 16. After annealing in O_2, further reactions result in the formation of a three-layer structure consisting of a distinct SiO_y layer at the interface, a mixed $(SiO_2)_x(Gd_2O_3)_{1-x}$ layer and stoichiometric Gd_2O_3 layer at the top surface (Fig. 3-9). The as-deposited films exhibited high leakage currents, and that the interfaces were significantly improved by the post-deposition anneal. The dielectric constant of the film is significantly reduced, however, due to the formation of low dielectric constant material at the interface.

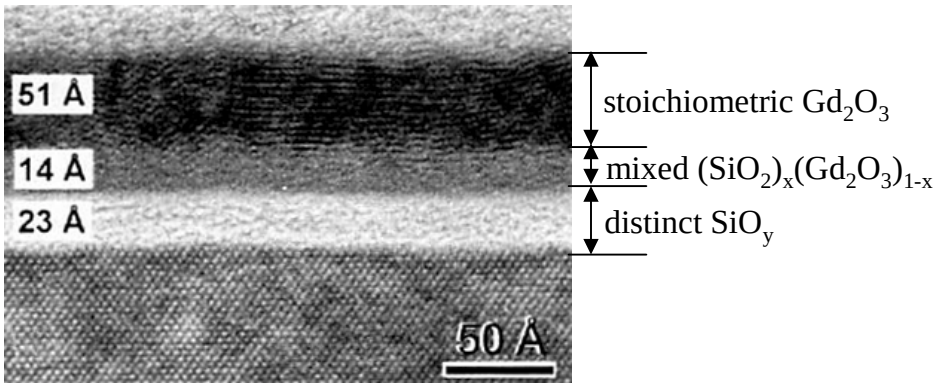
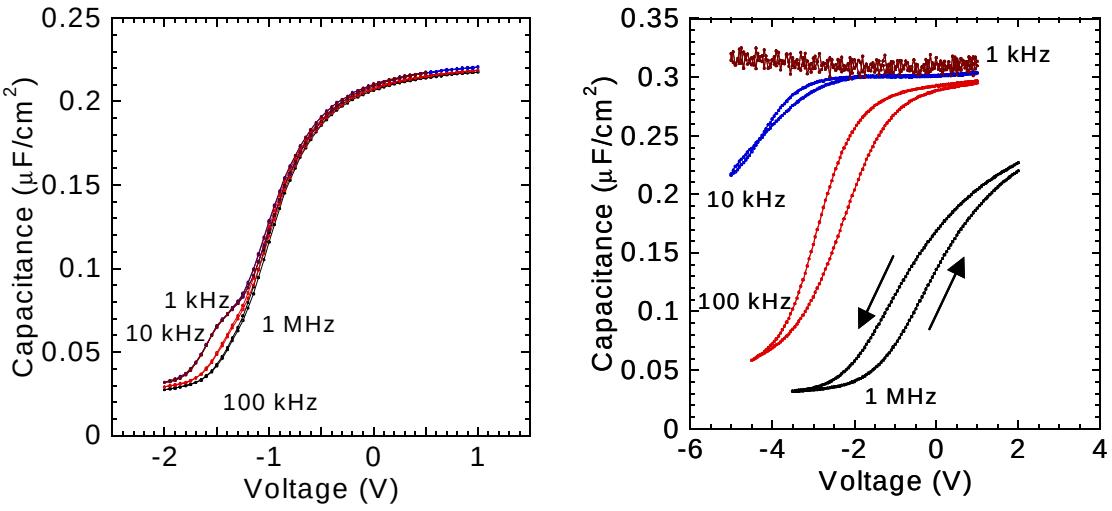


Fig. 3-9 Cross sectional TEM image for Gd_2O_3 film deposited at 500°C on Si(100) and annealed 10 min in O_2 at 700°C.

3.4.2 Characterization of Gd_2O_3 thick films

In the reported result, Gd_2O_3 films have high dielectric constant and have been studied as promising candidates. To investigate the physical properties of Gd_2O_3 film, thick Gd_2O_3 films deposited and analyzed.

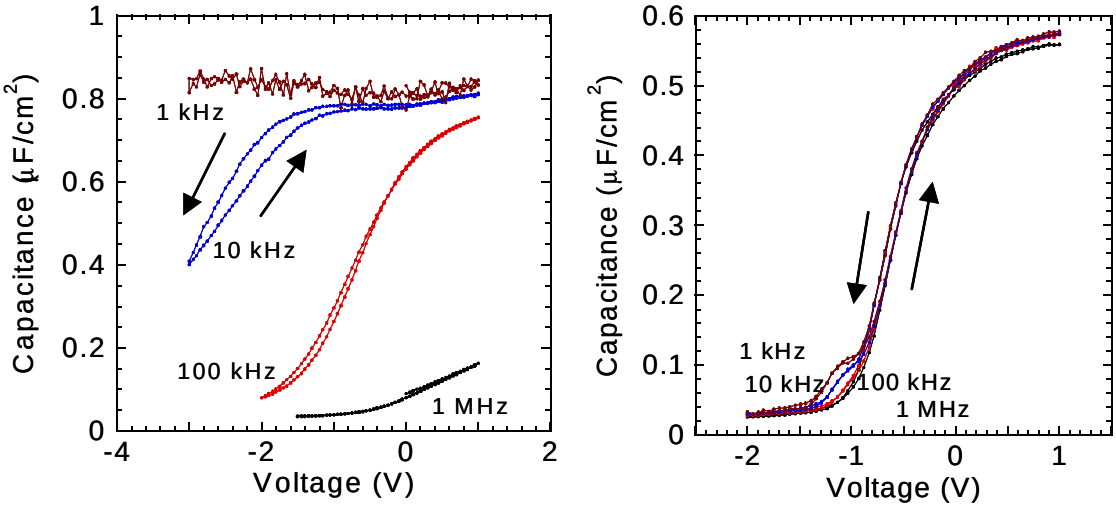
Figure 3-10 shows the C-V characteristics for 53 nm-thick Gd_2O_3 films before and after annealing. The annealing condition was O_2 400°C for 5 min. As-deposited sample showed strange C-V curve and large frequency dependence. The direction of hysteresis curve, the hysteresises were caused by ion drift. After annealing, the C-V curve got well figure and there was a little frequency dependence was observed at depletion region. CET value of annealed sample was 15.7 nm, and the dielectric constant of the film that calculated from accumulation capacitance was about 13.



(a) O_2 400°C 5 min (b) As-depo.

Fig. 3-10 C-V characteristics for 53 nm-thick Gd_2O_3 films

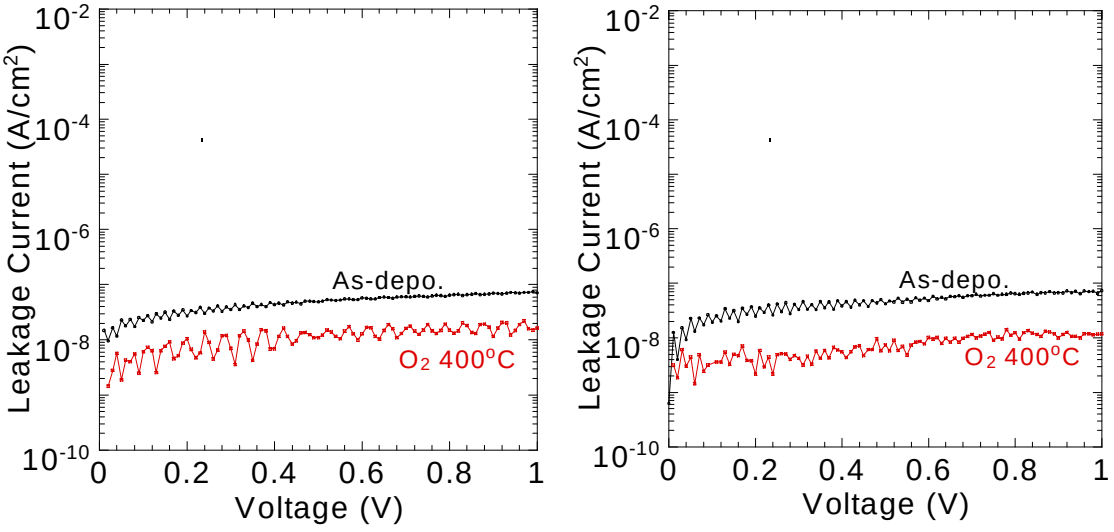
Figure 3-11 shows the C-V characteristics for 24 nm-thick Gd_2O_3 films before and after annealing. The C-V characteristics for these films were almost the same behavior the film that physical thickness was 53 nm. CET value of annealed sample was 6.2 nm, and the dielectric constant of the film that calculated from accumulation capacitance was about 16. These dielectric constant was the almost the same value for the reported data (8-20).



(b) As-depo. (a) O_2 400°C 5 min

Fig. 3-11 C-V characteristics for 24 nm-thick Gd_2O_3 films

Figure 3-12 shows J-V characteristics for these samples. As the thick film, the leakage current was very low (about 10^{-8} A/cm^2) for all samples.



(a) 53 nm-thick films (b) 24 nm-thick films

Fig. 3-12 J-V characteristics for 53 and 24 nm-thick Gd_2O_3 films

For gate insulator, the film state is the important parameter, in order to analyze crystallization, XRD measurement and AFM observation carried out.

Figure 3-13 shows XRD pattern for thick Gd_2O_3 films (Physical thicknesses were 53 and 24 nm). XRD pattern of as-deposited samples were amorphous for both 53 nm and 24 nm cases. After the annealing, 53 nm sample exhibits a peak near $2\theta=28.6^{o}$. The peak corresponds to the crystal of cubic (222) Gd_2O_3. However, this peak was not observed for the 24 nm film. Thus, we estimated that the Gd_2O_3 films with thickness less than 24 nm kept in the amorphous state even after annealing.

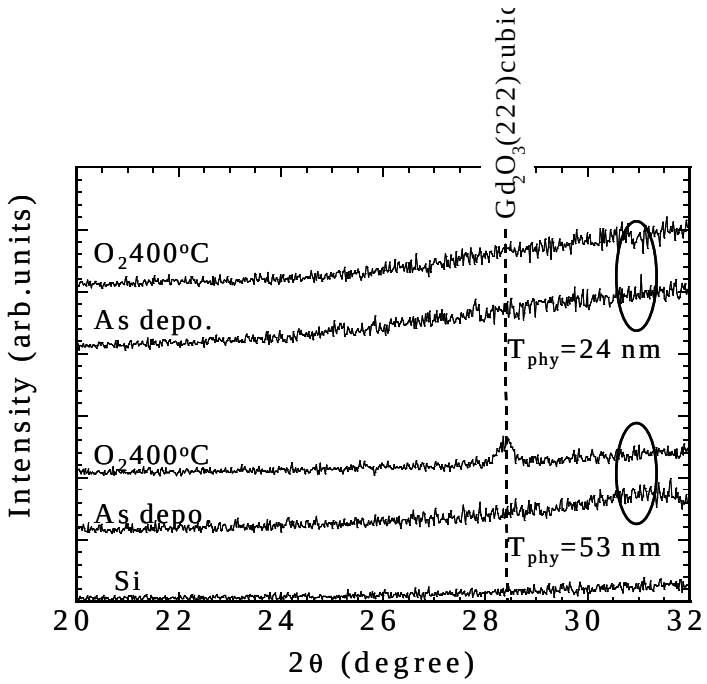
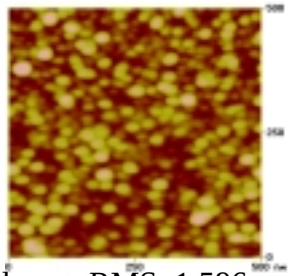
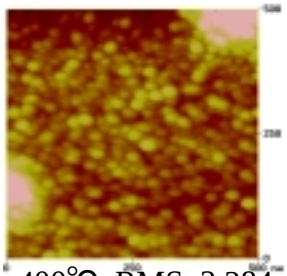


Fig. 3-13 XRD pattern for 53 and24 nm-thick Gd_2O_3 films

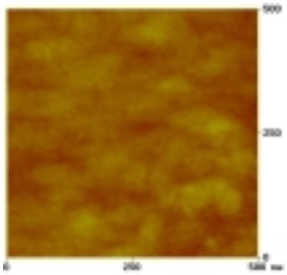
Figure 3-14 shows the AFM images for these samples. In case of 53 nm-thick films, for as-deposited sample, many small peaks were observed at the surface (RMS: 1.6 nm). After annealing, some large grain was observed (RMS: 3.3 nm). It was considered that small peaks gathered and made same grain for annealing, the crystallization was caused these grains. On the other hand, in case of 24 nm-thick films, the surface was smooth for as-deposited samples (RMS: 0.17 nm), however, the surface roughness was observed after annealing (2.6 nm). From the XRD result, 24 nm-thick film kept amorphous state, so the reason for the large roughness has not found.



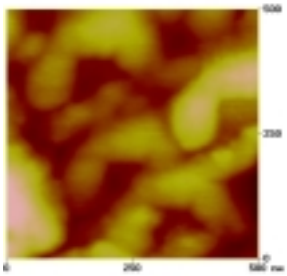
As depo. RMS: 1.596 nm



O_2 400℃ RMS: 3.284 nm



As depo. RMS: 0.174 nm



O_2 400℃ RMS: 2.585 nm

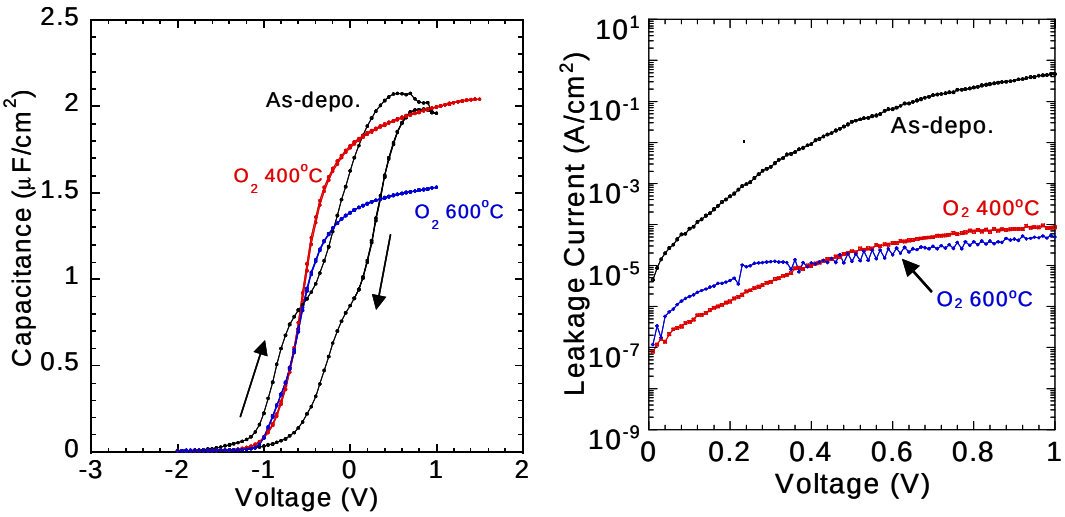
Fig. 3-14 AFM images for 53 and 24 nm-thick Gd_2O_3 films

3.4.3 Characterization of Gd_2O_3 thin films

In the previous subsection, we discussed thick Gd_2O_3 films, however, for high-k gate insulator, we will use thin film below 10 nm. We estimated that below 24 nm Gd_2O_3 film keeps in the amorphous state. Thus, in this subsection, we will investigate the amorphous Gd_2O_3 film below 5 nm.

The first, effect of the annealing condition was investigated for the 3.5 nm-thick Gd_2O_3 film was deposited at R.T..

Figure 3-15 shows C-V and J-V characteristics with annealing temperature as a parameter, the annealing in O_2 ambient and annealing time was 5 min. C-V characteristics were measured at 100 kHz. The as-deposited film was observed high leakage currents (0.46 A/cm^2) and large hysterisis (0.5 V), it was considered that the film and interface quality were not good because of without thermal process. The direction of hysteresis curve, the hysteresises are caused by charge trapping. The film and interface conditions were significantly improved by the post-deposition anneal that the suppressed leakage current and the hysteresis becomes negligibly small. When the films were annealed, the leakage current decreased while the accumulation capacitance decreased so that CET increased (from 1.7 nm to 2.3 nm). These results indicated that low dielectric constant interfacial layer was grown with during high temperature annealing in O_2 ambient. Considering that the MIS capacitor using Al electrodes for n-Si, flat band voltage in this plot suggest that the positive fixed charges exist at the interface.



(a) C-V characteristics (b) J-V characteristics

Fig. 3-15 3.5 nm-thick Gd_2O_3 film was deposited at R.T

Figure 3-16 shows C-V characteristics for the same film with frequency as a parameter, the measurement frequency was 1 MHz, 100 kHz, 10kHz and 1 kHz. It was observed large frequency dependence at accumulation capacitance for 1 MHz. It seems that the frequency dependence was caused by substrate doping density.

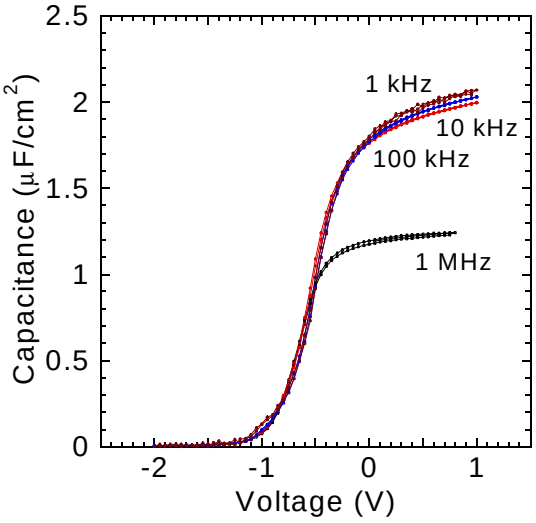


Fig. 3-16 3.5 nm-thick Gd_2O_3 film with frequency as a parameter

Figure 3-17 shows the AFM images and root mean square (RMS) of surface of the same film. The scan size was 0.5x0.5 μm and the z direction was 5 nm/div. The electrical characteristics were changed with annealing conditions, however, the surface roughness were not changed even after annealing. All the thin Gd_2O_3 films showed smooth surfaces and small RMS values (about 0.2 nm).

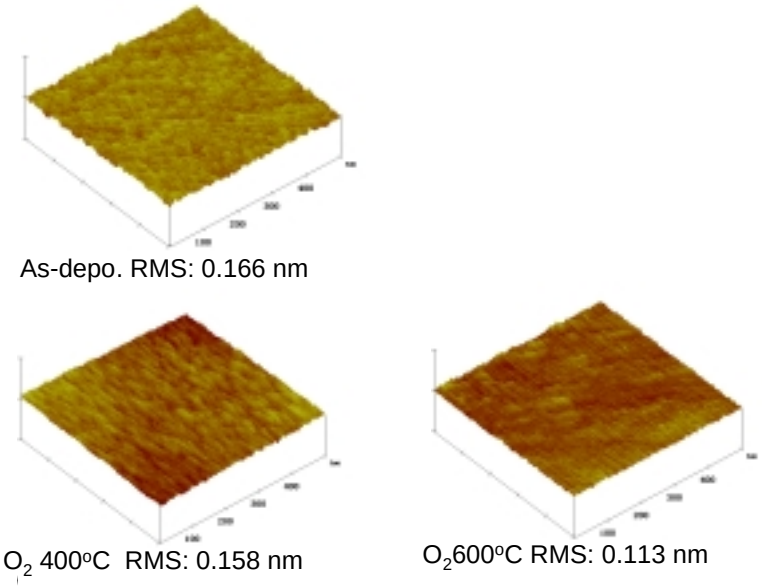


Fig. 3-17 AFM images for 3.5 nm-thick Gd_2O_3 film was deposited at R.T

3.5 Discussion

In this chapter, we investigated the conventional characteristics of MIS capacitor using rare earth oxides such as Yb_2O_3 and Gd_2O_3.

Yb_2O_3 indicated the interface conditions were significantly improved by the post-deposition anneal, because the negative flat band shift decreased while annealing temperature increased. And the hysteresis became negligibly small with annealing at higher than 400^{o}C. On the other hand, Gd_2O_3 did not indicate the fact.

Thick Gd_2O_3 film was crystallized by post-deposition anneal, however, thin Gd_2O_3 kept the amorphous state even after annealing. In case of Yb_2O_3, we did not carry out RHEED observation or XRD measurement, so the real state of Yb_2O_3 film has not found.

Chapter 4
Effect of Surface Treatment

4.1 Introduction

Surface treatment of Si substrate is the important method to obtain high quality interfacial layer.

In this chapter, we will discuss the effect of surface treatment for MIS capacitor using rare earth oxides, especially Gd_2O_3 and analyze electrical characteristics, surface and interface.

4.2 Fabrication of MIS capacitor

The fabrication processes of MIS capacitor using surface treatment Si substrates are as follows.

In this study, rare earth oxide was mainly Gd_2O_3 and annealing condition decided O_2 400^oC for 5 min.

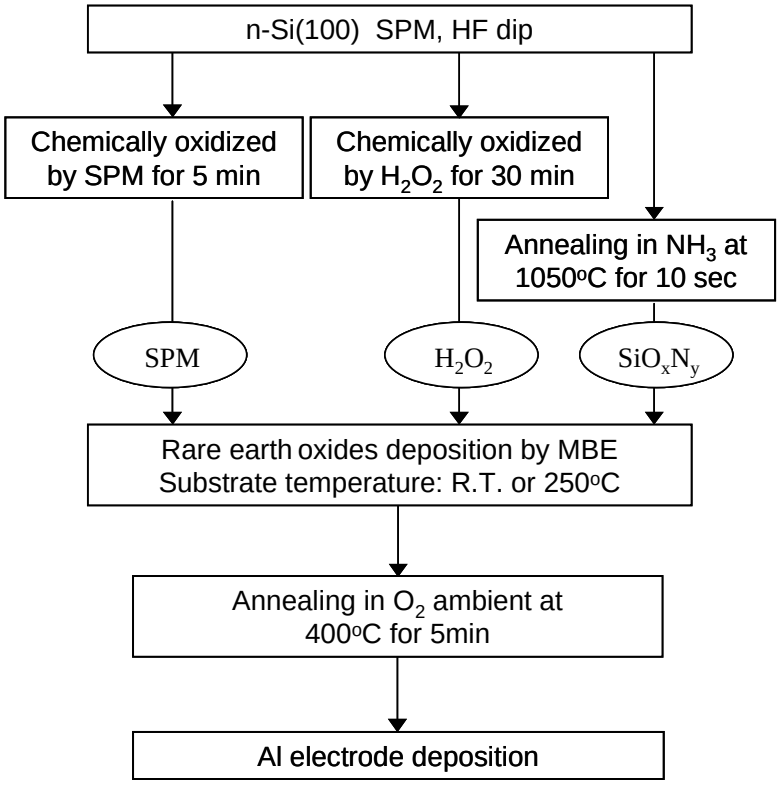


Fig.4-1 Fabrication process of MIS capacitor

4.3 Effect of surface treatment

4.3.1 Electrical characteristics

In this subsection, we will discuss the effect of surface treatment for electrical characteristics. 2.8 nm-thick Gd_2O_3 film was deposited at 250^{o}C, annealing in O_2 400^{o}C 5 min was used in this study.

Figure 4-2 shows the C-V characteristics for the HF-last sample, in this section HF-last sample's result decided to the initial characteristic for this film. The measurement frequency was 1 MHz, 100 kHz, 10kHz and 1 kHz. This sample was not observed frequency dependence. This sample obtained CET (1.7 nm) and interface state density ($3.6x10^{12}$ $eV^{-1}cm^{-2}$) was calculated by Terman method.

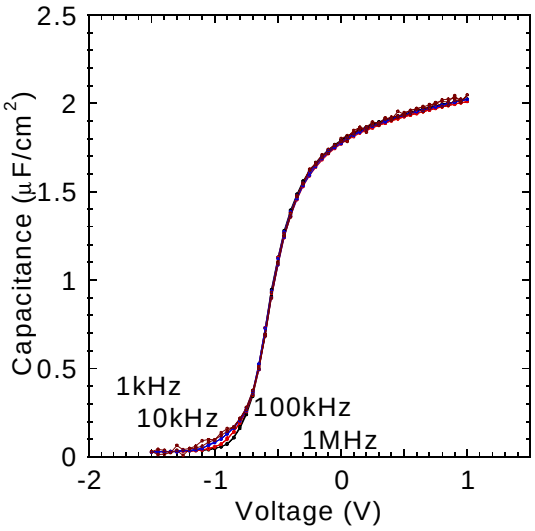
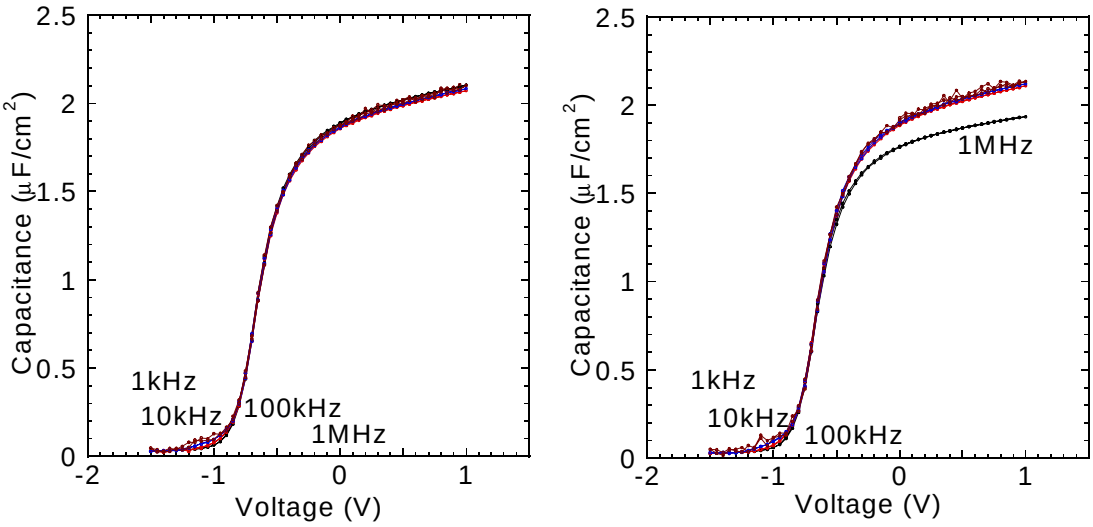


Fig.4-2 C-V characteristics for HF-last sample

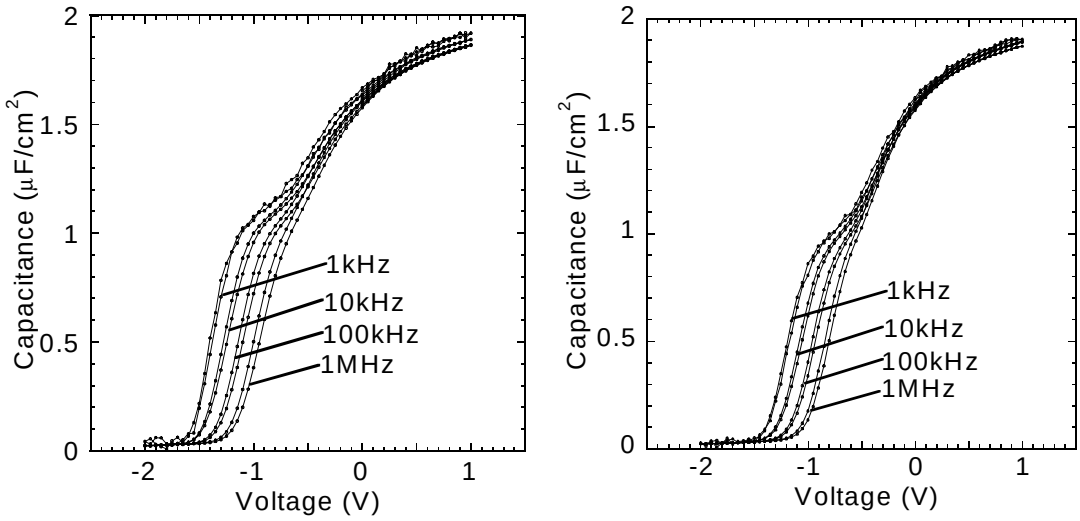
Figure 4-3 shows the C-V characteristics for the chemically oxidized sample. The measurement frequency was 1 MHz, 100 kHz, 10 kHz and 1 kHz. The sample using H_2O_2 solution was not observed frequency dependence. This sample obtained CET (1. 7 nm) and interface state density ($2.7x10^{12}$ $eV^{-1}cm^{-2}$) calculated by Terman method. In case of the sample using SPM solution was observed frequency dependence at accumulation capacitance for 1 MHz. This sample obtained CET (1.6 nm) and interface state density ($3.0x10^{12}$ $eV^{-1}cm^{-2}$) was calculated by Terman method.



(a) Using H_2O_2 solution (b) Using SPM solution

Fig.4-3 C-V characteristics for chemically oxidized sample

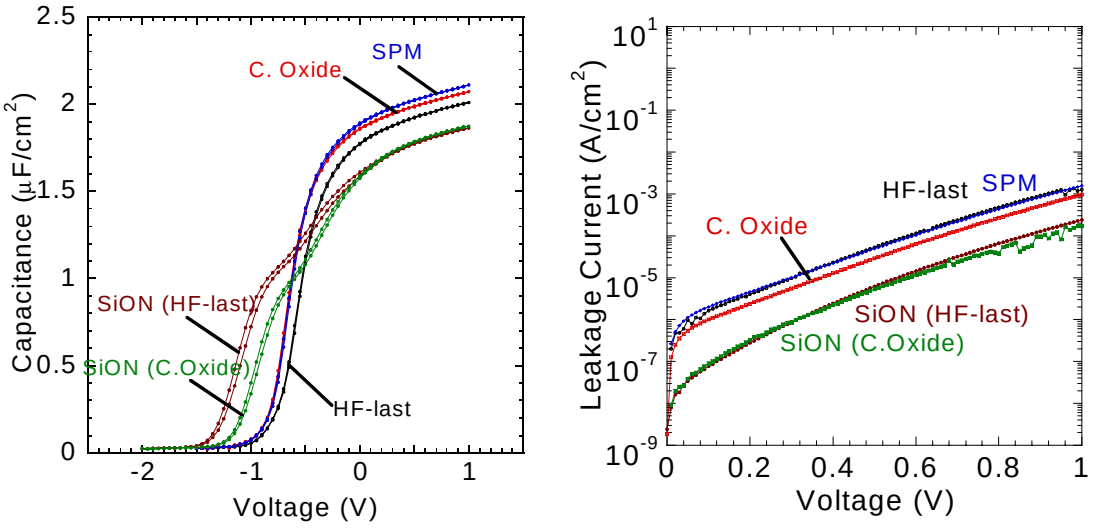
Figure 4-4 shows the C-V characteristics for the oxy-nitrided sample. The measurement frequency was 1 MHz, 100 kHz, 10kHz and 1 kHz. The sample using HF-last substrate was observed large frequency dependence at depletion region for all frequency. There was not observed the frequency dependence at accumulation capacitance. This sample obtained CET (1.9 nm) and interface state density (7.4×10^{13} $eV^{-1}cm^{-2}$) calculated by Terman method. In case of the sample using chemically oxidized substrate improved large frequency dependence at depletion region. This sample obtained CET (1.8 nm) and interface state density (5.4×10^{13} $eV^{-1}cm^{-2}$) was calculated by Terman method.



(a) Using HF-last substrate (b) Using chemically oxidized substate

Fig.4-4 C-V characteristics for oxy-nitrided sample

Figure 4-5 shows the C-V and J-V characteristics for all samples were measured at 100 kHz. In this figure, RTA did not form the high quality oxy-nitride interfacial layers, and thicker interfacial layers were formed compared to chemical oxide.



(a) C-V characteristics (b) J-V characteristics

Fig.4-5 C-V and J-V characteristics for surface treatment

Tale 4-1 shows the summery of electrical characteristics for surface treatments. In this result, it is difficult to obtain high quality oxy-nitride interfacial layer. At next subsection, the samples which have same CET value, will compared.

	HF-last	C. Oxide	SPM	SiO_xN_y (HF-last)	SiO_xN_y (C. Oxide)
CET (nm)	1.72	1.67	1.64	1.85	1.82
Leakage current density (A/cm^2) @ Vg=+1 V	$1.3x10^{-3}$	$9.7x10^{-4}$	$1.6x10^{-3}$	$1.7x10^{-4}$	$1.7x10^{-4}$
Interface state density ($eV^{-1}cm^{-2}$) (Terman method)	$3.6x10^{12}$	$2.7x10^{12}$	$3.0x10^{12}$	$7.4x10^{13}$	$5.4x10^{13}$

Table 4-1 Summery of electrical characteristics for surface treatments

4.3.2 Compared to same CET

In the previous subsection, we discussed the electrical characteristics for various surface treatments for 2.8 nm-thick Gd_2O_3 film. In this subsection, the films, which have same CET value, were compares to several analysis methods.

Figures 4-6 shows C-V characteristics for HF-last, chemically oxidized and oxy-nitrided Si substrate, respectively. The physical thickness of HF-last and chemically oxidized samples were 3.5 nm, and oxy-nitrided sample was 2.8 nm. They have almost the same CET value about 1.8 nm at 1 MHz. The C-V characteristics of the oxy-nitrided samples show significant distortion due to interface states as well as hysterisis. The direction of hysteresis, the hysteresises were caused by charge trapping. Figure 4-7 shows the plots of negative flat band shift and interface state density for HF-last, chemically oxidized and oxy-nitride samples. Negative flat band shift and interface state density of the oxy-nitrided samples were significantly larger than those have HF-last and chemically oxidized samples. This indicates the bad interfacial quality of the oxy-nitrided samples.

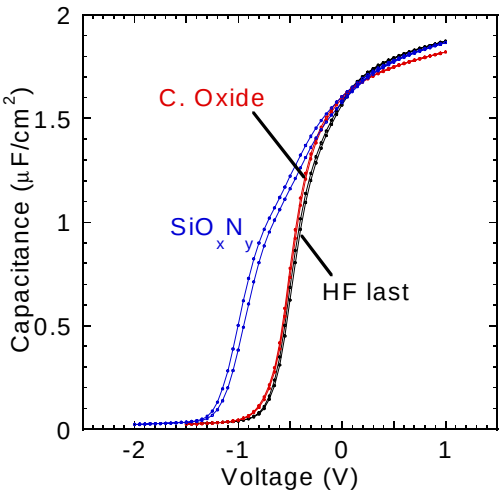


Fig.4-6 C-V characteristics

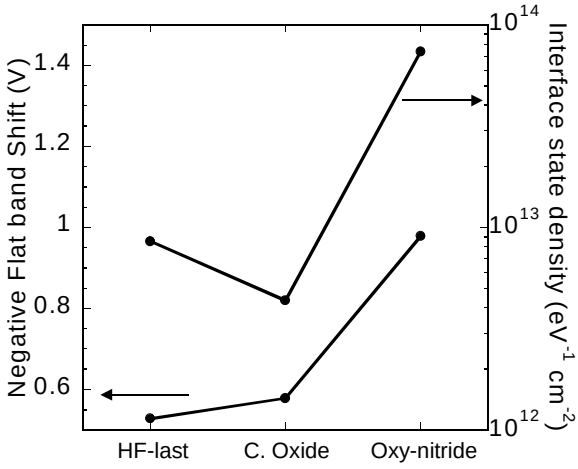
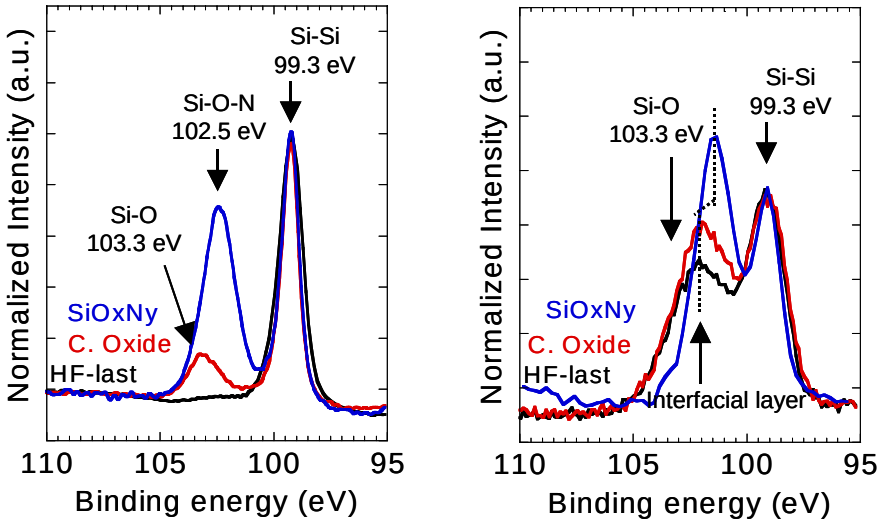


Fig.4-7 negative flat band shift and interface state density

Figure 4-8 show the XPS Si2p3/2 spectrum for these samples before and after depositions. Before deposition, peak position of chemical shift for chemically oxidized sample showed 103.3 eV, this position is corresponding to the stoichiometric SiO2 layer. And the chemical shift of oxy-nitrided sample was shown at 102.5 eV, this

peak maybe Si-O-N binding. The peak intensities rate of Si2p3/2 and Si-O binding for chemically oxidized sample indicated that the physical thickness of SiO_2 layer was 0.67 nm. In order to investigate the composition of oxy-nitride layer, peak separation for Si3/2 was carried out. From this result, the rate of oxygen and nitrogen binding with Si was about 1 to 1, and the physical thickness was 1.76 nm. On the other hand, after deposition, Si-O binding should be at 103.3 eV, however, chemical shifts were observed to lower binding energy for all samples. This result suggested that the Gd-silicate layer was formed at the interface during annealing. The chemical shift for oxy-nitrided sample showed large peak intensity at lower binding energy compare with HF-last and chemically oxidized samples. For oxy-nitrided sample, the S-O binding (103.3 eV) was not observed. It was considered that the defect of oxygen induced the degradation of interface condition.



(a) Before depo. (b) After depo.

Fig.4-8 XPS Si2p3/2 spectrum

Figure 4-9 shows J-V characteristics of the HF-last, chemically oxidized and oxy-nitrided samples. The Leakage current of chemically oxidized sample decreased compared to HF-last sample (from 1.0×10^{-2} to 6.0×10^{-6} A/cm^2 @ +1 V). Although, the quality of the oxy-nitrided layer is not good, the layer helps to suppress the leakage current (1.7×10^{-4} A/cm^2). The chemically oxidized shows better suppression of the leakage current than that of the oxy-nitride.

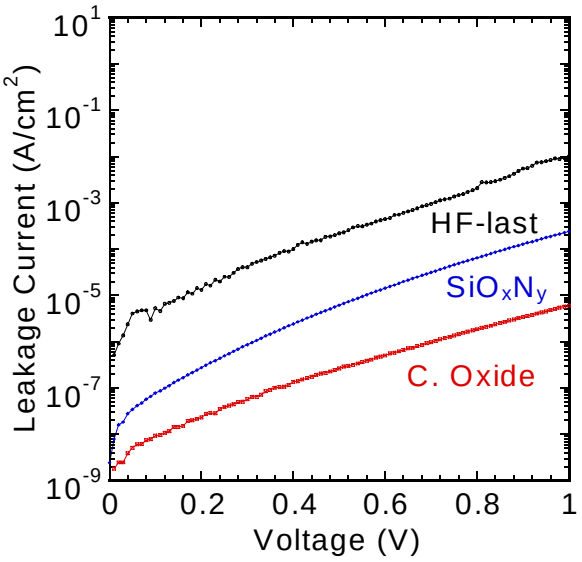


Fig. 4-9 J-V characteristics of the HF-last, chemically oxidized and oxy-nitrided samples

Tale 4-2 shows the summery of electrical characteristics for surface treatments. In this result, it is difficult to obtain high quality oxy-nitride interfacial layer, so we will analyze the detail for chemical oxide interfacial layer in the next chapter.

	HF-last	Chemical oxide	SiO_xN_y
CET (nm)	1.84	1.89	1.82
Leakage current density (A/cm^2) @ Vg=+1 V	$1.0x10^{-2}$	$6.0x10^{-6}$	$1.7x10^{-4}$
Interface state density ($eV^{-1}cm^{-2}$) (Terman method)	$8.2x10^{12}$	$4.4x10^{12}$	$5.4x10^{13}$

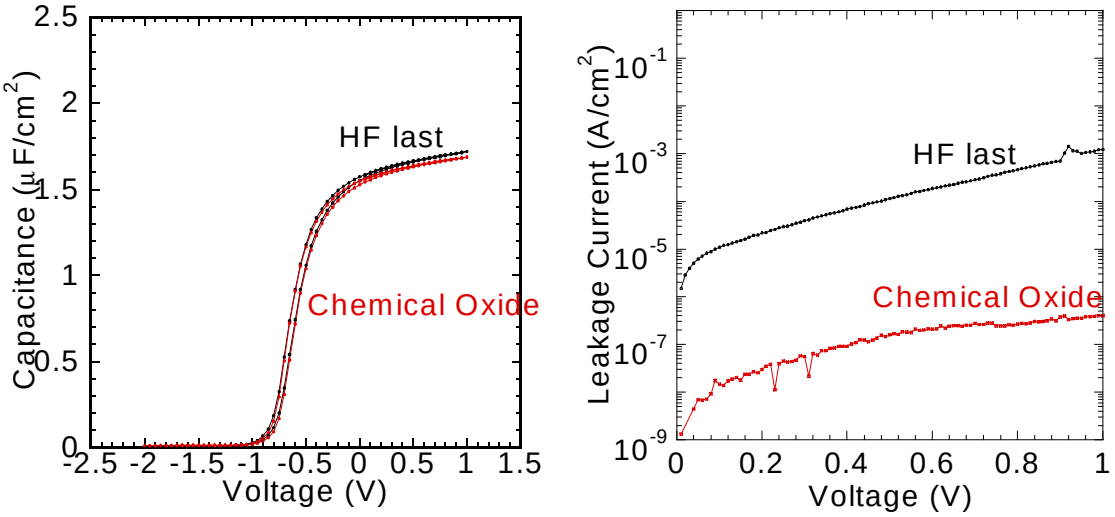
Table 4-2 Summery of electrical characteristics for surface treatments

4.4 Effect of chemical oxide (Gd_2O_3)

4.4.1 Electrical characteristics

The details of the effects of the chemically oxidized Si substrates were investigated.

Figure 4-10 shows C-V and J-V characteristics for 5.3 nm-thick on HF-last and chemically oxidized Si substrate. CET values were evaluated for the HF-last sample (2.0 nm) and for the chemically oxidized sample (2.1 nm). In spite of almost the same CET values, the leakage current density of the chemically oxidized sample was found to be about three orders of magnitude smaller than that of the HF-last sample (from $1.2x10^{-3}$ to $4.1x10^{-7}$ A/cm^2).

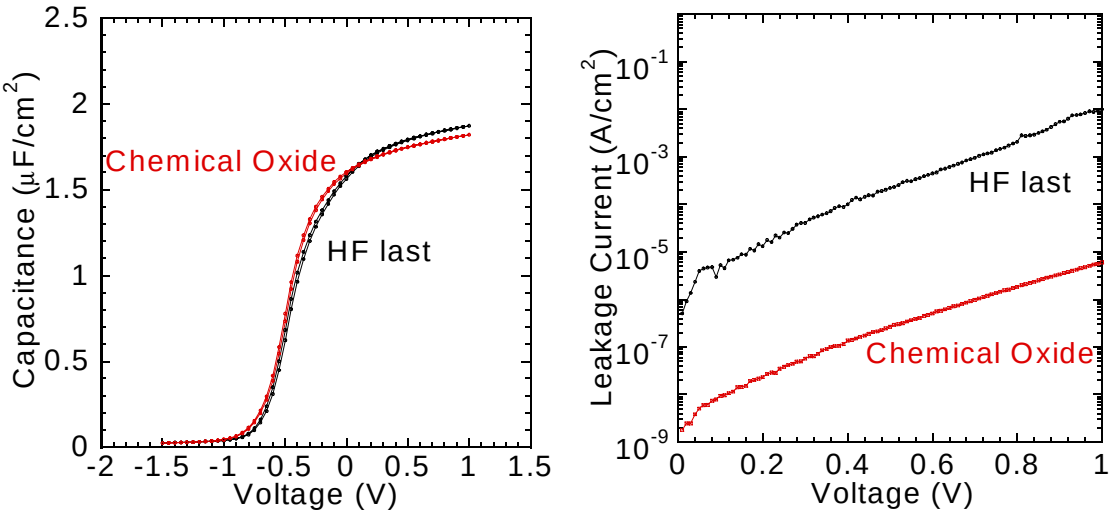


(a) C-V characteristics (b) J-V characteristics

Fig.4-10 C-V and J-V characteristics for 5.3 nm-thick film

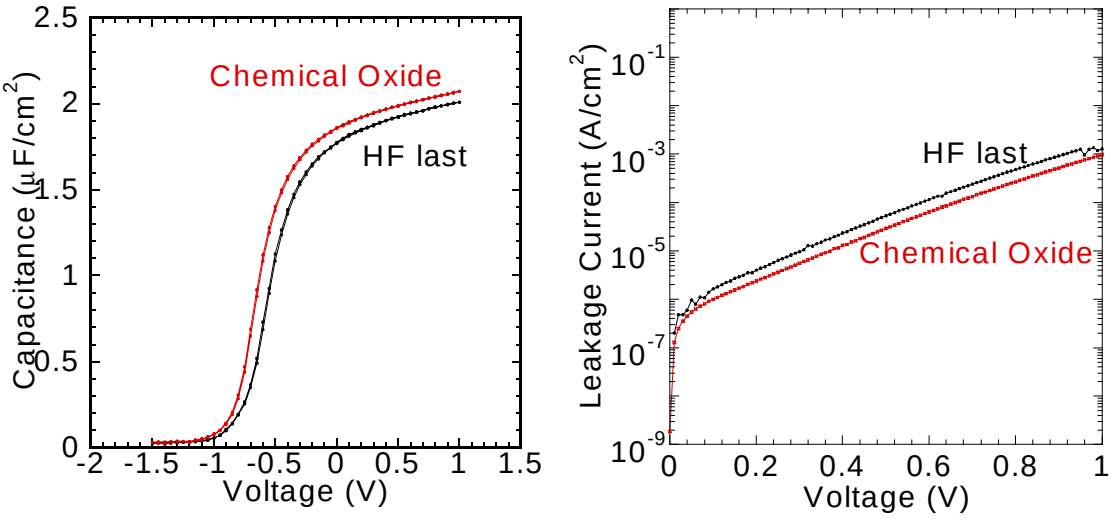
Figure 4-11 shows C-V and J-V characteristics for 3.5 nm-thick on HF-last and chemically oxidized Si substrate. CET values were almost the same (about 1.9 nm), however the leakage current of the chemically oxidized sample shows three orders of magnitude smaller than that of the HF-last samples (from $1.2x10^{-3}$ to $4.1x10^{-7}$ A/cm^2). This result was similar to the case of 5.3 nm films.

However, when the physical thickness was 2.8 nm, the leakage current of the HF-last sample improved significantly and reached the level of the chemically oxidized sample (Fig. 4-12). It was considered that high quality interfacial layer is formed during the O_2 annealing, when the thickness was relatively thin.



(a) C-V characteristics (b) J-V characteristics

Fig.4-11 C-V and J-V characteristics for 3.5 nm-thick film



(a) C-V characteristics (b) J-V characteristics

Fig.4-12 C-V and J-V characteristics for 2.8 nm-thick film

Figure 4-13 shows the summary of relation between the CET and leakage current densities at +1 V for the samples with various physical thicknesses. Since flat band voltage of the all samples showed above were –0.76±0.1 V, such comparison of leakage current density at the almost the same electric field in the films. For the physical thickness larger than 3.5 nm, the leakage current densities of the chemically oxidized samples were significantly decreased than that of HF-last samples. However the physical thickness was 2.8 nm, the leakage current of the HF-last sample decreased significantly to the same order of the chemically oxidized sample.

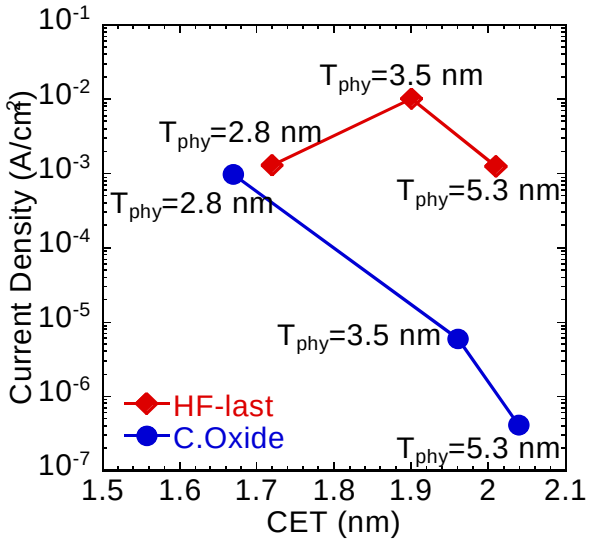


Fig.4-13 Relation between the CET and leakage current densities at +1 V

4.4.2 Surface Morphology

In the previous subsection, it found to chemical oxide improved electrical characteristics. In this subsection, the effect of chemical oxide for film surface will discuss.

Figure 4-14 shows the AFM images for the 5.3 nm-thick films before and after annealing in O2 400oC for 5 min. The scan size was 0.5x0.5μm and the z direction was 5 nm/div. In case of as-deposited samples, both HF-last and chemically oxidized samples showed smooth surface (RMS: 0.19 and 0.12 nm). However, the samples after annealing, RMS values of the HF-last samples significantly increased (RMS: 0.94 nm). On the other hand, chemically oxidized sample kept smooth surface and small RMS value (RMS: 0.16 nm).

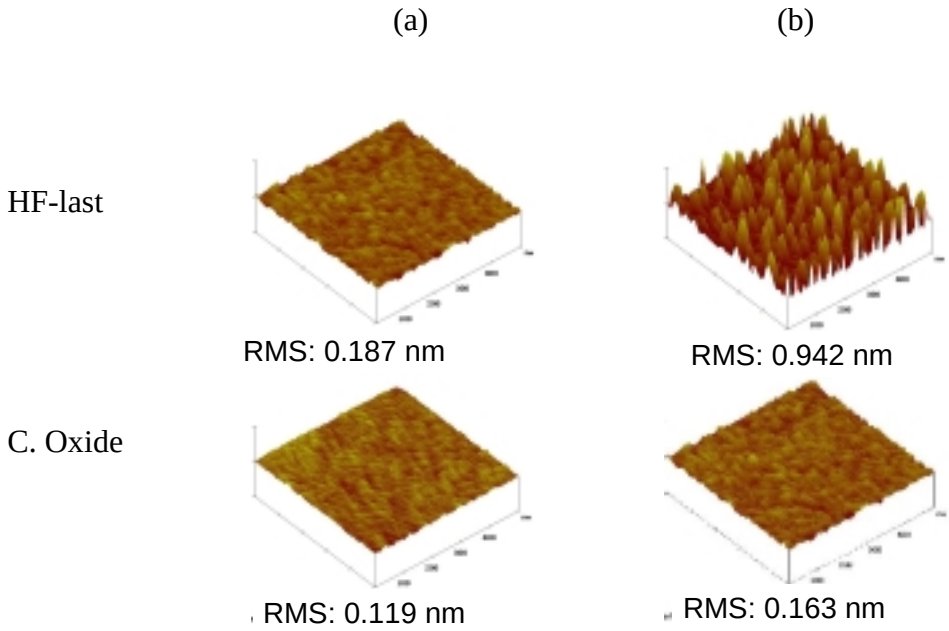


Fig.4-14 AFM images for the 5.3 nm-thick film
(a) as-depo., (b) after annealing

Figure 4-15 shows the AFM images of the films after annealing. Their physical thicknesses were (a) 5.3, (b) 3.5 and (c) 2.8 nm. For the 5.3 and 3.5 nm films on HF-last Si substrate, the surface was very rough (RMS: 0.94 and 0.70 nm), on the other hand the film on chemically oxidized Si showed smooth surface even after annealing (RMS: 0.16 and 0.13 nm). However in case of 2.8 nm thick, both HF-last and

chemically oxidized samples showed smooth surface (RMS: 0.12 and 0.12 nm).

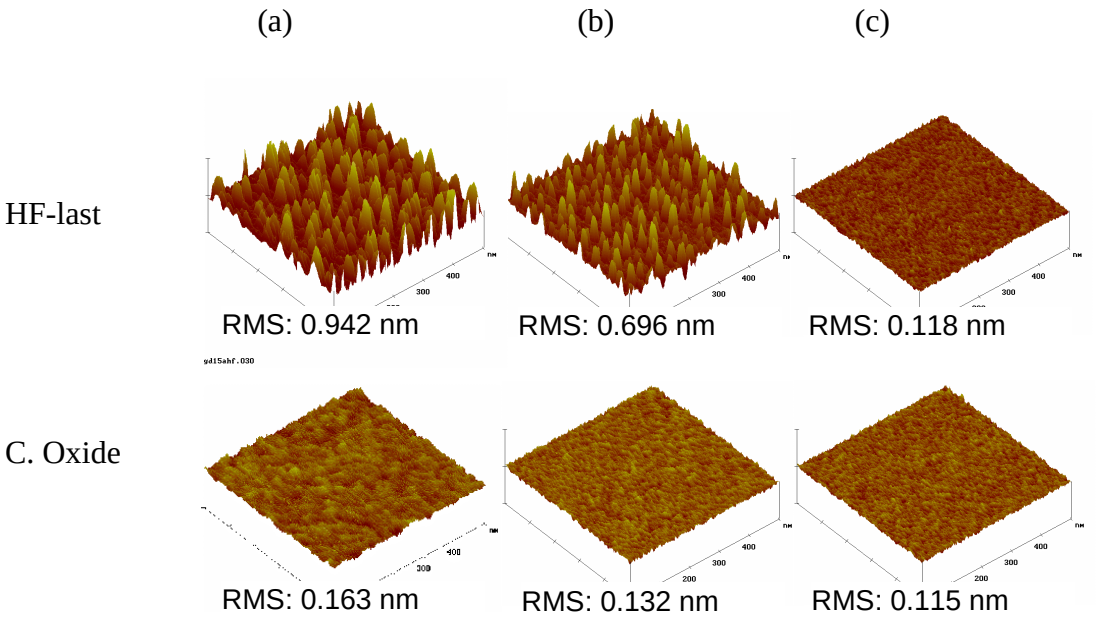
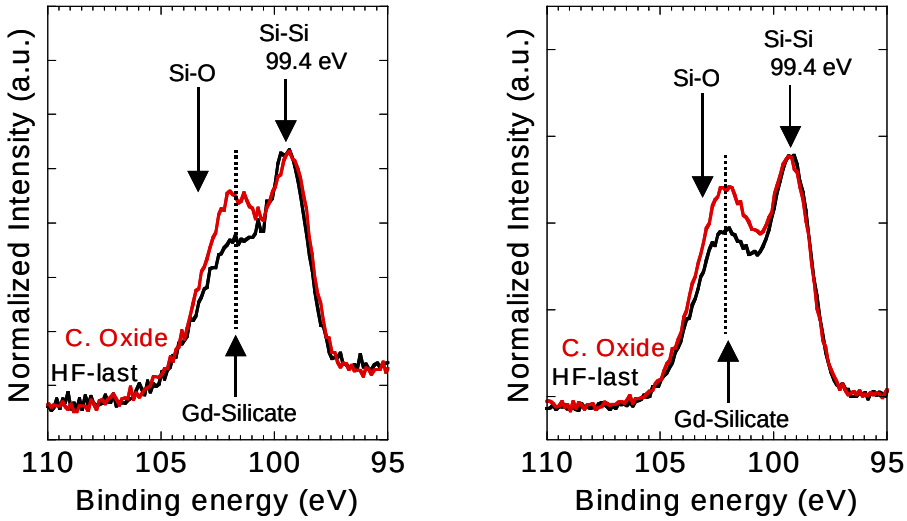


Fig.4-15 AFM images of the films after annealing
Physical thicknesses were (a) 5.3 nm (b) 3.5 and (c) 2.8 nm

4.4.3 XPS analysis

Figure 4-16 shows the XPS Si2p spectra for the samples of (a) 3.5 nm-thick films and (b) 2.8 nm-thick films. Si-O binding should be at 103.23 eV, however, chemical shifts were observed to lower binding energy. This result suggested that the formation of Gd-silicate layer at the interface during annealing. In case of 3.5 nm-thick films, the peak intensity ratios of Si-O/Si-O-Gd bindings for HF-last and chemically oxidized sample were 0.4 and 0.9, respectively. However, in the case of 2.8 nm-thick films, the peak intensities of Si-O/Si-O-Gd bindings were about 0.7. This suggested that both HF-last and chemically oxidized Si substrate formed almost the same interfacial layer.

This result indicated that Gd-silicate-rich interfacial layer was formed for 3.5 nm-thick films on chemically oxidized Si substrate, while SiO_2-rich layer was formed for 2.8 nm-thick films. Furthermore, thicker interfacial layer was formed by the deposition on chemically oxidized substrates that might have suppressed the leakage current.

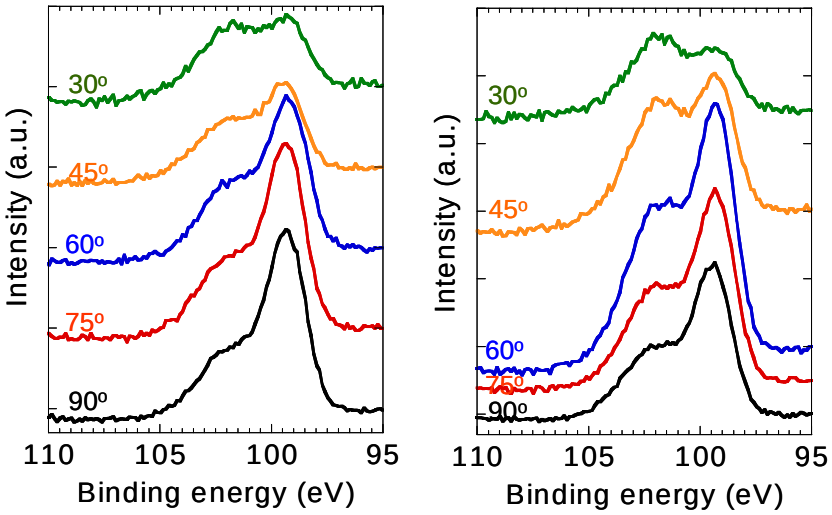


(a) 3.5 nm-thick films (b) 2.8 nm-thick films

Fig.4-16 XPS Si2p spectra.
Take-off angle was set at 45°

To analyze the detail of the interfacial layer, angle resolved XPS measurement and peak separation were carried out.

Figure 4-17 shows the XPS results for 3.5 nm-thick film cases.

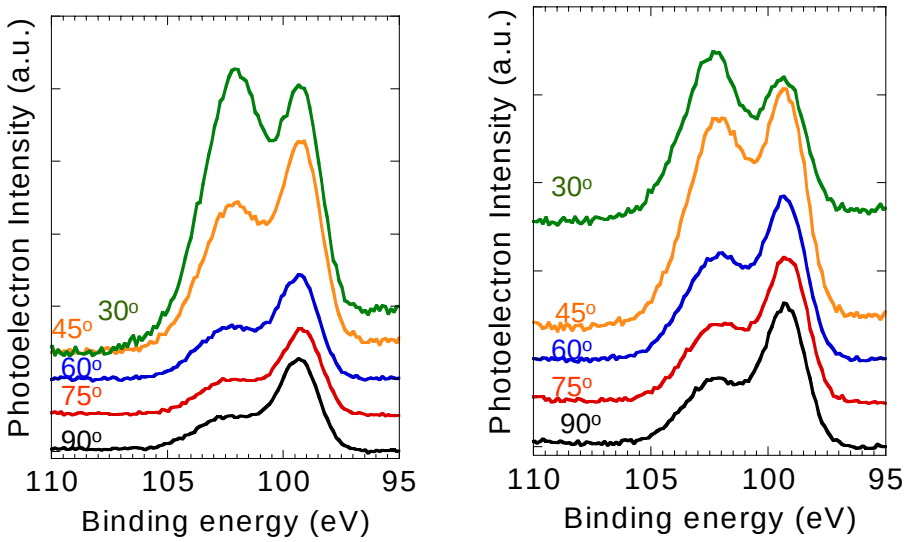


(a) HF-last (b) C. Oxide

Fig.4-17 Angle resolved XPS Si2p spectra.
Take-off angle was set at 45°

From this result, in case of chemically oxidized sample formed SiO_2-rich silicate layer at the bottom of film that take off angle was 90° (Si-O /Si-O-Gd =0.38) and Gd_2O_3-rich silicate layer formed at the close to surface that take off angle was 30° (Si-O /Si-O-Gd =0.29). In case of HF-last sample, SiO_2-poor silicate layer formed at the bottom of film (Si-O /Si-O-Gd=0.25), however, at the close to surface, the peak intensity of ratios increased (Si-O /Si-O-Gd=0.5). It was considered that the interfacial layer was not formed normally gradation.

Figure 4-18 shows the XPS results for 2.8 nm-thick film cases.



(a) HF-last (b) C. Oxide

Fig.4-18 Angle resolved XPS Si2p spectra.
Take-off angle was set at 45°

From this result, the uniform interfacial layer were formed both HF-last and chemically oxidized sample. The peak intensity ratios were about Si-O /Si-O-Gd=0.4 for chemically oxidized and Si-O /Si-O-Gd=0.5 for HF-last.

	T_{phy}	θ	HF-last	C.Oxide
SiO_2/Silicate	3.5 nm	30	0.50	0.29
		90	0.25	0.38
	2.8 nm	30	0.57	0.38
		90	0.53	0.40

Table 4-3 summery of XPS results

Tale 4-3 shows the summery of XPS results for effect of chemical oxide. The measurement take off angle were 30° (close to surface) and 90° (close to interface). In this result, gradual interfacial layer formed for 3.5 nm-thick chemically oxidized sample, and uniform interfacial layer formed for 2.8 nm-thick HF-last and chemically oxidized sample. It was considered that the one of the reason that decreased leakage current for 3.5 nm-thick chemically oxidized sample, formation SiO_2-rich silicate layer at the interface that had higher barrier.

4.4.4 TEM observation

In the previous subsection, we discussed the interfacial condition for 3.5 and 2.8 nm-thick Gd_2O_3 film were deposited on HF-last and chemically oxidizes Si substrates. In this section, we will discuss the film quality and interfacial condition using cross sectional TEM images for 3.5 nm-thick films.

Figure 4-19 shows the TEM image for HF-last sample.

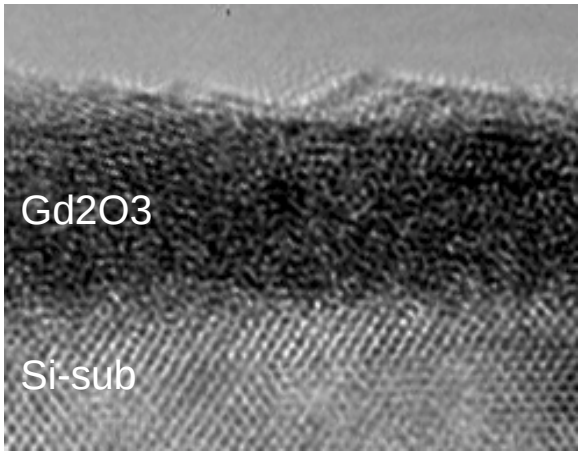


Figure 4-19 TEM image for HF-last sample

Figure 4-20 shows the TEM image for chemically oxidized sample.

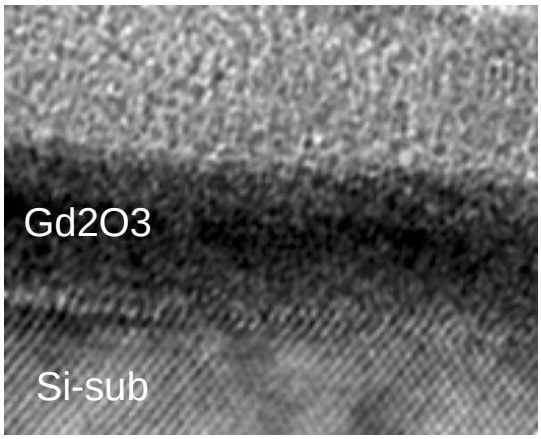


Figure 4-20 TEM image for chemically oxidized sample

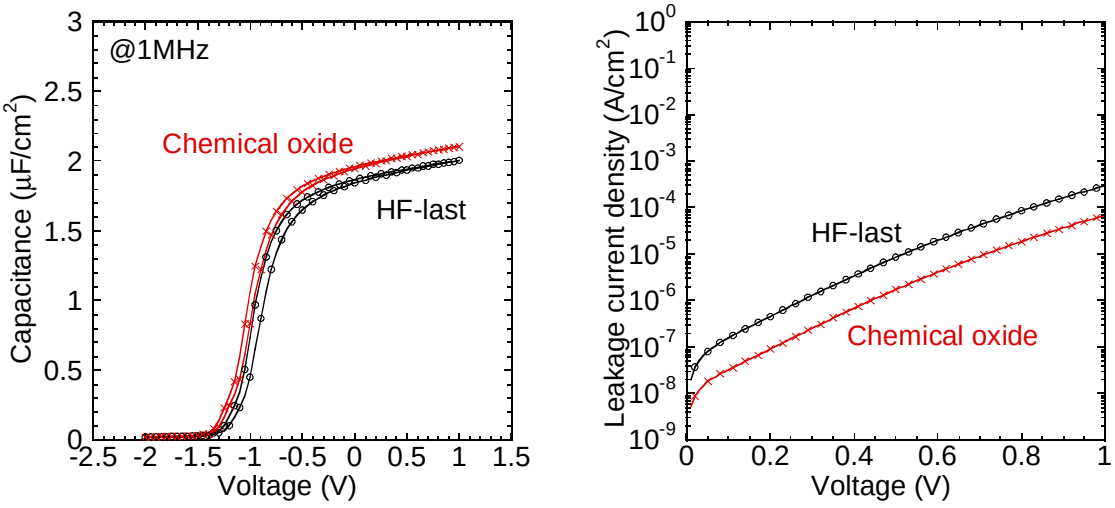
These figures show the HF-last and chemically oxidized sample exhibited amorphous state even after annealing, and their physical thickness were about 3.6 nm.

From this result, high quality interfacial condition was not observed for HF-last sample, it had roughness and oxidizing Si layer at the interface. On the other hand, chemically oxidized sample showed gradual interface condition.

4.5 Effect of Chemical oxide (Another rare earth oxide)

4.5.1 La_2O_3

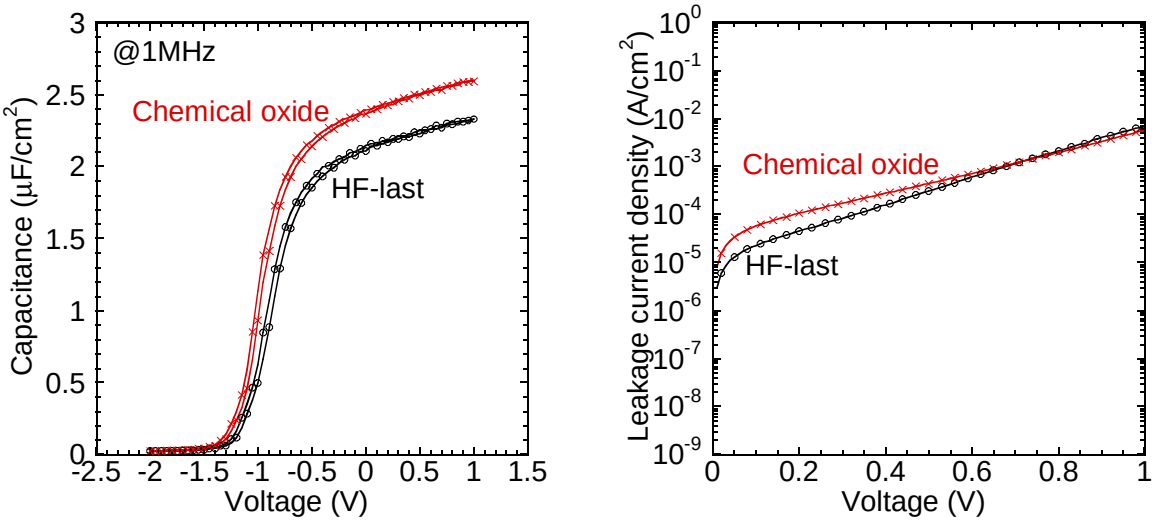
Figure 4-21 shows C-V and J-V characteristics for 4.5 nm-thick La_2O_3 films deposited at 250°C. These samples were annealing in O_2 at 400°C for 5 min. For C-V characteristics, accumulation capacitance of chemically oxidized sample was larger than that of HF-last sample, so CET for chemically oxidized sample was 1.4 nm, and 1.6 nm of HF-last sample. It was considered that the growth of interfacial silicate layer was promoted as formed chemical oxide prior to deposition. Leakage current of chemically oxidized sample was smaller than that of HF-last sample.



(a) C-V characteristics (b) J-V characteristics

Fig.4-21 Electrical characteristics of 4.5 nm-thick La_2O_3 films

Figure 4-22 shows C-V and J-V characteristics for 3 nm-thick La_2O_3 films deposited at 250°C after annealing. Accumulation capacitance of chemically oxidized sample was larger than that of HF-last sample. And CET of chemically oxidized sample was 1.1 nm, and 1.2 nm of HF-last sample. However, the leakage current of these samples showed almost the same value. This is the same result for Gd_2O_3 case.



(a) C-V characteristics (b) J-V characteristics

Fig.4-22 Electrical characteristics of 3 nm-thick La_2O_3 films

Figure 4-23 shows XPS Si2s spectra for the 3 nm-thick film after annealing. In this figure, chemically oxidized sample growth the interfacial silicate layer compare with HF-last sample. In case of La_2O_3, from XPS result, interfacial SiO_2 layer was not formed even after O_2 annealing. The interfacial layer was all silicate. As formed chemical oxide prior to deposition, the reactive La_2O_3 and SiO_2 formed high quality silicate layer.

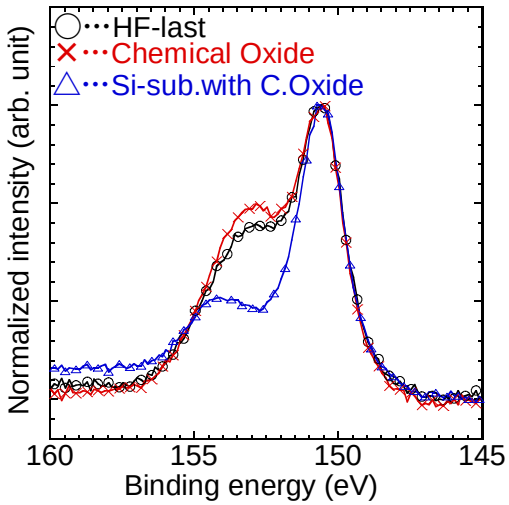
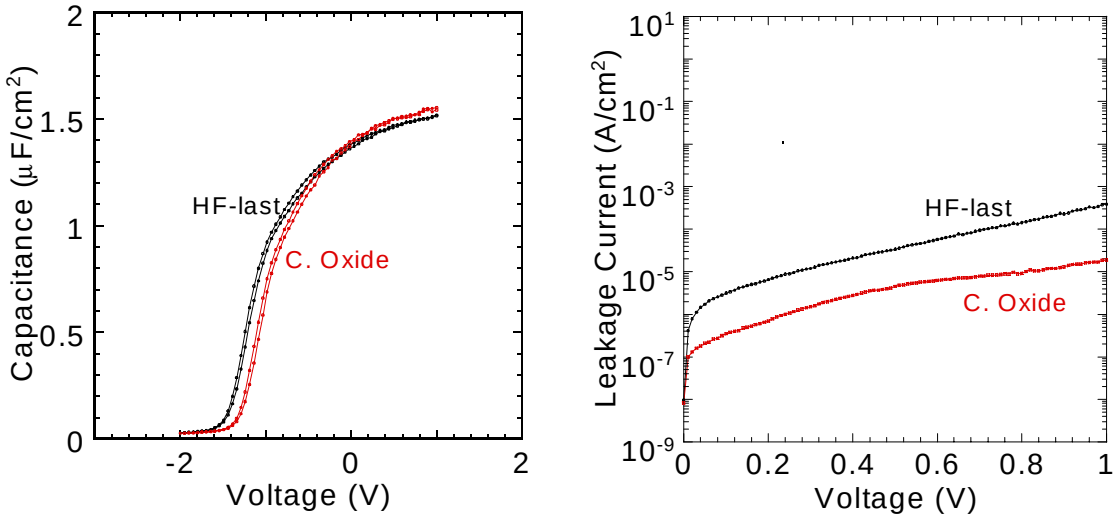


Fig.4-23 Si2s XPS spectra of 3 nm La_2O_3 films after annealing.
Take-off angle was set at 45^o

4.5.2 CeO_2

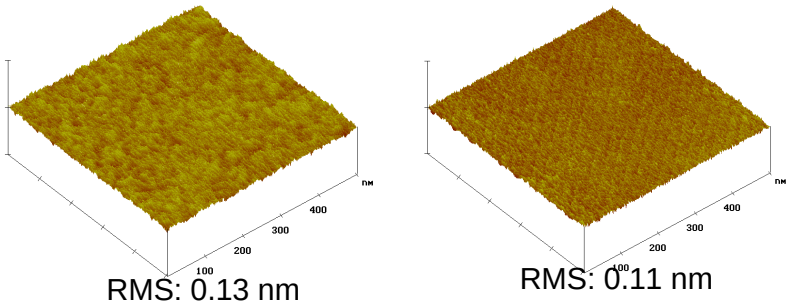
Figure 4-24 shows C-V and J-V characteristics for 5.5 nm-thick CeO_2 films deposited at 250°C. These samples were annealing in O_2 at 400°C for 5 min. For C-V characteristics, accumulation capacitance of HF-last and chemically oxidized sample was almost the same, CET for chemically oxidized sample was nm, and nm of HF-last sample. Although the CET values were almost the same, the leakage current of the chemically oxidized sample showed 1.5 orders of magnitude smaller than that of the HF-last sample.



(a) C-V characteristics (b) J-V characteristics

Fig.4-24 Electrical characteristics of 4.5 nm CeO_2 films

Fig 4-25 shows the AFM images and root mean square (RMS) of surface for annealing samples. The scan size was 0.5x0.5 μm and the z direction was 5 nm/div. Both HF-last and chemically oxidized samples were observed smooth surface (RMS: 0.13 and 0.11 nm).



(a) HF-last (b) C. Oxide

Fig.4-25 AFM images for 5.5 nm CeO_2 films at 250^{o}C deposition

Though CeO_2 film deposited on HF-last Si substrate kept smooth surface even after annealing, the chemically oxidized sample decreased leakage current. It was considered that the reason for decreased leakage current was formation SiO_2-rich layer at the interface.

4.6 Discussion

In this chapter, we discussed the effect of surface treatment for Si substrate.

Formation chemical oxide prior to deposition, we obtained excellent electrical characteristics. However, after annealing the effect of chemical oxide had dependence of physical thickness. The physical thickness became less than 3 nm, in was not observed the decrease of leakage current.

Considering the results from AFM and XPS observations, the low leakage current densities of Gd_2O_3 films on chemically oxidized Si substrates, especially for 3.5 and 5.3 nm-thick, were considered that high quality silicate layer were formed at the interface. On the other hand, the samples on HF-last Si substrate, the rough surfaces might be originated from non-uniform silicate formation, and it should result in large leakage current. In the case of 2.8 nm-thick samples, the effect of chemical oxide was not observed and probably because the interfacial layer formation by the oxygen penetration through the film during annealing, for HF-last sample. However, the angle resolved XPS measurement, after annealing, 2.8 nm-thick film formed uniform silicate layer, both HF-last and chemically oxidized sample.

Chapter 5
Conclusion

In this chapter, we will conclude of this study and describe the future issue.

5.1 Result of this work

In this study, we aim to improve the interfacial characteristic for high-k gate dielectrics -- film uniformity, interface state density and leakage current -- by using MBD method. Formation chemical oxide prior high-k deposition obtained excellent characteristics.

The conclusions of this study are as follows:

The first, we investigated the conventional characteristics for MIS capacitor using rare earth oxides, in this study, we used Yb_2O_3 and Gd_2O_3.

From this result, Yb_2O_3 indicated the interface conditions were improved by the post-deposition anneal, however, Gd_2O_3 did not indicate the fact. Thick Gd_2O_3 film has high-dielectric constant about 16, and thick Gd_2O_3 was crystallized by post-deposition anneal. However, thin Gd_2O_3 (less than 24 nm) kept the amorphous state even after annealing.

The second, the effect of surface treatment of Si substrate was investigated. In this study, we used mainly Gd_2O_3.

In this study, high-quality oxy-nitride buffer layer did not obtained, so MIS capacitor using oxy-nitrided Si substrate degradation interfacial state density. However, MIS capacitor using chemical oxide by H_2O_2 dip, obtained high-quality interfacial condition and electrical characteristics. From XPS result, high-quality interfacial layer found to be silicate. Silicate is the suitable at Si interface, and promising candidates for next generation gate insulator. In case of 3.5 nm-thick Gd_2O_3 film on chemically oxidized Si substrate obtained the high-quality silicate layer. Obtained excellent result is as follow:

EOT: 1.58 nm (CET: 1.89 nm)
Leakage current: 6.0×10^{-6} A/cm^2
RMS: 1.3 nm

However, the effect of chemical oxide had dependence of physical thickness. The physical thickness became less than 3 nm, in was not observed the decrease of leakage current. In case of less than 3 nm, the interfacial layer formation by the oxygen penetration through the film during annealing, for HF-last sample. The angle resolved XPS measurement, after annealing, 2.8 nm-thick film formed uniform silicate layer, both HF-last and chemically oxidized sample.

5.2 Future issues

In this study, we obtained excellent result for rare earth gate dielectrics. However we remained some unresolved problems and new potential for rare earth gate dielectrics.

In these results, the effect of surface treatment, especially chemical oxide by H_2O_2 dip, is the useful method to obtained high-quality interfacial silicate layer. Though silicate is suitable at Si interface compared to another high-k material, it does not have high dielectric constant (about 30). In the future issue, it will fabricate high dielectric constant and high quality silicate layer, and obtain EOT less than 1 nm. And we think that chemical oxide will improve the transistor characteristics. The next goal is the improvement of mobility and interface state density.

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