Master Thesis

Study on Fabrication Process for High-k Gate MOSFET Using Rare Earth Oxides

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Chapter 1.

Introduction

1.1 Aggressive Scaling of Silicon Based CMOS Devises

In recent years, Information Technology society developed dramatically, for example the tremendous growing population of using internet, mobile phone, car navigation and many kinds of so called “IT products”. There is no doubt that the progress of recent Information Technology is realized by the improvement of the electronics, especially by the Silicon based Large Scale Integrated (LSI) circuits technology. The improvement of LSI has been achieved by the downsizing of its components such as Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Because of the downsizing, capacitance of the components reduces, resulting in high-speed, high-frequency and low power operation of the circuits. Of course, size reduction and high-integration of the circuits can be also realized at the same time with the performance improvement. Now, already with the demonstration of excellent operation of 15 nm gate length CMOS [1], 10 nm and even blow becomes within a good range of R & D target.

The downsizing of the components has been accomplished by the scaling method [2]. In the scaling method, lateral and vertical dimensions and supply voltage are scaled down by the same factor S, while Si-substrate impurity concentration is increased by the factor S as shown in Fig. 1.1 and Table 1.1. It should be noted that the trend of the down-scaling has been accelerated by every update of the ITRS (International Technology Roadmap for Semiconductors), because of the very severe competitions between the rival LSI produces for high performance device, such as high clock frequency operated microprocessors. In order to realize such high performance microprocessors, downsizing of the gate length becomes the most important issue. According to the ITRS 2002 update, gate length of 18 nm is to be realized in 2010 as shown in Table 1.2.

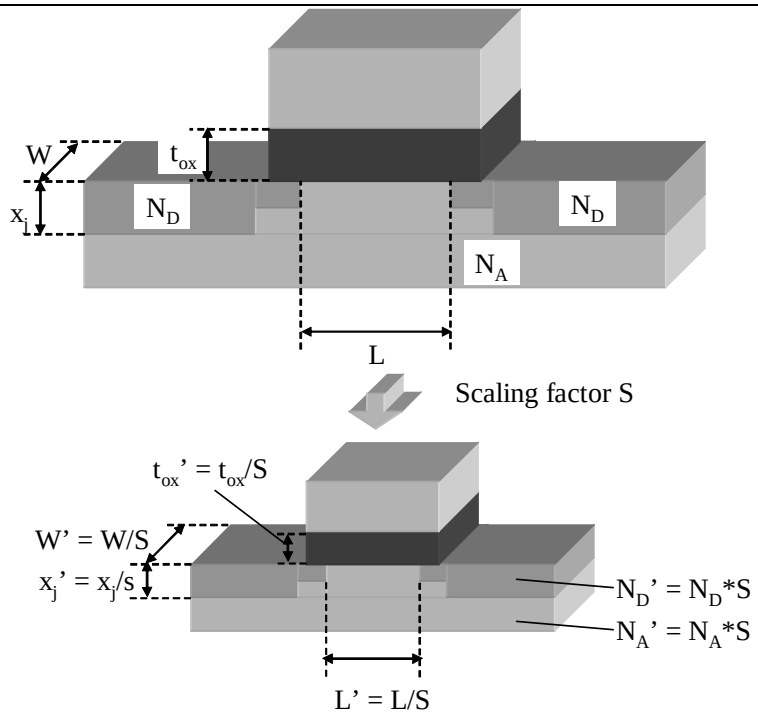


Fig. 1.1. Schematic structure of a typical MOSFET and scaling of it by a factor of S.

Table 1.1 Scaling of MOSFET by a scaling factor of S.

Quantity	*Before scaling*	*After scaling*
Channel length	L	$L' = L/S$
Channel width	W	$W' = W/S$
Device area	A	$A' = A/S^2$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/S$
Gate capacitance per unit area	C_{ox}	$C_{ox}' = S*C_{ox}$
Junction depth	x_j	$x_j' = x_j/S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{TO}/S$
Doping densities	N_A	$N_A' = S*N_A$
	N_D	$N_D' = S*N_D$

Table 1.2. International Technology Roadmap for Semiconductors (2002 Update).

year	2002	2004	2010	2016
DRAM 1/2 pitch (nm)	115	90	45	22
Physical gate length (nm)	53	37	18	9
EOT(physical) (nm)	1.2 – 1.5	0.9 – 1.4	0.5 – 0.8	0.4 – 0.5
Nominal power supply voltage (V_{DD}) (V)	1.1	1	0.6	0.4

1.2 Limit of SiO_2

However, so many difficulties are expected with the downsizing. Figure 1.2 shows limiting factor for sub-10 nm gate length CMOS transistor. One of the biggest concern is the thinning of the physical equivalent gate oxide thickness (EOT), because as the gate dielectric becomes thinner, direct-tunneling leakage current increases. From ITRS 2002 update, EOT of less than 1 nm is required at 2004. In the case of conventional SiO_2 gate dielectrics, the leakage current of 100 A/cm^2 flows through 1 nm thick SiO_2 as shown in Fig.1.3[3,4]. This results in huge leakage current in an entire LSI chip and becomes big problem for power consumption.

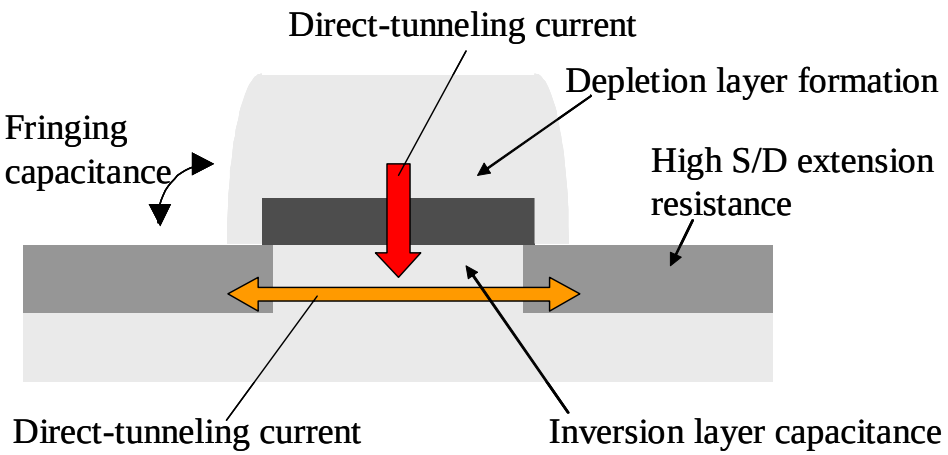


Fig. 1.2. Limiting factor for sub-10 nm CMOS.

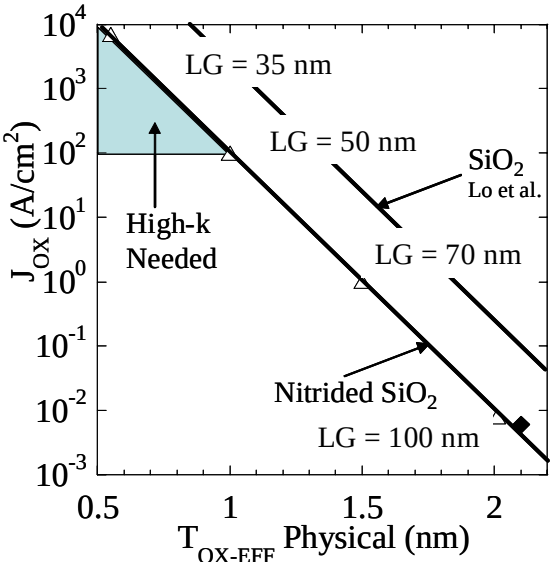


Fig. 1.3. Gate leakage current vs. EOT for SiO_2 and nitrided SiO_2.

1.3 Requirement of High-k dielectric materials

To overcome this problem, high-k (high-dielectric constant) materials have been attracted much attention. Replacing conventional SiO_2 with high-k materials for gate insulator, the required physical gate thickness for the same EOT becomes thicker, and thus, the leakage current could be suppressed. Figure 1.4 represents the schematic description of differences between the cases using SiO_2 and high-k material for gate insulator.

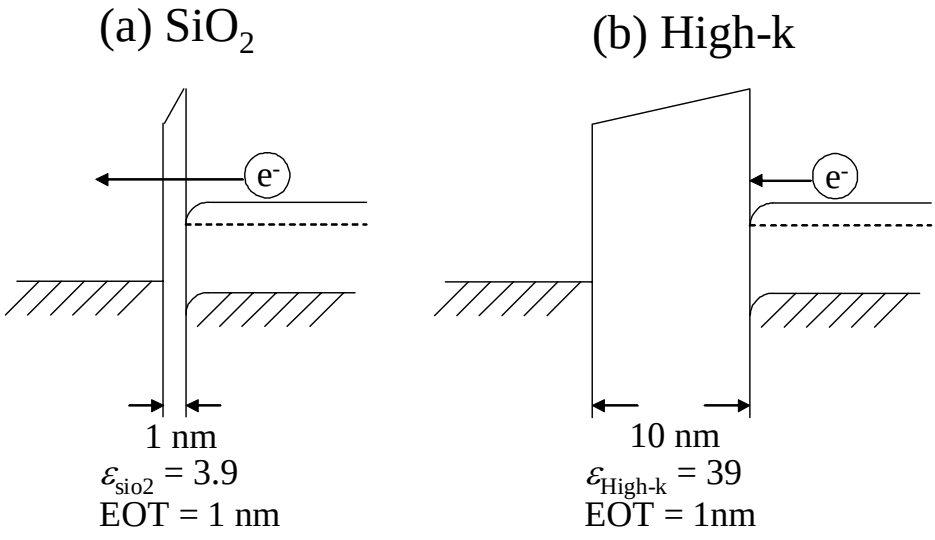


Fig. 1.4. Schematic description of differences between the cases using (a) SiO_2 and (b) High-k for the gate insulator in MIS structure.

Already 1.5 nm oxynitride gate dielectrics have been used in high speed logic LSI products. However, further higher-k materials are requested because NO stack film suppresses the gate leakage current only 1.5 orders of magnitude, as shown in Fig. 1.3. The gate dielectric should meet the following fundamental requirements: (1) No radioactivity, (2)Being solid at the Si-LSI process temperature, (3) Being chemically stable at Si interface. Metal oxides (MO_x) are promising candidates for the high-k gate materials. Considerable materials which oxides satisfy above requirements are shown in Table 1.3, as without shade column [5].

Various high-k materials have been investigated by many organizations, so far. Figure 1.5 shows high-k gate dielectrics reported resent 2 year conferences [6]. As shown in this figure, HfO_2 and its aluminates, silicates are now the most popular candidates. However, there are still various problems to be solved as shown in Table 1.4 [6]. The problems of interfacial layer growth and crystallization during the post deposition high-temperature annealing led to the increase of EOT and gate leakage current. New techniques or dielectrics are necessary to realize further reduction of EOT value deep into sub-1.0 nm region.

Table 1.3. Candidates for the metal whose oxide is suitable for gate insulator of MOSFETs.

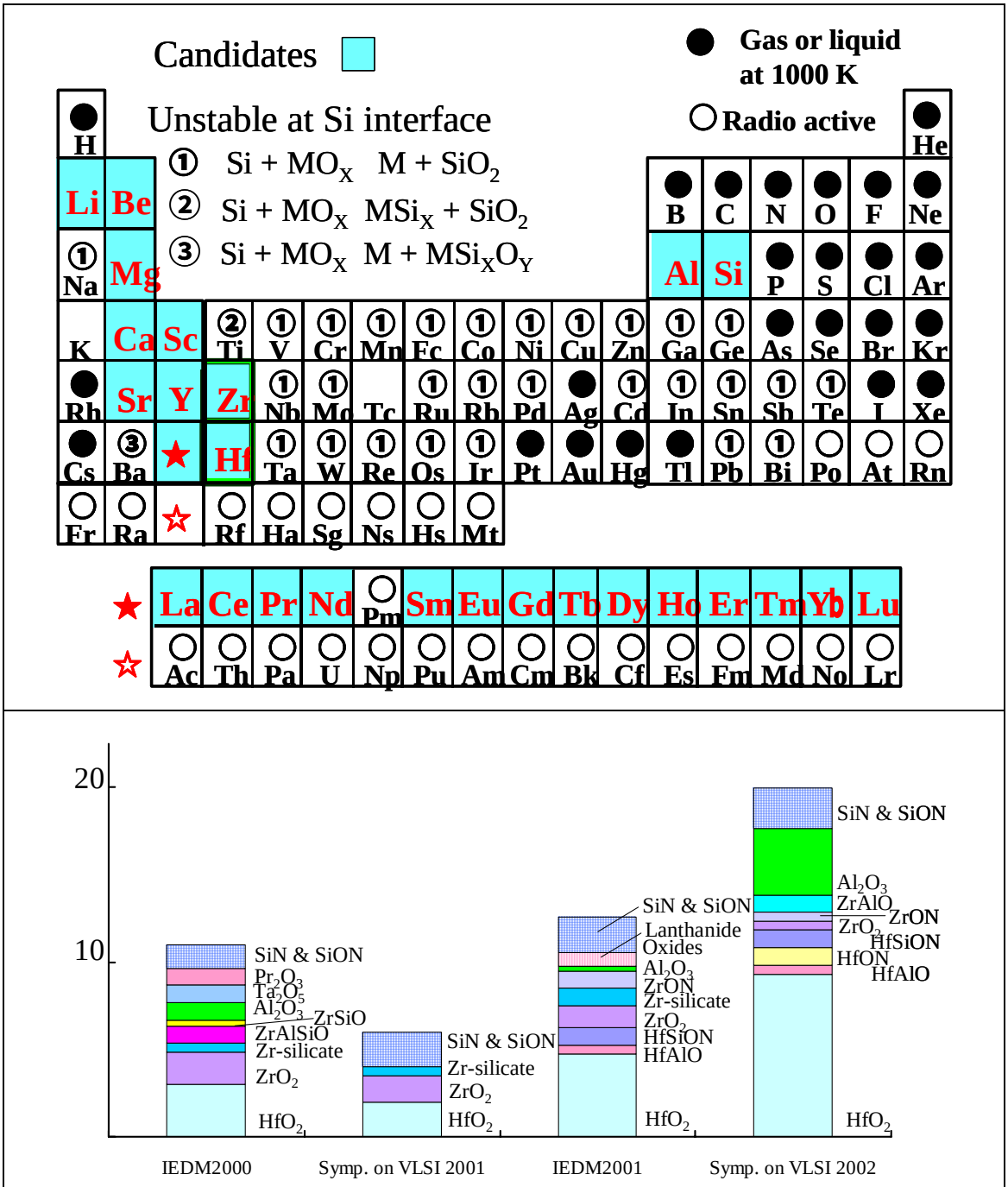


Fig. 1.5. Reported High-k materials.

Table 1.4. Problems of High-k.

(1) Interfacial layer formation
(2) Micro crystal growth
(3) Lateral oxidation at gate edge
(4) Lower mobility
(5) Fixed charge, Flatband shift
(6) Higher density of interface states
(7) Boron penetration
(8) Contamination from precursor for CVD

1.4 Rare Earth Metal Oxides

Rare earth metal oxides (or Lanthanide oxides) are also good candidates for the high-k dielectrics gate insulator. Recently, excellent results of their thin films such as La_2O_3 [7], Pr_2O_3, [8], and CeO_2 [9] have been reported. In the case of La_2O_3, A. Chin et al. [7] reported that EOT of 0.48 nm and leakage current of 0.06 A/cm^2 at -1 V were achieved with physical thickness of 3.3 nm. It was also reported that EOT of 0.38 nm was achieved by using CeO_2 for gate dielectrics. The EOT of 0.38 nm is the smallest value ever reported for high-k gate dielectric [9]. Table 1.5 [10] shows physical properties for various high-k materials. This table suggests that La_2O_3 is the most attractive candidates among the listed materials. Thus, rare earth metal oxide thin films are thought to be one of the most attractive alternates as post HfO_2 high-k gate dielectrics because of their good property. There are 15 elements in rare earth metal oxides. Values of bandgap and lattice energy for the rear earth metal oxides are shown in Fig. 1.6 and 1.7 [11].

Unfortunately, rare earth metal oxides have also problems. Moisture absorption of rare earth oxides which led to film degradation is well known as the biggest problem and its solutions are seriously being developed. Under normal pressure at room temperature, rare earth metal oxides react with H_2O and CO_2, and produce hydroxide, $Ln(OH)_3$, and carbonate, $Ln(CO_3)_3$ or mixture of them. The hydroxylation takes place all over the oxide. On the other hand, carbonation does in the outer layer only [11]. There is a big concern that moisture absorption might be a stumbling block for the application of these high-k dielectrics into the conventional CMOS fabrication process.

Table 1.5. Physical properties for various high-k materials.

	SiO_2	Al_2O_3	HfO_2	ZrO_2	$ZrSi_xO_y$	La_2O_3
K value	3.9	9.5	20-25	20-25	10-12	27
Bandgap (eV)	9	8.8	4-5	5.8	~6	5.5
Amorphous Phase Stability	High	High	Low	Low	-	-
Oxygen Diffusion at 950°C (cm^2/s)	$2x10^{-14}$	$5x10^{-25}$	-	10^{-12}	-	-
Lattice enregy (kJ/mol)	13125	15916	-	11188	-	12452

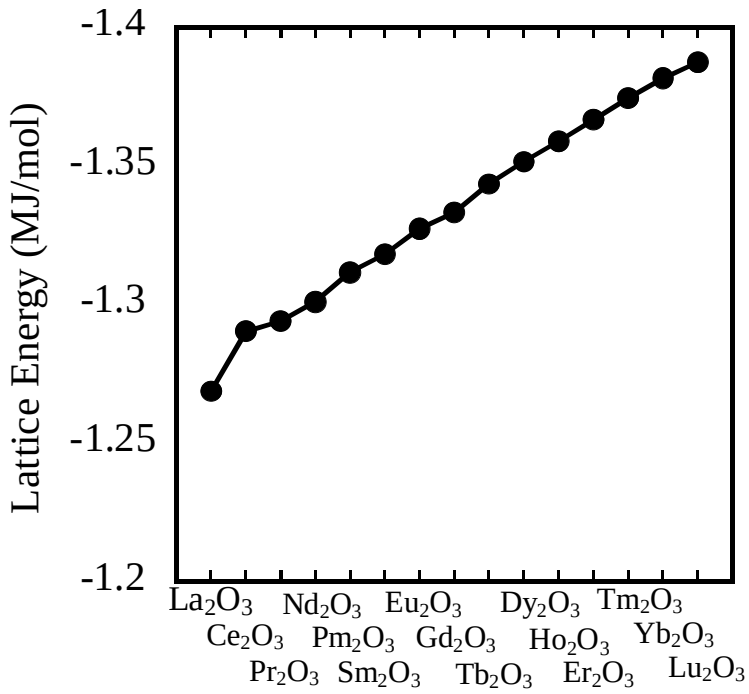


Fig. 1.6. Lattice energy of lanthanide oxides.

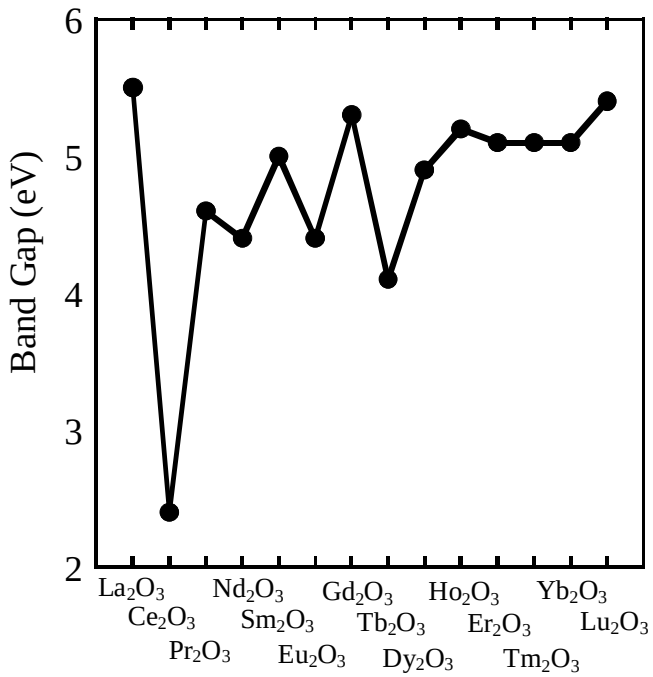


Fig. 1.7. Band gap of lanthanide oxides.

1.5 Purpose of This Study

There has been no other research about the stability of the rare earth metal oxide thin films to introduce to the conventional CMOS fabrication process. Thus, the purpose of this study is to investigate the stability of rare earth metal oxide thin films for the conventional CMOS fabrication process. There are two big problems during the CMOS fabrication process as shown in Fig. 1.8, one is the chemical wet cleaning process, and the other one is the S/D activation annealing process. To investigate the stability for the wet process, the stability tests for moisture ambient, ultra-pure water and resist process were carried out. Additionally, for the preliminary step to the investigation of the stability of high-k thin films for the heat process, TiN films were investigated which has been one of the leading candidates to be the next generation of metal gate electrode.

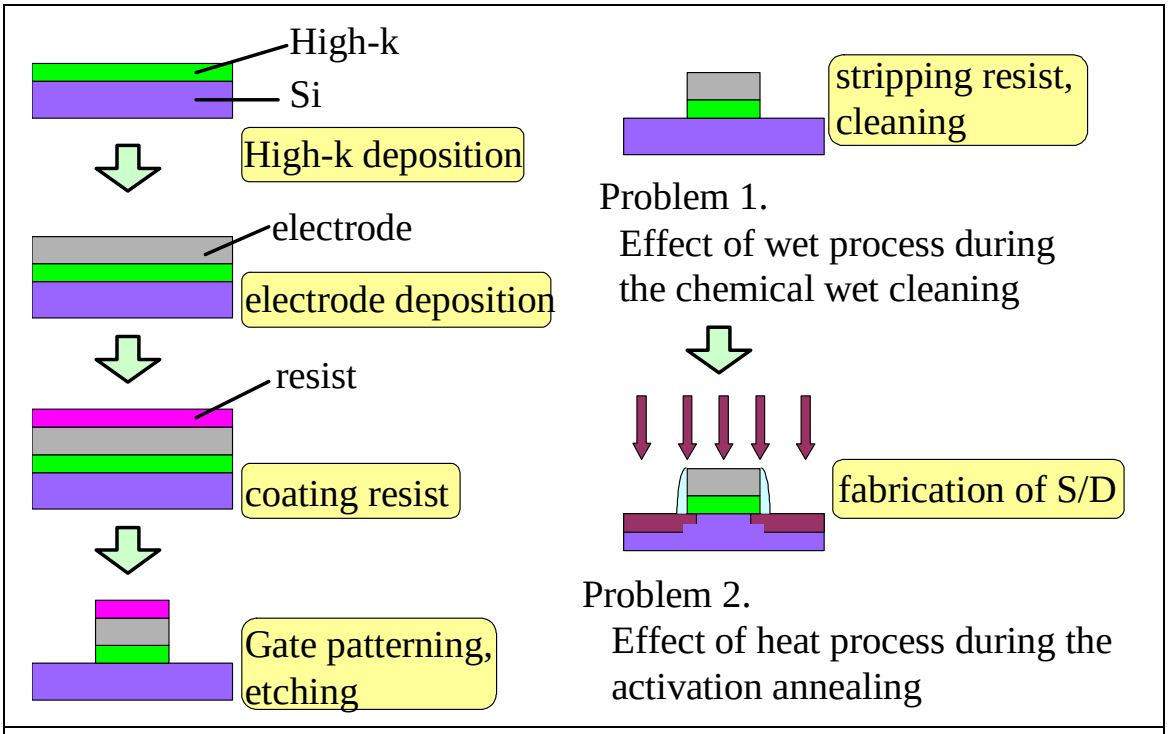


Fig. 1.8. Flowchart of the CMOS fabrication process.

Chapter 2.

Fabrication and Characterization Methods

2.1 Fabrication methods for MIS (Metal-Insulator-Semiconductor) Capacitors

2.1.1 Chemical Cleaning of Silicon Substrate

Prior to use a bare Si substrate for the sample fabrication, it should be chemically cleaned to remove the particles as well as any traces of organic and metallic impurities from the surface.

One of most important chemicals used in the substrate cleaning processes is a DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. In this study, DI water with the receptivity of larger than 18.2 MΩ-cm at 25^{o}C, and the TOC (Total Organic Carbon) of less than 1 ppb was used.

In this Si substrate was cleaned using hydrofluoric acid as shown Fig. 2.1, which was based on the RCA cleaning method which was proposed by W. Kern et al. In this process, a cleaning step in a solution of sulfuric acid (H_2SO_4) / hydrogen peroxide (H_2O_2) (H_2SO_4 : H_2O_2 = 1 : 4, SPM) was performed to remove any organic material and metallic impurities. The step in a solution of diluted hydrofluoric acid was performed to remove any oxide which might have been formed on the Si surface through this process. Finally, the substrate is rinsed with DI water.

After the cleaning process, the substrate was loaded into the loading chamber immediately.

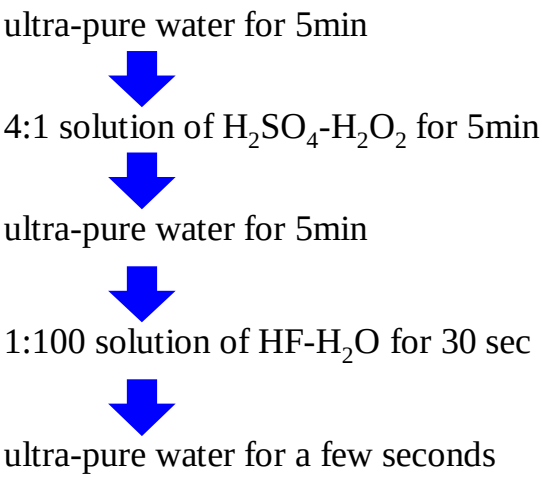


Fig 2.1. Flowchart of chemical cleaning of Si-substrate.

2.1.2 Molecular Beam Deposition (MBD)

In this study, Molecular Beam Deposition (MBD) equipment with ultra-high vacuum was used for the deposition of the amorphous high-k films on n-type (100) Si substrate. MBD has advantages to Chemical Vapor Deposition (CVD) and sputtering in terms of film purity and Si substrate damages, respectively. The schematic drawing of MBD equipment is shown in Fig. 2.2. The back pressure of the deposition chamber was 10^{-10} Torr, and the pressure at the deposition was 10^{-7} ~ 10^{-9} Torr. The ultra-high vacuum is important to suppress the formation of the interfacial layers. 4 targets can be installed for the equipment as shown in Fig. 2.2. In this study, metal oxides were used as the sources. Physical thickness of the film is monitored with a film thickness counter using crystal oscillator. The temperature of the substrate is controlled by a substrate heater and is measured by a thermocouple.

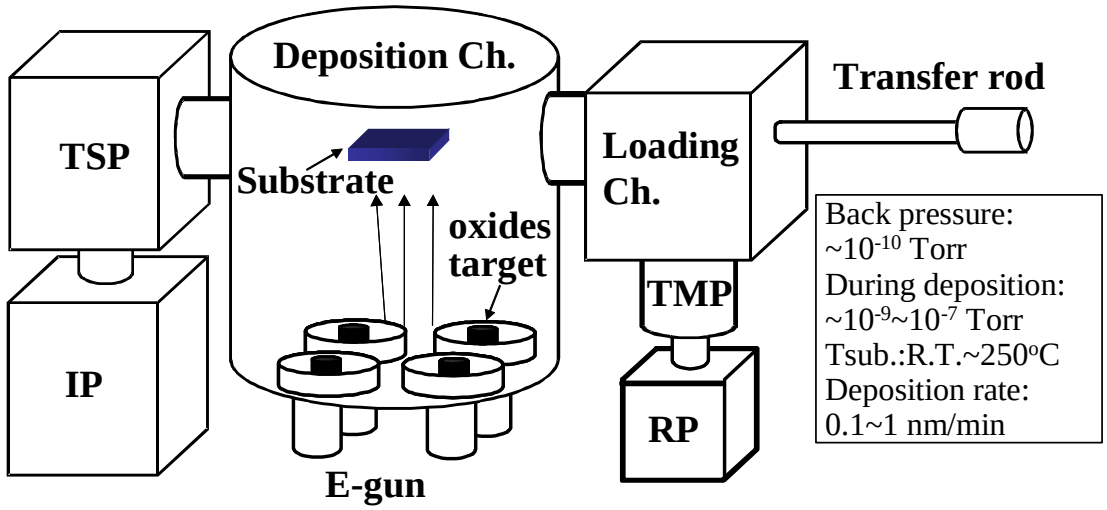


Fig. 2.2. Schematic drawing of MBD equipment.

2.1.3 Rapid Thermal Annealing (RTA)

Rapid Thermal Annealing (RTA) equipment (MILA-300, ULVAC Co Ltd.) was used to anneal the samples. The RTA equipment which was used in this study is shown in Fig. 2.3. The gas flow rate was 1.2 *l* per minute, and G3 grade gas was used. The furnace was not vacuumed prior to the annealing. Thus, the remaining air or moisture of the furnace cannot be replaced by the gases completely, although its content is assumed to be extremely small. Most of the deposited films were subsequently annealed by RTA at 600^{o}C in O_2 or N_2 for 5min. This RTA equipment was also used to anneal TiN to investigate its thermal stability. In this case, the samples were annealed in N_2 ambient to avoid oxidation.

Fig. 2.3. RTA equipment (MILA-3000) used for annealing in O_2 or N_2.

2.1.4 Vacuum Evaporation Method

For the electrical measurement, Al electrodes were deposited for the top and bottom through a metal hard mask, using a vacuum evaporation equipment with bell jar. Al was evaporated by heated W filament at high vacuum. The pressure was 1~2 x 10^{-5} Torr during the deposition. The diameter of the mask for the top electrode was 100-μm. Schematic image of the metal evaporation is shown in Fig. 2.4.

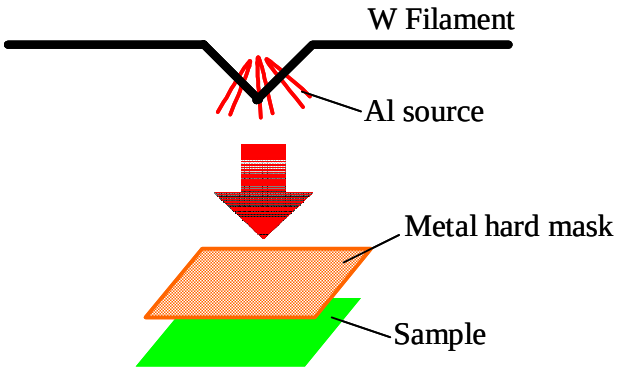


Fig. 2.4. Schematic image of the metal evaporation.

2.1.5 Radio Frequency Magnetron Sputtering

Radio Frequency Magnetron Sputtering (JEOL SP360R) system was used to deposit TiN electrode on the high-k films. Schematic diagram of sputtering system is shown in Fig. 2.5. There are advantages to sputtering: (1) controlled stoichiometry of the deposit, (2) improved adhesion, (3) better control of film thickness. The RF power source was operated at a frequency of 13.56 MHz. In this study, the RF power was 100 ~ 150 W. The plasma is confined between the two closely spaced electrodes.

Two types of gas, Ar and N_2 were applied in the chamber. The ratio of Ar / N_2 was 4 / 0 ~ 4 / 2. TiN and Ti metal target were used to compare the samples which was sputtered by Ar gas only and sputtered by Ar and N_2 (reactive sputtering). The distance between the substrate and the target was 5.5 cm.

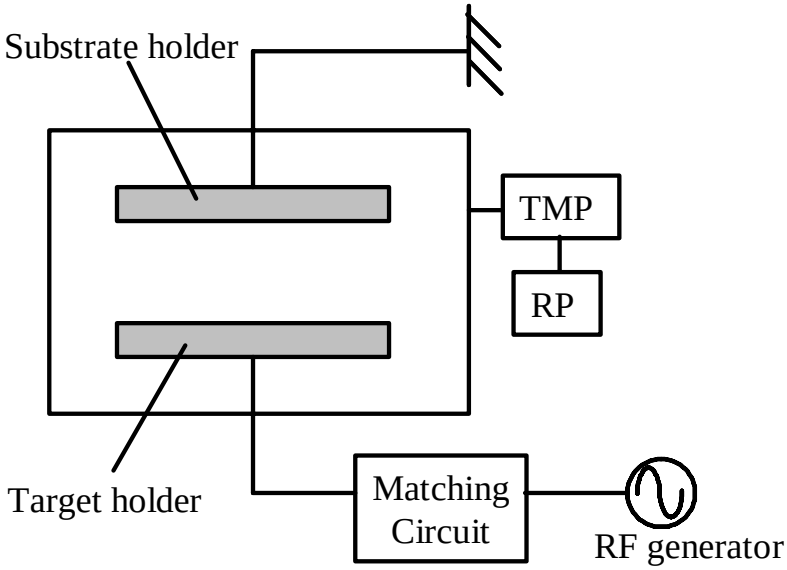


Fig. 2.5. Schematic drawing of RF sputtering system.

2.1.6 Photo-lithography

In this study, to pattern the TiN gate of the MIS capacitor, photo-lithography process was used. The various step of the photo-lithography performed in this study are summarized bellow.

Prior to application of resist, the bake was conducted at a temperature of 100^{o}C for 5min. Then a liquid adhesion promoter (OAP, Tokyo Ohka Co. Ltd.) was coated at 500 rpm for 5 sec followed by 5000 rpm for 20 sec. And then, the photoresist OFPR-50 cp (Tokyo Ohka Co. Ltd.) was coated at 500 rpm for 5 sec followed by 5000 rpm for 20 sec. After the coating photoresist, pre-baking was conducted at a temperature of 110^{o}C for 90 sec. The photoresist is exposed through the mask with high-intensity ultraviolet light. In this study, exposure process was performed by contact-type mask aligner, MJB3 (Karl Suss Co. Ltd.). The photoresist was developed using the MND-3 (Tokyo Ohka Co. Ltd.) Following the development, additional baking was conducted process at 110^{o}C for 5 min. After gate patterning was performed by etching process, photoresist was removed by acetone.

2.1.7 Etching Process

In this study, wet chemical etching was used to etch TiN. For the etchant, the solution of NH_4OH / H_2O_2 = 1 / 1 was used. At room temperature, etching rate of this solution is about 5 nm / min. The gate patterned sample of TiN/SiO_2/n-Si(100) is shown in Fig. 2.6.

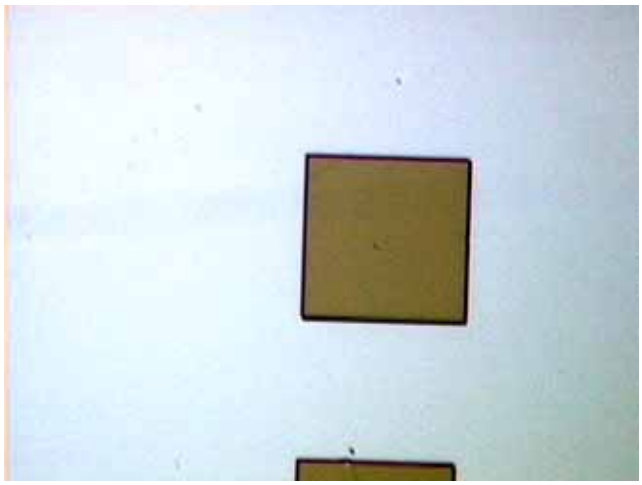


Fig. 2.6. A photograph of patterned TiN film using NH_4OH:H_2O_2 solution.

2.2 Characterization Methods

2.2.1 Electrical Characteristics

2.2.1.1 Capacitance-Voltage (C-V) Characteristics

Capacitance vs. voltage (C-V) characteristics was measured by precision LCR meter (HP4284A, Hewlett-Packard Co. Ltd.) at the frequency range from 10 kHz to 1 MHz.

Ideal C-V characteristics and effect of interface state on C-V characteristics of MIS capacitor is shown in Fig. 2.7. As shown in Fig. 2.7, in the case of interface state exists in the MIS capacitor, the capacitance at low frequency is lager than that of high frequency, because the response of the filling and emptying interface states cannot follow the applied ac signal at high frequency. From the accumulation capacitance at 1 MHz, capacitance equivalent oxide thickness (CET) is calculated as

$$CET = \varepsilon_0 \cdot \varepsilon_{SiO2} \frac{S}{C} \qquad (2.1)$$

where ε_0, ε_{SiO2} and S are permittivity of vacuum, dielectric constant of SiO_2 and area of MIS capacitor respectively.

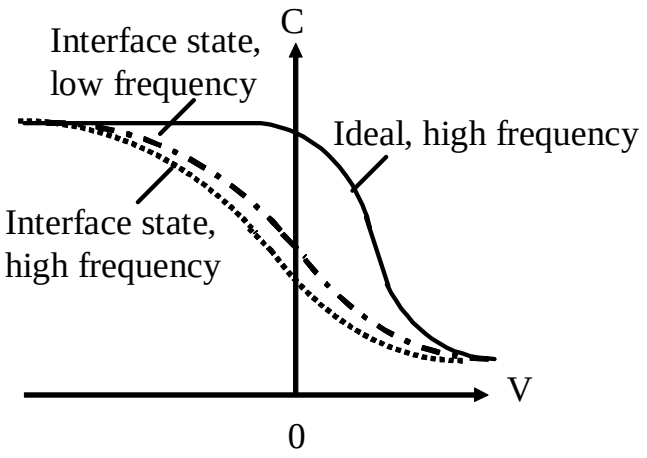


Fig. 2.7. Typical C-V characteristics of MIS capacitor in case of p-type semiconductor.

2.2.1.2 Leakage Current Density-Voltage (J-V) Characteristics

To suppress the leakage current density is one the most essential purpose to use high-k in LSI for the suppression of power consumption. Leakage current density vs. voltage (J-V) characteristics was measured by semiconductor-parameter analyzer (HP4156C, Hewlett-Packard Co. Ltd.).

2.2.2 Atomic Force Microscope (AFM)

The surface morphology of the film was observed by Atomic Force Microscope (AFM, Nano Scope 3, Digital Instrument Co. Ltd.) in tapping mode. The scan rate was generally selected to 1 Hz. The measurement area was 500 nm square.

2.2.3 X-ray Diffraction (XRD)

XRD is a method for determining the arrangement of atoms in a substance. Since the wave length of x-rays is comparable to atomic spacings, diffraction can occur. Bragg's law shows the relationship between the angle measured for each peak and the corresponding spacing:

$$n\lambda = 2d\sin\theta \qquad (2.2)$$

where n is an integer, γ is the wavelength of the radiation, d is the spacing between adjacent planes in a crystal, and θ is the Bragg angel. In this study, crystallinity of the sample was evaluated by X-ray Diffraction method (XRD, RIGAKU Co. Ltd.) using the θ-2θ method with Cu $K\alpha$ radiation. The values of tube voltage and current were 35 kV and 20 mA, respectively.

2.2.4 X-ray Photoelectron Spectroscopy (XPS)

In XPS, also called electron spectroscopy for chemical analysis (ESCA), a beam lf low-energy x-rays is used to probe the sample surface. All the photon energy is absorbed and interacts with the inner shell electrons, causing photoemission of an electron. The electronic transition is shown in Fig. 2.8. From the measured kinetic energy of the emitted electron (E_{kin}), its binding energy (E_B) can be calculated from the known photon energy ($h\upsilon$) and the difference in work function between the sample and the spectrometer ($\Delta\phi$):

$$E_K = h\upsilon - E_B - \Delta\phi \qquad (2.3)$$

In this study, PHI model 550ESCA with the K-α line of the Mg (1253.6 eV) was used.

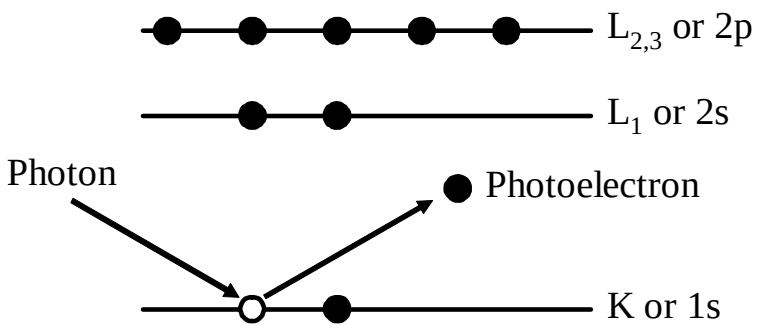


Fig. 2.8. Electronic transition involved on XPS.

2.2.5 Rutherford Backscattering Spectrometry (RBS)

Rutherford Backscattering Spectrometry (RBS) yields quantitative information about elemental and quantitative depth profiles and is used in the analysis of both metal and dielectrics. In this study, to measure the amount of the atoms on the substrate, RBS method was used. The basis for the measurement is the scattering of impinging ^{4}He ions by atoms (of mass > mass of ^{4}He) in a solid. The energy of the ion and the scattering angle were selected at 1.5 MeV and 15^o, respectively.

2.2.6 Four-Terminal Method

Four-terminal method was used to measure the resistivity of the TiN metal film. The schematic image of the four-terminal method is shown in Fig. 2.9. For a thin wafer with thickness W much smaller than either a or d, the sheet resistance is given by

$$Rs = \frac{V}{I} \cdot CF \qquad (2.4)$$

where CF is the correction factor shown in Fig. 20. The resistivity is calculated below,

$$\rho = R_s W \qquad (2.5)$$

In this study, the length of *s* is 1mm.

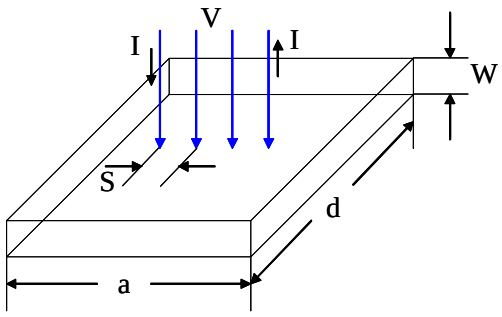


Fig. 2.9. Schematic drawing of direct measurement of sheet resistance using four-point probe.

Chapter 3.

Stability of Rare Earth Metal Oxides for Wet Process

3.1 Introduction

Firstly, for the application of wet process, the stabilities of rare earth metal oxides thin films for moisture ambient, ultra-pure water (UPW) and resist process were investigated.

3.2 Experimental Procedure

Figure 3.1 shows experimental procedure. high-k thin films were deposited directly on chemically cleaned HF-last n-type silicon (100) substrates by using ultra high vacuum molecular beam deposition (MBD). The pressure during the deposition was 10^{-9}~10^{-6} Torr. The deposited films were subsequently annealed by RTA (Rapid Thermal Annealing) at 600^{o}C in N_2 for 5min. Then, the stability tests for moisture ambient, ultra-pure water and resist processes were carried out for these samples. For the stability tests for moisture ambient, ZrO_2 and various rare earth oxides (La_2O_3, Pr_2O_3, Sm_2O_3, Eu_2O_3, Gd_2O_3, Dy_2O_3, Yb_2O_3, and Lu_2O_3), were investigated. Table 3.1 shows sample fabrication conditions for each material. Figure 3.2 shows the experimental equipment for moisture absorption test. Ultra-pure water was used as the moisture supply. The samples were kept in moisture ambient for 120 hours. During the test, the temperature and humidity were maintained at 20^{o}C and 80%, respectively. To investigate the stability for ultra-pure water, high-k thin films were dipped in ultra-pure water. To investigate the stability for the resist process, OFPR (30cp) was spin coated to the films, and stripped 30 minutes later by acetone. Finally, for the electrical measurement, Al electrodes (ϕ100 μm) were deposited by vacuum evaporation as top and bottom electrodes through a metal hard mask. In this study, the tests after Al gate electrode formation were also carried out to investigate whether the film degradation could be suppressed or not by the gate electrode coverage.

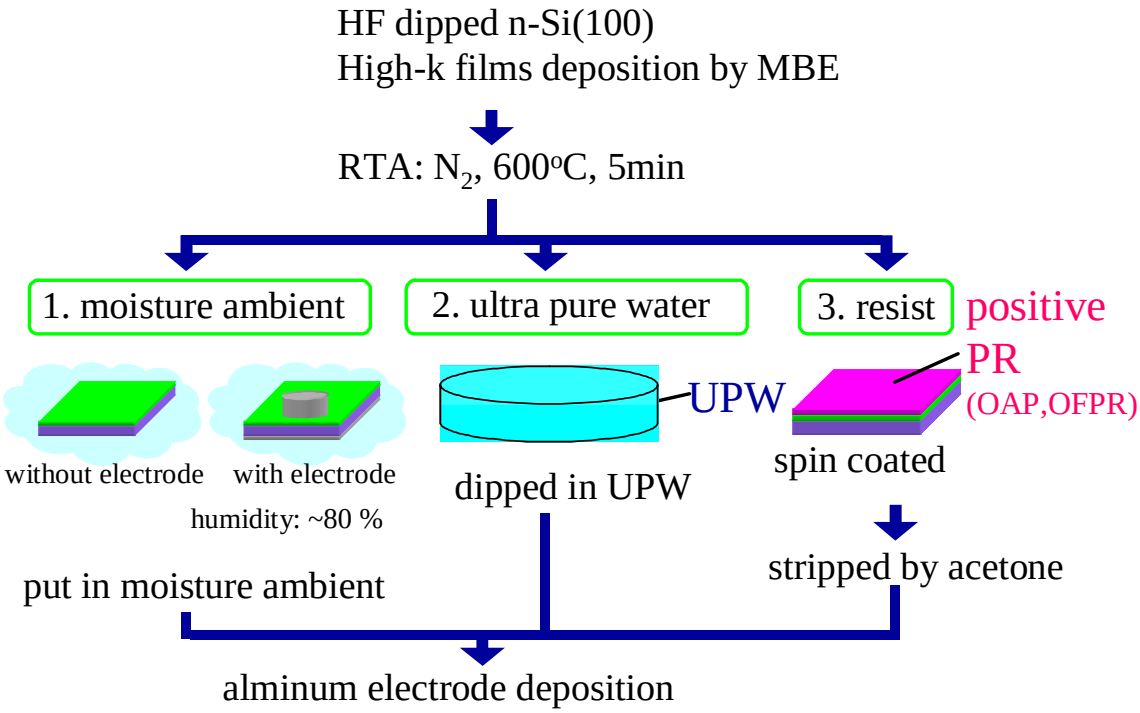


Fig. 3.1. Experimental procedure.

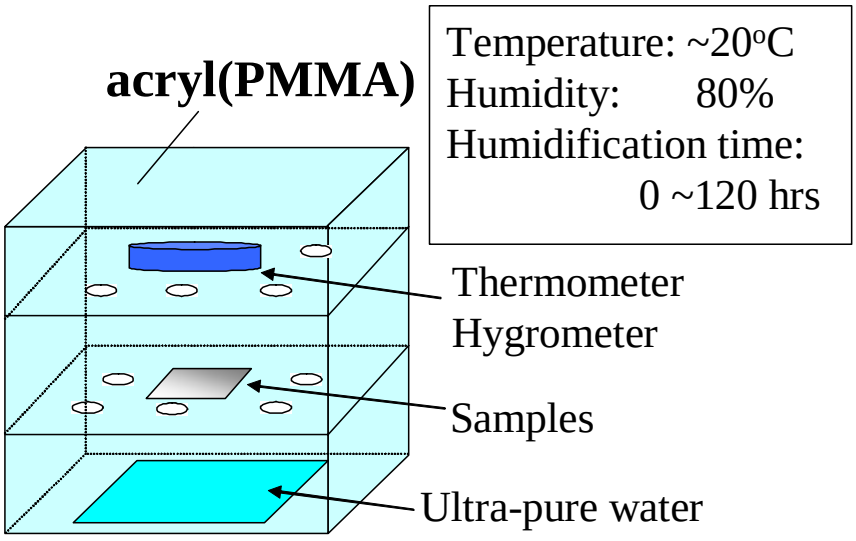


Fig. 3.2. Experimental equipment for the moisture test.

Table 3.1. Sample fabrication conditions.

	La_2O_3	Pr_2O_3	Sm_2O_3	Eu_2O_3	Gd_2O_3	Dy_2O_3	Yb_2O_3	Lu_2O_3	ZrO_2	SiO_2
$T_{sub.}$ (°C)	250	R.T.	R.T.	250	250	R.T.	R.T.	R.T.	R.T.	-
$T_{phys.}$ (nm)	5	7	7.5	3	10.5	5.5	4	3	2.5	5

3.3 Stability of Rear Earth Metal Oxides for the Moisture Ambient

3.3.1 Characterization of the film properties for without electrode samples

Figure 3.3 shows changes of C-V characteristics at 100 kHz for MIS capacitor of ZrO_2, Yb_2O_3 and Sm_2O_3 before and after the moisture absorption tests. After the test, not only rare earth oxides, but also ZrO_2 showed the decrease of accumulation capacitance and significant degradation of C-V characteristics.

Figure 3.4 shows the change of J-V characteristics of ZrO_2, Yb_2O_3 and Sm_2O_3, respectively. These are corresponded to the C-V data which was shown in Fig.3.3. In the case of ZrO_2 and Yb_2O_3, the leakage current density @+1V decreased after the test. On the other hand, the leakage current density of Sm_2O_3 increased. In general, the moisture-absorbed thicker film is expected to have smaller leakage current. However, when the roughness of the film increases, the leakage current is expected to increase. It can be explained by the surface roughness observation, as shown below.

Figure 3.5 shows the typical AFM images of ZrO_2, Yb_2O_3 and Sm_2O_3 films before and after the test. The scan size was 0.5 x 0.5 nm and the z direction was 5 nm / div. The surface roughness of ZrO_2 and Yb_2O_3 changed little, while that of Sm_2O_3 became dramatically large. It was considered that this rough surface caused the increase of leakage current density for Sm_2O_3 film after the test.

Figure 3.6 and 3.7 shows the degradation of film characteristics for all studied samples. Figure 3.6 shows change of CET − Capacitance Equivalent Thickness, before and after the test for all studied samples. All high-k films, even including ZrO_2, showed significant degradation or increase of CET after the tests, while no degradation was observed for SiO_2, indicating very good stability in moisture ambience. Figure 3.7 shows surface roughness dependence on the degradations of leakage current density. From this figure, it is clear that there is strong relation between degradation of leakage and film roughness.

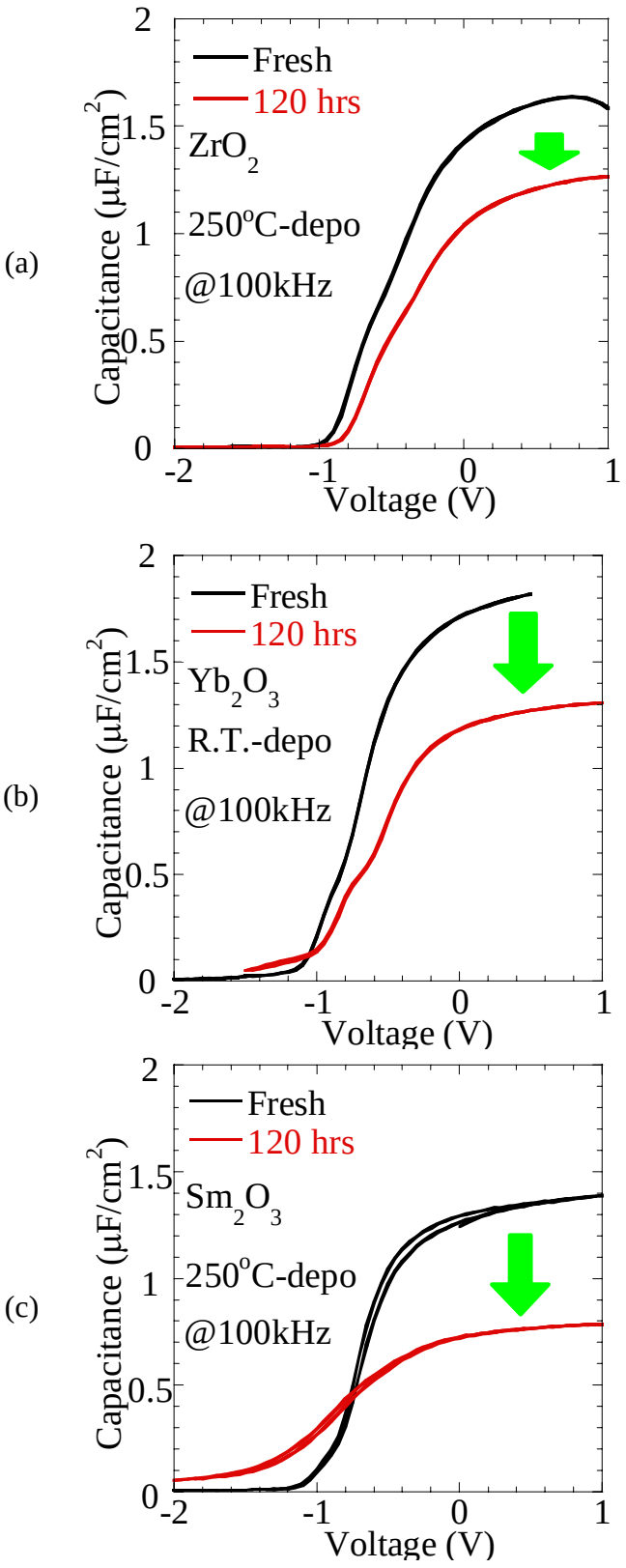


Fig. 3.3. Change of C-V curves for (a) ZrO_2, (b) Yb_2O_3, (c) Sm_2O_3 before and after the moisture stability test.

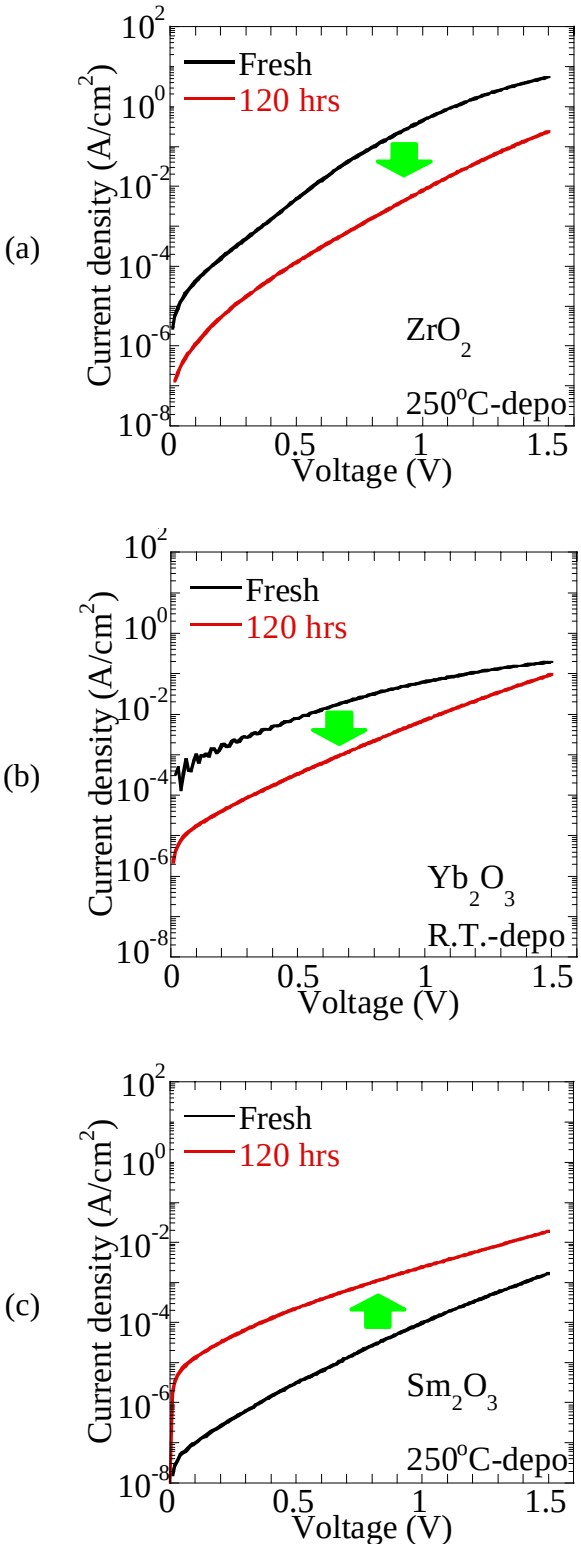


Fig. 3.4. Change of J-V curves for (a) ZrO_2, (b) Yb_2O_3, (c) Sm_2O_3 before and after the moisture stability test.

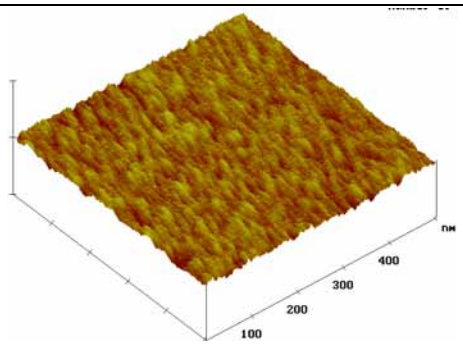
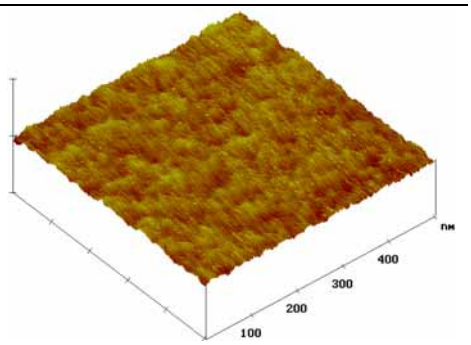
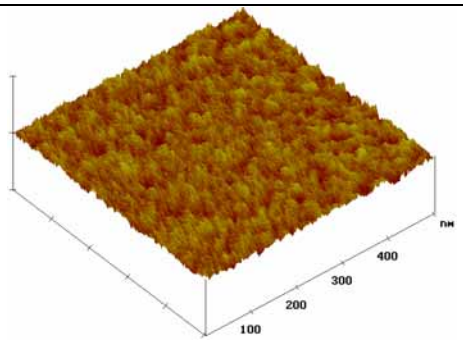
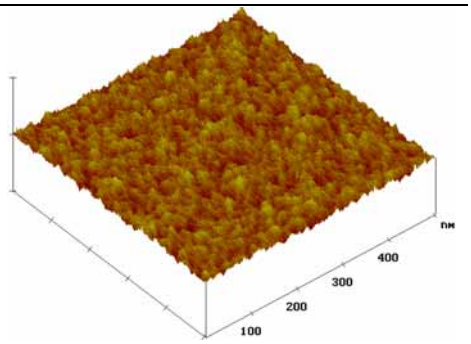
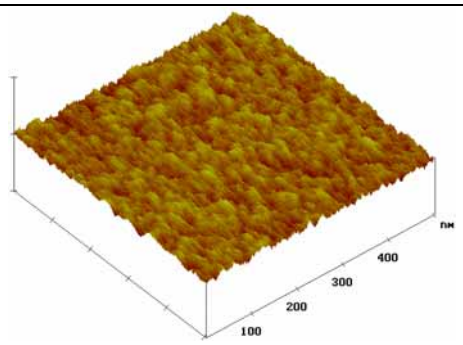
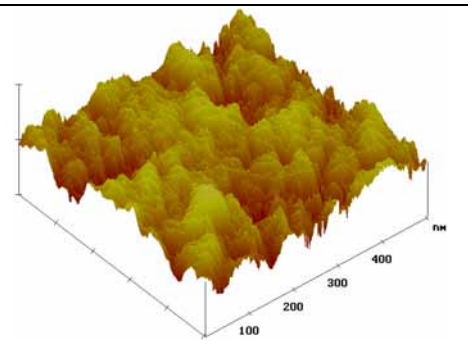
	Fresh	120 hours
(a) ZrO_2	 RMS:0.144 nm	 RMS:0.136nm
(b) Yb_2O_3	 RMS:0.162 nm	 RMS:0.167nm
(c) Sm_2O_3	 RMS:0.187 nm	 RMS:0.898 nm

Fig. 3.5. Degradation of surface roughness for (a) ZrO_2, (b) Yb_2O_3, (c) Sm_2O_3 before and after the moisture stability test.

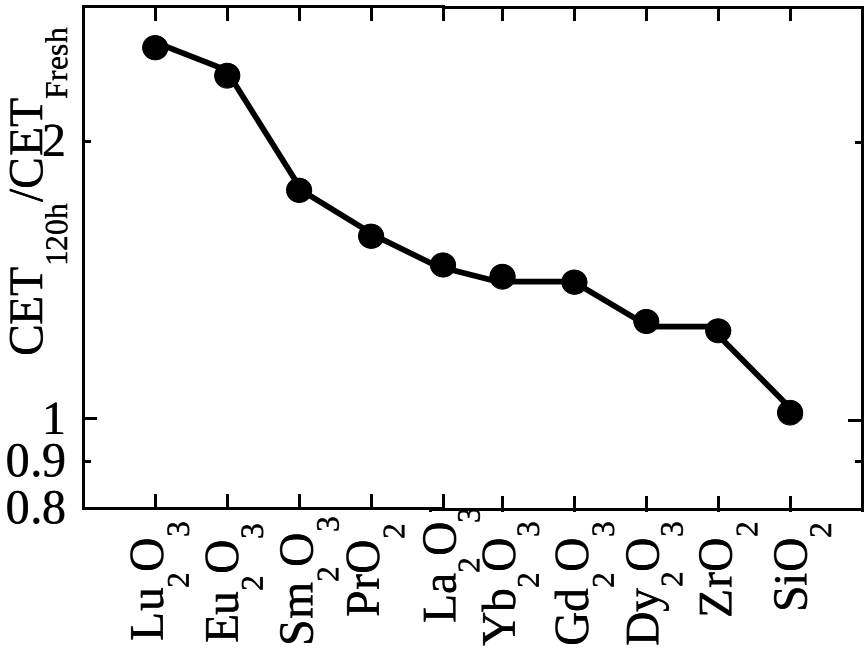


Fig. 3.6. CET_{120hrs}/CET_{Fresh} for all studied samples.

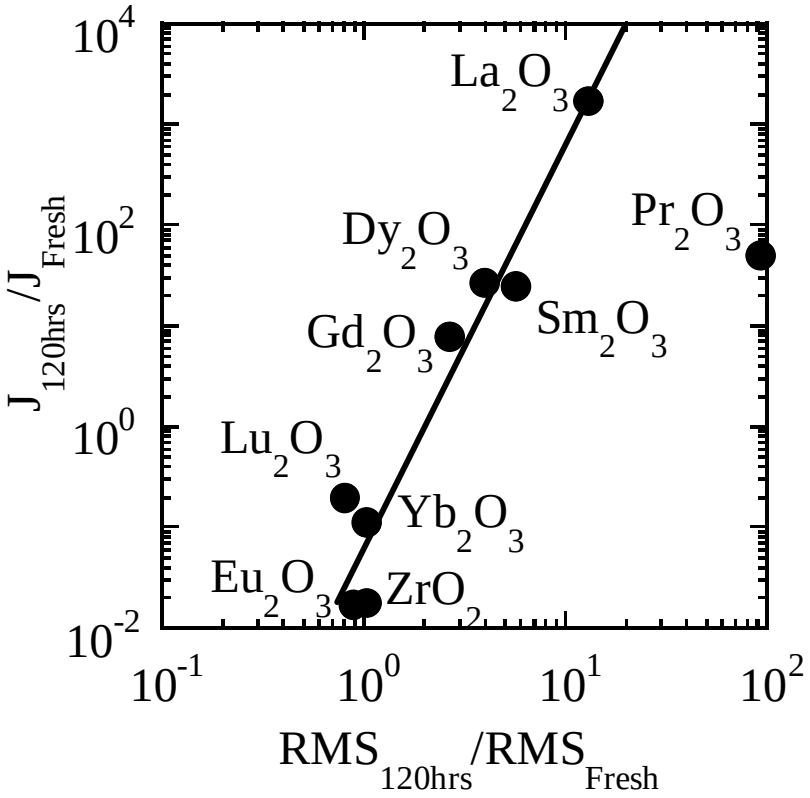


Fig. 3.7. J_{120hrs}/J_{Fresh} vs. RMS_{120hrs}/RMS_{Fresh} for all studied samples.

3.3.2 Characterization of the film properties for with electrode samples

The moisture absorption test after Al electrode deposition was also carried out. In Fig. 3.8 and Fig. 3.9 C-V and J-V characteristic of before and after the test were shown. There was little degradation observed even after 120 hours test. It was found that the degradation was completely suppressed by gate electrode coverage.

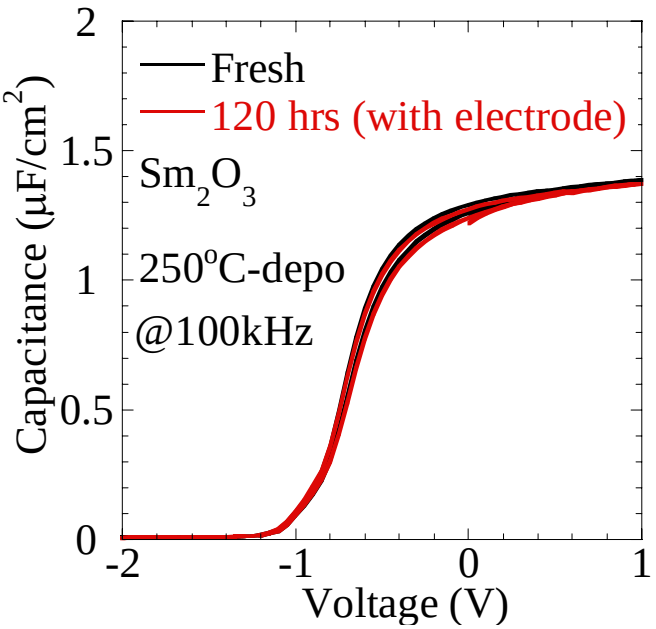


Fig. 3.8. Change of C-V characteristics for Sm_2O_3 (with electrode sample).

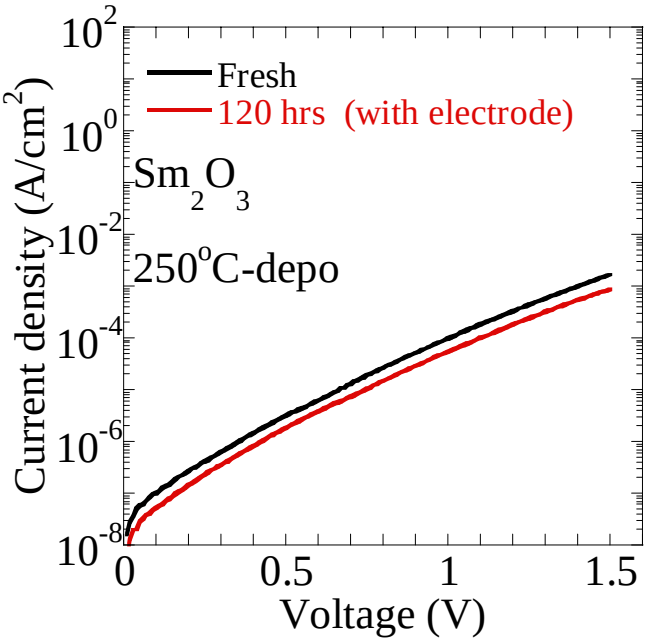


Fig. 3.9. Change of J-V characteristics for Sm_2O_3 (with electrodes sample).

3.4 Stability of Rear Earth Metal Oxides for the Ultra-Pure Water

3.4.1 Characterization of the film properties for without electrode samples

First, the stability tests for ultra-pure water were carried out. Figure 3.10 shows change of high-frequency C-V characteristics (@100 kHz) for Al/Lu_2O_3/n-Si(100). Lu_2O_3 is one of the rare earth oxides, and it is considered to be one of the most stable materials because of its highest lattice energy among the rare earth oxides. The time in the plot indicates dipped time in the ultra-pure water. The C-V curve of the sample which was dipped 5 minutes in ultra-pure water changed little. However, the accumulation capacitance of 30 minutes dipped sample was increased significantly, and it started to decrease 1 hour later. The C-V curve for 24 hours dipped sample was not good enough to obtain a reliable EOT value because of its huge leakage current.

Figure 3.11 shows change of J-V characteristics for Lu_2O_3 before and after the test. In the case of J-V characteristics, a drastic increase of the leakage current was observed after the test. From these changes in electrical characteristics, the film was expected to become thin during the dip.

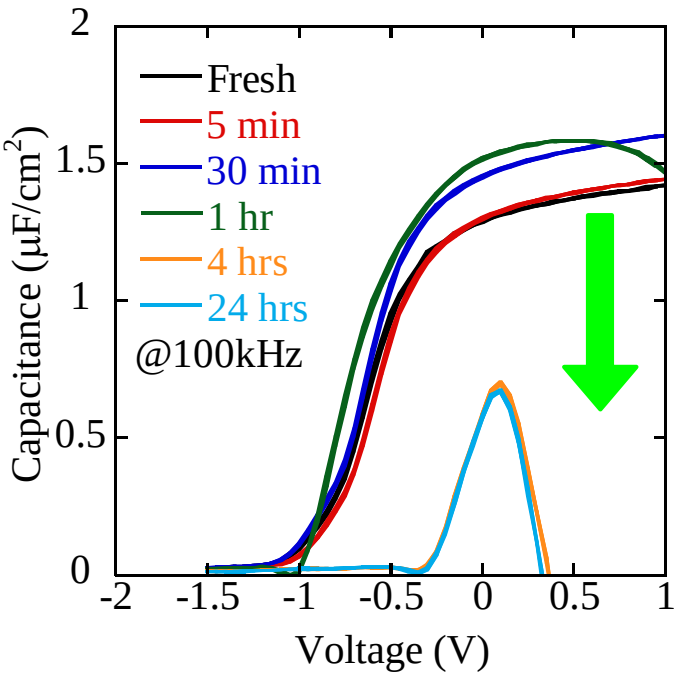


Fig. 3.10. Change of C-V of Lu_2O_3 before after the UPW stability test.

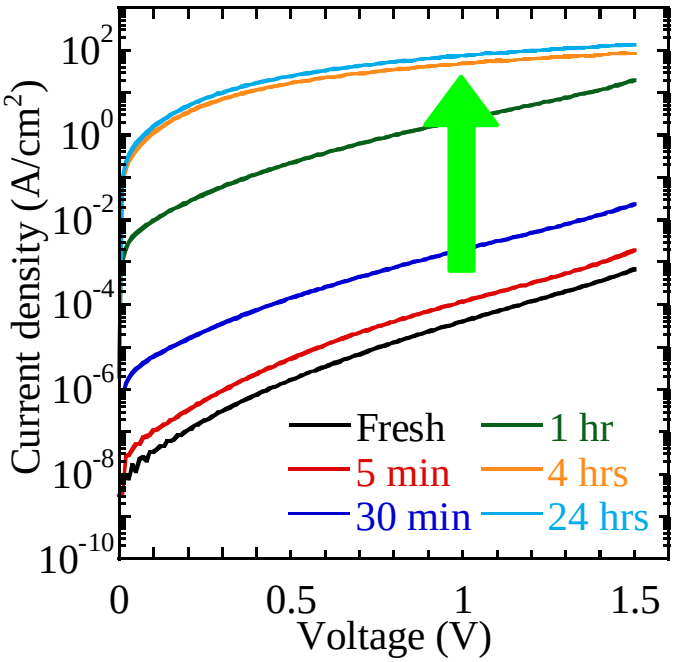


Fig. 3.11. Change J-V characteristics of Lu_2O_3 before after the UPW stability test.

The x-ray photoelectron spectroscopy (XPS) spectra was obtained by a PHI model 550 ESCA spectrometer. Figure 3.12 shows Lu 4d photoelectron spectra for fresh, 24 hours dipped in ultra-pure water and etched sample, respectively. Photoelectron take-off angle is 45^{o}. From Lu 4d spectra, it was found that Lu was completely vanished after 24 hours test, as same as the sample which was etched by HCl.

To clarify the reduction of the film during the dipped test, we performed RBS measurement. Figure 3.13 shows RBS spectra for Lu_2O_3 film. As shown inset of Fig. 3.13, it is clear that the amount of Lu atoms in the film was decreased with the dipped time. Lu_2O_3 is assumed to be dissolved in ultra-pure water after the test.

Figure 3.14 shows the typical AFM images for (a) fresh sample, (b) 30 minutes dipped sample and (c) 1 hour dipped sample, respectively. According to this figure, the surface of Lu_2O_3 became a little bit rough by dipped longer time.

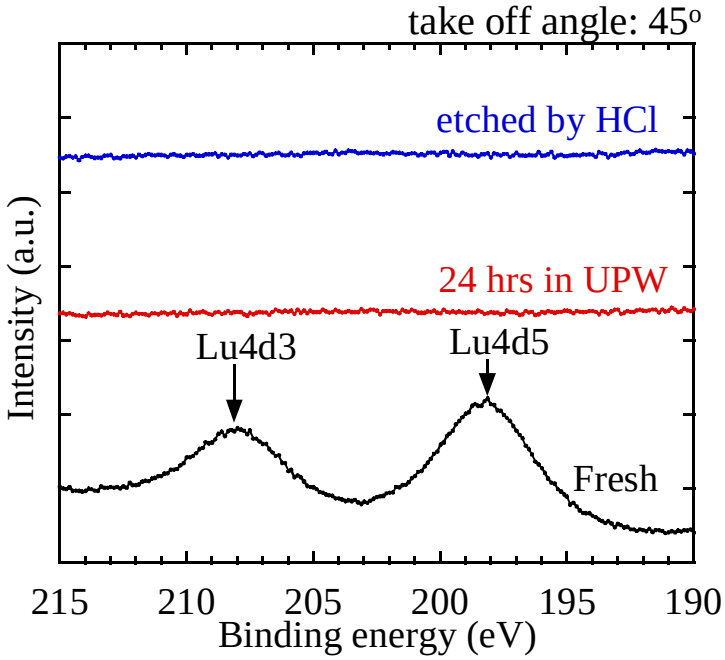


Fig. 3.12. XPS spectra of Lu4d of the Lu_2O_3 films for Fresh, dipped in UPW for 24 hours, etched by acetone.

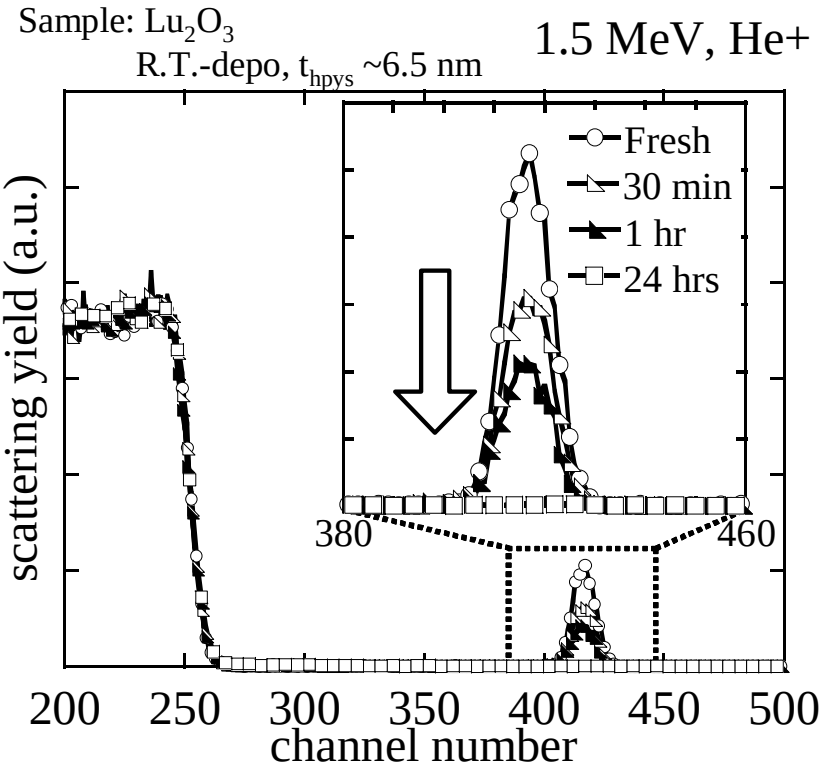


Fig. 3.13. Change of RBS spectra of Lu_2O_3 before and after the UPW stability test.

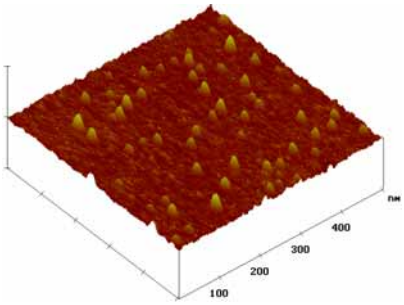
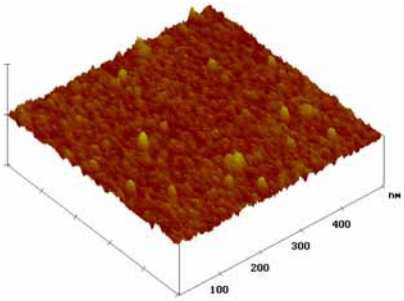
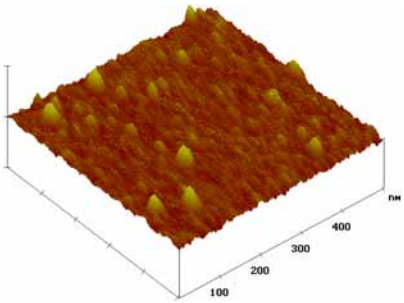
Fresh	 RMS: 0.197 nm
30 min in UPW	 RMS: 0.202 nm
1 hr in UPW	 RMS: 0.228 nm

Fig. 3.14. AFM images for Fresh, 30 minutes later and 1 hour later samples (0.5x0.5 μm, z: 5 nm/div).

Figure 3.15 shows the change of electrical characteristics for ZrO_2 before and after the test. It should be noted that after 24 hours test, the accumulation capacitance decreased compared with that of the fresh sample. That of EOT value increased at 5 %.

As a reference, the test for SiO_2 film was also carried out. The physical thickness of SiO_2 is 5 nm. In the case of SiO_2, as shown in Fig. 3.16, little degradation of accumulation capacitance was observed even after 24 hours test. It was confirmed that SiO_2 has good stability for ultra-pure water.

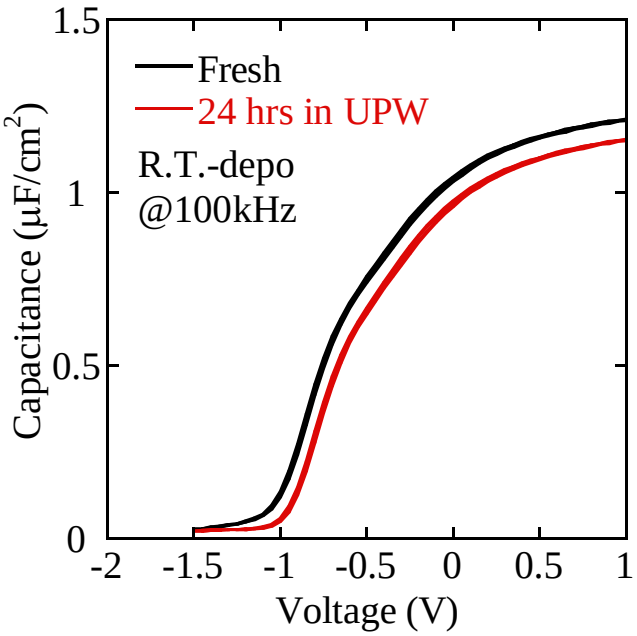


Fig. 3.15. C-V characteristics for ZrO_2 before and after the UPW stability test.

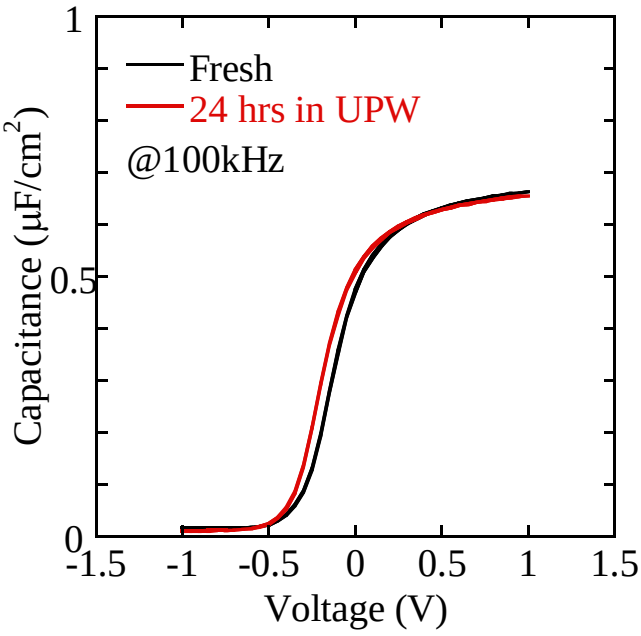


Fig. 3.16. C-V characteristics for SiO_2 before and after the UPW stability test.

3.4.2 Characterization of the film properties for with electrode samples

The dipping test in ultra-pure water after Al electrode deposition was also carried out. In Fig. 3.17, C-V characteristic of before and after the test were shown. There was little degradation observed even after the 24 hours dipping test. It was found that the degradation was completely suppressed by gate electrode coverage.

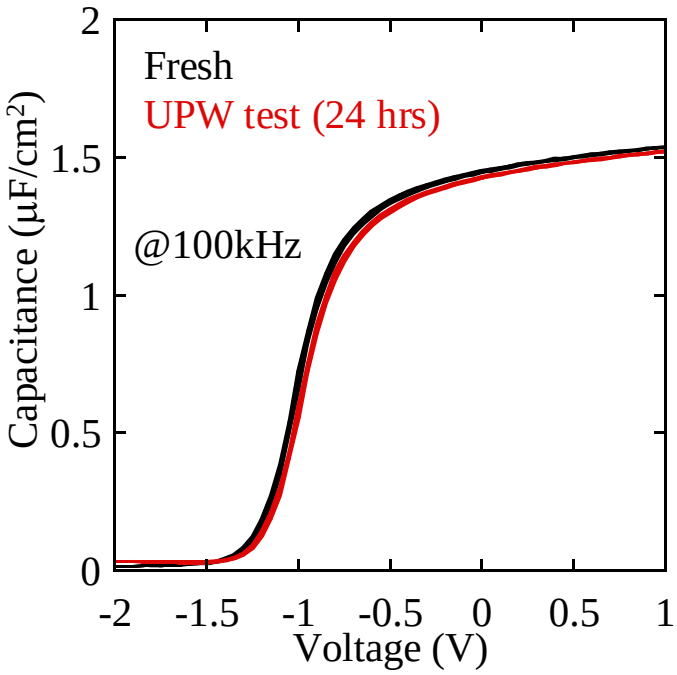


Fig. 3.17. Change of C-V characteristics for La_2O_3 (with electrode sample).

3.5 Stability of Rear Earth Metal Oxides for the Resist Process

3.5.1 Characterization of the film properties for without electrode samples

The test of the stability of rare earth oxide thin films for the resist process was also carried out. Figure 3.18 shows the change of C-V characteristics for Lu_2O_3 before and after the test. The accumulation capacitance decreased significantly after the test, and ion-drift type hysteresis loop was also observed. Figure 3.19 shows J-V characteristics of the same samples. The leakage current density of the sample which was applied resist decreased 4 orders of magnitude than that of fresh film. From these changes of electrical characteristics, the thickness of the film expected to increase after the test.

Figure 3.20 shows the AFM images of Lu_2O_3 for (a) before and (b) after the test. The RMS (Root Means Square) was degraded from 0.112 nm to 0.436 nm after the test. It was considered that the film became very rough because the film reacted with the resist. This was also the reason that the sample showed degraded electrical characteristics after the test.

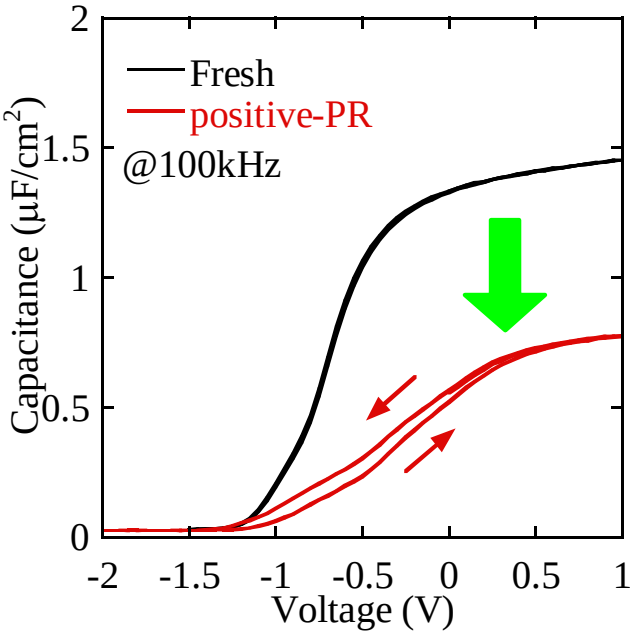


Fig. 3.18. Change of C-V characteristics for Lu_2O_3 before and after the resist stability test.

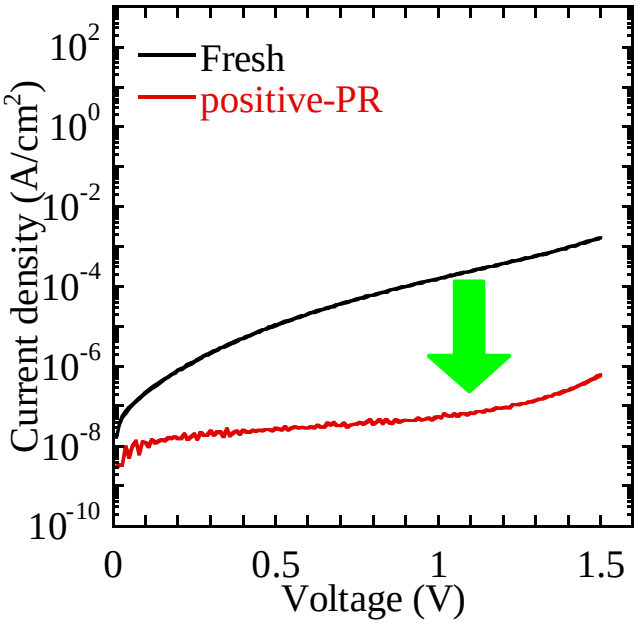


Fig. 3.19. Change of J-V characteristics for Lu_2O_3 before and after the resist stability test.

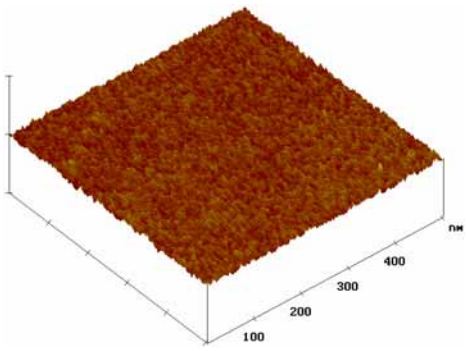
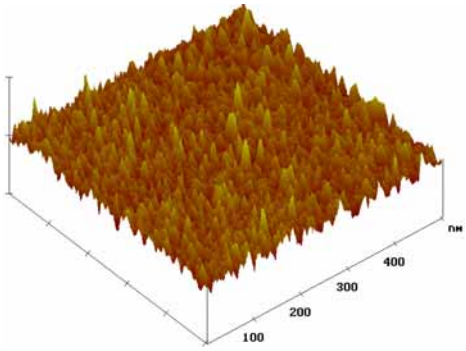
Fresh	After the resist test
	
RMS: 0.122 nm	RMS: 0.436 nm

Fig. 3.20. Change of surface roughness for Lu_2O_3 before and after the resist stability test.

In order to clarify the effect of resist-removal process on the film degradation, the stability test for acetone was carried out. As shown in Fig. 3.21, accumulation capacitance decreased after dip in acetone. However, the degradation of C-V characteristics is much smaller than that of resist applied sample. This result suggests that the degradation of the film during the resist process is mainly caused by the resist (OFPR-50cp).

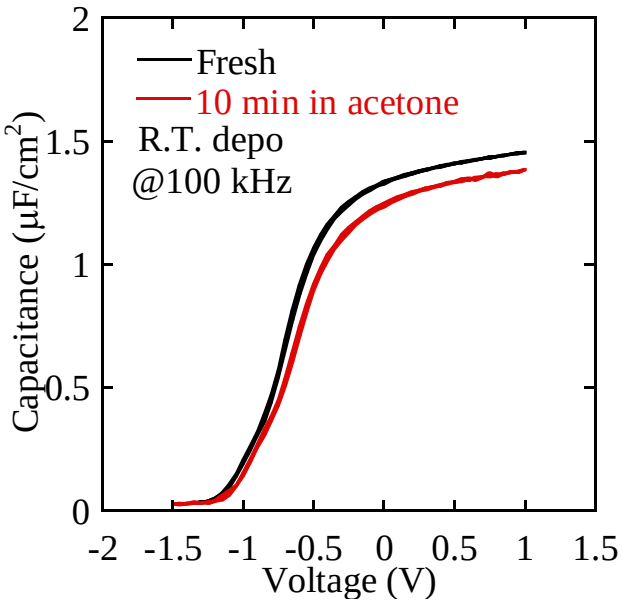


Fig. 3.21. Change of C-V curves for Lu_2O_3 before and after acetone dipping.

3.5.2 Characterization of the film properties for with electrode samples

The dipping test in ultra-pure water after Al electrode deposition was also carried out. In Fig. 3.22, C-V characteristic of before and after the test were shown. There was little degradation observed even after the resist process test. It was found that the degradation was completely suppressed by gate electrode coverage.

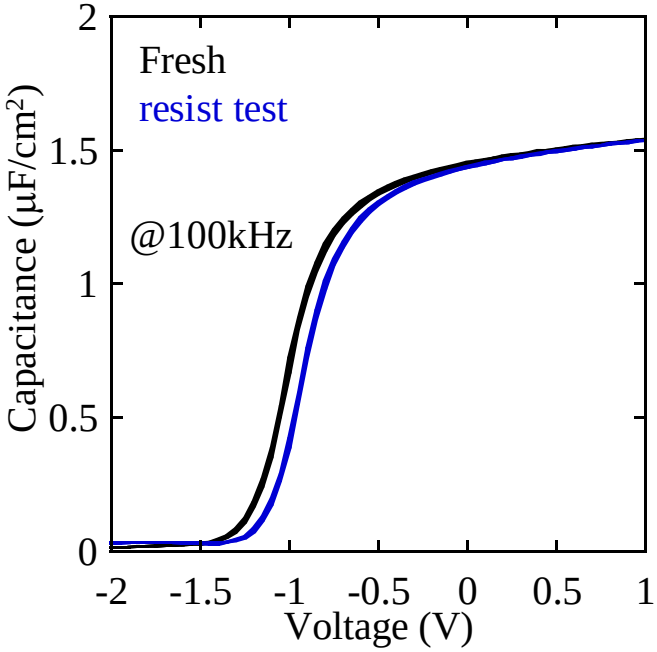


Fig. 3.22. Change of C-V characteristics for La_2O_3 (with electrode sample).

3.6 Summary

The stability of high-k thin films for moisture ambient and wet processes was investigated. Not only rare earth oxides but also ZrO_2 was degraded in moisture ambient. It was also found that rare earth oxides thin films completely dissolved in ultra-pure water after 24 hours. Additionally, rare earth oxides showed weak stability against the resist processes. However, It was confirmed that the degradation was completely suppressed by gate electrode.

Chapter 4.

Stability of Rare Earth Metal Oxides with TiN electrode for Heat Process

4.1 Introduction

For the preliminary step to the investigation of the stability of high-k thin films for the heat process, TiN was investigated which has been one of the leading candidates to be the next generation of metal gate electrode due to its chemical and metallurgical stability. Also, TiN shows good adhesion to SiO_2 because the free energy change of oxidation is lower in the Ti-O system than in the Si-O system. The physical properties for various gate metal materials are shown in Table 4.1.

One of the biggest problems of TiN is that TiN has a tendency to strongly react with oxygen. Generally, the oxidation of the metal gate electrode is not taken up to the problem because S/D activation anneal is carried out in the nitrogen ambient. However, concerning about device integration and the existence of residual oxygen in the nitrogen ambient, the oxidation might occur and become severe damage to the devices.

In this chapter, the fundamental characteristics of TiN electrode deposited by reactive sputtering are discussed.

Table 4.1. Physical properties for various gate metal materials.

Materials	W	TiN	Ta	Mo	Ti	Al
Melting point (°C)	3387	2950	2996	2610	1675	660
Resistivity (μΩ-cm)	6-15	50-200	15-20	6-15	45-50	3-4
Schottky barrier hight (eV) (on n-type Si)	0.65-0.7	0.45-0.5	0.55-0.6	0.6-0.7	0.5-0.55	0.65-0.75

4.2 Experimental Procedure

The TiN layers were deposited upon the thermal oxidized SiO_2 layers. The thickness of the SiO_2 is 5 nm. The base pressure was 1.5×10^{-5} Pa, and during the deposition, the pressure was kept at 6.0×10^{-1} Pa. Before the deposition, the target was pre-sputtered in the Ar gas for 10 min. Two targets were used, one is Ti target and another is TiN alloy target. The gas flow ratio of N_2 / Ar + N_2 was changed from 0% to 33%. The RF power was changed from 100 W to 150 W. The deposition temperature was fixed at room temperature (R.T.). The deposition rate was typically 2 nm/min. The thickness of TiN was kept at approximately 150 nm. After the deposition of the TiN films, the samples were annealed (Post Metal Anneal, PMA) in

nitrogen ambient at 400^{o}C to 800^{o}C for 5 min. And then, resistivity by four probe method, XPS, XRD measurement was carried out.

Additionally, TiN/La_2O_3/n-Si(100) MIS capacitor was fabricated to investigate its electrical characteristics. After the deposition of TiN electrode, the gate of 60 nm x 60 nm square was patterned by photolithography and etching process. CV and JV characteristics measurement were carried out.

4.3 Characterization of TiN Electrode

4.3.1 Optimal Deposition Conditions of TiN Films

To obtain the stoichiometric TiN film with good property, various conditions were carried out.

First, gas flow dependence on the property of TiN films was investigated. During this investigation, gas flow ratio of N_2 / Ar + N_2 was changed form 0% to 33%. The conditions except gas flow ratio were fixed. The RF power was fixed at 100 W. Two targets, Ti and TiN alloy were used for the deposition.

Figure 4.1 shows dependence of the resistivity of TiN films on gas flow ratio of N_2 / Ar + N_2. From this figure, there is little change from the N_2 / Ar + N_2 ratio of 0% to 20%. However, the resistivity of the TiN films increased with increasing N_2 flow lager than the N_2 / Ar + N_2 ratio of 20%. It is known that resistivity values are related to the x of TiN_x. In the case of the sample which was deposited with the gas ratio of N_2 / Ar + N_2 33%, the x of TiN_x was expected lager than 1, and it caused large resistivity. Figure 4.2 shows dependence of the RMS (Root Means Square) of the surface roughness on gas flow ratio of N_2 / Ar + N_2. From Fig. 4.2, to much N_2 causes increase of surface roughness.

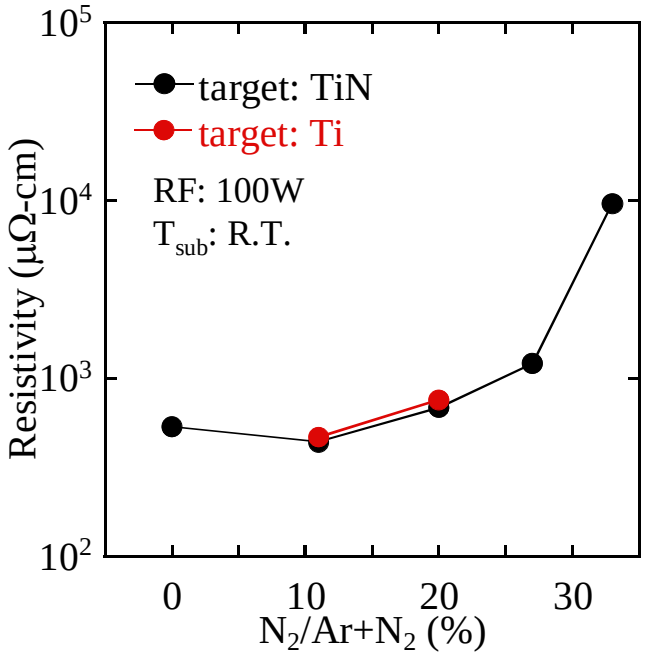


Fig. 4.1. Dependence of the resistivity of TiN films on gas flow ratio of N_2 / Ar + N_2.

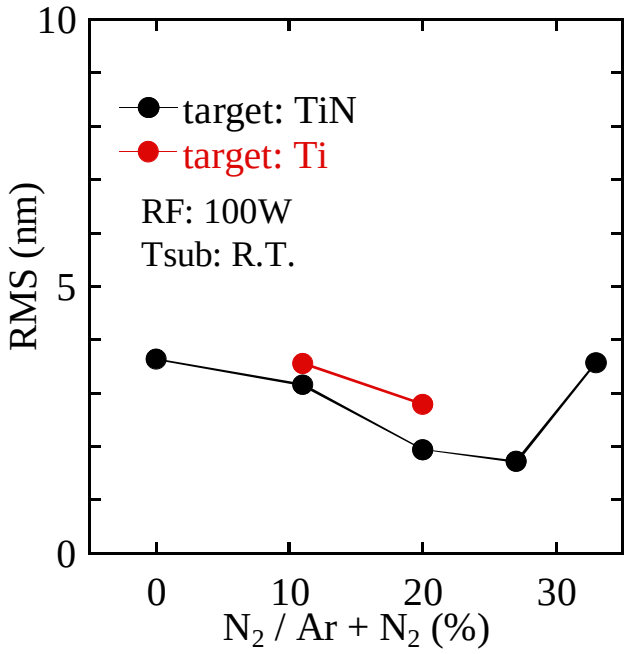


Fig. 4.2. Dependence of the RMS (Root Means Square) of the surface roughness on gas flow ratio of N_2 / Ar + N_2.

Secondly, RF power dependence on the property of TiN films was investigated. During this investigation, RF power was changed form 100 W to 150 W. The conditions except RF power were fixed. The gas flow ratio of N_2 / Ar + N_2 was fixed at 20%. Two targets, Ti and TiN alloy were used for the deposition.

Figure 4.3 shows dependence of the resistivity of TiN films on RF power. From this figure, there is a little decrease of resistivity with Ti target at 100 W. However, the decrease of the resistivity is not dramatically. From the view point to minimize radiation-induced damage of the gate insulator during the sputtering, the RF power must be kept as low as possible. Therefore, the condition of the sputtering with RF power kept at 100 W was selected.

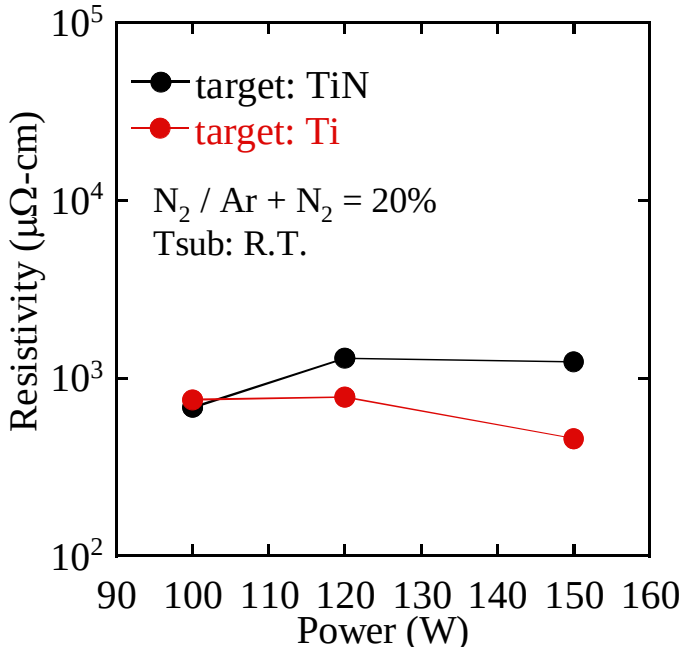


Fig. 4.3. Dependence of the resistivity of TiN films on RF power.

Figure 4.4 shows XPS depth profiling of the sample with the TiN layer grown on a SiO_2/Si(100) substrate. The time in the graph indicates sputtered time. The Ti 2p binding energies are assignable to Ti $2p_{1/2}$ at high energy and Ti $2p_{3/2}$ at low energy. The Ti 2p spectra of the without sputtering sample in Fig.4.4 shows Ti-O peaks at a binding energy of 458.1 eV for the native oxide. The native oxide layer was removed after sputtering of 5 min, as seen by the decrease in the Ti-O peak at binding energies of 458.1 (Ti $2p_{3/2}$) and 464.1 eV (Ti $2p_{1/2}$) as shown in Fig. 4.4. After the sputtering for 5 min, the dominant peaks are Ti-N peaks at binding energies of 455.2 (Ti $2p_{3/2}$) and 461.1 (Ti $2p_{1/2}$) eV. From this XPS profiles, it was confirmed that TiN films with good binding states of Ti-N was fabricated.

Based on those results, the deposition condition to investigate the thermal stability of TiN gate electrode was determined like that using Ti target with the gas flow ratio of N_2 / Ar + N_2, and RF power 100 W.

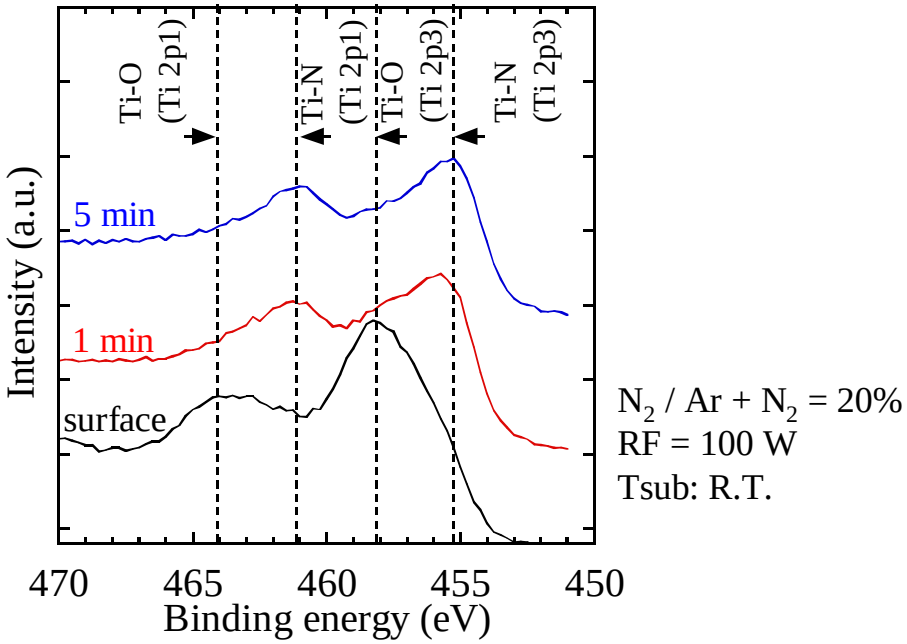


Fig. 4.4. XPS Ti2p spectra as a function of removal time of TiN.

4.3.2 Thermal Stability of TiN Gate Electrode

To investigate the thermal stability of TiN films, the samples were annealed (Post Metal Anneal, PMA) in nitrogen ambient from 400°C to 800°C for 5 min. Figure 4.5 shows the resistivity and RMS of TiN films as a function of the post metal annealing (PMA) temperature. As shown in this figure, the samples which were annealed under 600°C, the values of the resistivity and RMS changed little. On the other hand, TiN which was annealed at 800°C of values increased abruptly. Figure 4.6 shows AFM images of surface of these TiN samples. Scan size was 1μm x 1μm. As shown in this figure, the surface morphology became very rough after annealed at 800°C.

Figure 4.7 shows XRD patterns as a function of annealing temperature for the TiN films. In the case of without annealed sample, the diffraction peak intensity of TiN (111) can be seen as shown in Fig. 4.7. However, the peak intensity of TiN (111) decreased clearly after annealed at 600°C.

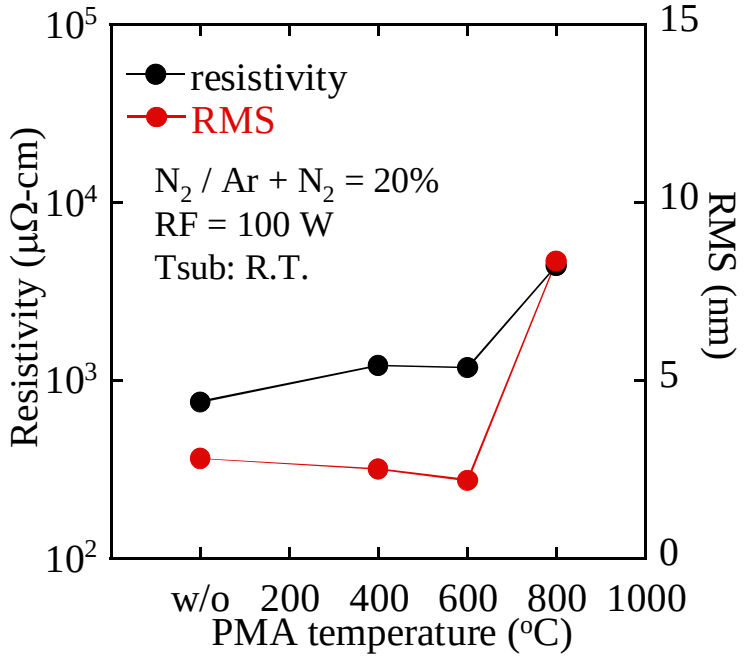


Fig. 4.5. Resistivity and RMS of TiN films as a function of the post metal annealing (PMA) temperature.

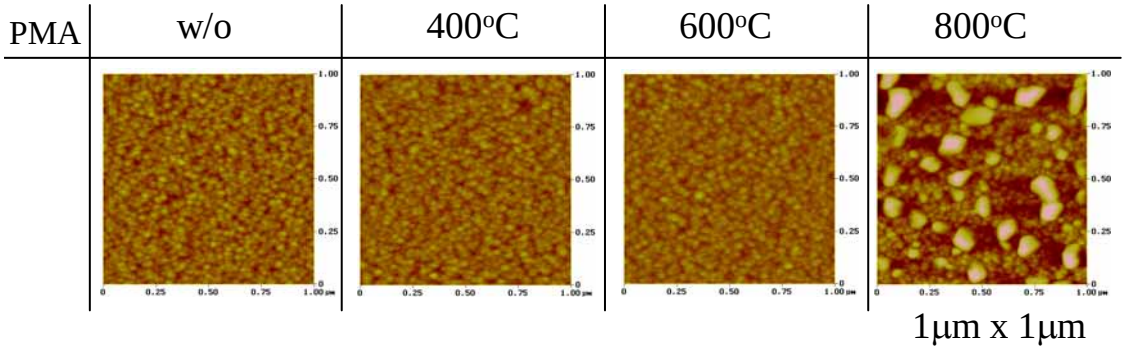


Fig. 4.6. AFM images of surface of TiN samples

Figure 4.8 shows Ti2p spectra of TiN films without PMA and with PMA at 800°C for 5 min. After annealed at 800°C, the peaks of Ti-N disappeared completely, and the binding energy shifted to a higher energy corresponding to that of Ti-O. Consequently, this observation indicates that the TiN film was oxidized after annealed at 800°C. From this the XPS data, the increase of resistivity of TiN which was annealed at 800°C can be explained like below. When the sample annealed at 800°C, the oxidation reaction in the bulk of the TiN films became active such that the formation of high-resistivity phases such as TiO_2. This reaction caused the increase of the resistivity of the sample which was annealed at 800°C.

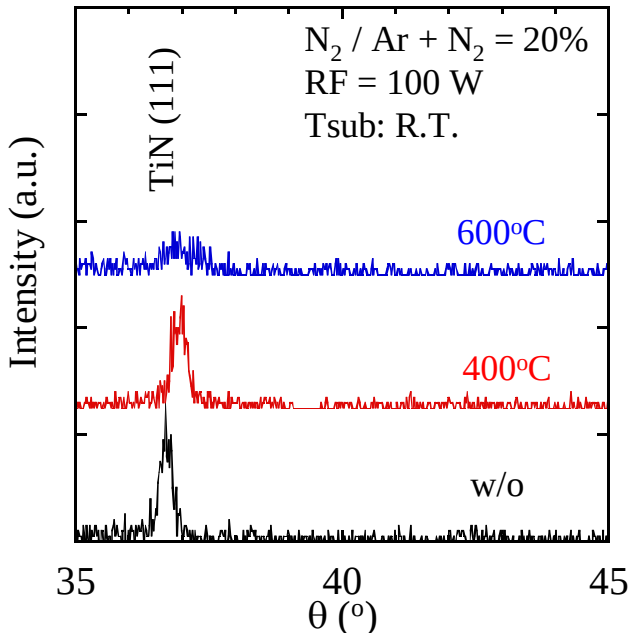


Fig. 4.7. XRD patterns as a function of annealing temperature.

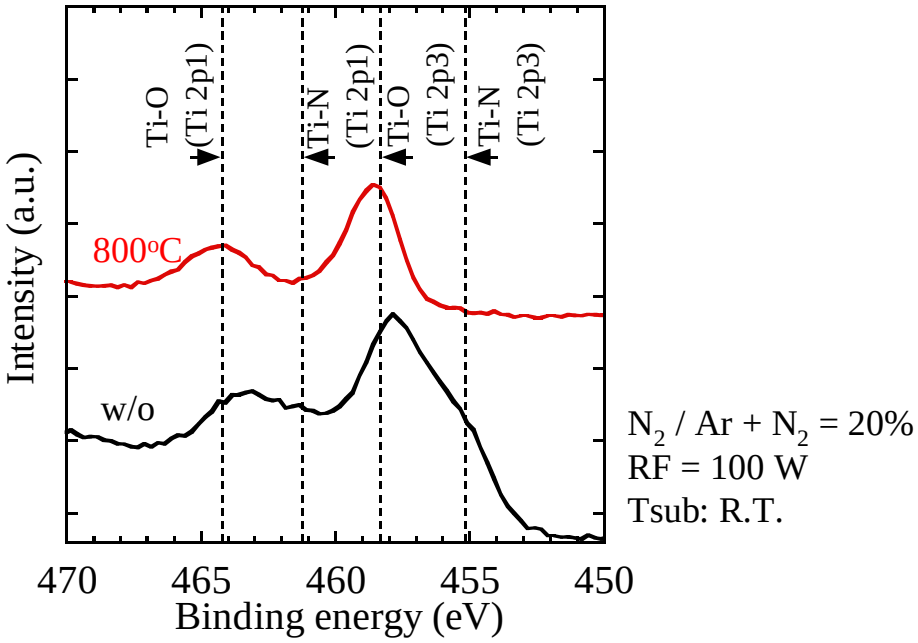


Fig. 4.8. Ti2p spectra of TiN films without PMA and with PMA at 800°C for 5 min.

4.4 Characterization of TiN/La_2O_3/n-Si(100) MIS Capacitors

Figure 4.9 shows the fabrication flow of the TiN/La_2O_3/n-Si(100) MIS capacitors. Figure 4.10 shows C-V characteristics of MIS capacitors. The temperature in the graph indicates PMA temperature. The deposition temperature of

La_2O_3 film is room temperature, and it was annealed in N_2 at 600°C. For the comparison, C-V curve of the Al electrode sample was shown in the same graph. As shown in Fig. 4.10, in the case of TiN electrode without PMA sample, charge-injection type hysteresis was observed. In addition, the capacitance value at 1 V of TiN without PMA sample decreased significantly than Al electrode sample. On the other hand, TiN gate sample with PMA at 400°C showed good c-v curve at accumulation and depletion region. However, at inversion region, the c-v curve inversion occurred. This suggests that so many surface states exist at the interface between TiN and La_2O_3.

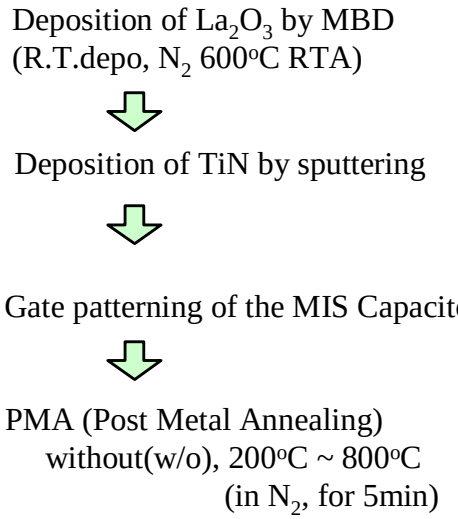


Fig. 4.9. Fabrication flow of the TiN/La_2O_3/n-Si(100) MIS capacitors.

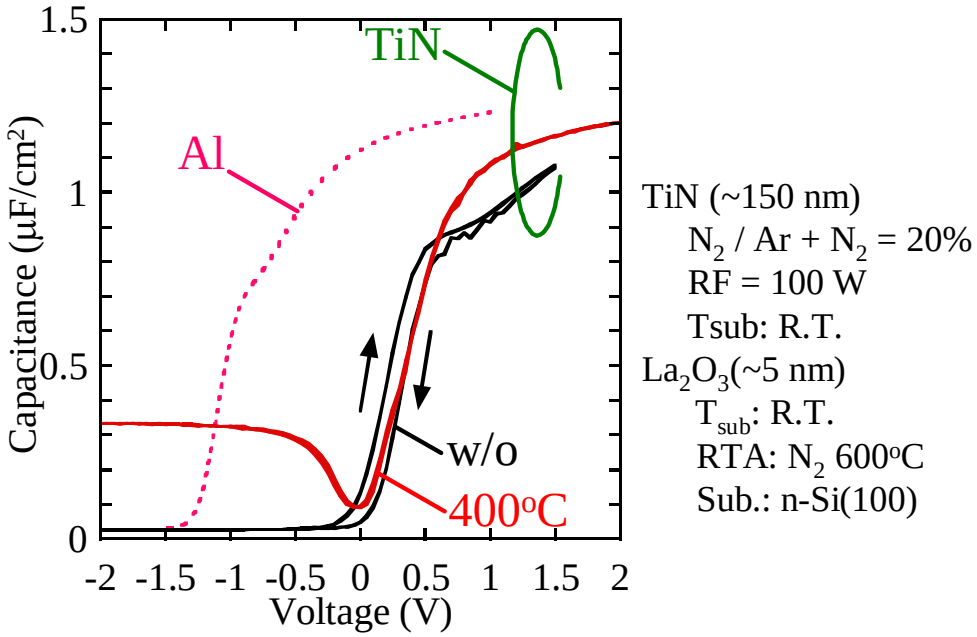


Fig. 4.10. C-V characteristics of TiN/La_2O_3 MIS capacitor.

To suppress the oxidation of TiN, PMA in vacuum was carried out. Figure 11 shows C-V characteristics for TiN/La_2O_3/n-Si MIS capacitor. The temperature in the graph indicates PMA temperature. TiN resistivity of 709 μΩ-cm was achieved even after 600°C PMA. In addition, as shown in Fig. 11, no hysteresis and good C-V curve was observed. It was confirmed that La_2O_3 film shows good electrical characteristics after 600°C PMA.

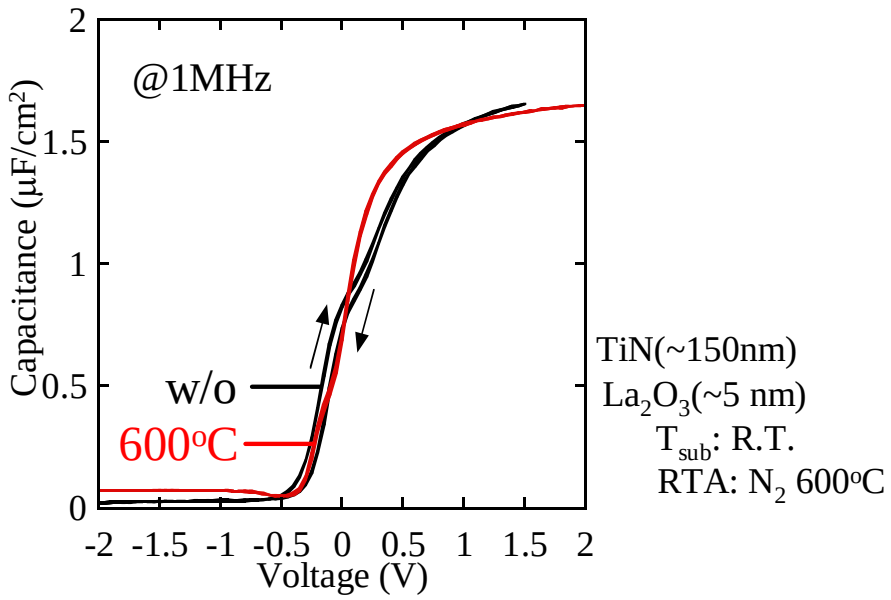


Fig. 4.11. C-V characteristics of TiN/La_2O_3 MIS capacitor for w/o PMA and 600°C PMA in vacuum samples.

4.5 Summary

For the preliminary step to the investigation of the stability of high-k thin films for the heat process, TiN films were investigated. TiN films were fabricated by RF magnetron sputtering method. TiN film which was deposited at the N_2 / Ar + N_2 flow of 20% with RF power of 100 W gave the resistivity of 756 Ω-cm. However, dramatic increase of resistivity and surface roughness occurred by annealing N_2 ambient at 800°C.

Additionally, charge-injection type hysteresis and degradation of accumulation capacitance was observed from the C-V characteristics of TiN/La_2O_3/n-Si(100) MIS capacitor. However, in the case of the sample which was annealed in vacuum condition, good C-V characteristic was observed even after 600°C PMA.

Chapter 5.

Conclusions

5.1 Conclusions Acquired From This Study

The research about the stability of rare earth metal oxides thin films for the conventional CMOS fabrication process was studied.

Firstly, the stability of high-k thin films for moisture ambient and wet processes was investigated. All high-k thin films were deposited by MBD method using sintered Metal-Oxides as targets. Not only rare earth oxides but also ZrO_2 was degraded in moisture ambient. It was also found that rare earth oxides thin films completely dissolved in ultra-pure water after 24 hours. Additionally, rare earth oxides showed weak stability against the resist processes. However, it was confirmed that the degradation was completely suppressed by gate electrode.

In conclusion, to suppress the degradation of the film property of the high-k thin films during the wet process, it is recommendable to cover the high-k films completely with gate electrode and sidewalls by in-situ dry process.

Secondly, for the preliminary step to the investigation of the stability of high-k thin films for the heat process, TiN films were investigated. TiN films were fabricated by RF magnetron sputtering method. TiN film which was deposited at the N_2 / Ar + N_2 flow of 20% with RF power of 100 W gave the resistivity of 756 Ω-cm. However, dramatic increase of resistivity and surface roughness occurred by anneling N_2 ambient at 800^{o}C. From the XPS measurement, it was confirmed that these degradations caused by the oxidation of TiN film during the annealing. Additionally, TiN/La_2O_3/n-Si MIS capacitor showed charge injection type hysteresis and degradation of accumulation capacitance. In the case of PMA in vacuum condition, TiN resistivity of 709 μΩ-cm was achieved. In this case, it was also confirmed that TiN/La_2O_3/n-Si MIS capacitor showed good electrical characteristics even after 600^{o}C PMA.

5.2 Future Issues

It is necessary to suppress the oxidation for the integration of the metal gate to advanced CMOS process. To suppress the oxidation during the heat process, investigation of double structure such as TiN covered with the good stability film against the oxidation, is needed.

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