Master thesis

A study on dependence of amorphous or crystalline rare earth gate oxides on Si surface orientation

(アモルファス及び結晶化した希土類ゲート酸化膜のSi基板面方位依存性に関する研究)

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Chapter 1

Introduction

In this chapter, research background is described, whose the basic concepts is that the LSI progress resulted from the MOSFET downsizing. Starting with the scaling method of MOSFET and the limits of gate SiO_2. The necessity of high-k dielectric ¯lm developments and the requirements for high-k materials are desctibed. Rare earth oxides, the promissing candidates for the next generation, are introduced and the reason why Yb_2O_3, Tm_2O_3 and Gd_2O_3 are chosen in this study is explained. The features of amorphous and crystalline high-k ¯lms, and then new reports about Si substrate orientation dependence are intrduced. The purpose and construction of this study are described.

1.1 Backgrounds

1.1.1 Scaling method of MOSFET and the role of SiO_2

Electronics is the most important invention in the 20th century and Si LSI is now one of the biggest industry in manufacturing. It is not an exaggeration to say that the technology of Si LSI and its fundamental devices, Metal-Oxide-Semiconductor Field-E®ect-Transistor(MOSFET) realize the present information society. It will de¯nitely last for least ¯fty years until new technology take over from Si LSI.

The technical improvement of LSI, such as large integration, multiple functions, high-speed processing and low-power consumption were realized by device downsizing according to scaling law. In fact, developments of microscopic devices fabrication process have supported "Moore's law", which published in 1965 and indicated that the number of transistor in the integration circuit will double in 18-24 months. In 100 years, the feature size reduced by one million times, overcoming many downsizing limits. It was predicted by Moore himself that "Moore's law" will probably last for least ten years from now.

Figure 1.1.1 shows the roadmap of (a) gate length and (b) equivalent SiO_2 thickness(EOT) from the speci¯cation in the International Technology Roadmap for Semiconductor(ITRS). Gate length of MOSFET means the distance which carriers must run by one switching. Acceleration of gate length shortening shown as ¯gure 1.1.1 (a) tells an unexpectedly rapid downsizing.

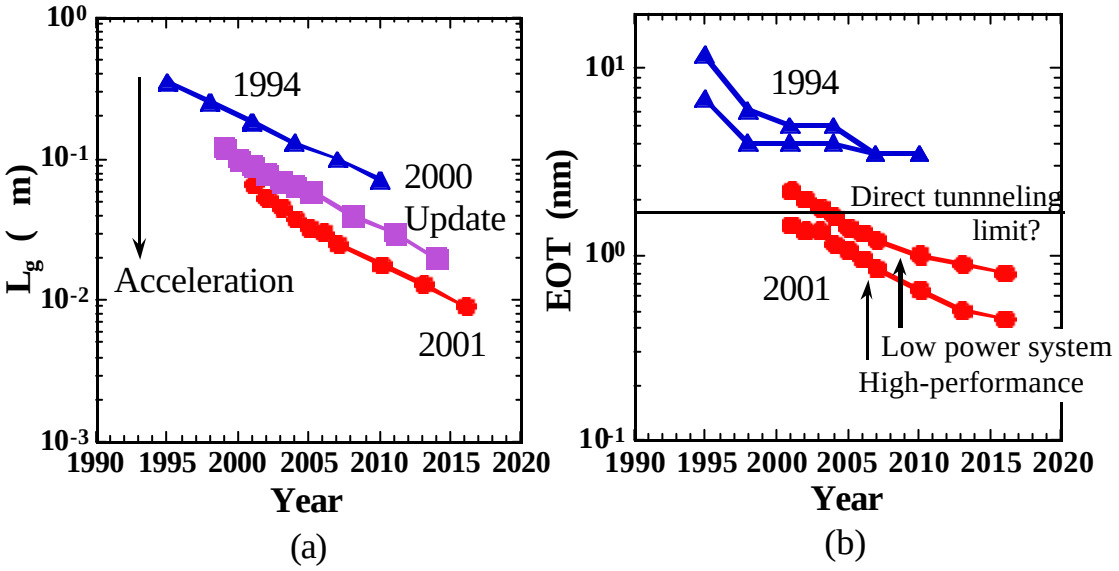

Figure 1.1.1: The requirements for (a) gate length and (b) EOT by ITRS(2001).

It can be easily imagined that some parameters in MOSFET cannot reduce according to scaling de¯nite ratio. Supply voltage is a typical example. It can be also easily noticed that rapid downsizing bring some harmful e®ects. High electrical ¯eld in channel or short length of gate length cause the short channel e®ect. It is the phenomenon that source/drain' ¯eld cannot be negligible in the channel and accordingly gate ¯eld weaken. Gate cannot induce inversion charge at on-state at last and un-control switching.

Gate dielectric SiO_2 has been thin alternatively to increase gate charges. The capacitance "C_i" of gate dielectric at unit area is expressed with the following equation,

$$C_i = \frac{\varepsilon_0 k}{d} \tag{1.1}$$

where ε_0 and k are vacuum and gate dielectrics dielectric constant, respectively and d is the thickness of gate dielectric. The reduction of "d" is the most e®ective way to increase capacitance. Figure 1.1.1 (b) shows that downsizing speed accelerated years by years, and EOT reach the direct tunneling limit in a few years.

SiO_2 is a key material to operate MOSFET because dielectric/Si interface is critical which carriers run through at. The reason why SiO_2 played a hystrical role in the invention of transistor and is a necessary material in fabrication process will be introduced before discussions of SiO_2 limits.

Although the idea of MOSFET has come ¯rst, it is the bipolar junction transistor to be used as commercial products. The ¯rst MOSFET using a thermally oxidized Si demostrated in 1960. One of the big problems to producing integrated circuits with MOSFETs was the stability of these transistors. To ¯nd and understand the concept of mobile charges in gate SiO_2 was important and the necessity of ultra-clean process was becoming to recognize.

Another key advantage of SiO_2 was the idea of SiO_2 masking. They learned how to form a glassy, protective SiO_2 layer on Si surface and use it as a selective mask against the di®usion of impurities. This techniques were developed into the planar manufacturing process that would soon revolutionize the semiconductor industry. SiO_2 was also used as passivation ¯lms naturally protected many contaminations.

MOSFETs were thus beginning to displace bipolar transistors in many integrated circuits with SiO_2. MOSFETs are the devices that cannot consume any power without being on-state. These "normally-o® type" transistor made it possible to build a large integrated circuit system.

The direct tunneling, the fatal problem that we face now about gate SiO_2 and the answer will be discussed in next subsection.

1.1.2 Requirements for high-k gate dielectrics and rare earth oxides of the candidates

Figure 1.1.2 shows the schematic band diagram explaining direct tunneling mechanism.

This is Ag/SiO_2/p-Si depletion condition, and SiO_2 thickness is so thin that leakage current run through SiO_2 even when $V_{ox} < ©_B$. This is called direct tunneling, and the leakage mechanism is called Fowler-Nordheim tunneling when $V_{ox} > ©_B$. The gate leakage current exponentially increase in tunnel current with decreasing dielectrics thickness.

The SiO_2 thickness limit of direct tunneling was originally thought about 3-4 nm, and Semiconductor Industry Association (SIA) con¯gured that the reduction of the gate SiO_2 thickness was stopped at 3 nm in 1997. However, it was found that performance of transistor cannot be improved with keeping SiO_2 thickness. And it was demonstrated that the transistor with 1.5 nm SiO_2 normally operated because leakage currents decrease in proportion to gate area with shortening gate length. The SiO_2 thickness limit is thought to decided by trade-o® between the reliability and leakage currents [1]. We have common knowledge that SiO_2 can last about 0.8 nm nowadays, however he physical explanation has not been done. (1.5 nm has been already passed from ITRS 2001!)

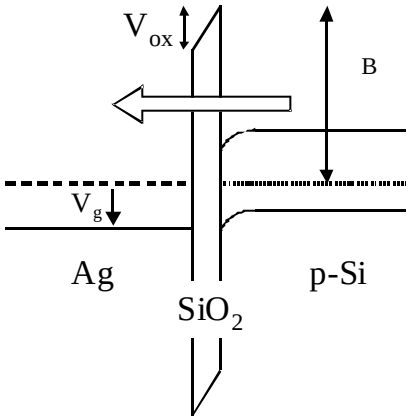

Figure 1.1.2: The schematic band diagram for thin SiO_2 MOS capacitor.

The answer of this problem is to introduce new materials, which have high dielectric constant. From the equation (1.1), gate dielectric thickness of d was decrease to increase capacitance of C_i, what is called scaling law. If gate dielectric constant of k is double, even if thickness of gate dielectric ¯lm is double, the equivalent capacitance value can be maintained. Thus, by using high dielectric constant materials for gate dielectric, physical thickness of ¯lm can be increased with still keeping the same capacitance value of SiO_2

gate dielectric and it is possible to reduce the gate leakage currents.

The materials, which have higher dielectric constant than SiO_2 of 3.9 are called "high-k dielectrics" and thus have attracted much attention. It is not easy, however to develop these materials because materials itself are contaminations.

High-k dielectrics must satisfy some requirements to replace SiO_2. First of all, materials must have higher dielectric constant, but it is inconvenient for materials have dielectric constant larger than 50. It has been reported that high-k gate dielectrics are promising for sub-100 nm MISFETs, and the phenomena related to high-k gate dielectrics such as fringing-induced barrier lowering (FIBL), zero-bias internal barrier lowering (ZIBL) and fringing-induced barrier shielding (FIBS) have been studied so far [2, 3, 4]. The larger phisycal thickness of high-k gate dielectrics introduce drain electric ¯eld to the channel and capacitive coupling occur. This is FIBL phenomena that compromise o®-state leakage. Even a low drain voltage can draw large o®-state currents in high-k devices suggesting that built-in voltages are involved. This e®ect is called ZIBL, so barrier lowering occurs in the channel due to the interfacial boundary conditions such as k of thickness of gate dielectrics. A source side high-k dielectrics lower saturation current through FIBS. The source coupling competes with gate to keep the channel potential near zero voltage and governs drain currents. From these reasons much larger k and thicker physical thickness are not necessary and a desirable alternative gate dielectric should have k between 10 to 50.

For high-k materials which have dielectric constant of k, their insulative performance is appreciated by the leakage current density at one capacitance equivalent thickness (CET). CET is given by

$$C_i = \frac{\epsilon_0 k}{d} = \frac{\epsilon_0 \epsilon_{SiO_2}}{CET} \tag{1.2}$$

where $\epsilon_{SiO_2} = 3{:}9$ is substituted. Note that we discriminate CET from EOT. EOT is de¯ned in this thesis that: the value calculated with quantum, leakage e®ect (measured frequency e®ect) or something necessary to use programs. NCSU CVC program is one of the popular programs used all over the world, which contained quantum e®ects. On the other hand, CET is simple and experimental value, which obtained from the accumulation capacitance in C-V characteristics To suppress the gate leakage consumption under 10 % of power consumption, it is necessary to gate leakage current density in MOSFET of 1 A/cm^2. For SiO_2 of 1.1 nm cause leakage of 10^3 A/cm^2 and for Si nitride of 10^2 A/cm^2.

Secondly, new dielectric materials should be thermodynamically stable in contact with Si surface at temperatures exceeding 1000 K. In LSI fabrication, there are some processes

with 1000 K, such as activation after doping. The formation of SiO_2 or MxSyOz(silicate) at high-k/Si interface must be prevented because These interfacial layer decrease the total dielectric constant drastically. According to latest reports, however, some interfacial layer are required to reduce interfacial state density, leakage currents or boron penetration(from poly-Si gate). The total dielectric constant and these value are serious trade-o® to design devices.

Moreover especially MxSy(silicide) formation and micro-crystal growth in the ¯lms must be prevented because these dramatically increase leakage currents.

Thirdly for most of the investigated high-k materials, the band gap is roughly inversely proportional to the dielectric constant. As the dielectric constant increase, the band gap decreases. Not only large band gap but large band o®sets to Si are necessary because this is barrier for leakage currents due to Schotky emission. Thus the conduction band o®sets become another critical factor in the selection of dielectric materials.

For gate dielectric application, at last, lower channel mobility compared with a MOSFET of SiO_2 is concerned. Mobility is thought to be degraded by the carrior scattering at high-k/Si interface. Fixed charge in high-k ¯lm induced Coulomb scattering, so that °atband voltage shift has to be suppressed. (ref. subsection (2.2.9) about the relation between ¯xed charge and °at band voltage shift.) By the same reason, higher density of interface states and the roughness of high-k/Si interface have to be suppressed. Using chemical oxide at the interface is one of the new idea to engineer the interface.

Table 1.1 shows major high-k dielectric properties reported recently.

Table 1.1: Candidates for high-k dielectrics and their physical properties.

Materials	SiO_2	Al_2O_3	ZrO_2	HfO_2	La_2O_3	Pr_2O_3
Dielectric constant	3.9	8.5-10	11-18.5	24	27	13
Band gap (eV)	9	6-8	5.2-7.8	5.7	5.4	3.9
Structure	Amo.	Amo.	Crystal T>600°C	Crystal T>700°C	Amo.	Crystal T>700°C
Contact stability with Si (kJ/mol) $Si + MO_x \rightarrow M + SiO_2$	Stable	+63.4	+42.3	+47.6	+98.5	
Lattice energy (kJ/mol)	13125	15916	11188		12452	12938

SiO_2 has biggest band gap and highest barrier for both electrons and holes. SiON and SiN are thought to be next dielectrics before starting high-k dielectric process. Nitrogen doping in SiO_2 improve the leakage currents properties. Al_2O_3, HfO_2 and ZrO_2 have

been seriously studied so far and thought the most promising, and most of the papers or presentations were reported about HfO_2 or ZrO_2 in the latest conferences.

Recently, excellent results of rare earth oxides thin ¯lms such as La_2O_3, CeO_2, Pr_2O_3 and Gd_2O_3 have been reported.

Figure 1.1.3 shows rare earth materials without Pm which has radioactive and physical properties of rare earth oxides. Their values are quite di®erent from each other and La, Gd and Lu have large band gap more than 5.3 eV as shown ¯gure 1.1.3 (a). And other oxide have enough value around 5.0 eV. Lattice energy means the strength between atoms and it is expected that the oxides having large lattice energy show good stability or easy crystallization.

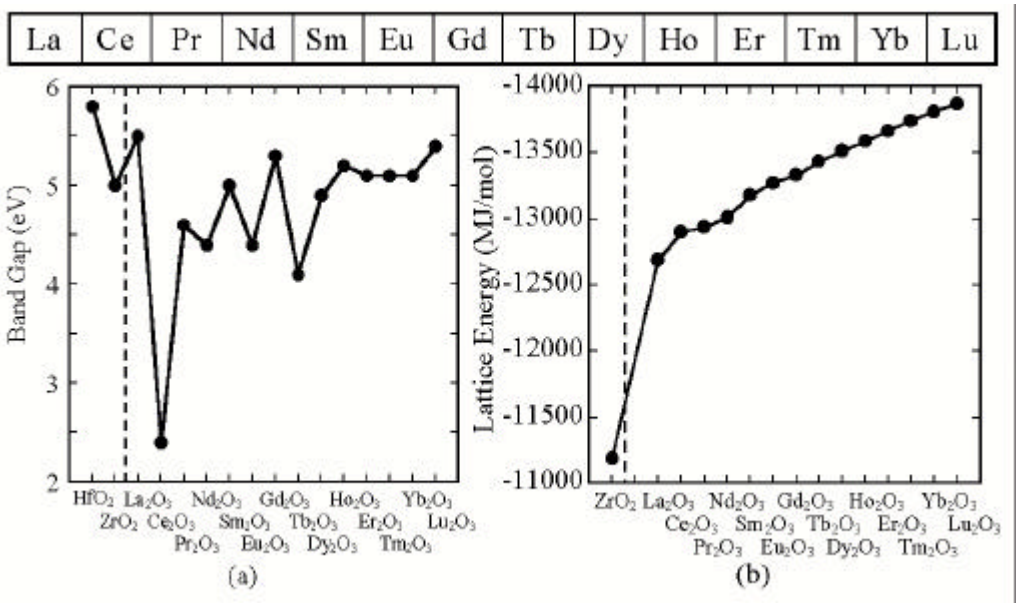

Figure 1.1.3: Properties of rare earth oxides. (a) band gap and (b) lattice energy.

The dielectric constants of all rare earth oxide were calculated [5] and they decreased with increasing atomic number. It should be noted that La_2O_3 has reported large dielectric constant of 27 [6] and they are regarded as prospective candidates for the post HfO_2 in ITRS2001,

In terms of the deposition methods or equipments, by the way, CVD is thought to be appropriate for production, but di±culty to develop the precursor and problem of contaminations such as H, C and Cl from precursor remain unresolved. Evaporation, sputtering and laser ablation are suitable for research of fundamental ¯lm properties. Molecular Beam Epitaxy(MBE) method is thought to have advantages to CVD and sputtring in terms of ¯lm impurity and Si substrate damage, respectively. It is necessary for high-k ¯lms to control the physical thickness layer by layer during the deposition. And

atmosphere, pressure and temperature in the chamber have to be controlled precisely, so in this study MBE method was used for deposition of rare earth oxide thin ¯lms.

1.1.3 Amorphous or crystalline ¯lms for rare earth oxides

The high-k gate insulator ¯lms should keep amorphous phase after high temperature LSI process as described in previous subsection. If high-k ¯lms cannot keep amorphous and poly-crystallized, it causes leakage current. Thus amorphous or single-crystal ¯lms are usually preferred and eptaxially grown ¯lms directly on Si have some advantages. They have a probability that higher dielectric constant than that of amorphous ¯lms is obtained because of the polarization. The crystalline ¯lms without any leakage path have excellent insulator properties, and epitaxial growth layer by layer is easy to contral ¯lm thickness by atomic level. However, there are three oxides in rare earth that reported epitaxial ¯lms for high-k gate dielectric application.

Epitaxial Pr_2O_3 was reported by H. J. Osten et al. and Pr_2O_3 cubic structure with dielectric constant of 31 on Si(100) [7]. This ¯lms had good leakage current density of $5 £ 10^{i10}$ A/cm^2 for EOT of 1.4 nm. This leakage currents were better than that of amorphou Pr_2O_3 on Si(100) reported in our laboratory [8]. It was also demonstrated that crystal structure depended on Si substrate orientation and Pr_2O_3 on Si(111) was hexagonal structure. Figure 1.1.4 shows crystal structure of rare earth oxides.

J. Kwo et al. have reported amorphous Gd_2O_3 properties, which had dielectric constant of 14 and epitaxial Gd_2O_3 ¯lms, whose leakage current density of 10^{i3} A/cm^2 for EOT of 1.4 nm [9]. Gd_2O_3 has small miss matching with Si as shown in table 1.2.

CeO_2, whose crystal structure is fruorite has also very small miss matching and S. Nishikawa et al. reported the amazing large dielectric constant of 52 using epitaxial CeO_2 directly deposited on Si(111) [10]. The reason why this ¯lm had twice higher dielectric constant than that ever reported of 26 was at the interface without any layer. This result indicated new e®ect on epitaxial ¯lms.

For other rare earth oxide, the study on not only amorphous but also srystalline ¯lmes will provide some new properties, and to obtain epitaxial growth is meaningful developent. In summary I chose Gd_2O_3, Tm_2O_3 and Yb_2O_3 for the study on amorphous properties. And I chose Gd_2O_3 and Tm_2O_3 to realize epitaxial growth and to study theie electrical properties. Tm_2O_3 and Yb_2O_3 seemed to have good stability and easy crystallization because of higher lattice energy in rare earth oxides. It is also necessary for Tm_2O_3 and Yb_2O_3 to investigate the fundamental electrical properties because there were few reports about thin Tm_2O_3 and Yb_2O_3 ¯lms for gate dielectric apprication.

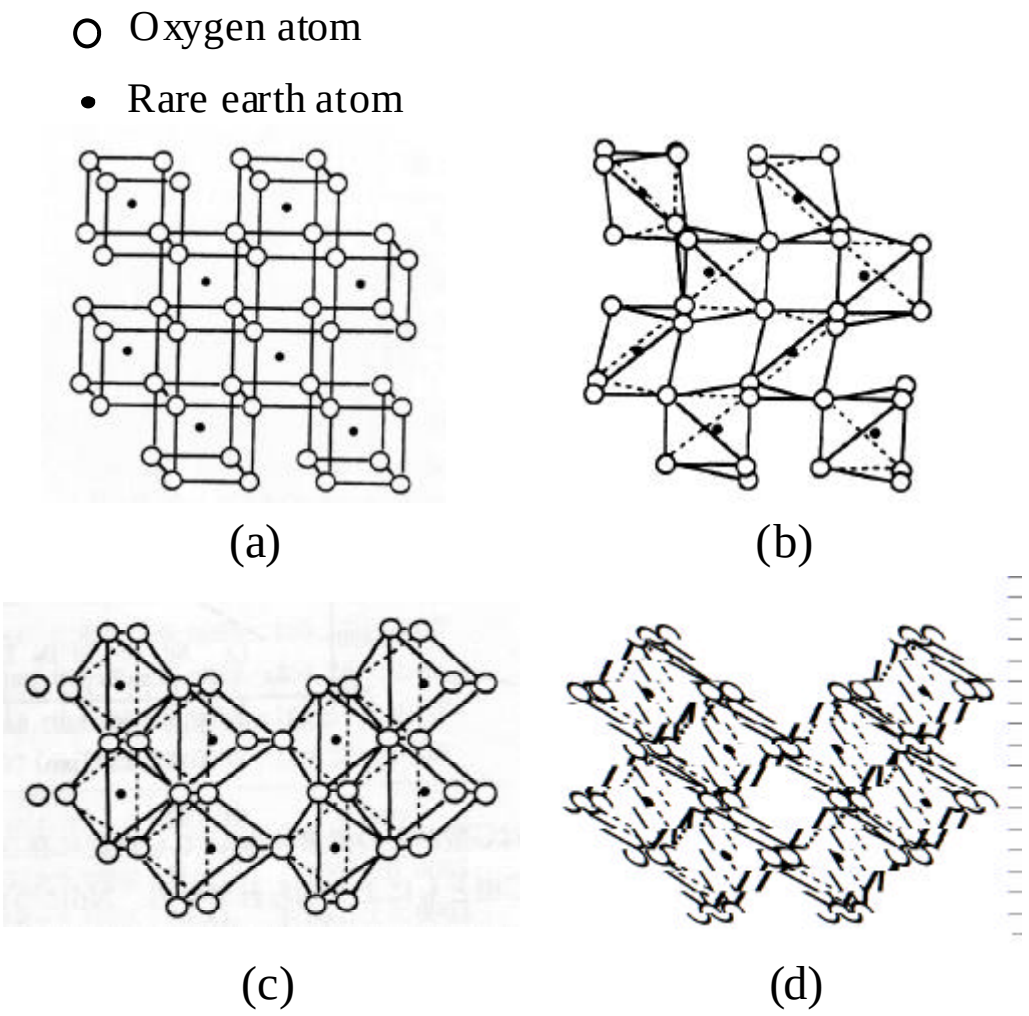

Figure 1.1.4: Schematic crystal structures of rare earth oxides. (a) °uorite, (b) cubic, (c) monoclinic and (d) hexagonal type.

Table 1.2: Physical properties of crystalline rare earth oxides

Rare earth element [Ln]	Crystal structure [oxide formula], lattice constant (nm, °) and (lattice miss matching with Si %)			
	Fluorite [LnO_2]	Cubic [Ln_2O_3]	Monoclinic [Ln_2O_3]	Hexagonal [Ln_2O_3]
La		1.136 (+4.6%)		0.39372 0.61295
Ce	0.5411 (-0.37%) on Si(111)	1.116		0.389 0.607
Pr	0.5393 (-0.67%)	1.1152 (+2.7%) on Si(100)		0.3857 0.6016 on Si(111)
Gd		1.0813 (-0.45%) on Si(100)	1.4061 0.3566 0.8760 100.1	
Tm		1.0488 (-3.4%)	1.381 0.3447 0.8505 100.2	
Yb			1.373 0.3425 0.8452 100.17	

1.1.4 Dependence of interfacial properties on Si surface orientation

For amorphous high-k ¯lms, high-k/Si interfacial properties are most critical issues and as gate dielectrics become thinner, electrical characteristics of the dielectrics are strongly a®ected by interfacial properties. To obtain excellent interfacial properties, we have been trying to optimize the Si surface treatment, high-k deposition and annealing conditions. Seen from another standpoint, it is well known that Si substrate orientation very sig-ni¯cantly a®ects the Si/SiO_2 interfacial properties. Currently, (100)-oriented Si wafer is employed in manufacturing lines. This is because lower interface charges and states for MOS interface can be obtained, and electron channel mobility of MOSFET fabricated on Si(100) is higher than that on Si(110) or (111).

Figure 1.1.5 shows the crystal models of Si at the surface of (100), (110) and (111). The available bonds per unit area on the Si surface are different, and the (111) surface has the largest number of available bonds and the (100) has the smallest. If we assume that the origin of interfacial trap is due to excess Si in SiO_2, then the smallest available bonds, the smaller the amount of the excess Si, thus the (100) surface should have the smallest interface state density.

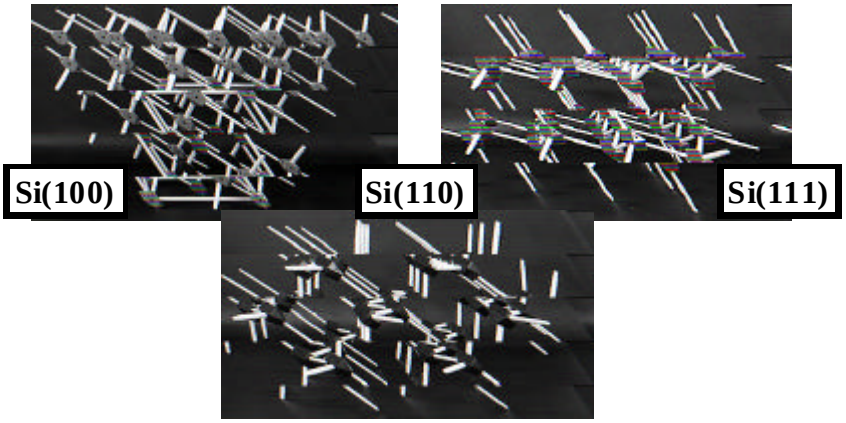

Figure 1.1.5: The crystal models for Si(100), (110) and (111) surface.

However, these results were confirmed on SiO_2 hundreds of nm thick, not on oxides less than a few nm thick. For amorphous high-k films, the dependence of electrical properties on Si substrate orientation has not been reported. Does the film whose materials were evaporated and fell on various substrate have Si orientation dependence?

Recently some papers indicated the new results about Si surface orientation dependence. It was reported that an atomically flat Si surface can be easily obtained on a (111) surface compared to a (100) [11].

Another paper demonstrated that the oxidation rate for (111) substrate is larger than that for (100) substrate in relatively thick oxide region, while that for (111) is slightly lower than that for (100) in less than 2.0 nm oxide thickness regions [12]. It also showed that the reliability of the oxides on (100) and (111) are almost the same.

Various new structures, such as vertical and concave MOSFETs, are investigated with the expected limitation in the conventional CMOS downsizing. These 2 or 3-dimentional types of MOSFETs have a special feature that the channel of the MOSFETs consists of various surface with different crystal orientation. The information about Si orientation dependence provide possibility for these new device structure developments.

In terms of the channel mobility, it was suggested that there is a possibility to increase current drive capability of MOSFET by changing the Si surface orientation [13]. Detailed

measurements of the e®ective mobility(^1_e) on many surface orientations for both n- and p-type Si have shown $^1_e(100) > {}^1_e(111) > {}^1_e(110)$ for conduction of electrons in inversion layers, and $^1_h(110) > {}^1_h(111) > {}^1_h(100)$ for conduction of holes in inversion layers. This dependence of the e®ective mobility on orientation has been correlated with the anisotropy of the conductivity e®ective mass in Si. Si(100) is now used in fabrication lines, however, the gate width for n-type has to be larger than that for p-type because of the mobility di®erence. To increase n-type MOSFET it is available to change the Si substrate orientation and the direction of the current °ow from source to drain [14]. For example, drain currents on Si(110) at the gate-length direction of one certain have maximum value because this direction from the source to drain of transistor in which Si-Si bond surface is parallel to the Si/SiO_2 interface.

For crystalline ¯lms on the other hand, the dependence of interfacial properties on Si substrate orientation is more complicated problem than that for amorphous ¯lms, because the crystal structure are di®erent by Si surface orientation. Thus it is hard to decide which e®ects are critical for electrical properties, the ¯lm of crystalline or the interface on various oriented Si surface.

1.2 Purpose of this study

The research of this thesis focuses on the Si substrate orientation, whose a®ect the oxide ¯lm/Si interface properties. Yb_2O_3, Tm_2O_3 and Gd_2O_3 are chosen for the research materials. The purpose of this study is to investigate these thin ¯lm properties on Si(100) at ¯rst such as dielectric constant and leakage currents. Then dependence of amorphous thin ¯lm properties on Si orientation is demonstrated. The e®ect on chemically oxidized Si substrate is also introduced. The high temperature deposition is demonstrated to obtain epitaxial high-k ¯lms on various oriented Si. The crystalline structure on each oriented Si is cleared and electrical properties of amorphous and crystal ¯lms are compared. At last the questions are answered:
Which is the best Si substrate orientation for amorphous or crystalline ¯lm?
Which has the better electrical properties, amorphous or crystalline ¯lm?

1.3 Construction of this thesis

Through this chapter, backgrounds and purpose of this study have been introduced and reviewed. In this section, construction of this thesis will be explained. The fabrication and characterization methods of rare earth oxide ¯lms are described in chapter 2. In

chapter 3, Yb_2O_3, Tm_2O_3 and Gd_2O_3 properties for high-k gate dielectrics application are discussed. Major problems of high-k dielectrics are discussed using electrical characteristics of Yb_2O_3. The e®ect on chemical oxide are also introduced. The dependence of amorphous Tm_2O_3 or Gd_2O_3 properties on Si substrate orientation is explained in chapter 4. In chapter 5, Tm_2O_3 or Gd_2O_3 properties deposited at higher temperature to realize epitaxial growth on Si are explained. The dependence of crystal structure and electrical properties on Si substrate orientation are also discussed. In chapter 6, I would like to summarize of this thesis.

Chapter 2

Fabrication and characterization methods in this thesis

In this chapter, the fabrication and characterization methods of rare earth oxide ¯lms are described. Cleaning and treatments of Si substrate, MBE method and RTA conditions used in this study are explained. A lot of characterization methods were used to study not only the electrical but also the physical properties. XRD, RHEED, RBS were used for evaluation of crystal properties. SIMS was the strong measurement to investigate the atomic pro¯ling in the ¯lm and XPS was used for the same purpose. Ellipsometry for measuring the physical ¯lm thickness, cross-sectional TEM image for check the ¯lm and interface observation and AFM for survey the surface morphology were done. Characterizations of electrical properties were most important instruments and purpose in this study. These characterization methods and their principles are expained.

2.1 Rare earth MIS capacitor's fabrication methods

2.1.1 Cleaning and treatments of Si substrate

Si substrate cleaning is one of the most important process because some contaminations or particles are critical for nano-size rule devices. Especially hetero epitaxial growth requires very clean Si surface. The cleaning process used in this study is shown in Table 2.1.

The cleaning process now typically used is based on the RCA cleaning method proposed in 1970. This is the wet cleaning method mainly using H_2O_2 and some chemical liquid. SPM cleaning removes organic material and metal contaminations. Mixing H_2SO_4(96 %) and H_2O_2(30 %) generate heat (120-150^oC) and this also help organic material oxidation. HF dip removes natural or chemical oxides and also terminated the Si surface bonds with hydrogen(H). We use 1 % HF and call this Si substrate condition "HF-last" substrate. We use room temperature ultra-pure water of for the last rinse. H terminated Si surface is hydrophobic and hard to oxidized because Si-H protect oxygen absorption.

Ultra-pure water system we used in this study is composed of the primary pure water fabrication system and the ultra-pure water fabrication system. There are particles whose diameter are larger than 0.1 ^{1}m under 1piece/ml, dissolved oxygen under 2 parts per billion(ppb) and total organic carbon(TOC) under 1 ppb in the ¯nal ultra-pure water. Its resistivity is usually higher than 18.2 M- cm.

Si chemical treatment is important for rare earth oxide ¯lm/Si interfacial properties. Chemical oxidation of Si substrate has two meanings. First, We tried to make a bu®er layer on Si to compare with HF-last Si substrate. Secondly, we use chemical oxide as a passivation layer before thermal °ash. After HF dip, Si substrate is oxidized in room temperature H_2O_2 for 30 minutes to make 0.5 nm SiO_2. We call this condition chemical oxidized Si substrate and its surface is hydrophilic.

These Si are quickly loaded into MBE chamber. To obtain epitaxial growth, passivation chemical oxide is removed by thermal °ash at 900^oC in high vacuum 10^{-8} Torr. Chemical oxide become SiO around 1000^oC and come o®. In-situ RHEED observation was used to check SiO_2 removal and Si surface reconstruction.

2.1.2 Molecular Beam Epitaxy (MBE) method

In this study, MBE equipment was used for deposition of rare earth oxides on Si substrates. The ¯lm deposition method is identi¯ed two types. One is physical vapor deposition such as vacuum evaporation (PVD), sputtering and laser ablation. The other

Table 2.1: Si substrate cleaning process in this study.

1. Ultra pure water rinse	10 min.	
2. SPM cleaning	5 min.	
(H_2SO_4 : H_2O_2 = 4 : 1)		
3. Ultra pure water rinse	10 min.	
4. HF dip	5 min.	
(HF : H_2O =1 : 100)		
5. Ultra pure water rinse	10 sec.	HF-last
6. Chemical oxidation	30 min.	
(at room temp. in H_2O_2)		
7. Ultra pure water rinse	10 sec.	C.oxide
8. Thermal °ash 850° C	5-30 min.	T. °ash

is chemical vapor deposition (CVD) using chemical reaction. MBE is one of the PVD method. Molecular beam means the uniform molecule °ow heading one direction. MBE has some following advantages and disadvantages.

1. Low back pressures of 10^{-10} Torr and low contamination
2. controllability of ¯lm thickness
3. ability of epitaxial growth
4. inadequacy of in-plane uniformity for large size wafer and not for production

Figure 2.1.1 shows schematic drawing of MBE equipment used in this study. Rare earth oxide target is evaporated by using electron beam in ultra high vacuum. There were two vacuum chambers. One is loading chamber which is opened for each deposition and the other is growth chamber. The background pressure in growth chamber is about 10^{-10} Torr and the pressure during deposition is 10^{-8} Torr. There are four pumps, which are turbo-molecular pump(TMP in Figure 2.1) and rotary pump(RP) in loading chamber, and titanium sublimation pump(TSP) and ion pump(IP) in growth chamber. There are also four E-guns and targets, and two power supplies that are capable to evaporate two materials in the same time. (we used one E-gun accelerated by -5 kV in this study.) The purity of Yb_2O_3, Gd_2O_3 and Tm_2O_3 targets were 99.99, 99.99 and 99.9 % respectively. The 4 or 3 centimeters square substrate is rotated to improve uniformity of ¯lm thickness. The ¯lm thickness during deposition was monitored with the In¯con crystal oscillator sensor. We could use in-situ RHEED system for crystallinity analysis

at the surface, and quadrupole gas analyzer for the analysis of the gas in the growth chamber. This measurement is based on the mass spectrometry and usually there are some peaks observed at 2, 18, 28 and 44 of molecule mass. These peaks were thought to indicate H_2, H_2O, N_2 and CO_2. And the intensity ratio was about 50:1:3:1. During the heating Si substrate, the intensity of H_2O was a little bit higher than that of CO_2 and during deposition, this magnitude relation were reversed.

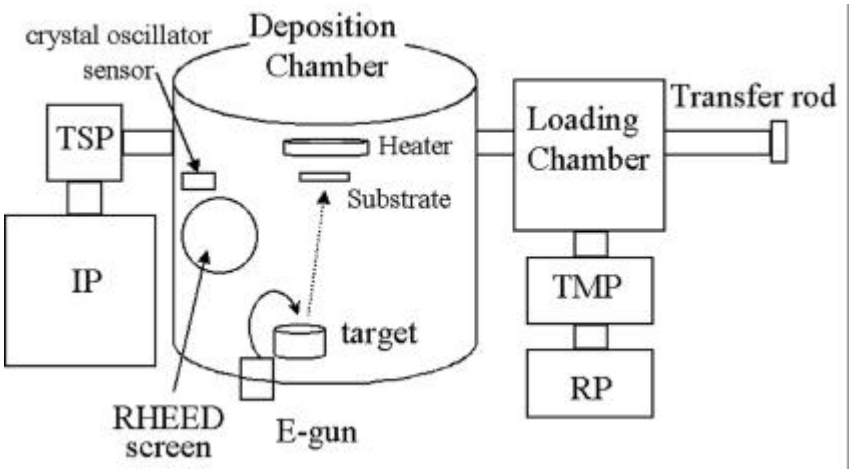

Figure 2.1.1: The schematic drawing of MBE equipment.

2.1.3 Rapid Thermal Annealing (RTA) method

To obtain high quality ¯lms, annealing after deposition is necessary. The annealing e®ects are thought of the lowering oxygen defect in the ¯lm and surface roughness. These come along the improvements of °at band voltage shift and hysteresis in C-V curve, and leakage currents in J-V curve.

The equipment used for annealing was MILA-3000(ULVAC Co. Ltd.) and Table 2.2 shows set up condition. The samples were heated by four infrared lamps surrounding the sample stage which were made of carbon and coated by SiC. The heat temperature was controlled by thermo couple feedback. Annealing was carried out in respective O_2 or N_2 ambient with °ow rate of 1.2 l/min. The remaining air of the furnace was replaced by the gas °ow for 5-10 minutes not be vacuumed, so there was a little O_2 in N_2 ambient. There is also time lag for annealing holding time of about ten seconds.

Table 2.2: RTA set up conditions in this study.

Annealing temp.	Step2 Warm-up time	Step3 Holding time	Step4 Cool down
200°C	30 sec.	5 min. or 2 min.	ambient
300°C	45 sec.	5 min. or 2 min.	ambient
400°C	1 min.	5 min. or 2 min.	ambient
600°C	1.5 min.	5 min. or 2 min.	ambient
800°C	2 min.	5 min. or 2 min.	ambient

2.1.4 Vacuum evaporation of top and bottom metal

Al was used for n-type Si MIS capacitor's top and bottom electrodes, and Ag was for p-type Si. Figure 2.1.2 shows band diagram for (a) Al/insulator/n-Si and (b) Ag/insulator/p-Si before junction. From Al' work function of 4.1 eV and Ag of 5.1 eV, °at band voltage shifts of $©_m$ ¡ $Â_s$ are calculated about -0.2 V and 0.2 V respectively. To minimize the °at band voltage shifts di®erent metals were used for top electrode.

Figure 2.1.3 also shows band diagram for (a) n-Si/Al and (b) p-Si/Ag as back contact. If di®erence between $©_m$ and $©_s$ is positive value, $©_m$ ¡ $Â_s$ is barrier height and this is shottoky contact. If $©_m$ ¡ $Â_s$ is minus value, this is ohmic contact. For n-Si Al makes ohmic contact and for p-Si, Ag does as shown in Figure 2.1.3. Table 2.3 shows the properties of Si wafers used in this study.

Al(99.9%) and Ag(99.99%) source was heated on Tungsten ¯lament and evaporated in vacuum bell jar with the pressure of 10^{i6} Torr.

Table 2.3: Properties of Si wafers in this study.

Substrate No.	Resistivity (- cm)	Doping N_{ss} (cm^{-3})	Diameter (inch)	type and orientation
1	8-20	4.25×10^{14}	6"	n-Si(100)
2	13-15	3.4×10^{14}	5"	n-Si(100)
3	0.8-1.2	5.5×10^{15}	4"	n-Si(100)
4	2-8	4.4×10^{15}	4"	p-Si(100)
5	3-5	3.55×10^{15}	4"	p-Si(110)
6	10-20	1.03×10^{15}	4"	p-Si(111)
7	0.012-0.02	5.0×10^{18}	2"	p-Si(100)
8	0.01-0.05	9.5×10^{17}	4"	p-Si(110)
9	0.02-0.06	1.3×10^{18}	2"	p-Si(111)

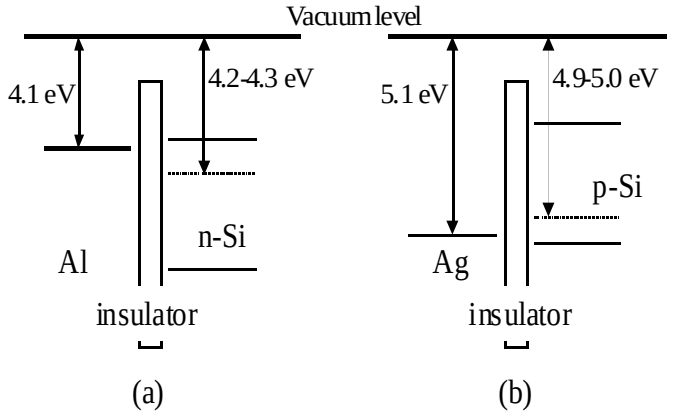

Figure 2.1.2: The band diagram for (a) Al/insulator/n-Si and (b) Ag/insulator/p-Si before junction

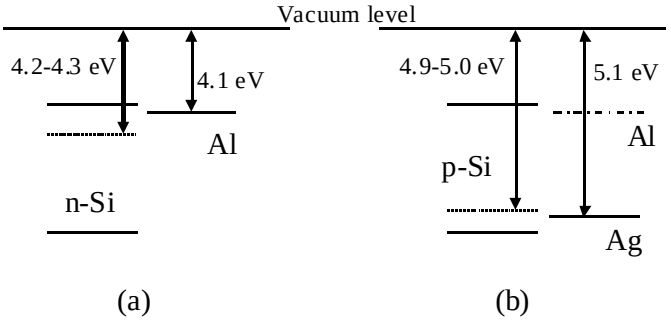

Figure 2.1.3: The band diagram for (a) n-Si/Al and (b) p-Si/Ag before junction

2.2 Characterization methods in this thesis

2.2.1 X-ray di®raction (XRD) method

XRD is very well-known and widely used method to analysis the ¯lm crystallization.

Figure 2.2.1 (a) shows two dimensions model of di®raction in crystalline. X-ray beam whose wavelength is ¸ enter into ¯lms at the angle of µ, and re°ect at each crystal aspect, where d is the distance of lattice planes. The pathway di®erence between an aspect and next one is 2d sinµ. When this length is equal to integral multiple of wavelength, in other words the relationship

$$2d\sin\mu = n\lambda \tag{2.1}$$

is satis¯ed, re°ection intensify and peak appears. This equation is called Bragg's formula.

The schematic drawing of XRD equipment using in this study is shown in Figure 2.2.1 (b). There are three slits, which are named divergence, receiving and scattering slit. Slit width is 0.5, 0.6 and 0.5 mm respectivily. X-ray's source is Cu(wavelength were $K_{®1}$: 0.15443 nm, $K_{®2}$: 0.15405 nm, $K_{¯}$: 0.13922 nm). Generator voltage of 40 kV and tube current of 30 mA was used normally. To identify the peaks, the database can be available which is editted and published by Joint Committee on Powder Di®raction Standards (JCPDS) in International Center for Di®raction Data (ICDD). These are called JCPDS-ICDD data cards.

2µ ¡ µ scan is used to decide the crystal structure and its orientation. For example, Si cubic single crystalline shows 4 peaks from 10-70 degree of (111), (220), (311) and (400) at 28.5, 47.3, 56.2 and 69.1 degree because of the extinction rule with crystal structure factor. One method to estimate its crystallinity, measuring FWHM (Full Width at Half Maximum) of each peak were done. It is called rocking curve measurements. After 2µ ¡ µ scan, 2µ value was ¯xed at the purposed peak and µ scan was carried out. FWHM is calculated from this µ curve and excellent crystalline shows intensity curve like delta function.

The pattern of MBE source pellet were measured by powder XRD method, which is major measurements using XRD equipment. Figure 2.2.2 (a) shows Gd_2O_3 source µ ¡ 2µ pattern. These peaks indicate Gd_2O_3 monoclinic crystalline and all peaks agree the card No. 42-1465. Figure 2.2.2 (b) shows Tm_2O_3 source µ ¡ 2µ pattern. These peaks indicate Tm_2O_3 cubic crystalline and all peaks agree the card No. 41-1090.

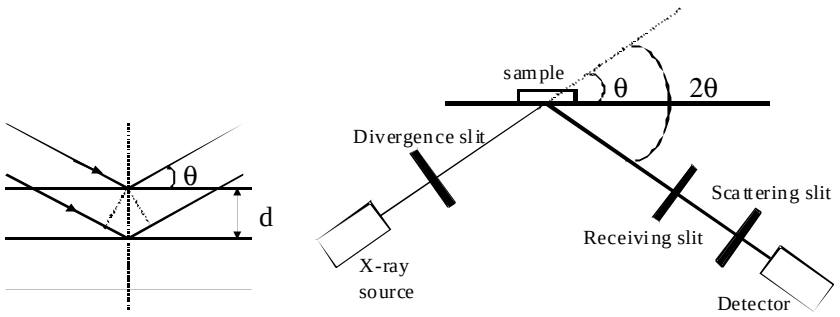

Figure 2.2.1: The schematic drawing of (a) lattice plane and X-ray re°ection and (b) XRD measurement system.

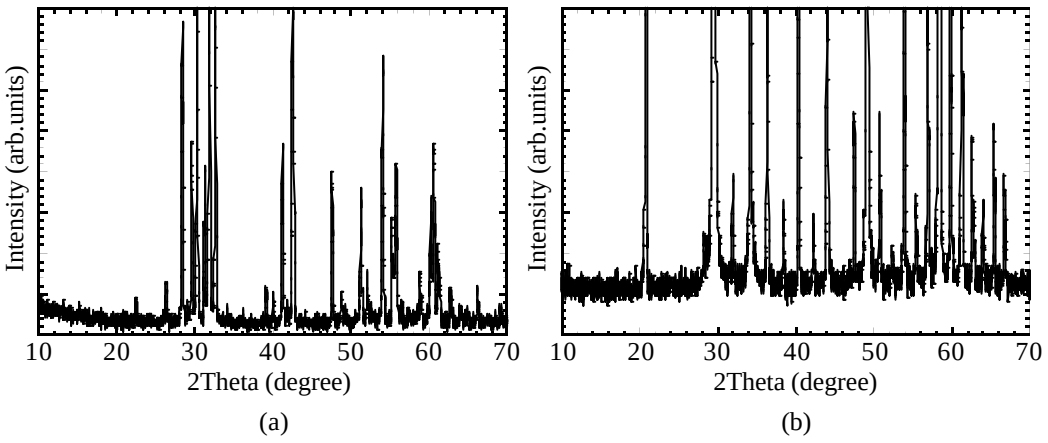

Figure 2.2.2: XRD patterns for MBE source pellet. (a) Gd_2O_3 (b) Tm_2O_3.

2.2.2 Re°ection High Energy Electron di®raction (RHEED) method

RHEED is e®ective in-situ method to obtain the condition of growing ¯lm and Si substrate surface. Figure 2.2.3 shows the components of RHEED diagrammatically. Electron beam is accelerated to 10-15 keV to sample surface at low angle of 1-3 degree. Structures of crystal surface are evaluated by the pattern, which was made by di®racted e-beam on the screen. We con¯rmed Si surface reconstruction and crystalline rare earth oxide ¯lms. When Si(100) substrate is heated at 900^{o}C and chemical oxide is removed thermally, RHEED pattern shows 2×1. For Si(111), 7×7 is obtained. Surface reconstruction occurs to reduce the number of dangling bonds and surface energy. "7×7" means $7 \times 7 = 49$ atoms compose one unit sell.

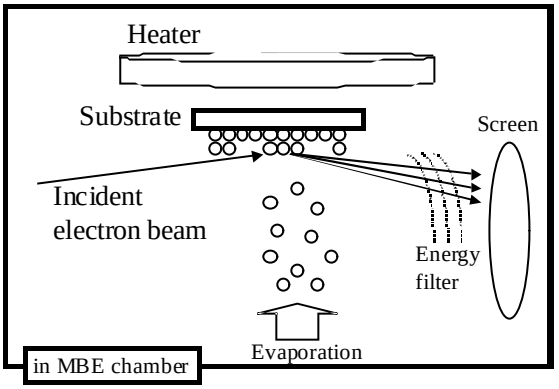

Figure 2.2.3: The schematic drawing of RHEED system.

2.2.3 Rutherford Backscattering Spectroscopy (RBS) method

RBS is based on bombarding a sample with energetic ions, typically He ions of 1 to 3 MeV, and measuring the energy of the backscattered ions. It allows determination of the masses of the elements in a sample, their depth distribution over distances from 10 nm to a few ¹m from the surface, and the crystal structure in a non-destructive manner.

Figure 2.2.4 (a) shows RBS schematic. A small fraction around $10^{i 6}$ of the number of incident ions undergoes elastic collisions and is backscattered from the samples at various angles. Calculation using the mass and energy of projectile, the energy of backscattered ion and the incidence angle can be determined the mass of target atom.

Figure 2.2.4 (b) shows typical RBS spectrum, and y-axis indicates simply counts as a function of backscatterd ion energy. The channel from 100 to 109 and the channel from 210 to 219 were de¯ned this time as the bulk Si and the Si surface respectively. The ratio

of the all counts of Y(M) from the metal sample and average counts of $H_{Si}(S)$ from Si surface contains two imformation, the incident ion and metal intensity. The metal oxide physical thickness is obtained by the product of $Y(M)/H_{Si}(S)$ and one constant. This constant includes some parameter, that is the metal capture cross section, the metal oxide density and its molecular weight, and it's 0.652 for Gd_2O_3 and 0.514 for Tm_2O_3.

The fundamental principle to evaluate whether the sample crystallized or not will be explained below. When the primary ions enter the crystalline ¯lm in parallel with the atom direction, the backscattered probability decrease extensively. In other words, intensity of the metal yiald decrease at the certain angle in conjunction with the Si because of the epitaxy growth. This is called channeling spectrum and the ratio (%) of channeling Y(M) and not channeling, i.e. ramdom Y(M) is the index which means the epitaxial growth quality.

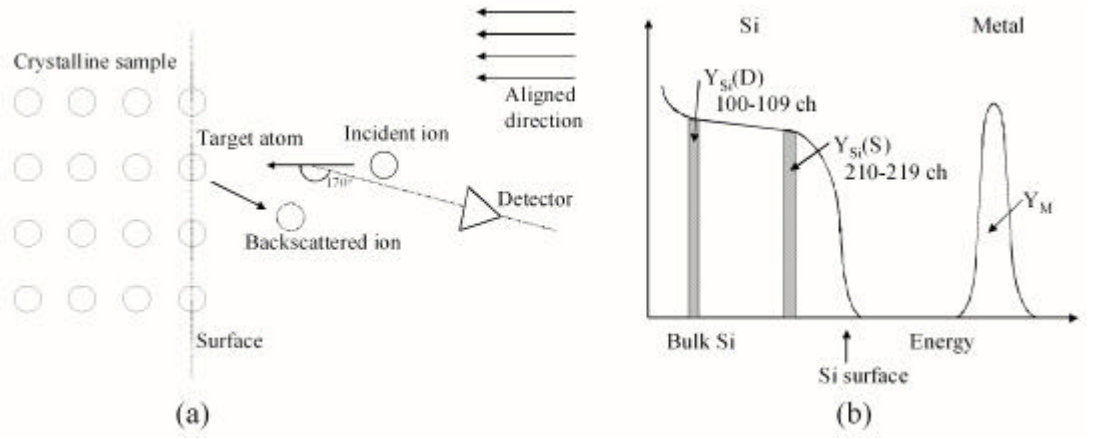

Figure 2.2.4: The schematic drawing of (a) RBS measurements and typical spectrum of Metal oxide/Si.

2.2.4 Secondary Ion Mass Spectroscopy (SIMS) method

SIMS is an analysis that can be used to characterize the surface and near surface (about 30 ¹m) region of solid samples. The technique uses a beam of energetic (0.5-20 keV) primary ions to sputter the sample surface, producing ionized secondary particles that are detected using a mass spectrometer. Figure 2.2.5 illustrates the SIMS method. The primary beam can be O_2^+, O^i, Cs^+, Ar^+, etc. and O_2^+ is typically used for the detection of electropositive species. Figure shows schematic illustration of sample surface and particles sputtered by primary ions. Many species are formed by the interaction of the beam with the samples, but the positive and negative secondary ions are meaningful imformation for SIMS. These species are called "secondary ions" and extracted by electric

¯elds and then energy and mass analyzed. Detection is by electron multiplier, Faraday cup, or ion sensitive image ampli¯er fo imaging.

SIMS can give three types of results. For a low sputtering rate, a complete mass spectrum can be recorded for surface analysis while the mass spectrometer scans the mass range. It consists of the secondary ion intensities of the species detected as a function of mass. The intensity of one or more masses for one particular mass can be obtained as a function of time with sputtering at a higher sputter rate. Such a plot must be converted to concentration versus depth. This use of SIMS for depth pro¯ling has become a primary mode of use. SIMS can also be used in a mode of data collection that is analogous to SEM. Element-speci¯c images or maps can be generated to monitor the secondary ions emitted from the samples with a mass spectrometer.

The size of crater that formed by sputtering is about 250 ¹m and the width of slit that secondary ions are detected thorough is 10 ¹m. In this study, only the depth pro¯les and the concentration of Si are used.

Figure 2.2.5 also shows schematically the sample consisted of the thin ¯lm A and substrate B, and the ideal depth pro¯ling. If the sample has rough surface , the incline of atom A and B pro¯ling are gradual and the width indicated by arrow in the pro¯le becomes large. This is also observed for the sample, which has rough interface. Note that correct pro¯ling can not be obtained for these samples.

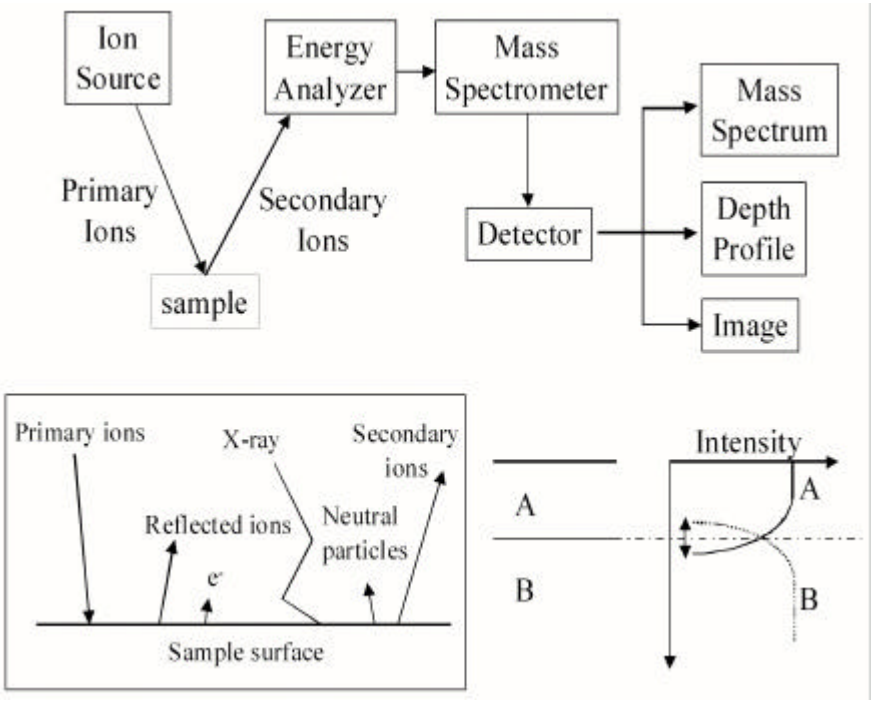

Figure 2.2.5: The schematic drawing of SIMS system, secondary elements and an example of depth pro¯ling by SIMS.

2.2.5 Ellipsometry method

Ellipsometry is the measurement method of ¯lm thickness using the di®erence of polarization before and after re°ection. The incident light which pass through the polarizer have two polarization parts of E_p and E_s as shown in Figure 2.2.6. These two parts have same intensity and phase, but the re°ection have the di®erent intensity and phase from each part. This amplitude ratio α and phase di®erence ϕ are called ellipso-parameters. If the sample is composed Air/thin ¯lm/substrate, α and ϕ are functions of ¯lm's complex refractive index, ¯lm's thickness, incident angle and measurement wavelength. Hence ¯lm thickness can be decided by wavelength dependence of α and ϕ. Wavelength of λ 200-800 nm (FE-5000,Otsuka Electronics Co.,Ltd.)

For transparent thin ¯lm its complex refractive index N_i is given by

$$N_i = n_i - jk_i \tag{2.2}$$

where n_i and k_i are refractive index and transmission factor, respectively, and $k_i = 0$. This refractive index of n_i approximates the following equation named "n_Cauchy dispersion" :

$$n_i = \frac{C_3}{\lambda^4} + \frac{C_2}{\lambda^2} + C_1 \tag{2.3}$$

where C_1, C_2 and C_3 are the parameters of n_Caushy. These value and ¯lm's thickness of d are decided with the least squares method ¯tting to experimental polarization spectrum. C_1 is easy to translate into dielectric constant of k using

$$k = C_1^2: \tag{2.4}$$

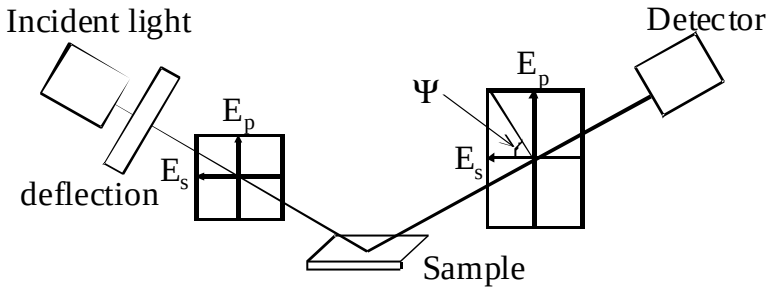

Figure 2.2.6: The schematic drawing of Ellipsometry system.

2.2.6 Atomic Force Microscopy (AFM) method

AFM observation was used for the examination of surface roughness. Figure 2.2.7 shows the schematic drawing of AFM equipment (Nano Scope III, Digital Instrument Co. Ltd.). The raser and fhoto diode detect the bending which results from the force between the cantilever edge and the atoms of sample surface. And the cantilever was controlled by z direction feedback circuit. In tapping mode AFM the cantilever is vibrated by piezoelectric device, and the prove doesn't contact the sample all the time. An image of the surface is obtained by scanning in x and y directions.

The surface roughness is evaluated by the values of R_{MS} and R_{MAX}. R_{MS} is short for Root Mean Square and given by the following equation:

$$R_{MS} = \sqrt{\frac{\S(Z_i - Z_{ave})^2}{N}} \tag{2.5}$$

where Z_i is the Z value of each data point, Z_{ave} is the average of all Z value and N is the number of data points. R_{MAX} is the di®erence between the maximum and minimum height.

Note that it is di±cult to judge whether the ¯gures obtained by AFM measurements are correct because the worn cantilever shows the completely di®erent images.

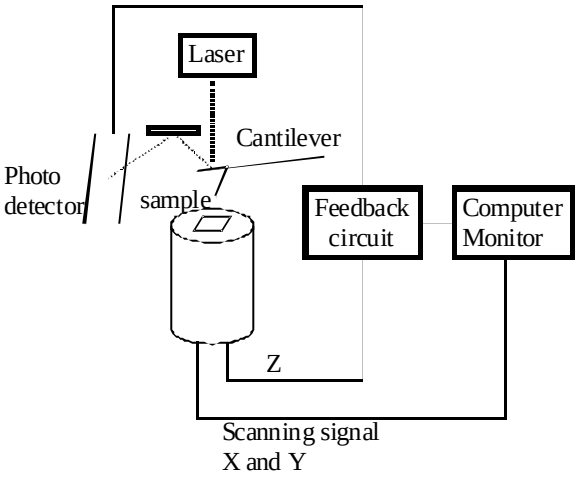

Figure 2.2.7: The chematic drawing of AFM system.

2.2.7 Cross-sectional Transmission Electron Microscopy (TEM) observation

Cross section of the sample observed by TEM can provide a lot of imformation visually such as interfacial layer and ¯lm crystallization. The electron beam is accelerated and incident into the sample. Three level lens and two level apertures are usually used, and images magni¯ed over million fold is obtained. However there are many di±culties in making samples and TEM observation. The e-beam has to be passed through very thin ¯lm samples shaved for 100 nm with sandpaper, dimple grinder and ion milling.

The samples must be thin enough to transit the beam less than 30 um. We grinned by our hand and the ion milling without using (FIB).

The rare earth oxides were thought to be seen darker than Si atoms because of their heavy mass. There is a worry that the sample was changed during the observation when the electron beam is narrowed down to obtain high magni¯cation ¯gure.

2.2.8 X-ray Photoelectron Spectroscopy (XPS) method

XPS, also known as Electron Spectroscopy for Chemical Analysis (ESCA), is primarily used for identifying chemical species at the sample surface, allowing all elements. When X-rays of 1-2 keV energy are incident on a solid, they can eject electrons from their orbital. Photoemission consequently occurs as long as the X-ray energy exceeds the binding energy, and the energy of the eject photoelectrons from samples were measured to determine the chemical states. This electron binding energy is in°uenced by its chemical surroundings. For example, Si 2p spectrum has the peak at eV when the Si has four covalent bindings with Si. If Si connects with other materials such as O or metal atom, this peak shifts positively. The major use of XPS is for identi¯cation of compounds using energy shifts due to changes in the chemical structure of the sample atoms. And XPS is a surface-sensitive method because the emitted photoelectrons originate from the upper 0.5-5 nm of the sample. In this study XPS was used to examine the amounts of Si bindings in thick (>10 nm) ¯lms. The peak of Si=Si at eV were not seen in many cases because Si=Si binding meant that Si substrate was seen. However the peak which shifted about 1-3 eV from eV were seen, that is, SiO_2 or rare earth silicate exist in the ¯lms. I would like to discuss Si amount in the ¯lms comparing the same thick samples.

2.2.9 Characterization of electrical properties

High-frequency C-V measurements

In this study, leakage current density and equivalent SiO_2 thickness are most important information for gate dielectric application. These are obtained by measuring MIS capacitor electrical properties. High-frequency C-V characteristics were obtained with Precision LCR Meter (HP 4284A, Agilent) to measure the MIS capacitor's impedance as RC series circuit. The high-frequency voltage, whose amplitude was 20 mV, was applied on the d. c. voltage for bias.

Figure 2.2.8 shows ideal high-frequency C-V Characteristics of p-type Si MIS capacitor.

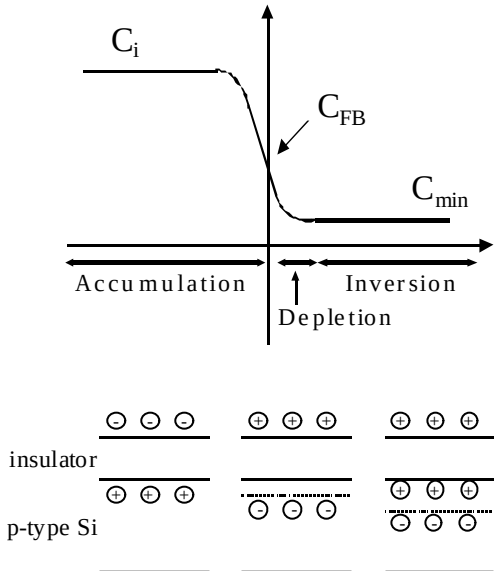

Figure 2.2.8: Ideal high-frequency C-V characteristics for MIS capacitor and charge distribution.

The ideal equivalent circuit is composed of a series capacitance of insulator component, C_i and Si surface component, C_s. When minus bias applied to the metal plate, it is called "accumulation" region. For an ideal MIS capacitance there is no current °ow in the structure, so voltage causes band bending at Si surface and accumulation of majority carriers(holes). This is because this case is "accumulation". Total MIS capacitor in unit area of C is independent of applied voltage and given by

$$C = C_i = \frac{^2{}_0 k}{d}: \qquad (2.6)$$

C decreases near zero bias because broadening of accumulation charge cause series capacitance.

When zero bias applied and surface potential is zero, this is the case of "°at band condition". Si surface capacitance of C_s is not zero and given by

$$C_{sFB} = q\sqrt{\frac{\varepsilon_{Si} N_a}{kT}} \tag{2.7}$$

where N_a is Si substrate doping concentration. We obtain °at band capacitance of C_{FB} :

$$C_{FB} = C_{sFB} == C_i : \tag{2.8}$$

When a small positive voltage is applied, surface band bend downward and apart from Felmi level. This is the case of "depletion" because the majority carriers are depleted at the surface. C keeps decreasing because depletion region act as a dielectric in series with the insulator.

When a larger positive voltage is applied, the bands bend even more downward such that the intrinsic level at the surface crosses over the Felmi level. At this point the number of electrons(minority carriers) at the surface is larger than that of holes, the surface is thus inverted, and this is the case of "inversion". The total capacitance goes through a minimum because of following two reasons. First, the recombination-generation rates of electron cannot keep up with higher frequency signals. Experimentally for Metal-SiO_2-Si system it is possible at the frequency between 5 to 100 Hz that total capacitance increase again to the insulator capacitance. Second, once strong inversion occurs, the depletion-layer width reaches a maximum because the semiconductor is e®ectively shielded by further penetration of electric ¯eld by the inversion layer. Accordingly, the maximum width, W_m, of the surface depletion region can be obtained

$$W_m^2 = \frac{4\varepsilon_0^2 \varepsilon_{Si}}{q^2 N_a} kT \ln\left(\frac{N_a}{n_i}\right) \tag{2.9}$$

where n_i is intrinsic doping concentration.
And the corresponding total capacitance is given by

$$C_{min} = C_i == C_{smin} = \frac{\varepsilon_0 k}{d} == \frac{\varepsilon_0^2 \varepsilon_{Si}}{W_m} : \tag{2.10}$$

Actually for MIS capacitor °at band voltage of V_FB is not zero because there is the work function di®erence between Φ_m and Φ_s (ref. subsection(2.1.4). V_{FB} is given by

$$V_{FB} = \Phi_m - \Phi_s \tag{2.11}$$

$$= \Phi_m - (\Phi_{Si} + E_g/2 + \Phi_F) \tag{2.12}$$

where $\copyright_{Si} = 4{:}05eV$ and $E_g = 1{:}11eV$. And $\copyright_F$ is the difference between intrinsic level and Felmi level.

For a practical MOS capacitor, interface traps and oxide charges exist that will, in one way or another, affect the ideal MOS characteristics. These effects of charges in the SiO_2 and at the SiO_2/Si interface have been studied extensively. It has not been understood now whether these theories can apply to ultra-thin SiO_2 or high-k films. We consider here only two type factors, charges and traps. Charges in the dielectrics is called the fixed charge Q_f, and it can not be charged or discharged over a wide variation of applied gate voltage. The fixed charge density Q_f is located near the high-k/Si interface and its origin is thought excess Si(trivalent Si) or the loss of and electron from excess oxygen centers (nonbridgeing oxigen) near the high-k/Si interface. This positive Q_f causes the C-V curve to shift to more negative values of gate bias with respect to the the ideal C-V curve for both n-type and p-type substrates. The magnitude of the shift is generally evaluated at flat band voltage and ΔV_{FB} is used which is calculated as the difference between ideal V_{FB} and experimental V_{FB}. At the Si surface, there are some located states with energy in the forbidden energy gap of Si because the lattice of bulk Si and all the properties associated with its periodicity terminate. These surface(interface) states trap some charges when the surface potential bend down and states locate under the Felmi level. The trapped charges are consequently changed by the applied voltage, so the C-V curve doesn't shift in parallel compared with the ideal one. This also depend on the measured frequency because these trapping or releasing can not follow the ac voltage swing. The hysteresis loop in C-V curve occurs on the same reason. The interface state density(D_{it}) is evaluated by the density of the states located at the center of the forbidden band. Note that Q_f and D_{it} have difference unit, [C/cm^2] and [number of charges/eV cm^2], respectively.

These trapped charge affect not only the C-V characteristics but also MISFET characteristics. By trapping electrons and holes, surface states can reduce the conduction current in MISFETs. Furthermore, the trapped electrons and holes can act like charged scattering centers, located at the interface, for the mobile carriers in a surface channel, and thus lower their mobility. Interface states can also act like localized generation-recombination centers. These can lead to generation-recombination leakage currents and affect the dielectric reliability.

Terman method

Terman method is the estimation method of interfacial state densities by comparing measured high-frequency C-V curve with ideal one. Interfacial state density was calculated

by shift value from these curve and the value at the middle of forbidden band.

CVC program was suggested by North Carolina state university. It can calculate EOT considering quantum e®ect. Note that EOT is the value which is considered some compensation such as quantum e®ect or measuring frequency e®ect by leakage currents, not equal CET.

Leakage current density(J-V) measurements

J-V characteristics of MIS capacitor was measured by Precision Semiconductor Parameter Analyser (HP 4156C, Agilent). In an ideal MIS capacitor the conductance of the insulation ¯lm is assumed to be zero. Real insulators, however show carrier conduction by electrons and/or holes when the electric ¯eld or temperature is su±ciently high. The two types of conduction models will be explained here. First, Poole-Frenkel model is due to ¯eld-enhanced thermal excitation of trapped electrons into the conduction band and this is called trap-assist conduction . The expression of Poole-Frenkell emission is given by

$$J \propto E \exp\left[\frac{-q\left(\Phi_B - \sqrt{\frac{qE}{\pi\varepsilon}}\right)}{kT}\right] : \tag{2.13}$$

A plot of ln(J/E) versus $\sqrt{E}$ yields a straight line with a slope determined by the dielectric constant of the insulator and the plot segment contains the information of the barrier height as trapped charge in the insulator. This conduction process also has temperature dependence and J versus 1/T yields a straight line.

Second, Fowler-Nordheim model is one of tunneling emission caused by ¯eld ionization of trapped electrons into the insulator conduction band or by electrons tunneling from the metal Felmi energy into the insulator conduction band. The expression is given by

$$J \propto E^2 \exp\left[-\frac{4\sqrt{2m^*}\sqrt{q\Phi_B^3}}{3qhE}\right] \tag{2.14}$$

and a plot of ln(J/E) versus $\sqrt{E}$ yields a straight line. The Fowler-Nordheim (tunnel) emission has the strongest dependence on the applied voltage but is essentially dependent of the temperature. These plots and/or temperature dependence thus decide the carrier transport type.

Chapter 3

Fabrication and characterization of amorphous Yb_2O_3, Tm_2O_3 and Gd_2O_3

In this chapter, the fundamental electrical properties of amorphous Yb_2O_3, Tm_2O_3 and Gd_2O_3 are investigated. The temperature of Si substrate during the deposition was room temperature or 250°C to obtain amorphous ¯lms, not crystallized. The dielectric constants of Yb_2O_3, Tm_2O_3 and Gd_2O_3 are introduced at ¯rst. Surface morphology and electrical properties are demonstrated, and typical dependence on RTA temperature is described. It was found that good interface layer of silicate growing during RTA can suppress the leakage currents and realize the excellent C-V curve. Tm_2O_3 and Gd_2O_3 were deposited on not only HF-last but also chemically oxidized Si. It seems to be the same reason why the better electrical properties are obtained by deposition on chemically oxidized Si than that on HF-last Si.

3.1 Fabrication of amorphous ¯lms

The fabrication processes of 5 nm-thick Yb_2O_3 ¯lms in section 3.2 and 3.3 can be summarized as follows:

- HF-last n-Si(100), 8-20 - cm (substrate No.1 as shown in table 2.3)
- substrate temperature during deposition of room temperature
- RTA at 200, 300, 400, 600°C in O_2 or N_2 ambient for 5 min.

The fabrication processes of 12 nm-thick Tm_2O_3 and 25 nm-thick Gd_2O_3 ¯lms in section 3.2 and 3.3 can be summarized as follows:

- HF-last n-Si(100), 0.8-1.2 - cm (substrate No.3 as shown in table 2.3)
- substrate temperature during deposition of room temperature
- RTA at 400, 600, 800 and 1000°C in O_2 ambient for 5 min.

The fabrication processes of thin Tm_2O_3 and 3.5 nm-thick Gd_2O_3 to investigate the e®ect of Si substrate chemical oxidation before ¯lm deposition in section 3.4 can be summarized as follows:

- HF-last n-Si(100) and chemically oxidized substrate which has 0.5 nm-thick chemical oxide, 0.8-1.2 - cm (substrate No.3 as shown in table 2.3) for Tm_2O_3
- HF-last n-Si(100) and chemically oxidized substrate which has 0.5 nm-thick chemical oxide, 13-15 - cm (substrate No.2 as shown in table 2.3) for Gd_2O_3
- substrate temperature during deposition of 250°C
- RTA at 400°C in O_2 ambient for 5 min.

Al for top and bottom metal electrode was evaporated to make MIS capacitors.

3.2 Surface morphology for these ¯lms

First of all, AFM measurements were done to check surface roughness and crystallization of Yb_2O_3, Tm_2O_3 and Gd_2O_3. Figure 3.2.1 (a) shows AFM images of as-deposited Yb_2O_3, whose physical thickness was 5 nm, showing very smooth surface like SiO_2. After RTA at 400°C in O_2, the sharp dots appeared at the surface as shown in Figure 3.2.1 (b), and RMS value dramatically increased from 0.065 nm to 0.892 nm. After RTA at 600°C in O_2, RMS value was a little smaller than that for 400° RTA and their dots size became bigger. This tendency was also seen in N_2 RTA samples, in other words,

the samples annealed from 200 to 400°C had rough surface and 600°C anneal a little bit suppressed the roughness. The surface roughness is caused by the atomic migration with some heating, not by the ¯lm crystallization as follows. First, if ¯lms crystallized and these dots were crystal grains, the grain size was too small. The typical grain size are about a few ¹m. Next it was reported that thin Lu_2O_3 ¯lms of 4.5 nm were able to suppress the agglomeration and/or crystallization during the RTA [15]. The e®ect of surface roughness on leakage currents will be discussed next section.

It was also demonstrated for Gd_2O_3 ¯lms that smooth surface roughened by RTA. For 12 nm-thick Tm_2O_3 ¯lms, the large hillocks were observed after 400°C RTA as shown in Figure 3.2.2 (a) and (b). The height of these hillocks were approximately twice higher than the ¯lm thickness of 12 nm from R_{MAX} value of 19.6 nm. 1000°C RTA created completely di®erent reaction from the heat migration or agglomeration as shown in Figure 3.2.2 (c) and (d). It was con¯rmed that Tm_2O_3 ¯lms deposited at room temperature were amorphous even for 800°C RTA, but after 1000°C RTA, the small peak of cubic Tm_2O_3(222) was observed. This crystal structure of cubic(222) was also observed in the patterns of Lu_2O_3 on Si(100) [15]. It seemed that thicker ¯lms were easily crystallized after high temperature RTA although thinner ¯lms less than 5 nm kept amorphous state.

Figure 3.2.3 (a) shows the cross-sectional TEM image for Al/Yb_2O_3/Si(100). This ¯lm was annealed at 200°C in O_2 for 5 minutes, and ¯lm thickness was estimated for 5.0 nm from this ¯gure. Yb_2O_3 was amorphous and extremely smooth Yb_2O_3/Si interface was realized. It can be hardly observed any interfacial layer, so RTA at 200°C seemed to grow no interfacial layer. However, the contrast in the ¯lms was not de¯nite and it is di±cult to decide the ¯lm/Al electrode interface. It indicated two possibility. First the ¯lm had gradual distribution of Yb, O and/or Si. Second interfacial layer like Al_2O_3 exist at the top interface because Al_2O_3 is easy to form without higher heating.

In contrast, Figure 3.2.3 (b) shows the cross-sectional TEM image for Gd_2O_3/Si(100). This ¯lm was deposited at 250°C and annealed at 400°C in O_2 for 5 minutes. Gd_2O_3 was amorphous but unclear Gd_2O_3/Si interface showed some Gd-silicate layer made by Gd, O and Si mixing during deposition and/or RTA.

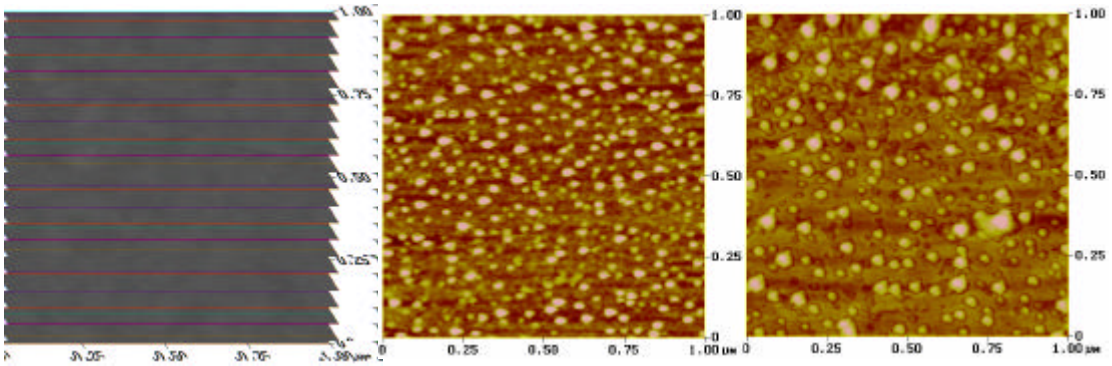

Figure 3.2.1: AFM images for Yb_2O_3 ¯lms(1 ¹m £ 1¹m, z:5 nm/div.).
(a) as-deposited (RMS:0.065 nm), (b) after 400ºC RTA in O_2 (RMS:0.892 nm) and
(c) after 600ºC RTA in O_2 (RMS:0.620 nm).)

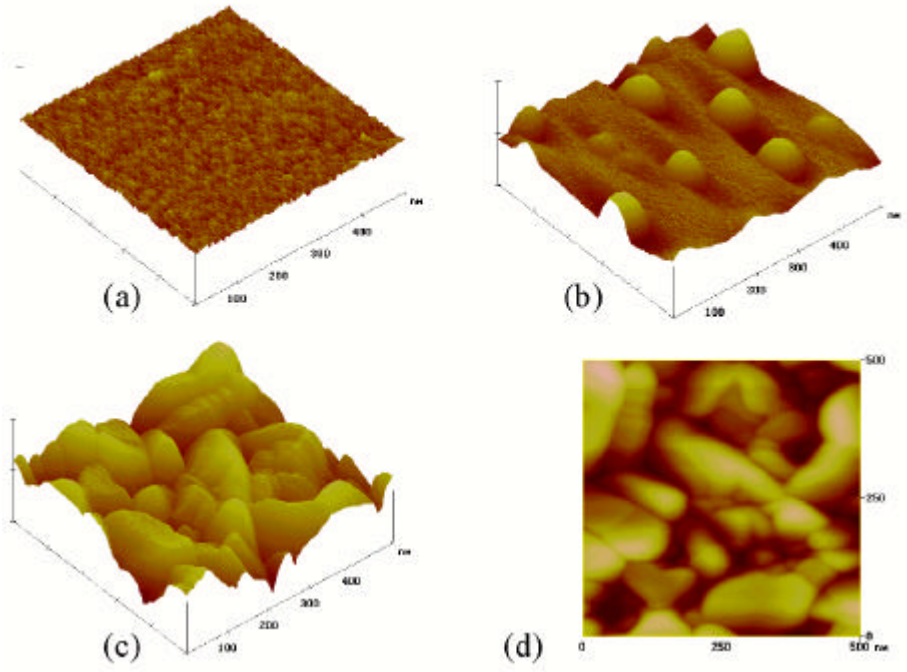

Figure 3.2.2: AFM images for Tm_2O_3 ¯lms(500 nm £ 500 nm).
(a) as-deposited (RMS:0.110 nm, z:5 nm/div.),
(b) after 400ºC RTA (RMS:2.64 nm, z:25 nm/div.),
(c) after 1000ºC RTA (RMS:4.88 nm, z:25 nm/div.) and
(d) two dimension surface image after 1000ºC RTA (z:25 nm/div.)

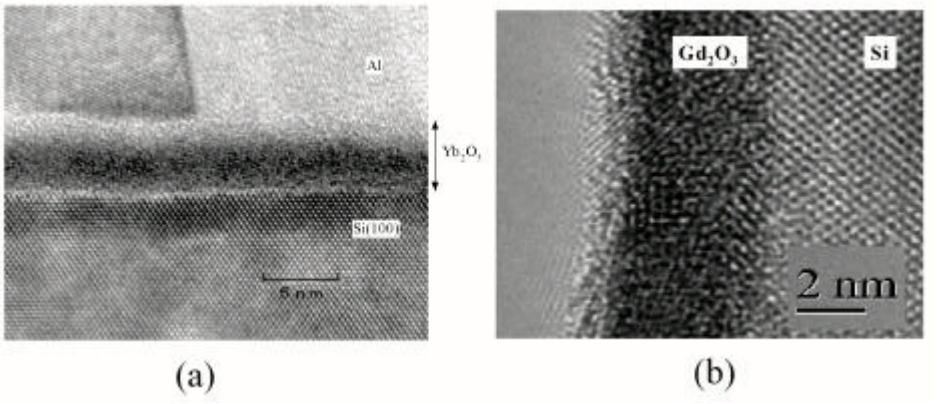

Figure 3.2.3: Cross-sectional TEM image for (a) $Al/Yb_2O_3/Si(100)$ and (b) $Gd_2O_3/Si(100)$.

3.3 Electrical properties of MIS capacitor

Figure 3.3.1 shows the C-V characteristics for 5.0 nm-thick Yb_2O_3 at the di®erence frequencies. As-deposited ¯lm had large frequency dependence and large V_{FB} shifts, as shown in Figure 3.3.1 (a). The hysteresis was observed and this is polarization type, which suggested that mobile charges or traps in the ¯lms had slow response. This indicated, in other words, there were high D_{it} and/or large Q_{ss} in the ¯lms. Note that frequency dependence is likely to be caused by higher resistivity of Si substrate because RC series circuit were joined in the equivalent capacitance circuit. However it is not correct characteristics because the curve measured at 10 kHz went down to minus values for negative voltage.

Figure 3.3.1 (b) shows the C-V characteristics for the same ¯lm followed by the 400°C RTA in O_2. Frequency dependence at accumulation capacitance was smaller than that of as-deposited ¯lm , and V_{FB} was improved to -1 V. This clearly shows the values of D_{it} and Q_{ss} decrease by RTA. This e®ect also appeared after 600°C RTA, as shown in Figure 3.3 (c), however the frequency dependence at the weak inversion region was caused.

Figure 3.3.2 (a) shows C-V characteristics measured at 100 kHz for as-deposited or annealed Yb_2O_3 in O_2 or N_2 at 200, 300 and 400°C. The accumulation capacitance of N_2 annealing was a little higher than that of O_2 annealing. This indicates that the interfacial layer is easier to grow in O_2 ambient because O_2 atoms additionally penetrate into the ¯lm during RTA . It was also found that 200°C RTA hardly made interfacial layer, which was also con¯rmed by TEM image shown in Figure 3.2, because the accumulation capacitance didn't degrade compared with that of as-deposited sample. The CET of the sample after 200°C RTA in N_2, which was calculated by the accumulation capacitance

at 0.5 V, was 1.38 nm. From the equation of (1.2), dielectric constant of thin Yb_2O_3 was approximately 14. Hysteresis width increased after 200°C RTA and decrease after 300°C RTA. The reason of this is not clear but it was found that su±cient temperature annealing distinguished mobile charges and hysteresis. V_{FB} was improved by higher temperature RTA to ideal V_{FB} of 0.23 V little by little.

Figure 3.3.2 (b) shows C-V characteristics measured at 100 kHz for as-deposited or annealed Yb_2O_3 in O_2 at 200, 400 and 600°C. The accumulation capacitance was largely degraded after 400°C RTA and dielectric constant of the ¯lm after 600°C RTA decreased approximately 7. This value was so small that the ¯lm consisted of SiO_2 and Yb-silicate not of Yb_2O_3. V_{FB} was improved to 0.5 V after 600°C RTA. However, gentle capacitance rising from inversion to accumulation region indicated the D_{it} existence these traps, and this seems to be caused by interfacial mixing by high temperature RTA. The reason why V_{FB} remained 0.5 V was thought to be in Al/Yb_2O_3 interface.

Figure 3.3.3 shows the relationship of CET calculated by the accumulation capacitance at 0.5 V and leakage current density (J) at 1.0 V as a function of RTA temperature. All samples were annealed in O_2. Leakage current decreased with increasing CETs, showing interfacial layer like SiO_2 suppressed leakage currents e±ciently. It also showed that leakage currents were decided by interfacial layer thickness or interfacial gradual composition

Figure 3.3.4 (a) shows dependence of 12 nm-thick Tm_2O_3 C-V characteristics on RTA temperature at 1 MHz. As-deposited Tm_2O_3, having large frequency dependence and charge-injection-type hysteresis. The dielectric constant of 15 was obtained from 100 kHz C-V curve. After 400°C RTA, frequency dependence and hysteresis were completely disappeared. Physical thickness, which were obtained by Ellipsometry, was about 1 nm larger than that of as-deposited ¯lm. It was found that RTA increased the ¯lm thickness and interface layer was not SiO_2 because of the capacitance calculation. This is the same reaction as Yb_2O_3 case and interface layer was Tm-silicate. ¢ V_{FB} was improved by higher temperature RTA little by little. After 1000°C RTA, however, C-V curve were degraded and because the ¯lm was crystallized.

Figure 3.3.4 (b) shows J-V properties for the same samples. The leakage currents after 400°C RTA increased dramatically compared with as-deposited ¯lm, not suppressed. AFM images shown in Figure 3.2.1 explained this leakage mechanism: The rough surface after 400°C RTA had a lot of leakage path from Si to metal electrode. However higher temperature RTA such as 800°C made thick interfacial layer, which suppressed leakage currents e±ciently.

On the other hand, for 25 nm-thick Gd_2O_3 ¯lms deposited at room temperature

and annealed at 400°C in O_2, the same experiments and evaluation were done and the dielectric constant of 13 was obtained. Note that this value contained somewhat interfacial layer of Gd-silicate.

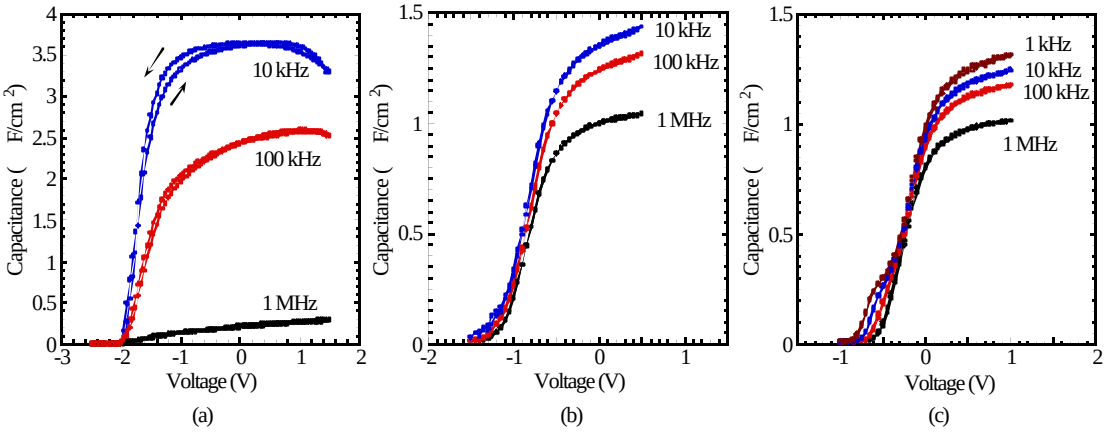

Figure 3.3.1: C-V characteristics for Yb_2O_3. (a) as-deposited, (b) after 400°C RTA in O_2 and (c) after 600°C RTA in O_2

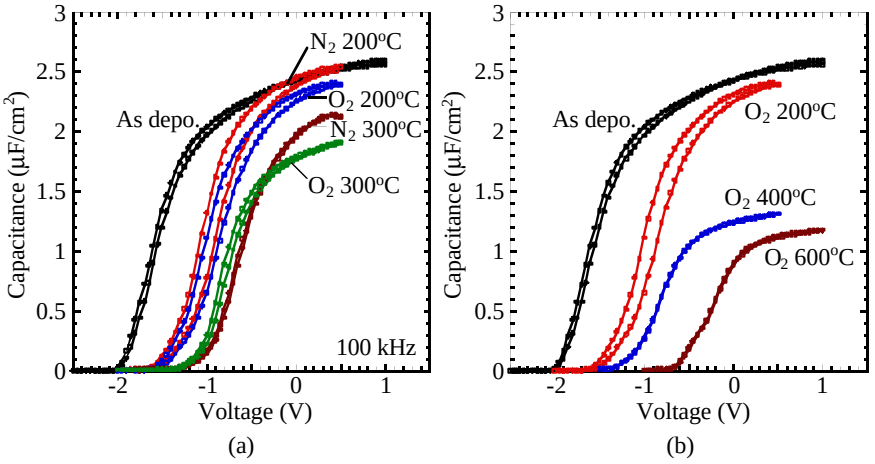

Figure 3.3.2: C-V characteristics at 100 kHz for Yb_2O_3
(a) as-deposited and after RTA in O_2 or N_2 at 200, 300 and 400°C and
(b) as-deposited and after RTA in O_2 at 200, 400 and 600°C.

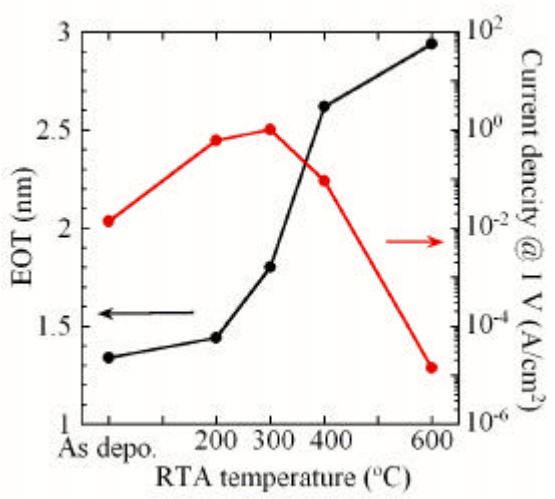

Figure 3.3.3: CET and J plot for Yb_2O_3 as a function of RTA temperature.

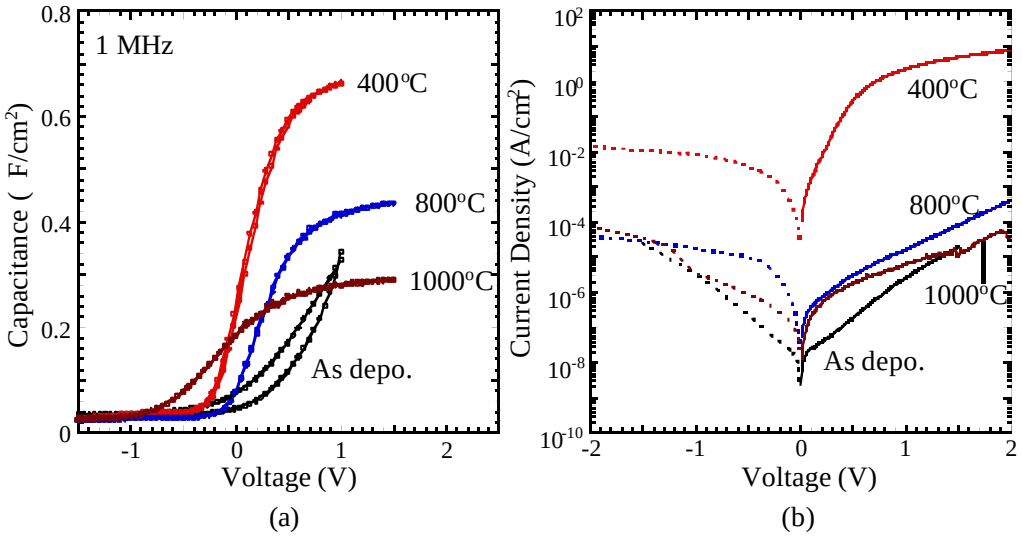

Figure 3.3.4: (a) C-V and (b) J-V characteristics for as-deposited and annealed Tm_2O_3.

3.4 E®ect of Si chemical oxidation before ¯lm deposition

We tried to oxidize clean HF-last Si substrate to make 0.5nm-thick chemical oxide. The interfacial properties and the e®ect on electrical properties are discussed in comparison with samples deposited on HF-last Si. Tm_2O_3 or Gd_2O_3 thin ¯lms were deposited on HF-last and chemically oxidized Si at 250°C and annealed at 400°C in O_2 simultaneously.

Figure 3.4.1 (a) shows C-V characteristics for thin as-deposited Tm_2O_3 on HF-last Si substrate and Figure 3.4.1 (b) shows C-V characteristics for as-deposited Tm_2O_3 on chemically oxidized Si substrate. Hysteresis width and frequency dependence were suppressed by interface chemical oxide. Figure 3.4.1 (c) and (d) show C-V characteristics for 400°C RTA Tm_2O_3 on HF-last and chemical oxidized Si substrate. ¢V_{FB} shifts of the sample on chemically oxidized Si were 0.1 V smaller that of the sample on HF-last Si.

Figure 3.4.1 (d) and (e) show J-V properties for the same samples. In spite of almost the same CET values, the leakage current density of the sample on chemically oxidized Si was found to be about one orders of magnitude smaller than that on the HF-last Si.

The surface morphology was examined by AFM images. RMS values of all samples were very small around 0.1 nm. It was found that RTA didn't roughen for these thin ¯lms and there were any di®erences between HF-last and chemically oxidized Si.

On the other hand, for 3.5 nm-thick Gd_2O_3, leakage currents were dramatically deacreased three orders of magnitude on chemically oxidized Si compared with the ¯lms on HF-last Si although both C-V curves complete the same. From AFM observation, surface morphology on chemically oxidized Si was °at compared with that on HF-last Si.

These results indicated two facts. The interfacial layer of silicate on chemical oxidized Si were like SiO_2 properties with rich SiO_2 and a®ected the barrier in the MIS structure band diagram, accordingly leakage currents were e±ciently suppressed by chemical oxide.

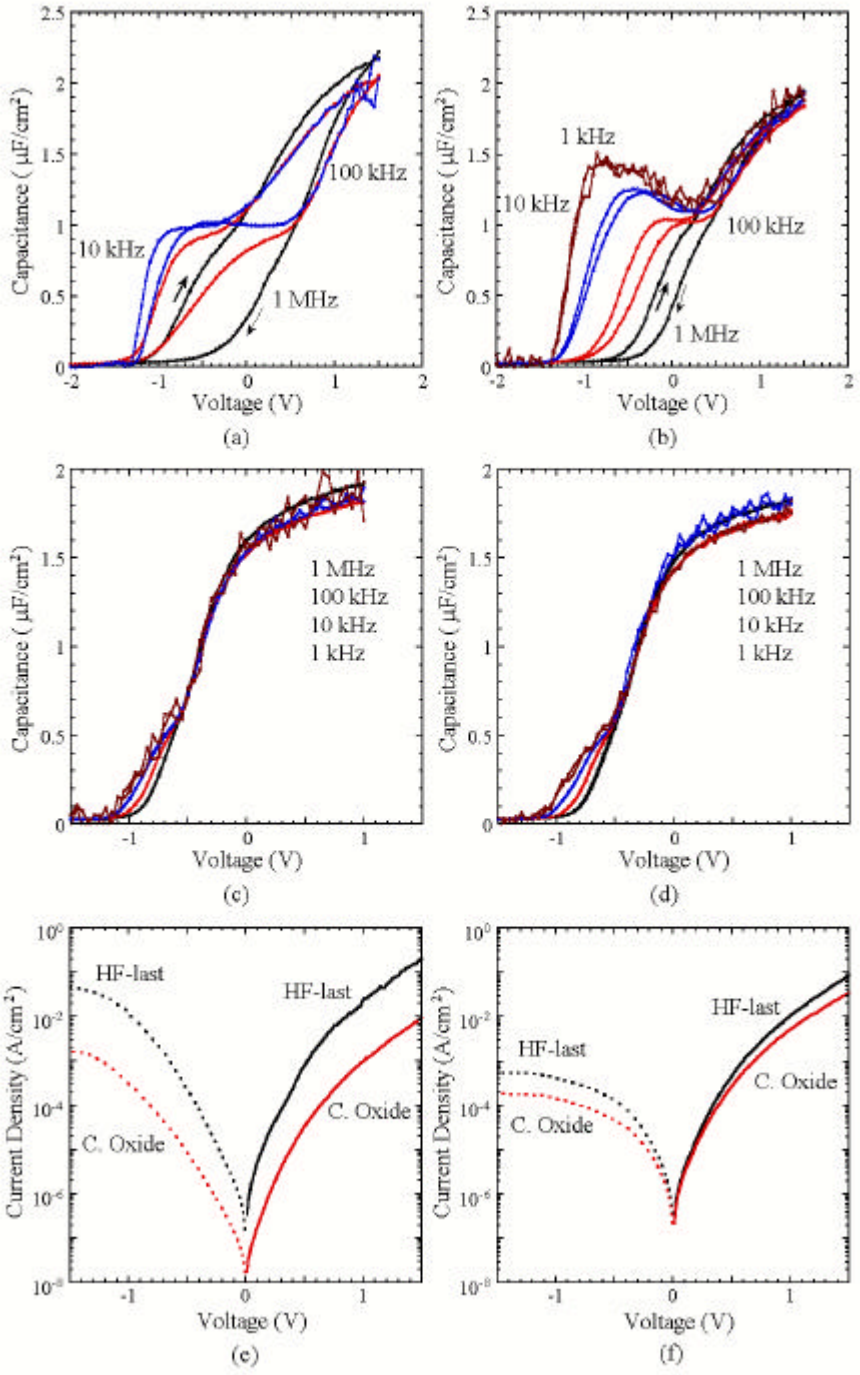

Figure 3.4.1: The improvements of C-V and J-V characteristics for Tm_2O_3 films. C-V characteristics for (a) as-deposited Tm_2O_3 on HF-last Si, (b) as-deposited Tm_2O_3 on chemically oxidized Si, (c) Tm_2O_3 on HF-last Si after 400°C RTA and (d) Tm_2O_3 on chemically oxidized Si after 400°C RTA.
J-V characteristics for (e) as-deposited Tm_2O_3 on HF-last and chemically oxidized Si and (f) Tm_2O_3 on HF-last and chemically oxidized Si after 400°C RTA.

3.5 Some problems for gate dielectrics application

So far, RTA was especially essential process to improve the electrical properties of high-k ¯lm as discussed in previous section, and its condition has to be determined with much carelessness. For example, insu±cient RTA time caused large negative ¢V_{FB}. It is di±cult to ¯nd the best temperature because leakage currents and CET have trade-o®. To summarize the electrical properties for not only rare earth oxide but all high-k oxides, Figure 3.5.1 shows some parameters as a function of RTA temperature by using Yb_2O_3 data.

The ratio of accumulation capacitance measured at 1 MHz and that at 100 kHz shown in Figure 3.5.1 (a) and ¢V_{FB} shifts at 1 MHz shown in Figure 3.6 (b) decreased progressively. These results indicated that the defects and charge traps in the ¯lms decreased with increasing RTA temperature. Hysteresis width at 1 MHz shown in Figure 3.5.1 (c) disappeared after 400°C RTA, however after 600°C RTA it appeared again. Maximum voltage di®erence between 1 MHz and 10 kHz at rising region from inversion to accumulation in C-V curve correspondingly decreased and increased again from 200°C RTA, shown in Figure 3.5.1 (d).

It is clearly showed that RTA temperature for best electrical properties has one point not the highest temperature. Note that there were opposite two facts. One is the e®ect appeared both C-V and J-V characteristics, for example the large leakage currents with increasing hysteresis width shown in the Yb_2O_3 data from as-depo. to 200°C RTA. The other is the e®ect appeared either C-V and J-V characteristics, for example the small leakage currents for the same C-V curve in the Gd_2O_3 data on HF-last and chemically oxidized Si.

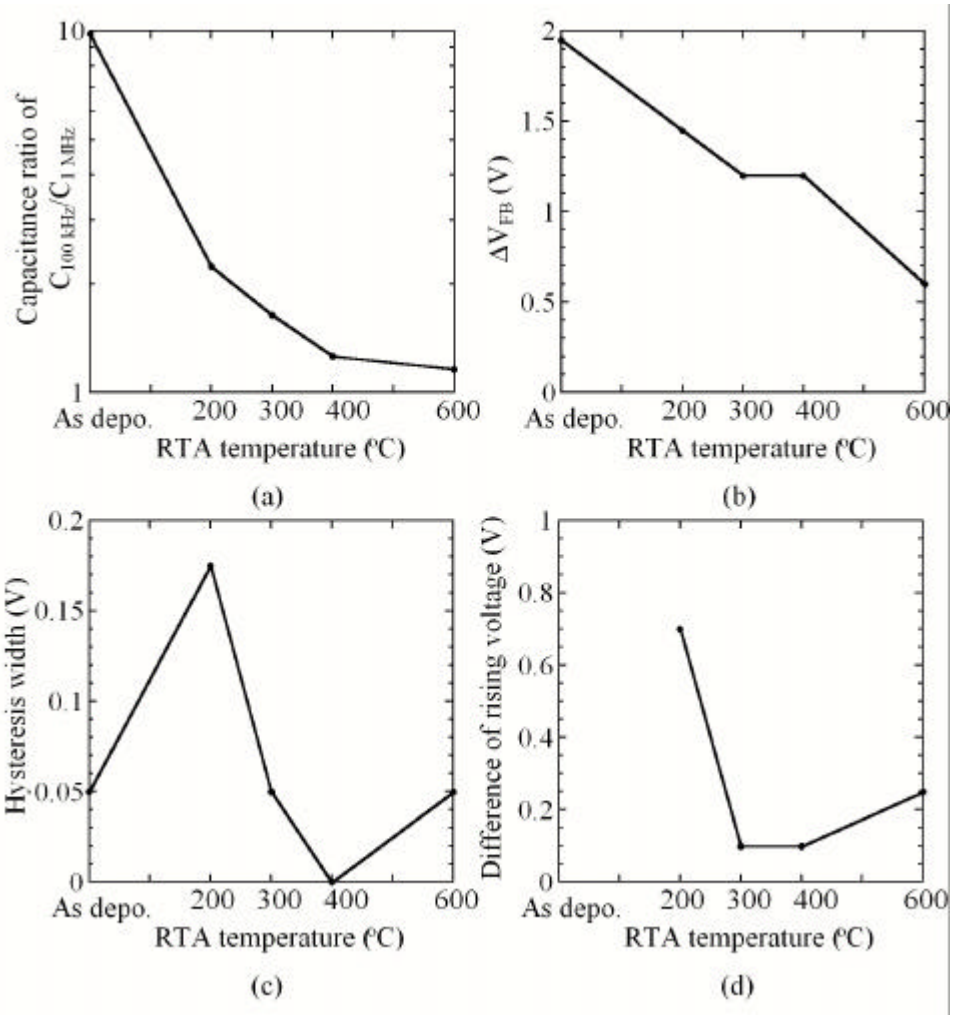

Figure 3.5.1: Summary of the C-V characteristics as a function of RTA conditions.
(a) Capasitance ratio of 1 MHz / 100 kHz (b) V_{FB} shifts at 1 MHz
(c) Hysteresis width at 1 MHz (d) Di®erence of rising voltage from 1 MHz to 10 kHz

Chapter 4

Dependence of amorphous Tm_2O_3 and Gd_2O_3 properties on Si surface orientation

In this chapter, amorphous Tm_2O_3 and Gd_2O_3 were deposited on HF-last Si(100), (110) and (111) substrate simultaneously at 250°C. First, the electrical properties for MIS capacitors of Tm_2O_3 or Gd_2O_3 are investigated. In C-V characteristics, CET, ¢V_{FB} and D_{it} are important parameters to evaluate the dependence on Si orientation. Next, the leakage properties are demonstrated and the di®erences of leakage currents on Si orientation are discussed. The e®ect of chemically oxidized Si on these Si orientation dependence are also demonstrated.

4.1 Fabrication of amorphous ¯lms on various oriented Si

The fabrication processes of 4 nm-thick Tm_2O_3 and 3 nm-thick Gd_2O_3 MIS capacitor in this chapter can be summarized as follows:

- HF-last p-Si(100),(110) and (111) substrate with
  2-8, 5-8 and 10-20 - cm respectively (substrate No.4, 5 and 6 shown in table 2.3)
- substrate temperature during deposition of 250°C
- RTA at 400°C in O_2 ambient for 5 min.
- Ag top and bottom electrode evaporation

4.2 Dependence of electrical properties on Si orientation

Figure 4.2.1 (a) shows C-V characteristics for Tm_2O_3 on Si(100), (110) and (111) substrate after 400°C RTA. The physical thickness of 4 nm measured by ellipsometry showed that the deposition rate or ¯lm thickness were not signi¯cantly di®erent on various oriented Si. So the di®erence of accumulation capacitance was thought to be caused by ¯lm composition. ¢V_{FB} were so small that the dependence on Si orientation was not clear. considering the Si substrate resistivity di®erences. For 12nm-thick Tm_2O_3, V_{FB} shifts were also small (less than 0.1 V) and the dependence of surface orientation wasn't observed.

Figure 4.2.1 (b) shows C-V characteristics for 3 nm-thick Gd_2O_3 on HF-last Si(100), (110) and (111) substrate after the same 400°C RTA. CETs were 0.5 nm di®erence on (110) and (111) although these ¯lms were deposited and annealed simultaneously. To con¯rm the amount of Gd atoms, RBS measurements were performed. Figure 4.2.2 shows the RBS spectra for these as-deposited ¯lms and they had almost the same Gd amount. It was clear that di®erence of CET didn't depend on Gd_2O_3 deposition rate but was caused by the interfacial layer on various oriented Si. It suggested in other words that the compositions and/or thickness of interfacial Gd-silicate layer were di®erent.

¢V_{FB} depended on Si surface orientation as shown in Figure 4.2.3. An example of SiO_2 with same CET of 1.5 nm is also plotted as a reference [16]. V_{FB} shifts for (110) was larger than that of (100) and the V_{FB} shifts of (111) was largest among them. It was similar to the SiO_2 case and the ¯xed charge density in the Gd_2O_3 on (111) was the

largest. ¢V_{FB} of 20 nm-thick Gd_2O_3 is also plotted and the di®erence of the values was smaller. D_{it} calculated roughly by Terman method had the same tendency like ¢V_{FB}.

Figure 4.2.4 (a) shows J-V characteristics for the same samples. There was a little dependence of the leakage currents on Si surface orientation. The surface roughness was very small and little orientation dependence was observed from AFM images. Figure 4.2.4 (b) shows the leakage current density at -1 V as a function of CET. Our amorphous data showed lower leakage currents compared with the crystalline Gd_2O_3 ¯lm reported by [9]. It should be noted that leakage current density and CET had a correlation. In other words, the leakage current density was the largest for the smallest CET. It suggested that the equivalent interfacial layer on Si(111) was thinnest of the three and this interfacial layer mainly determined the leakage currents.

Figure 4.2.5 (a) shows the cross-section TEM image for Al/Gd_2O_3/Si(110) structure. It was observed that Si crystal grain entered the Gd_2O_3 ¯lm although this was as-deposited ¯lm but It is possible for Gd_2O_3 that much Si was penetrated during only 250°C deposition and silicate reaction occurred. However there were some factor in TEM sample fabrication process because rare earth ¯lms had some problems such as moisture degradation or something. When higher electron beam focused the ¯lm, the Gd_2O_3 ¯lm changed its form as shown in Figure 4.2.5 (b). It seemed that the ¯lm was deoxidized and separated from Si substrate. So it is di±cult to evaluate the interface properties visually using TEM images.

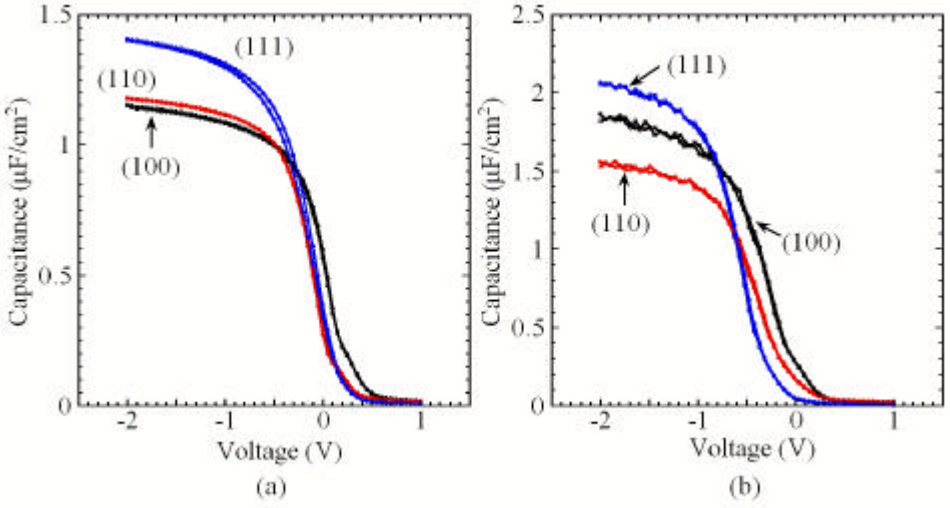

Figure 4.2.1: C-V characteristics for (a) 4 nm-thick Tm_2O_3 and (b) 3 nm-thick Gd_2O_3 on HF-last Si(100), (110) and (111) substrate after 400°C RTA.

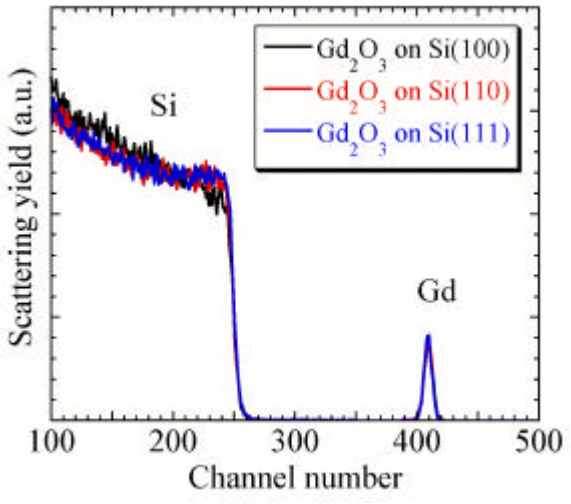

Figure 4.2.2: RBS spectra for as-deposited Gd_2O_3 ¯lms on Si(100), (110) and (111) substrate.

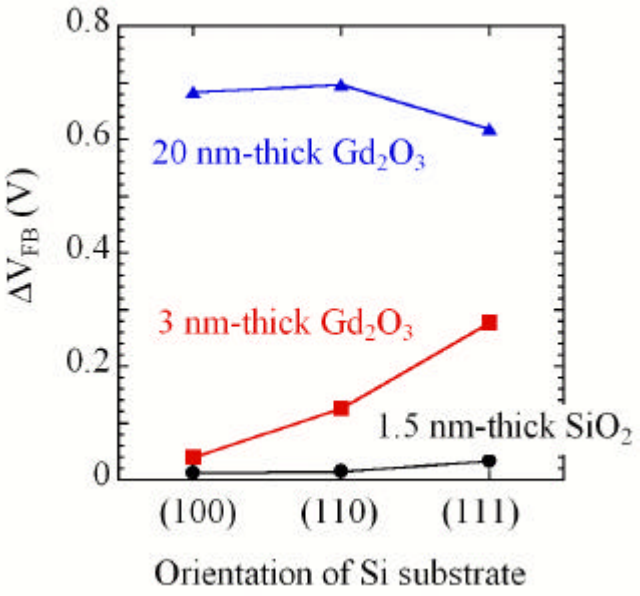

Figure 4.2.3: Dependence of ¢V_{FB} on Si substrate orientation

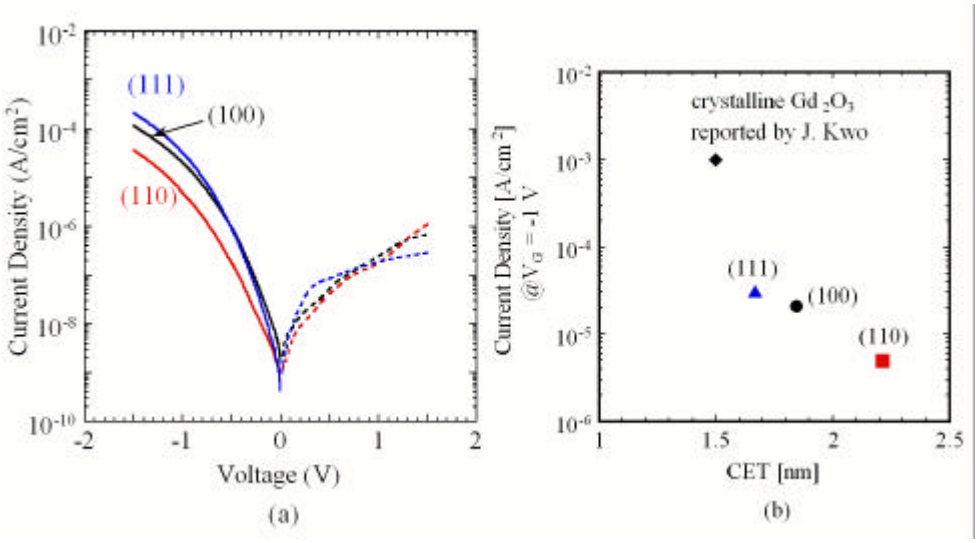

Figure 4.2.4: (a) J-V characterisitcs and (b) leakage current density as a function of CET on various oriented Si.

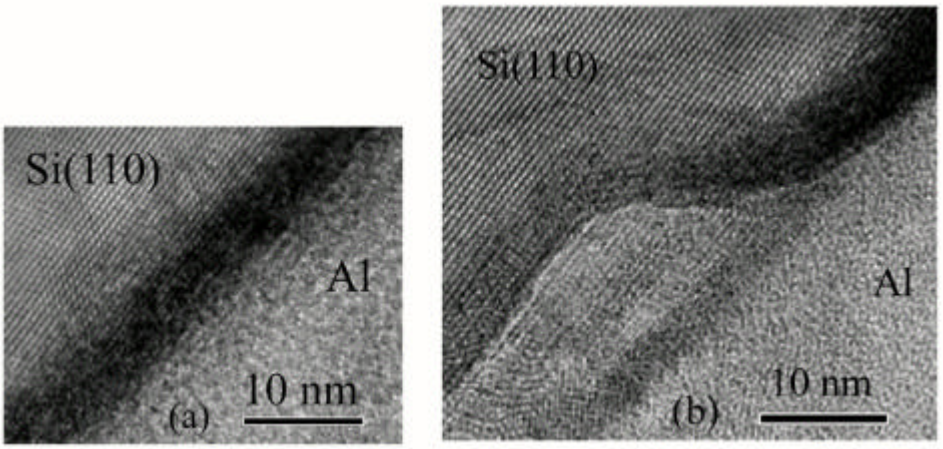

Figure 4.2.5: Cross-sectional TEM image for $Al/Gd_2O_3/Si(110)$.

4.3 The effect of substrate chemical oxidation on the Si orientation dependence

It has already known that the samples on the chemically oxidized Si had smaller leakage currents because high quality Gd-silicate at the interface and smooth surface could be obtained as discussed in previous chapter. The dependence of the electrical properties on chemically oxidized Si(100), (110) and (111) are demonstrated here using Gd_2O_3 as shown in Figure 4.3.1 because the effect of chemical oxide was significantly observed for 3.5 nm-thick Gd_2O_3 as described in section 3.4. Amorphous Gd_2O_3 films were deposited on chemically oxidized Si at 250°C as the same way of HF-last Si.

The orientation dependence of CET was much smaller compared to the case on HF-last Si as shown in Figure 4.3.1 (a). It suggested that uniform interface layers were formed by the use of chemical oxide on each oriented Si. Although the effect of orientation on CET seemed to be disappeared by the existence of chemical oxide, there was the same orientation dependence of V_{FB} shifts as SiO_2. Figure 4.3.1 (b) shows the dependence of leakage current density at -1 V on substrate orientation. It was found that the dependence of leakage currents on chemically oxidized Si was significantly smaller than that on HF-last Si. For as-deposited films, the dependence of leakage currents on HF-last Si orientation was significant large. It is explained by the available bonds per unit area on Si surface whose number in turn of (100) < (110) < (111). Ultra-thin chemical oxide suppress this effect and the orientation dependence was so small. After RTA, the difference became very small on both HF-last and chemically oxidized Si, and this result indicated that interface quality for leakage currents were improved to the almost the same level.

We have performed Terman method to determine D_{it}. Figure 4.1.10 shows the dependence of D_{it} on substrate orientation. It was found that the dependence of D_{it} on both HF-last and chemically oxidized oriented substrate were similar to that of SiO_2.

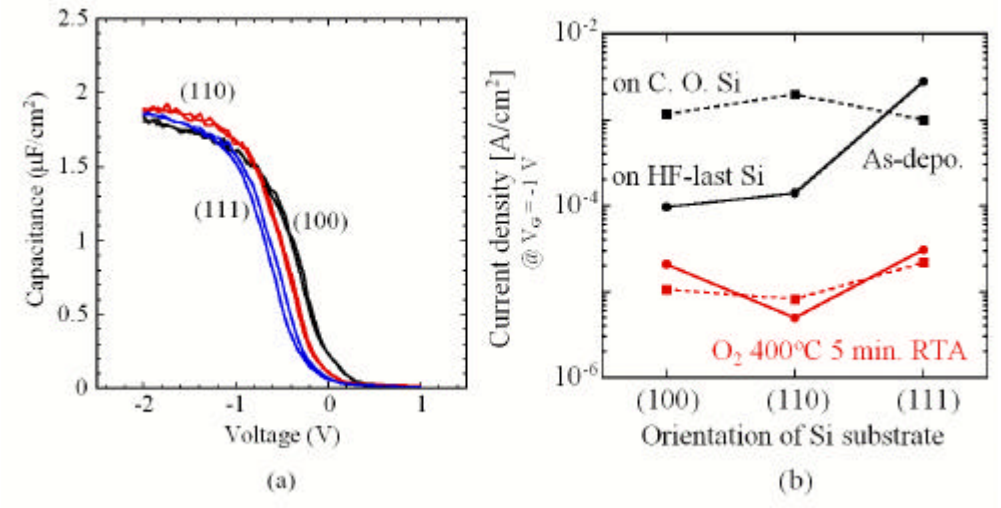

Figure 4.3.1: (a) C-V characteristics for Gd_2O_3 on chemically oxidized Si(100), (110) and (111) and (b) leakage current density on HF-last or chemically oxidized various oriented Si.

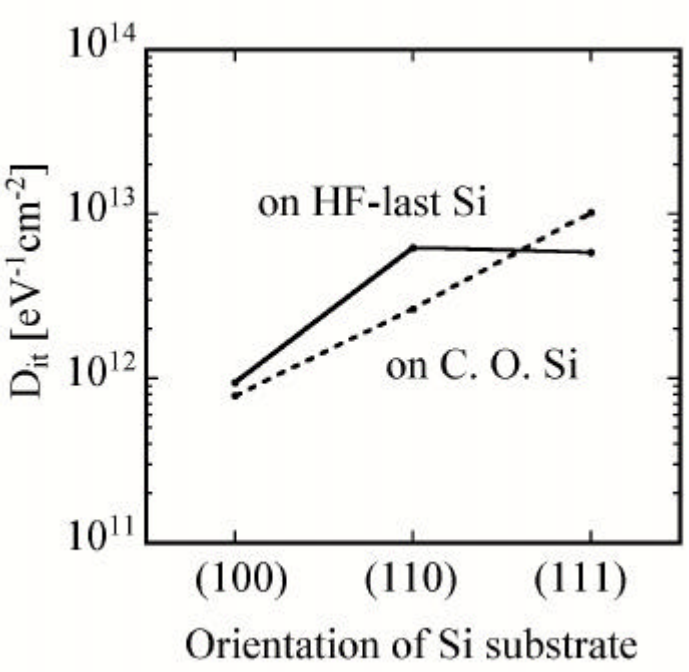

Figure 4.3.2: Dependence of D_{it} on Si substrate orientation.

4.4 Summary of this chapter

Electrical characteristics of amorphous Gd_2O_3 and Tm_2O_3 on p-type Si(100), (110) and (111) were studied. It was con¯rmed that the Gd or Tm amount deposited on various oriented Si were almost the same. The orientation dependence of ¢V_{FB} and D_{it} of Gd_2O_3 were similar to those of SiO_2 and Si(100) had the best characteristics among them. The interfacial layer formations on HF-last Si(100), (110) and (111) were considered to be di®erent in composition and/or thickness, and this layer e®ectively suppressed leakage currents. The dependence of ¢V_{FB} and D_{it} on oriented Si were observed using chemically oxidized Si although CET dependence was disappeared. For Tm_2O_3, the dependence of ¢V_{FB} and D_{it} on oriented Si were small compared with the Gd_2O_3 case.

Chapter 5

Dependence of crystalline Tm_2O_3 and Gd_2O_3 properties on Si surface orientation

In this chapter, Tm_2O_3 and Gd_2O_3 were deposited on HF-last Si(100), (110) and (111) substrates simultaneously at over 600°C. Tm_2O_3 or Gd_2O_3 crystal structure is thought to be different on each Si orientation, so at first the dependence of Tm_2O_3 or Gd_2O_3 crystal structure on Si orientation are demonstrated. The electrical properties for MIS capacitors of crystallized Tm_2O_3 or Gd_2O_3 are investigated. Leakage currents are most important parameter for epitaxial films, so leakage mechanism are discussed using AFM images and SIMS depth profiling. Moreover temperature dependence of C-V and J-V characteristics are demonstrated as a function of Si orientation.

5.1 Fabrication of crystallized ¯lms on various oriented Si

Tm_2O_3 and Gd_2O_3 were deposited on Si(100),(110) and (111) substrate at over 600°C to obtain the epitaxial ¯lms. The fabrication processes of 25 nm-thick Tm_2O_3 and 12 nm-thick Gd_2O_3 MIS capacitor in this chapter can be summarized as follows:

- TF p-Si(100),(110) and (111) substrate with 2-8, 5-8 and 10-20 - cm respectively (substrate No.4, 5 and 6 shown in table 2.3) for Tm_2O_3 and 0.012-0.02, 0.01-0.05 and 0.02-0.06 - cm respectively (substrate No.7, 8 and 9 shown in table 2.3) for Gd_2O_3
- substrate temperature during deposition of 600°C for Tm_2O_3 and 650°C for Gd_2O_3
- RTA at 800°C in O_2 ambient for 5 min. for Tm_2O_3 and 2 min. for Gd_2O_3
- Ag top and bottom electrode evaporation

First of all, Si surface crystal structure before deposition was con¯rmed by using RHEED. Si(100), (110) and (111) substrates were heated at 850°C for 10-30 minutes prior deposition to obtain clean reconstructed surface by removering 0.5 nm-thick chemical oxide with some particles. It is called thermal °ash (TF), and TF Si substrate was used in this chapter. Figure 5.1.1 (a)(b)(c) shows RHEED patterns of Si substrates with 0.5 nm-thick chemical oxide, which were immediately loaded into the MBE chamber. Electron beam could path through the ultra-thin chemical oxide and each crystal pattern were obtained. After TF, the reconstructed surface patterns appeared as shown in Figure 5.1.1 (d)(e)(f). 2£1 Si(100) and 7£7 Si(111) were con¯rmed.

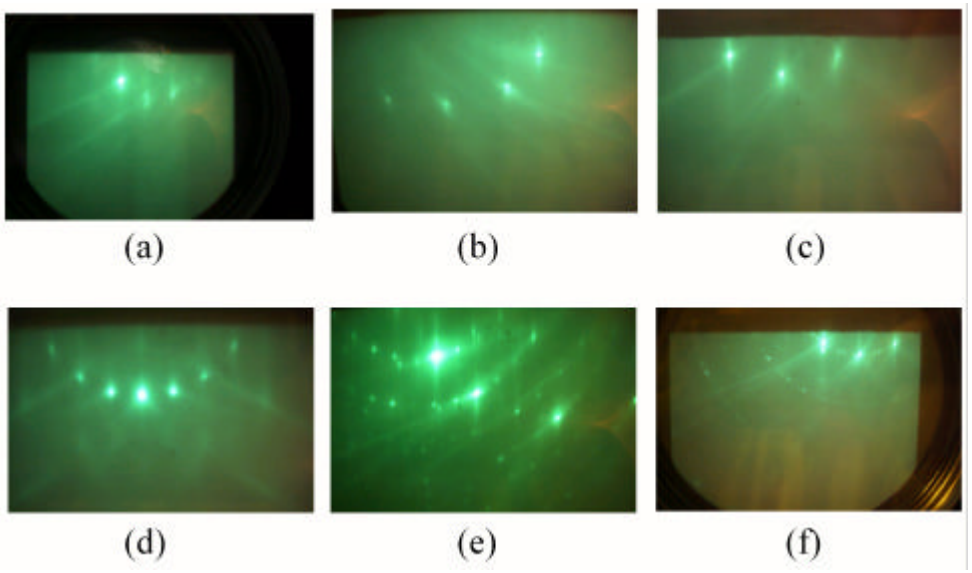

Figure 5.1.1: RHEED patterns of chemical oxidized (a) Si(100), (b) Si(110) and (c) Si(111) substrate, and reconstructed (d) Si(100), (e) Si(110) and (f) Si(111) substrate after TF.

5.2 Crystal structure and surface morphology on various oriented Si

To con¯rm the ¯lm crystallization, RHEED observation were done during deposition of Gd_2O_3 at 650°C. Figure 5.2.1 shows RHEED patterns of Gd_2O_3 on various oriented Si substrate. The ring pattern appeared at the screen, which showed poly-crystallized Gd_2O_3 on Si(100). For Gd_2O_3 on Si(110) and (111), no patterns at the beginning of the deposition, but streak pattern appeared after a while on only Si(111).

XRD patterns of as-deposited Gd_2O_3 on various oriented Si as shown in Figure 5.2.2 to determine the crystal structure and their orientation. There were only cubic (222) and (440) peaks in Gd_2O_3 on Si(100) although RHEED pattern of Gd_2O_3 on Si(111) was observed.

Figure 5.2.3 shows XRD patterns of Tm_2O_3 on various oriented Si. These Tm_2O_3 ¯lms were deposited at 600°C. XRD peak from Tm_2O_3 cubic (440) was obtained on Si(100), peaks from Tm_2O_3 cubic (211), (222) and (444) were obtained on Si(110) and peaks from cubic (222) and (444) were obtained on Si(111). Hexagonal (002) and cubic (222) peaks are very close, so pole scan was used to determined the crystal structure. These peaks show that 20 nm-thick Tm_2O_3 ¯lms deposited at 600°C were crystallized and their orientations were di®erent in Si substrate orientation. Next, the crystalline quality of Gd_2O_3 and Tm_2O_3 on Si(111) were examined by RBS measurements because

XRD peak intensity of Tm_2O_3 on Si(111) was largest of the three substrates and streak pattern of Gd_2O_3 on Si(111) was observed by RHEED. In fact, these ¯lms had aligned spectra by channeling measurements as shown in Figure 5.2.4. Channeling minimum yield $\hat{A}_{min}$ of 40 % for Tm_2O_3 and 76 % for Gd_2O_3 were obtained, which is de¯ned as the ratio of the aligned yield to the random yield. Although this value is no su±ciently low, it was ¯rstly reported epitaxial grown Tm_2O_3 on Si(111) for gate dielectric application.

Figure 5.2.5 shows AFM images of as-deposited Tm_2O_3 and Gd_2O_3 surface. Note that the physical thickness of Tm_2O_3 of nm and Gd_2O_3 of 10 nm were evaluated by ellipsometry, and the amount of Tm or Gd in the ¯lms were evaluated by RBS to con¯rm the no Si orientation dependence. The hillocks and holes were observed ant the Tm_2O_3 surface on Si(100), and Tm_2O_3 on Si(110) and (111) had deltaic hillocks, especially steps at the surface of Tm_2O_3 on Si(111) were shown. The di®erence of surface morphology was a®ected by the crystal structure di®erence, and this is the oriented Si dependence.

For Gd_2O_3 the morphology dependence was smaller than that for Tm_2O_3. RMS value of Gd_2O_3 on Si(100) was largest of the three, at the opposite tendency of Tm_2O_3 because Gd_2O_3 on Si(100) was poly-crystallized. And RMS values were much larger than that of Tm_2O_3, considering their physical thickness.

In summary the surface roughness were all larger than that of amorphous thin ¯lms. Electrical properties of these ¯lms will be discussed in next section.

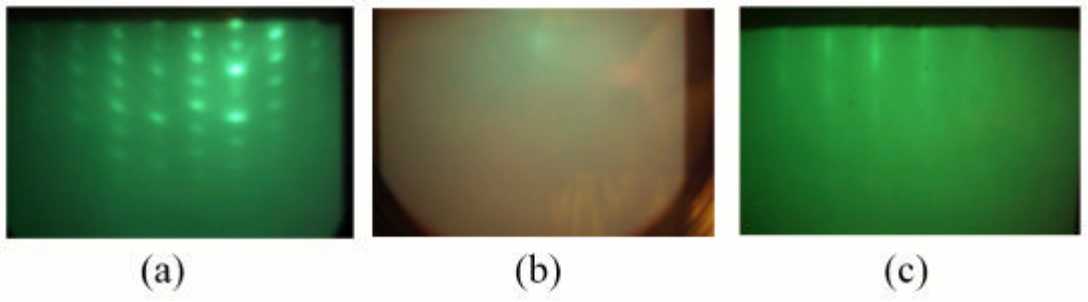

Figure 5.2.1: RHEED patterns of Gd_2O_3 on (a) Si(100), (b) Si(110) and (c) Si(111) during the deposition.

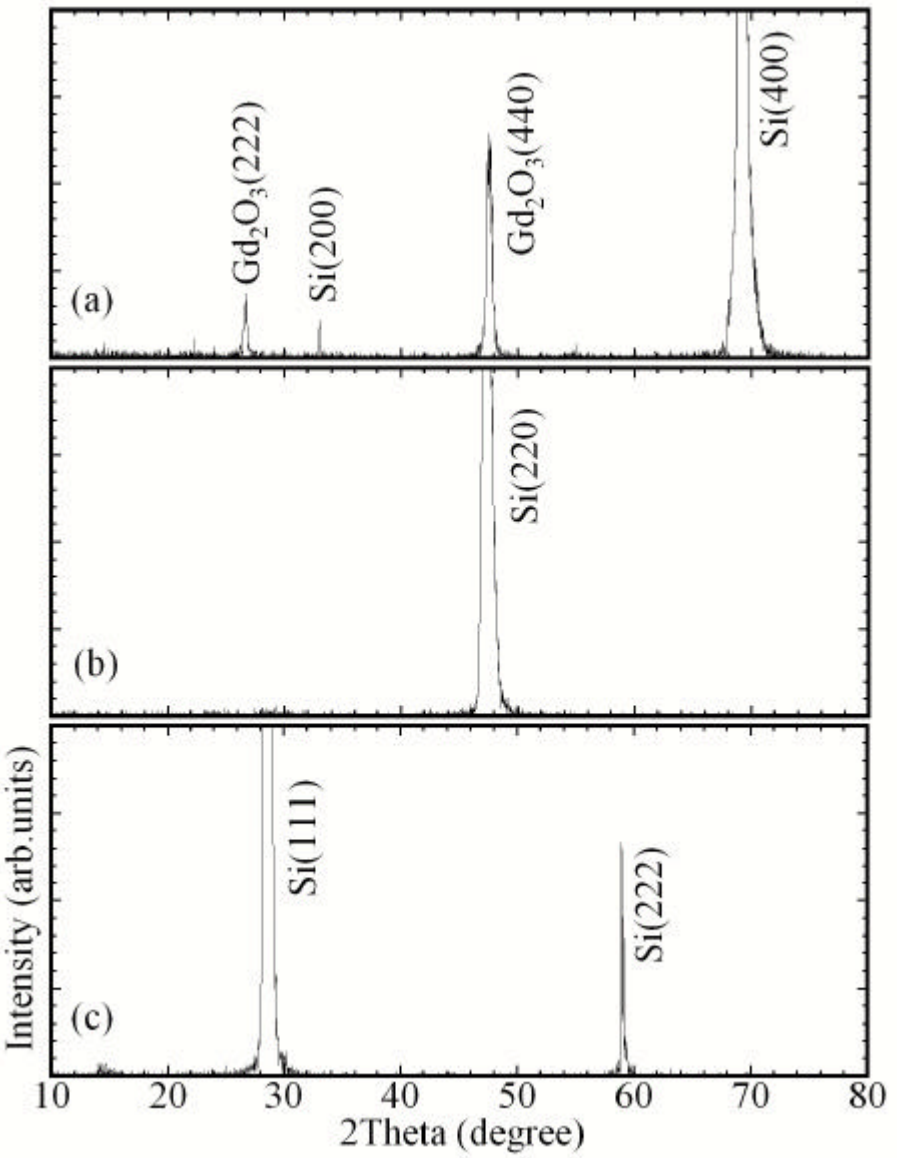

Figure 5.2.2: XRD patterns of 2µ ¡ µ scan Gd_2O_3 on (a) Si(100), (b) Si(110) and (c) Si(111).

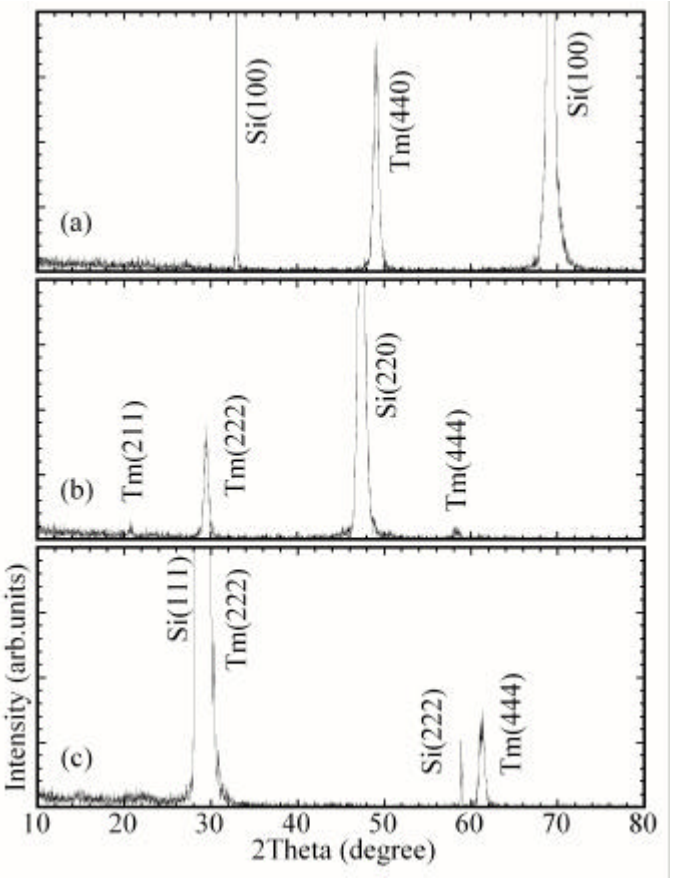

Figure 5.2.3: XRD patterns of 2μ ᵢ μ scan Tm_2O_3 on (a) Si(100), (b) Si(110) and (c) Si(111).

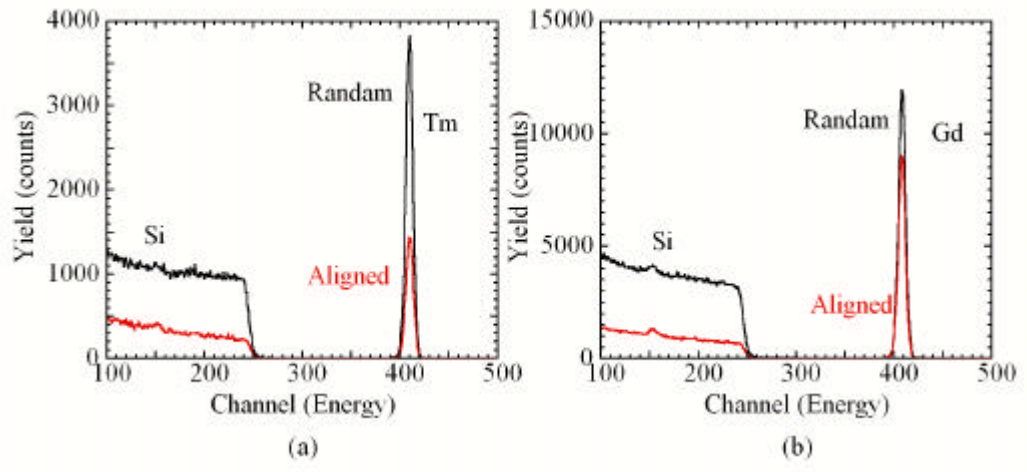

Figure 5.2.4: RBS spectra of as-deposited (a) Tm_2O_3 and (b) Gd_2O_3 on Si(100).

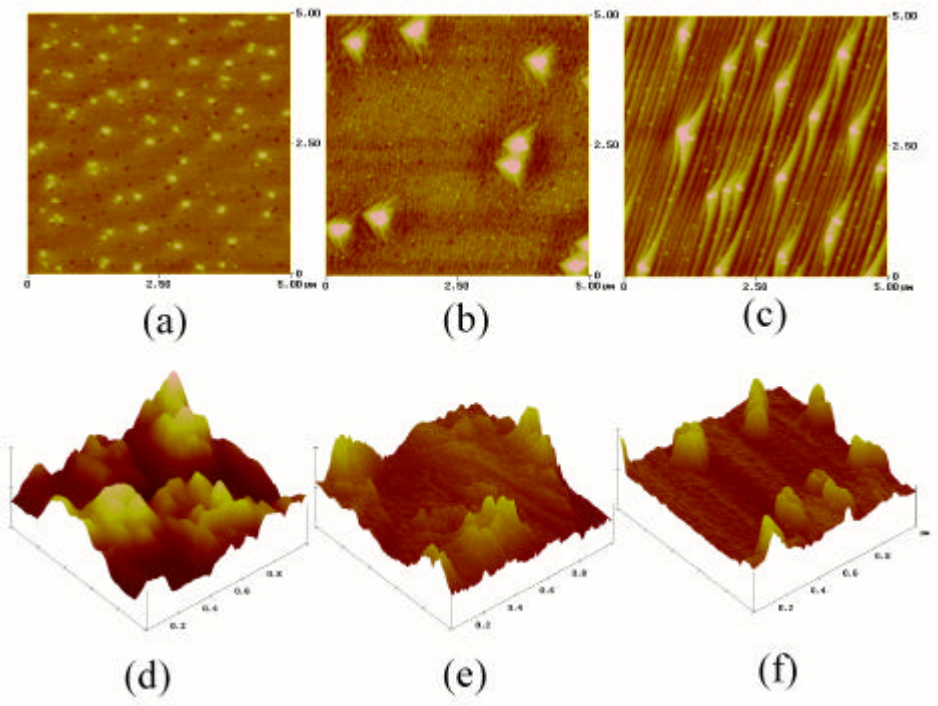

Figure 5.2.5: AFM images of as-deposited 25 nm-thick Tm_2O_3 (5 ¹m £ 5 ¹m, z:30 nm/div.). (a) on Si(100) (RMS:1.67 nm), (b) on Si(110) (RMS:3.38 nm) and (c) on Si(111) (RMS:3.78 nm). AFM images of as-deposited 10 nm-thick Gd_2O_3 (1 ¹m £ 1 ¹m, z:30 nm/div.). (a) on Si(100) (RMS:9.3 nm), (b) on Si(110) (RMS:6.5 nm) and (c) on Si(111) (RMS:6.0 nm).

5.3 Dependence of electrical properties on Si orientation

Figure 5.3.1 shows leakage current density of as-deposited 12 nm-thick Tm_2O_3 on TF Si(100) and (111). One was amorphouse ¯lm deposited at 250°C, and the other was crystalline deposited at 600°C. Figure 5.3.2 shows the dependence of leakage current density for as-deposited Gd_2O_3 on Si substrate orientation. The 3 nm-thick amorphouse Gd_2O_3 deposited at 250°C on HF-last Si, while the 10 nm-thick crystalline deposited at 650°C on TF Si. Leakage currents of crystallized ¯lms were signi¯cantly larger than that of amorphous ¯lms although the physical thickness of crystallized ¯lms were about three times larger than that of amorphous ¯lms. Moreover leakage currents of crystallized ¯lms had small dependence on Si orientation. In fact, there were not so much di®erences between single-crystallized, poly-crystallized and amorphous ¯lms in the data for Gd_2O_3. This result indicated that thicker ¯lms deposited at higher temperature had much leakage path in the ¯lms, such as surface roughness or some defects. Note that leakage currents of as-deposited amorphous ¯lms clearly depended on Si orientation of (100) < (110) < (111) resulted from Si surface bonds. These as-deposited crystallized ¯lms had to be annealed at higher temperature than that they were deposited at.

Figure 5.3.3 shows C-V and J-V characteristics for 25 nm-thick Tm_2O_3 after 800°C RTA in O_2 for 5 minutes. Large CET values showed thick interfacial layer and Si orientation dependence were seen. And it was clearly shown that ¢V_{FB} dependence on Si orientation. After 800°C RTA leakage currents were signi¯cantly decreased. The hard breakdown or something destructive points were observed and this voltage were not the same. This di®erence showed the dependence of ¯lm properties on Si orientation, this is the dependence of leakage mechanism.

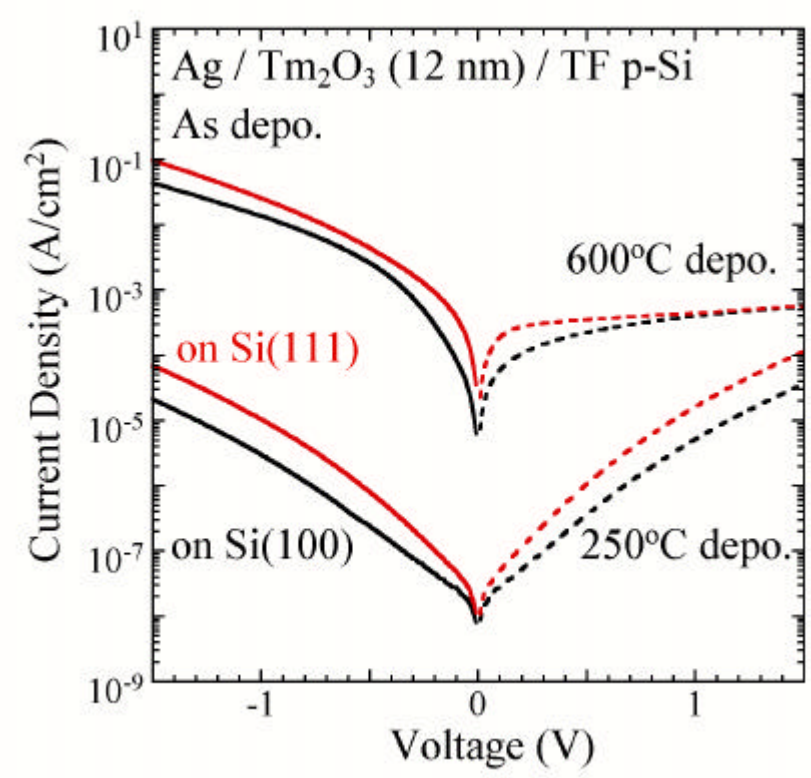

Figure 5.3.1: J-V characteristics for 12 nm-thick Tm_2O_3 on TF Si(100) and (111) deposited at 250°C or 600°C.

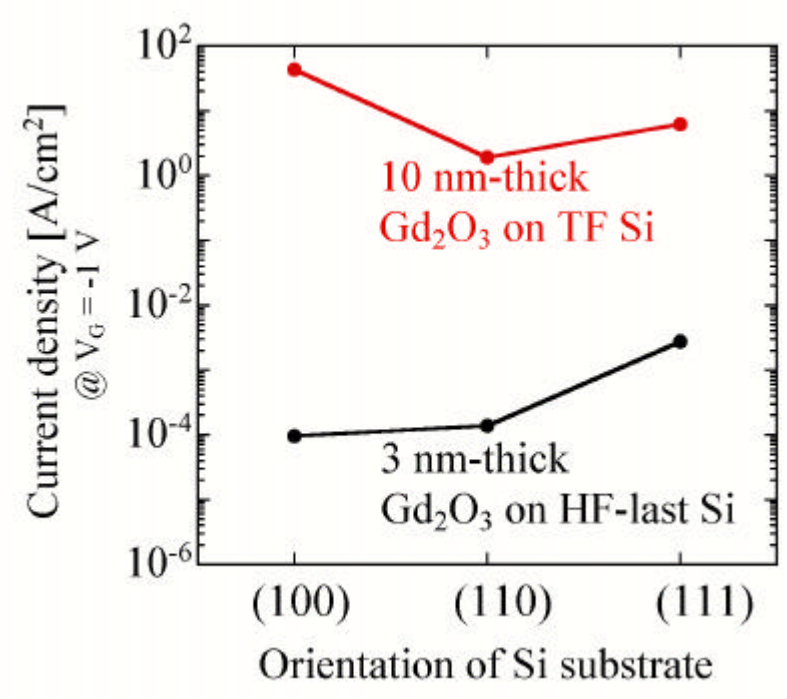

Figure 5.3.2: Dependence on Si orientation of 10 nm-thick crystalline and 3 nm-thick amorphous Gd_2O_3 leakage currents.

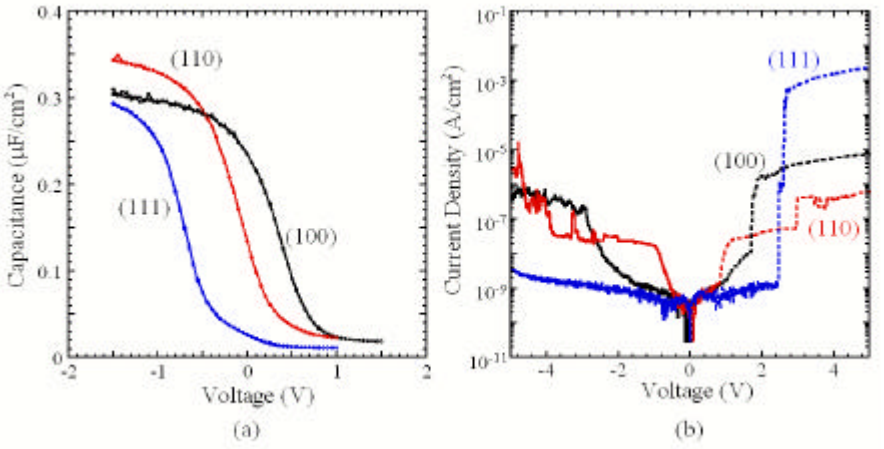

Figure 5.3.3: (a) C-V and (b) J-V characteristics for 25 nm-thick crystallized Tm_2O_3 after 800°C RTA.

5.4 Discussion about the Si amount in ¯lms

As discussed in previous section, huge leakage currents were observed for as-deposited Tm_2O_3 and Gd_2O_3 ¯lms. In C-V characteristics there were so large hysteresis and frequency dependence were shown that some parameters such as dielectric constant or ¢V_{FB} were not obtained. To study their ¯lm properties XPS and SIMS measurements were done, focusing the Si amount in the ¯lms. Figure 5.4.1 shows XPS Si2s and O1s spectra for (a) 12 nm-thick as-deposited Tm_2O_3 deposited at 250°C, (b) 25 nm-thick as-deposited Tm_2O_3 deposited at 600°C and (c) 25 nm-thick Tm_2O_3 deposited at 600°C after 800°C RTA. These ¯lms were all deposited on Si(100). The peak which showed Si-Tm-O binding between Si-Si and Si-O binding. The intensity of this peak, which seemed to show the amount of Tm-silicate, have to be discussed considering the O1s spectra because these data contained some measuring e®ects and the absolute values can not be used. Tm-silicate peak was observed for (b) while (a) had no peak. The intensity for the peak of (c) was larger than that of (b).

Consequently these results indicated two facts. First 600°C deposition induced more Si into the ¯lm surface and Tm-silicate exist than 250°C deposition. Secondly much more Si exist after 800°C RTA compared with the as-deposited ¯lms.

Figure 5.4.2 shows XPS Si2p and O1s spectra for 25 nm-thick as-deposited Tm_2O_3 deposited at 600°C on various oriented Si. Note that the spectra showed in Figure 5.4.1 (b) and that in Figure 5.4.2 (a) are same ¯lm. To correct the spectra with Tm-O peak, the amount of Tm-silicate at the surface was described this relation; on Si(100) = (100) > (111). In fact, Si penetrated easily into the poly-crystal ¯lms.

These tendency were demonstrated at the SIMS depth pro¯ling as shown in Figure 5.4.3. Si amount is as-deposited Tm_2O_3 depended on the deposition temperature, and higher temperature induced much Si into the ¯lms. Moreover Si amount depended on Si orientation, and poly-crystal ¯lm on Si(100) had much amount of Si compared with the epitaxial ¯lm on(111).

Next, Gd-silicate (Si amount in Gd_2O_3) were evaluated by the same measurements. Figure 5.4.4 shows SIMS depth pro¯ling for 10 nm-thick as-deposited Gd_2O_3 on Si(100) and (110), and Gd_2O_3 on Si(100) after 800°C RTA for 2 minutes. These ¯lms were deposited at 650°C simultaneously. The ¯lms had much more Si compared with the Tm_2O_3, and there was not so large di®erence between (100) and (110). However, after RTA Si amount increased dramatically and it was on the same order to Si substrate. It seemed to cause large leakage currents and small dielectric constant, and a lot of Si and hard mixing in Gd_2O_3/Si interface explained the di±culty in epitaxial growth. It

seemed that crystal Gd_2O_3 on Si(100) certainly had same orientation of Si(111) but the amorphous interfacial layer existed, reducing the channeling $\hat{A}_{min}$ in RBS spectra and showing no pattern in RHEED observation at the beginning of the deposition.

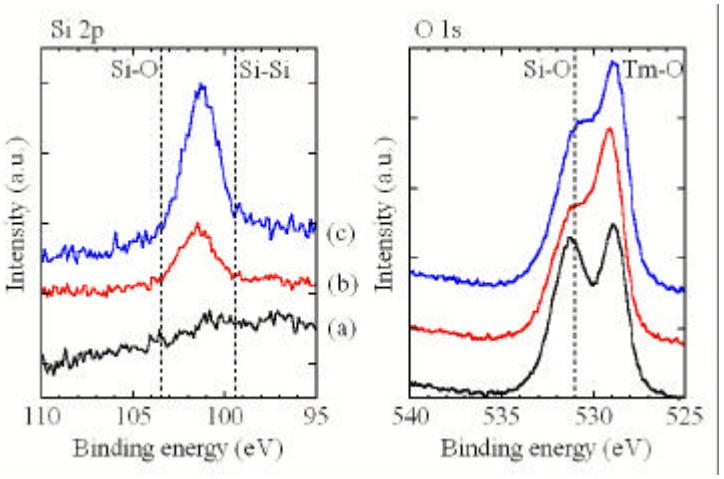

Figure 5.4.1: XPS Si2p and O1s spectra for (a) as-deposited Tm_2O_3 deposited at 250°C, (b) as-deposited Tm_2O_3 (25 nm) deposited at 600°C and (c) as-deposited Tm_2O_3 (12 nm) deposited at 250°C.

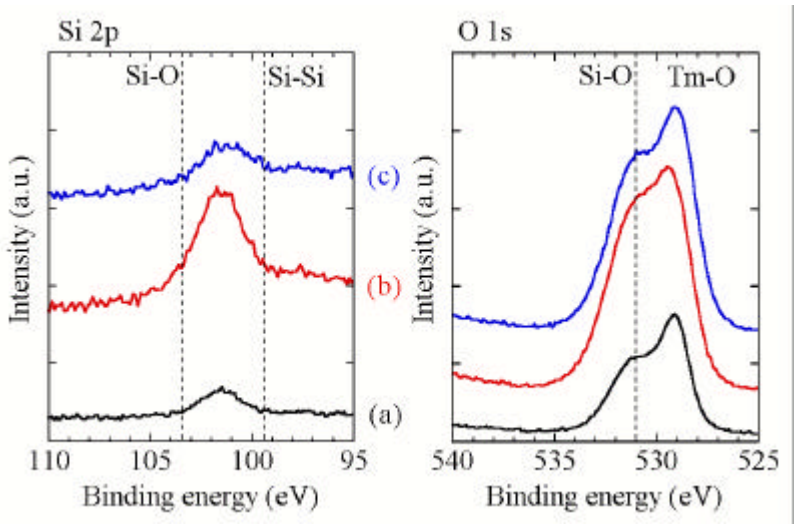

Figure 5.4.2: XPS Si2p and O1s spectra for as-deposited Tm_2O_3 deposited at 600°C on (a) Si(100), (b) (110) and (c) (111).

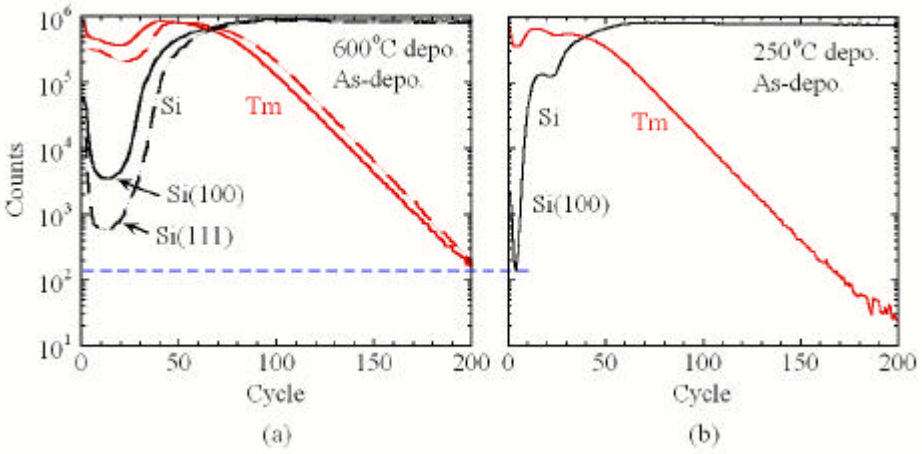

Figure 5.4.3: SIMS depth pro¯le for (a) as-deposited Tm_2O_3 (25 nm) deposited at 600°C on Si(100) and Si(111), and (b) as-deposited Tm_2O_3 (12 nm) deposited at 250°C on Si(100).

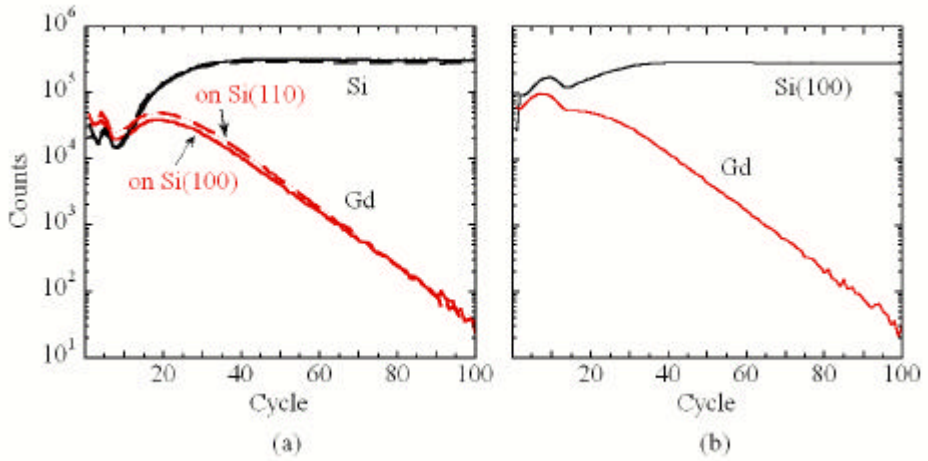

Figure 5.4.4: SIMS depth pro¯le for (a) as-deposited Gd_2O_3 (10 nm) deposited at 650°C on Si(100) and Si(110), and (b) Gd_2O_3 (10 nm) deposited at 650°C on Si(100) after 800°C RTA.

5.5 Temperature dependence of electrical properties

C-V and J-V measurements were done at several temperature of 20, 80 and 140°C to investigate the dependence on temperature and the di®erence of Si orientation. Figure 5.5.1 shows the leakage current density at -1 V of Gd_2O_3 as a function of temperature and Si orientation. These 10 nm-thick ¯lms were simultaneously deposited at 650°C and annealed at 800°C for 2 minutes. The leakage currents of Gd_2O_3 on Si(100) and (111) increased dramatically with increasing measured temperature although that on Si(100) and (110) were almost the same at 20°C. If the leakage mechanism at higher temperature was controlled by PF emission, the slope of the line between 140°C to 80°C indicates the dielectric constant, which means the probability for charge capture and reemission. This slope on Si(100) and (111) were almost the same, while the values of leakage currents were di®erent. The slope and absolute values were small, however, the theoretical explanations weren't done now.

Figure 5.5.2 shows C-V characteristics at each temperature. The accumulation capacitance in C-V curve on Si(100) increased with measured temperature and V_{FB} shifted to positive direction. The capacitance increasing in C-V curve on Si(110) was small, but the same curve couldn't be observed after high temperature measurements. The C-V curve shifted to negative direction. The accumulation capacitance in C-V curve on Si(111) increased and decreased irregularly and curve inversed at 80°C. Reproducible results were hardly obtained especially in C-V curve on Si(111).

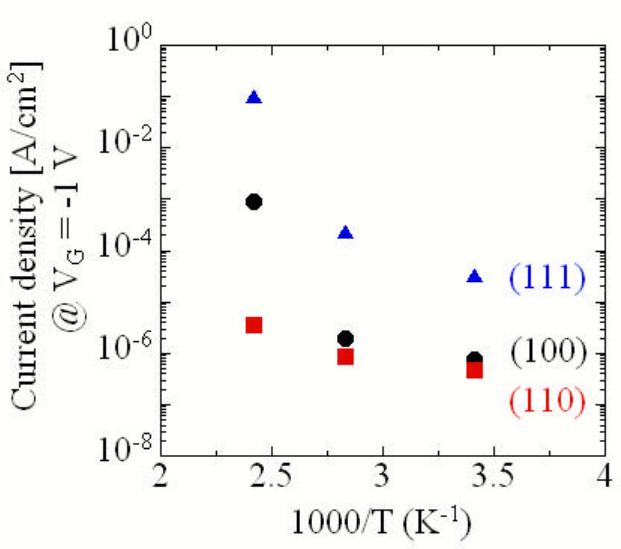

Figure 5.5.1: Temperature properties of leakage currents as a function of Si orientation.

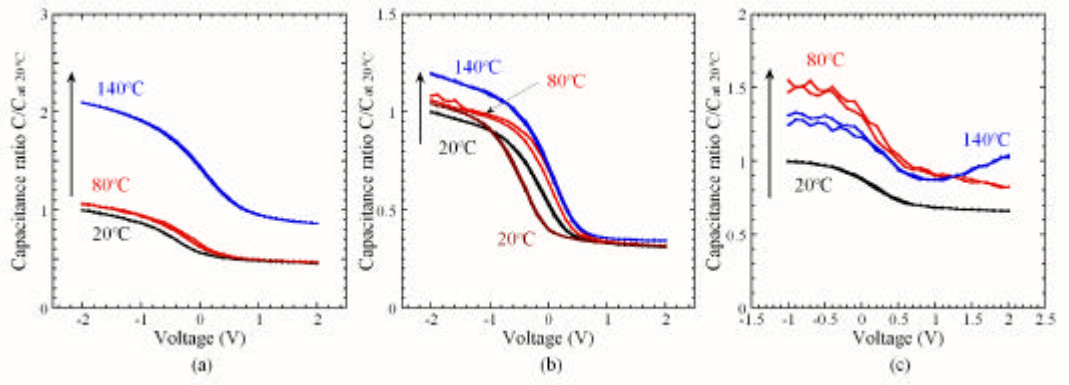

Figure 5.5.2: Temperature properties of C-V characteristics as a function of Si orientation.

5.6 Summary of this chapter

Tm_2O_3 and Gd_2O_3 were deposited at 600 or 650ºC on p-type Si(100), (110) and (111) to obtained epitaxial ¯lms. Tm_2O_3 was poly-crystallized on (100) and (110), and epitaxial ¯lm was obtained on (111) substrate. Gd_2O_3 was poly-crystallized on (100) and amorphous on (110), and epitaxial ¯lm was also obtained on (111) substrate. $\hat{A}_{min}$ of 40 % for Tm_2O_3 and 76 % for Gd_2O_3 on Si(111) were obtained. The surface of these ¯lms were very rough, especially Gd_2O_3. A lot of Si penetrated into the ¯lm, and Si amount dependence on Si orientation was con¯rmed. Leakage currents were signi¯cantly large compared with amorphous ¯lms. The dependence of C-V and J-V temperature properties on Si orientation was demonstrated.

Chapter 6

Conclusion

6.1 Results of this study

For application of high-k gate dielectrics, taking the place of SiO_2, the electrical properties of Yb_2O_3, Tm_2O_3 and Gd_2O_3 thin films, whose physical thickness were less than 25 nm were investigated. Dielectric constants of amorphous Yb_2O_3, Tm_2O_3 and Gd_2O_3 were calculated to be 15, 14 and 13, respectively, which were deposited on HF-last Si(100) by MBE. This is the first report about Tm_2O_3 for gate dielectrics. It was found that RTA improved ΔV_{FB} and D_{it} in electrical properties of MIS capacitor using Yb_2O_3 on Si(100), while CET increased with increasing RTA temperature. Leakage current densities were largely decreased because of Yb-silicate, which grew at the interface suppressed effectively. It is also demonstrated that 0.5 nm-thick chemical oxide on Si suppressed leakage currents dramatically although C-V curves using Gd_2O_3 on HF-last and chemically oxidized Si were completely the same.

Electrical characteristics of amorphous Tm_2O_3 and Gd_2O_3 on p-type Si(100), (110) and (111) were studied. It was confirmed that interfacial layer formations on HF-last Si(100), (110) and (111) were different although the Tm or Gd amount deposited on various oriented Si were almost the same. Leakage currents depended on CET and interfacial layer composition and/or thickness decided the currents. The orientation dependence of ΔV_{FB} and D_{it} of Gd_2O_3 were similar to those of SiO_2, and Si(100) had the best characteristics among them. This dependence was also observed using chemically oxidized Si although CET dependence was disappeared. For Tm_2O_3, the dependence was small compared with the Gd_2O_3 case.

Tm_2O_3 and Gd_2O_3 were deposited at 600 or 650°C on p-type Si(100), (110) and (111) to obtain epitaxial films. Tm_2O_3 was poly-crystallized on (100) and (110), and epitaxial film was obtained on (111) substrate. Gd_2O_3 was poly-crystallized on (100), amorphous on (110) and epitaxial film was also obtained on (111) substrate. $\AA_{min}$ of 40

% for cubic(111) Tm_2O_3 and 76 % for Gd_2O_3 on Si(111) were obtained. The surface of these ¯lms were very rough, especially Gd_2O_3. A lot of Si penetrated into the ¯lm, and Si amount in Tm_2O_3 dependence on Si orientation ((100) > (111)) was con¯rmed. And Si amount in Gd_2O_3 was larger than that in Tm_2O_3, and it seemd one reason why epitaxial Gd_2O_3 crystallinity was poor compared with Tm. Leakage currents were signi¯cantly large compared with amorphous ¯lms. The dependence of C-V and J-V temperature properties on Si orientation was demonstrated. It was found that the leakage currents of crystallized Gd_2O_3 increased with increasing temperature, although the ¯lm reliability was not enough to discuss its temperature dependence.

6.2 Future study

Deposition and/or RTA conditions have to be optimized to obtain epitaxial ¯rms at ¯rst. The survey for other rare earth oxides of electrical properties on various oriented Si substrate orientation to con¯rm the Si orientation dependence and to ¯nd easy-crystallized materials . However, much Si penetration in rare earth oxides may prevent from the formation of good epitaxial ¯lms. So epitaxial silicate ¯lms are also promissing candidates for gate dielectrics because silicate formation can not be prevented. In conclusion, it has to be develop how to realize smooth surface and small leakage currents.

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