3D Source/Drain Doping Optimization in Multi-Channel MOSFET

K. Tachi[1, 3, 4], N. Vulliet[2], S. Barraud[1], B. Guillaumot[2], V. Maffini-Alvaro[1], C. Vizioz[1], C. Arvet[2], Y. Campidelli[2], P. Gautier[1], J.M. Hartmann[1], T. Skotnicki[2], S. Cristoloveanu[3], H. Iwai [4], O. Faynot[1] and T. Ernst[1]

[1]CEA-LETI, Minatec, 17 rue des Martyrs, 38054 Grenoble, France,
[2]STMicroelectronics, 850 rue J. Monnet, 38926 Crolles, France,
[3]IMEP-LAHC, INPG-MINATEC, 3 Parvis Louis Neel, 38016 Grenoble Cedex 1, France,
[4]Frontier Research Center, Tokyo Institute of Technology, 4259, Nagatsuta, Midori-ku, Yokohama, 226-8502, Japan
Phone: +33 4 38 78 01 39, Fax: +33 4 38 78 30 34, e-mail: kiichi.tachi@cea.fr or thomas.ernst@cea.fr

***Abstract*—We demonstrate that the integration of in-situ doped Si Source and Drain (S/D) in three-dimensional Multi-Channel Field-Effect Transistors (MCFETs) leads to improved electrical performances. The combination of in-situ doped Selective Epitaxial Growth (SEG) and ion implantation indeed enables to drastically reduce the S/D resistance (down to 72 Ω.µm for nFET and 227 Ω.µm for pFET). Ion implantation induces a small mobility degradation, which becomes negligible in short gate length (L_G) MCFETs. Gate width down-scaling otherwise needed to suppress the overall mobility degradation with L_G and obtain the best electrical properties.**

I. Introduction

The performances of silicon-based large-scale-integrated circuits (LSIs) have improved dramatically in the past 40 years. Those improvements were based on the down-scaling of individual Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). However, the scaling of the planar bulk MOSFETs gate length reduction becomes more and more problematic due to the degraded gate electrostatic control of the channel potential leading to short-channel effects (SCEs) — threshold voltage roll-off, drain-induced barrier lowering (DIBL), subthreshold slope (SS) degradation, etc. Multi-gate devices are nowadays considered as the most promising solutions to minimize SCEs [1]. Vertically-stacked Multi-Channel FETs and 3D-stacked nanowire FETs, because of their reduced footprint, benefit from superior ON current performances [2-6]. Gate-source/drain (S/D) capacitances $C_{GS/GD}$ and S/D resistance R_{SD} have however to be further minimized in order to boost performance and reduce the intrinsic delay in such devices [5,6]. The recent introduction of internal spacers in MCFETs led to 39 % decrease of the intrinsic CV/I delay [4]. In this work, we have used in-situ doped Selective Epitaxial Growth (SEG) in order to fabricate the MCFET S/Ds. A homogenous and efficient S/D doping was thus achieved, resulting in higher electrical performance.

II. MCFET Structure

A cross-sectional TEM image of the fabricated five-channel MCFET structure on a SOI substrate is shown in Fig.1. This structure is composed of two double-gate (DG) transistors (channels 1&2 and 3&4) and a bottom single-gate transistor on SOI (channel 5). The self-aligned gates completely surround channels 1 to 4, with consequently a better electrostatic control. The SiN internal spacers with "Elevated flat-shaped" Si S/D are located on both sides. HfO_2/TiN/Poly-Si was used as the gate stack. The resulting equivalent oxide thickness EOT is ~2.5 nm. The fabrication process is similar to that reported in [4], except for the in-situ doped Si SEG S/D. In this study, we compare three types of samples with different S/D doping schemes in order to investigate their impact on S/D resistance as shown in Table 1. In sample A, S/D were ion-implanted after the intrinsic SEG step. In sample B, the S/D were in-situ doped during the SEG step. In sample C, we cumulated both of them (with the same conditions). Here, the gate length L_G is the average of channels 1 to 5 estimated from cross-sectional TEM images.

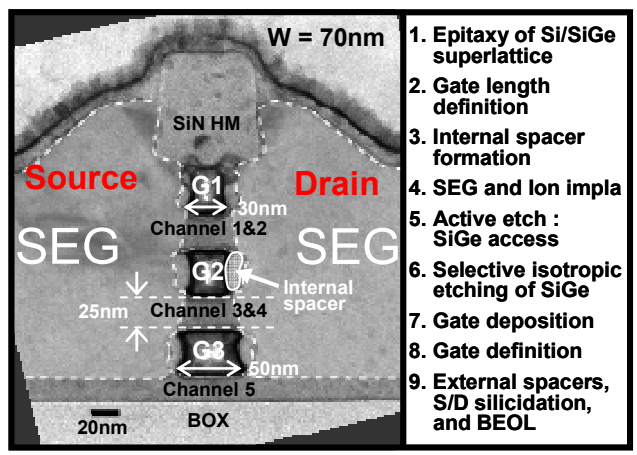

Figure 1. Cross-sectional Transmission Electron Microscopy image of a MCFET with internal spacers and 'flat' shaped S/D, and the process flow.

TABLE I. Source/Drain Doping Conditions

	Process A	*Process B*	*Process C*
Intrinsic Si SEG	✓		
In-situ doped Si SEG		✓	✓
Ion implantation	✓		✓

III. Electrical Results

First of all, we compare the impact of the S/D doping conditions on the transistors drive current. Fig. 2 shows the I_{ON}-I_{OFF} characteristics of the MCFETs with 70-nm-L_G. All the currents are normalized by the footprint of the channel width W. Changing the doping process from B to C improves the I_{ON} current by 72 % for nFET and 37 % for pFET at the same I_{OFF} of 10^{-8} A/µm. In order to precisely extract the device parameters and thus understand those improvements, we have used the Y-function-based technique [7-9]. The second order mobility attenuation factor Θ_2 (which is related to the surface roughness effect [10]) is notably taken into account with this method. Fig. 3 shows the I_D and g_m

comparisons between the measured data and the model. A good agreement is obtained.

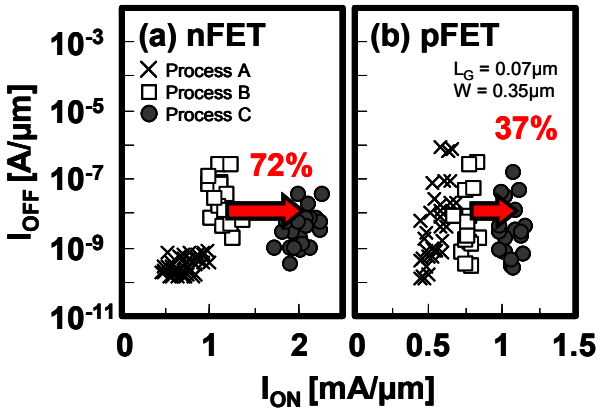

Figure 2. I_{ON}-I_{OFF} characteristics for n-FET (a) and p-FET (b). I_{ON} is the drain current at V_G-V_T = 0.9 V and -0.9 V, I_{OFF} is the off current at V_G-V_T = -0.3 V and 0.3 V for n- and p-FET, respectively. $|V_D|$ = 1.2 V.

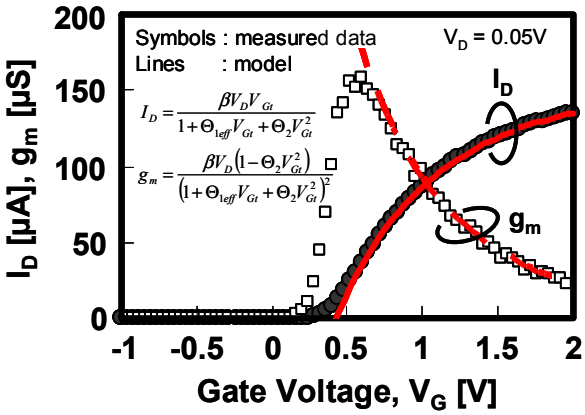

Figure 3. Comparison of I_D-V_G and g_m-V_G curves' fitting with the model shown in the figure. β is the current factor of the transistor ($\beta = \mu_0 W C_{ox}/L_{eff}$), V_{Gt} is the gate drive voltage ($V_{Gt} = V_G - V_T - V_{DS}/2$), and Θ_{1eff} and Θ_2 are the first- and second-order mobility attenuation factors, respectively. Θ_{1eff} represents the mobility limitation caused by phonon scattering and includes the R_{SD}: $\Theta_{1eff} = \Theta_1 + R_{SD}\beta$. The measured device is the C process nMCFET. Gate length and width are 70 nm and 350 nm, respectively.

A. *Source/Drain Resistance*

R_{SD} was extracted by plotting Θ_{1eff} versus β. Fig.4 shows the good linearity of the relationship between Θ_{1eff} and β for all gate lengths down to 70 nm. The resulting extracted values reveal that R_{SD} reduction was successfully reduced by combining in-situ doped SEG with ion implantation for both n and pFETs.

B. *Carriers Mobility*

The junction architecture may have a role in the mobility degradation when reducing the gate length due to the possible introduction of neutral defects by the S/D ion implantation [11, 12]. In the following, by comparing process B and process C MCFETs, we will quantify the ion implantation impact on the effective mobility. The latter was extracted versus the inversion charge density for electrons and holes by an improved split C-V method [13]. Indeed, for short-channel devices, extraction errors can be caused by the parasitic capacitances subtraction from the measured gate-to-channel capacitance (C_{GC}). The effective mobility (μ_{eff}) values extracted by this method were compared with the mobility calculated with the device parameters extracted in the former section, as shown in Fig. 5. It is shown that the μ_{eff} values, both with and without any R_{SD} correction, were well accounted for by the Y-function models.

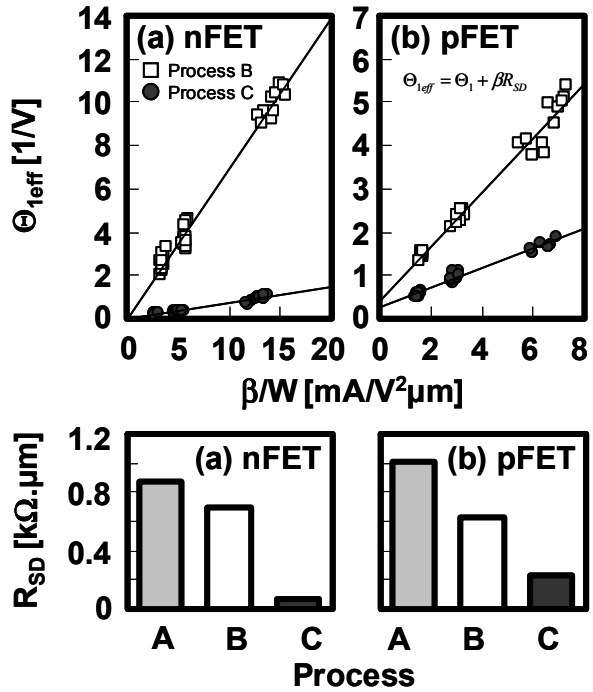

Figure 4. Extraction of R_{SD} from Θ_{1eff} – β plots and comparison of the resulting values for nFET(a) and pFET (b). The MCFETs with process C has a low R_{SD} value of 72Ω.µm and 227 Ω.µm for nFET and pFET, respectively.

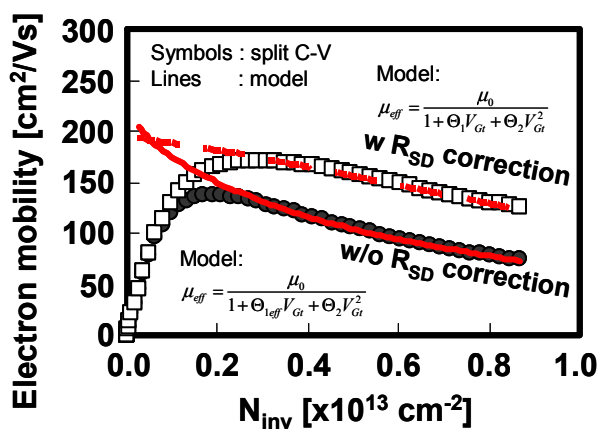

Figure 5. Effective mobility extraction with R_{SD} correction. The measured device is a 70-nm-L_G-nMCFET with process C. Gate length and width are 50 nm and 350 nm, respectively. R_{SD} are corrected by $I_{DS0}=I_{DS}/(1-I_{DS}R_{SD}/V_{DS})$

Fig. 6 compares process B with process C for a 70 nm L_G. For process C, μ_{eff} was slightly degraded for both electrons and holes. It may be due to the impact of ionized defects. It can be expected that such small mobility degradation does not significantly impact the I_{ON} current as compared to the benefit of R_{SD} reduction. However, it is important to know for the device scaling whether or not this mobility degradation depends on L_G. Thus, we plotted the low field mobility (μ_0) versus L_G (Fig. 7). For process B and C, μ_0 is degraded for both electrons and holes as L_G decreases. In order to analyze those behaviors, we used the L_G dependent mobility

degradation fitting model proposed by G. Bidal *et al.* [12]:

$$\frac{1}{\mu_0(L)} = \frac{1}{\mu_{max}} + \frac{\alpha_\mu}{L} \quad (1)$$

The two fitting parameters are the maximum mobility μ_{max} [$cm^2.V^{-1}.s^{-1}$], which is generally equal to the long channel mobility, and a mobility degradation factor α_μ [$V.s.cm^{-1}$]. First, the C_{GC}-V_G curves were compared for various L_G (Fig. 8). No differences were observed. This means that MCFETs with process C should have electrically the same effective gate length, equivalent gate oxide thickness, parasitic capacitance, and threshold voltage than the ones with process B. The ion implantation has however a large impact on the extracted μ_{max} values. The mobility for sample C is indeed degraded by ion implantation, this even in long channel FETs (as in [12]). On the other hand, α_μ values were similar. Such L_G dependent degradation might partially be attributed to ballistic transport [15].

IV. Gate Length Scaling

In the former section, we have discussed the R_{SD} reduction occurring when combining in-situ doped SEG with ion implantation and the mobility degradation dependence on L_G. In this section, we examine the global MCFETs down-scaling, including SCEs. The I_{OFF} behavior, when normalized by a common threshold voltage V_T, reflects the subthreshold properties such as DIBL and SS (not the V_T roll-off, however). Fig. 9 shows the I_{ON}-I_{OFF} characteristics of n- and p-MCFET with several L_G and W. The currents were normalized by the total channel surface W_{total} (W_{total} = W x 5ch. + T_{Si} x 6side-ch.). When reducing L_G down to 70 nm, I_{OFF} increases progressively due to the enhanced DIBL, while the SS value remains constant at ~70 mV/decade for nFET and ~75 mV/decade for pFET. MCFETs with L_G smaller than 70 nm have degraded subthreshold properties without the expected I_{ON} enhancement. This kind of degradation can be suppressed by adding the lateral gates electrostatic control through W down-scaling [14]. Drive current gains of 14 % for nFET and 20 % for pFET were observed when W was reduced from 350 nm down to 100 nm. We measured in the meantime an improved mobility μ_0 of 11 % and 18 % for nFET and pFET, respectively. This suggests that W down-scaling may reduce the L_G dependent mobility degradation. Additional investigation is needed in order to obtain a physical explanation of this phenomenon which is compatible with volume inversion.

Lastly, we present the scaled MCFETs characteristics with the process C. Fig. 10 shows I_D-V_G and I_D-V_D characteristics associated to 50-nm-L_G 80-nm-W nMCFET and 40-nm-L_G and 70-nm-W pMCFET. We obtained extremely high I_{ON}-currents of 4.1 mA/µm for nFET and a record 2.7 mA/µm for pFET at V_{DD} = 1.2 V. These values are obtained thanks to the 3D configuration of the vertically stacked channels and the enhanced impact of lateral conduction with small gate width. However, I_{OFF} is still high due to the non-optimized threshold voltage on those samples. When normalized at V_{OFF}+V_{DD}, the I_{ON}-currents are 3.3 mA/µm for nFET and 2.0 mA/µm for pFET. When normalized by W_{total}, the I_{ON}-currents at V_{OFF}+V_{DD} for n- and p-FET are 538 µA/µm and 396µA/µm, respectively. These normalized I_{ON} values are comparable to planar fully depleted – SOIFETs when using the same (unoptimized) gate stack [16].

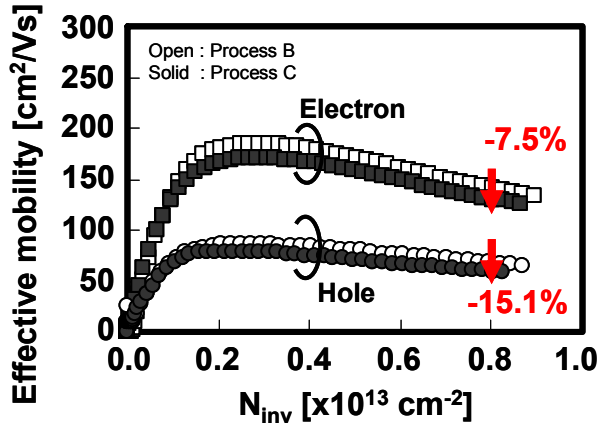

Figure 6. Effective mobility comparison between process B and process C. Gate length and width are 70 nm and 350 nm, respectively.

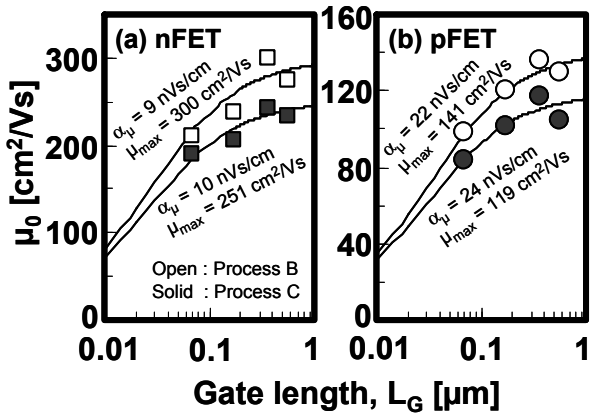

Figure 7. Low-field mobility μ_0 behavior as a function of the gate length. The lines result from L_G dependent mobility degradation modelling.

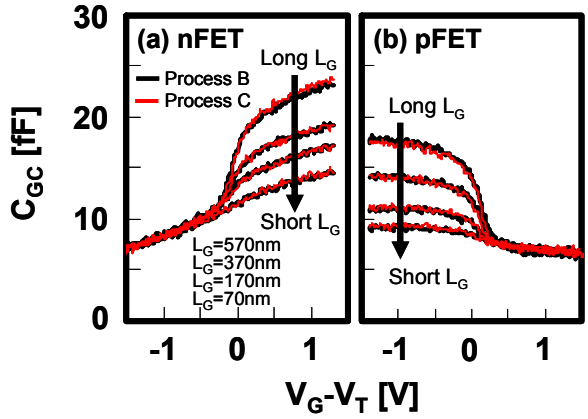

Figure 8. Gate-to-channel Capacitance C_{GC} as a function of V_G for several gate lengths.

V. Conclusion

We have successfully reduced the R_{SD} values for both n- and p-MCFETs by combining in-situ doped SEG and ion implantation. These reductions led to dramatic I_{ON} gains. Mobility was however degraded by S/D ion implantation. For short-channels MCFET, this mobility degradation was nevertheless negligible. The gate length scaling maximizes the drive current gains in MCFETs when compared to planar.

Gate width down-scaling enables to obtain the highest drive currents due to both the lateral conduction and the suppression of the L_G dependent mobility degradation.

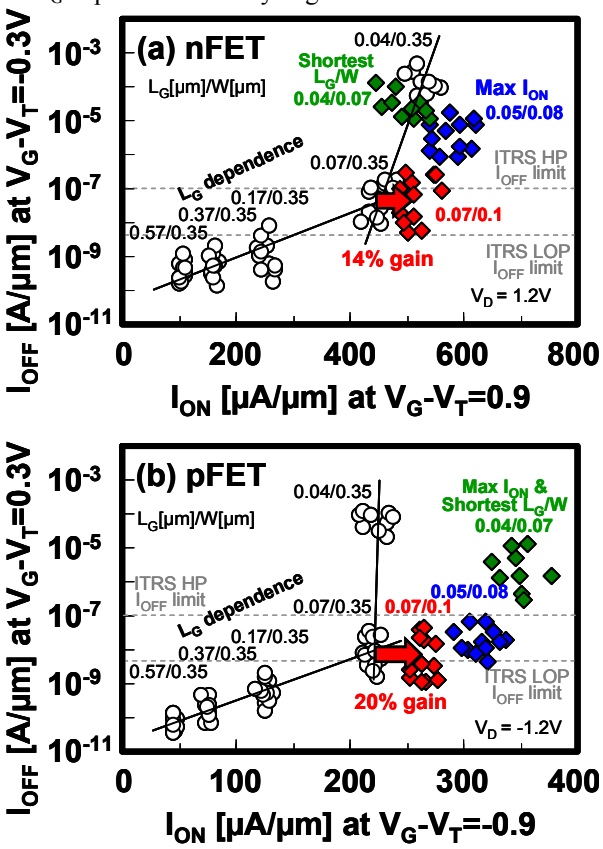

Figure 9. I_{ON}-I_{OFF} characteristics with several channel sizes for nMCFET (a) and pFET (b).

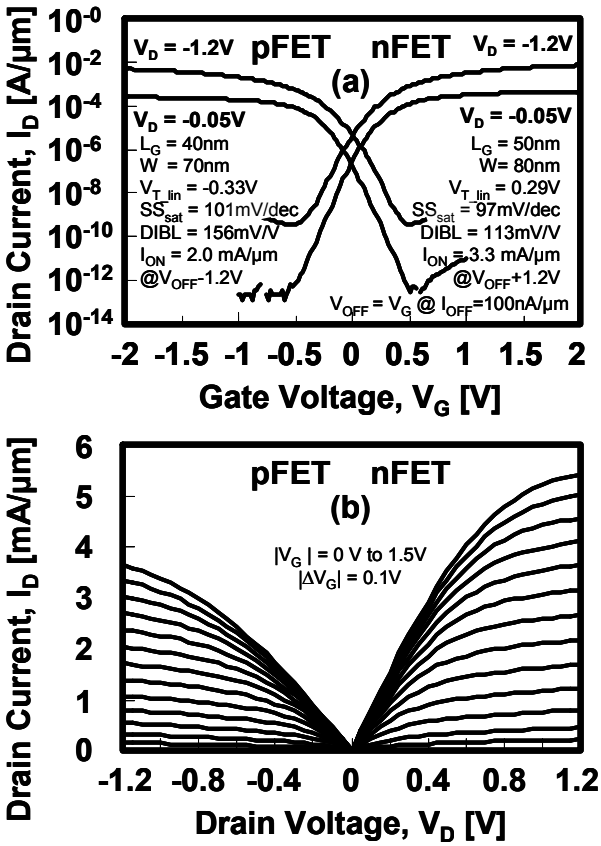

Figure 10. I_D-V_G (a) and I_D-V_D (b) characteristics for the scaled MCFETs.

ACKNOWLEDGMENT

This work was performed as part of the IBM-STMicroelectronics-CEA/LETI-MINATEC Development Alliance. Several authors acknowledge the support from Nanosil, Eurosoi and WCU projects.

REFERENCES

[1] J-T. Park and J-P Colinge, "Multiple-Gate SOI MOSFETs: Device Design Guidelines," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 2222–2229, Dec. 2002.

[2] C. Dupre *et al.*, "15nm-diameter 3D Stacked Nanowires with Independent Gates Operation: ΦFET," in *IEDM Tech Dig*. 2008, pp. 749-752.

[3] K. Tachi *et al.*, "Relationship between mobility and high-k interface properties in advanced Si and SiGe nanowires," in *IEDM Tech Dig*. 2009, pp. 313–316.

[4] E. Bernard *et al.*, "First Internal Spacers' Introduction in Record High I_{ON}/I_{OFF} TiN/HfO_2 Gate Multichannel MOSFET Satisfying Both High-Performance and Low Stanby Power Requirements," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 148–151, Feb. 2009.

[5] S-Y. Lee *et al.*, "Sub-25nm Single-Metal Gate CMOS Multi-Bridge-Channel MOSFET (MBCFET) for High Performance and Low Power Application," in *VLSI Symp. Tech. Dig.*, 2005, pp. 154–155.

[6] E. Bernard *et al.*, "Multi-Channel Field-Effect Transistor (MCFET) – Part II: Analysis of Gate Stack and Series Resistance Influence on the MCFET Performance," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1252–1261, June 2009.

[7] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters*, vol. 24, no. 9, pp. 543–545, 28th Apr 1988.

[8] B. Cretu *et al.*, "New ratio method for effective channel length and threshold voltage extraction in MOS transistors," *Electronics Letters*, vol. 37, no. 11, pp. 717–719, 24th May 2001.

[9] T. Tanaka, "Novel parameter extraction method for low field drain current of nano-scaled MOSFETs," in *Proc. IEEE Int. Conf. Microelectronic Test Structure (ICMTS'07)*, Tokyo, Japan, Mar. 2007, pp. 265–267.

[10] G. Reichert and T. Ouisse, "Relationship between empirical and theoretical mobility models in silicon inversion layers," *IEEE Trans. Electron Devices*, vol. 43, no. 9, pp. 1394–1398, Sep 1996.

[11] A. Cros *et al.*, "Unexpected mobility degradation for very short devices: A new challeng for CMOS scaling," in *IEDM Tech. Dig.*, 2006, pp. 663–666.

[12] G. Bidal *et al.*, "Guidelines for MOSFET Device Optimization acounting for L-dependent Mobility Degradation," in *IEEE 2009 Silicon Nanoelectronics Workshop*, Kyoto, Japan, June 2009, pp. 5–6

[13] K. Romanjek *et al.*, "Improved split C-V method for effective mobility extraction in sub-0.1 µm Si MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 583–585, Aug. 2004.

[14] E. Bernard *et al.*, "Novel integration process and performances analysis of Low STandby Power (LSTP) 3D multi-channel CMOSFET (MCFET) on SOI with metal / high-K gate stack," in *VLSI Symp. Tech. Dig.*, 2008, pp. 16-17, 17–19.

[15] K. Huet *et al.*, "Monte Carlo Study of Apparent Mobility Reduction in Nano-MOSFETs," in *ESSDERC proceedings*, 2007, pp. 382-385.

[16] F. Andrieu *et al.*, "Comparative scalability og PVD and CVD TiN on HfO_2 as a metal gate stack for FDSOI cMOSFET down to 25 nm gate length and width," in *IEDM Tech. Dig., 2006*, pp. 641–644.