Gate Semi-Around Si Nanowire FET Fabricated by Conventional CMOS Process with Very High Drivability

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***Abstract*— Gate semi-around silicon nanowire (SiNW) FETs have been fabricated and their electrical characteristics, especially on the drivability, have been assessed for future high performance devices. Among different wire size, a SiNW FET with a cross-section of 12×19 nm^2 has shown an improvement in the on-current (I_{ON}) when normalized by the channel peripheral length. A high I_{ON} over 1600 μA/μm at an overdrive voltage of 1 V has been achieved with a gate length and an oxide thickness of 65 and 3 nm, respectively. The origin of the high drivability has been speculated by higher carrier density, improved carrier mobility and the reduction in the series resistance.**

I. Introduction

Performance improvements by downsizing the CMOS technology have required new structures, including ultra-thin SOI and double-gate devices, to overcome the severe short channel effects (SCE), which induces an increase in off-state leakage current (I_{OFF}) to degrade the on-off ratio. Recently, silicon nanowire (SiNW) FETs have attracted much attention as they enable strong channel potential controllability by the gate electrode [1]. Beside, improvements in on-current (I_{ON}) with SiNW FETs have been reported, which are advantageous for high-speed with low power consumption application [2]. In this paper, gate semi-around SiNW FETs have been fabricated using conventional CMOS processes and their electrical characteristics, especially on the drivability, have been assessed for future high performance devices.

II. Device fabrication process

A (100)-oriented SOI wafer was used as a starting material with an SOI layer and a buried oxide thickness of 75 and 50 nm, respectively. SiNWs were formed by oxidation of fin patterns with a Si-nitride mask atop. Rectangular-like shape SiNWs with a wire height (h_{NW}) of 12 nm and wire widths (w_{NW}) of 19, 28 and 39 nm were fabricated. The Si-nitride mask suppresses the excess thinning of the embedded source and drain (S/D) pad regions to avoid any unexpected increase in the series resistance (R_{SD}). After striping the nitride and the formed oxides, a conventional self-aligned gate stack formation including gate oxidation and poly-Si deposition was conducted. The gate oxide thickness was set to 3 nm. Phosphorus ion implantations (boron for pFET) were chosen for extension formation with doses of 1×15 cm^{-2} at 15keV and 5×15 cm^{-2} at 5 keV for S/D region. After S/D activation annealing, a nickel self-aligned silicidation process was applied to reduce the R_{SD}. The key process is summarized in figure 1 and the detailed processes to fabricate semi gate-around SiNW FETs are shown in ref [3]. The SEM and TEM images of the fabricated SiNW FET are shown in figure 2.

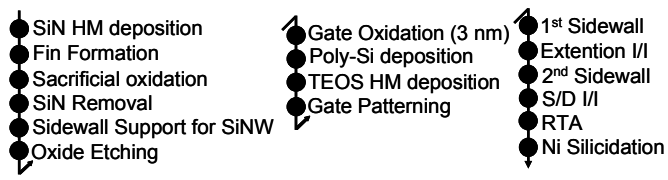

Figure 1. The key process flow for SiNW FETs using CMOS compatible process.

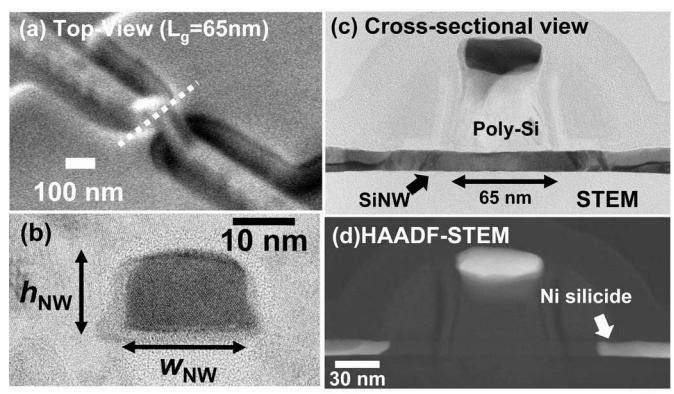

Figure 2. Typical SEM and TEM images of the fabricated SiNW FET.

III. Electrical Characteristics

The dc-characteristics (I_d-V_d and I_d-V_g curves) of the smallest (h_{NW} of 12 nm and w_{NW} of 19 nm) SiNW FETs with a gate length and gate oxide of 65 and 3 nm, respectively, are shown in figure 3. A well behaved transistor operation was confirmed for both *n*- and *p*-FET. The on-current of *n*-FET under an overdrive and a drain voltage of 1 V showed a large

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value of 60 μA, whereas that of p-FET was as low as 22 μA. The low on-current of pFET is mainly due to large R_{SD} and still needs process optimization. A fairly nice on-off current ratio of $>10^6$ with a DIBL and a favorable SS of 62 mV/V and 70 mV/dec., respectively have been obtained, owing to the large channel potential control of the gate electrode. The smaller w_{NW} was, the better SCE immunity represented by V_{th} roll-off and SS was obtained, which indicate the advantages of small cross section against the SCE, which is in good agreement with previous reports [4]. Moreover, SS of 62-63 mV/dec. with L_g over 150 nm was obtained which strongly suggests that the density of surface states (D_{it}) is negligible with a rectangular-like shape SiNW.

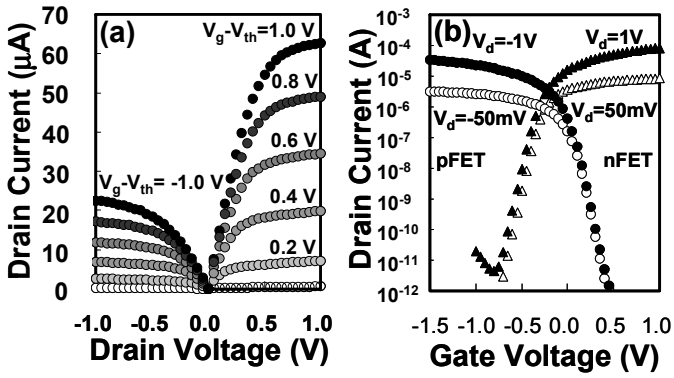

Figure 3. Dc characteristics of the fabricated gate semi-around SiNW FET (h_{NW}=12nm, w_{NW}=19nm) with L_g=65nm and T_{ox}=3nm.

The on-current per wire and on-current normalized by the channel peripheral width (I_{ON}) of the SiNW FETs with three different w_{NW} were plotted against the effective gate length (L_{eff}) in figure 4. A large on-current per wire can be obtained by wider SiNW mostly owing to the larger channel peripheral width. However, when normalized with channel peripheral length, the I_{ON} showed large improvements with smaller size. As the only difference among the three SiNW is the w_{NW}, one can speculate the effect of the rounded corner of the channel for I_{ON} improvement. Moreover, the I_{ON} showed an increasing trend with L_{eff} scaling, indicating further improvement in the drivability by L_g scaling.

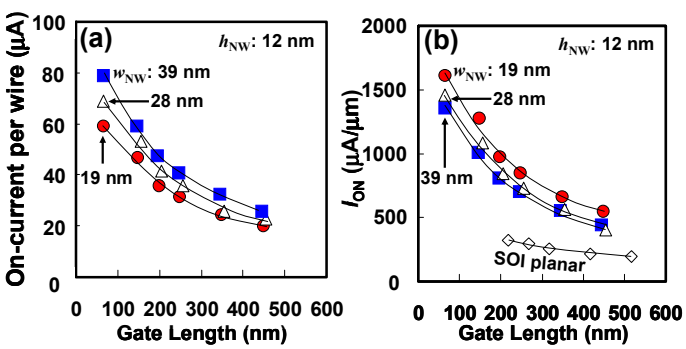

Figure 4. (a) On-current per wire and (b) I_{ON} normalized by peripheral channel width of three SiNW FET. The I_{ON} of planer SOI FETs fabricated on the same wafer are plotted as references.

To examine the drivability of SiNW FETs, planer SOI FETs with T_{Si} of 28 nm were fabricated simultaneously on the same wafer and are shown in the figure as references. One can observe improved I_{ON} by more than 2 times with SiNW FET, especially with the smallest cross-section.

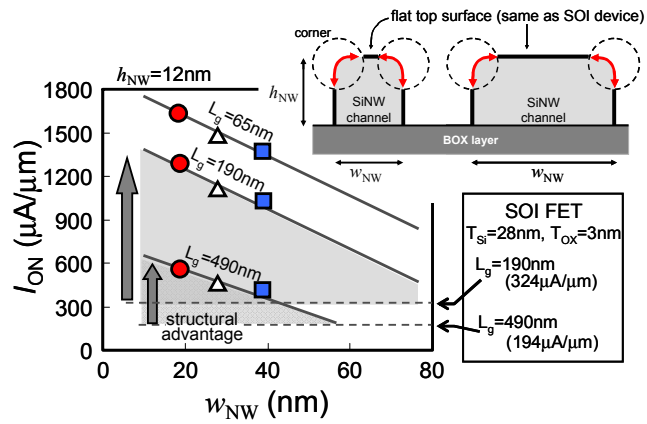

Figure 5. Structural advantage of SiNW FETs over SOI FETs with smaller w_{NW} for high drivability.

The effect of w_{NW} for SiNW FETs on the I_{ON} drivability is shown in figure 5. Compared to the planar SOI FETs with the same L_{eff}, a structural advantage of rectangular-like shape SiNW is more pronounced at smaller w_{NW}. Note that the existence of multiple V_{th} may be the concern with the rounded corners, however, no kink effect in the subthreshold characteristics was observed with our devices due to low-doped channel [5].

The I_{ON}-I_{OFF} characteristics measured from L_{eff} of 500 to 65 nm are shown in figure 6. Here the I_{OFF} is defined as the drain current normalized by the peripheral channel width at an overdrive voltage of -0.3 V and a drain voltage of 1 V. Although little difference is observed at large L_{eff} region, a distinct improvement on the on-off ratio is obtained with smaller cross-section when L_{eff} scaling is conducted. A large I_{ON} over 1600 μA/μm at an I_{OFF} of 1 nA/μm was achieved with a SiNW FET of 12×19 nm^2, L_{eff}=65 nm, and T_{ox}=3 nm.

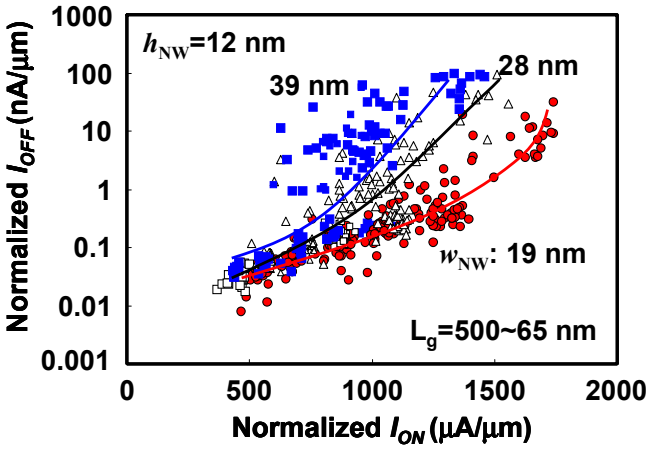

Figure 6. I_{ON}-I_{OFF} characteristics of SiNW with different w_{NW}.

To analyze the origin of the large drivability of I_{ON} with SiNW FETs, the effective electron mobility (μ_{eff}) were extracted by SiNW FETs with multi-wire channel (N=64) using advanced split-CV method, which are shown in figure 7. To avoid any unexpected parasitic effects for gate-to-channel capacitance measurements, an advanced split-CV method was adopted using two different FETs; gate mask length of 550 and 250 nm [6]. The inversion carrier density (N_s) was calculated using the sum of peripheral channel width of the SiNW obtained from TEM images. A large μ_{eff} peaking at 452 cm^2/Vs and 405 cm^2/Vs at N_s of 10^{13} cm^{-2} was extracted with a SiNW of 12×19 nm^2. Compared with the μ_{eff} of the planer SOI FET, a large improvement especially at high N_s can be obtained, presumably due to lower vertical electric field to the nanowire channel. The μ_{eff} showed little dependency on the w_{NW}, indicating small surface roughness at the top of SiNW. However, a large degradation in μ_{eff} was observed when a large h_{NW} was designed, especially at high N_s region where roughness scattering dominates. The reason might be the increase in the area of the etched side-surface to degrade the surface morphology so that process optimization including damage free plasma may improve the performance [7].

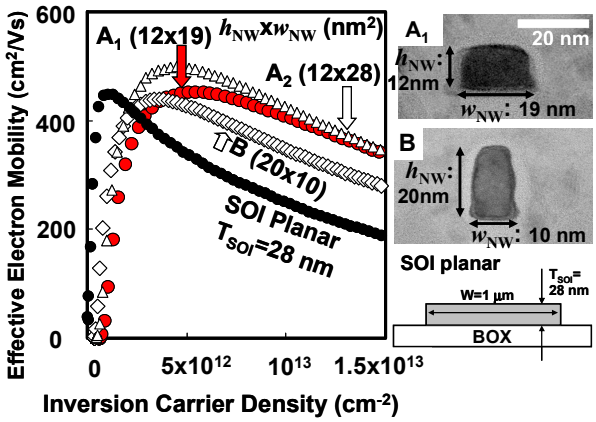

Figure 7. μ_{eff} of SiNW FETs obtained from advanced split-CV method.

The R_{SD} was extracted using the above devices based on Chern's method. A small R_{SD} of 1.5 kΩ was obtained irrespective of the w_{NW}. (fig. 8) This R_{SD} value corresponds to only 10% of the total channel resistance (R_{tot}) for L_{eff} of 65 nm, owing to the process optimization for S/D formation. Note that As implantation instead of P resulted in 10 times higher R_{SD}, presumable due to the damages in the S/D regions as well as the difference in the Ni silicide formation [8].

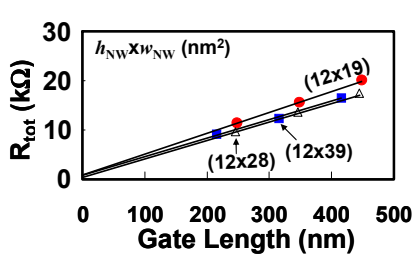

Figure 8. Extracted R_{SD} of the SiNW nFETs usning Chern's method.

Another reason to enhance the drivability of the SiNW FETs might be the distribution in the carrier concentration. Here, a two-dimensional simulation to extract the inversion carrier concentration distribution profile in the SiNW channel were carried out using a Taurus device simulator under modified local density approximation (MLDA) method [9]. The simulated device was designed to have the same cross sectional shape as was obtained experimentally. The work function of the metal electrode was set to 4.1 eV and a non-doped channel was assumed. Figure 9 shows the carrier concentration profile under a gate overdrive voltage of 1 V. High density regions can be observed near the corners of the channels, owing to the electrostatics at the rounded surface and one can see that large amount of carriers located within the SiNW away from the surface. As the w_{NW} decreases, the high-density regions at the corners approach, so that the portion of the high-density region within the cross section increases. Line profiles at the corner and at the top planer regions showed an increase in the carrier concentration by 2.5 times at the corner for both structures, indicating advantage for higher drivability at corners.

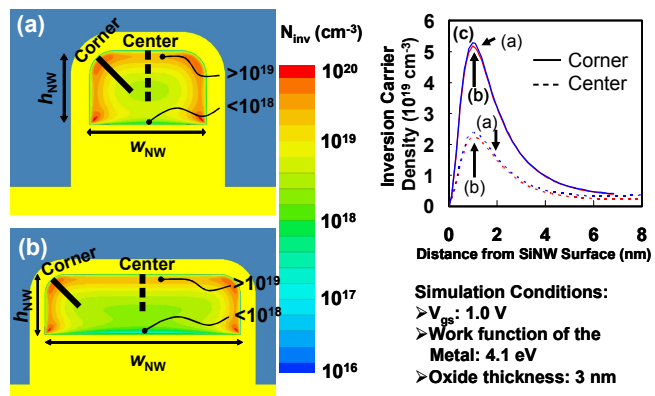

Figure 9. Two-dimensional simulation of the inversion carrier concentration within the SiNW chanels of (a) 12×19 nm^2 and (b) 12×38nm^2. (c) Line profile of the carrier concentration at the top planar and at the coner.

Based on the above characterizations, the improvement in the drivability from SOI to SiNW FET and further enhancement with smaller SiNW size could be speculated as attributions of the effect of corners in the cross section of the SiNW channel. As the NWs were fabricated by high temperature thermal oxidation, the corners of the NW have rounded shapes with a curvature radius of 4 nm. Given that the SiNW FETs were fabricated on the same wafer, the peripheral length of the corners can be considered as constant among three devices; only the proportion of the top flat and corner surface within the channel peripheral width changes. Assuming that the top flat surface region performs the same I_{ON} as the planer SOI device with an I_{ON} of 324 μA/μm for L_g=190 nm, the drivability of each corner can be extracted as shown in figure 5. The vertical etched surfaces of the channels at both sides are basically (110) surfaces, so that the μ_{eff} of the carriers at these surfaces may be degraded compared to the flat surface at the top [10]. However, the effect can be considered as a minor factor in this work as the h_{NW} is small compared to the w_{NW}.

TABLE I. BENCHMARK OF MULTI-GATE FETS REPORTED

	This work	Ref[11]	Ref[12]	Ref[13]	Ref[14]	Ref[15]	Ref[4]	Ref[16]	Ref[17]
NW Cross-sectional shape	Rectangular-like	Rectangular-like	Rectangular-like	Circular	Circular	Elliptical	Elliptical	Fin	Tri-Gate
NW Size (nm)	10×20	10×20	14	10	10	12	13×20		
L_g (nm)	65	25	100	30	8	65	35	25	40
EOT or T_{ox} (nm)	3	1.8	1.8	2	4	3	1.5		
V_d (V)	1.0	1.1	1.2	1.0	1.2	1.2	1.0	1	1.1
I_{ON}(uA) per wire	60.1	102	30.3	26.4	37.4	48.4	43.8		
I_{ON}(uA/um) by circumference	1609	2054	430	841	1191	1283	825	1296	1400
SS (mV/dec.)	70	79	68	71	75	~75	85	83	76
DIBL (mV/V)	62	56	15	13	22	40-82	65	83	89
I_{ON}/I_{OFF}	~1E6	>1E6	>1E5	~1E6	>1E7	>1E7	~2E5	~3E4	~1E4

By solving linear equations of the I_{ON} for the top-flat and corner parts with different SiNW-FETs, a corner with a curvature radius of 4 nm can exhibit a high I_{ON} of 3000 μA/μm can be calculated. On this account, one can calculate that the 80 % of I_{ON} is dominated at the rounded corner with the smallest device of h_{NW} and w_{NW} of 12 and 19 nm, respectively.

IV. DISCUSSION

Table 1 summarizes the benchmarking of the reported SiNW FETs. Although our device has relatively large L_g and T_{ox} among the SiNW FETs listed in the table, the 2nd-highest I_{ON} over 1600 μA/μm was demonstrated. One could expect further higher performances with the dimension scaling. For example, with decreasing both the gate length (65 to 32.5 nm) and gate oxide thickness (3 to 1.5 nm) I_{ON} over 3000 μA/μm by circumference could be expected. Among various cross sectional shape of SiNW shown in the table, including rectangle-like, elliptical and circular shapes, one can see a trend that a large I_{ON} normalized by channel peripheral width is achieved with rectangle-like shape, possibly the effect of rounded corners in the channel.

V. CONCLUSION

Very high on-current of gate semi-around SiNW FETs fabricated with conventional CMOS process have been demonstrated. A rectangular-like shape SiNW with a height and a width of 12 and 19 nm, respectively, has revealed a high on-current over 1600 μA/μm with a gate length and an oxide thickness of 65 and 3 nm, respectively. The origin of high drivability has been explained by fairly nice effective mobility, and low S/D parasitic resistance as well as the enhancement in the carrier concentration at the rounded surface of SiNW. There is a good possibility that the drivability over 3000 μA/μm by circumference could be obtained by future scaling of L_g and EOT even using convention CMOS process.

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