Relationship between mobility and high-*k* interface properties in advanced Si and SiGe nanowires

K. Tachi[1, 2, 4], M. Casse[1], D. Jang[2], C. Dupré[1], A. Hubert[1], N. Vulliet[3, 1], C. Maffini-Alvaro[1], C. Vizioz[1], C. Carabasse[1], V. Delaye[1], J. M. Hartmann[1], G. Ghibaudo[2], H. Iwai[4], S. Cristoloveanu[2], O. Faynot[1], and T. Ernst[1]

[1]CEA-LETI, MINATEC, 17 avenue des Martyrs 38054 Grenoble Cedex 9, France, [2]IMEP-LAHC, INPG-MINATEC, 3 Parvis Louis Neel, 38016 Grenoble Cedex 1, France, [3]STMicroelectronics, 850 rue J. Monnet, 38926 Crolles Cedex, France, [4]Frontier Research Center, Tokyo Institute of Technology, 4259, Nagatsuta, Midori-ku, Yokohama, 226-8502, Japan

Phone: +33 4 38 78 01 39, Fax: +33 4 38 78 30 34, e-mail: kiichi.tachi@cea.fr or thomas.ernst@cea.fr

Abstract:

For the first time, interface properties between high-*k* and Si or SiGe nanowires (NWs) have been experimentally investigated by adapting charge pumping technique and low-frequency noise measurement. It is found that the interface state density (D_{it}) of circular Si NWs is ~3 times higher than that of rectangular ones. Oxide trap density in SiGe NWs is ~3.5 times higher than that of Si NWs. The trap densities are well correlated to with the carrier mobility values.

Introduction:

Gate-All-Around (GAA) Silicon nanowire transistors (SNWTs) are promising candidates for future CMOS devices due to their reduced short-channel effects [1]. Recently, an overall mobility degradation has been evidenced for small NW diameters (<10nm) [2-3]. Random Telegraph Noise measurements were also performed on SNWTs [4]. Tensile-strained Si NWs and compressive-strained SiGe NWs for electron and hole mobility enhancement have been demonstrated [5-6]. Mobility lowering components - remote coulomb, surface roughness, and phonon scattering, for example – have, however, not experimentally been investigated in details. In particular, the possible degradation of the Si/gate oxide interface and its relationship with the NW shape was not studied.

In this paper, we experimentally investigate the mobility lowering components of Si and SiGe NWs as a function of their geometry. In particular, we discuss their interface quality based on the charge pumping method and low-frequency noise measurements.

Device fabrication:

3D-stacked Si NWTs (NMOS and PMOS) and SiGe NWTs (PMOS) with high-*k* /metal gate stacks (HK/MG) were fabricated. Fig.1 shows the process flow of 3D-stacked NWTs which was modified compared to previous work [7]. SOI (001) wafers were used for Si and compressively (c)-strained SiGe NWs. Tensile-strained SOI (001) wafer was for un-strained SiGe NWs, respectively. After anisotropic and isotropic etching of $Si/Si_{0.8}Ge_{0.2}$ superlattices [8], a 2 nm-thick-Si capping layer was grown at 650 °C on the liberated SiGe NWs to achieve higher mobility [9]. A HfO_2 (3 nm) / TiN (10 nm) / Poly-Si gate stack was deposited on NWs. The gate is overlapped on S/D areas which have SiN hard masks on top of the Si/SiGe superlattices. Fig.2 (a) shows cross sectional TEM images of 3D-stacked SNWTs with HK/MG. Circular cross-sectional shape NWs are successfully formed by H_2 annealing at 750°C for two minutes as shown in Fig.2 (c). We can also confirm that a lower-k SiO_2-like interfacial layer (T_{IL}: 1.5~2 nm) grows due to non-optimized thermal process [10]. The resulting EOT is 2.6 nm. The NW diameter is controllable down to 5 nm by self limited oxidation while keeping regularly arrayed NWs as shown in Figs. 2 (d), (e), and (f) [11]. Figs. 3 (a) and (b) shows cross sectional TEM images of 3D-stacked $Si_{0.8}Ge_{0.2}$ NWs with HK/MG. The cross-sectional shape was hexagonal with {111} facetted sidewalls most likely due to the thermal budget used during the Si capping. Long c-strained SiGe NWs are bended as shown in Figs. 3 (a) and (c), while short c-strained SiGe NWs and un-strained SiGe NWs are straight as shown in Figs. 3 (d) and (e). All measured NWs are [110]-oriented, 3 levels vertically-stacked, and horizontally arrayed with 50 parallel wires.

Silicon nanowires:

Figs.4 and 5 show I_D-V_D and I_D-V_G characteristics of 3D-stacked 5 nm diameter SNWTs with L_G=120 nm. The currents are normalized by the top view NW width (W_{NW}). I_D-V_G plot exhibits near-ideal subthreshold swing (SS=61 mV/dec for n-FET and SS=60 mV/dec for p-FET) and very low DIBL (7mV/V for both n- and p-FETs). The off-currents I_{OFF} are low with an I_{ON}/I_{OFF} ratio $>10^6$. On-currents I_{ON} at V_{DD}=1.2 V equal to 13.3 mA/μm and 7.5 mA/μm are obtained for n- and p-FETs, respectively. These extremely high values are due to the 3D configuration of 3 levels vertically-stacked NWs and to the normalization by W_{NW}. If I_{ON} is normalized by the number of wires, the I_{ON} values are 22.1 μA/wire for nFET and 11.5 μA/wire for pFET, respectively.

Effective mobility μ_{eff} of SNWTs is extracted thanks to the double L_m method, where two different gate lengths (250 nm and 600 nm) are designed to remove the effect of parasitic capacitance and resistance [12]. The electron mobility of 5 nm circular SNWTs is clearly degraded (Fig. 6). For rectangular SNWTs, the mobility is degraded as W_{NW} decreases. This is attributed to the lower electron mobility on (110) sidewalls. This, however, does not explain the very small mobility of 5 nm circular SNWTs. Fig. 7 shows a mobility comparison between rectangular and circular cross-section NWs with similar size (see Fig. 2 (b) and (c)). A circular shape leads to mobility degradation at low inversion charge density (N_{inv}). For both SNWTs, the mobility at high N_{inv} is degraded compared to our FD-SOI FET reference due to a higher surface roughness component [13]. Improvement of μ_{eff} at high N_{inv} is however observed for circular NWs because their surface roughness is reduced by the H_2 annealing. Fig. 8 (a) shows electron mobility at low and high N_{inv} as a function of W_{NW}. At low N_{inv}, the mobility of circular Si NWs is considerably lower than that of rectangular ones. The mobility degradation trend in Fig. 8 (b) is similar to already published SNWTs results [2-3].

Mobility lowering components at low inversion charge density N_{inv}:

Mobility at low N_{inv} is mainly limited by (remote) coulomb scattering due to interface and oxide charges and/or interface dipoles between high-*k* and interfacial layer in the case of HK/MG stack [14,15]. Figs. 9 and 10 show the linear V_{TH} of SNWTs as a function of W_{NW} and L_G, respectively. The V_{TH} of the 20nm circular SNWTs is negatively shifted (~ -100mV) compared to rectangular SNWTs for all gate lengths. This can, however, not be attributed to the increase of the curvature radius [16]. This V_{TH} shift could be related to the interface dipole modulation which may depend on the cross-sectional shape, and in turn causes the observed mobility degradation. Alternatively interface charges, enhanced in MG devices [15], lead also to V_{th} shift and mobility degradation at low N_{inv}. We have quantified the D_{it}, for the first time on NWs, by adapting the charge pumping method with gated-diode structures. A schematic view of the experimental set-up is shown in Fig.11. The cross-section image shows undoped Si NWs and n^+ and p^+ implanted regions. The NW gated-diode allows direct measurement of the D_{it} thanks to the p^+ region which acts as a 'substrate' contact [17]. Fig. 12 shows the charge pumping current (I_{cp}) in Si NWs which exhibits a typical "hat" shape. The peak I_{cp}-freqency (f) plots shows a good linearity in Figs. 13 and 14. Circular NWs have roughly 3 times higher mean D_{it} values than rectangular ones with no significant difference between narrow and wide Si NWs. Figs. 15 and 16 show the energy profiles of D_{it} (obtained by modifying the rise and fall times of the pulses). At both the upper and lower regions of the gap, the D_{it} of circular NWs is higher, leading to higher mean D_{it} values. Fig.16 summarizes the physics underlying the mobility limiting factors in SNWTs with HK/MG. The circular SNWTs have poor mobility at low N_{inv} due to higher D_{it} (likely caused by the continuously varying surface orientation) together with possible additional interface dipoles. H_2 annealing, however, reduces surface roughness and improves mobility at high N_{inv}. In addition, phonon-limited mobility may also be degraded for Si NWs with diameter less than 10 nm [18].

SiGe nanowires as PMOS-FETs boosters ?

C-strained SiGe and un-strained SiGe NWs were evaluated in order to boost pFET performances. Fig. 18 shows I_{ON}/I_{OFF} characteristics of Si, c-strained and un-strained SiGe NWs. The currents are normalized by the number of wires. The lower V_{th} measured on c-SiGe NWs (Fig. 19) provides a larger I_{ON} current than for Si NWs. However the best I_{ON}/I_{OFF} performance is obtained for Si NWs in agreement with μ_{eff} measurement (Fig. 20). Low-frequency noise measurements performed on the NWs, show an oxide trap density (N_t) for SiGe NWs 3.5 times larger than for Si NWs. (Fig. 21). This higher trap density is well correlated with the lower mobility observed. Additionally the hexagonal cross section of SiGe NWs with (111) sidewalls could also contribute to the mobility degradation.

Conclusion:

We have studied the relationship between NW cross-sectional shape, material (Si or SiGe) and D_{it}. Charge pumping shows that circular shape SNWTs have higher D_{it} than rectangular ones, leading to low-field mobility degradation. This high D_{it} might be caused by the continuously-varying surface orientation. This could explain the quite low mobility in 5nm diameter SNWTs: the surface orientation changes much more rapidly when the diameter of circular NWs decreases. The mobility of SiGe NWs is lower than that of Si NWs due to higher N_t and facetted (111) sidewalls.

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References:
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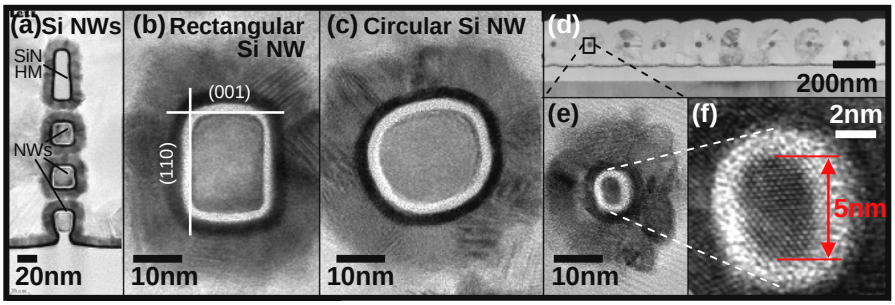

Figure 2: Cross-sectional TEM micrographs of 3D-stacked SNWTs with high-*k*/metal gate stacks; (a) 3D-stacked SNWTs, (b) enlarged image of a rectangular nanowire, (c) circular nanowire by H_2 annealing, (d) regularly arrayed 5nm-diameter SNWTs, (e) 5nm-diameter SNWT, and (f) enlarged image of 5nm-diameter SNWT. The crystalline quality of those circular SNWs is good, as shown by the high resolution TEM image in (f).

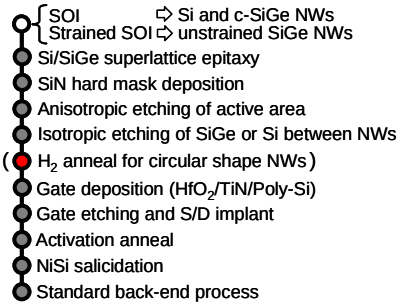

Figure 1: Process flow of 3D-stacked NWs. H_2 annealing is performed at 750°C. 3 nm-thick-HfO_2 layer is deposited on 0.8 nm-chemical oxide.

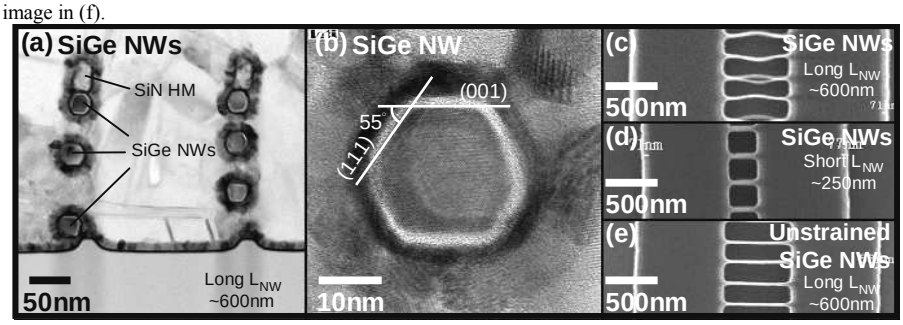

Figure 3: (a) Cross-sectional TEM micrographs of 3D-stacked SiGe NWTs with compressive stress, (b) enlarged images of c-strained SiGe NW, (c) top view of bended c-strained SiGe NWs with L_{NW}=600nm, (d) top view of c-strained SiGe NWs with L_{NW}=250nm, and (e) top view of un-strained SiGe NWs with L_{NW}=600nm. Short length SiGe NWs are straight.

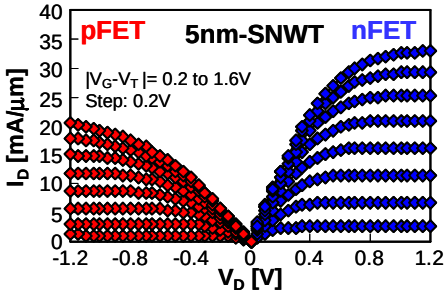

Figure 4: I_D-V_D characteristics of 3D-stacked 5 nm-diameter SNWTs. L_G is 120 nm. Currents are normalized by the top view width W_{NW}.

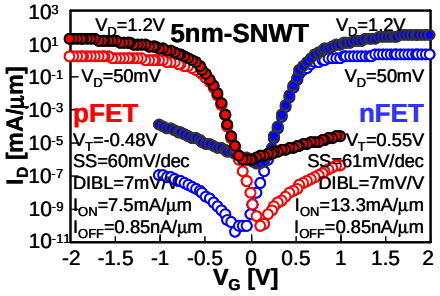

Figure 5: I_D-V_G characteristics of 3D-stacked 5 nm-diameter SNWTs. L_G is 120 nm. Near ideal subthreshold characteristics are obtained.

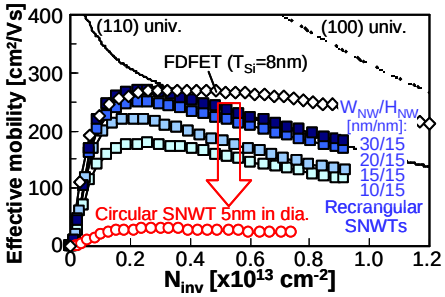

Figure 6: NW size dependence of effective electron mobility. The height of rectangular SNWTs is 15 nm. The mobility of 5 nm-diameter circular SNWTs is clearly degraded.

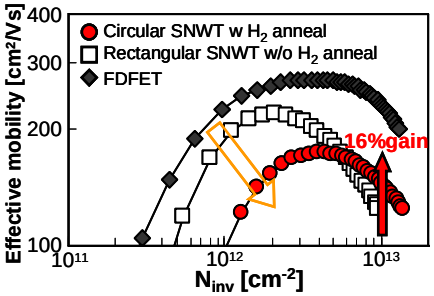

Figure 7: Impact of H_2 annealing. The high field mobility is increased by H_2 anneals, whereas the low field mobility is degraded. Rectangular and circular NWs are W_{NW}/H_{NW}=15nm/20nm and 20nm in diameter (Fig. 1 (b) and (c))

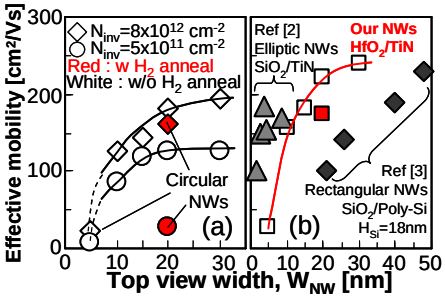

Figure 8: Electron mobility as a function of top view NW width. (a) Comparison between high and low N_{inv}. (b) Comparison with reported SNWTs at medium N_{inv}.

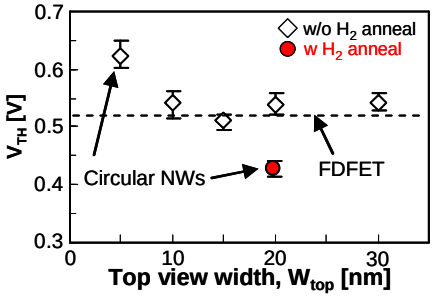

Figure 9: Threshold voltage as a function of top view NW width. V_{TH} are shifted by changing the NW shape from rectangular to circular.

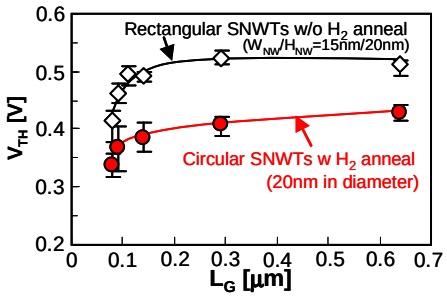

Figure 10: Threshold voltage as a function of gate length. The V_{TH} of circular NWs are systematically lower than those of rectangular NWs, whatever the gate length is.

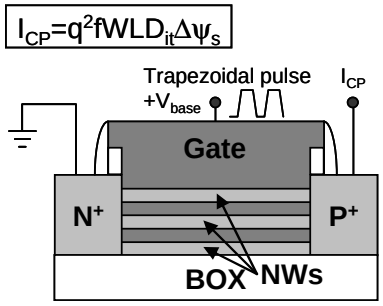

Figure 11: Schematics of the 3D-stacked NWs gated diode used for charge pumping. The gate is pulsed using a trapezoidal waveform generator and varying the base voltage V_{base}. The I_{cp} current is measured on the p^+ contact.

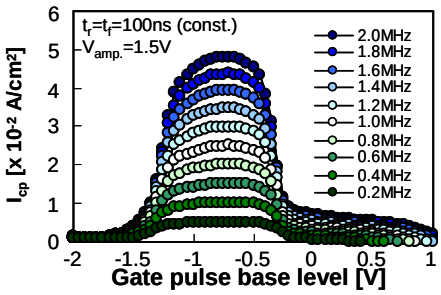

Figure 12: Charge pumping currents (I_{cp}) obtained during base voltage sweep on NW gated-diode structures with L_G=240nm, W_{NW}/H_{NW}=20nm /15nm. The I_{cp} are normalized by total NW surface obtained from TEM images.

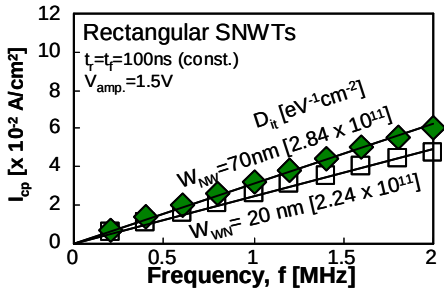

Figure 13: I_{cp} as a function of frequency (f). A good linearity of I_{cp}-f plots is obtained. No degradation of interfacial state density (D_{it}) is observed between wide and narrow NWs.

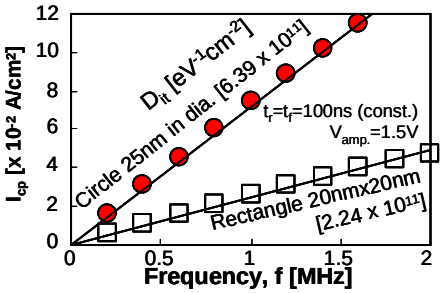

Figure 14: I_{cp} as a function of frequency (f). The D_{it} of circular NWs is three times larger than for rectangular NWs.

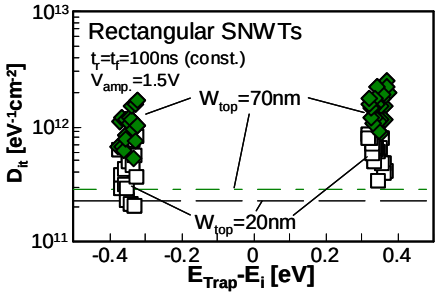

Figure 15: D_{it} energy profile of rectangular Si NWs measured by modifying the rise and fall times of the pulse. The broken lines are the mean D_{it} given in Fig. 13.

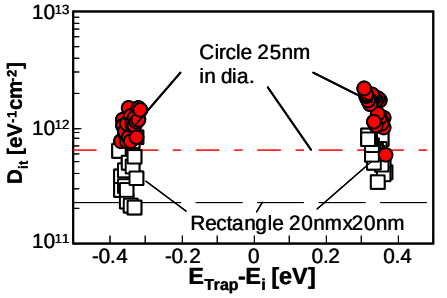

Figure 16: D_{it} energy profile of circular NWs shows no difference between the upper and lower regions of the gap. The broken lines are the mean D_{it} given in Fig. 14.

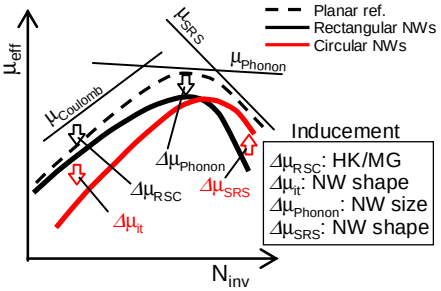

Figure 17: Schematic illustration of mobility limiting factors in SNWTs with HK/MG. A lower coulomb-limited mobility is associated to circular NWs due to higher D_{it}.

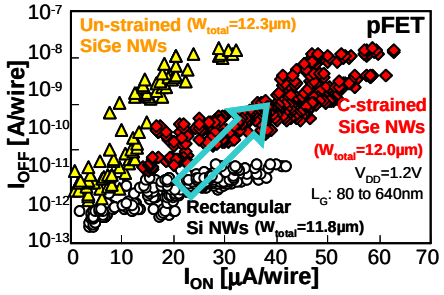

Figure 18: I_{ON}/I_{OFF} characteristics of Si, c-strained and un-strained SiGe NWs normalized by the number of wires. The total NW surface W_{total} is estimated from the cross-sectional TEM images. The W_{NW} of all NWs is ~20nm.

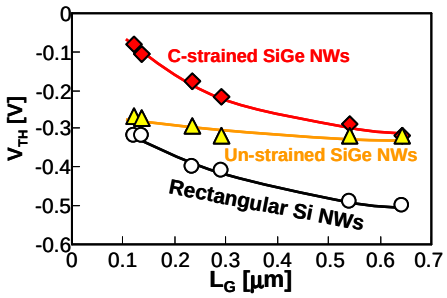

Figure 19: Threshold voltage of Si, c-strained and un-strained SiGe NWs as a function of gate length. The W_{NW} of all NWs are ~20nm.

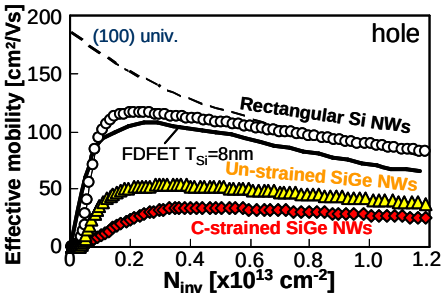

Figure 20: Effective hole mobility of Si, c-strained and un-strained SiGe NWs. The W_{NW} of all NWs are ~20nm.

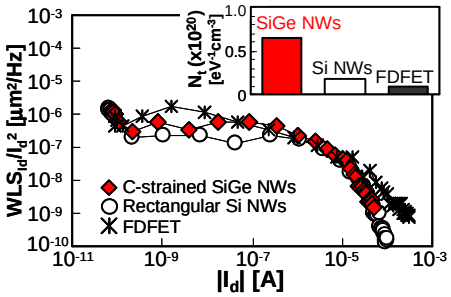

Figure 21: Low-frequency noise of Si and c-strained SiGe NWs. Inserted figure is a comparison of oxide trap density (N_t). L_G and W_{NW} are ~290nm and ~20nm, respectively.