High-Performance Si Nanowire FET with a Semi Gate-Around Structure Suitable for Integration

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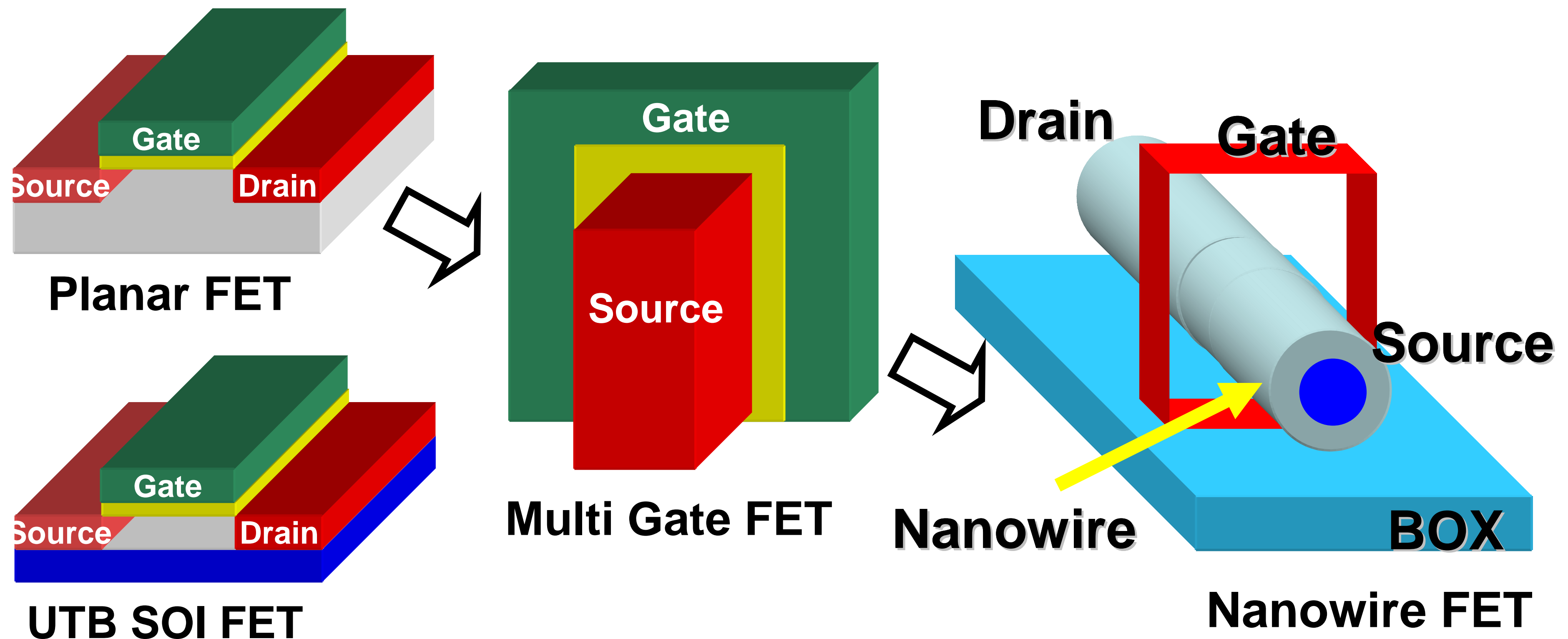
Outline

- Introduction of SiNW FET
- Purpose of this Study
- Device Fabrication Process
- Electrical Characterization
    - I_dV_g I_dV_d Curves
    - Carrier Mobility
- Performance Assessment of Si NW FET
- Conclusion

Introduction of Si Nanowire FET

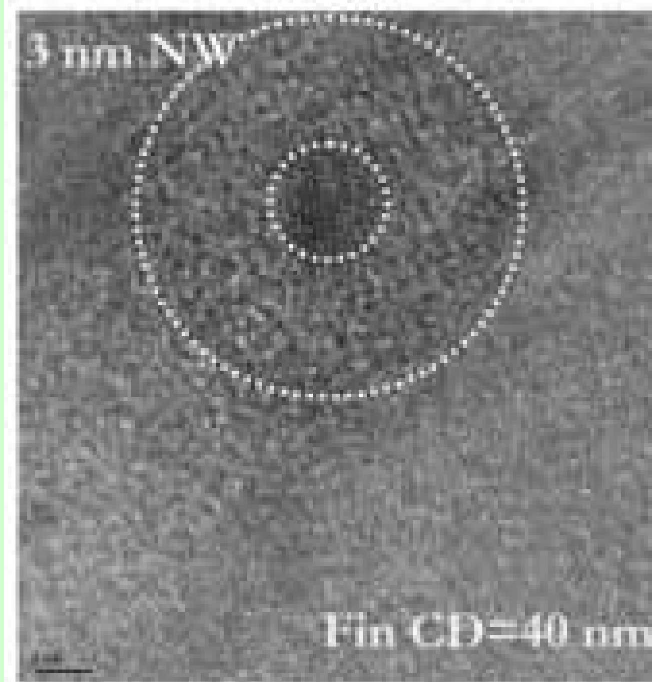


Effective electrostatic control of 1-D channel due to the gate all-around structure.

Low I_{off} can be achieved.

Gate all-around SiNW FETs

Ultra narrow NW FET

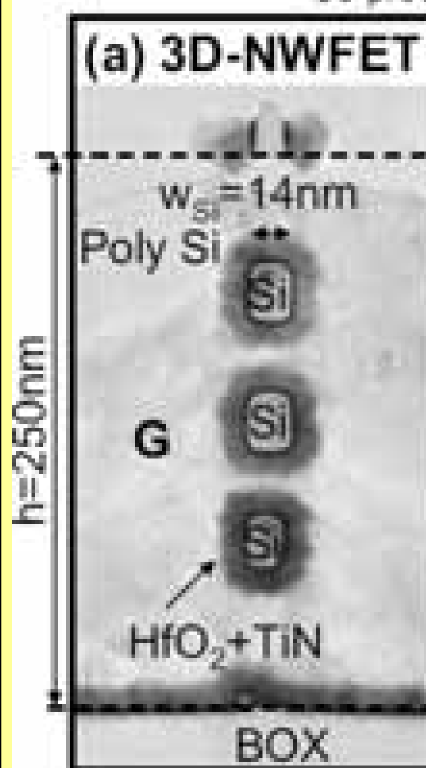


N. Singh, IEDM 2006

SS~60mV/dec, $I_{on}/I_{off} > 10^6$

Oxidation in 875°C for 4 hours

3-Dimensionally Stacked NW multiple channels



Excellent On-current
6.5mA/μm NMOS
3.3mA/μm PMOS
SS: 68/65 mV/dec

C. Dupre, IEDM 2008

Repetitive deposition of Si / SiGe

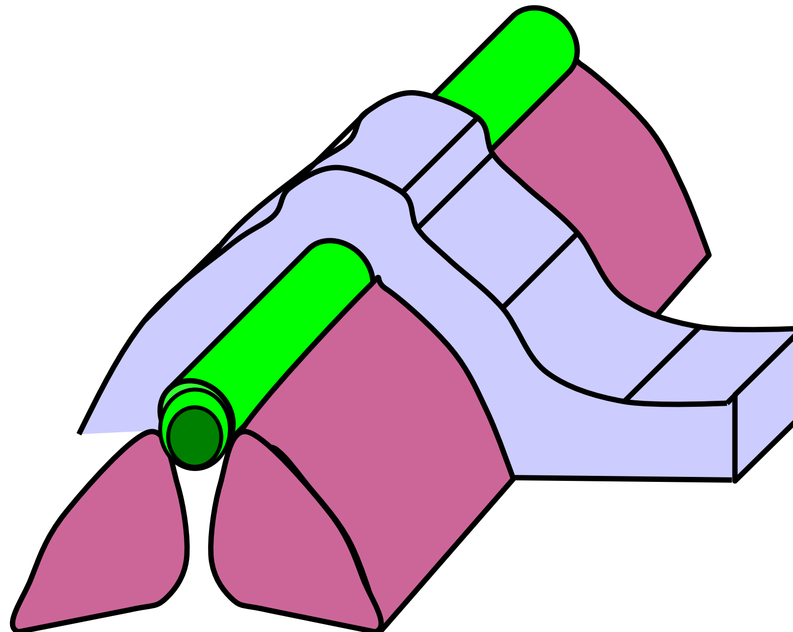
Promising performance for future MOS device

Dedicated process for SiNW FET is necessary

SiNW FET fabrication using conventional CMOS process

Semi Gate-Around Structure

- Si NW channel connected with substrate (BOX Layer) so as not to be released.
- Suitable for application to industrial manufacturing



Purpose of This Work

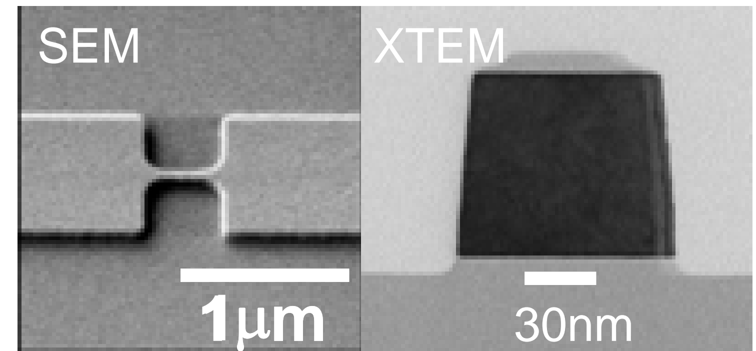
◆Fabrication of a semi-gate around SiNW FET using conventional CMOS processing

◆Demonstration and analysis of FET performance

◆Outlook of semi-gate around SiNW FET for future CMOS devices

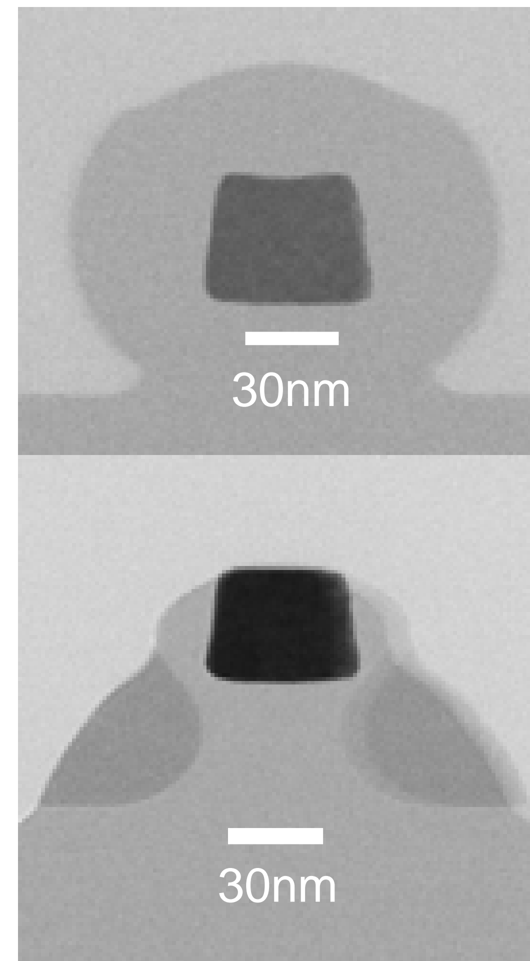
Si NW FET Fabrication

Starting wafer: 300mm SOI (61 / 145 nm)

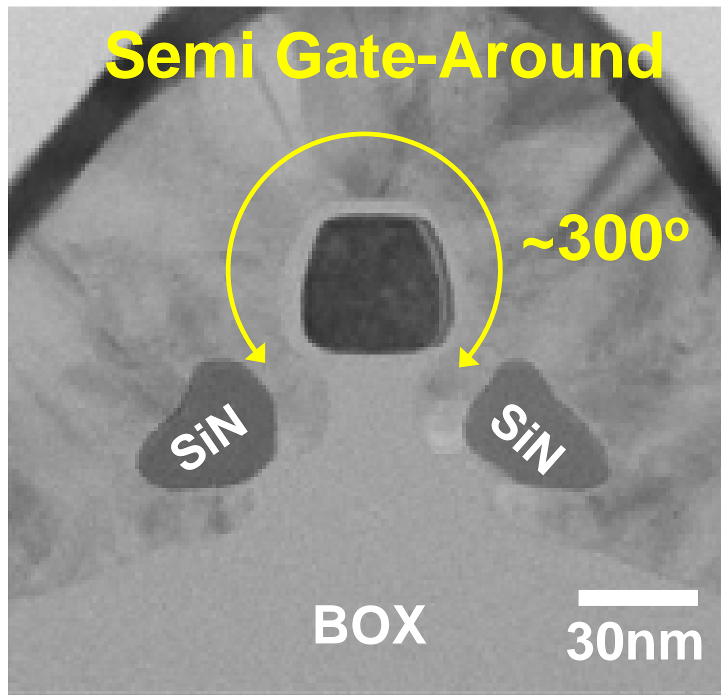


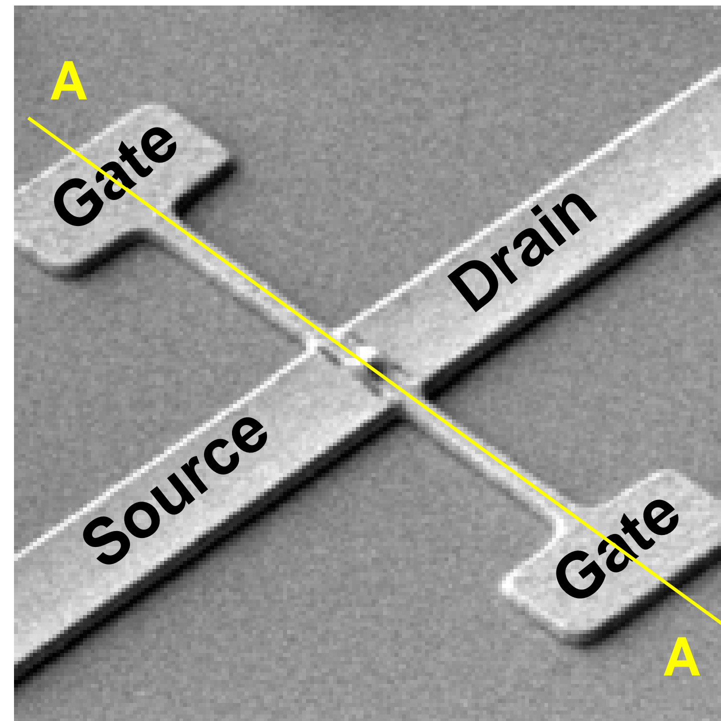
- S/D & Fin Patterning
- Sacrificial Oxidation & Oxide Removal
  DryOx 1000°C for 1 hour
  (not completely released from BOX layer)
- Nanowire Sidewall Formation
  (Oxide Support Protector)
- Gate Oxidation & Poly-Si Deposition
- Ion Implantation (As) into gate Poly-Si
- Gate Lithography & RIE Etching
- Gate Sidewall Formation & S/D Implantation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)

Standard Recipes for CMOS Processes

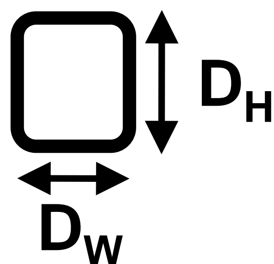


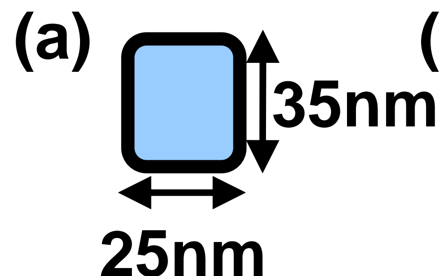
Images of Fabricated SiNW FET

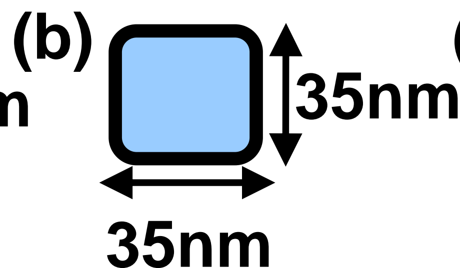


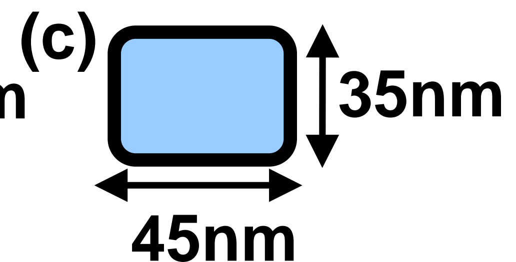


Fabricated Samples

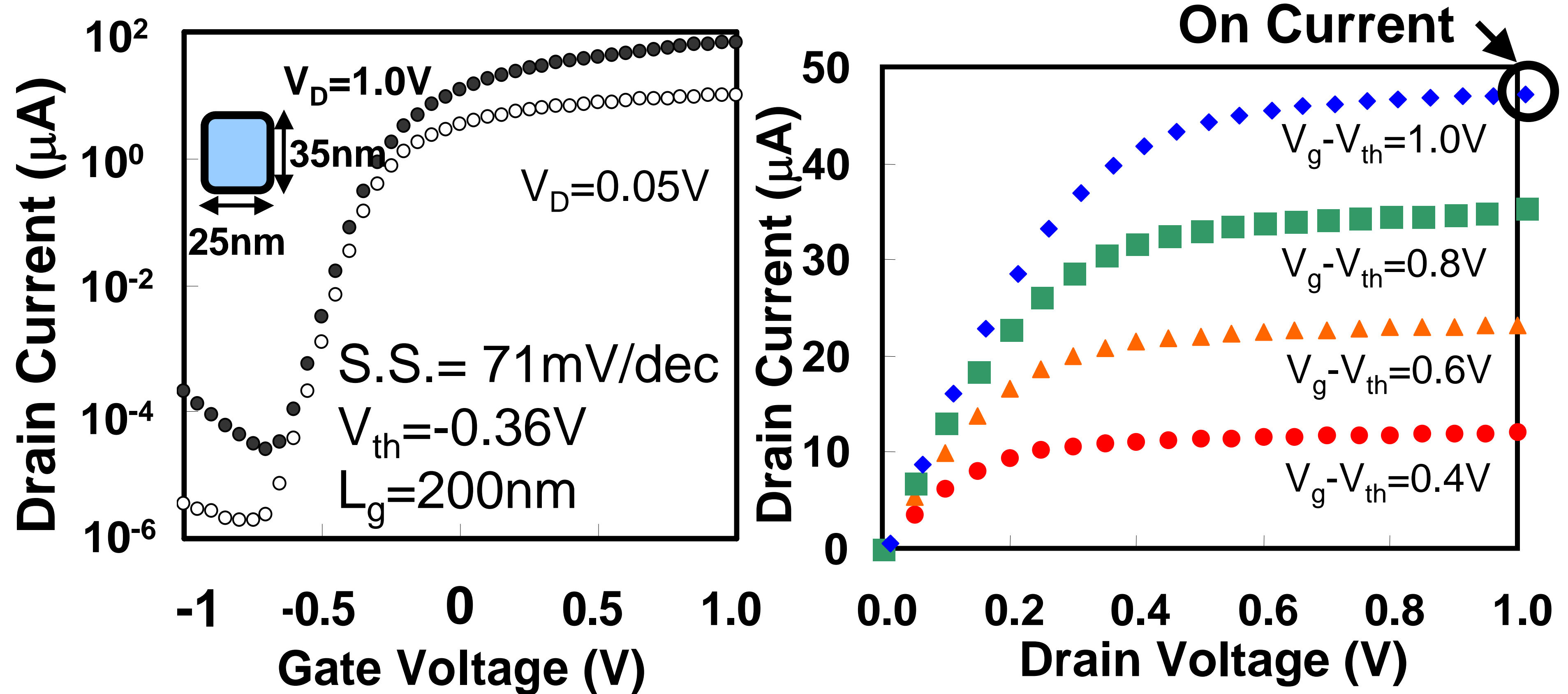








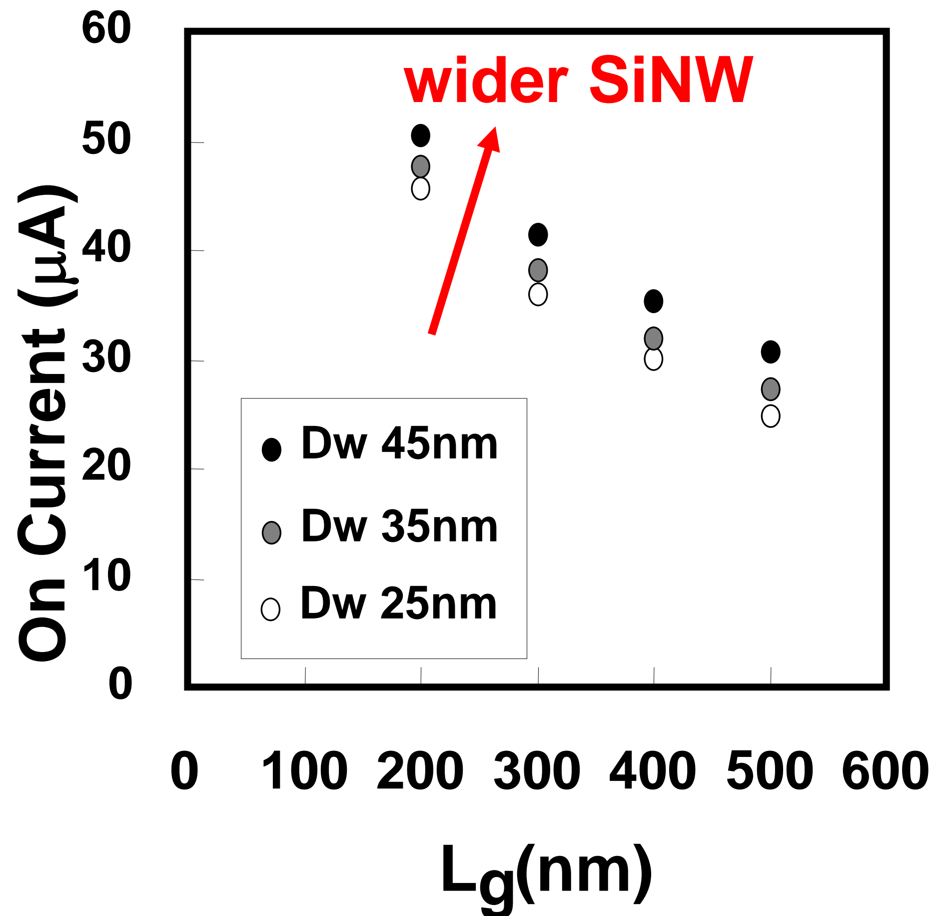
I_dV_g and I_dV_d Characteristics

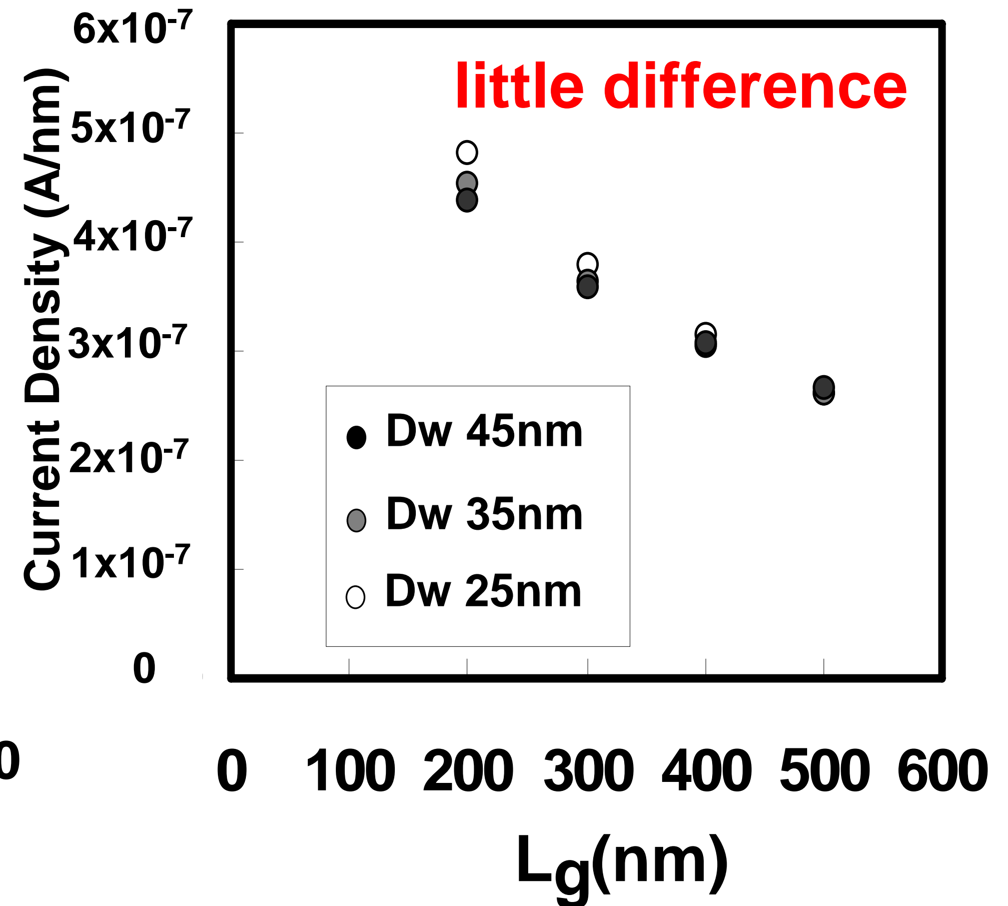


Fairly nice FET operation with I_{on}/I_{off} ~10^7

Large I_{on} of 49μA per wire was achieved

On Current of Si NW FET

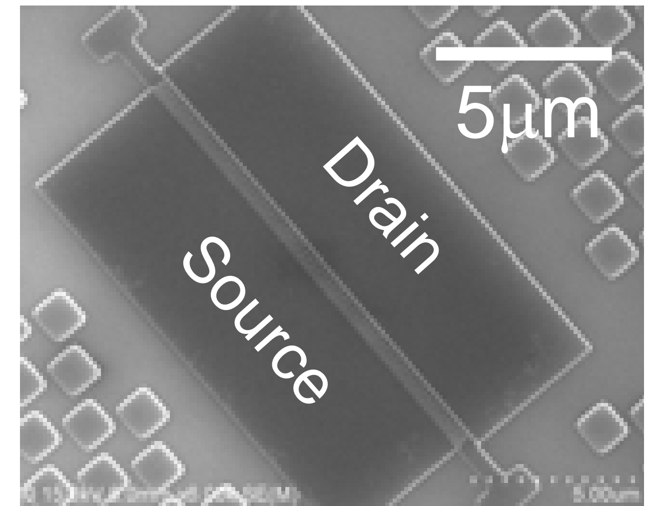




Carriers are formed on the surface of Si Nanowire

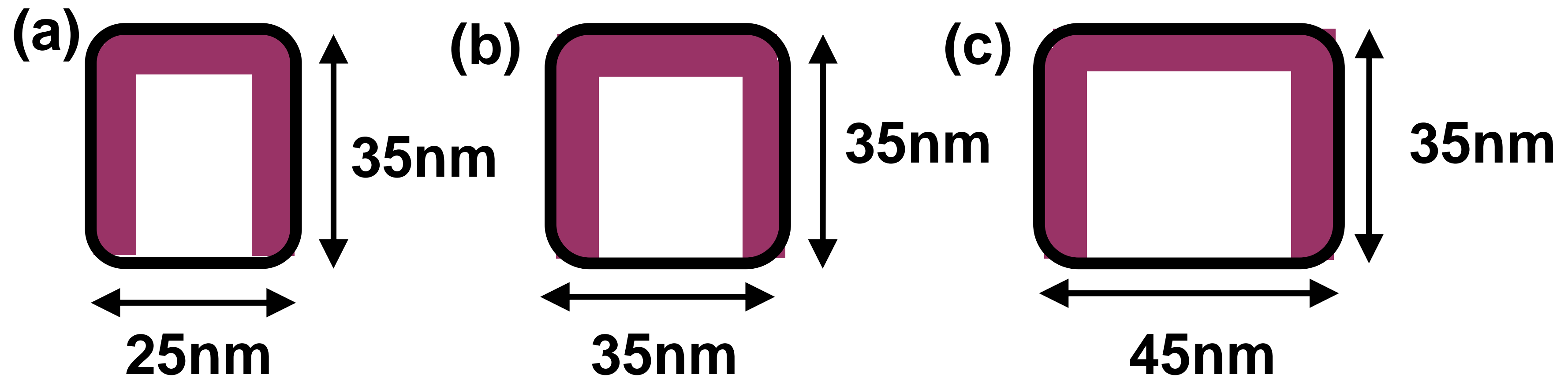
Effective electron mobility of SiNW FET

800
600
400
200
0
μ_{eff} (cm^2/Vs)
L_g=500nm
64 wires in parallel
Planar SiO_2 (100)
(a)
35nm
25nm
measured in room temperature
0
$5x10^{12}$
$1x10^{13}$
$1.5x10^{13}$
Inversion Carrier Density (cm^{-2})



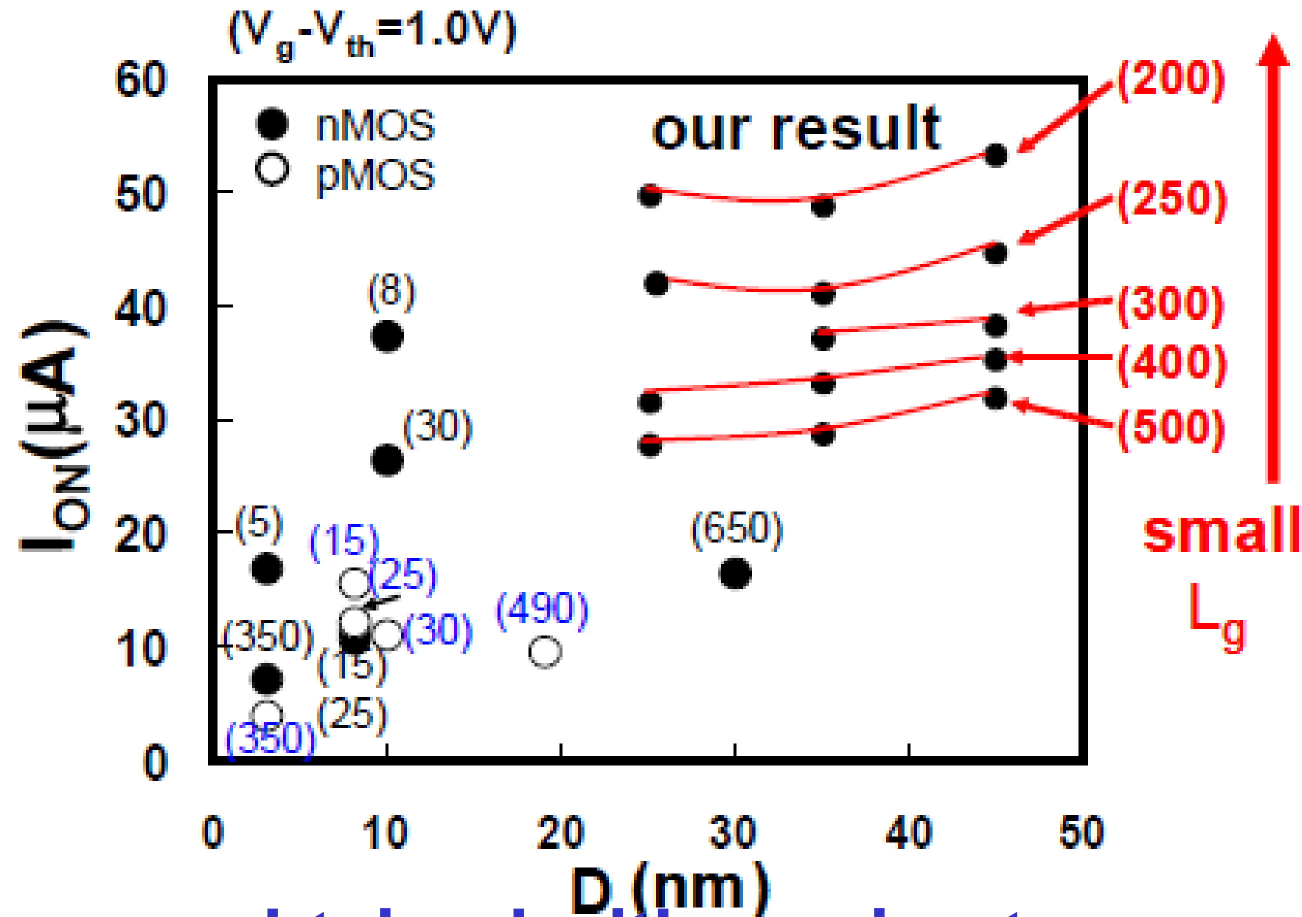
High effective mobility can be achieved with semi-gate around SiNW FET

Design of Channel Shape for High On-Current



- The Si NW FET in this work is the surface channel device.
- Larger I_{on} with longer peripheral length.
- Higher aspect ratio has advantage for large I_{ON}
- The narrowest Si NW FET is the most efficient considering printed area

Benchmark of our SiNW FET

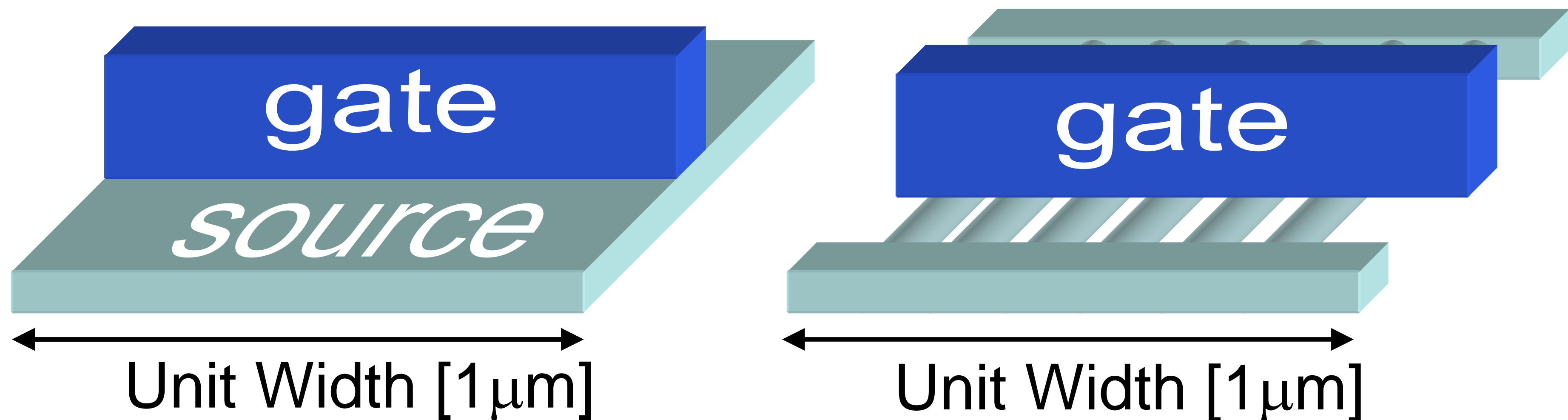


High I_{on} were obtained with semi-gate around Si NW FET

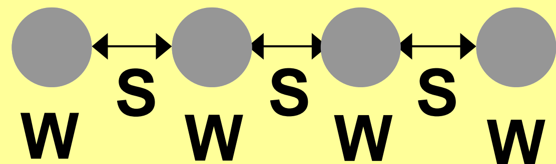
Moreover, further performance can be expected with L_g scaling

Expected On-current Evaluation with SiNW FET

I_{on} should be compared based on unit width.



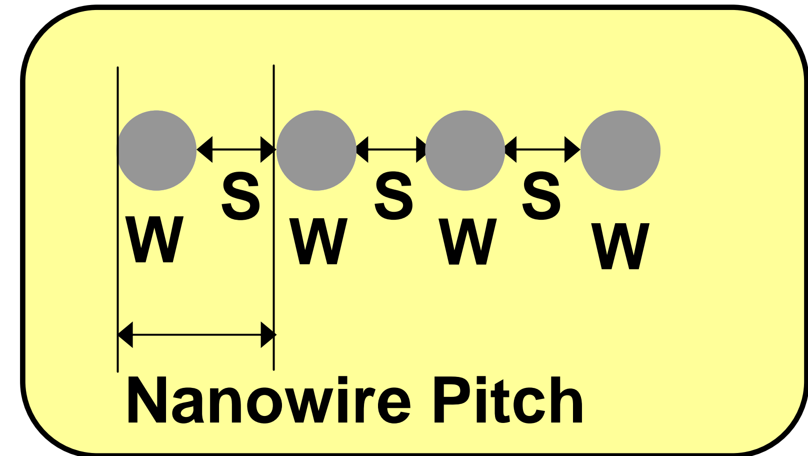
The number of NWs = 1000/ (S+W)

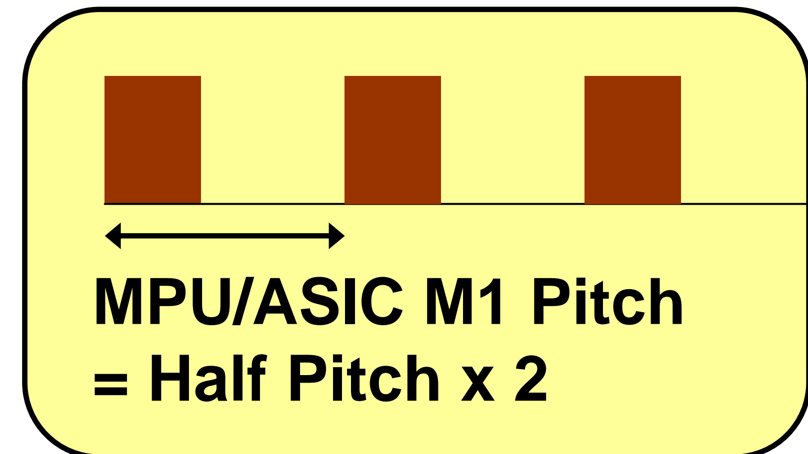


Separation: S [nm]
Diameter: W [nm]
Pitch: S+W [nm]

Estimation of the Number of Si NWs in the Unit Width

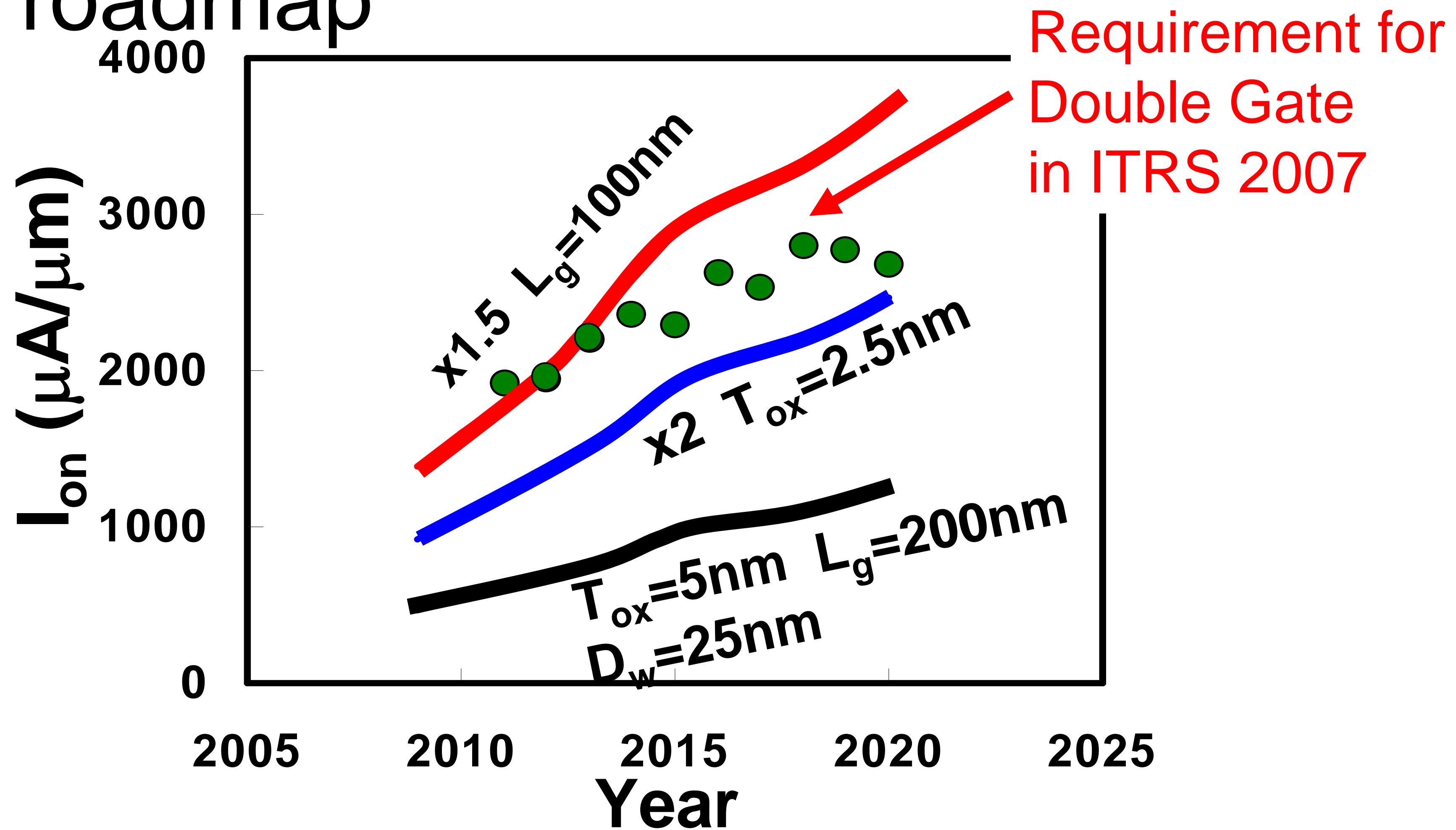
	MPU/ASIC M1 H.P. [nm]	The number of NWs
2010	45	11
2014	28	17
2016	22	21
2018	18	23





The number of NWs is calculated using H.P. of MPU/ASIC M1 pattern

On-current assessment of SiNW FET in roadmap



With device scaling SiNW FET has a potential for future FET structure with high I_{ON}

Conclusion

◆Semi gate-around SiNW FET with conventional CMOS process has been successfully fabricated and performed I_{on}/I_{off}~10^7 and I_{ON} of 49.6μA.

◆From peripheral normalization, surface channel are formed with high mobility.

◆On-current evaluation reveals high potential of SiNW FET to be one of the candidates for future CMOS structure.

Acknowledgement

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