Transport Optimization with Width Dependence of 3D-stacked GAA Silicon Nanowire FET with High-*k*/Metal Gate Stack

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Abstract

3D-staked gate-all-around Silicon Nanowire transistor (SNWT) with high-*k*/metal gate stack is successfully demonstrated and shows excellent transport properties. A high drive current per wire of 39μA for nFET was obtained. The carrier mobility degradation due to the high-*k* was not observed. However, low-temperature measurements show that the surface roughness limited mobility, which significantly affects the gate leakage, is lower than in FD-FET and FinFET, while phonon limited mobility remains unchanged.

Introduction

Gate-All-Around (GAA) silicon nanowire transistors (SNWTs) are most promising candidates for future CMOS due to reduced short-channel effects [1]. Simulation results indicate that the gate lengths in these devices can be scaled down to as small a dimension as the NW diameter itself [2]. To increase the drive current per device, for high density of integration, vertical stacking of NWs is very efficient thanks to increase in the available silicon surface per device [3-5]. In addition, the use of a metal gate and a high-*k* gate dielectric is also required to reduce the gate leakage, with a given equivalent oxide thickness (EOT), for further aggressive scaling [6].

In this paper, 3D-staked GAA SNWTs with high-*k*/metal gate stack are investigated. In particular, we demonstrate the impact of nanowire width on the carrier mobility limiting factors and gate leakage, using room and low temperature measurements.

Device Fabrication

Fig.1 shows a cross-sectional TEM image and a top view SEM image of 3D-stacked SNWTs. First, Reduced Pressure-Chemical Vapor Deposition (RP-CVD) was used to epitaxially grow (25 nm-Si /25 nm-SiGe)x3 superlattice on (100)SOI wafers in order to make vertically stacked wires. NWs are formed by using a hybrid DUV/e-beam lithography and a selective dry plasma etching [4].After chemical cleaning of the channel surface, a HfO_2 (3 nm) / TiN (10 nm) / Poly-Si gate stack was deposited. Fig.2 shows the cross sectional TEM images of NWs with various size. We can also confirm that a lower-k SiO_2-like interfacial layer (T_{IL}: 1.5~2 nm) grows due to thermal process in Fig.2. Finally, the EOT, which is extracted from the NCSU CVC model and the CV curve normalized by the estimated effective surface area, is 2.6 nm. The minimum width of the wire is 10 nm as shown in Fig.2 (a).

Electrical Results

Fig.3 shows I-V curves of 15 nm 3D-stacked GAA SNWTs with L_G=120 nm. The currents are normalized by top view NW width. I_D-V_G plot exhibits near-ideal S.S. (62mV/dec for both n- and p-FET) and low DIBL (17mV/V for both n- and p-FETs). The off-currents I_{OFF} are low with I_{ON}/I_{OFF} ratio $>10^6$. On-currents I_{ON} at V_{DD}=V_G=1.2V of 5.7mA/μm and 3.9mA/μm are obtained for n- and p-FETs, respectively. These extremely high values are due to the vertical stacked NWs (3 stacked wires) and the normalization by the top view width (15 nm in diameter). If I_{ON} is normalized by the effective width, the values are 465μA/μm for nFET and 313μA/μm for pFET. To evaluate the carrier transport property, I_{ON} per wire at V_G-V_{TH}=0.9V is plotted in Fig.4. In comparison with reported values [7-12], I_{ON} of 39μA/wire for nFET with L_G=120 nm is very high. Fig.5 shows I_{OFF}/I_{ON} characteristics with various L_G from 120 nm to 640 nm. Compared with FinFETs, the I_{OFF} of NWs are suppressed. Although HfO_2 was directly deposited on Si surface, Subthreshold Slope (S.S.) shows near ideal value in the whole NWs width range as shown in Fig. 6. Low interfacial trap density might be attributed to the SiO_2 interfacial layer, which was grown during thermal steps [13].

The effective mobility of SNWTs is extracted by using split C-V method with two different gate lengths to remove the overlap capacitance as shown in Fig.7 and 8. In pFET, the mobility for W > 15 nm is higher than (100) universal mobility at high N_{inv}. This striking feature may be attributed to two potential reasons; (i) SiGe layers or TiN metal gate induce compressive stress in the silicon channel [14, 15] and (ii) (110) side surface enables better mobility for pFETs. For narrower nanowire, it is clear that the mobilities of both n and pFET are degraded. The carrier mobility degradations due to the high-*k* is not observed by comparison with SiO_2 and planar bulk FET references [16-25] as shown in Fig.11 and 12, while the gate leakage current is not suppressed (Fig.13 (a)). It is probable that the relatively high leakage is due to the electric field concentration at the corner of quadrangular Si. In addition, the gate leakage increases with decreasing nanowire size as shown in Fig.13 (b). This may be also attributed to that the subband energy increases and the carriers approach the gate oxide interface, thereby increasing the tunneling probability [29]. Fig.14 and 15 show temperature dependence of mobility. By assuming $\mu(T)^{-1} = \mu_{ph}^{-1} + \mu_{sr}^{-1}$ at $N_{inv}=1x10^{13}cm^{-2}$ (T: temperature, μ_{ph}: phonon-limited mobility, μ_{sr}: surface- roughness limited mobility) and μ_{sr}=μ(10K), μ_{ph} of SNWT is the same as in FinFET and FD-FET, while μ_{sr} is lower. This high surface roughness also significantly affects the gate leakage [30].

Conclusion

The 3D-staked GAA SNWTs with high-*k* /metal gate stack have been studied. The mobility for both electron and hole decreases with decreasing NW size, while specific mobility degradation due to high-*k* is not observed. In addition, near ideal S.S. is obtained in spite of the use of high-*k* /metal gate. From these investigations, it appears that the performance of GAA SNWTs will be even enhanced by using further aggressive EOT scaling. However, their surface roughness must be controlled.

References

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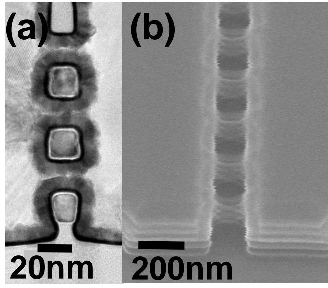

Fig. 1 3D-stacked NWs. (a) Cross sectional TEM image. (b) Top view SEM image.

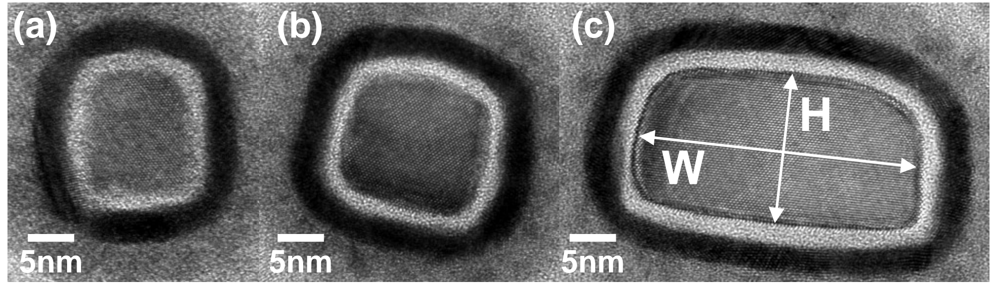

Fig.2 Cross sectional TEM images of 3D-stacked NWs with HfO_2/TiN gate stack. (a) Rectangular NW with Si Width (W)/Height (H)=10nm/15nm. (b) Square NW with W/H=15nm/15nm. (c) Rectangular NW with W/H=30nm/15nm.

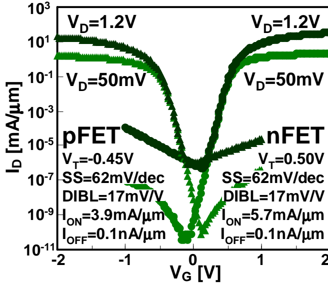

Fig.3 I_D-V_G characteristics of nFET and pFET NWs of 15nm width. L_G=120nm.

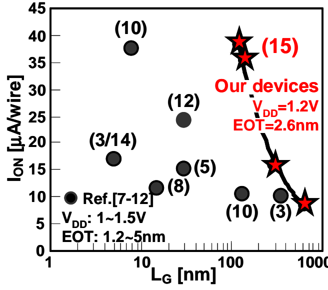

Fig.4 I_{ON} current per wire. The values (in nm) in brackets are the diameters.

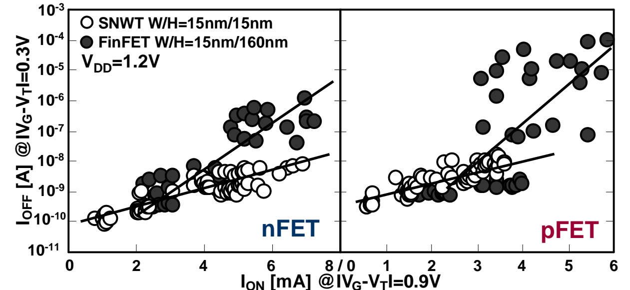

Fig.5 I_{ON}/I_{OFF} characteristics of nFET and pFET. L_G=120~640nm. Compared with FinFETs, the I_{OFF} of NWs are suppressed.

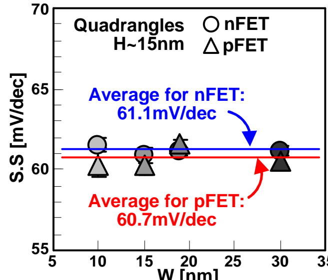

Fig.6 S.S. trend as a function of NW width.

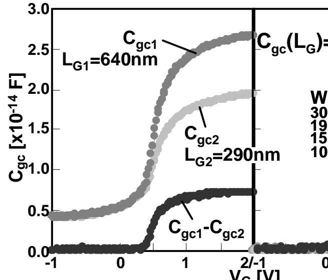

Fig.7 C_{gc} extraction. The overlap capacitance is eliminated by using two different gate lengths.

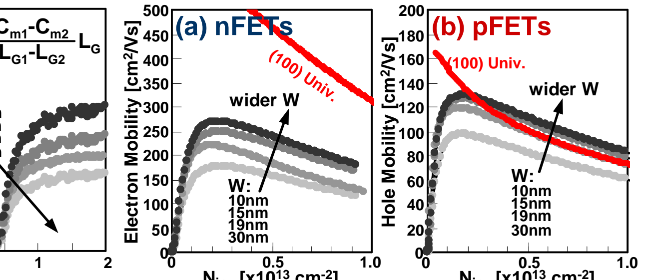

Fig.8 (a) Electron and (b) hole mobility characteristics of NWs. L_G=570nm.

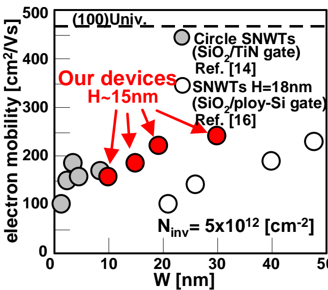

Fig. 11 Electron mobility at N_{inv}= $5x10^{12}cm^{-2}$ as a function of NW width in comparison with SiO_2 SNWTs.

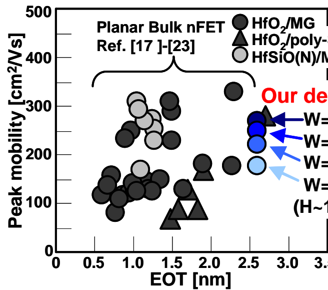

Fig.12 Comparison of peak electron mobility in NWs and planar bulk FETs.

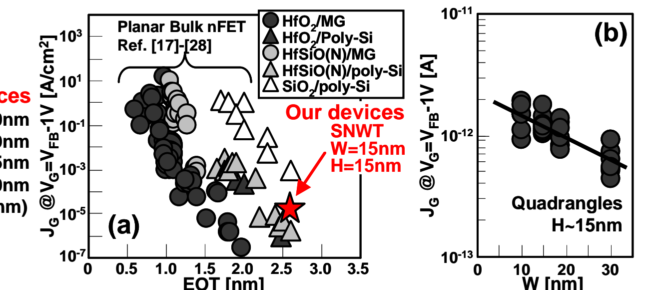

Fig13. Gate leakage current density of SNWT with HfO_2/TiN gate stack. (a) Comparison with planar bulk FETs. (b) NW width dependence.

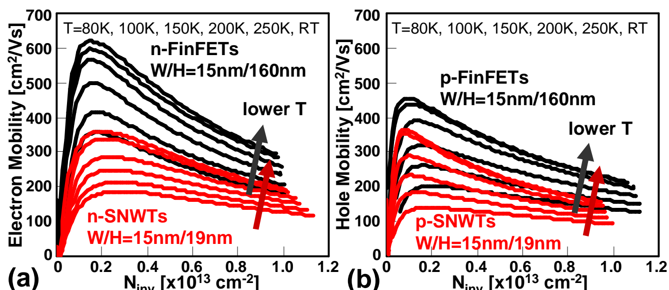

Fig.14 Temperature dependence of (a) electron and (b) hole mobility of SNWT and FinFET.

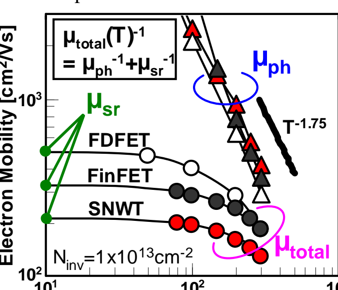

Fig.15 Extraction of surface roughness and phonon limited mobility by Matthienessen's rule. W/H=15nm/19nm for nSNWT. W/H=15nm/160nm for nFin FET. W/T_{Si}=10µm/10nm for nFDFET.

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