Experimental Study for High Effective Mobility with directly deposited HfO_2/La_2O_3 MOSFET

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Abstract

We experimentally examine the effective mobility in nMOSFETs with La_2O_3 gate dielectrics without SiO_x-based interfacial layer. The reduced mobility is mainly caused by fixed charges in High-k gate dielectrics and the contribution of the interface state density is approximately 30% at $N_s = 5x10^{11}cm^{-2}$ in the low $10^{11}cm^{-2}eV^{-1}$ order. It is considered that one of the effective methods for improving mobility is to utilize La-Silicate layer formed by high temperature annealing. However, there essentially exists trade-off relationship between high temperature annealing and small EOT.

Keyword; High-k; effective mobility; direct contact;

1. Introduction

Reduced mobility has been still one of the most important issues in high-k gate MOSFETs [1]. Although SiO_x-based interfacial layer is typically inserted or regrown to suppress the mobility reduction in MOSFETs with high-k gate dielectrics [2], there exists a limitation for further scaling. It is required that high-k gate dielectrics should be directly in contact with Si substrate without any SiO_x interfacial layer [3].

We focus on La_2O_3 as a gate dielectric to achieve a structure without any SiO_x interfacial layer, and La-Silicate layer is formed after annealing instead of SiO_x interfacial layer [4]. One of the concerns for direct contact high-k on Si is relatively high interface state density, D_{it}, and the issue is that to what extent the D_{it} affects to the effective mobility. In this study, we experimentally investigate the contribution of D_{it} on the effective mobility with directly formed high-k/Si

MOSFETs. In addition, we also provide a guidline for improving mobility without SiO_x interfacial layer.

2. Experiment

High-k gate dielectrics (La_2O_3 and HfO_2) were deposited on a HF-last source and drain pre-formed p-Si wafer (N_{sub} = $3x10^{16}cm^{-3}$). La_2O_3 film, followed by HfO_2 one was deposited by e-beam evaporation in an ultra-high vacuum chamber. Tungsten (W) gate electrode was formed by RF sputtering without breaking ultra-high vacuum to avoid any contamination. The samples were post-metallization annealed in F.G. ambient (H_2:N_2=3%:97%) at 500 ^{o}C for 30min. Al was deposited on the source/drain region and back side of the substrate as a contact. Effective mobility was measured by Split-CV method [5]. The gate length and the gate width of the measured devices were 2.5 and 50 μm, respectively. The interface state density was measured by charge pumping method [6].

3. Results and Discussion

Fig. 1 shows the EOT dependence of **(a)** low field mobility and **(b)** D_{it} of HfO_2/La_2O_3 stacked FET where La_2O_3 thickness is fixed to 1 and 2 nm with various HfO_2 thicknesses. The low field mobility is reduced at small EOT, moreover, the mobility observed for 2nm-thick La_2O_3 is lower than that of La_2O_3 1nm indicating larger D_{it} or fixed charge [2]. The D_{it} increases with decreasing EOT. In order to evaluate whether the reduced mobility is mainly caused by D_{it} or not, we intentionally increase the D_{it} by applying an electrical stress of -2 V to the gate to experimentally estimate the contribution of the D_{it} on the effective mobility [7]. **Fig. 2 (a)** shows the surface carrier density, N_s, dependence of effective mobility before and after the electrical stress. After the electrical stress, mobility degradation is clearly observed. We confirmed an increase of $\Delta D_{it}=2x10^{11}cm^{-2}eV^{-1}$ by charge pumping measurement. Note that no hysteresis in gate-channel capacitance, C_{gc} - V_g and I_d - V_g characteristics was observed which means the generation of bulk traps in High-k dielectrics is negligibly small after the electrical stress. **Fig. 2 (b)** shows the comparison of μ_{eff}-N_s characteristics between EOT of 2.24 and 1.76 nm for 1nm-thick La_2O_3 nMOSFETs. Matthiessen's rule,

$1/\mu_{it}=1/\mu_{After\text{-}Stress}-1/\mu_{Initial}$,

$1/\mu_{EOT}=1/\mu_{A}-1/\mu_{B}$,

is utilized in order to extract the contribution of $\Delta D_{it}=2x10^{11}cm^{-2}eV^{-1}$ on the effective mobility. **Fig. 3** shows the N_s dependence of extracted mobility. The μ_{it} and μ_{EOT} at N_s = $5x10^{11}cm^{-2}$ are evaluated to be about 2000 and 600 cm^2/Vsec, respectively. The contribution of $\Delta D_{it}=2x10^{11}cm^{-2}eV^{-1}$ on the effective mobility is approximately 30% at N_s = $5x10^{11}cm^{-2}$. Thus, the effective mobility is mainly reduced by Coulomb charges in high-k gate dielectrics and the impact of D_{it} is relatively small.

As previously mentioned, the low field mobility is sensitive to La_2O_3 thickness. In order to investigate the effect of La_2O_3 thickness on the effective mobility more precisely, we fabricated samples which have the same EOT but with different La_2O_3 and HfO_2 physical thickness. **Fig. 4** shows the electrical characteristics of MOS Capacitors and MOSFETs for various gate stacks. Humps to C-V curve was found to decrease by decreasing the La_2O_3 thickness shown in **Fig. 4. (a)**. Subthreshold slop is increased while increasing the La_2O_3 thickness shown in **Fig. 4. (b)**. **Fig. 4. (a)** and **(b)** indicate that thinning the La_2O_3 layer improves the amount of trap states in La_2O_3. **Fig. 4. (c)** shows the effective mobility for various gate stacks. It is clearly observed the effective mobility with 2nm-thick La_2O_3 is reduced in both low and high effective field. This result suggests that phonon or surface roughness scattering is enhanced at 2nm-thick La_2O_3 [2]. The impact of D_{it} on the effective mobility is relatively small, as discussed previously. In order to investigate the trap charges in La_2O_3, we performed the variable amplitude charge pumping measurement [6]. **Fig. 5** shows the charge pumping measurement by varying the V_{amp}. I_{cp} increase with increasing La_2O_3 thickness, which means the large amount of bulk traps exist in thick La_2O_3 layer. Therefore, the trap charges near the substrate bring about the severe mobility degradation. Since the large amount of trap charges still exists in La_2O_3, it is considered that high temperature annealing will be effective in reducing trap charges. However, there are essentially trade-off relationship between high temperature annealing and small EOT.

4. Conclusion

We experimentally examined the origin of decrease in effective mobility with direct contacted High-k on Si substrate. The effective mobility decreases mainly by the fixed charges in high-k gate dielectrics even if without any SiO_x interfacial layer. It was clarified that the effective mobility is severely degraded with increasing La_2O_3 thickness. Our experimental results suggest that La-silicate film will be utilized to improve the effective mobility without SiO_x interfacial layer. It is considered that La-silicate formed by high temperature annealing is to improve the performance of MOSFET. However, there are basically trade-off relationship between small EOT and high annealing temperature.

Acknowledgements

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Figure Captions

Fig. 1. EOT dependence of **(a)** low field mobility and **(b)** interface state density.

Fig. 2. Surface carrier density, Ns, dependence of Effective mobility. **(a)** Comparison of effective mobility between before and after the electrical stress and **(b)** Effective mobility as a function of EOT. La_2O_3 thickness is fixed to 1 nm with varying HfO_2 thicknesses.

Fig. 3. N_s dependence of μ_{it} and μ_{EOT} in nMOSFETs. μ_{it} and μ_{EOT} are extracted by Matthiessen's rule.

Fig. 4. Electrical characteristics of MOSCapacitors and MOSFETs for various gate stacks. **(a)** C-V characteristics of MOSCapacitors. **(b)** Subthreshold slop as a function of La_2O_3 thickness. **(c)** Effective mobility versus effective field.

Fig. 5. I_{cp} as a function of gate pulse amplitude.

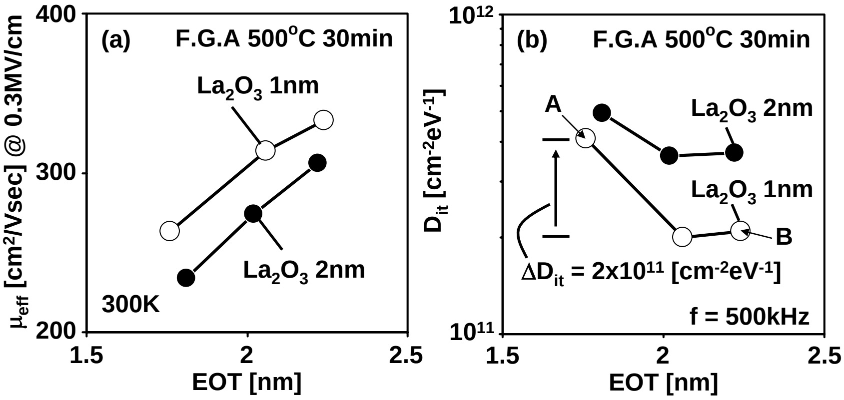


Fig. 1.

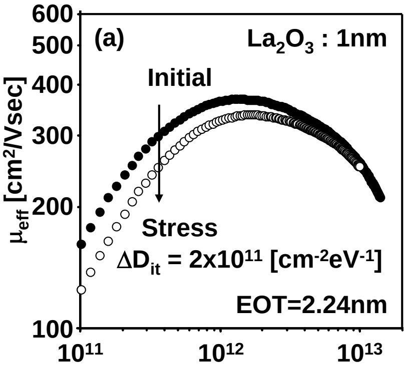


Fig. 2. (a)

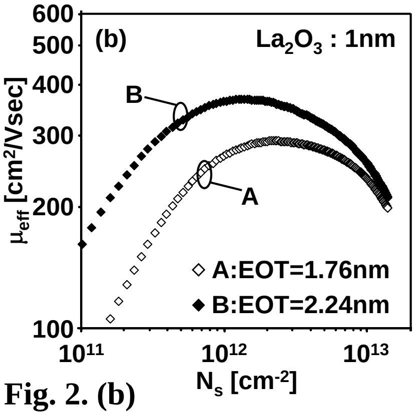


Fig. 2. (b)

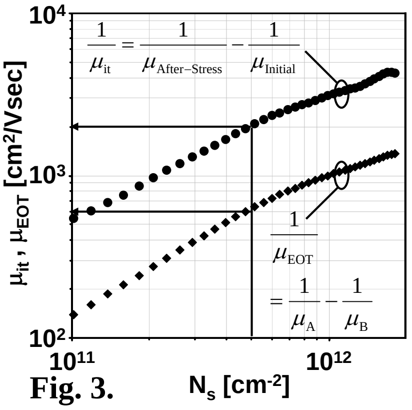


Fig. 3.

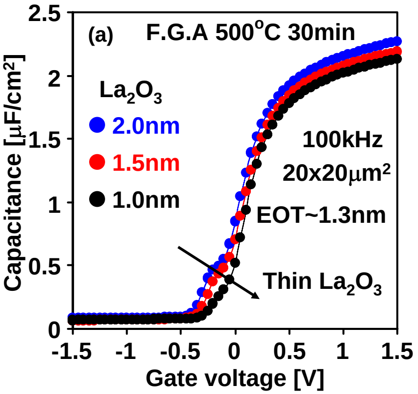


Fig. 4. (a)

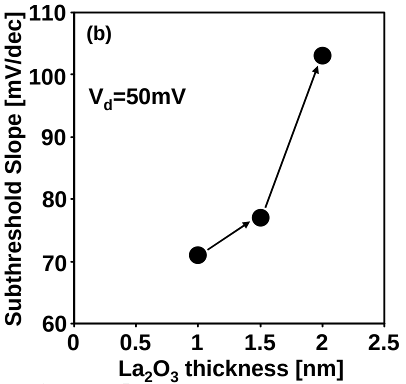
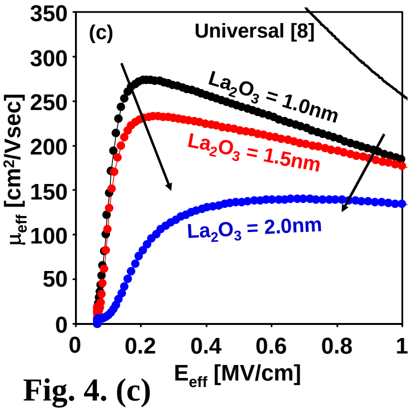


Fig. 4. (b)



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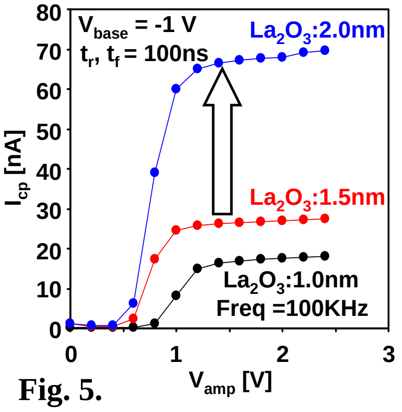

Fig. 5.