Bachelor Thesis

Electrical Characterization of La_2O_3-Gated MOSFET with Mg Incorporation

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Abstract of Bachelor Thesis

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In order to improve the performance of VLSI technology, the introduction of high-k gate dielectrics into MOSFET is essential. However, mobility degradation of MOSFETs with high-k gate dielectrics has been one of the major issues. It is considered that fixed charges in the high-k layer induce remote Coulomb scattering (RCS) to degrade the mobility. On the other hand, it has been reported that Mg incorporation into the dielectrics of Hf-based MOSFETs shows large improvement in mobility and reliability as well. This is mainly attributed to the decrease of charged defects associated with oxygen vacancies.

Among various high-k materials, La_2O_3 is one of the most promising materials, as it can achieve an interface without an SiO_2-like layer, which is advantageous for further gate dielectric scaling. It would be worth trying to incorporate Mg into La_2O_3 to suppress the generation of fixed charges. This paper focuses on the electrical characteristics of La_2O_3 with Mg incorporation. It is confirmed that the fixed charge generation as well as mobility degradation has been suppressed. Moreover, the interfacial state density (D_{it}) has been improved. Therefore, incorporation of Mg can be regarded as a technology for further scaling in gate dielectric.

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1 Introduction

1.1 Introduction of high-k dielectrics into MOSFETs

Metal-oxide-semiconductor field effect transistor (MOSFET) is essential for very large scaled integrated circuit (VLSI) technology, which is used in the various electrical units including central processing unit (CPU), dynamic random access memory (DRAM) and so on. For example, the units are used in PC, cell-phone and TV. So, our life is filled with the VLSI technology. In order to make the technology with higher performance, devices, which are composed of the VLSI, should be miniaturized and to be densely packed. The MOSFETs should be also, of course, miniaturized by device scaling. SiO_2 have been used as gate dielectrics of the MOSFETs because of its high stability and heat resistance. But, as the device scaling goes on, physical thickness (t_{py}) of SiO_2 dielectrics becomes thin and large leakage current by quantum tunneling effect between gate and Si-substrate increases exponentially. Because of the extreme leakage current (I_{leak}), MOSFETs consume large power. In this reason, MOSFETs with SiO_2 dielectrics will not be in use for further scaling. But, because drain current (I_{ds}) is in inverse proportion to t_{py} and in proportion to dielectric constant (k) of the dielectrics, as described in Appendix A, I_{ds} can be increased without decreasing t_{py} by using high-k materials. Moreover, at a same equivalent oxide thickness (EOT), MOSFETs using high-k dielectrics have less I_{leak} than SiO_2 because the former can get larger t_{py} as shown in Fig 1.1. The EOT can be written as

$$EOT = \frac{\varepsilon_{SiO2}}{\varepsilon_{highk}} t_{py}, \quad (1.1)$$

where ε_{SiO2} and ε_{highk} are respectively the permittivity of SiO_2 dielectrics and that of high-k dielectrics. EOT is regarded as important index.

In these reasons, various high-k materials have been studied.

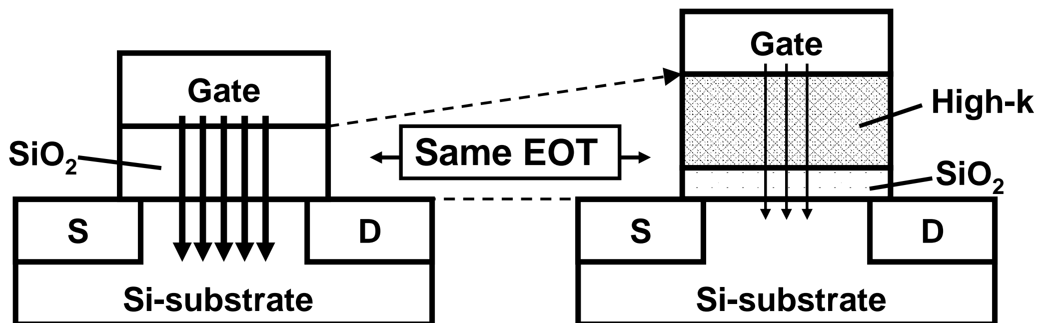

Fig.1.1 High-k dielectrics can get larger physical thickness than SiO_2 in spite of the same EOT. As a result leakage current decreases.

1.2 Issues in high-k dielectrics for MOSFET

In terms of I_{leak}, MOSFETs with high-k gate dielectrics are superior to those using SiO_2 dielectrics. However, mobility degradation of MOSFETs with high-k has been one of the major issues [1]. It is considered that fixed charges in the high-k layer induce remote Coulomb scattering (RCS) to degrade the mobility. The fixed charges are generated mainly because of diffusion of the metal gate into the dielectric. The schematic illustration of the RCS mechanism is shown in Fig.1.2. One of the solutions is to form a SiO_2-based interfacial layer to keep the fixed charges in the high-k layer away from the channel. However, the EOT will increase with the use of SiO_2. In order to further reduce the EOT with scaling, high-k should be directly in contact to Si-substrate as shown in Fig.1.3. But, among various high-k materials, SiO_2 interfacial layer is formed after thermal treatment with worse interfacial electrical property. Therefore, the choice of high-k material is very important.

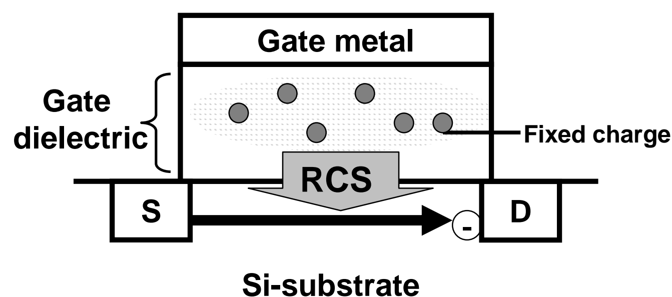

Fig.1.2 The fixed charges have a bad influence on the electrons in the channel by Coulomb force, which degrade the mobility.

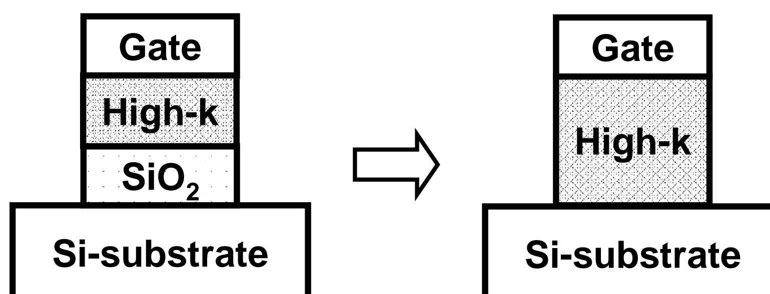

Fig.1.3 In order to get lower EOT, high-k dielectrics should be directly contacted to Si-substrate.

1.3 La_2O_3 as gate dielectrics

Among all high-k materials, La_2O_3 is one of the promising high-k dielectrics. As shown in Fig.1.4, if the La_2O_3 is in direct contact, an EOT below 1 nm can be achieved by forming a La-silicate layer, which has a k-value ranging from 8 to 14 at the interface and shows fairly nice performance [2]. Therefore, MOSFETs with La_2O_3 dielectrics is expected to be a material for next-generation technology. However, as shown in Fig.1.5(a) and (b), additional mobility degradation has been observed in the range of EOT below 1.4 nm accompanied by a negative shift in flat band voltage (V_{fb}). It is also considered to be due to fixed charges in high-k. Therefore, another method to reduce the fixed charges is required.

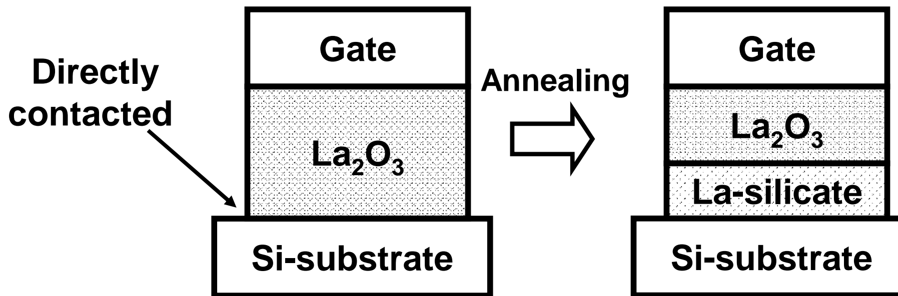

Fig.1.4 La_2O_3 forms a La-silicate layer at the interface, which has a k-value ranging from 8 to 14.

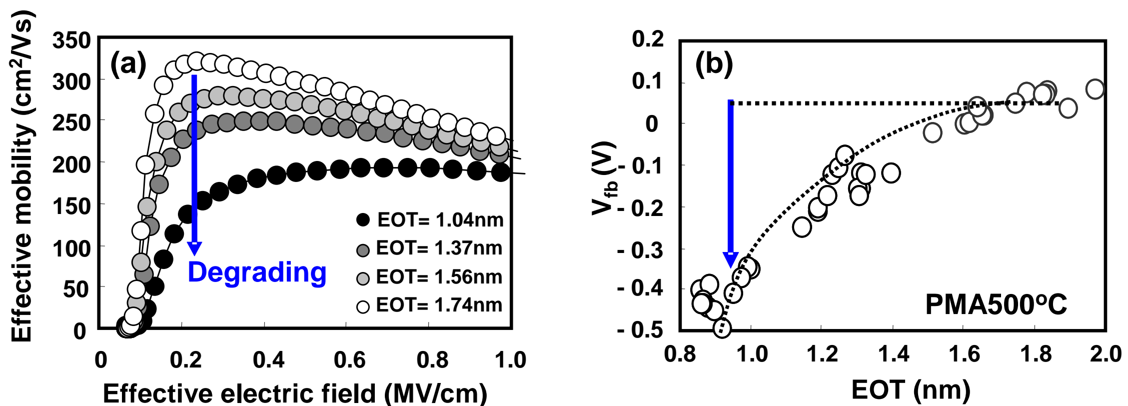

Fig.1.5 (a)Mobility degradation has observed especially in the range of below 1.4nm. (b) A negative shift in flat band voltage is also observed.

1.4 Mg incorporation into gate dielectrics

It has been reported that incorporation of Mg into Hf-based dielectrics shows marked improvement in mobility and reliability as well (Fig.1.6)[3]. This is mainly attributed to the decrease of charged defects associated with oxygen vacancies. [4] Therefore, it would be worth trying to incorporate Mg into La_2O_3 to suppress the increasing fixed charges while reducing the EOT.

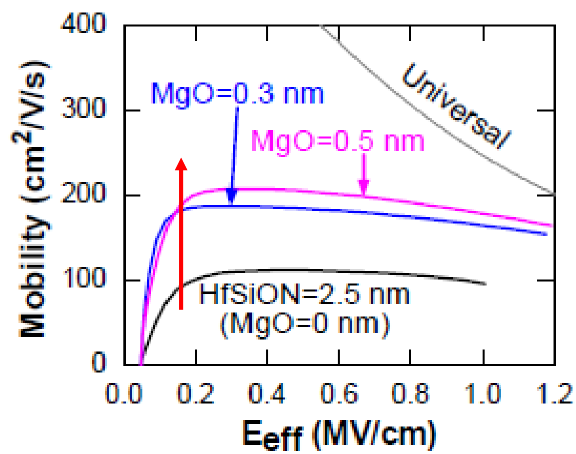

Fig.1.6 It has been reported that mobility of Hf-based MOSFET was improved with Mg incorporation.[3]

1.5 Purpose of this study

The purpose of this study is to elucidate the effect of Mg incorporation into La_2O_3 gated MOS capacitors and FETs performance.

Chapter 1 indicates the background and the purpose of this study. Chapter 2 expresses the experimental procedure and the principles performed. In chapter 3, physical analysis and electrical characteristics are performed and the advantage of Mg is discussed. Chapter 4 summarizes this study and the outlook is described.

2 Experiment

2.1 Experimental principle

2.1.1 SPM cleaning and HF treatment process

In order to get high reliability of MOSFETs, the cleaning of the wafer is very important. Sulfuric-peroxide mixture (SPM) cleaning is one of the most effective cleaning methods. The wafer is immersed into the H_2O_2 and H_2SO_4 mixed liquid (H_2O_2:H_2SO_4 = 1:4) heated 100°C during 10 min. Because the liquid is strong oxidizing agent, the metal or carbon related contamination on the wafer are oxidized and separated from the wafer. But, because of the strong oxidation power, the surface of Si is also oxidized and become about 0.8-nm-thick SiO_2, which is called chemical oxide. In order to eliminate the SiO_2, the wafer is immersed again into 1% HF during 1~2min. Schematic illustration of this process is shown in Fig.2.1.

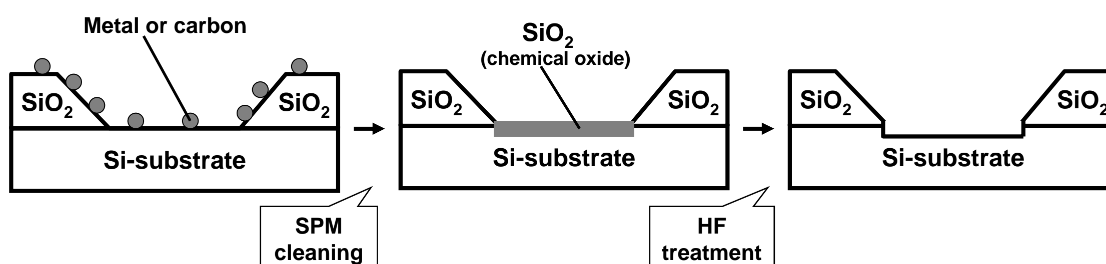

Fig.2.1 Schematic illustration of SPM cleaning and HF treatment.

2.1.2 E-beam evaporation and RF magnetron sputtering deposition

Electron beam (E-beam) evaporation is one of the effective methods for deposition of the gate dielectrics. E-beam evaporation is one of the deposition methods and is used in molecular beam epitaxy (MBE). In ultra high vacuum, the e-beam is spotted on the source material. The current generates on the material and Joule heat is caused. Because of the Joule heat, the material is heated to emit the molecules. The molecules are in the ultra high vacuum, so they evaporate without striking other molecules to be deposited on the wafer. This method that the molecules of the source material can be deposited without striking other molecules in the ultra high vacuum is called MBE. In this experiment, La_2O_3 and Mg were deposited using this method as shown in Fig.2.2(a). By moving the shutter as shown in Fig.2.2(b), the thickness of La_2O_3 was controlled from 2 nm to 4 nm in one operation and the various values of EOT were

obtained.

Radio frequency (RF) magnetron sputtering is one of the deposition methods for the gate metal. In this study, W as the gate metal was deposited by RF magnetron sputtering using the Ar gas. In the chamber filled with the Ar gas, the high voltage is applied in high frequency between the target (W) side and the sample side. The Ar molecules are divided into Ar ions and electrons because of the difference of mass. Because the sample side keeps conductive and the target side keeps dielectric, the electrons gathered on the sample side can flow into the circuit but those on the target side are kept gathered. The target side has the minus bias and Ar ions with momentum crash to the target. By the crush, the particles of the target are emitted and deposited on the samples. In the magnetron sputtering, because the plasma is generated on the target side by the magnetic force, the samples are not damaged by the plasma as shown in Fig.2.3. [5]

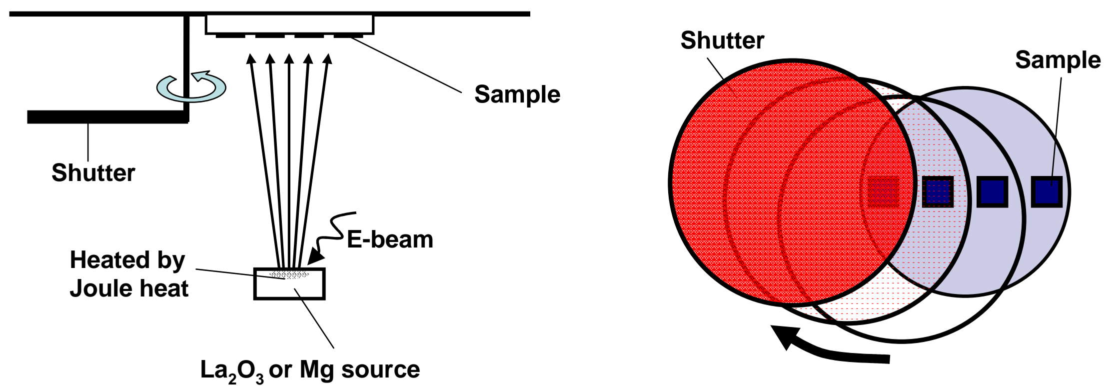

Fig.2.2(a) La_2O_3 and Mg were deposited by e-beam evaporation.
(b) The thickness of La_2O_3 was adjusted by moving the shutter.

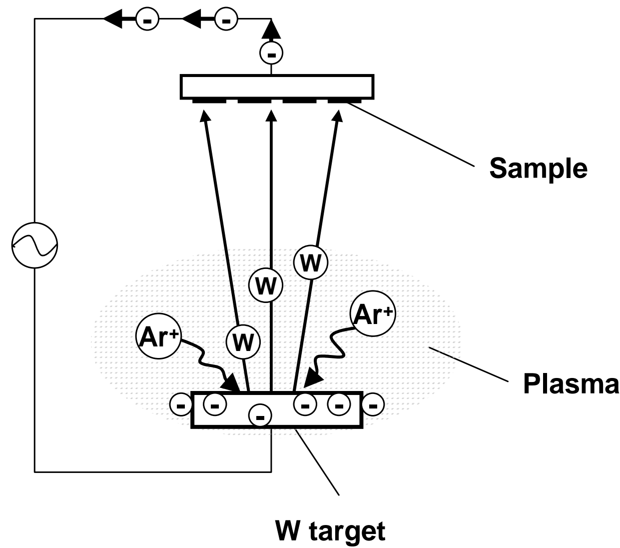

Fig.2.3 Schematic illustration of RF magnetron sputtering. By the crash of the Ar ions, the W particles were emitted and deposited.

2.1.3 Dry and wet etching process

Reactive ion etching (RIE) is one of the dry etching methods. In the same way as the RF sputtering, the gas in the chamber is plasmanized and crashed to the samples. But, in the RIE process, not the physical crash but the chemical reaction between the ions and samples is important. W combined with F^- and get WF_6, which boiling point is 18^oC. WF_6 is evaporated and eliminated from the sample. So, in this experiment, SF_6 is used as etching gas for W etching. Mg was considered to be also etched by SF_6 because Mg layer was very thin. On the other hand, the resist, which is attached to the sample by the photolithography, reacts with not SF_6 but O_2 and is eliminated. This phenomenon is called ashing. O_2 is used as the etching gas of the resist. Fig.2.4 shows the RIE process.

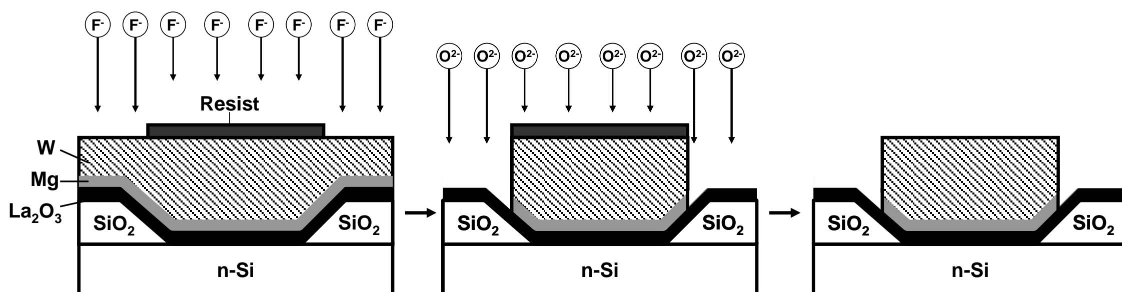

Fig.2.4 Schematic illustration of RIE. W is eliminated by F^- and the resist is eliminated by O^{2-}.

HCl and buffered HF (BHF) were used for the wet etching. BHF is the mixture liquid of HF, NH_4F and H_2O. HCl dissolves La_2O_3 and SiO_2 and BHF dissolves SiO_2. But, both HCl and BHF don't dissolve the resist. The resist is dissolved by the acetone. By these chemical reactions, the dielectrics are etched. The wet etching process is shown in Fig.2.5.

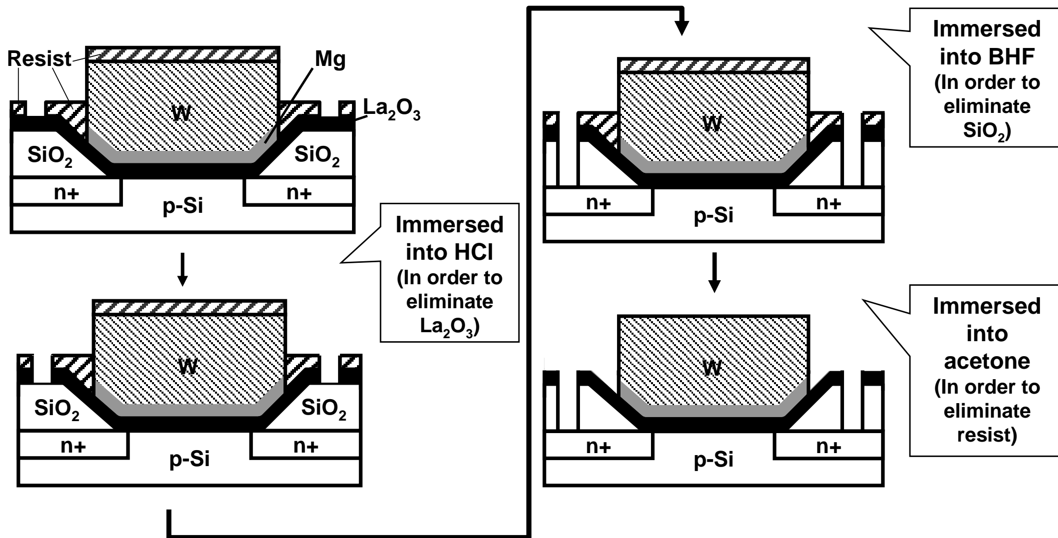

Fig.2.5 Schematic illustration of the wet etching process. La_2O_3 and SiO_2 were respectively eliminated by HCl and BHF. Finally, the resist was eliminated by acetone.

2.1.4 Decrease of D_{it} by PMA

The improvement of the interfacial state density (D_{it}) at the Si/La_2O_3 interface is one of the problems. Generally, it is considered that the interface traps are caused by the dangling bonds of Si. In order to decrease the dangling bonds, the post-metalization annealing (PMA) in a hydrogen-containing ambient is effective. As shown in Fig.2.6, the dangling bonds are eliminated by combining with H^+. So, in this study, the PMA was carried in forming gas (F.G.) (N_2: H_2 = 97% : 3%) ambient at 500 ^oC for 30 min. [6]

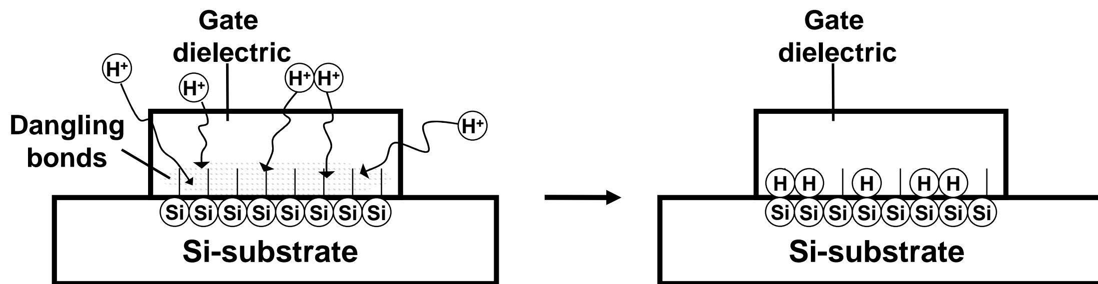

Fig.2.6 The dangling bonds of Si combine with H^+. As a result, the number of dangling bonds are decreased.

2.1.5 Al deposition by vacuum evaporation method

In this study, Al was used for the backside electrode and Al wiring. Al was deposited by vacuum evaporation method. Al source was set on W boat in the chamber. The large current was passed in the W boat and the W boat was heated by the Joule heat. Because the boiling point of Al and the melting point of W are respectively about 2000°C and 3400°C in the atmosphere, the Al source evaporates without the W boat melting. In this way, Al was deposited. The schematic illustration of this deposition is shown in Fig.2.7.

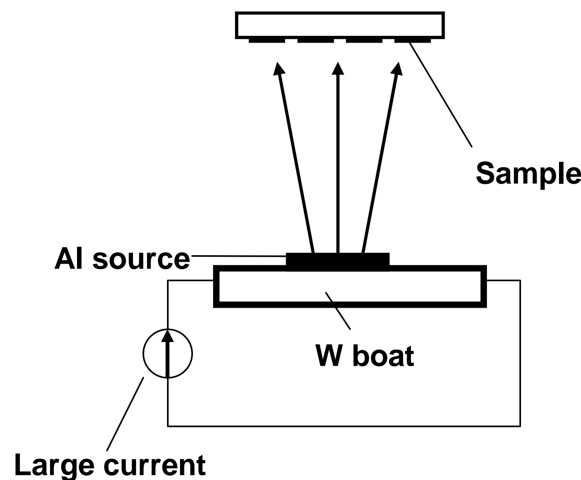

Fig.2.7 Large current is passed in the W boat. The Al source is heated and evaporate by the Joule heat. Finally, Al is deposited on the samples.

2.1.6 Effective mobility calculation by split C-V method

The effective mobility (μ_{eff}) is one of the most important electrical characteristics of MOSFETs. In order to determine the μ_{eff}, split C-V method is often used.

In the condition of the low voltage between source and drain (V_{ds}), I_{ds} can be express:

$$I_{ds} = \frac{W\mu_{eff} Q_n V_{ds}}{L}, \tag{2.1}$$

where W is the channel width, L is the channel length, Q_n is the mobile channel charge density and μ_{eff} is the effective mobility.

Eq.(2.1) can be written as

$$\mu_{eff} = \frac{g_d L}{W Q_n}, \tag{2.2}$$

by using the drain conductance (g_d) defined as

$$g_d = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{Vg=Vg'(=const.)} . \tag{2.3}$$

Q_n is also expressed by measuring the gate-to-channel capacitance (C_{gc}) as

$$Q_n = \int_{\infty}^{V_g'} C_{gc} dV_g \ . \tag{2.4}$$

In fact, Q_n in the low V_g region ($V_g < V_{fb}$) is very low and negligible. So, Eq.(2.4) can be written as

$$Q_n = \int_{V_{fb}}^{V_g'} C_{gc} dV_g \ . \tag{2.5}$$

The circuit for measuring C_{gc} is shown in Fig.2.8. It is called split C-V method.

In this study, C_{gc} was measured at 100kHz. Using Eq.(2.3) and Eq.(2.5), μ_{eff} is calculated from the slope of the I_{ds}-V_{ds} characteristic and the are of the C_{gc}-V_g characteristic as shown in Fig.2.9(a) and (b). [7]

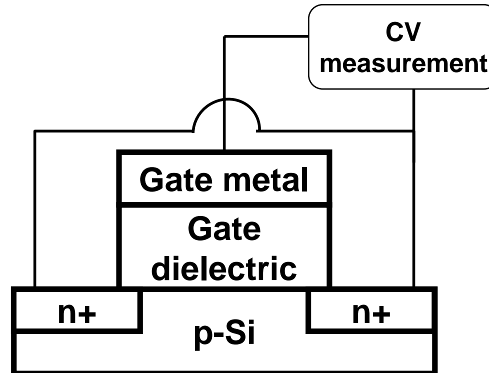

Fig.2.8 Schematic illustration of Cgc measurement.
This method is called split C-V method.

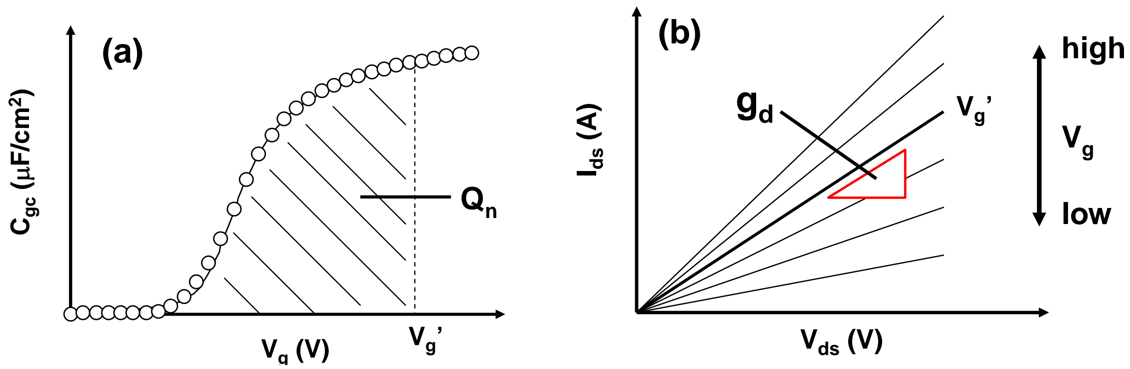

Fig.2.9(a) Q_n is obtained from C_{gc}-V_g characteristic as the area.
(b)g_d is obtained from I_{ds}-V_{ds} characteristic as the slope.

2.1.7 Subthreshold slope

Generally, I_{ds}-V_g characteristic of MOSFETs is described as Fig.2.10 and subthreshold slope (S) is defined as

$$S = \left(\frac{d(\log I_{ds})}{dV_g} \right)^{-1}, \tag{2.6}$$

where V_g is the gate voltage and satisfies the relation of $V_g < V_{th}$. So, S is one of the important characteristics of MOSFETs because it describes how MOSFETs switch on or off. [8]

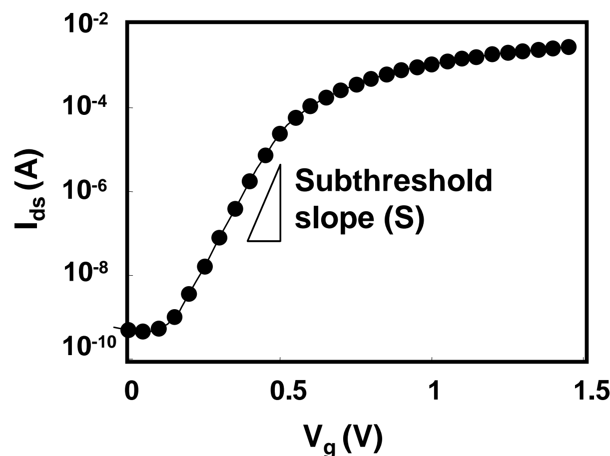

Fig.2.10 S is obtained from the slope of I_{ds}-V_g characteristic, describing how MOSFETs switch on or off.

2.1.8 Charge pumping method

D_{it} is the value of describing the interfacial state between Si-substrate and the gate dielectric. Charge pumping method is one of the most effective methods for measuring D_{it} of the MOSFETs. Considering the n-MOSFET, under the inversion condition, the electron are induced at the interface and trapped by the interfacial traps. If immediately the condition is changed to the accumulation by the high frequency pulse voltage, the holes are induced and recombine with the trapped electrons. Because of the recombination, the surface recombination leakage current is generated and this is defined as charge pumping current (I_{cp}). By measuring the I_{cp}, D_{it} is calculated. This is the charge pumping method. Fig.2.11 shows the schematic illustration of the principle of the charge pumping method. D_{it} is expressed using I_{cp}:

$$D_{it} = \frac{I_{cp}}{q \cdot f \cdot A_g}, \tag{2.7}$$

where q is electronic charge, f is the frequency of the pulse voltage and A_g is the area of the channel.[9]

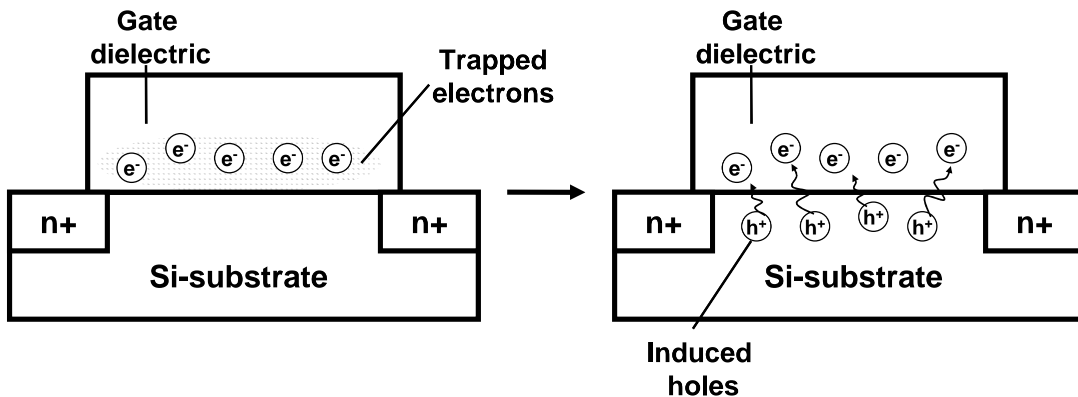

Fig.2.11Schematic illustration of the principle of the charge pumping method. Trapped electrons combines with induced holes recombine, and I_{cp} is generated.

2.2 Experimental procedure

2.2.1 Fabrication of MOS capacitor

Fig.2.12 shows the schematic illustrations of fabrication of La_2O_3-gated MOS capacitors. 300-nm-thick SiO_2 isolated n-Si (100) wafer was used for capacitor. The wafer was divided into 2 cm x 2 cm samples and the samples were used. After SPM cleaning and HF treatment, which took 10 min and 1.5 min respectively, La_2O_3 layer ranging from 2 to 4 nm were deposited by e-beam evaporation at a rate of about 0.002 nm/s. 1-nm-thick Mg layer was successively deposited on the La_2O_3 layer at the same rate as La_2O_3 layer. These layers were deposited at a pressure of 10^{-8}~10^{-7} Pa. Then, 60-nm-thick W was *in situ* deposited using RF magnetron sputtering at a rate of 2 nm/s without exposing the wafers to air in order to avoid absorbing any moisture or carbon-related contamination. Substrate temperature during the depositing was set to 300 ^{o}C. Gate metal was patterned by RIE using SF_6 chemistry to form gate electrode. PMA using a rapid thermal annealing (RTA) furnace was carried out in forming gas (F.G.) (N_2: H_2 = 97% : 3%) ambient at 500 ^{o}C for 30 min. A 50-nm-thick Al layer on the backside of the substrate was finally deposited as a bottom contact by thermal evaporation and the rate of the deposition was 0.1 nm/s.

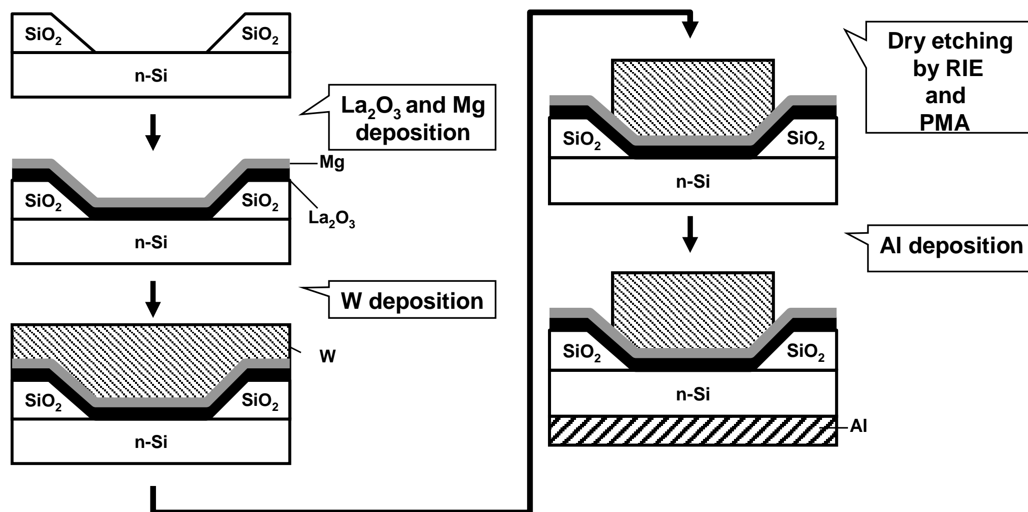

Fig.2.12Fabrication flow of W/Mg/La_2O_3/n-Si gate stack structure MOS capacitor.

2.2.2Fabrication of MOSFET

For MOSFET, local-oxidation-of–silicon (LOCOS) isolated p-Si (100) wafer with pre-formed source/drain was used. Schematic illustration of fabrication of MOSFET is shown in Fig.2.13. After SPM cleaning and HF treatment, La_2O_3 and Mg were deposited and gate metal was patterned in the same way as the fabrication process for MOS capacitors. In order to contact with source and drain, La_2O_3 and Mg layers were etched by buffered HF (BHF) and HCl. After PMA, 60-nm-thick Al layer for contact hole and 50-nm-thick Al layer on the backside of the substrate were deposited by thermal evaporation at a rate of 0.1 nm/s.

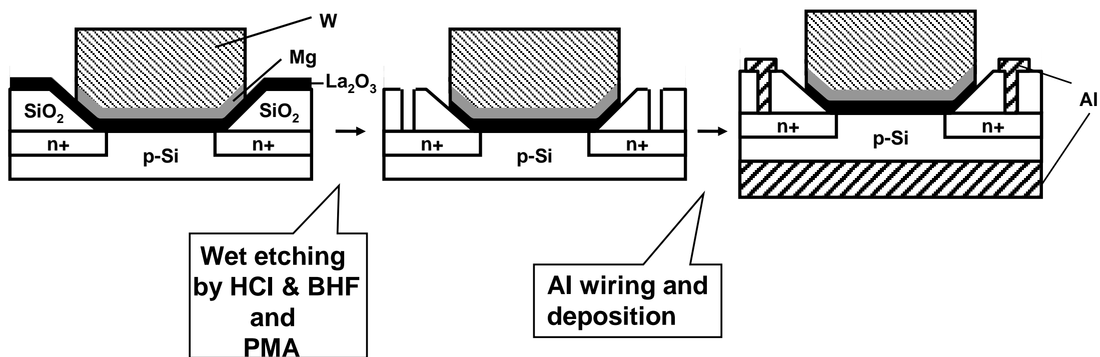

Fig.2.13 Fabrication flow of W/Mg/La_2O_3/p-Si gate stack structure MOSFET.

2.2.3 Analysis of dielectrics and measurement of electrical properties

In order to reveal the movement of incorporated Mg atoms and the condition of dielectrics after PMA, one capacitor of W/Mg/La_2O_3/p-Si gate stack structure after thermal treatment was analyzed by transmission electron microscope (TEM), energy dispersion x-ray (EDX) and hard x-ray photoemission spectroscopy (XPS). The principles of these physical analyses are described in Appendix B.

Electrical characteristics of MOS capacitors and MOSFETs were measured using an Agilent E4980A precision LCR meter and Agilent 4156C semiconductor parameter analyzer. Capacitance-voltage (C-V) characteristics were measured at 100kHz.

Both experimental procedures of MOS capacitors and MOSFETs are shown in Fig.2.14.

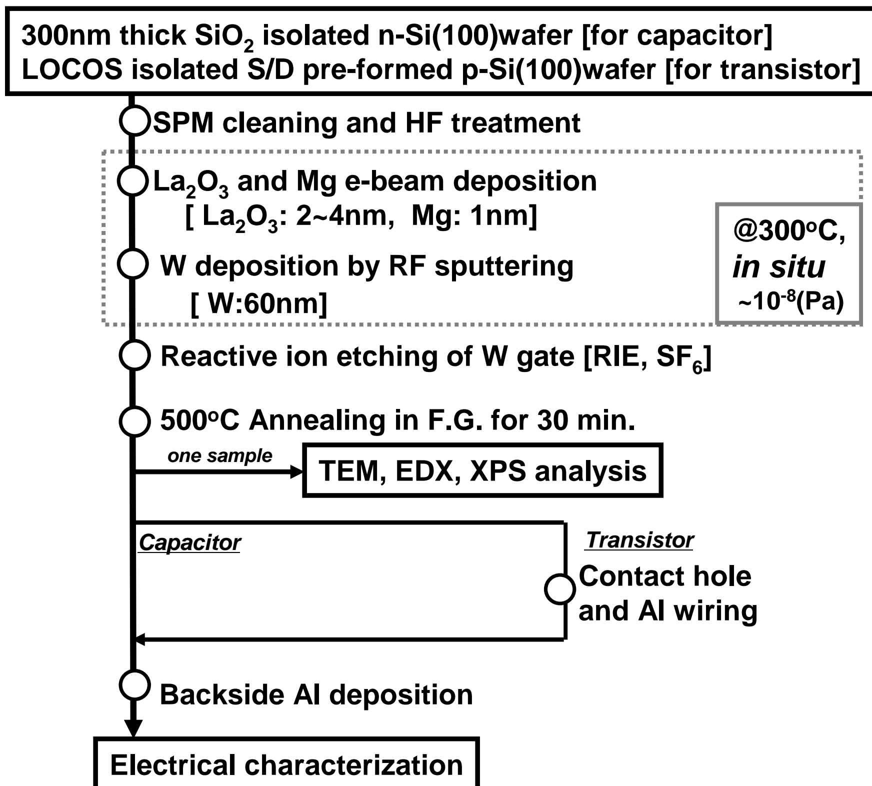

Fig.2.14 Experimental procedures of MOS capacitor and MOSFET.

3 Results and Discussion

3.1 Physical analysis of the gate dielectrics

A cross sectional TEM image and EDX line profile are shown in Fig3.1(a). From these results, the inserted Mg atoms are thought to diffuse into La_2O_3 and also to the gate W electrode by thermal treatment. Besides Mg diffusion, La_2O_3 reacted with Si-substrate to form La-silicate. The incorporated Mg was found to be in oxidized state that was indicated by the result of XPS analysis as shown in Fig.3.1(b). Fig.3.2 shows schematic illustration of the fabricated structure at as-deposited state and after PMA.

A slight increase in EOT may happen with Mg incorporation, however, considering that MgO has a k-value of 9.8[10] which is comparable to that of La-silicate and also that the incorporated amount is so small, the effect of Mg on EOT can be negligible for our case.

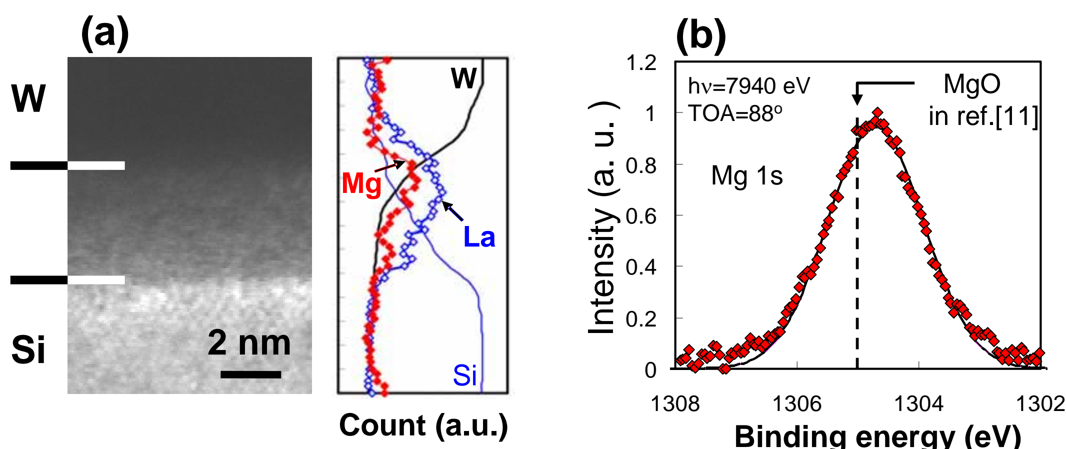

Fig.3.1(a) Cross sectional TEM image and EDX line-profile of a fabricated MOS capacitor indicates Mg and La atoms' diffusion. (b) Result of XPS analysis. The shift indicates that the incorporated Mg is oxidized.

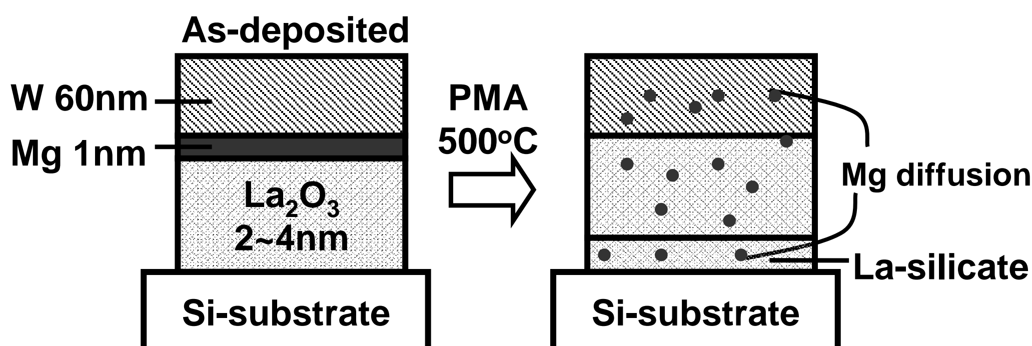

Fig.3.2 Schematic illustration of the MOS structure at as-deposited condition and after PMA.

3.2 Electrical characteristic of MOS capacitor with Mg incorporation

3.2.1 Fixed charge estimation with Mg incorporation

V_{fb} and *EOT* were taken from the *C-V* characteristics using CVC model. The dependence of V_{fb} on EOT with and without Mg incorporation is shown in fig.3.3. A negative shift in V_{fb} at EOT values below 1.7 nm is well suppressed with the use of Mg. This result indicates an effective suppression of fixed charge generation. Generally, fixed charges are considered to locate inside the high-k layer and at the interfaces. The number of fixed charges can be roughly estimated by defining a fixed charge density inside the high-k layer (ρ_{high-k}) and a fixed charge density at high-k/Si interface ($\sigma_{high-k/Si}$). Assuming that ρ_{high-k} is constant, the V_{fb} dependence on *EOT* can be

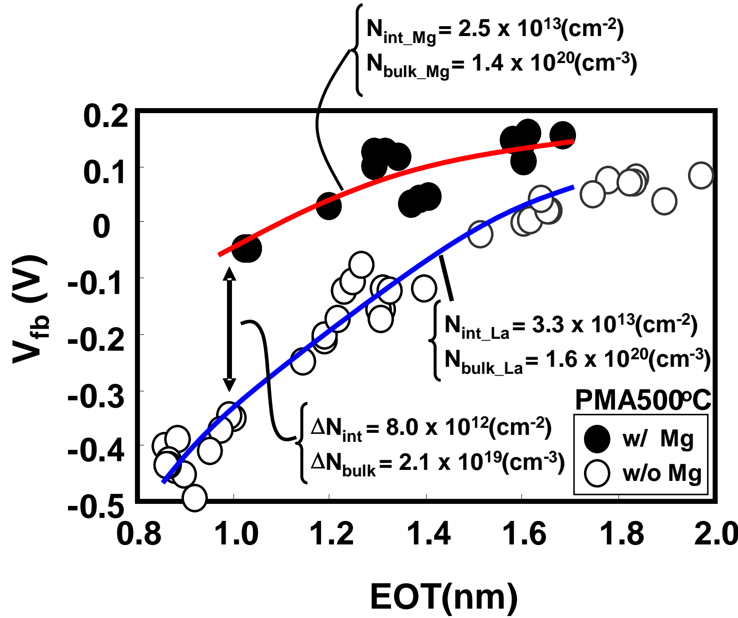

Fig.3.3 A negative shift is well suppressed with the incorporation of Mg, which indicates an effective suppression of fixed charge generation.

expressed as follows,

$$V_{fb} = -\frac{\rho_{high-k}}{2\varepsilon_{SiO2}} EOT^2 - \frac{\sigma_{high-k/Si}}{\varepsilon_{SiO2}} \cdot EOT + \phi_{ms} , \quad (3.1)$$

where ε_{SiO2} and ϕ_{ms} are the permittivity of SiO_2 and the work function difference of metal and Si substrate, respectively. Eq.(3.1) is calculated in Appendix C. Using Eq.(3.1), the numbers of interface fixed charges (N_{int}) of the capacitors with and without Mg at *EOT* below 1.7 nm can be calculated as 2.5x10^{13} cm^{-2} and 3.3x10^{13} cm^{-2}, respectively. As the same way, the numbers of fixed charges inside high-k layer (N_{bulk}) are estimated 1.4x10^{20} cm^{-3} and 1.6x10^{20} cm^{-3}. Both of the differences of 8.0x10^{12}cm^{-2} for N_{int} and 2.1x10^{19} cm^{-3} for N_{bulk} can be considered as the effect of Mg incorporation.

It can be estimated that the amount of only 0.37 % of the inserted Mg contribute to reduce the fixed charge as the inserted Mg layer thickness is 1 nm. Therefore, only small amount of Mg is required to effectively suppress the fixed charge, otherwise an excess Mg incorporation may lead to increase in *EOT*. The reduction in fixed charges at interface also can be considered as the effect of Mg that diffuse down to the interface of Si. The difference in the effective metal work function, which can be derived at the intersection point at EOT= 0 nm, may be attributed to the induced dipole formation of Mg-O-Si at the high-k/Si interface[12]. This fact may also support the diffusion of Mg to the interface.

3.2.2 EOT dependence on leakage current

Fig.3.4 shows the EOT dependence on I_{leak}. The characteristic didn't change with or without Mg incorporation. It indicates I_{leak} doesn't get worse with Mg incorporation in spite of the improvement of other electrical characteristics.

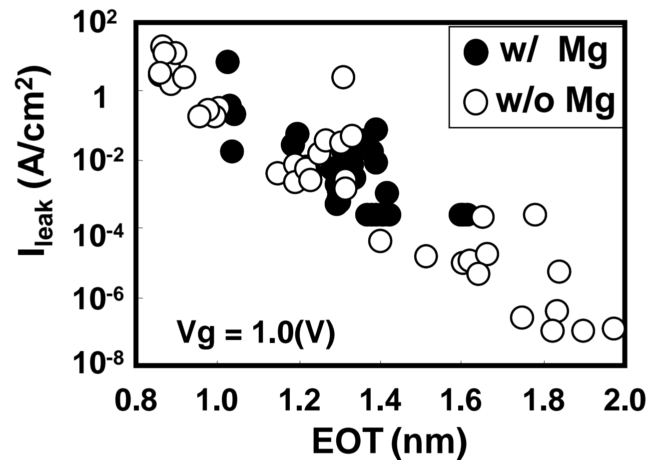

Fig3.4 The EOT dependence on I_{leak} didn't change with or without Mg incorporation.

3.2 Impact of Mg incorporation to MOSFET operation

3.2.1 Improvement of effective mobility

Fig.3.5 shows the *EOT* dependence on threshold voltage (V_{th}) of La_2O_3-gated MOSFET with and without Mg incorporation. Here, the same V_{th} trend was observed as the V_{fb} trend in capacitors and the similar effect of Mg was confirmed also with MOSFETs.

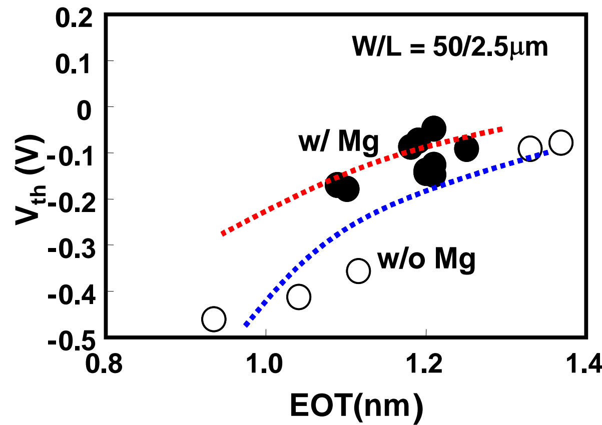

Fig.3.5The same V_{th} trend in FETs was observed as the V_{fb} trend in capacitors

μ_{eff} of the FETs was evaluated with split *C-V* technique. The μ_{eff} comparison with an *EOT* around 1.1 nm is shown in fig.3.6(a). A large improvement in μ_{eff}, especially at low effective field was observed. To analyze the additional scattering factor was performed based on Mattissen's rule as the samples have the same doping concentration. The calculated results demonstrates that the additional scattering (μ_{add}) obeys with $E_{eff}^{0.5\sim0.6}$ dependency, indicating a remote Coulomb scattering, as shown in fig.3.6(b)[13]. Therefore, the improvement in μ_{eff} can be attributed to reduced fixed charges, which is in good agreement with the V_{fb} and V_{th} shift.

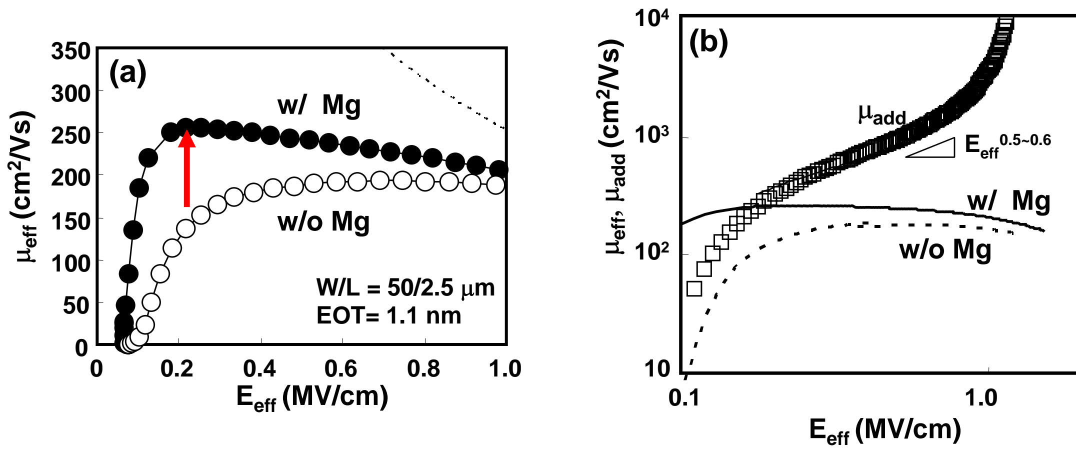

Fig.3.6(a) μ_{eff} with the same EOT around 1.1 nm. (b) Extracted μ_{add} with $E_{eff}^{0.5\sim0.6}$ dependency, indicating remote Coulomb scattering.

3.2.2 Decrease of interfacial state density

D_{it} is considered as degrading the μ_{eff} at low effective field, in other words, at low V_g region. S is also the value of at low V_g region. So, the decrease of both D_{it} and S also improve the μ_{eff} at low effective field.

Fig.3.7(a) shows the EOT dependence on S. Improvement in S especially below 1.2 nm of *EOT* was obtained. Moreover, an improvement in D_{it}, which is measured by charge pumping method, was also confirmed with Mg incorporation as shown in fig.3.7(b). Mg incorporation has a good effect on making the interfacial state better. This effect is also considered one of the causes the improvement of μ_{eff} at low effective field.

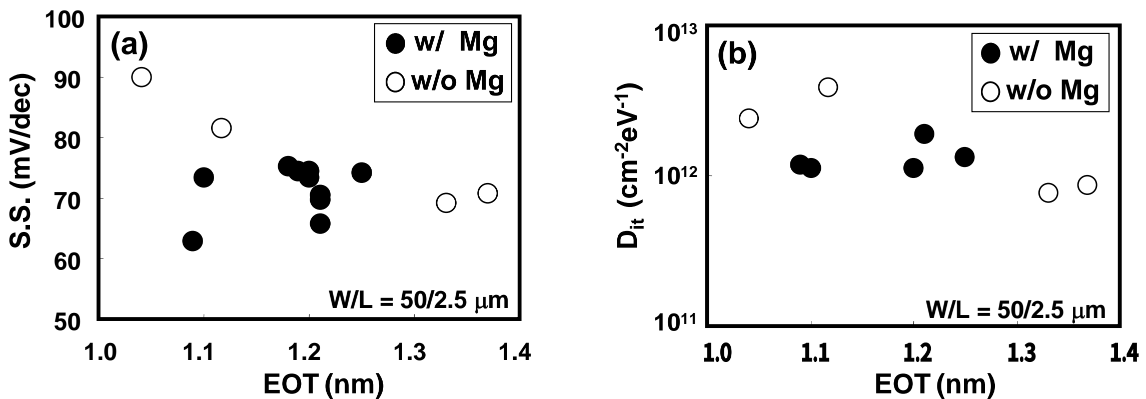

Fig.3.7(a) S.S. as a function of EOT. Improvement in S.S. below 1.2nm was also observed. (b)D_{it} degradation below 1.2 nm can be suppressed with Mg incorporation.

4 Conclusion

The effect of Mg incorporation into La_2O_3 gate dielectric has been investigated through MOS capacitors and FETs characteristics. A negative shift in flatband voltage below equivalent oxide thickness (EOT) of 1.7 nm has been well suppressed with Mg incorporation. This is attributed to the reduction of fixed charges by 24 % at Si interface. The corresponding effective mobility improvement has been confirmed at an EOT of 1.1 nm, where peak mobility increased by 25 % to $255cm^2/Vs$. Note that leakage current has not got worse with Mg incorporation. Therefore, incorporation of Mg can be regarded as a technology for further scaling in gate dielectric.

Appendices

A. I_{ds} dependence on t_{py} and k-value

When substrate doping density is low and the bulk depletion charge is neglected, I_{ds} can be expressed by using gradual channel approximation (GCA) and charge sheet model:

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} (V_g - V_{th}) \cdot V_{ds} \tag{a.1}$$

in the linear region and

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \cdot \frac{(V_g - V_{th})^2}{2} \tag{a.2}$$

in the saturation region,

where μ_{eff} is the effective mobility, C_{ox} is the capacitance of the gate dielectrics, W is the channel width, L is the channel length, V_g is the gate voltage and V_{th} is the threshold voltage. [14]

Then, C_{ox} is can be written as

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{py}} \quad , \tag{a.3}$$

where ε_0 and ε_r are vacuum permittivity and k-value respectively.

Eq.(a.1) and Eq.(a.2) are respectively expressed:

$$I_{ds} = \mu_{eff} \frac{\varepsilon_0 \varepsilon_r}{t_{py}} \cdot \frac{W}{L} (V_g - V_{th}) \cdot V_{ds} \tag{a.4}$$

and

$$I_{ds} = \mu_{eff} \frac{\varepsilon_0 \varepsilon_r}{t_{py}} \cdot \frac{W}{L} \cdot \frac{(V_g - V_{th})^2}{2} . \tag{a.5}$$

Eq.(a.4) and Eq.(a.5) mean that I_{ds} is in inverse proportion to t_{py} and in proportion to k-value.

B Physical analysis methods

B.1 The principle of TEM and EDX analysis

TEM is one of the electron microscopes. By irradiating electrons to the thin sample, some electrons are scattered and others are transmitted. Because the amount of transmitted electrons depends on the structure or component of each portion, the image is generated by the interference of the transmitted electrons. The image is observed by being magnified with the use of the coil. On the other hand, the elements composing the sample are observed by EDX. By irradiating electrons to atoms in ground state, the electron at the inner shell is exited to outside of the atom and the hole is generated at the inner shell. Other electron moves into the hole and the characteristic x-ray is emitted. Because the x-ray is peculiar to each element, the elements consisting of the sample is determined by measuring the x-ray. The analysis by TEM and EDX can be done at the same time. The schematic illustration of TEM and EDX is shown in Fig.b.1(a) and(b). [15]

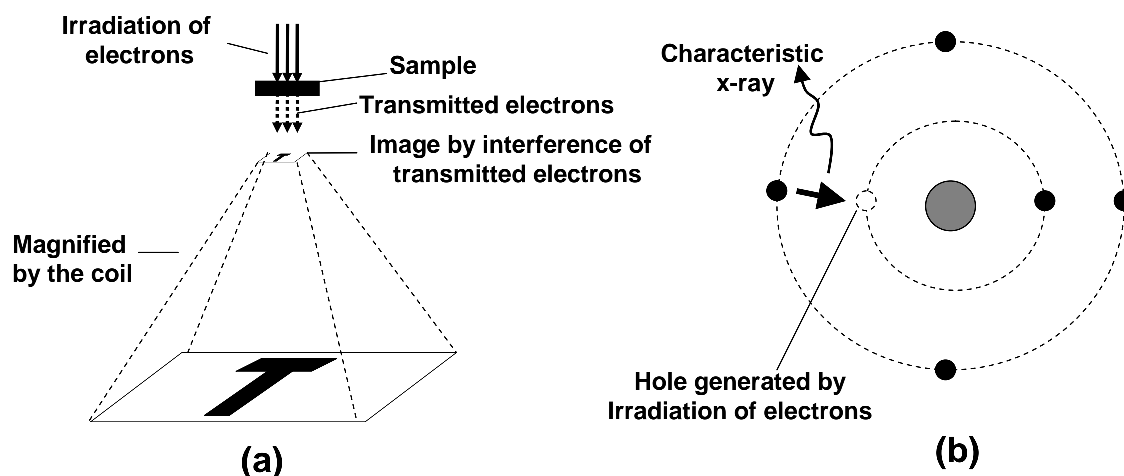

Fig.b.1(a)Magnified image is obtained by using the interference of transmitted electrons. (b) Characteristic x-ray is emitted by the transition of the electron from the outer shell to the inner.

B.2 The principle of XPS analysis

XPS is one of the most effective methods of determining the elements, which composing the sample. By irradiating x-ray to the thin sample, the electrons obtain the energy from the x-ray to be emitted with the kinetic energy. The relation of the energies can be expressed:

$$h\nu = E_k + E_b , \tag{b.1}$$

where $h\nu$ is the energy of the x-ray, E_k is the kinetic energy of the emitted electron and

E_b is the binding energy of the emitted electron. Because the value of $h\nu$ is constant, the E_b is determined by measuring the E_k as shown in Fig.b.2. The E_b is peculiar to each element and the elements consisting of the sample is also determined. [16]

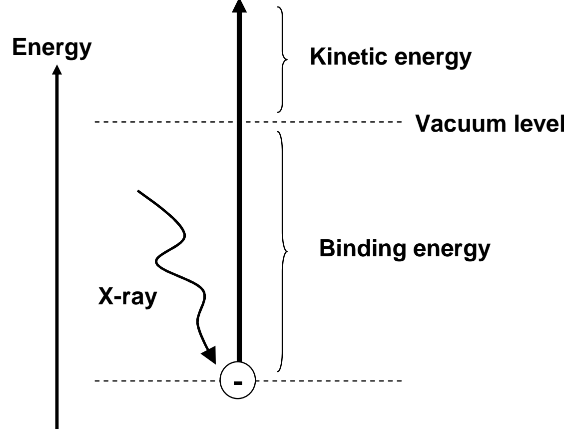

Fig.b.2 Schematic illustration of the principle of XPS. By measuring the K.E., the elements composing the sample are determined.

C V_{fb} dependence on fixed charge density and *EOT*

In order to consider the fixed charges inside the high-k layer, x is defined as shown in Fig.c.1(a) and $\rho_{bulk}(x)$, which is the density of the fixed charge at x in the high-k layer, is defined as shown in Fig.c.1(b). The increase of x is Δx and ΔV_{fb} is defined as the increase of the V_{fb}, which is required to eliminate the increase of the fixed charge ΔQ_{fix}. So, ΔQ_{fix} is expressed:

$$\Delta Q_{fix}(x) = C(x) \cdot \Delta V_{fb}, \quad \text{(c.1)}$$

where $C(x)$ is the capacitance at the point of x.

ΔQ_{fix} can be written as

$$\Delta Q_{fix}(x) = \rho_{bulk}(x) \cdot \Delta x \quad \text{(c.2)}$$

and $C(x)$ is expressed using the high-k dielectric permittivity ($\varepsilon_{high\text{-}k}$):

$$C(x) = \frac{\varepsilon_{high-k}}{x}. \quad \text{(c.3)}$$

Eq.(c.1) can be written by using Eq.(c.2) and Eq.(c.3) as

$$\Delta V_{fb} = \frac{\rho_{bulk}(x) \cdot x}{\varepsilon_{high-k}} \Delta x . \tag{c.4}$$

So, V_{fb_bulk}, which is required to eliminate the fixed charges in the high-k layer, is expressed: [17]

$$V_{fb_bulk} = \int_0^{t_{py}} \frac{\rho_{bulk}(x) \cdot x}{\varepsilon_{high-k}} dx . \tag{c.5}$$

Assuming $\rho_{bulk}(x) = \rho_{high-k} = const.$, Eq.(c.5) can be written:

$$V_{fb_bulk} = \frac{\rho_{high-k}}{2\varepsilon_{high-k}} t_{py}^{\ 2} . \tag{c.6}$$

Next, at the Si/high-k interface (at the point of $x = t_{py}$), V_{fb_int}, which is required to eliminate the fixed charges at the interface, is expressed:

$$V_{fb_int} = \frac{\sigma_{high-k/Si}}{\varepsilon_{high-k}} t_{py} , \tag{c.7}$$

where $\sigma_{high-k/Si}$ is the fixed charge density at the high-k/Si interface.

By using Eq.(1.1), Eq.(c.6) and Eq.(c.7), V_{fb} is expressed:

$$V_{fb} = -\frac{\rho_{high-k}}{2\varepsilon_{SiO2}} EOT^2 - \frac{\sigma_{high-k/Si}}{\varepsilon_{SiO2}} \cdot EOT + \phi_{ms} , \tag{c.8}$$

where ε_{SiO2} and ϕ_{ms} are the permittivity of SiO_2 and the work function difference of metal and Si substrate, respectively. Eq(c.8) is the same as Eq.(3.1).

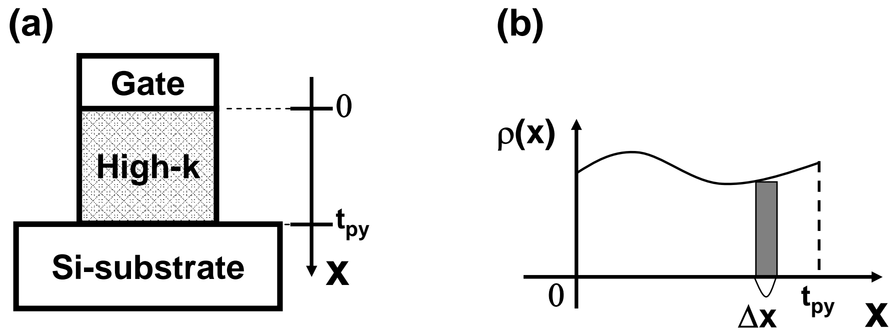

Fig.c.1(a)X is the distance from the gate metal interface.
(b)Distribution of Fixed charge density is difined.

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Tomotsune Koyanagi
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