Impact of Thin La_2O_3 Insertion for HfO_2 MOSFET

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The impact of La_2O_3 insertion for HfO_2 gated MOSFET is presented. The origin of a large negative shift in flat band voltage with La_2O_3 insertion has been carefully extracted to be the dipole presented at La_2O_3/SiO_2 interface. An improvement in effective electron mobility without degrading the interfacial state density has been performed with thin La_2O_3 insertion for HfO_2 MOSFET.

Introduction

As the scaling requires high-k material to replace the conventional SiO_2 gate dielectric, HfO_2 and its related oxides have been the major candidates to achieve equivalent oxide thickness (EOT) around 1 nm. Usually, thin layer of SiO_2 or SiON is introduced as an interfacial layer (IL) in order to improve the relatively high interface state density or degraded effective carrier mobility (1). This IL will eventually increase the EOT and there exists a limitation in terms of further scaling. On this account, new process or additional material incorporation is strongly required. Recently, La_2O_3, one of the rare earth oxides, has attracted much attention as it has wide bandgap and high dielectric constant with fairly nice interface property (2). In this paper, the impact of thin layer La_2O_3 insertion under HfO_2 layer on electrical properties of MOS capacitors and MOSFETs has been characterized.

High-k MOS Capacitor and MOSFET Fabrication

Fabrication of high-k MOS capacitor

Figure 1(a) shows the fabrication process flow of high-k gated MOS capacitors. High-k dielectrics were deposited on a 300-nm-thick SiO_2 isolated n-Si(100) wafer with thermally grown interfacial oxide layer (IL) with a thickness of 3.5 nm. HfO_2 and La_2O_3 were deposited by electron beam evaporation with O_2 partial pressure of 10^{-4} Pa. Substrate temperature during deposition was set to 300 ^{o}C and the deposition rate of high-k was controlled to be 0.3 nm/min. After high-k deposition, 60 nm-thick tungsten (W) was *in-situ* deposited using sputtering without exposing the wafers to air in order to avoid any moisture or carbon-related contamination absorption. W was patterned by reactive ion etching (RIE) using SF_6 chemistry to form gate electrode for MOS capacitors. Wafers were then post-metallization annealed (PMA) using a rapid thermal annealing (RTA) furnace in forming gas (F.G) (N_2:H_2=97%:3%) ambient at 420°C for 30 min. Backside Al was deposited as a bottom electrode by thermal evaporation. Capacitance-voltage (C-V) characteristics of MOS capacitors were measured at 100k and 1 MHz using Agilent 4284A precision LCR meter. The thickness of IL is chosen to be sufficient to avoid any

formation of oxygen vacancy in high-k. Moreover, as the annealing temperature studied in this work is below 500 ^{o}C, the Fermi level pining effect on V_{FB} can be neglected (3).

Fabrication of high-k MOSFET

For MOSFET, p-Si(100) with LOCOS isolated wafers with source/drain pre-formed substrates were used. No IL was intentionally formed before high-k deposition. HfO_2 and La_2O_3 were deposited in the same way as the MOS capacitors. For MOSFET, the annealing temperature was set to 500 ^{o}C. The process flow is shown in fig. 1(b). The electrical characteristics of the fabricated high-k gated MOSFETs were measured using Agilent 4156C semiconductor parameter analyzer.

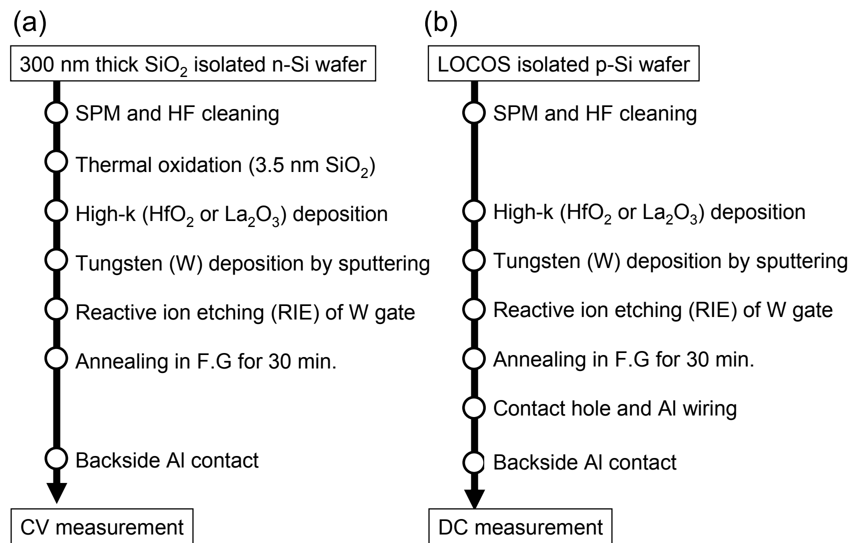

Figure 1. Fabrication process flow of high-k gated (a) MOS capacitor and (b) n-MOSFET.

Impact of La_2O_3 Insertion on Flat Band Voltage Shift of HfO_2 MOS Capacitor

Estimation of fixed charges and dipoles at each interface

Fixed charges and dipoles presented at each interface in a simple SiO_2/Si MOS structure can be expressed with equivalent oxide thickness (EOT) and flat band voltage (V_{FB}) as follows (4);

$$V_{FB} = -EOT\left(\frac{Q_0}{\varepsilon_0 \varepsilon_{ox}}\right) + \frac{\varphi_{ms}}{q} + (\Delta_{metal/SiO2} + \Delta_{SiO2/Si}), \qquad (1)$$

where Q_0 is the fixed charge presented at SiO_2/Si interface, φ_{ms} is the difference between work functions of metal and Si substrate, and $\Delta_{metal/SiO2}$ and $\Delta_{SiO2/Si}$ are the dipoles at metal/SiO_2 and SiO_2/Si interfaces, respectively. The fixed charges inside the oxide layer are neglected as the effects of these charges are small. When an interfacial layer (IL) with a thickness of EOT_{IL} is inserted under high-k oxide, then the Eq.(1) can be modified as,

$$V_{FB} = -EOT\left(\frac{Q_0 + Q_1}{\varepsilon_0 \varepsilon_{ox}}\right) + \frac{Q_1 \cdot EOT_{IL}}{\varepsilon_0 \varepsilon_{ox}} + \frac{\varphi_{ms}}{q} + (\Delta_{metal/high-k} + \Delta_{high-k/IL} + \Delta_{IL/Si}), \quad (2)$$

Here, Q_1 is the fixed charge located at high-k/SiO_2 interface and $\Delta_{metal/high-k}$ and $\Delta_{high-k/IL}$ are dipoles presented at metal/high-k and high-k/SiO_2 interfaces, respectively. A schematic model of the charge location in metal/high-k/SiO_2/Si stack is illustrated in Figure 2.

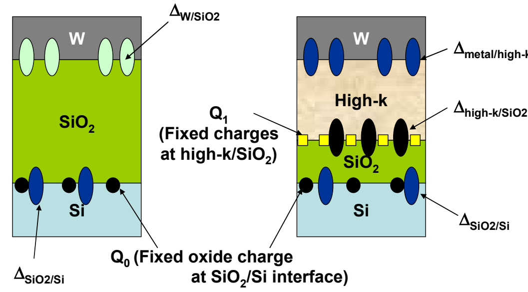

Figure 2. Schematic model of the fixed charge and dipole locations used in Eqs. (1) and (2).

Figure 3 shows the CV characteristics of MOS capacitors with different HfO_2 or La_2O_3 thickness on SiO_2 (3.5 nm) interfacial layer (IL). The thicknesses of La_2O_3 and HfO_2 vary from 5 to 10 nm. Capacitors with different SiO_2 thicknesses are also shown. It is clear that V_{FB} of the CV curves with HfO_2/SiO_2 stacks reside at positive direction compared to those of SiO_2 and La_2O_3/SiO_2 stacks. Figure 4 shows the V_{FB}-EOT plot from the obtained CV curves. Using the relation in Eq. (1), Q_0 of $-1.7x10^{12}cm^{-2}$ can be obtained by SiO_2 capacitors. Then, Q_1 for La_2O_3 and HfO_2 using Eq. (2) can be estimated to be $1.6x10^{12}$ cm^{-2} and $-2.8x10^{12}$ cm^{-2}, respectively. In this calculation, the presence of La-silicate layer, which was confirmed by transmission electron microscope (TEM) observation and X-ray photoelectron spectroscopy (XPS), was neglected as it did not show any influence on V_{FB}.

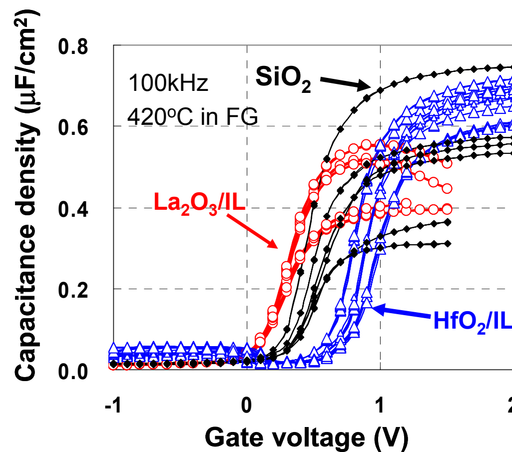

Figure 3. CV curves of HfO_2/SiO_2 and La_2O_3/SiO_2 with different thickness. Capacitors with different SiO_2 thicknesses are also shown.

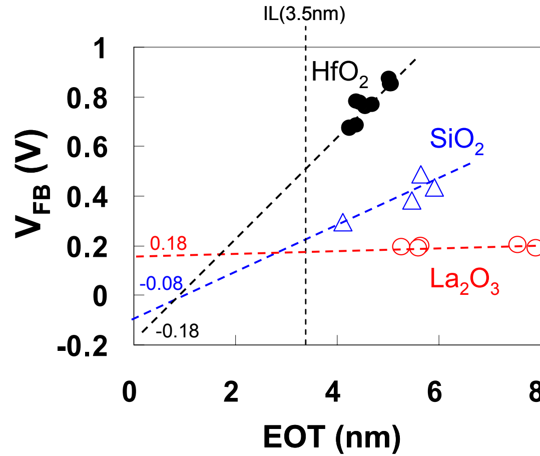

Figure 4. V_{FB}-EOT plot of the fabricated HfO_2/SiO_2 and La_2O_3/SiO_2 stacked MOS capacitors.

The difference of total dipoles between the capacitors, which is the difference between ($\Delta_{W/HfO2}+\Delta_{HfO2/IL}$) and ($\Delta_{W/La2O3}+\Delta_{La2O3/IL}$), can be calculated as 0.36 V. The dipole differences at W/high-k interface cannot be separated at this point, however, in the next sub-section, this contribution will be discussed through V_{FB} of stacked MOS capacitors.

Flat-band voltage behavior on stacked high-k MOS capacitors

To separate the contribution of metal/high-k and high-k/SiO_2, from the obtained total dipoles difference, capacitors with La_2O_3 and HfO_2 stacks with various thickness and combinations were fabricated and characterized. Figure 5 shows the schematic illustration of the fabricated MOS capacitors with high-k stacks. The total thickness of the high-k films were all set to 5 nm, in which the thickness of each layer was modified from 1 to 4 nm.

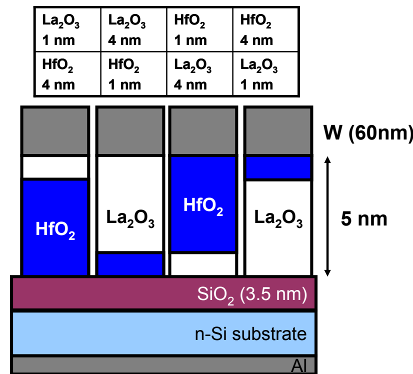

Figure 5. Schematic illustration of fabricated La_2O_3 and HfO_2 stacked MOS capacitors on SiO_2 interfacial layer.

Figure 6 shows the C-V characteristics of the stacked MOS capacitors. CV curves of HfO_2/SiO_2 and La_2O_3/SiO_2 capacitors are also shown for comparison. Capacitors with La_2O_3 on SiO_2 showed a negative shift in V_{FB}, regardless of the thickness, which corresponds to that of La_2O_3/SiO_2 capacitor. On the contrary, capacitors with HfO_2 on

SiO_2 showed a positive shift in V_{FB}, which correspond to HfO_2/SiO_2 capacitor. Therefore, it is clear that the main origin of V_{FB} shift exists at the interface of high-k/SiO_2 and the dipole differences at W/La_2O_3 and W/HfO_2 can be considered the same. Therefore, the contribution of dipoles at W/La_2O_3 or W/HfO_2 can be cancelled out in the calculation of total dipole difference. As the thickness of HfO_2 and La_2O_3 has little dependence on the shift of V_{FB}, the fixed charges or dipoles between the two high-ks, namely at the interface of La_2O_3 and HfO_2, can be ignored. Therefore, the obtained dipole difference of 0.36 V can be attributed to the difference of diploes at HfO_2/SiO_2 and La_2O_3/SiO_2.

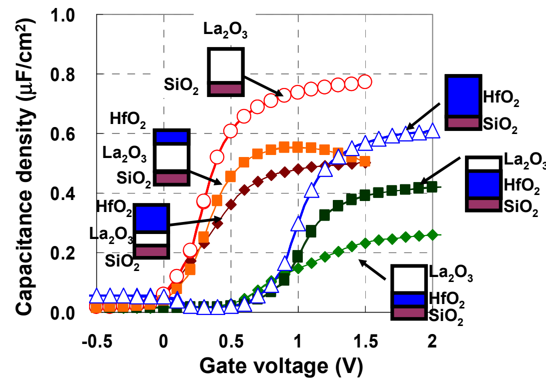

Figure 6. C-V characteristics of high-k stacked MOS capacitors on SiO_2. The V_{FB} is determined by the high-k material on SiO_2.

<u>HfO_2/SiO_2 MOS capacitors with ultra thin La_2O_3 insertion</u>

As discussed above, the high-k material on SiO_2 interface is dominant for the V_{FB}. Next, the V_{FB} shift of HfO_2/SiO_2 MOS capacitors with ultra thin La_2O_3 insertion, less than one mono layer (ML), at HfO_2/SiO_2 interface is examined. 3 samples with different La_2O_3 thickness were deposited by moving a mechanical shutter during the deposition. Then, HfO_2 with thickness of 4 nm was deposited on all capacitors at the same time. The thickness or the amount of inserted La_2O_3 was determined by TEM and XPS. The detailed measurement method is described in ref. 4. Figure 7 shows the CV curves of the fabricated capacitors with sub-ML La_2O_3 insertion at HfO_2/SiO_2 interface. HfO_2/SiO_2 and La_2O_3/SiO_2 capacitors are shown as references. By increasing the amount of La_2O_3 from 0.11 to 0.27 nm, the V_{FB} showed negative shift toward V_{FB} of La_2O_3/SiO_2 capacitor. Thus, it is clear that even an atomic insertion of La_2O_3 can largely shift the V_{FB} to negative direction.

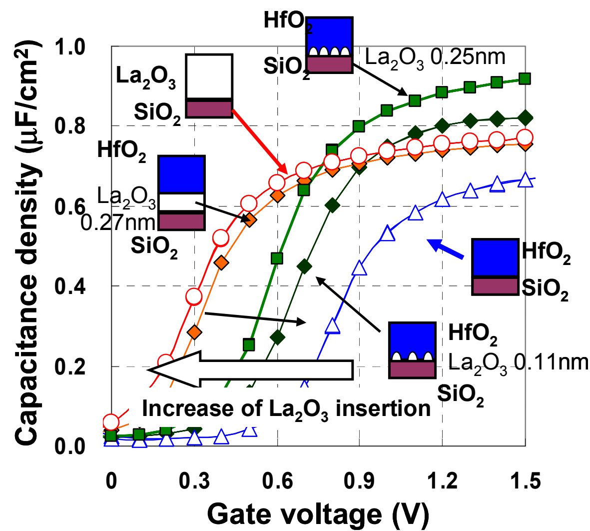

Figure 7. C-V curves of $W/HfO_2/SiO_2$ capacitors with different ultra-thin La_2O_3 insertion at HfO_2/SiO_2 interface.

Impact of La_2O_3 Insertion for HfO_2 MOSFET

The effect of thin La_2O_3 insertion for HfO_2 gated MOSFET is evaluated. La_2O_3 with thickness of 0.4, 0.8, 1.2 and 1.6 nm were fabricated by moving a mechanical shutter during the deposition with subsequent 4 nm-thick-HfO_2 deposition. In spite of different La_2O_3 insertion amount, the EOT of all samples were 1.5 nm, which is consistent with ref. 6. Id-Vg of the fabricated MOSFETs is shown in fig. 8. The threshold voltage shifted to negative direction as in the same way as the MOS capacitors, shown in the previous section. The subthreshold swings of the samples were about 70 mV/dec., and did not show any La_2O_3 insertion amount dependency.

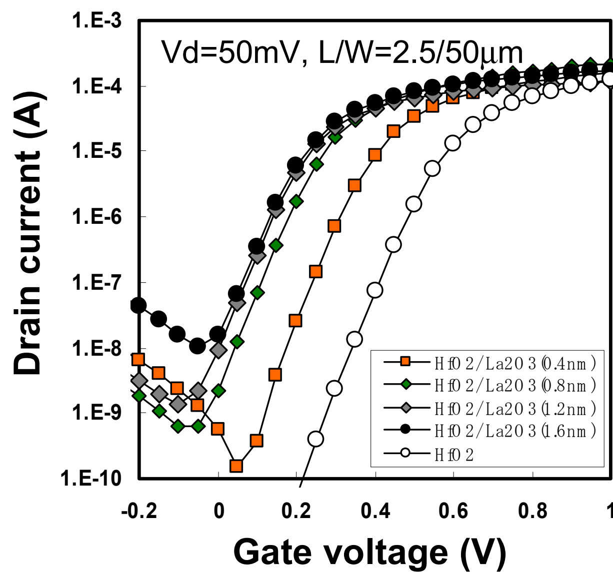

Figure 8. Id-Vg characteristics of La_2O_3 inserted HfO_2-gated MOSFETs.

The interface state densities (D_{it}) of the samples were measured by charge pumping (CP) technique. Due to large gate leakage current, CP current (I_{cp}) was extracted by subtracting two base currents measured at different frequencies (7). The obtained I_{cp} is shown in fig. 9. The D_{it} of La_2O_3 inserted HfO_2 MOSFETs were as low as $6x10^{10}$ $cm^{-2}eV^{-1}$. This D_{it} is comparable to that of HfO_2 MOSFET and is lower than that of La_2O_3 MOSFET. Therefore, thin layer of La_2O_3 insertion do not degrade the interface state.

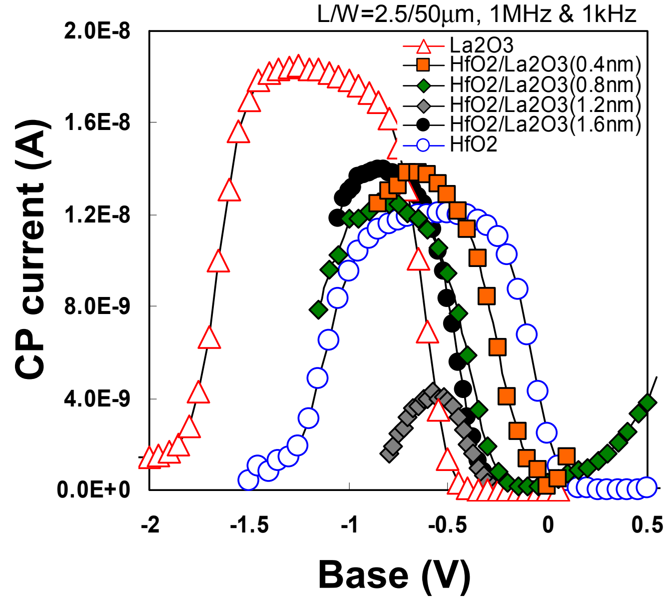

Figure 9. Charge pumping current of La_2O_3 inserted MOSFETs.

The effective electron mobility (μ_{eff}) of the fabricated MOSFET is evaluated by split-CV method(8). Figure 10 shows the calculated μ_{eff} also with HfO_2 and La_2O_3 MOSFETs, which have the same EOT of 1.5 nm. The peak mobility of La_2O_3 inserted HfO_2 varied from 250 to 300 cm^2/Vs. These values are clearly higher than that of HfO_2 gated MOSFET, which has a peak mobility of 220 cm^2/Vs. No dependency of La_2O_3 insertion amount was observed, however, it can be concluded that even a slight amount of La_2O_3 insertion can improve the mobility. The mechanism of this mobility improvement is still unclear, however, as the suppression of oxygen vacancy (V_o) formation by La incorporation in Hf-based oxide is reported (9), it can be anticipated that La atom can passivate the formed defects in HfO_2.

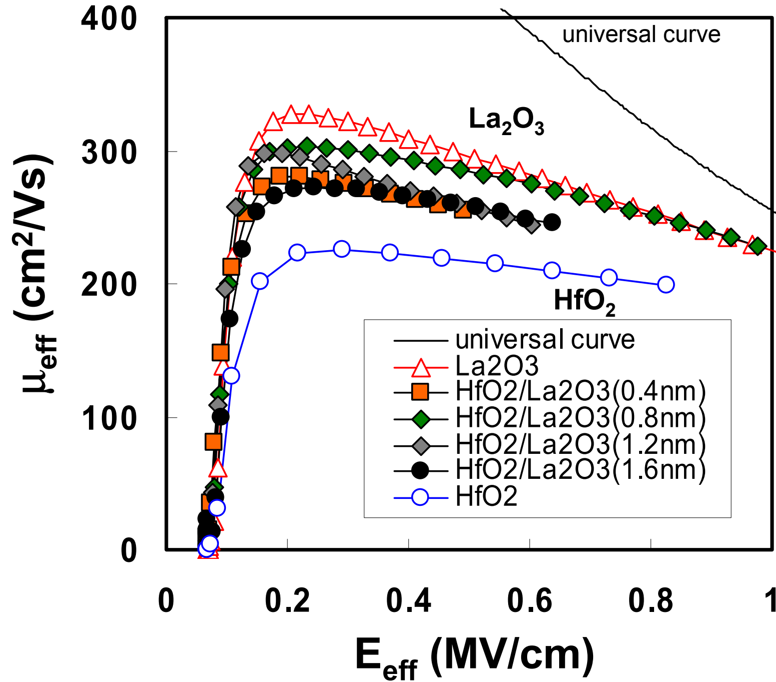

Figure 10. Effective electron mobility of La_2O_3 inserted HfO_2 MOSFET. The EOT of the samples are 1.5 nm.

Conclusion

The impact of La_2O_3 insertion for HfO_2 gated MOSFET is presented. The origin of a large negative shift in flat band voltage with La_2O_3 insertion has been carefully extracted to be the dipole presented at La_2O_3/SiO_2 or La_2O_3/substrate interface. An improvement in effective electron mobility without degrading the interfacial state density has been performed with thin La_2O_3 insertion for HfO_2 MOSFET.

Acknowledgments

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