Schottky-Barrier-Height Modulation of Ni Silicide/Si Contacts by Insertion of Thin Er or Pt Layers

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ABSTRACT

A new Schottky barrier height (Φ_b) modulation method for Ni silicide/Si contacts was proposed. A thin metal layer (Er or Pt of 0.9-3.6nm thick) was inserted between Si (100) substrate and Ni layer (100nm) before the silicidation annealing. In the case of Er insertion, the Φ_b for electrons decreased by 0.03-0.12eV in the annealing temperature range of 300-800^{o}C, compared to that of Ni silicide without the Er insertion. In the case of Pt insertion, the Φ_b for hole decreased by 0.08-0.2eV in the annealing temperature range of 300-700^{o}C. N-channel Schottky barrier source/drain MOSFETs were successfully fabricated using the Er insertion technique.

INTRODUCTION

The Schottky barrier source/drain MOSFET (SB-MOSFET) is one of the promising candidates for next generation devices, thanks to its shallow junction depth with lower electrode resistance and process temperature[1-2]. The major concern is, however, to reduce the Schottky barrier height (Φ_b) for electrons and holes, because the presence of large Φ_b severely limits the CMOS drive current [3]. Variety of silicides such as Pt silicide and Er silicide have been proposed for SB-PMOS and SB-NMOS use, and the Φ_b of 0.15-0.27eV in SB-PMOS using Pt silicide and that of 0.27-0.36 eV in SB-NMOS using Er silicide were reported [4]. Reports on middle gap materials such as NiSi and $CoSi_2$ also showed that the great possibility of those materials for applications of the SB-MOSFETs by employing Schottky-barrier-height modulation techniques [3].

In this paper, we report a new Schottky-barrier-height modulation method for Ni silicide by inserting a thin Er or Pt interlayer before silicidation process.

EXPERIMENTAL

Schottky diodes were formed on SiO_2 isolated n- and p-type bulk (100) Si wafers (doping concentration: 1.0×10^{15} cm^{-3}), as shown in Fig. 1. Before metal deposition, the patterned wafers were cleaned in mixed solution of H_2SO_4 and H_2O_2 followed by

chemical oxide removal by diluted HF. Metals were deposited subsequently by DC sputtering in Ar gas at a pressure of 5.0×10^{-1} Pa. The layered structures of Ni/Pt/Si and Ni/Er/Si with 100-nm-thick Ni layer and the Pt or Er layer thicknesses ranging from 0.9 to 3.6 nm were deposited. Ni (100 nm)/Si, Er (100 nm)/Si and Pt (100 nm)/Si structures were also deposited as references. The samples were annealed in forming gas (3% H_2 + N_2) at various temperatures from 300°C to 800°C for 1 min. After the removal of un-reacted metals by chemical etching, Al back contacts were formed by thermal evaporation. The Schottky barrier heights of the fabricated diodes were evaluated form current voltage characteristics. The structures of the formed silicide films were also analyzed by transmission electron microscope (TEM), energy dispersive X-ray spectroscopy (EDX) and Rutherford backscattering spectroscopy (RBS).

The back gate type N-channel SB-MOSFETs were also fabricated on boron-doped (1.0×10^{15} cm^{-3}) p-type silicon on insulator (SOI) wafers (SOI thickness: 40nm), as shown in Fig. 2. The buried oxide (BOX) layer of 140-nm-thick SiO_2 in the SOI structure was used as the gate oxide. Active regions were defined by lithography and reactive ion etching. Channel regions were covered with a 10-nm-thick thermal-oxide layer by the rapid thermal annealing in 5% O_2 at 1000°C for 9 min. Er and Ni layers of 3.6 and 100 nm thick, respectively, were subsequently deposited by DC sputtering in the same way as that described above. Then the samples were annealed in forming gas (3% H_2 + N_2) at 300°C for 1min. After the removal of un-reacted metals, Al back contacts were formed for a gate electrode.

RESULTS AND DISCUSSION

Typical current-voltage (*I-V*) curves of Schottky diodes fabricated from the Ni/Er/p-Si and Ni/Pt/n-Si structures are shown in Fig. 3(a) and (b). Φ_b was evaluated from the *I-V* curves in the forward bias region. The obtained Φ_b values are plotted against the annealing temperatures in Fig. 4.

In the case of the Er insertion, observed Φ_b values for holes were higher by 0.03-0.12eV from the value for the Ni silicide without the Er insertion, in the annealing temperature range of 300-700°C as shown Fig. 4(a). This means that the Er insertion is favorable for n-type MOSFETs because the Φ_b for electrons can be lowered. The values of Φ_b depended on the annealing temperature while not on the inserted Er thickness. EDX analysis revealed that an Er silicide layer was formed at the surface, while small amount of Er was incorporated in the entire NiSi layer, after the annealing at 500°C.

In the case of Pt insertion, observed Φ_b values for electrons were higher by 0.08-0.2eV from the value for Ni Silicide without the Pt insertion, in the annealing temperature range of 300-700°C as shown Fig. 4(b). This means that the Pt insertion is favorable for p-type MOSFETs because the Φ_b for holes can be lowered. RBS analysis revealed that most of the Pt remained at the Ni Silicide/Si interface, after the annealing at 500°C.

The remained Pt and Er at the Ni silicide/Si interface might contribute to the Φ_b modulation for both cases although the properties of segregation are apparently different in the Er inserted case and Pt inserted case.

Fig. 5(a) and (b) show I_D-V_G and I_D-V_D characteristics of the fabricated n-type SB-MOSFET with 20 μm channel length. Because the 140-nm-thick SiO_2 BOX layer was used as the gate oxide, the obtained value of subthreshold slope was 235 mV/dec.

This high value of subthreshold slope may improved by reducing the gate oxide thickness.

CONCLUSION

We have proposed a new Φ_b modulation method for Ni silicide by inserting Er or Pt layer to Ni/Si interface. The Φ_b modulation of 0.03-0.12eV lowering for electrons and 0.08-0.2eV lowering for holes by the Er insertion and Pt insertion, respectively, was performed. The modified values of Φ_b were insensitive to variation of the annealing temperatures employed in the experiments. N-type Schottky barrier source/drain MOSFET was successfully fabricated using Er insertion technique

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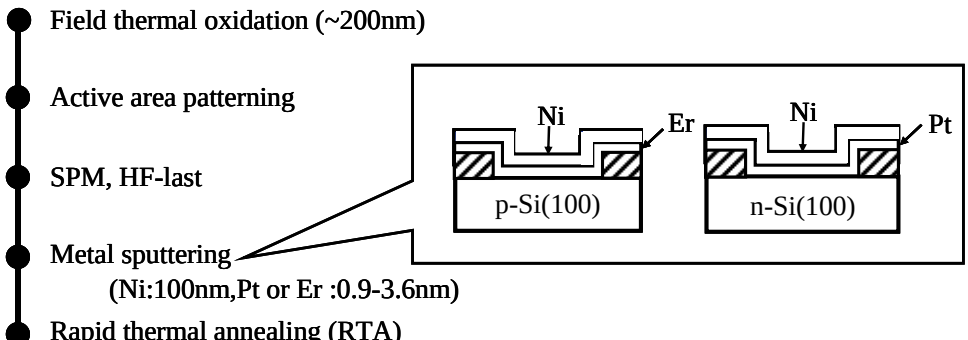

Fig.1 Fabrication process of the Schottky barrier diodes from the initial structures of Ni/Er/p-Si and Ni/Pt/n-Si.

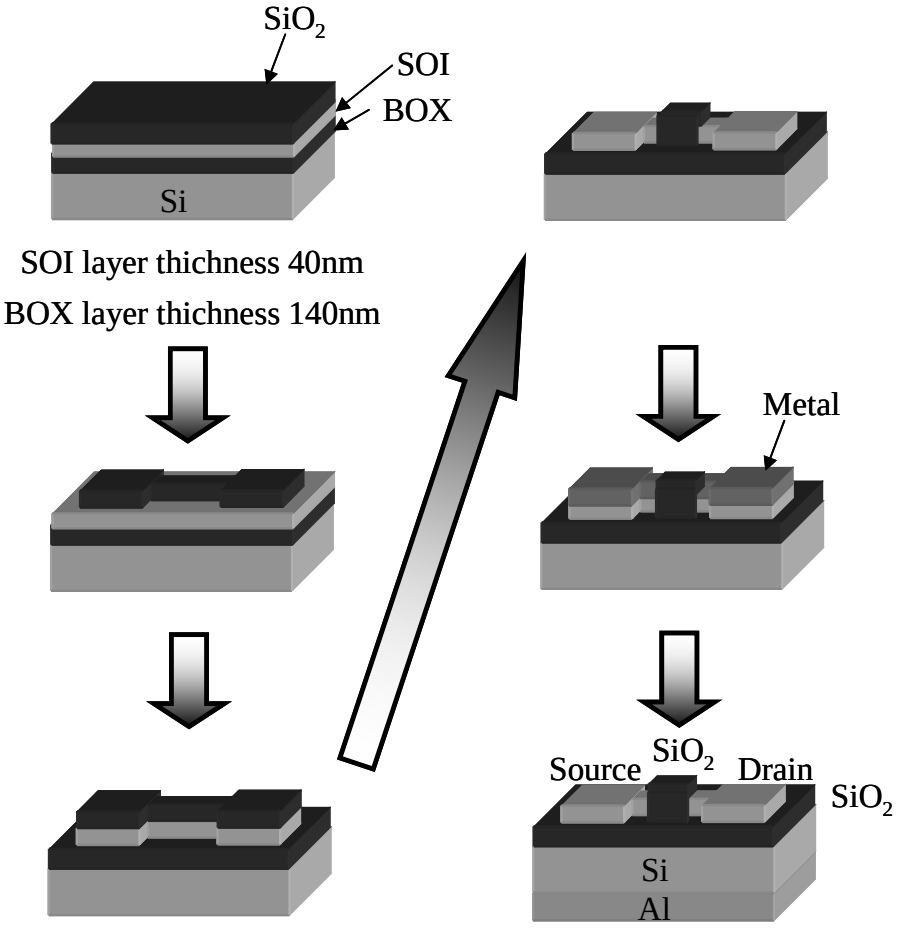

Fig.2 Schematic illustration of fabricated N-channel SB-MOSFET.

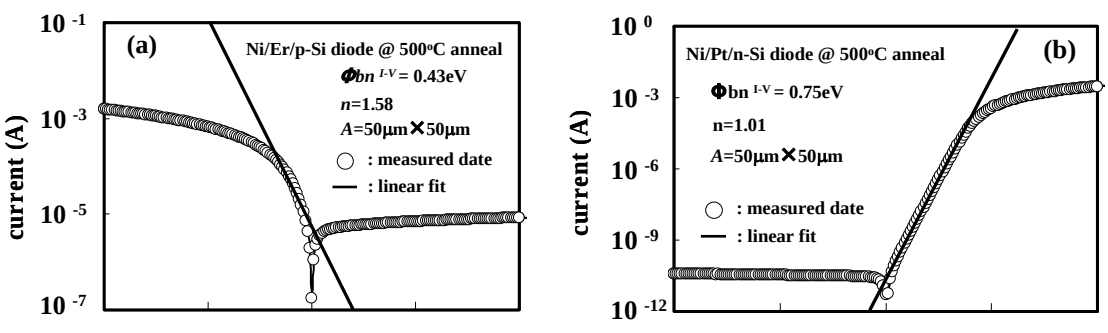

Fig.3 Current-voltage (*I-V*) characteristics of Schottky diodes formed from the initial structures of (a) Ni/Er(3.6 nm)/p-Si and (b) Ni/Pt(3.6 nm)/n-Si.

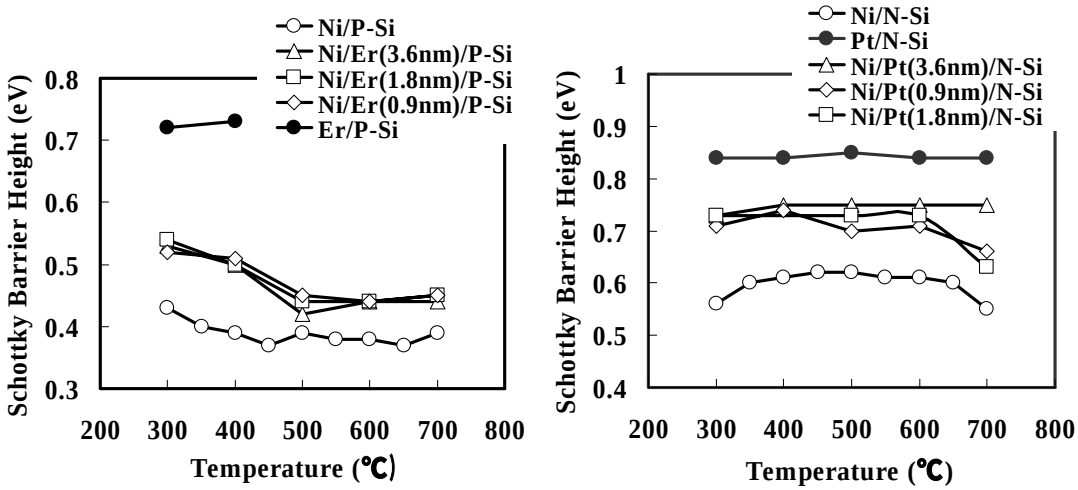

Fig.4 Annealing temperatures dependence of Schottky barrier heights for the diodes formed from the initial structures of Ni/Er/p-Si and Ni/Pt/n-Si with various thicknesses of Er or Pt layers.

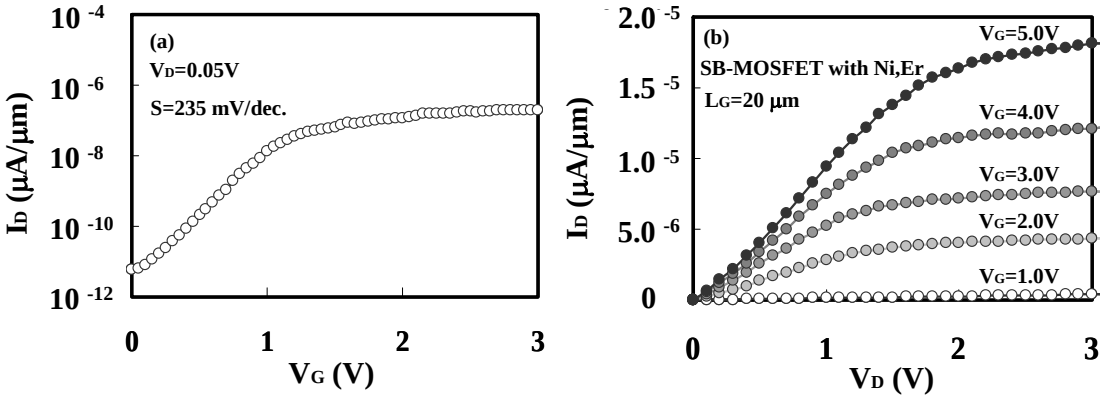

Fig. 6 (a)I_D-V_G and (b)I_D-V_D characteristics of the fabricated N-channel SB-MOSFET.