Improvement of interfacial properties with interfacial layer in La_2O_3/Ge Structure

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Abstract

The electrical characteristics and interfacial properties of La_2O_3/Ge structures under various post-deposition annealing (PDA) conditions are studied. We found that the interfacial Ge oxide layer reduced the D_{it}, while redundant growth of the oxide led to increment of CET. In order to satisfy small CET and low D_{it}, appropriate interfacial layer (IL) thickness is assumed to be 1.0-1.5 nm. On the other hand, Ge sub-oxide in the IL caused to increase hysteresis. Instead, by introducing the Ge chemical oxide, an interfacial La-germanate layer formed with PDA at 500 °C in N_2, which could reduced both the hysteresis and D_{it}.

Keywords: high-k; lanthanum oxide; La_2O_3; germanium; interface trap density; germanate, PDA

1. Introduction

As the scaling of silicon metal-oxide-semiconductor field-effect transistor (MOSFET) reaches its fundamental limits, germanium has drawn high attention for high performance applications thanks to its high mobility. However, due to the thermally unstable and water soluble properties of Ge oxide, it seems difficult to obtain better device characteristics in GeO_2/Ge structure compared to SiO_2/Si. On the other hand, in order to achieve smaller equivalent oxide thickness (EOT) without increasing the leakage current, high dielectric constant (high-k) materials are required for gate insulator of Si MOSFET. With recent development of high-k dielectric film formation, high-k materials such as ZrO_2, Al_2O_3, HfO_2 and HfO_xN_y have been also studied for gate insulator of Ge MOSFETs [1-3]. In many high-k materials, La_2O_3 which possesses high dielectric constant (~27) and large band-gap [4] is more attractive than other high-k materials for gate insulator, and it has been extensively studied on Si

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substrates [4-7]. In case of La_2O_3/Si structure, trapped charges at the La_2O_3/Si interface degrade effective mobility [7]. In this work, we report the improvement of interfacial properties with interfacial layer in La_2O_3/Ge structures.

2. Experiments

Ge-MOS structures were fabricated on n-type Ge (100) wafers with resistivity of 1.9~2.4 Ω-cm. Ge native oxide was removed by dipping in an HCl/H_2O (1/4) solution followed by rinsing in de-ionized water. After that a protective Ge Oxide layer was formed by $NH_4OH/H_2O_2/H_2O$ (1/2/20) treatment [8]. The protective Ge oxide was removed by annealing at 600°C in ultra-high vacuum (UHV) chamber. La_2O_3 films were deposited by electron-beam (E-beam) evaporation under pressure of ~1×10^{-6} Pa at substrate temperature of 250 ^{o}C in the same UHV chamber. After the deposition, post-deposition annealing (PDA) was carried out under various annealing conditions. Pt was used as a gate electrode. Interface trap density (D_{it}) was evaluated by conductance method [9]. The physical thicknesses were optically measured by spectroscopic ellipsometry (SE) using a Cauchy model and a single layer approximation with variable refractive index. High resolution transmission electron microscopy (HR-TEM) and x-ray photoelectron spectroscopy (XPS) were performed for structural and chemical analyses.

3. Results and Discussion

3.1 PDA in oxygen ambient

Figure 1 shows (a) 100kHz C-V characteristic and (b) D_{it} for Pt/La_2O_3/Ge MOS structure with PDA in N_2, 3%-H_2+N_2 (FG) or 5%-O_2+N_2 ambient at 425 ^{o}C for 30 minutes. A bulky hump was observed on the C-V curves for the samples with the N_2 and FG PDA, while little hump appeared for the 5%-O_2+N_2 PDA. The bulky hump of the N_2 and FG PDA samples could be observed due to the large amounts of interface trap density as shown in Fig. 1-(b). Figure 2 shows Ge3d spectra obtained by XPS, in which peak deconvolution was carried out using four Ge sub-oxide peaks [10]. Ge oxide components (GeO_x), especially Ge^{3+}, increased with the 5%-O_2+N_2 PDA. The GeO_x is determined to be located at the interface between La_2O_3 and Ge substrate considering the results obtained by angle-resolved analysis (inset of Fig. 2). It is assumed that the grown GeO_x layer decrease the amount of the hump on the C-V curves and interface trap density as shown below.

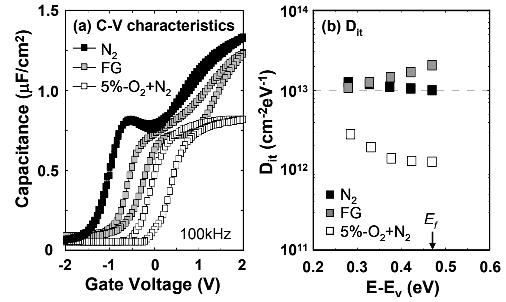


Fig.1. (a)100kHz C-V characteristics and (b)D_{it} of Pt/La_2O_3/Ge structures with PDA in N_2, FG or 5%-O_2+N_2 ambient at 425 ^{o}C for 30 minutes. D_{it} was evaluated by conductance method [9].

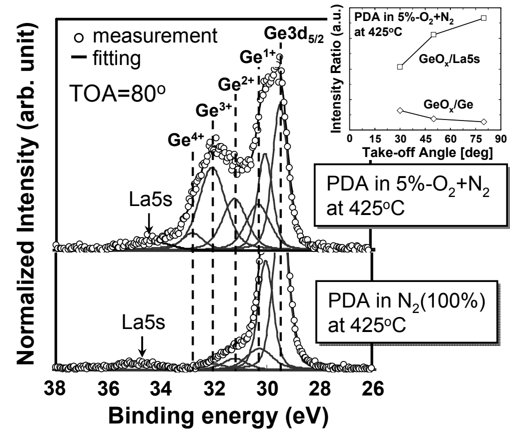


Fig.2. Deconvoluted XPS spectra of Ge3d for the samples with PDA in 5%-O_2+N_2 and N_2 at 425 ^{o}C for 5 minutes. The intensity ratio of GeO_x/La5s and GeO_x/Ge against take-off angle (TOA) is shown in the inset.

In order to control the thickness of the interfacial layer (IL), PDA was carried out in 5%-O_2+N_2 at various temperatures and durations. Fig. 3 shows D_{it} and physical thickness for samples with PDA in 5%-O_2+N_2 at 400-500 ^{o}C for 5 minutes. Higher annealing temperature induced the physical thickness increment due to the IL formation, while improvement in D_{it} was observed. The growth of the IL, which was confirmed by HR-TEM (in Fig. 4), seems effectively

to suppress the D_{it}. Changing the duration of annealing at 425 °C in 5%-O_2+N_2 could also change the IL thickness. Figure 4 shows D_{it} and CET change as a function of the IL thickness estimated by SE and HR-TEM. The samples were either annealed at various temperatures for 5 minutes or various durations at 425 °C. The dielectric constant of the IL calculated from the plot of total CET versus IL thickness was 5.8, while the dielectric constant of La_2O_3 calculated from the plot of CET versus La_2O_3 thickness [11] (not shown) was about 18-19. In order to obtain both small CET and D_{it}, appropriate IL thickness is estimated to be 1.0-1.5 nm. The leakage current density with this IL was ~1x10^{-4} A/cm^2 at 1 V.

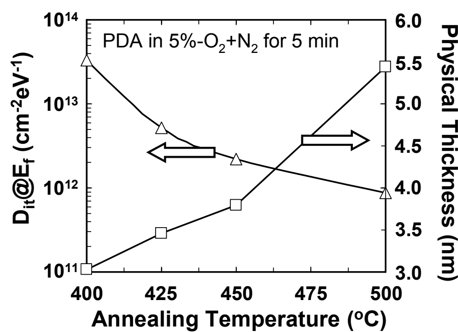


Fig.3. Interface trap density (D_{it}) and physical thickness change against annealing temperature.

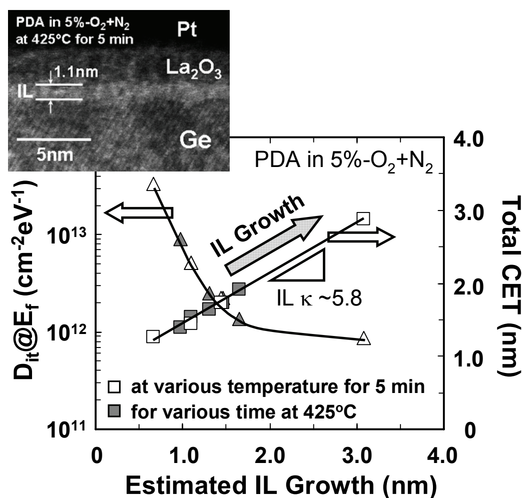


Fig.4. D_{it} and total CET change against IL thickness. The IL thickness was estimated from HR-TEM for the sample with PDA in 5%-O_2+N_2 at 425 °C for 5 min and SE results as shown in Fig. 3.

3.2 Introduction of chemical oxide IL

The large hysteresis was observed for the sample with PDA in 5%-O_2+N_2 as shown in Fig. 1. This hysteresis could be generated by the growth of Ge sub-oxide as shown in Fig. 2 [12]. In order to examine the effect of interfacial Ge oxide layer with little amount of sub-oxide, a Ge chemical oxide (CO) layer was formed with H_2O_2 solution before the La_2O_3 deposition. The thickness of the CO layer measured by SE was 1.3-1.5 nm. A La_2O_3 layer of 10.2 nm was deposited at room temperature below the sublimation temperature of CO that is considered to be 150 °C in the UHV chamber. Figure 5 shows hysteresis and D_{it} obtained by various annealing conditions with and without the CO layer. Although little difference was observed at as-deposited state, samples with the CO layer showed significant improvement after PDA. The smallest hysteresis with low D_{it} was achieved by PDA in N_2 at 500 °C with the CO layer.

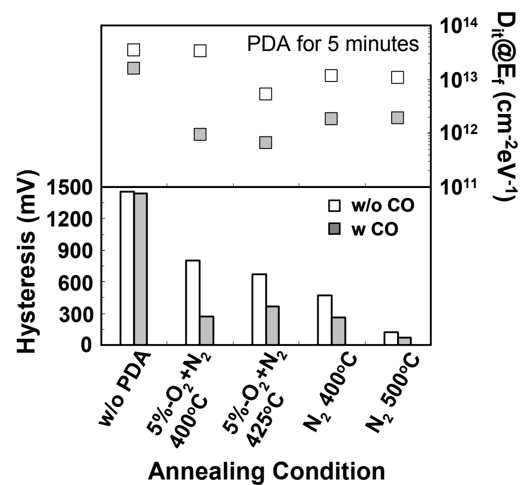
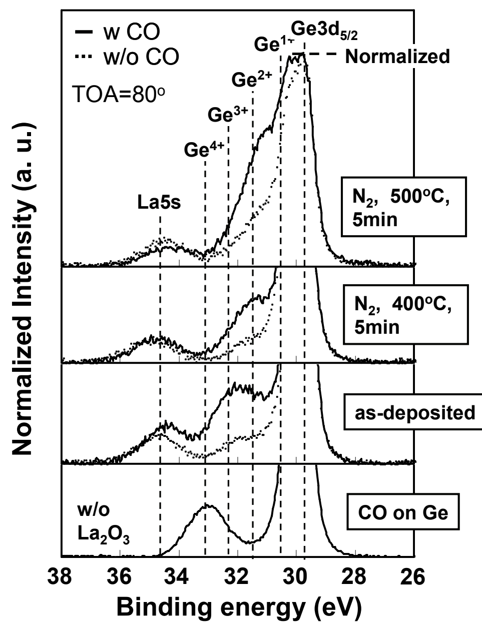


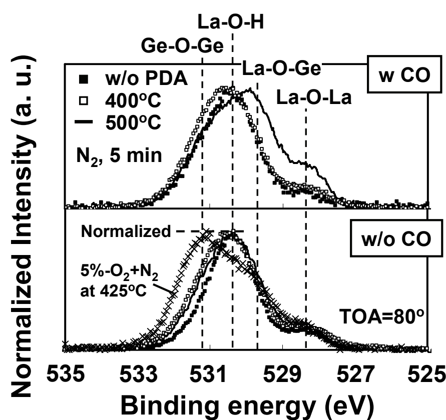
Fig.5. Hysteresis and D_{it} on various annealing condition with and without CO layer. Hysteresis and D_{it} significantly reduced with CO layer.

Figure 6 shows XPS spectra of (a) Ge3d and (b) O1s in samples with and without the CO layer. As shown in Fig. 6-(a), the chemically formed GeO_2 showed single peak of Ge^{4+}, however, various sub-oxide signals were detected after La_2O_3 deposition in samples with the CO layer. Furthermore, PDA treatment eliminated the GeO_2 component

completely so as to form sub-oxide. On the O1s spectra, an extra peak with binding energy of 529.6 eV was observed after the 500 °C PDA with the CO layer, suggesting the formation of La-germanate. Therefore, the formation of La-germanate, which appeared as sub-oxide in Ge spectra, can effectively improve both the D_{it} and hysteresis.



(a) Ge3d spectra



(b) O1s spectra

Fig.6. XPS spectra of (a) Ge3d and (b) O1s for samples with and without CO layer. PDA was conducted in N_2 at 400-500 °C for 5 minutes.

4. Conclusion

We have studied the electrical characteristics and interfacial properties of the La_2O_3/Ge structures under various annealing conditions. The interfacial layer grown by PDA in oxidation ambient could reduce the D_{it}, however, simultaneously grown Ge sub-oxide became the origin of hysteresis. By using the interfacial chemical oxide layer with the proper annealing, both hysteresis and D_{it} reduced. This would be attributed to the formation of La-germanate at the interface of La_2O_3 and Ge substrate.

Acknowledgements

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