Improvement of Interface Properties of W/La_2O_3/Si MOS Structure Using Al Capping Layer

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Electrical characteristics of W/La_2O_3/Si MOS capacitors have been investigated under various annealing condition. Relatively high interface state densities (D_{it}) of 10^{12} $cm^{-2}eV^{-1}$ observed after annealing at 200 to 500 ^oC was effectively reduced down to 10^{11} $cm^{-2}eV^{-1}$ by using an Al capping layer in the annealing process. However, a trade off between high capacitance density and low D_{it} has been observed in this method.

Introduction

Metal oxide semiconductor field effect transistors (MOSFETs) which are the core of semiconductor integrated circuits have been advanced by the scaling. Currently, downsizing of the gate length has reached 32 nm, and the physical thickness of the silicon oxy-nitride (SiON) gate dielectric has become 1.2 nm, which corresponds to three atomic layers of Si (1). Therefore, the scaling of the gate dielectric will firstly reach its critical limit, where the gate leakage currents by tunneling through the thin SiON layer increases exponentially. As a solution of the problem, introduction of new dielectric materials with higher dielectric constant (high-k) having the identical equivalent oxide thickness (EOT) is promising because of their thicker physical thickness. The exploration of the high-k materials for gate dielectric has been continued for more than ten years worldwide. Up to now, hafnium dioxides (HfO_2) exhibits superior characteristics in the EOT range around 1 nm among various high-*k* dielectrics (2). However, it has been revealed that HfO_2 film need to be mixed with Si and that insertion of a thin SiO_2 or SiON layer (0.5 ~ 0.7 nm) between the high-k film and Si substrate is necessary in order to satisfy the requirements of high-temperature-process endurance and relatively high carrier mobility (3). Consequently, the lower limit of EOT is estimated to be about 0.8 nm as far as using this structure. In the future generation in which EOT less than 0.8 nm is required, it is necessary to direct contact of high-k layer with Si substrate without any Si-oxide based interfacial layer.

We have focused on Lanthanum (La) –based oxide as a candidate of new high-k dielectric, which is expected to realize EOT less than 0.8 nm. Lanthanum oxide (La_2O_3) is known to have high *k* value of ~27 and wide band-gap of ~5.5 eV (4). The main issues of La_2O_3 to be solved are thermal stability for high temperature annealing which increases the interfacial state density, and hygroscopic properties which lowers the dielectric constant. In this paper, we demonstrate firstly that EOT of 0.8 nm or less is achievable with W/La_2O_3/Si MOS structure using the *in situ* deposition process. And

secondly, decrease in interface state density (D_{it}) by using Aluminum (Al) capping layer in the annealing process is discussed.

Experiment

Figure 1 summarizes device fabrication flow of La_2O_3 MOS-capacitors. La_2O_3 MOS capacitors were fabricated on n-type (100)-oriented 2-5 Ω-cm Si substrates. To determine the capacitor area and to avoid unexpected peripheral water absorption, a 200 nm-thick thermal oxide layer was formed and active areas were patterned by photolithography. The wafers were then cleaned by a mixture of H_2SO_4/H_2O_2 at 85 ^oC for 5 min to remove all the resist-related organic contamination, followed by diluted HF cleaning. Thin film of La_2O_3 was deposited by e-beam evaporation method from a La_2O_3 pressed target in an ultra-high vacuum chamber whose base pressure was 10^{-6} Pa. For all the samples, the substrate temperature during the deposition was kept at 300 ^oC by infrared heater and the deposition rate was 0.5 nm/min controlled by quartz thickness monitor. To avoid the water absorption to the La_2O_3 film, tungsten (W) layer of 60 nm in thickness was deposited *in situ* on the La_2O_3 film by RF sputtering with power of 150 W. For some samples, an Al capping layer was evaporated *ex situ* on the W layer. Electrodes of W or Al/W were lithographically patterned to form MOS capacitors. Post metallization annealing (PMA) was carried out for 30 minutes in either N_2 or the forming gas (H_2 3%+N_2 97%) ambient.

Capacitance-voltage (*C-V*) and current density-voltage (*J-V*) measurements have been performed using Agilent 4284A multi-frequency LCR meter and Agilent 4156C semiconductor parameter analyzer, respectively. EOT and flat-band voltage (V_{FB}) have been extracted from the *C-V* data using the NCSU CVC modeling program (5). The *C-V* data measured at 1 kHz to 1 MHz were obtained from 20 μm x 20 μm square capacitors, and the *J-V* data were obtained from 10 μm x 10 μm square capacitors.

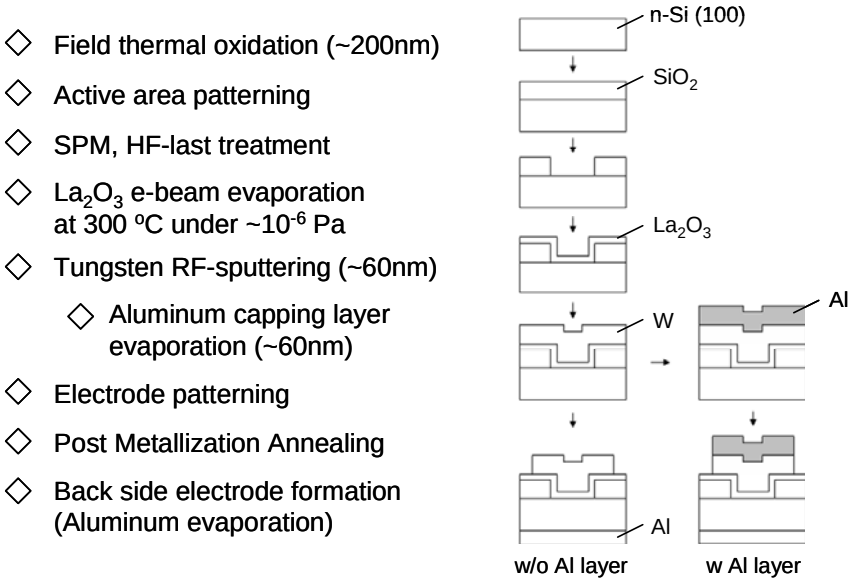

Figure 1 Process flow of Tungsten gate La_2O_3 MOS-Capacitors using Al capping layer.

Results and Discussions

W/La_2O_3 MOS Capacitor with EOT = 0.5 nm

Moisture absorption due to hygroscopic properties of La_2O_3 lowers the dielectric constant, which is attributed to formation of $La(OH)_3$ having lower permittivity (6). Figure 2 shows *C-V* and *J-V* characteristics of a sample before annealing in which W was coated *in situ* on the La_2O_3 films with thickness of ~ 3 nm. The gate voltage was swept from inversion to accumulation to get forward *C-V* and from accumulation to inversion to get reverse *C-V*. The large capacitance density with low leakage current (1.2 x 10^{-2} A/cm^2 at 1 V) was achieved. The EOT determined by CVC fitting with quantum effect correction revealed to be 0.50 nm. However, the large hysteresis of ~ 100 mV in the *C-V* curve is also observed due to the oxide traps close to the interface, which can communicate with the Si substrate (7). The "shoulder" in the 1 kHz to 1 MHz range (see the inset in Figure 2), appeared in the depletion region near the flat band voltage, which strongly suggests high D_{it}, particularly, silicon dangling bonds at the interface.

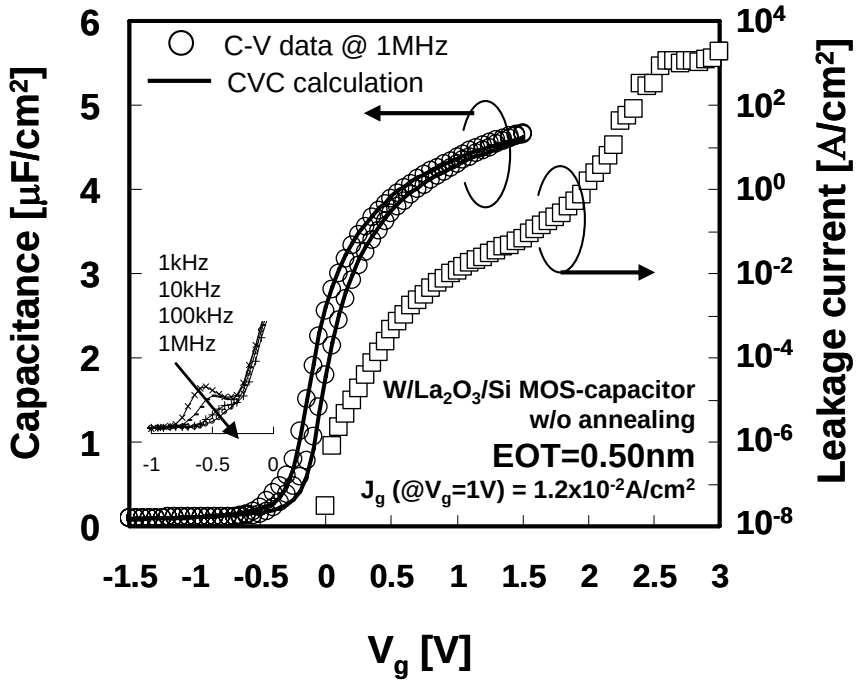

Figure 2. *C-V* and *J-V* characteristics of W/La_2O_3/n-Si capacitor without annealing. EOT was evaluated to be 0.50 nm. The leakage current was 1.2 x 10^{-2} A/cm^2 at V_g = 1 V. The inset is expanded *C-V* curve in the 1 kHz to 1 MHz range around the flat band voltage.

For the directly deposited La2O3 capacitors, improvement of interfacial quality is a very significant issue. The values of Dit were extracted by the conductance method (8). Capacitance (Cm) and conductance (Gm) in parallel circuit mode were measured at frequencies ranging from 100 Hz to 1 MHz. The equivalent parallel conductance over angular frequency (GP/) can be expressed as

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad [1]$$

where C_{ox} is the capacitance of insulator at accumulation. G_P/ω versus frequency ($f = \omega/2\pi$) is plotted in Figure 3. The applied V_g has been converted to the band bending. An approximate expression giving the D_{it} in terms of the maximum conductance is

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{\max} \quad [2]$$

where q is the electronic charge. The inset in Figure 3 shows D_{it} of the sample with EOT of 0.50 nm as a function of the band bending. As a result, the large D_{it} over 10^{12} $cm^{-2}eV^{-1}$ is obtained, and it should be reduced in order to satisfy requirements of high performance MOSFETs.

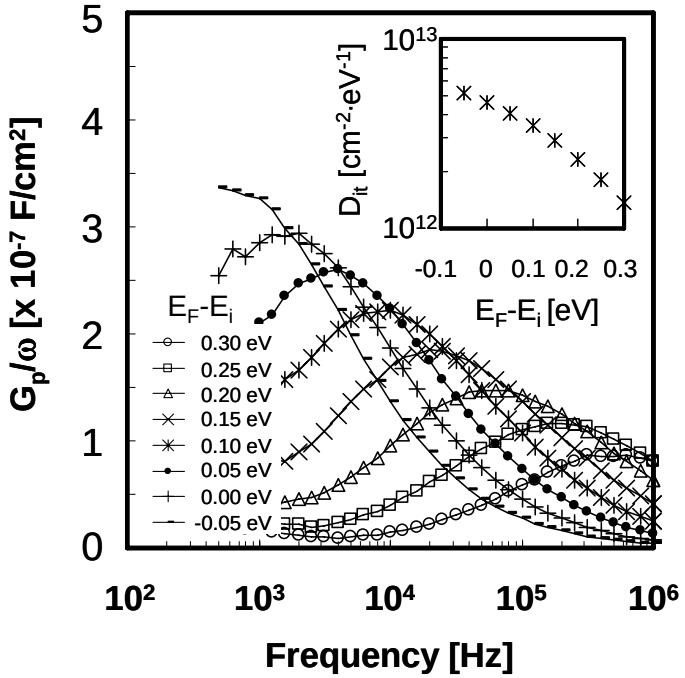

Figure 3. Equivalent parallel conductance over angular frequency versus frequency plots for a W/La_2O_3/n-Si capacitor. E_F-E_i represents the band bending at silicon surface in eV. The inset is D_{it} versus band bending at the surface of silicon.

Effect of Forming Gas Annealing with Al Capping Layer

Figure 4 (a) shows Dit at Etrap = Ei as a function of annealing temperature in W/La2O3/n-Si capacitors with and without Al capping layer. Usually, low-temperature PMA at 350- 450 oC in forming gas (FG) have been successfully used in MOS fabrication technologies to passivate silicon dangling bonds, and consequently, to reduce Dit at SiO2/Si interface (9). For the samples without Al capping layer, relatively high

values of Dit were observed entire temperature range, however, the decrease in Dit over 400 oC down to 2.1 x 1012 cm-2eV-1 at 500oC was observed. The tendency of decrease in Dit at higher temperature is similar to that observed in the HfO2 case, where high temperature over 500 oC is required to enhance hydrogen diffusion through high-k towards interface in order to passivate Si dangling bonds (10). Compared to annealing in N2 ambient, it is speculated that interface states are passivated by hydrogen. These results suggest that more injection of hydrogen is required for further improvement of the interface properties.

On the other hand, in the case of the sample with Al capping layer, D_{it} has been significantly decreased, either in N_2 or FG ambient, where minimum D_{it} of 3.3 x 10^{11} $cm^{-2}eV^{-1}$ was obtained under FG annealing at 350 ^{o}C. H. Shang *et al*. reported that the capped Al on W/SiO_2/Si system contributes to produce atomic hydrogen by reacting with water vapor and to introduce hydrogen atoms into tungsten gate (11). It is indicated that the produced hydrogen atoms can passivate the SiO_2/Si interface effectively in MOS structures. Similar effects are expected in our case. Figure 4 (b) shows dependence of D_{it} on annealing time at 300 ^{o}C and 500 ^{o}C in N_2 ambient. In the case of 300 ^{o}C annealing, the D_{it} decreased with PMA time. On the contrary, the D_{it} increased with PMA time in the case of 500^{o}C annealing.

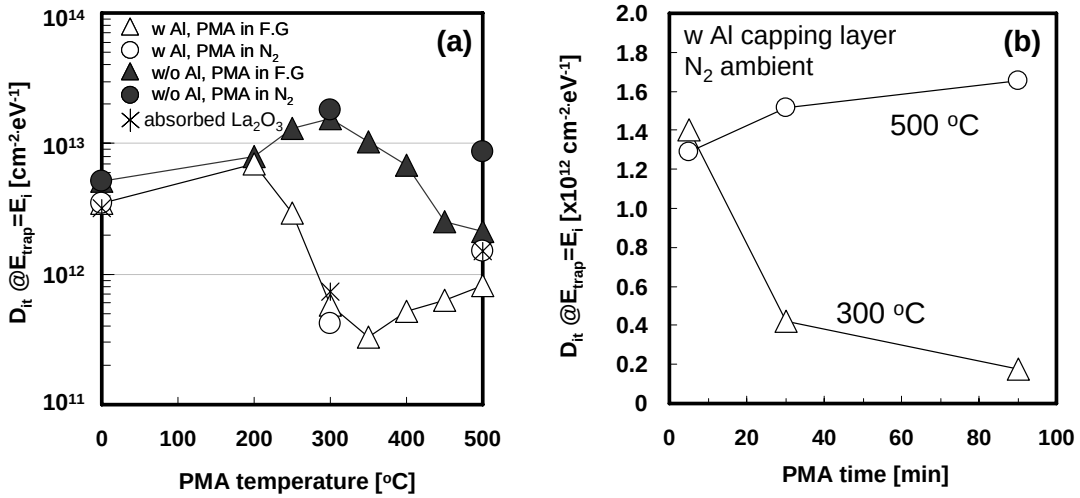

Figure 4. (a) D_{it} at $E_{trap} = E_i$ as a function of PMA temperature in FG and N_2 ambient for W/La_2O_3/n-Si capacitors with and without Al capping layer. For the moisture absorbed La_2O_3 MOS capacitors, PMA in N_2 was performed. (b) Dependence of D_{it} on annealing time at 300 ^{o}C and 500 ^{o}C in N_2 ambient.

Figure 5 shows the *C-V* curves with and without Al capping layer after PMA at 350 ^{o}C in FG ambient. It is obvious that the “shoulder”, which may be attributed to interface states due to Si dangling bonds, in the depletion region near the V_{FB} disappears by using capping with Al. However, the significant decrease in capacitance was observed in the case of use of the Al capping. Figure 6 shows EOT change as a function of PMA temperature in either FG or N_2 ambient for W/La_2O_3/n-Si capacitors with and without Al capping layer. It is clear that the EOT increment on the sample with Al capping layer is quite different from that without Al capping layer. The largest difference in EOT is observed around 300 ^{o}C at which a minimum D_{it} is obtained.

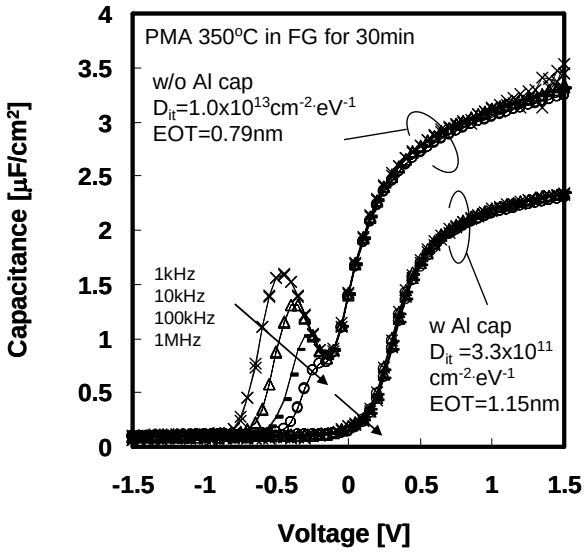

Figure 5. *C-V* curves with and without Al capping layer after PMA at 350 °C in FG ambient

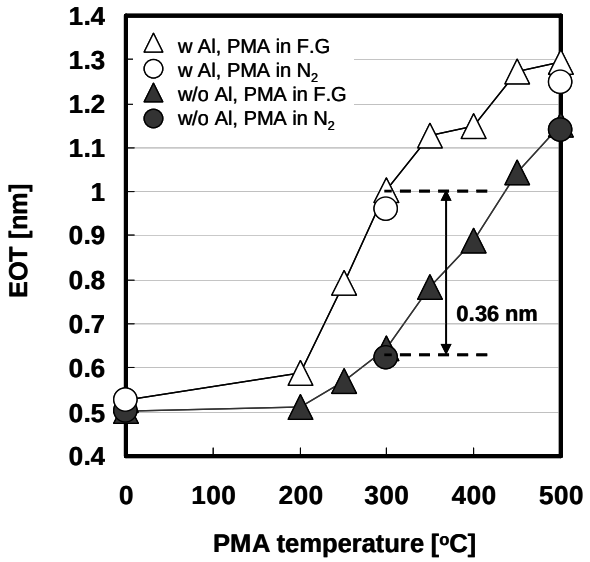

Figure 6. EOT as a function of PMA temperature in FG and N_2 ambient for W/La_2O_3/n-Si capacitors with and without Al capping layer.

The decrease in capacitance can be explained by the following three possible mechanisms. Firstly, the Al diffuses into the W layer, which has columnar crystalline structure, by annealing, then eventually form an Al_2O_3 layer (*k*: 8.5∼10) at the W/La_2O_3 interface. The difference in EOT at 300 °C PMA in FG ambient is 0.36 nm as shown in Fig. 6. If the dielectric constant of Al_2O_3 is 8.5, EOT of 0.36 nm corresponds to physical thickness of 0.78 nm by Al_2O_3. Figure 7 shows a cross sectional TEM image of the sample with Al layer after PMA at 500 °C in FG ambient. Al_2O_3 layer can hardly observe from this image, therefore, the diffusion of Al to form Al_2O_3 is not be the origin of the capacitance decrease probably.

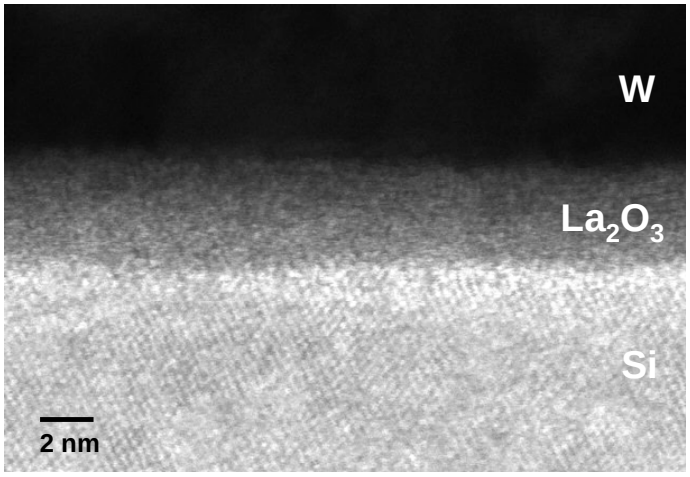

Figure 7. Cross sectional TEM image of the sample with Al layer after PMA at 500 ^{o}C in FG ambient.

Secondly, in addition to these hydrogen atoms, hydroxyl ions are also generated during decomposition of water by the Al capping layer. Considering that the D_{it} of the capacitors with Al capping is close to that of water absorbed La_2O_3 as shown in Figure 4 (a), OH^- can also penetrate into La_2O_3 film to form $La(OH)_3$, which can increase the EOT. Figure 8 shows the V_{FB} as a function of PMA temperature in N_2 or FG ambient. The V_{FB} is dependent on high-k/Si interfacial dipole or fixed charge. Here, the V_{FB} of $La(OH)_3$ capacitor differs from that of La_2O_3 capacitor as shown in Figure 8. In the case of the sample with Al capping layer, the V_{FB} approaches to that of moisture absorbed La_2O_3 around 300 ^{o}C PMA. In addition, negative shift in V_{FB} above 400 ^{o}C may be caused by thermal decomposition of $La(OH)_3$ (12). The existence of $La(OH)_3$, however, has not yet been confirmed. Finally, the further La_2O_3/Si interface reaction may be the other possible origin for the EOT increment by Al capping layer. This is because high-k/Si interface reaction is strongly dependent on the gate electrode structure, material and fabrication conditions, especially residual oxygen in gate metal.

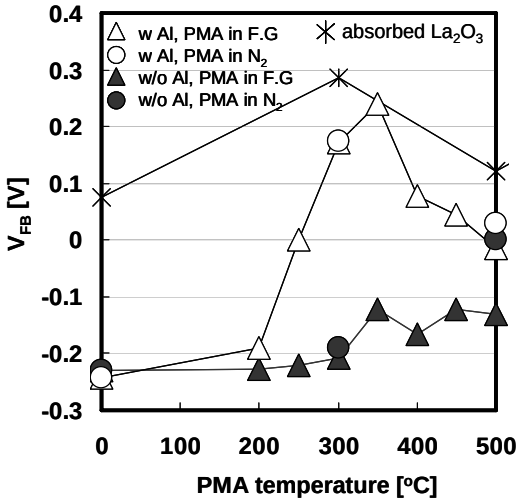

Figure 8. V_{FB} as a function of PMA temperature in N_2 or FG ambient for W/La_2O_3/n-Si capacitors with and without Al capping layer. For the moisture absorbed La_2O_3 MOS capacitor, PMA in N_2 is performed as references.

Conclusion

In this report, we demonstrated that EOT of 0.5 nm is achievable with W/La_2O_3/Si MOS structure. However, the large D_{it} over 10^{12} cm^{-2} eV^{-1} is observed. The effect of Al capping layer on W/La_2O_3/Si system have been investigated in order to improve interfacial properties. The Al capping layer can decrease D_{it}. However, serious increase in EOT was observed. This may be induced by the formation of $La(OH)_3$ or the difference of La_2O_3/Si interface reaction between the cases of with and without the Al capping layer. Further study is necessary to solve this problem.

Acknowledgments

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