Control of Flat Band Voltage by Partial Incorporation of La$_2$O$_3$ or Sc$_2$O$_3$ into HfO$_2$ in Metal/HfO$_2$/SiO$_2$/Si MOS Capacitors

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Abstract

High-k/SiO$_2$ interfacial properties are most critical factors determining the high-k gate MOSFET characteristics. We fabricated MOS capacitors of metal/HfO$_2$/SiO$_2$/Si structures in which were contained in the HfO$_2$ layer. Flat-band voltage ($V_{FB}$) shifts were measured by changing composition in metal/HfO$_2$/(HfO$_2$)$_{1-x}$(La$_2$O$_3$)$_x$/SiO$_2$/Si and metal/HfO$_2$/(HfO$_2$)$_{1-x}$(Sc$_2$O$_3$)$_x$/SiO$_2$/Si structures. It was found that $V_{FB}$ shift arises mainly from high-k/SiO$_2$ interface rather than metal/high-k interface. $V_{FB}$ could be effectively controlled by incorporating La$_2$O$_3$ or Sc$_2$O$_3$ near the high-k/SiO$_2$ interface.

Introduction

Combination of metal and high-k dielectrics is necessary in order to achieve smaller EOT for eliminating the poly-Si gate depletion effect without excess leakage current. HfO$_2$ based materials have been the promising candidates for next generation gate dielectric thanks to its high temperature endurance and relatively high permittivity. One of the issues of HfO$_2$ based oxides is the difficulty in reducing the threshold voltage ($V_{th}$) as relatively high $V_{th}$ were obtained with HfO$_2$ based oxides whatever the electrode material is. On the other hand, it has been reported that La$_2$O$_3$ and Sc$_2$O$_3$ produce negative shift in $V_{FB}$ with respect to HfO$_2$ reference $^{[1]}$. However, the detailed mechanism is not clarified yet. In this paper, first we extract the effective work function (EWF) of tungsten gate metal on high-k dielectrics, and then investigated the effect of La$_2$O$_3$ or Sc$_2$O$_3$ incorporation into a HfO$_2$ layer in a metal/HfO$_2$/SiO$_2$/Si MOS capacitor.

Experimental

Si(100) substrates with 200 nm-thick field SiO$_2$ in which diode holes were opened (1-10 ohm-cm) were cleaned in a mixed solution of H$_2$SO$_4$ and H$_2$O$_2$, followed by dipping in diluted HF. The substrates were then thermally oxidized to grow 3.5-nm-thick SiO$_2$ film. High-k dielectrics were deposited on these substrates by e-beam evaporation with O$_2$ partial pressure of 1x10$^{-4}$ Pa. Tungsten (W) gate electrode was in-situ deposited by RF sputtering. The W film was lithographically patterned and etched by reactive ion etching (RIE) using SF$_6$ chemistry to form gate electrodes for MOS capacitors. Annealing in forming gas (3 %-H$_2$+97 %-N$_2$) was performed at 420 °C for 30 min. Finally, aluminum (Al) was thermally evaporated on backside of the wafers for bottom electrode. Capacitance-voltage (C-V) characteristics of the fabricated MOS capacitors were measured at 100 kHz using Agilent 4284A precision LCR meter, from which $V_{FB}$ and EOT were calculated using NCSU CVC program.
The dielectrics studied here are La$_2$O$_3$, HfO$_2$ and Sc$_2$O$_3$. To evaluate the main reason of $V_{FB}$ shift, laminated dielectric stacks of HfO$_2$/La$_2$O$_3$ were fabricated. Moreover, mixed dielectrics of HfO$_2$-La$_2$O$_3$ and HfO$_2$-Sc$_2$O$_3$ with HfO$_2$ atop were also fabricated by co-evaporation of the two oxides.

Results and Discussions

Effective Work Function (EWF) Extraction

A schematic model of the charge locations in a metal/SiO$_2$/Si structure and metal/high-k/SiO$_2$/Si structure are illustrated in Fig.1. As the thickness of the dielectric layer is small, the bulk charges of each oxide can be neglected. Indeed, the results shown in Fig. 2 revealed a linear relationship between $V_{FB}$ and the EOT, thus, it is reasonable to assume low charge concentration inside the SiO$_2$ and the high-k layer. Under the assumption, the effective work function (EWF) of metal on a SiO$_2$ can be derived from the relation of $V_{FB}$ and EOT using the following equation,

$$V_{FB} = -\left(\frac{Q_{SiO2/Si}}{\varepsilon_0\varepsilon_{ox}}\right) \cdot EOT + \frac{\varphi_{ms} + q\Delta_{SiO2/Metal}}{q} + \varphi_{ms}$$

where $Q_{SiO2/Si}$ is the fixed charge at the SiO$_2$/Si interface, $\varphi_{ms}$ is the work function difference of gate metal and semiconductor and $\varphi_{SiO2/Metal}$ is the dipole at metal/oxide interface. The EWF of gate metal, defined as $\frac{\varphi_{ms} + q\Delta_{SiO2/Metal}}{q}$, can be extracted by the y-intercept from the $V_{FB}$-EOT slope. When interfacial SiO$_2$ layer (IL) is inserted between high-k dielectric and Si substrate, the Eq.(1) can be modified using total EOT as shown in eq.(2),

$$V_{FB} = -\left(\frac{Q_{high-k/IL} + Q_{SiO2/Si}}{\varepsilon_0\varepsilon_{ox}}\right) \cdot EOT + \frac{Q_{SiO2/high-k}}{\varepsilon_0\varepsilon_{ox}} \cdot EOT_{IL} + \frac{\varphi_{ms} + q\Delta_{Metal/high-k}}{q} + \varphi_{ms}$$

Here, $Q_{high-k/IL}$, $\Delta_{high-k/Metal}$ and $EOT_{IL}$ are the fixed charge at high-k/IL interface, the dipole at high-k/metal interface and the EOT of IL, respectively. Eventually, the EWF of metal on high-k/SiO$_2$ stack can be expressed as follows,

$$EWF_{(high-k)} = EWF_{(SiO2)} + (q\Delta_{high-k/Metal} - q\Delta_{SiO2/Metal})$$

Figure 2 shows the typical C-V curves of La$_2$O$_3$/IL, HfO$_2$/IL and Sc$_2$O$_3$/IL capacitors. The difference between $V_{FB}$(HfO$_2$/IL) and $V_{FB}$(La$_2$O$_3$/IL) is about 0.48 V, whereas difference between $V_{FB}$(HfO$_2$/SiO$_2$) and $V_{FB}$(Sc$_2$O$_3$/SiO$_2$) is 0.15 V. Figure 3 shows the result of $V_{FB}$ of La$_2$O$_3$/IL, HfO$_2$/IL and Sc$_2$O$_3$/IL capacitors with different high-k thicknesses. Capacitors with SiO$_2$ with different thickness are also shown to derive $Q_{SiO2/Si}$. Using the equations (1)-(3), EWF of W on SiO$_2$, HfO$_2$, La$_2$O$_3$ and Sc$_2$O$_3$ can be calculated and summarized in Table.1. The smallest EWF of 4.46 eV was obtained with La$_2$O$_3$, whereas relatively large value was obtained with HfO$_2$. These results suggest high
$V_{th}$ in nMOSFET when HfO$_2$ is used as gate dielectrics. In the next subsection, the origin of $V_{FB}$ is examined in detail.

Fig.1 Schematic model of the charge locations used in the extraction of fixed charge.

Fig.2 C-V characteristics of MOS capacitors with single layered high-k dielectric (HfO$_2$, La$_2$O$_3$, Sc$_2$O$_3$)
Fig. 3 $V_{FB}$-EOT plot obtained from the analysis of $C$-$V$ curves.

Table 1. Effective work function of W gate electrode on various gate dielectric (SiO$_2$, La$_2$O$_3$, HfO$_2$, La$_2$O$_3$)

<table>
<thead>
<tr>
<th>Gate Oxide</th>
<th>SiO$_2$</th>
<th>La$_2$O$_3$</th>
<th>HfO$_2$</th>
<th>Sc$_2$O$_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>EWF (eV)</td>
<td>4.59</td>
<td>4.46</td>
<td>4.80</td>
<td>4.75</td>
</tr>
</tbody>
</table>
In order to investigate the $V_{FB}$ shift on stacked dielectrics, double layer stacked films were fabricated, as shown in Fig. 4. Capacitors with single layer of HfO$_2$ or La$_2$O$_3$ are also fabricated as references. The total thickness of the high-k film was designed to have 5 nm. Figure 5 shows the $C-V$ characteristics of W/HfO$_2$/La$_2$O$_3$/IL stacked MOS capacitors. The $C-V$ curves of the stacked capacitors showed negative $V_{FB}$, which are close to that of the single La$_2$O$_3$ layer reference. From these results, it is clear that the $V_{FB}$ shift is determined by the high-k material in contact to SiO$_2$ IL. It is known that positive charges or dipole at the interface could attribute to negative shift in $V_{FB}$, however, either or both effects on these results are not clarified yet. Nonetheless, it is expected that by changing the composition of high-k at the high-k/IL interface might allow precise $V_{FB}$ control.

Fig.4 Schematic illustration of fabricated MOS capacitors with stack of HfO$_2$ and La$_2$O$_3$. Capacitors with single HfO$_2$ or La$_2$O$_3$ layer are fabricated as references.
In this subsection, the $V_{FB}$ shift depending on the amount of La$_2$O$_3$ at the high-k/SiO$_2$ interface is investigated. From the result that even 1 nm of La$_2$O$_3$ at high-k/SiO$_2$ interface can negatively shift the $V_{FB}$, the amount of the incorporated La$_2$O$_3$ to realize controllability of $V_{FB}$ should be less than 1 nm. To obtain precise controllability of amount of La$_2$O$_3$ during the deposition process, we employed co-evaporation of HfO$_2$ and La$_2$O$_3$ with different concentration, those are 20, 50 and 80%. The thickness of the mixed high-k layers was set to 1 nm. HfO$_2$ with 5 nm thickness was capped on the mixed high-k. The schematic illustrations of the fabricated capacitors are shown in Fig. 6. The C-V characteristics of the mixed high-k stack capacitors together with those of the references with La$_2$O$_3$ and HfO$_2$ capacitors are shown in Fig. 7. With the La$_2$O$_3$ concentration of 80%, the $V_{FB}$ of C-V curves showed almost identical value for the La$_2$O$_3$ reference, where that of 20% showed in between of those of HfO$_2$ and La$_2$O$_3$ references. With 50% of La$_2$O$_3$ incorporation, the $V_{FB}$ was slightly positive to the La$_2$O$_3$ reference. Also from these results, it is noted that the EWF of the gate metal is mainly dominated by the high-k/IL interface, not at the Metal/high-k interface. By plotting the $V_{FB}$ on La$_2$O$_3$ concentration, as is shown in Fig. 8, we obtain a monotonic relation between concentration and $V_{FB}$. It can be concluded that $V_{FB}$ can be effectively controlled by changing the concentration of the mixed high-k at the high-k/IL interface.
Fig. 6 Schematic illustration of fabricated MOS capacitor incorporating La$_2$O$_3$ into HfO$_2$/SiO$_2$ interface

Fig. 7 C-V curves of W/HfO$_2$/(HfO$_2$)$_{1-x}$(La$_2$O$_3$)$_x$/SiO$_2$ structure
The same experiments were carried out using Sc$_2$O$_3$ and HfO$_2$. In this case, the thickness of Sc$_2$O$_3$-HfO$_2$ mixed high-k and HfO$_2$ capping layer were set to 5 nm and 0.5 nm, respectively. The structure is depicted in Fig. 9. The concentrations of Sc$_2$O$_3$ were set to 33, 50 and 67%. Figure 10 shows the C-V curves of the Sc$_2$O$_3$ incorporated HfO$_2$ capacitors. Also Sc$_2$O$_3$ and HfO$_2$ references are shown. Negative shifts of $V_{FB}$ with increase in the concentration of Sc$_2$O$_3$ were obtained. The relation between the concentration and $V_{FB}$ is shown in Fig. 11. From this figure, the $V_{FB}$ control range of 0.15 V was achieved using Sc$_2$O$_3$ incorporation into HfO$_2$. This value is smaller than that of La$_2$O$_3$, which can be expected from Sc$_2$O$_3$ single layer capacitor. Therefore, Sc$_2$O$_3$ and La$_2$O$_3$ incorporation technique is useful as fine and coarse tuning of $V_{FB}$, respectively.

$V_{FB}$ Controlled by Sc$_2$O$_3$ Incorporation into HfO$_2$

![Fig.8 $V_{FB}$ shift depending on concentration of incorporation La at HfO$_2$/SiO$_2$](image-url)
Fig. 9 Schematic illustration of fabricated MOS capacitors incorporating Sc$_2$O$_3$ into HfO$_2$/SiO$_2$ interface.

Fig. 10 C-V curves of W/HfO$_2$/Hf$_x$Sc$_{1-x}$O/SiO$_2$ structures.
The $V_{FB}$ shift was found to be dominated by the high-k/SiO$_2$ interface property. The most considerable causation is an existence of the dipole at the high-k/SiO$_2$ interface. We observed the $V_{FB}$ shift for the MOS capacitors using (HfO$_2$)$_{1-x}$(La$_2$O$_3$)$_x$/SiO$_2$ or (HfO$_2$)$_{1-x}$(Sc$_2$O$_3$)$_x$/SiO$_2$ as gate dielectrics. The $V_{FB}$ is dependent on concentration of La$_2$O$_3$ or Sc$_2$O$_3$, and the large concentration results in large negative $V_{FB}$ shift up to the $V_{FB}$ obtained for the capacitors using La$_2$O$_3$/SiO$_2$ or Sc$_2$O$_3$/SiO$_2$. Coarse and fine tuning of $V_{FB}$ for HfO$_2$ gate dielectrics were successfully observed by La$_2$O$_3$ and Sc$_2$O$_3$ incorporation, respectively. $V_{FB}$ of MOS capacitors using high-k dielectrics could be controlled by the incorporation of La$_2$O$_3$ or Sc$_2$O$_3$ at the HfO$_2$/SiO$_2$ interface.

Fig.11 $V_{FB}$ shift depending on incorporation of Sc at HfO$_2$/SiO$_2$ interface
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References


