ポストHfO2技術

希土類酸化膜

PVDデポ

High-k Gate Dielectric Candidates Choice of high-k

k value less than 50 is desirable for suppression of short channel effects

Material	k	HfAl _x O _y	10-15
NO stack	5-6	HfSi _x O _y N _z	10-15
Al_2O_3	8-9	ZrO_2 , HfO_2	20-30
HfSi _x O _y	10-15	Lanthanide Oxides	15-30

Other options?



R. Hauser, IEDM Short Course, 1999

Band offsets for High-k dielectrics on Si



* ^CEstimates.

参考文献: J.Robertson Journal of Non-Crystalline Solids 303(2002) P98

Experimental data by XPS by Prof. T. Hattori



 $\sqrt{\phi_{B}} * k$: Figure of Merit of High-k

Insulating Films on Semiconductors Barcelona June 18-20, 2003





Our Molecular Beam Deposition System



Cross sectional TEM images for Al/La₂O₃/n-Si. 400°C depo., 400°C RTA in N₂.



Physical thickness = 2 nm

EOT = 0.6 nm

T_{ox} Electrical Equivalent vs. Current Density



From IEDM 2000, IEDM 2001, SSDM 2001 and VLSI Symp. 2001(Advanced Program)

Annealing (5min)		EOT [nm]	Vfb [V]	∆Vfb [V]	Relative Dielectri c Constant	Leakag e [A] @1V
without		1.760	0.806	0.123	17.0	1.06e-2
0 ₂	200°C	1.762	0.823	0.165	15.6	3.09e-6
	300°C	1.617	0.870	0.257	16.9	9.51e-7
	400°C	3.103	0.391	-0.700	9.62	1.37e-5
N ₂	200°C	1.106	0.784	0.083	27.0	3.04e-7
	300°C	1.443	0.785	0.081	26.1	7.27e-6
	400°C	1.280	0.808	0.123	23.3	2.77e-6

$$V_{fb,fitted} = \Delta W_{func} + \Delta V_{fb,Calc} = W_{gate} - W_{silicon} + V_{fb,Calc}$$

Preliminary results Der Vfb Dry N2 annealing Bei

Densification: good Vfb shift: problem Being solved by PM anneal



ID - VD Characteristics ($Lg = 2.5 \ \mu m$)

Chemical Oxide, Deposition Temp. = $250^{\circ}C$, Lg = $2.5 \mu m$, W = $27 \mu m$, EOT = 3.0 nm



Deposition Temp. = 250° C, Tphy = 10 nm, Annealed in O₂ 400°C 5min



Electrical Characteristics – Mobility μ_{eff}



High effective mobility of nearly the same to the universal curve was obtained with EOT = 3nm La_2O_3 gate dielectrics. Flicker noise at $V_{ds}=100mV$



Results and Discussion (6) LF Noise – Comparation with SiO₂



The normalized noise spectrum of n-type MISFET's with La_2O_3 gate dielectrics is about one order in magnitude higher than that of SiO₂ obtained from thermal oxidation.

Absorption of moisture and CO₂

The oxides become hydroxide and carbonate in H_2O and CO_2 ambient.



Experimental apparatus





*PMMA : $CH_2C(CH)_3COOCH_3$



Absorption test in case of acryl apparatus after the AI electrode formation for Pr_2O_3 .



研究目的



Ref. S.Ohmi, et al., *J. Electrochem. Soc.*, 150, F134(2003) H.Nohira et al., *J. Appl. Surf. Sci.*, 216(2003)



La₂O₃で界面層成長と微結晶化を抑える Lu₂O₃で膜全体silicateを抑え、耐湿性を向上 誘電率を保ちつつリーク電流を抑制

積層構造(Lu₂O₃/La₂O₃/n-Tr)の作製

nMIS 250°C堆積, annealed at 400°C, Al電極を使用



<u>Lu₂O₃の耐湿性により、電気特性が改善した</u>

Conduction Modes and Expressions

	Mode	Expression	
Bulk-Free	Schottky* DT** F-N Ohmic	(1) $\ln(J) \propto E^{1/2}$ (2) $\ln(J) \propto E$ (3) $\ln(J/E^2) \propto 1/E$ (4) $J \propto E$	$\ln(J/T^{2}) \propto -1/T$ $\int J \propto T^{2} (weak)$ $\ln(J) \propto -1/T$
Bulk-Limited	Poole P-F SCLC***	(5) $\ln(J) \alpha E$ (6) $\ln(J/E) \propto E^{1/2}$ (7) $\ln(J/E) \propto E$ (8) $J \propto E^2$	$\left \ln(J) \propto -1/T \right $

*Thermionic Current, **Direct Tunneling Current,

***Space-Charge-Limited Current : single trap level for shallow (7) and deep (8) distributi

Al Electrode Case – Leakage Current



2003.11.30.修正

超高真空アニール後のLa₂O₃薄膜中のトラップ準位

